



DEVICE RESEARCH CONFERENCE

CONFERENCE DIGEST

JUNE 25-27, 2001

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Location McKenna Hall
Welcoming Reception 6:30PM–8:30PM
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MONDAY AM, JUNE 25TH, 2001

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- I-3 “Low-Noise, High-Speed Avalanche Photodiodes” *Joe C. Campbell*¹; ¹The University of Texas at Austin, Microelectronics Research Center, 10100 Burnet Road, Mail Code R9950, Austin, TX 78712 USA
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- VI.A.-2 “Thermal Conductivity in Semiconductor Thin Films and Nanowires”** *Jie Zou¹*; Alexander A. Balandin¹; ¹University of California at Riverside, Dept. of Electl. Eng., Riverside, CA 92521 USA
- VI.A.-3 “Quantum Mechanical Calculation of QCA Molecule Properties”** *Christopher J. Russo¹*; *Craig S. Lent¹*; ¹University of Notre Dame, Electl. Eng., 275 Fitzpatrick, Notre Dame, IN 46556 USA
- VI.A.-4 “Nano-Transistor Modeling: Two Dimensional Green’s Function Method”** *A. Svizhenko¹*; M. P. Anantram¹; T. R. Govindan¹; B. Biegel¹; ¹NASA, Ames Rsrch. Ctr., MS T27A-1, Moffett Field, CA 94035-1000 USA
- VI.A.-5 “A Coupled Schrödinger/Monte Carlo Technique for Quantum-Corrected Device Simulation”** *Brian Winstead¹*; Umberto Ravaioli¹; ¹University of Illinois at Urbana–Champaign, Beckman Inst., Urbana, IL 61801 USA
- VI.A.-6 “Quantitative Prediction of Threshold Voltage Fluctuations in Sub-100 nm MOSFETs by a New Dopant Model”** *Hiroiyuki Yamamoto¹*; Yos-himitsu Okada¹; Nobuyuki Sano¹; ¹University of Tsukuba, Inst. of Appl. Phys., 1-1-1 Tennoudai, Tsukuba, Ibaraki, 305-8573 Japan

- VLB-1 “High Gamma Coatings for Plasma Display Panels: A Comparison”** *P. K. Bachmann¹*; V. Van Elsbergen¹; C. McGrath¹; ¹Phillips Research Laboratories, Weissshausstrasse 2, D-52066 Aachen, Germany
- VLB-2 “Rare-Earth Doped GaN Electroluminescent Devices for Robust Flat Panel Displays”** *J. Heikenfeld¹*; A.J. Steckl¹; ¹University of Cincinnati, Nanoelectronics Lab, Cincinnati, OH 45221-0030 USA
- VLB-3 “Novel Three-Color Polymer Light-Emitting Devices for Passive-Matrix Flat Panel Displays”** *Ke Long¹*; Min-Hao Lu¹; Florian Pschenitzka¹; J. C. Sturm¹; ¹Princeton University, Department of Electrical Engineering, Center for Photonics and Optoelectronic Materials (POEM), Princeton, NJ 08544 USA
- VLB-4 “Flexible Liquid Crystal Displays Driven by Organic Thin Film Transistors on Polymeric Substrates:** *C. D. Sheraw¹*; L. Zhou¹; J. R. Huang¹; L. Jia¹; J. A. Nichols¹; C. C. Kuo¹; D. J. Gundlach¹; T. N. Jackson¹; M. G. Kane²; I. G. Hill²; M. S. Hammond²; J. Campi²; B. K. Greening²; J. Franc³; J. West³; ¹The Pennsylvania State University, Center for Thin Film Devices, University Park, PA 16802 USA; ²Sarnoff Corporation, Solid State Display Laboratory, Princeton, NJ 08543 USA; ³Kent State University, Liquid Crystal Institute, Kent, OH 44242 USA

SESSION VII.A. TFTs

183–196

- VIIA-1 “Organic-Inorganic Electronic Devices Based on Hybrid Perovskites”** *D. B. Mitzi¹*; C. D. Dimitrakopoulos¹; L. L. Kosbar¹; ¹IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA
- VIIA-2 “CMOS Polysilicon Circuits on Flexible Steel Substrates”** *Ming Wu¹*; Sigurd Wagner¹; ¹Princeton University, Department of Electrical Engineering, Princeton, NJ 08544 USA
- VIIA-3 “High-Performance Thin-Film Transistor Fabricated on Poly-Si Films Prepared by Metal Imprint Technology”** *Kenji Makihiro¹*; Masahito Yoshii¹; Tanemasa Asano¹; ¹Kyushu Institute of Technology, Center for Microelectronic Systems, 680-4 Kawazu, Iizuka, Fukuoka 820-8502, Japan
- VIIA-4 “Excimer Laser Annealed, Poly-Si Thin Film Transistors for Flat Panel Imager Application”** *J. P. Lu¹*; K. Van Schuylenbergh¹; J. Ho¹; Y. Wang¹; P. Nylen¹; J. B. Boyce¹; R. A. Street¹; ¹Xerox Palo Alto Research Center, 3333 Coyote Hill Road, Palo Alto, CA 94304 USA
- VIIA-5 “Amorphous Si TFTs on Plastically-Deformed Substrates with 3-D Shapes”** *P. I. Hsu¹*; H. Gleskova¹; Z. Suo¹; S. Wagner¹; J. C. Sturm¹; ¹Princeton University, Center for Photonics and Optoelectronic Materials (POEM), Princeton, NJ 08544 USA
- VIIA-6 “Gate Control in Ultra-Short Channel Double-Gate MOSFETs Accounting for 2D and Quantum Confinement Effects”** *M. Mouis²*; F.-N. Genin¹; A. Poncet¹; ¹Laboratoire de Physique de la Matière, UMR-CNRS n° 5511, INSA-Lyon 20, Avenue Albert Einstein, F-69621 Villeurbanne, France; ²CEA-Grenoble, LETI/DTS/CPMA, 17 rue des Martyrs, 38054 Grenoble, Cedex 9 France

SESSION VII.B. WIDE BANDGAP SEMICONDUCTORS

197–212

- VII.B-1 “K-Band GaN Power HFET’s with 6.6 W/mm CW Saturated Output Power Density and 35 % Power Added Efficiency at 20 GHz”** *Miro Micovic¹*; Jeong S. Moon¹; Ara Kurdoghlian¹; Paul Hashimoto¹; Danny Wong¹; Loren McCray¹; Tahir Hussain¹; Paul Janke¹; ¹HRL Laboratories LLC, 3011 Malibu Canyon Road, Malibu, CA 90265 USA
- VII.B-2 “Linearity of High Al-Content AlGaIn/GaN HEMTs”** *T. Jenkins¹*; L. Kehias¹; P. Parikh²; Y.-F. Wu²; P. Chavarkar²; M. Moore²; U. Mishra²; ¹Air Force Research laboratory, 2241 Avionics Circle, Wright-Patterson AFB, OH 45433 USA; ¹Cree Lighting Company, 340 Storke Road, Goleta, CA 93117 USA
- VII.B-3 “Demonstration of Push-Pull Operation of AlGaIn/GaN HEMTs on SiC”** *Jong-Wook Lee¹*; Sungjae Lee¹; Keven J. Webb¹; ¹Purdue University, School of Electrical and Computer Engineering, West Lafayette, IN 47907 USA
- VII.B-5 “An X-Band Silicon Carbide IMPATT Diode”** *Luo Yuan¹*; Michael R. Melloch¹; James A. Cooper, Jr.¹; Kevin J. Webb¹; ¹Purdue University, School of Electrical and Computer Engineering, West Lafayette, IN 47907 USA
- VII.B-6 “The Effect of Emitter Implant and Anneal on High-Voltage 4H-SiC BJTs”** *Yi Tang¹*; Jeffrey B. Fedison¹; T. Paul Chow¹; ¹Rensselaer Polytechnic Institute, Center for Integrated Electronics and Electronic Manufacturing, Troy, NY 12180 USA
- VII.B-7 “Diamond Surface Channel FET with $f_{\max}$ Above 30 GHz”** *A. Aleksov¹*; A. Denisenko¹; U. Spitzberg¹; E. Kohn¹; ¹University of Ulm, Dept. of Electron Devices and Circuits, Albert-Einstein-Allee 45, D-89081 Ulm, Germany

Plenary Session

MONDAY AM, JUNE 25TH, 2001

Session Organizer: Sanjay Banerjee, The University of Texas at Austin

Session Chair: Mark Rodwell, University of California at Santa Barbara

8:30 AM, Welcoming Remarks

Plenary Speakers:

9:00 AM, I.1 Invited

SOI and Nanoscale MOSFETs: *Chenming Hu*¹; ¹University of California, Department of Electrical Engineering and Computer Sciences, Berkeley, CA 94720 USA

9:40 AM, I.2 Invited

Vertical Cavity Surface Emitting Laser - Exploratory, Emerging, or Disruptive?: *K. Iga*¹; ¹Tokyo Institute of Technology, 4259 Nagatsuta, Midoriku, Yokohama 226-8502 Japan

10:20 AM Break

10:45 AM, I.3 Invited

Low-Noise, High-Speed Avalanche Photodiodes: *Joe C. Campbell*¹; ¹The University of Texas at Austin, Microelectronics Research Center, 10100 Burnet Road, Mail Code R9950, Austin, TX 78712 USA

11:25 AM, I.4 Invited

Status, Prospects and Commercialization of SiC Power Devices: *Dietrich Stephani*¹; ¹SiCED Electronics Development GmbH & Co. KG, Paul-Gossen-Str. 100, D91052 Erlangen, Germany

Chenming Hu
 Dept. of Electrical Engineering and Computer Sciences
 University of California, Berkeley, CA 94720

Introduction

Because SOI offers moderate speed or power improvements over bulk technology, IBM, AMD and other semiconductor companies are committed to produce products using SOI technology. One speed advantage stems from floating the body thereby eliminating the body effect in NAND, NOR, and pass gates. Furthermore, the floating body can take on a potential through DC and capacitive coupling to the drain, gate and source. The result is that V_t , and therefore speed and transistor leakage current depend on the history of the terminal voltages. If properly harnessed, this floating body effect can produce an additional performance gain. Fortunately, these effects can be accurately modeled for circuit design with BSIMPD[1], jointly developed by UC Berkeley and IBM, which uses the model for production.

An intriguing new role for SOI is to provide novel MOSFET structures whose gate lengths can be scaled to below 25nm, where bulk MOSFET scaling is very difficult.

The Simple Physics of MOSFET Scaling

MOSFET scaling limit may be explained by noting that the channel potential must be controlled by the gate rather than the drain. Therefore, C_g must be much larger than C_d in Fig. 1. Otherwise the drain, not the gate, will determine whether current can flow and the device will behave like a (nonlinear) resistor, not a transistor. As the channel length is reduced, C_d increases. To accommodate that, the oxide thickness must be reduced. 1.5 nm (5 layers of SiO_2) thin gate oxides are in use now. How much scaling is left? Fig. 1 shows that when the interface potential is well controlled by the gate through the ultra thin gate dielectric, the worst-case leakage path may be $\text{Leff}/2$ below the interface where the gate control is much weaker. This subsurface leakage makes MOSFET scaling much more difficult.

Ultra-thin-body (UTB) and Double-gate (DG) MOSFETs

The solution is to eliminate all the silicon material that is more than $L/4$ away from the interface as shown in Fig. 2. The UTB FET is basically an SOI MOSFET with a body thinner than a quarter of the channel length. In the DG FET, also, no silicon body material is farther than $\text{Leff}/4$ from both gates, i.e. the body is thinner than $\text{Leff}/2$. Both UTB and DG FETs depend on a thin body to facilitate gate-length scaling. To reduce the series resistance, the thin body should be thickened as shown in Fig.2, or silicided, in the S/D regions.

Fig. 3 shows a UTB FET with 30nm gate flanked by nitride/oxide spacers and raised S/D by selective Ge deposition[2]. Fig. 3 also shows

73mV/decade swing and very small V_t dependence on V_d .

Also demonstrated is a 20nm gate-length UTB FET with low-barrier silicide S/D[3]. The key technology is PtSi for PMOS and $\text{ErSi}_{1.7}$ for NMOS to achieve acceptably low contact resistances in the UTB structure.

UTB FETs have been successfully fabricated on bulk substrates[4]. Ultra thin body is formed by lateral solid-phase epitaxy starting with a thin film of amorphous Si. Starting with a-SiGe film, SiGe UTB PFET was fabricated and 70% increase in current compared with Si UTB PFET was achieved[5].

FinFET—a Relatively Simple Double-gate FET

One additional advantage of DG FET (see Fig.2) is the presence of twice the inversion charge and therefore twice the I_d per μm of W . Fig.4 shows the only successful demonstration of this potential with a record 860 $\mu\text{A}/\mu\text{m}$ in a PFET[6]. A 18nm gate length was also demonstrated. The device structure is schematically shown in Fig.4 [7]. The thin body is a vertical fin (hence the name FinFET) etched out of an SOI film. The gate straddle both sides of the fin—hence double gate. Mixed mode simulations shows that FinFET provides up to 3x higher speed than a well-tempered bulk FET due to better swing, higher mobility, and no bulk charge effect[7]. Simulation results in Fig. 5 shows that FinFET gate length can be scaled to below 10nm[8].

Summary

SOI may facilitate the fabrication of two attractive scalable MOSFET structures. Ultra-thin body FET has been demonstrated at 20nm gate length, using low-barrier silicide S/D, with selectively deposited Ge raised S/D, on bulk substrate, or with Si-Ge channel. FinFET is a simple double gate FET with excellent performance and can be scaled to below 10nm gate length—a candidate as the ultimate CMOS device. Adjusting the threshold voltage of a device with very thin body is challenging although several novel methods have been suggested[8].

Acknowledgement

Research was performed by faculty and students of UC Berkeley listed in the References. Research is partially supported by the DARPA AME Program, contract N66001-97-1-8910, SRC Task 850.01, AMD and MICRO.

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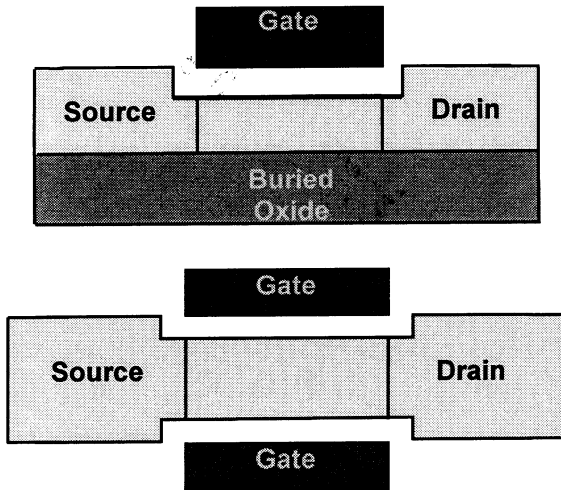


Fig. 2 Two scalable MOSFET structures. Top: Ultra-thin-bosy (UTB). Bottom: Double-gate.

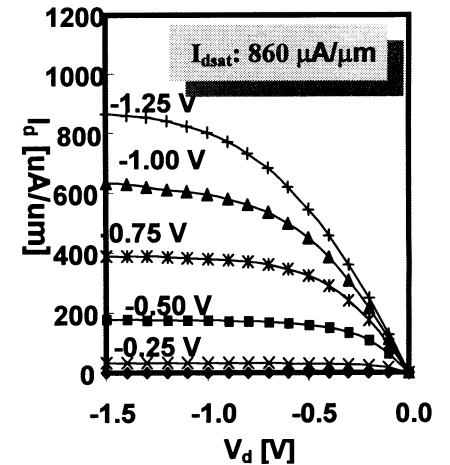
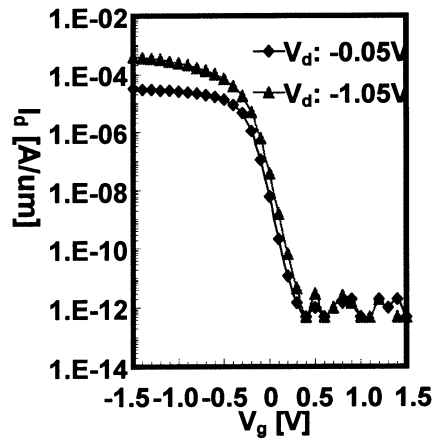
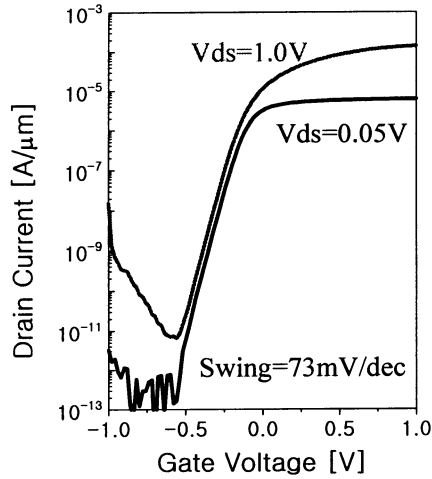


Fig.4 FinFET is a double gate MOSFET that achieved record current for PFET. Swing is 69 mV/decade. Also, 18nm gate-length FinFET was demonstrated [6].

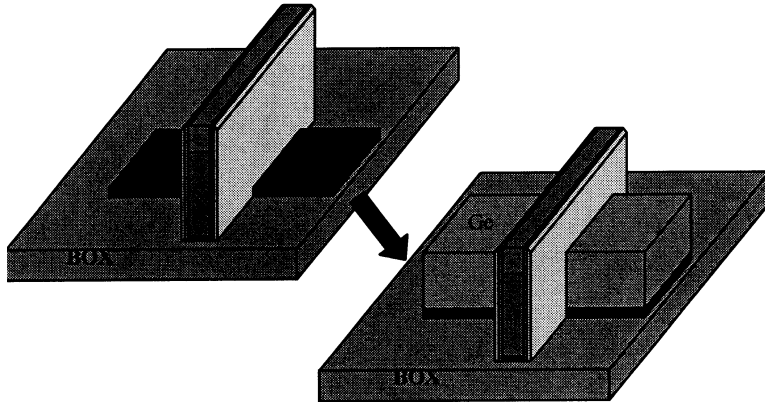


Fig.3 After 30nm gate is patterned over the 8nm ultra-thin body, Ge raised S/D is selectively deposited to reduce series resistance. $S = 73mV/decade$ [2]. 20nm-gate UTB FETs with PtSi and ErSi complimentary S/D [3], and using Si-Ge channel [5] were also reported.

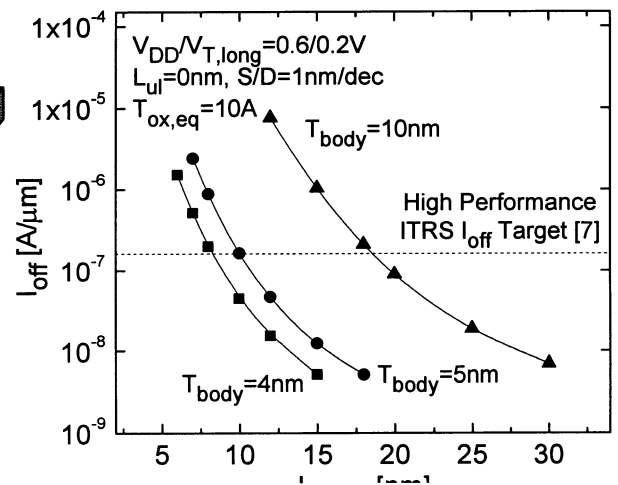


Fig. 5 Simulations show that FinFET can be scaled to below 10nm gate length and still meet ITRS leakage target[8]. Note the advantage of thin body thickness.

Vertical Cavity Surface Emitting Laser - Exploratory, Emerging, or Disruptive? -

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1. Introduction

The vertical cavity surface emitting laser (VCSEL) as shown in Fig. 1 [1]-[4] is a relatively new class of semiconductor laser which can be monolithically fabricated. It is now considered as one of important devices for Gigabit Ethernet, high speed LANs, computer links, optical interconnects, and so on. In this talk, we review the technical progress of devices ranging from infrared to ultraviolet spectra by featuring physics, materials, fabrication technology, performances such as threshold, output powers, polarizations, modulation, tunability, reliability, and so on. Then, we will discuss on some emerging applications[5].

The present author suggested the device of VCSEL in 1977[1][2]. The first device came out in 1979, where we used 1300nm wavelength GaInAsP/InP material for active region[3]. The first room temperature continuous wave (CW) device using GaAs material was demonstrated in 1988[4]. Since 1992, VCSELs based on GaAs have been extensively studied and some of 980, 850 and 780nm devices were commercialized into lightwave systems. Aiming at exploring applications, 1300-1550nm, red color GaInAlAs, and blue-ultraviolet GaN devices are now being studied[5].

2. Device Physics

The structure common to most of VCSELs consists of two parallel reflectors which sandwich a thin active layer. The reflectivity necessary to reach the lasing threshold should normally higher than 99.9 %. Together with the optical cavity formation, the scheme for injecting electrons and holes effectively into small volume of active region is necessary for current injection device. An AlAs oxidation is considered to be the most effective process to perform it.

The VCSEL structure may provide a number of advantages including ultra-low threshold operation due to its small cavity volume V_a . We may have some scaling laws describing the VCSEL performances. The threshold current I_{th} is given by the equation;

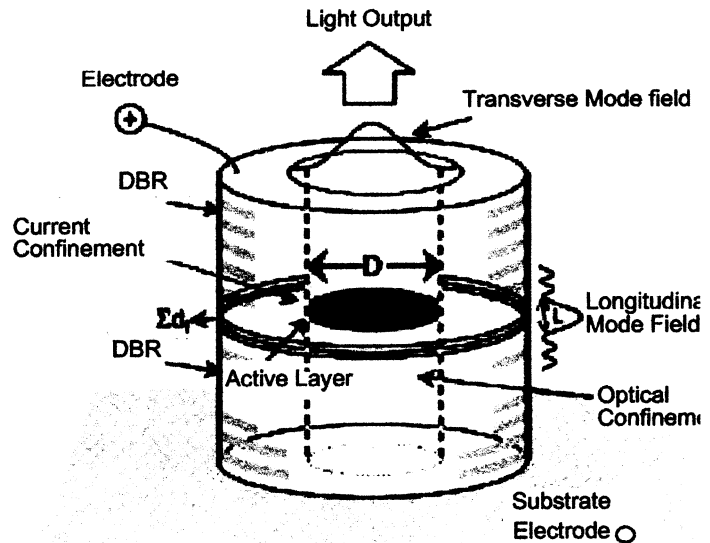


Fig. 1 A model of vertical cavity surface emitting laser.

$$I_{th} \cong \frac{eB_{eff}}{\eta_i \eta_{spon}} N_{th}^2 V_a \quad (1)$$

The relaxation frequency f_r is given when the driving current is much larger than threshold current by the equation;

$$f_r = \frac{1}{2\pi\tau_s} \sqrt{\frac{\tau_s}{\tau_p} \frac{\eta_i \eta_{spon}}{eB_{eff} N_{th}^2} \frac{I}{V_a}} \quad (2)$$

High speed modulation is possible due to small active volume V_a .

On the other hand, the free spectral range of surface emitting laser is expressed in terms of cavity length L_c by;

$$\Delta\lambda = \frac{\lambda_0^2}{2n_{eff}} \frac{1}{L_c} \quad (3)$$

Dynamic single mode operation is maintained due to this single mode condition. Wide frequency tuning range is based on the same physics.

Due to these physics the VCSEL may provide a number of advantages shown below;

- Ultra-low threshold operation is expected from its small cavity volume.
- Dynamic single mode operation.
- Wide and continuous wavelength tuning.
- Large relaxation frequency.
- Easy coupling to optical fibers.
- Monolithic fabrication and easy device separation without perfect cleaving requirement.
- Vertical stack integration by MEMS technology.

3. Technical Progress

We show some of semiconductor materials for surface emitting lasers in Fig. 2. In practical 850 nm devices, sub-mA thresholds and 10 mW outputs have been achieved. The power conversion efficiency of >50% has been demonstrated. As for the reliability of VCSELs, 10^7 hours of room temperature operation is estimated. Life test results on oxide-defined devices exhibited higher reliability. The Gigabit Ethernet has already been in markets by the use of

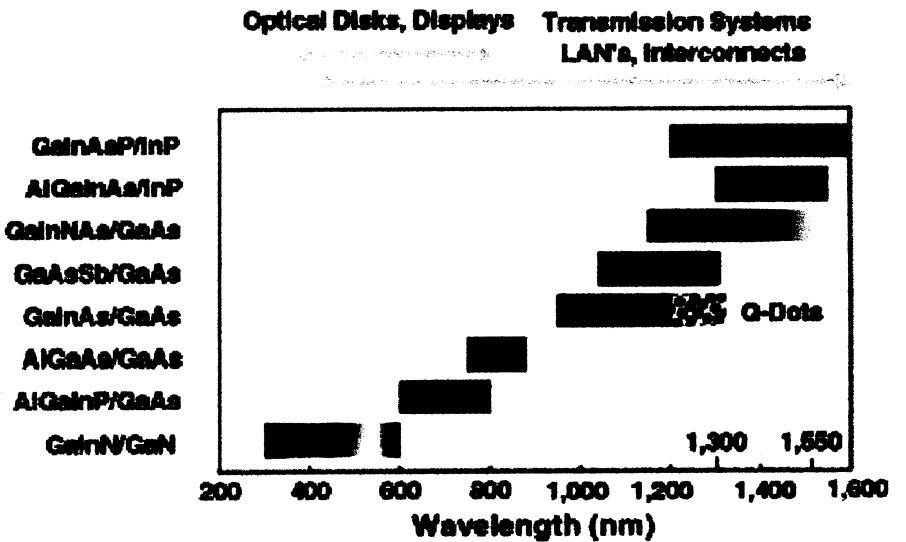


Fig. 2 Materials for VCSELs

multimode-fiber-based optical links. This system is being extended to 10 Gigabits/s Ether.

The importance of 1,300 or 1,550 nm devices is currently increasing for metropolitan area networks (MAN). A 1,550 nm VCSEL with MEMS tunable functions began to be introduced into a high end MAN system. One of viable materials for long wavelength emitters is a GaInNAs system which can be formed on GaAs substrates shown in Fig. 3[6].

In order to control the polarization of VCSEL output, (311)B substrate has been introduced and >30dB of orthogonal polarization suppression ratio (OPSR) was obtained even in high speed modulation condition. Recent results of (311)B VCSEL are shown in Fig. 4 and 5[7].

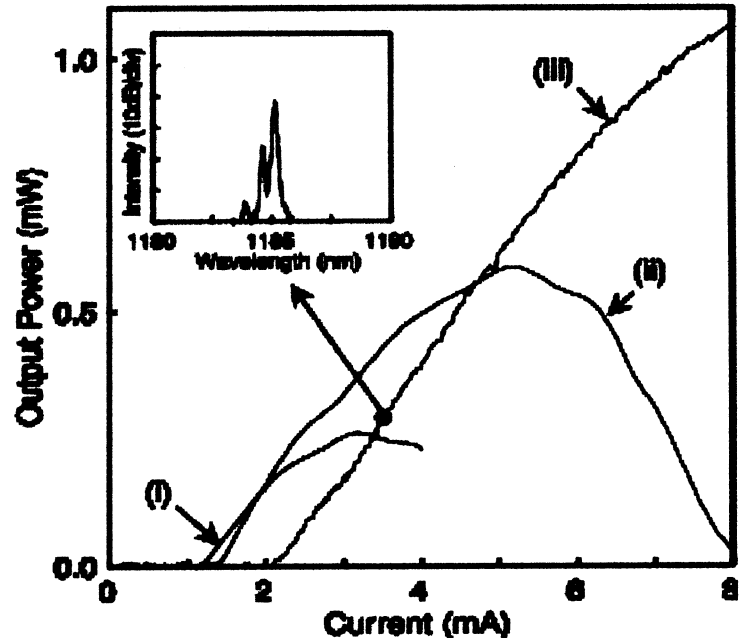


Fig. 3 GaInNAs VCSEL grown by CBE/MOCVD.

4. Exploratory, Emerging, or Disruptive?

The VCSEL itself is basically an exploratory device and generated a Gigabit Ethernet and fiber channel applications. It s emerging into higher class of data communication system such as 10 Gigabit Ethernet, high speed LAN's, optical interconnects, optical links, and so on. Moreover, long wavelength VCSELs have been developed toward long distance metropolitan area networks(MANs). It is noted that a continuous and wide range wavelength tunability is a unique solution among many other candidates for this purpose. It may be a disruptive technology to replace distributed feedback (DFB) lasers.

It is found that temperature dependence upon threshold and quantum efficiency could be removed by properly designing the device structure and material. The highly strained GaInAs/GaAs emitting 1200nm band is one of the candidates. The GaInNAs system may follow.

The application into optical disks looks to be another disruptive technology to simply replace currently existing lasers and pickups by taking the advantage of easy moduling scheme. GaN VCSEL may open up new field, if realized.

The positioning of VCSELs in wide spectral ranges is shown in Table I as a summary.

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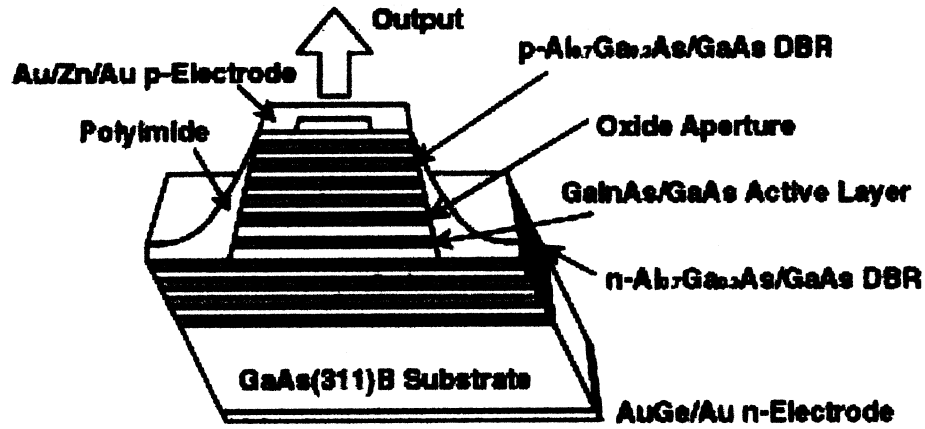
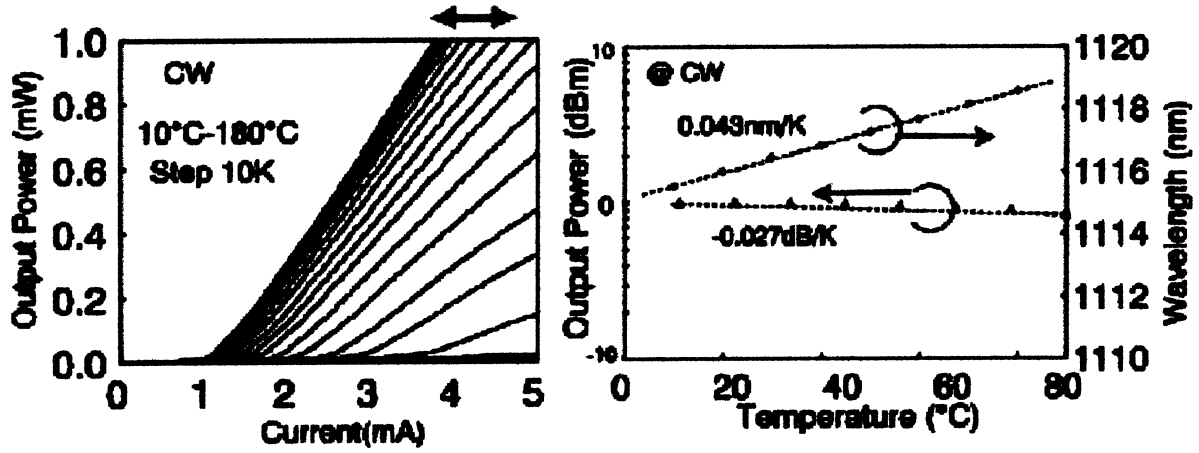


Fig. 4 GaInAs/GaAs VCSEL grown on (311)B substrate



(a) Light output vs current characteristics

(b) Temperature characteristics

Fig. 5 Lasing characteristics of GaInAs/GaAs VCSEL grown on (311)B substrate

Table I VCSEL technology map and wavelength (x=undefined)

Wavelength	Exploratory	Emerging	Disruptive
410 nm	Disks	x	x
650 nm	x	POF	x
850 nm	10G-Ether	Gbit-Ether	LAN/Link
980 nm	Interconnect	x	x
1200 nm	x	x	LAN
1300 nm	LAN	x	x
1550 nm	x→	x	Metro

Low-Noise, High-Speed Avalanche Photodiodes

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INTRODUCTION

For high-bit-rate, long-haul fiber optic communications, the avalanche photodiode (APD) is frequently the photodetector of choice owing to its internal gain, which provides a sensitivity margin relative to PIN photodiodes. APDs can achieve 5-10 dB better sensitivity than PINs, provided that the multiplication noise is low and the gain-bandwidth product of the APD is sufficiently high. The multiplication region of an APD plays a critical role in determining the gain, the multiplication noise, and the gain-bandwidth product. According to the local-field avalanche theory [1-4], both the multiplication noise and the gain-bandwidth product of APDs are determined by the ratio of the electron and hole ionization coefficients of the semiconductor in the multiplication region. Since this ratio is a material property, for a given electric field, efforts to improve the APD performance have focused on optimizing the electric field profile and characterizing new materials. Recently, lower multiplication noise and higher gain-bandwidth products have been achieved by submicron scaling of the thickness of the multiplication region [5-13]. This is in direct contrast to what would have been predicted by the local-field model and is due to the nonlocal nature of impact ionization, which can be neglected if the thickness of the multiplication region is much greater than the “dead length”, the distance over which carriers gain sufficient energy to impact ionize. However, when the dead space accounts for a significant portion of the multiplication region, the number of ionization chains that result in multiplication greatly in excess of the average gain is reduced, which, in turn, yields lower noise for a given gain. The minimum value to which the multiplication region can be scaled is ultimately determined by the onset of tunneling, which will result in excessive dark currents. Recently it has been shown that the noise of APDs with thin multiplication regions can be reduced even further by incorporating new materials and impact ionization engineering with beneficially designed heterostructures [14,15]. High gain-bandwidth products have been achieved by incorporating low-noise multiplication regions into resonant-cavity and waveguide structures [12,16].

IMPACT-IONIZATION-ENGINEERED AVALANCHE PHOTODIODES

Recently, we have achieved ultra-low multiplication noise by impact ionization engineering (I^2E). This approach utilizes heterojunctions to provide greater localization of impact ionization than can be achieved in spatially uniform structures.

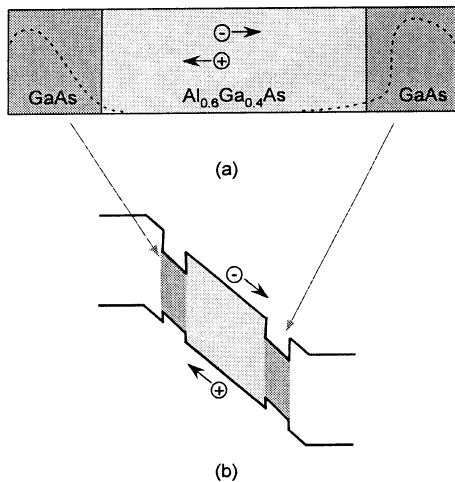


Figure 1. (a) Schematic and (b) bandstructure of the impact ionization engineered (I^2E) multiplication region.

The basic idea of I^2E is to place thin layers with relatively low threshold energy (referred to in the following as the multiplication layers) on each side of a region with higher ionization coefficients, the separation layer. Chia et al. have investigated impact ionization in multiplication regions consisting of Al_{0.3}Ga_{0.7}As(50nm)/GaAs(50nm) single heterojunctions [17]. They found that electrons passing from the Al_{0.3}Ga_{0.7}As region to GaAs ionize primarily in the GaAs, particularly at low electric fields. On the other hand, the holes that were injected into the Al_{0.3}Ga_{0.7}As from GaAs exhibited ionization properties characteristic of Al_{0.3}Ga_{0.7}As, which has lower ionization coefficients than GaAs. The goal of the I^2E structure is, therefore, to enhance impact ionization at the edges in the twin multiplication layers and to suppress it in the center while, at the same time, using the central separation layer to energize the carriers in transit. Figure 1 shows (a) a schematic of the layers and (b) the bandstructures. The implementation shown in Fig. 1 has GaAs multiplication layers and an Al_{0.6}Ga_{0.4}As separation layer. The dashed lines in Fig. 1(a) qualitatively represent the ionization rates. Structurally, the I^2E is similar to a truncated multiple quantum well APD [18,19], however, operationally there is a fundamental difference in that the I^2E does not invoke heterojunction band discontinuities.

Figure 2 shows measured excess noise factors $F(M)$ for four types of APDs; the InP/InGaAs APD that has been widely deployed for telecommunications, an AlInAs/InGaAs APD described in Ref. [12], a Si APD, and the I²E APD. The dotted lines are plots of $F(M)$ for $k=0, 0.02, 0.05$, and 0.3 using the local field model. These plots are presented solely for reference because the k value has become a widely used figure of merit for excess noise. The I²E APDs had 50-nm-thick multiplication layers and an 85 nm-thick separation region. For $M < 20$ the multiplication noise would correspond to negative k values, which is further confirmation of the inadequacy of the local-field model for this kind of APD.

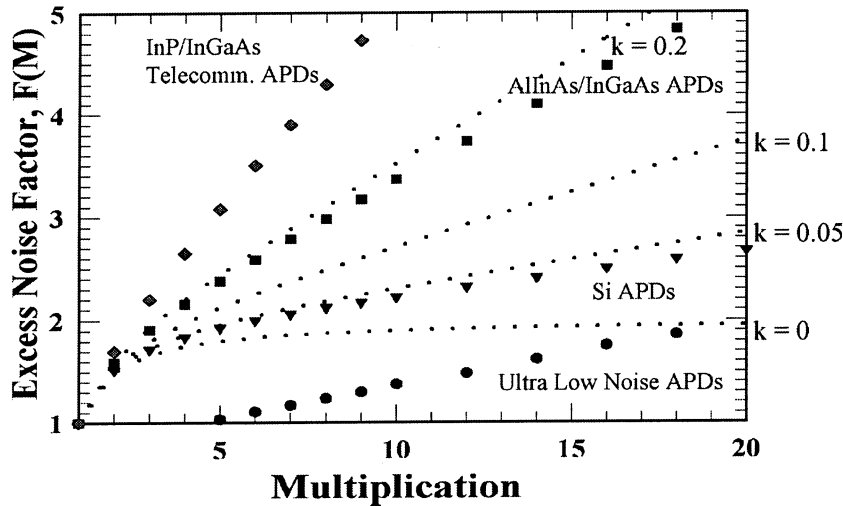


Figure 2. Excess noise of an InP/InGaAs telecommunication APD, an AlInAs/InGaAs APD, a Si APD, and an I²E APD.

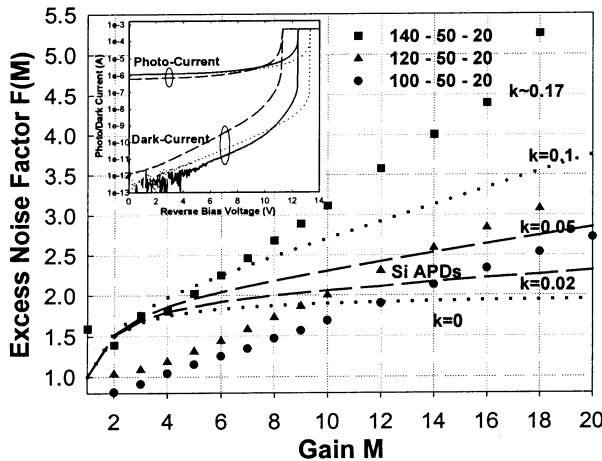


Figure 3. The measured excess noise factors for GaAs/Al_{0.6}Ga_{0.4}As single-heterostructure APDs with different Al_{0.6}Ga_{0.4}As acceleration layer thickness. The inset shows the dark current and photoresponse with dashed, dotted, and solid lines for the 100nm, 120nm, and 140nm acceleration regions, respectively.

It has been found that comparable noise levels to the twin-well structures can be achieved with single heterojunctions. The structure is similar to that in Fig. 1 except that the multiplication region nearest the p-region has been removed. Simulations show that for pure electron injection, electrons ionize predominantly in the GaAs region,

while the secondary holes ionize primarily in the Al_{0.6}Ga_{0.4}As region. At very high field intensities, both electrons and holes contribute to the gain by impact ionization. However, at lower fields, electron ionization is dominant with few hole ionizations. The preference for single-carrier ionization and the spatial localization result in very low noise. The extent to which acceleration of the electrons in the wide-bandgap layer plays a roll is still an open question.

The effect of changing the thickness of the separation layer is shown in Figure 3. The GaAs multiplication layer was 50nm, the nominal dopant diffusion offset was 20nm, and the separation layers were 140nm, 120nm, and 100nm. Low dark current and high gain were achieved. The reference curves correspond to $k=0, 0.02, 0.05$, and 0.1 . The noise was observed to decrease with decreasing acceleration layer thickness. For an acceleration layer of 120nm or 100nm, the noise level is comparable to silicon APDs, and for the 100nm case, the excess noise factor is even lower than that of Si APDs for $M < 15$.

WAVEGUIDE AVALANCHE PHOTODIODES

The demands of high-bit-rate receivers for optical fiber telecommunications systems operating at 40Gbit/s have made the implementation of wide-bandwidth avalanche photodiodes (APDs) increasingly attractive. For these applications, the key APD performance characteristics are a high gain-bandwidth product and low multiplication excess noise. In order to improve the bandwidth and the gain-bandwidth product of APDs, approaches that have achieved very high bandwidths for PIN photodiodes have been recently been utilized for APDs. The include

resonant cavity [20,21] and waveguide structures [22-24]. The edge-coupled waveguide configuration is attractive for high-speed applications because it permits the absorption region to be thinned in order to reduce carrier transit times without compromising the responsivity, which becomes a function of device length rather than thickness. Waveguide devices are also compatible with coplanar interconnects. Whereas conventional, vertically illuminated devices require a window in the top contact metal, the entire top surface of side-illuminated devices may be metallized, drastically reducing the contact resistance in small devices and thereby relaxing the bandwidth constraint imposed by the RC time constant. Further, waveguide APDs do not have the wavelength-selective response of the microcavity devices.

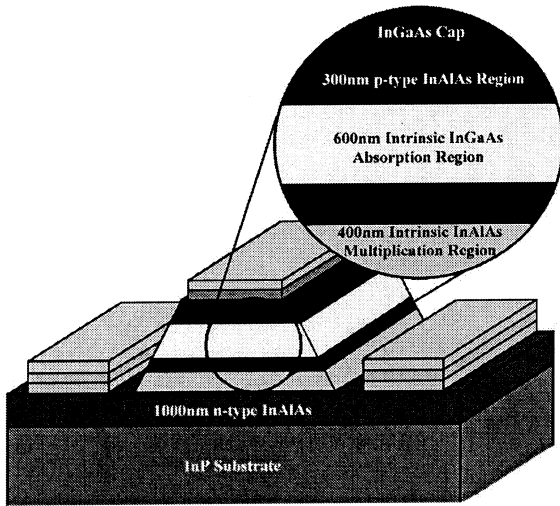


Figure 4. Cross-section of AlInAs/InGaAs waveguide APD.

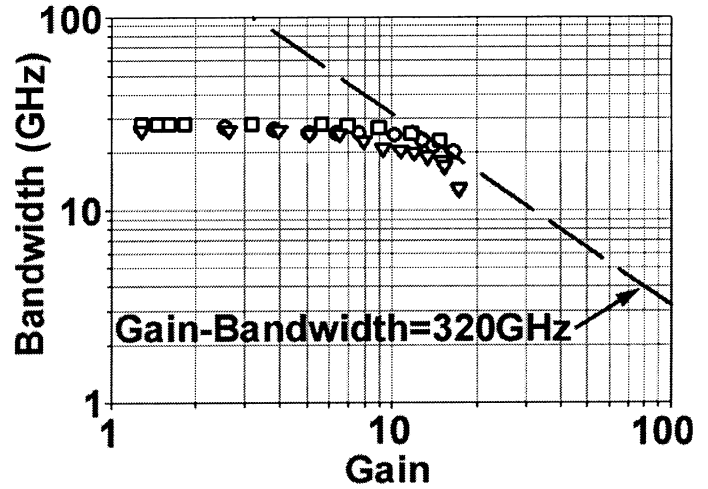


Figure 5. Bandwidth versus gain of AlInAs/InGaAs waveguide APD.

A schematic cross section of an SACM waveguide APD is shown in Fig. 4. The device layers were grown by metalorganic vapor phase epitaxy. A 100nm n-type InP buffer layer was followed by a 300nm n-type $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layer. The 150nm multiplication layer was grown using unintentionally-doped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$. This was followed by a 180nm $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ charge layer that was doped with Zn to a nominal level of $2.1 \times 10^{17} \text{ cm}^{-3}$. Two 100nm unintentionally-doped InAlGaAs guiding layers bracketed the 200nm unintentionally-doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ absorption layer. Finally, a 200nm p^+ $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layer was followed by a 50nm p^+ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ cap layer. To fabricate high-speed devices, a rectangular Ti-Pt-Au p-contact was deposited using a lift-off process.

The frequency response was measured using a 50GHz spectrum analyzer and a passively mode-locked Ti-sapphire laser. The results for several $10\mu\text{m} \times 10\mu\text{m}$ devices are shown in Fig. 5. The devices exhibited an optical (power) – 3dB bandwidth of 28GHz up to a gain of six. At higher gains, the speed was limited by the gain-bandwidth product, which was determined to be 320GHz. Noise measurements showed an equivalent k value of ~ 0.15 for multiplication up to 23. The quantum efficiency was measured using a tungsten-halogen light source, a spectrometer, and a lock-in amplifier. The highest external quantum efficiency of 16% was achieved with a cleaved device.

SUMMARY

We have described materials and structural modifications to the thin multiplication regions that have yielded ultra low multiplication noise. In the low gain regime, these APDs have achieved excess noise factors lower than that of Si APDs. We have also shown that very high gain-bandwidth products can be achieved by proper design of the multiplication region and the use of a waveguide structure.

ACKNOWLEDGMENTS

This work has been supported by DARPA. The author is grateful to A. G. Dentai, A. L. Holmes, and B. G. Streetman for supplying the crystals used in this work. The following graduate students have made this work possible: K. A. Anselm, C. Lenox, H. Nie, P. Yuan, G. S. Kinsey, S. Wang, X. G. Zheng, X. Sun, and R. Sidhu.

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Status, Prospects and Commercialization of SiC Power Devices

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Since more than a decade of years we have continuously performed research and developments devoted to SiC Power Devices. Stimulated by the successful work at Siemens Corporate Technology SiCED was founded in March 2000 as a joint venture of Siemens AG and Infineon Technologies AG, taking over all SiC device activities from Siemens Corporate Technology.

Up to now our activities were focused besides fundamental work on materials and technological issues on Schottky Diodes, MOSFET's, Vertical Junction Field Effect Transistors and Bipolar Diodes.

We have developed SiC Schottky diodes for blocking voltages ranging from 300 V to 1700 V covering a range of nominal currents from 4 A up to more than 25 A. Schottky diodes for blocking 300 V with nominal current ratings of 6 A and 10 A respectively, and for blocking 600 V with nominal current rating of 4 A and 6 A respectively, are already commercialized by our parent Company Infineon Technologies AG, Schottky diodes for blocking 1200 V will follow soon. For higher blocking voltages up to 3 kV also merged diodes were successfully developed.

We have also performed R&D on n-channel enhancement SiC MOSFET's. However, despite the promising performance (1800 V, 46 mΩcm² e.g.) SiC MOSFET's are still far away of their commercialization due to the lack of long term stability and an on-resistance sufficiently low enough to compete with their Silicon enemies.

As a rugged and very promising alternative to the SiC MOSFET we have developed Vertical Junction Field Effect Transistors (VJFET's). The drawback of these devices – they are normally on – can be overcome by using them in a cascode circuitry, e.g. in conjunction with a low voltage Silicon MOSFET. Taking advantage of DCB (Direct Copper Bond) substrates we have realized small cascode hybrid modules containing one Silicon MOSFET and up to three paralleled VJFET's. These small modules do show a performance of blocking 1800 V while having only 0,15 Ω on-resistance at room temperature to day.

Very recently, in February 2000, we were successful in demonstrating a vertical junction transistor blocking a voltage V_B of more than 3000 V while having a specific on-resistance R_{onsp} of only 25 mΩcm². The sometimes cited corresponding figure of merit - $V_B^2/R_{onsp} \approx 400 \text{ MW/cm}^2$ - demonstrates a breakthrough for high voltage, fast and rugged, solid state switching devices.

After the commercialization of SiC Schottky diodes we are convinced that as a novel generation of solid state power switches VJFET's will enter the market. The soon availability of e.g. 3-leg normally-off laboratory samples capable of blocking 1500 V and having only 0.5 Ω on-resistance while showing extremely good dynamic characteristics will certainly stimulate an interest by customers.

Fast switching, e.g. 10 kHz, high voltage, e.g. 3.3 kV, low loss unipolar devices become visible on the horizon of novel power devices. The possibility of getting fast unipolar power devices showing only 3.5 V forward voltage loss at a junction temperature of 125 °C and at a current density of 70 A/cm² will most probably create novel ideas in the field of power electronics.

Silicon Devices

MONDAY PM, JUNE 25TH, 2001

Session Organizer: Jeffrey Welser, IBM Technology Group

2:00 PM, II.A.-1, Invited

High-K Gate Dielectrics for Sub-100 nm CMOS Technology: *Dim-Lee Kwong*¹; ¹The University of Texas at Austin, Microelectronics Research Center, 10100 Burnet Road, Bldg. 160, Austin, TX 78758 USA

2:30 PM, II.A.-2

Fast Write Time and Long Retention 1T Memory: *Albert Chin*¹; M. Y. Yang¹; S. B. Chen¹; C. L. Sun²; S. Y. Chen²; ¹National Chiao Tung University, Dept. of Electronics Engineering, Hsinchu, Taiwan; ²National Chiao Tung University, Dept. of Materials Science Engineering, Hsinchu, Taiwan

2:50 PM, II.A.-3

Physical Origin of SILC and Noisy Breakdown in Very Thin Silicon Nitride Gate Dielectric: *Igor Polishchuk*¹; Tsu-Jae King¹; Chenming Hu¹; ¹University of California at Berkeley, Department of Electrical Engineering and Computer Sciences, Berkeley, CA 94720 USA

3:10 PM, II.A.-4

Low-Power CMOS at $V_{dd}=4kT/q$: *Andres Bryant*¹; Jeffrey Brown¹; Peter Cottrell¹; Mark Ketchen²; John Ellis-Monaghan¹; E. J. Nowak¹; ¹IBM Microelectronics Division, Essex Junction, VT 05452 USA; ²IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA

3:30 PM Break

3:50 PM, II.A.-5

A Sub-40nm Body Thickness N-Type FinFET: *David M. Fried*¹; Arthur P. Johnson¹; Edward J. Nowak¹; Jed H. Rankin¹; Christa R. Willets¹; ¹IBM Microelectronics Division, Essex Junction, VT 05452 USA

4:10 PM, II.A.-6

Quasi-Planar NMOS FinFETs with Sub-100nm Gate Lengths: *Nick Lindert*¹; Yang-Kyu Choi¹; Leland Chang¹; Erik Anderson²; Wenchin Lee³; Tsu-Jae King¹; Jeffrey Bokor¹; Chenming Hu¹; ¹University of California at Berkeley, Department of Electrical Engineering and Computer Sciences, Berkeley, CA 94709 USA; ²X-Ray Optics, Lawrence Berkeley National Laboratory, Berkeley, CA USA; ³Intel Corporation, Logic Technology Development, Hillsboro, OR USA

4:30 PM, II.A.-7

High Performance of Planar Double Gate MOSFETs with Thin Backgate Dielectrics: *Erin C. Jones*¹; Meikei leong²; Thomas Kanarsky²; Omer Dokumaci²; Ronnen A. Roy¹; Leathen Shi¹; Toshiharu Furukawa³; Robert J. Miller¹; H-S Philip Wong¹; ¹IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA; ²IBM SRDC, Hopewell Junction, NY 12533 USA; ³IBM Microelectronics Division, Essex Junction, VT 05254 USA

4:50 PM, II.A.-8

$Si_{1-x}Ge_x$ Channel Vertical PMOSFET with Asymmetric Ge Profile: *Xiangdong Chen*¹; Qiqing Ouyang¹; Sankaran Kartik Jayanarayanan¹; Freek E. Prins¹; Sanjay Banerjee¹; ¹The University of Texas at Austin, Microelectronics Research Center, 10100 Burnet Road, Bldg. 160, Austin, TX 78758 USA

High-K Gate Dielectrics for Sub-100 nm CMOS Technology

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Microelectronics Research Center
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High-K dielectric materials are being developed as an alternative to SiO_2 and SiO_xN_y based gate dielectrics beyond the 12-15Å equivalent oxide thickness (EOT) range. The need to replace the industry workhorse is due to the unacceptable level of quantum mechanical tunneling through the ultra thin dielectric resulting in high gate leakage and standby power dissipation. This is of major concern for the communications market segment that low power ASIC devices must address. The use of physically thicker, higher K materials is one approach that can alleviate tunneling. These materials pose unique challenges due to the complex nature of their interface with Si, thermal stability and electrical properties. In the extreme case, the generic CMOS process flow will have to be reversed. In addition, methods to measure reliability of these films must be demonstrated. Of particular interest is the ability to integrate these high-K materials into a conventional self-aligned dual-gate CMOS transistor process flow so as to achieve $\text{EOT} < 1\text{nm}$ with significantly reduced gate leakage but comparable carrier mobility to SiO_xN_y .

In this talk, the materials and processing challenges for the fabrication of high quality, ultra-thin ($\text{EOT} < 1\text{ nm}$) CVD high-K gate stack will be reviewed along with the most recent results on CVD ZrO_2 , HfO_2 and their silicates. The requirement for ultra thin and robust interface layers to avoid any thickness increase due to post-deposition processing to achieve thinnest EOT will be discussed. Results will be presented on thermal stability of high-K materials, and interfacial reactions of high-K/Si and high-K/gate electrode. We will also discuss key factors that govern the conduction and degradation mechanisms in high-K gate stack. Both poly-Si and poly-SiGe are explored as possible gate electrode materials and the upper thermal budget limit for such materials are discussed. CVD HfO_2 gate stack has been demonstrated with conventional n^+ -poly-Si gate electrode, achieving $\text{EOT} = 1\text{ nm}$ and $J_g = 3 \times 10^{-4}\text{ A/cm}^2$ @ $V_g = -1\text{ V}$, which is at least 4-5 orders of magnitude smaller than that of SiO_2 with similar EOT and flat-band voltage. These poly-Si-gated CVD HfO_2 gate stack shows SiO_2 -like hysteresis and interface states density, no C-V dispersion, excellent long-term TDDDB, negligible boron penetration, and are thermally stable up to 1000C. These and recent results of mobility and device characteristics on both n- and p-MOSFETs with these gate stacks fabricated using conventional poly-Si self-aligned process will be presented.

Fast Write Time and Long Retention 1T Memory

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Abstract

It is desirable to achieve both fast data access time and long data retention time simultaneously. We have developed 1T PZT/40Å-Al₂O₃ memory to achieve very fast write (program/erase) time <100ns, years long data retention, and good endurance >10¹⁰ P/E cycles. The small 1T size is highly competitive with other memory technologies.

Introduction

One difficult challenge for memory is to reach both fast write time and long data retention simultaneously. These can be understood in Table 1 by the fast write time in 1T1C DRAM cell but limited by the short retention time. On the contrary, years long retention can be obtained in 1T Flash memory but limited by the very long write time. The tread-off between write and retention time exists in DRAM and Flash memory is due to the required physical charge transfer. In contrast, memory technique using ferroelectric effect does not require physical charge transfer but based on atomic polarization that can be switched <ns and expected to have long retention time. However, little progress has been achieved in 1T memory because of the strong interface reaction between Si and ferroelectric gate dielectric [1]. In this paper, we have developed Pb(Zr,Ti)O₃ (PZT)/thin-Al₂O₃ gate dielectric 1T memory because Al₂O₃ has demonstrated good gate dielectric integrity in our previous study [2] with also superior diffusion barrier property. Very fast write (program/erase) time, long data retention, and good endurance are achieved simultaneously.

Experimental

After device isolation, a thin 40Å Al₂O₃ gate dielectric is formed as a diffusion barrier before 2500Å PZT deposition. The Al₂O₃ gate dielectric is formed on a native oxide free Si surface using HF-vapor passivation and *in-situ* desorption followed by Al evaporation, oxidation and annealing [2]. The thin Al₂O₃ gate dielectric is important because the strong interface reaction between PZT and Si will destroy both MOSFET and memory performance. The formed PZT/40Å-Al₂O₃ gate dielectric was further annealed in N₂ at 750°C for 1hr. Then Al gate MOS capacitor and MOSFET are fabricated to evaluate the electrical characteristics of 1T memory.

Results and Discussion

A. DC characteristics:

The strong interaction between PZT and Si is evidenced in Fig. 1 from the poor C-V characteristics and small threshold voltage change (ΔV_T) even growing 40Å SiO₂ on Si beneath PZT. In sharp contrast, much improved C-V and good memory characteristics are observed in Fig. 2 using PZT/Al₂O₃ gate dielectric that demonstrates excellent diffusion barrier and gate dielectric properties of 40Å Al₂O₃. The memory effect related ΔV_T decreases from 5V to 1V for $\pm 15V$ and $\pm 5V$ write voltages respectively. In this paper, only $\pm 10V$ were chosen, although typical breakdown voltage is $\sim 35V$ and the V_g dependent ΔV_T can be used for multi-level memory. Fig. 3 shows the I_D - V_D characteristics of this stacked gate MOSFET. Besides good I_D - V_D characteristics, this device shows a large I_D difference between on ($-10V$) and off ($10V$) state. The output current difference is further shown in Fig. 4, which is due to program/erase voltage induced ΔV_T .

B. Write speed, data retention, and reliability:

We have further measured the write time of this 1T memory. Figs. 5 shows the drain current I_d after writing on ($-10V$) and off ($10V$) state pulse of 10ns-0.1s. The fast on and off time of <100ns suggest the excellent performance of write speed comparable to SRAM or DRAM and much faster than Flash memory. The endurance characteristics of this fast write memory are shown in Fig. 6. Program/erase cycles >10¹⁰ is easily obtained. The good endurance suggests low defect density generated in PZT and PZT/Al₂O₃ interface during cycling. We have also measured the data retention of the stacked gate 1T memory. Fig. 7 shows the on and off state currents after writing $\pm 10V$ for 1sec. A retention time longer than 10 years is obtained if using a typical sense amplifier >1 $\mu A/\mu m$. Table 1 summarizes the comparison of different memories. The advantages of this memory are simultaneously achieving all the required memory merits of good endurance, small 1T size, DRAM-like fast write, and Flash-memory-like long retention. This memory also has potential to integrate with high-k Al₂O₃ MOSFET logic [2], and the simple 1T structure is highly competitive with other memories that are becoming more and more difficult for further scaling down.

Conclusions

We have achieved <100ns write time, years retention, and endurance >10¹⁰ P/E cycles for 1T PZT/Al₂O₃ MOSFET.

[1]. E. Tokumitsu *et al.* IEEE EDL-18, p. 160 (1997).

[2]. A. Chin *et al.* Symp. on VLSI Tech.(1999), p.133.

Table 1. Comparison of important memory parameters for DRAM, SRAM, Flash, and stacked gate Ferroelectric MOSFET (FeMOSFET). The 1T FeMOSFET in this paper has both DRAM-like fast write speed and Flash-memory-like long data retention.

	DRAM	SRAM	Flash	FeMOSFET
Size	1T1C	8T	1T	1T
Scalability	moderate	excellent	moderate	good
Write speed	50ns	10ns	10 μ s	<100ns
Data retention	0	0	>10year	>10year
Endurance	>10 ¹⁵	>10 ¹⁵	>10 ⁵	>10 ¹⁰

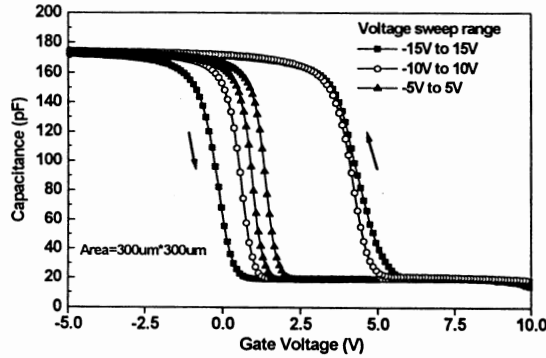


Fig. 2. The 1MHz C-V characteristics of stack gate 2500Å-PZT/40Å-Al₂O₃/Si capacitor. The capacitor size is 9×10^{-4} cm².

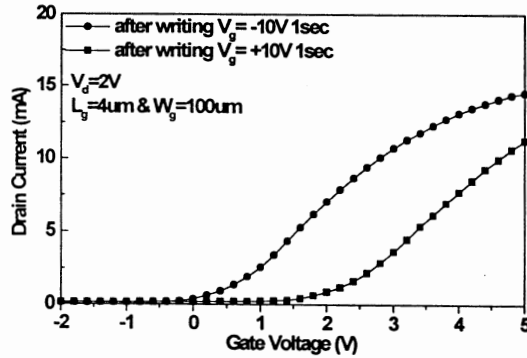


Fig. 4. The I_d - V_g characteristics of 4 μ m stack gate PZT/Al₂O₃ MOSFET after writing -10V and 10V for 1sec. The threshold voltage shift is due to the ferroelectric nature.

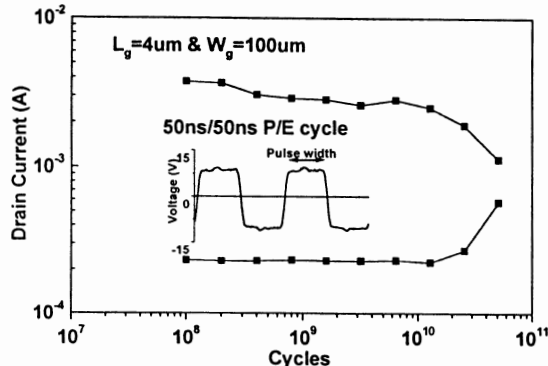


Fig. 6. Endurance characteristics of 4 μ m PZT/Al₂O₃ MOSFET at pulse widths of 50ns.

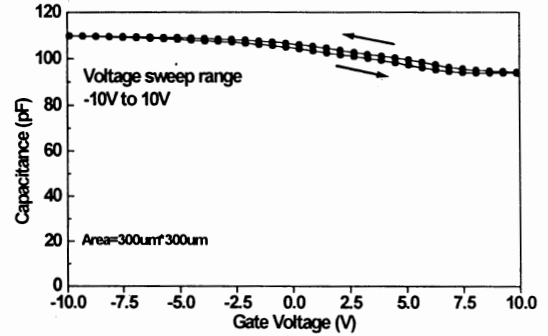


Fig. 1. The 1MHz C-V characteristics of stack gate 2500Å-PZT/40Å-SiO₂/Si capacitor. The capacitor size is 9×10^{-4} cm².

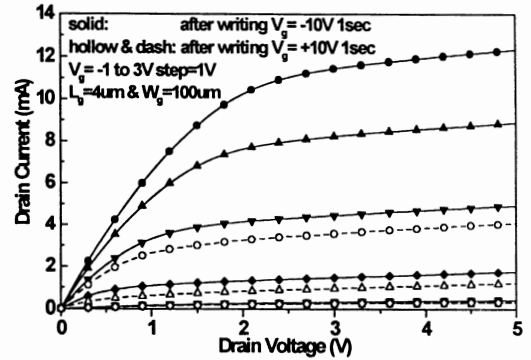


Fig. 3. I_d - V_d characteristics of 4 μ m gate length PZT/Al₂O₃ MOSFET. Solid and hollow marks show the I_d after writing -10V and 10V for 1sec, respectively.

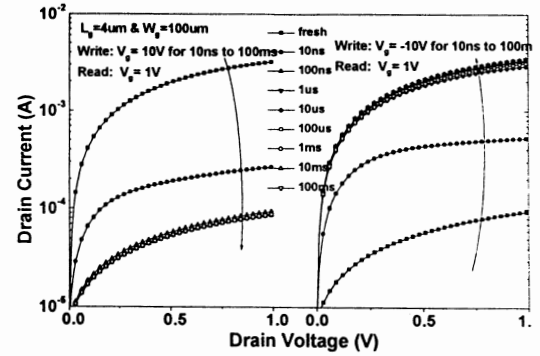


Fig. 5. I_d - V_d characteristics of 4 μ m PZT/Al₂O₃ MOSFET after writing 10V and -10V to gate with program time from 10ns to 100ms.

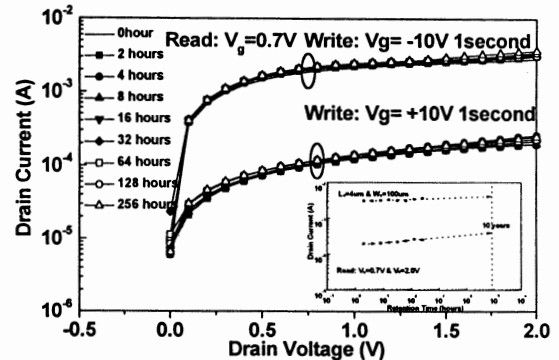


Fig. 7. I_d - V_d retention characteristics of 4 μ m PZT/Al₂O₃ MOSFET after biasing at -10V and 10V and leaving for different time.

Physical Origin of SILC and Noisy Breakdown in Very Thin Silicon Nitride Gate Dielectric

Igor Polishchuk, Tsu-Jae King, Chenming Hu

As the equivalent oxide thickness of the MOSFET gate dielectric continues to shrink, the transition to a material with a higher dielectric constant, such as Si_3N_4 , seems imminent. It is well recognized that stress-induced leakage current (SILC) and noisy (or soft) breakdown have become very important degradation phenomena in the ultra-thin gate dielectrics. A lot of attention has been recently paid to SILC¹ and soft breakdown² in SiO_2 gate dielectrics, however the physical origins of these phenomena have not been thoroughly investigated. An understanding of the physical mechanisms responsible for the degradation of the ultra-thin gate dielectrics is critical to the development of a reliability model for the future generations of CMOS technology. This paper offers for the first time a detailed examination of SILC and noisy breakdown in Si_3N_4 demonstrating that these two degradation phenomena have a common origin. The nature of the traps responsible for SILC and noisy breakdown is revealed. The proposed degradation mechanism also provides a key to understanding and modeling of the dielectric reliability in the ultra-thin SiO_2 and new high-K gate materials.

P-MOSFETs with JVD nitride³ gate dielectric of 1.4 nm equivalent oxide thickness were studied. After 10^5 s of -3 V constant-voltage stress, the gate current of a $10\mu\text{m} \times 10\mu\text{m}$ transistor increased by about 40%. While the amount of SILC is modest, post-stress I_g exhibited a telegraphic signal characteristic as shown in Figure 1. The observed on-off switching behavior is commonly referred to as noisy or soft breakdown. We propose the following model to explain how SILC and noisy breakdown are linked. A single bulk trap generated by stress is substantially responsible for the switching behavior observed in Fig. 1. The potential of a charged trap in Si_3N_4 (Fig.2) has a number of higher states (excited states) in addition to the deep ground state. It is commonly agreed that SILC is the result of trap-assisted tunneling (TAT) through bulk traps⁴. The electron tunneling time from an excited state can be estimated to be in the ns range when the trap is centrally-located, which is consistent with the observed current level of 0.3 nA (or 1 electron per 0.5ns). The electron capture and emission times for the ground state are much longer since they rely on unlikely multi-phonon processes. Once an electron is captured in the ground state it raises the potential barrier and prevents other electrons from tunneling, and I_g drops. When this electron is finally emitted, TAT resumes and I_g rises. A second trap (conduction path) contributing 0.03nA steps can also be observed in Figure 1. This explains the doublets in Figure 1b. Many even weaker paths are contributing to the low amplitude noise. After additional stress, additional weak conduction paths are created and the total level of leakage current increases while the contribution from the two larger paths remains unchanged (Fig. 1b).

The Random Telegraphic Noise (RTN) behavior in Figure 1 has been previously observed for MOSFET drain current. The fluctuations in the drain current are attributed to the change in carrier number and mobility when a surface state is emptied or occupied⁵. Similarly, capture and emission of an electron from a trap in the gate dielectric lead to RTN in our case. There is an important difference however. Since the surface trap exists in the vicinity of the substrate, its occupation probability is determined by the substrate Fermi level. Consequently, the ratio of capture to emission times changes by a factor of ten for every 60 mV change of the trap-level position with respect to the Fermi level. In our case that ratio remains constant (Fig 3). Furthermore, capture and emission times both change by a factor of 10 for every 120 mV change in V_{ox} , which suggests that the trap is located right in the middle of the dielectric. Since the trap captures electrons from the cathode (substrate), it is the substrate Fermi level that determines the capture time. The emission time, on the other hand, is determined by the Fermi level in the gate, because trapped electrons are emitted into the gate (Fig.2). Consequently, both capture and emission times decrease with increasing gate bias. Thus we attribute our RTN (i.e. both noisy breakdown and SILC) to the bulk traps.

To explore the nature of the bulk traps further we investigated the temperature dependence of RTN. Figure 4 shows I_g versus time measured at different temperatures. The amount of current flowing through a single trap (~ 1 nA) is rather insensitive to temperature change as expected for a tunneling current. The capture and emission rates on the other hand, increase exponentially with temperature (Fig. 5). This strong temperature dependence is expected since high-energy phonons are required to facilitate the capture and emission (Fig. 2). The activation energies for the capture and emission processes can be extracted from Figure 5. Consequently, we conclude that the trap level is 2.75 eV below the Si_3N_4 conduction band. A trap level at that energy in Si_3N_4 has been previously reported⁶.

In summary, a large number of weak conduction paths (off-center traps) contribute to SILC in silicon nitride. Soft or noisy breakdown occurs when a strong tunnel path (in our 1.4 nm nitride, a single trap located near the center of the film) is created by electrical stress. The ground state of the trap is 2.75eV below the E_C of the nitride. When the ground state is empty electrons from the cathode tunnel to the anode assisted by the higher energy states at the rate of one electron per 0.5ns. When the ground state captures an electron from the cathode, TAT is turned off until the captured electron tunnels out into the anode. The proposed model explains the physical origin of SILC and noisy breakdown, and can be applied to Si_3N_4 , SiO_2 and other gate dielectrics.

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² J. Suñé et al., IEEE Elec. Dev. Lett., 21, 167, (2000)

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⁶ V. J. Kapoor, The physics of MOS insulators, New York : Pergamon Press, 1980, p. 117

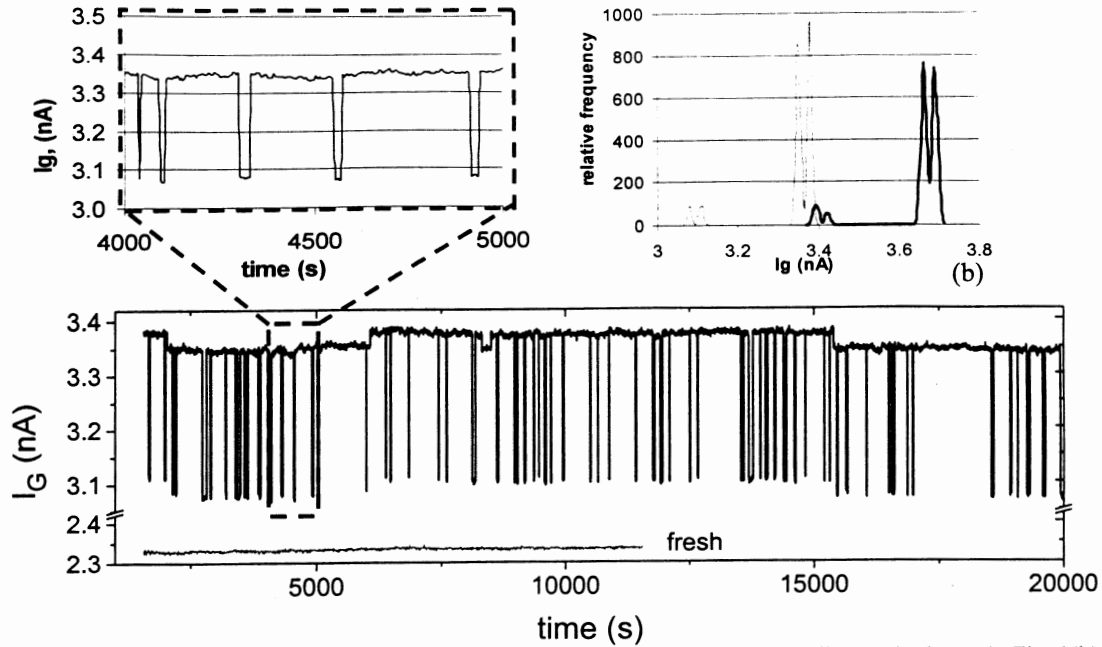


Fig. 1. Random telegraphic noise observed at $V_g = 1$ V. A histogram of I_g distribution is shown in Fig. 1(b). As additional weak conduction paths are created, the new histogram peaks (thick lines) are shifted to the right and broadened.

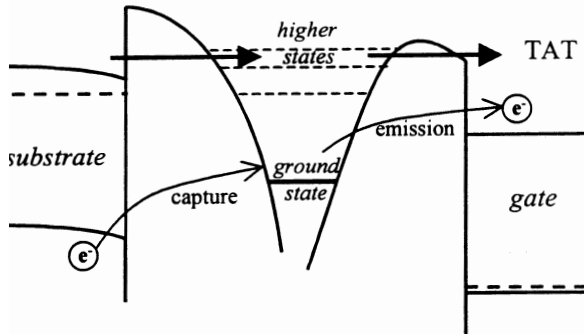


Fig. 2 Energy-band diagram of Si-Si₃N₄-Si structure with a bulk trap modeled as a coulombic potential well.

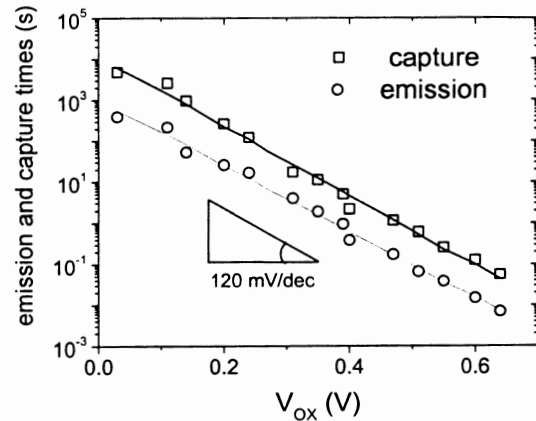


Fig. 3. The capture and emission (high I_g and low I_g) times both change by a factor of 10 for every 120 mV change in the oxide voltage

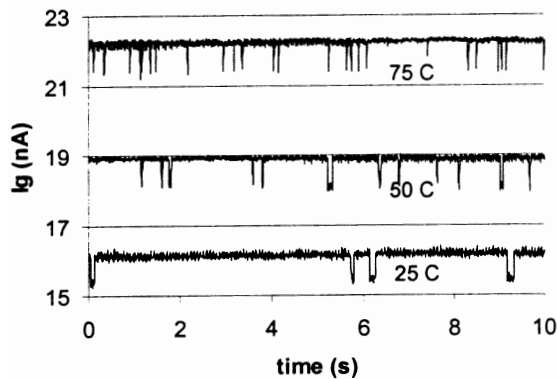


Fig. 4. Trapping and detrapping rates increase with temperature. $V_g = 1.3$ V.

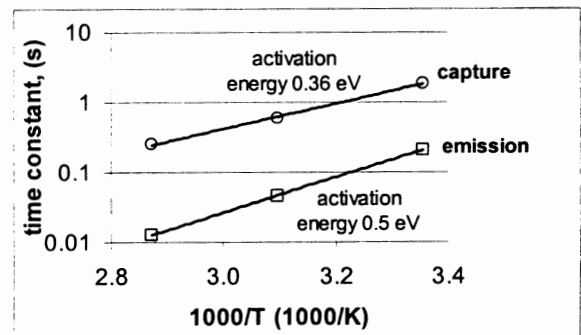


Fig. 5. Capture and emission times depend exponentially on temperature. Activation energies correspond to the energies absorbed by an electron during capture and emission.

Low-Power CMOS at $V_{dd}=4kT/q$

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Introduction.

This paper reports a CMOS inverter active power-delay product of less than 0.1fJ/stage at 25°C and at $V_{dd}=0.1V$. We believe this is the lowest reported. This is accomplished by using a novel technique to match NFET and PFET subthreshold currents and, thus, enable operation of a standard 1.5V 180nm CMOS technology in subthreshold at very low V_{dd} .

Theoretical analysis [2] reveals that operation of MOSFETs with $V_{gs}-V_t < 0$ (subthreshold) is required to attain the lowest possible power and voltage. The ideal limit for lowest operable voltage is expected to be $\sim 2n kT/q$ (~ 52 mV at 25°C for ideality $n=1$). To achieve this ideal limit, however, the NFET and PFET thresholds must be adjusted to ensure comparable off currents ($I_{offn}=I_{offp}$) [1]. Otherwise voltages in excess of $2kT/q$ will be required to ensure function. We experimentally demonstrate a novel technique which accomplishes this requirement over a range of process latitude and, thus, significantly enhances the manufacturability of CMOS subthreshold logic. This technique uses voltage feedback to the MOSFET wells to match the NFET off current (I_{offn}) and PFET off current (I_{offp}).

Drive-Matching Technique.

Threshold matching of NFETs and PFETs is governed by control of independent processes (e.g.; thermal activations, gate formation, and well, halo, and source/drain implants). Hence NFET and PFET I_{off} 's can vary significantly with respect to each other. Fig. 1 shows the simple well regulator circuit that will force I_{offn} and I_{offp} to be equal. The regulator output voltage is fed back to the regulator's NFET and PFET wells to force the matching condition. The MOSFET wells of the logic gates are then biased by the regulator output to match I_{offn} and I_{offp} . In our implementation we have used silicide to form firm electrical continuity between the nwell and p wells, thereby enabling the drive matching technique without using conventional metalization. The bias can be distributed through the common substrate or wells.

Process and Experimental Results.

Circuits and single FETs were built in a standard 180nm lithographic scale 1.5V CMOS technology with $T_{ox}=27\text{\AA}$. 61-stage inverter and 81-stage 2-input NAND ring-oscillators (RO's) were built with minimum 0.6 μm wide FETs to minimize power. Fig. 2 shows the NFET and PFET sub- V_t I_d - V_g curves at well biases of 0 and 0.1V. Fig. 3 shows the NFET and PFET subthreshold I_d - V_d output characteristics at 0V well bias. Since the PFET sub- V_t current is higher, the well regulator provides a positive well bias to match the N and P current drives (Fig. 4). However, a NAND circuit is further imbalanced because NFETs are stacked as indicated the NAND I/O transfer characteristics (Fig. 5). The added NAND imbalance can be eliminated by adjusting the W_p/W_n ratio of the well regulator.

Fig. 6 shows the output driver waveform NAND RO running at $V_{dd}=200\text{mV}$. The inverter switching energy (power-delay) per stage versus stage delay is shown in Fig. 7. Energies less than 0.1fJ were measured for $V_{dd}<200\text{mV}$ and are estimated to be 10x lower active power than previously reported at equal stage delay [2]. Operation at $V_{dd}=0.07V$ has been reported [3] but power is estimated to be significantly higher because zero- V_t FETs were operated above threshold. Fig. 7 also shows the energy when the inverter RO are operated above threshold.

Subthreshold Operation Discussion and Conclusions:

Several subtle points emerge from the operation of CMOS at subthreshold voltages. First, the I_{on}/I_{off} is only $\sim 10\times$ (Fig. 2). Thus, the standby power can be significant in comparison to the active power. It is also true that NFETs and PFETs have equal current drive when I_{off} 's are matched. Second, subthreshold operation is different from operation above threshold in that delay depends exponentially on V_{dd} and not linearly. Another point is that the capacitive loading is primarily due to junction, wire, and gate fringe capacitances because gate-to-inversion layer capacitance is much smaller than for operation above threshold. This implies that parasitic capacitances play a more dominant role in determining delay and suggests that SOI may have an interesting advantage in this operation regime for its low parasitic capacitances and its steep sub- V_t slope. Parasitic resistances, on the other hand, are of much less concern than under normal operating conditions since the channel resistance is much higher. This is a significant advantage for high density scaling that increases interconnect resistances. Furthermore, overlap capacitance can be minimized even at the expense of series resistance. In conclusion, we have demonstrated sub-0.1fJ switching at 5ns stage delays with subthreshold CMOS logic using well regulators to accurately match NFET and PFET currents. This power performance point has potential to carry us well into the teragate scale integration.

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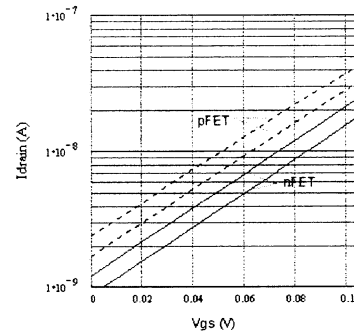
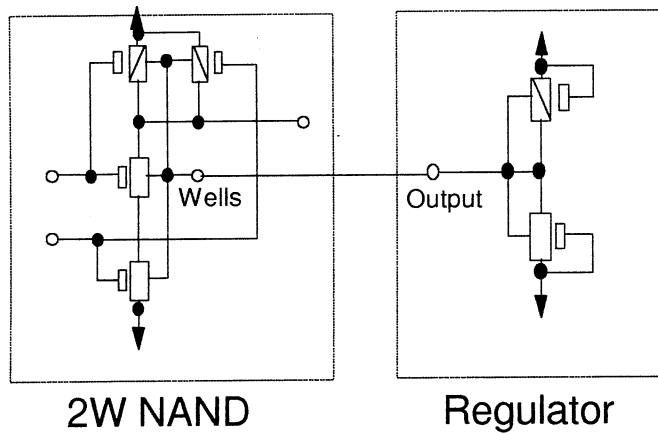


Figure 2: Id-Vg of nFET and pFET with W/L= 0.5um / 0.15um used in this work. Substrate/well biases of 0V and 0.1V are applied. Vd=0.25V.

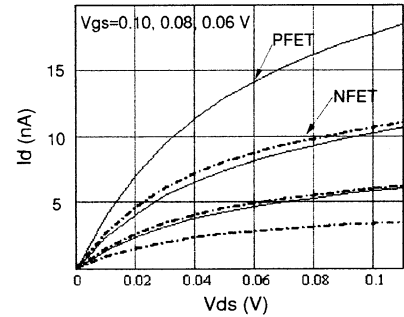


Figure 3: Id-Vd output characteristics of 0.5um / 0.15um PFET and NFET for 100 mV power supply.

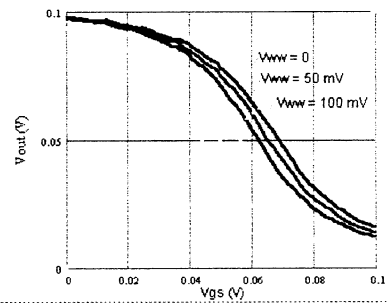


Figure 5: Input/Output transfer characteristics for 2W NAND with Vdd=100mV. Vwell is varied. Vn=Wp=0.6um. Note the imbalance.

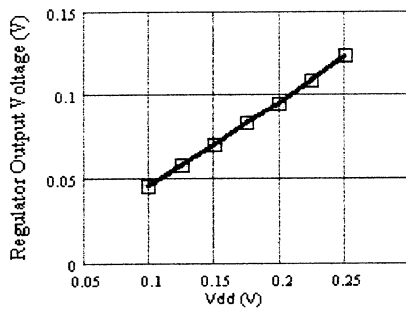


Figure 4: Regulator Output Voltage vs. Vdd. Output biases FET wells to match NFET and PFET Sub-Vt current drives.

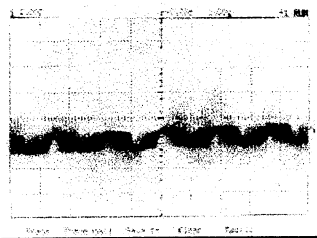


Figure 6: Output driver waveform of a 2-input NAND ring oscillator running 200 mV.

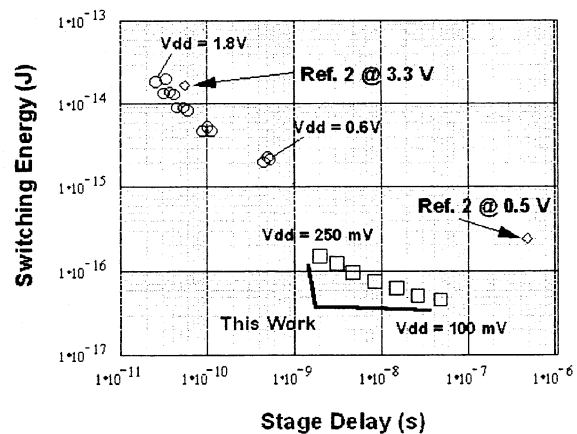


Figure 7: Inverter Switching Energy per stage vs Stage Delay shows energy per operation below 0.1fJ.

A Sub-40nm Body Thickness N-type FinFET

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Introduction.

We experimentally demonstrate near-ideal subthreshold behavior of fully-depleted fin-style double-gate N-type MOSFETs and the best measured transconductance $G_m\text{-sat} = 72 \text{ S/m}$ ($>400\text{S/m}$ intrinsic) for sub-40nm n-type FinFETs reported. This silicon NFET exhibits experimental ideality $n = 1.13$, in good agreement with the deviation from unity expected due only to source/drain coupling. These results comprise the best behavior for 100 nm-scale double-gate NFETs in terms of channel subthreshold characteristics and gate leakage observed experimentally to date. Hisamoto et al. [1] introduced experimental results on double-gate silicon MOSFETs in which the channel is formed by etching single-crystal silicon to leave a vertical 'fin' standing, forming a gate which wraps around the fin, forming source and drain regions on the two ends of the fin. This basic idea was further refined to sub-50 nm N-type MOSFETs [2] and then extended to sub-50 nm P-type MOSFETs [3]. Using simplified fabrication techniques, we demonstrate improved behavior, from an intrinsic channel point of view, of the nFET work [2], using conventional CMOS integration on n-type FinFETs.

Experimental Details.

SIMOX starting wafers with 160nm 5E15 p-type silicon on 370nm BOX are patterned with DUV lithography to form an oxide hard mask. This hard mask is further trimmed to the desired width and used to mask the etch of silicon fins. Due to the orientation of the fin mask with respect to that of the starting wafers, the resulting fin sidewalls, the inversion surfaces, are in the $\langle 110 \rangle$ plane, enabling simplified physical analysis. This is expected to result in lower mobility for electrons than that expected with $\langle 100 \rangle$ planes [4]. A sacrificial oxide was grown and stripped from the fin to remove RIE polymers and damage, and to further thin the fin. A conventional thermal oxidation was used to form gate insulator on both sides of the fin. This oxidation was nominally produces a 2.2nm physical oxide thickness when grown on a $\langle 100 \rangle$ plane. 75nm intrinsic polysilicon was deposited over the fin, gate oxide and remaining hard mask and then patterned to produce the gate electrode resulting in the FinFET in Fig. 1. The gate definition was performed using a standard hard-mask process with 248nm DUV lithography. The hard mask fin-etch scheme leaves well-defined source and drain regions where the gate conductor can be removed without destroying the fin and also a well-controlled gate edge, as is further demonstrated by the array of FinFETs seen in Fig. 2. To obtain uniform overlap of the source and drain by the gate, a quad As_2 extension implant is used 7° off vertical and oriented at 45° off axis from the fin and the gate (Fig 3). These extension implants serve to dope the gate electrode N+. A 900°C 3.5nm thermal oxide was grown followed by 975°C RTA and 400°C surface-state anneal in H_2 .

Electrical Results.

Probing was conducted at extension silicon probe (no deep implants or silicide) to investigate the subthreshold behavior of sub-40nm thick fins with full depletion. Fig. 4, a plot of source current as a function of gate voltage for drain voltages of 0.05V and 1.5V on a $L_{\text{gate}}=100\text{nm}$, $T_{\text{fin}}=38\text{nm}$ MOSFET, brings out three features immediately. Firstly, the linear-mode V_t is -260mV, in good agreement with simple long-channel expectations given by $V_t = \Phi_{\text{ms}} - \Psi_{\text{N+}} \sim -0.3\text{V}$. Secondly, despite the fact that the body is nearly intrinsic, the DIBL is well behaved at only 57mV/V. Third, the subthreshold swing S , of 68mV/decade at 25C yields ideality, $n=1.13$. In addition, unlike many double-gate structures, we obtain gate leakages consistent with that expected solely due to tunnel currents through the oxide. Based on these tunnel currents, we infer the physical oxide thickness to be 2.3nm. Fig. 6 shows the drain output characteristics of this FinFET exhibiting severe schottky contact type behavior due to direct probe of surface pads of lightly doped silicon. We use the probe-limited value of the $V_{\text{ds}}=50\text{mV}$ source current (Fig 7.) to extract a $G_m\text{-sat} > 400 \text{ S/m}$ from measured value of 72 S/m for this nFET (Fig. 8).

These results represent the best-behaved sub-100nm fin N-type MOSFET to date. The swing is in line with 'ideal' expectations given the DIBL, since a simple capacitive model (Fig. 5) predicts the relation between DIBL and swing of: $S = (kT/Q_e) * 1/(1 + \text{DIBL} * 2)$, which gives a predicted ideality of 1.11 vs. observed of 1.13. Hence this n-type FinFET is behaving in excellent agreement with the expected 'electrostatic' behavior of fully depleted double gate MOSFETs in the sub-100nm gate length regime.

Discussion.

Our ability to directly quantify the super-threshold behavior (e.g. G_{msat} , I_{dsat}) has been limited by lack of good contacts. Prior to the conference, the authors expect to have completed a spacers, deep S/D implants, silicide and metalization to improve the series resistance and characterize the device to further demonstrate the superthreshold properties.

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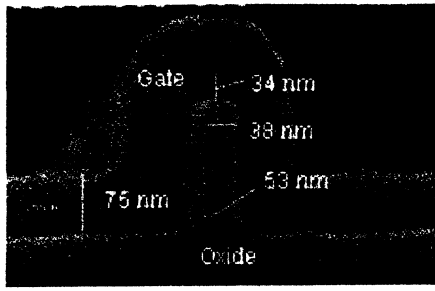


Figure 1: SEM view of $T_{\text{body}}=38\text{nm}$, $L_{\text{gate}}=140\text{nm}$ n-type FinFET. Channel width = $2 \times \text{fin height} = 2 \times 0.12 \mu\text{m} = 0.24 \mu\text{m}$.



Figure 2: SEM view of field of FinFETs illustrating structure.

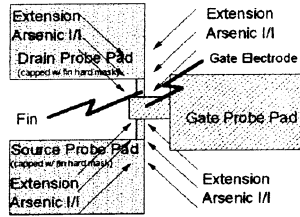


Figure 3: Source/Drain Ion-Implant angles from top down view. Implants are inclined 7 degrees from vertical axis.

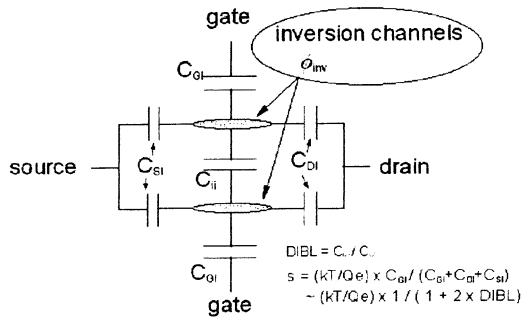


Figure 5: Relationship among subthreshold swing and DIBL expected for a fully-depleted double-gate MOSFET.

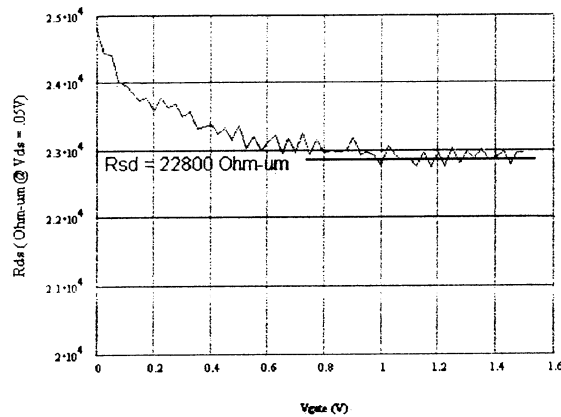


Figure 7: R_{sd} vs gate drive for $V_{\text{ds}}=0.05\text{V}$. Linear-mode device is current limited at $R_{\text{ext}} \sim 23800 \text{ Ohm-um}$.

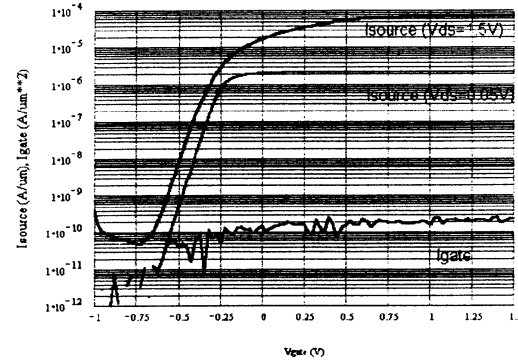


Figure 4: Source and gate currents vs. gate voltage for $L_{\text{gate}}=140\text{nm}$ n-type FinFET. I_{gate} was measured at $V_{\text{ds}}=0.05\text{V}$.

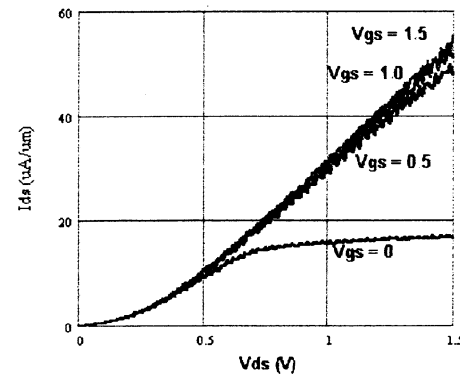


Figure 6: Drain output characteristic shows severe voltage drop from direct (W) probe to silicon.

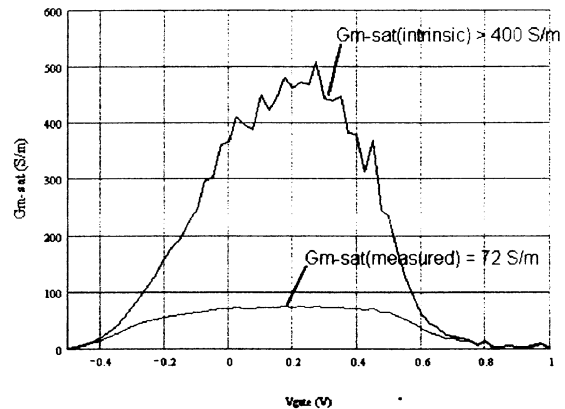


Figure 8: $G_{\text{m-sat}}$ as measured and as corrected to intrinsic based on R_{sd} measurements in Fig. 7.

Quasi-Planar NMOS FinFETs with Sub-100nm Gate Lengths

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Introduction

Double-gate MOSFETs alleviate short channel effects and allow for more aggressive device scaling. Simulations have shown that scaling double-gated devices can reach 10nm [1,2]. In the past, process complexity has prevented serious development of a scalable double-gate device. In 1998, Hisamoto et al introduced a FinFET process that provided a method to fabricate devices with promising performance and scalability [3]. Using a single poly layer across a silicon fin to form both gates in the double-gate structure, the FinFET benefits from having equally-sized, self-aligned gates.

PMOS FinFETs were subsequently fabricated and showed excellent I_{on} and I_{off} [4]. Both reports used a similar process flow. In this work, we have revamped the FinFET process flow to make it simpler. This improved process flow still has the self-aligned double-gate advantage without suffering from extra gate-to-drain overlap capacitance.

Device Fabrication

The simplified FinFET device is illustrated in Figures 1 & 2. SOI wafers were thermally oxidized to provide 50nm silicon films with a 50nm hard mask oxide. Phosphorous implants were used to provide n-type channel doping in the range of $1e15cm^{-3}$ to $1e18cm^{-3}$.

The gate stack included a 500Å oxide hard mask on top of 2400Å in-situ boron-doped $Si_{0.5}Ge_{0.5}$ on 18Å SiO_2 gate oxide. Si_xGe_{1-x} was used to engineer V_t [2]. E-beam lithography was used to define the critical fin and gate dimensions down to 50nm. Figure 3 shows a top view SEM of a 50nm gate across a 50nm fin prior to spacer formation. The gate-drain misalignment tolerance for this run was 100nm but tighter alignment can be achieved with improved e-beam stepping software.

After a spacer of 375Å nitride on 100Å oxide was formed, arsenic was implanted to form the source and drain. A 15 hour 600C anneal was used to recrystallize any portion of the silicon fin amorphized by the heavy As implant. This was followed by a short 900C activation anneal and a 450C forming gas anneal.

Results

Device results for a 90nm gate across a 80nm fin are shown in Figures 4 & 5. The width of a FinFET device is $2 \times (\text{fin height}) \times (\text{number of fins})$. All devices in this work use a single fin so W is 100nm. Larger W devices are possible with multiple fins [3,4]. In Figure 4, using $V_g - V_t = 1V$ and $V_d = 1V$ we evaluate $I_{dsat} \sim 375\mu A/\mu m$. An alternative, more aggressive definition of W as simply the fin height would effectively double the reported current to $750\mu A/\mu m$. Despite using n-type channel doping in the range of $1e15cm^{-3}$ to $1e18cm^{-3}$, the NMOS V_t remained $\sim 1V$, higher than expected for a p-type $Si_{0.5}Ge_{0.5}$ gate. This insensitivity to channel doping shows the importance of the gate workfunction for scaling double-gate devices.

FinFET turnoff characteristics depend heavily on the fin width as shown in Figure 6. This data suggests that L_{gate} , in this case study, can be scaled down to 1.3 times W_{fin} without suffering from excessive leakage current, even with n-type channel doping. The minimum W_{fin} fabricated for this work is 50nm so $L_{min} \sim 65nm$ as shown in Figures 7 & 8. Such de-coupling of short channel effects and channel doping is critical for scaling MOSFETs down to 10nm.

Conclusion

A simplified FinFET process was developed and first NMOS results are shown. Data suggest that FinFET scaling is very promising. Improved current for future devices can be realized by lowering V_t with improved gate workfunction engineering and with thinner T_{ox} . Further improvements can be made by using a raised S/D [5-6] or silicided S/D.

Acknowledgement

This research is sponsored by DARPA AME Program under Contract N66001-97-1-8910 and by SRC under Contract 2000-NJ-850.

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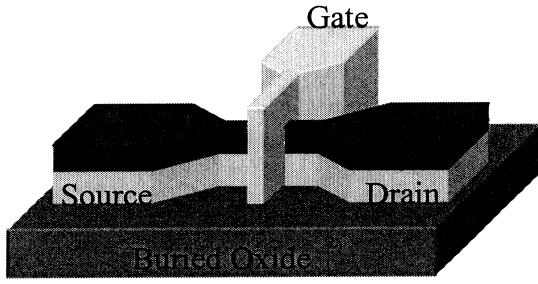


Fig. 1. 3D view of FinFET using simplified process flow.

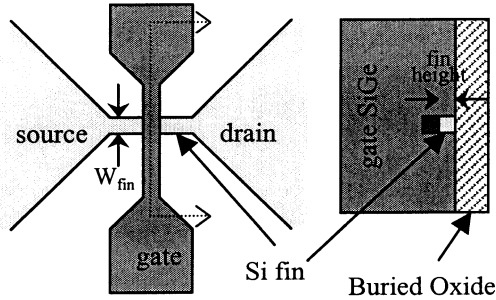


Fig. 2. FinFET layout and cross sectional view. Because the gate modulates the current on both sides of the fin, the transistor W is considered to be twice the fin height.

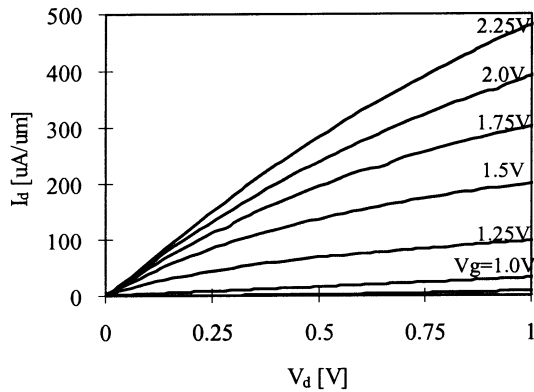


Fig. 4. I_d - V_d curves for a 90nm gate over a 80nm fin. $V_t \sim 0.9V$ so $I_d(V_g - V_t = 1V; V_d = 1V) \sim 375uA/um$ or $750uA/um$ if W is defined as one fin height.

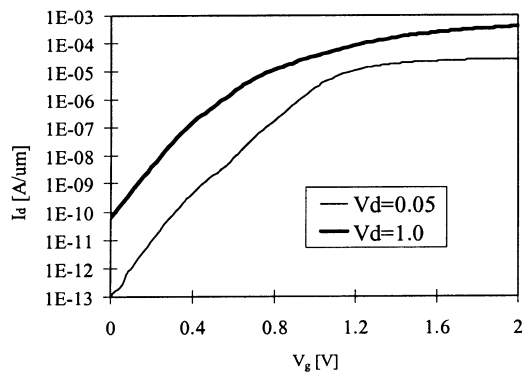


Fig. 5. I_d - V_g curves for a 90nm long gate over a 80nm fin.

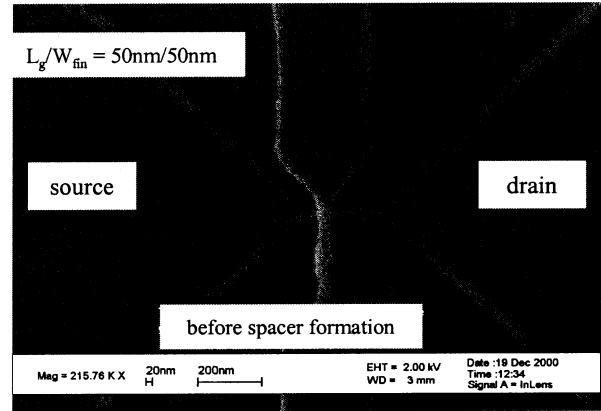


Fig. 3. Top view SEM after gate definition for 50nm gate and 50nm fin.

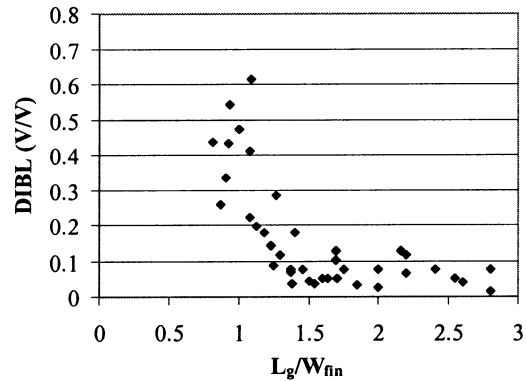


Fig. 6. DIBL is the shift between $V_d = 50mV$ and $V_d = 1V$ evaluated at $1e-8A/um$. The gate should be at least 1.3 times the width of the fin to provide adequate turnoff.

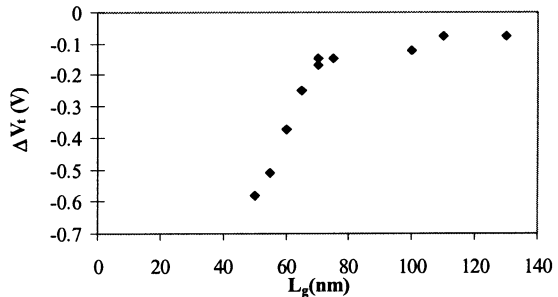


Fig. 7. V_t rolloff for $W_{fin} = 50nm$. $L_{min} \sim 65nm$

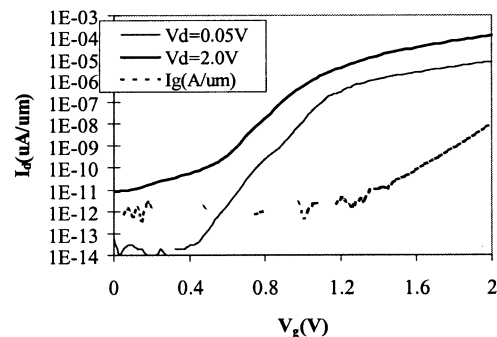


Fig. 8. I_d - V_g curves for $L = 65nm$, $W_{fin} = 50nm$

High Performance of Planar Double Gate MOSFETs with Thin Backgate Dielectrics

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Abstract

Planar double gate CMOS devices with thin silicon channels and electrically separate polysilicon top and bottom gates are fabricated. NFETs with $L_{\text{design}} = 175\text{nm}$ and $1.3\text{ mA}/\mu\text{m}$ and PFETs with $L_{\text{design}} = 125\text{nm}$ and $400\text{ }\mu\text{A}/\mu\text{m}$ are achieved at $V_{\text{dd}} = 1.2\text{V}$. To our knowledge, this is the largest current yet achieved in double gate NMOS devices. Electrical results show a high quality backgate dielectric, improvement of SCE using the backgate, and the importance of reducing external resistance in short channel devices.

Introduction

Double gate MOSFET devices are expected to extend MOS device scaling [1]. Simulations show that double gate and ground plane MOS devices are more effective than single gate SOI or bulk silicon devices for controlling threshold voltage and short-channel effects (SCE), and are expected to have excellent rolloff characteristics, improved subthreshold slopes, double the drive current of a single-gate device, and enable a lower minimum effective gate length for the same gate oxide thickness [2]. Here, a simple process for fabricating symmetric NFET and asymmetric PFET devices is developed. The devices show improved SCE, subthreshold swing, and current drive as predicted for double gate mode.

Device Fabrication

Fig. 1 shows the structure of simplified double gate MOSFET devices fabricated to study double gate operation in the DC mode. Starting substrates consist of a thin silicon channel layer (45-55 nm thick), with blanket layers of thin backgate dielectric (3-4 nm), n^+ polysilicon backgate (350 nm) and buried oxide (400 nm) materials underneath. Substrates are prepared by wafer bonding, starting with an SOI wafer, growing and depositing the desired films, polishing, bonding the wafer to a handle wafer, annealing, then grinding and etching away the backside and buried oxide of the original SOI wafer, similar to a method described previously [3]. The silicon channel was thinned by oxidation. Device processing follows a standard CMOS flow, including trench isolation, 2.5 nm gate oxide, n^+ / p^+ polysilicon gates, separate source/drain extension and contact region implants, and thin cobalt silicide. The active device channel is undoped in the NFET; the PFET has strong halos. For the front and back device channels to have similar L_{eff} , implant and anneal cycles for the source/drain extensions and contacts were designed to extend from the silicon surface to back interface, but with minimal lateral diffusion or backgate oxide damage. A cross section is shown in Fig. 2. As the n^+ polysilicon backgate is a blanket layer under the device active region, they are useful mainly to study DC double gate operation.

Device Performance

Fig. 3 shows front and back gate dielectric leakage currents. The front gate oxide exhibits about $1\text{mA}/\text{cm}^2$ leakage current at 1.2V, but the slightly thicker backgate dielectric leakage is below the detection limit. This is an especially positive result, as the backgate dielectric was present during the very long (> 2 hour), high temperature wafer bonding

anneal, which might be expected to cause damage to it [4].

Long channel (10 μm) NFET and PFET devices exhibit ideal double gate operation in Fig. 4: saturation current is increased 130% in the NFET in double gate mode, 97% in the PFET. Subthreshold swing is ideal in double gate mode, 60 mV/dec in both devices (Fig. 5), better than front or back gate operation alone (Fig. 6). In Fig. 5a, the undoped channel of the single gate NFET is punched through, but can be turned off in double-gate mode. This shows how effectively channel geometry can control short channel effects. In Fig. 5b, strong halos in the PFET control the short-channel effects, so there is only slight improvement in the subthreshold characteristics of the double-gate devices.

In short channel devices, performance enhancements are not so large, but absolute device performance is very good. In Fig. 7, an $L_{\text{design}} = 175\text{ nm}$ NFET has saturation current about $1.3\text{ mA}/\mu\text{m}$ at $V_{\text{gs}} = 1.2\text{V}$, the best double gate NFET performance reported to date. Double gate mode still exhibits improved DIBL and subthreshold swing, but the drive current enhancement is only 54%. The increased importance of series resistance in short channel devices reduces the enhancement from the long channel case. Series resistance is high due to the current of two channels being driven through a single set of contacts, a thinning of the channel towards the source and drain (Fig. 2), and a larger L_{eff} in the back channel, due to the difficulty of optimizing source/drain extension profiles there. This illustrates the importance of ensuring silicided contacts have access to both top and bottom channels in a double gate device technology.

Resistance plays an even larger role in the PFET, but is not entirely due to the source/drain region. Since the two gates are asymmetric, the bottom gate is not completely turned on in the double gate mode, and the backgate current path is never fully inverted. Even so, the PFET currents are noteworthy: Fig. 8 shows IV characteristics of a $L_{\text{design}} = 125\text{ nm}$ PFET, with $400\text{ }\mu\text{A}/\mu\text{m}$ saturation current at $V_{\text{gs}} = 1.2\text{V}$, a 25% performance enhancement over single gate operation.

Conclusion

Double gate MOSFETs are demonstrated with drive current enhancements more than 100% in long channel devices, and 25-54% in short channel devices, limited by series resistance. The best double gate NFET performance to date is reported, and excellent backgate dielectric performance is achieved in a planar device. Double gate mode is seen to improve SCE, subthreshold swing and DIBL.

Acknowledgments

The authors thank Paul Solomon, John Warlaumont, Mark Hakey, John Dukovic, Dave Seeger, Lijuan Huang, and the IBM ASTL Facility for generous support. This work was a result of DARPA contract N6601-97-1-8908.

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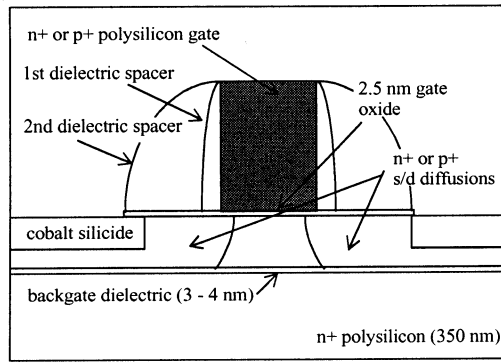


Fig. 1. Schematic cross section of simplified double gate device

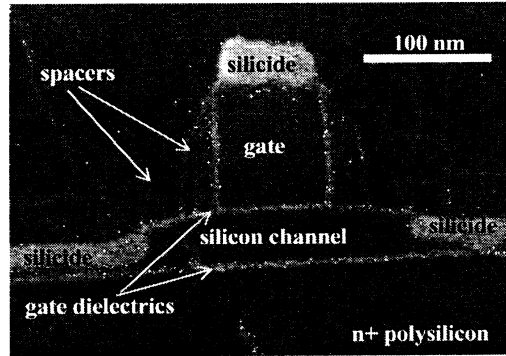


Fig. 2. SEM cross section of fabricated device.

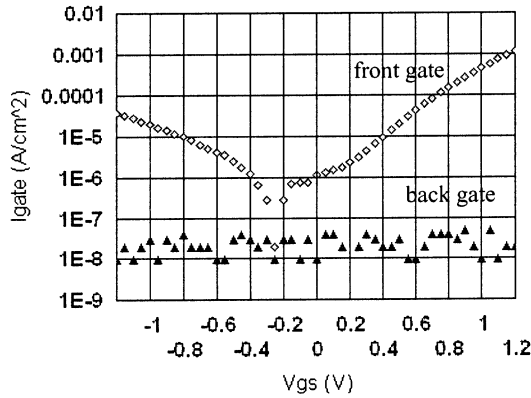


Fig. 3. Front and back gate leakage of large area (10 μm square) device.

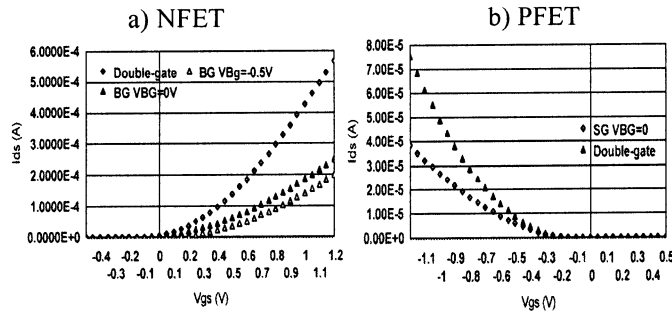


Fig. 4. I_d - V_g characteristics of long channel (10 μm x 10 μm) a) symmetric NFET and b) asymmetric PFET devices. NFET shows current enhancement of 130% and PFET shows enhancement of 97%. $V_{ds}=1.2\text{V}$.

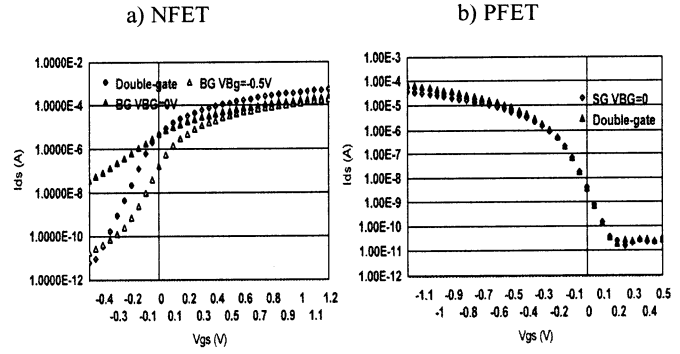


Fig. 5. Subthreshold characteristics of long channel a) symmetric NFET and b) asymmetric PFET. Devices are 10 μm x 10 μm with $V_{ds} = 1.2\text{V}$. In Fig. 5a, due to the low V_t of the NFET device, a clearer comparison between single and double gate modes is achieved by applying -500mV to turn off the backgate.

	NFET	PFET
front gate	77	73
back gate	84	85
double gate	60	60

Fig. 6. Subthreshold swing of devices under front gate, back gate, or double gate operation.

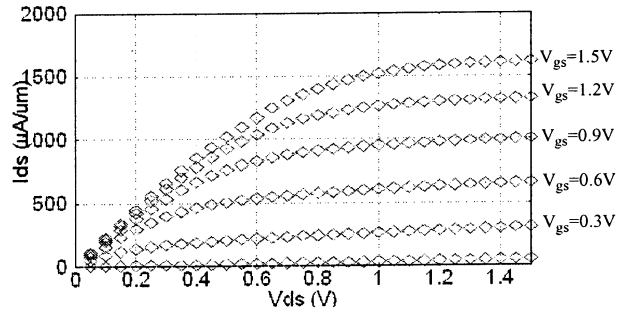


Fig. 7. IV characteristic of $L_{\text{design}}=175\text{nm}$ NFET.

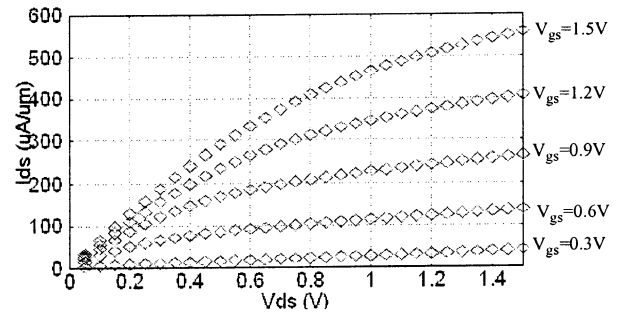


Fig. 8. IV characteristic of $L_{\text{design}}=125\text{nm}$ PFET.

Si_{1-x}Ge_x Channel Vertical PMOSFET with Asymmetric Ge Profile

Xiangdong Chen, Qiqing Ouyang, Sankaran Kartik Jayanarayanan, Freek E. Prins and Sanjay Banerjee

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Strained Si_{1-x}Ge_x has attracted much attention recently because of the hole mobility improvement in the strained layer, leading to PMOSFET drive current improvement[1]. However, the short channel effects and off-state leakage current are also degraded due to the smaller bandgap in the Si_{1-x}Ge_x layer. The channel doping next to the source and drain junction can be raised to reduce the short channel effects and off-state leakage current. A lateral asymmetric channel doping structure with high doping at source and low doping at the drain has also been proposed to increase the electric field at the source side and achieve both high drive current and good short channel performance [2]. In this study, we have fabricated a vertical PMOSFET with an asymmetric Si/Si_{1-x}Ge_x channel (Figure1). On the source side, the channel is made of Si, so the short channel performance is not degraded compared with a Si device. The rest of the channel is made of strained Si_{1-x}Ge_x and we still can take advantage of the high hole mobility in the strained Si_{1-x}Ge_x layer. The energy step (figure 2) in the channel increases the lateral electric field near the source and helps with carrier injection from the source to the channel[3].

Ultra-high vacuum chemical vapor deposition (UHV-CVD) was used to grow the device layers with *in situ* doping. Figure 3 shows the secondary ion mass spectroscopy (SIMS) profiles along the channel after the processing. The channel is made of Si (~20nm) and Si_{0.84}Ge_{0.16} (~80nm). Reactive ion etch (RIE) was employed to etch the mesa after the epi-growth. The size of the mesa is 20 μm $\times$ 20 μm . An 8 nm thick intrinsic Si cap was grown around the pillar for gate oxide growth. Gate oxidation was performed at 750°C in wet O₂. The oxide thickness is 5nm, as measured on a planar (100) Si control wafer oxidized simultaneously with the device wafers.

The top p+ layer is used as drain in the “normal” mode. In the “reverse” mode, the source and drain contacts are interchanged. Figure 4 shows the subthreshold characteristics of the asymmetric device measured in the normal and reverse mode. Although, the threshold voltage (V_T) in the normal mode is 70mV higher than that in the reverse mode, the drive current is still larger in the normal mode at the same gate voltage. The device in the reverse mode shows larger drain induced barrier lowering (DIBL) than that in the normal mode. The off-state leakage current in the reverse mode is larger than that in the normal mode. In figure 5, the device shows punchthrough characteristics in the reverse mode at $V_{DS} = -2.1\text{V}$. The output characteristics (figure 5) also show that the device has a smaller breakdown voltage in the reverse mode. These observations indicate that the smaller source and channel barrier in the strained Si_{1-x}Ge_x layer can degrade the short channel performance and increase the off-state leakage current, while, in the normal mode, the source-channel junction is made in Si, and the off-state device performance is not degraded.

At the channel length below 100nm, velocity overshoot takes place over a portion of the device [4], which is confirmed by hydrodynamic (HD) simulations. When the carrier velocity near the drain can reach rather high values in the high-field region near the drain, MOSFET currents are mainly controlled by the average velocity near the source end of the channel, and the inversion charge density $Q_i = C_{ox}(V_G - V_T)$, independent of the drain voltage. The carrier velocity near the source is determined by the electric field and carrier mobility in the channel region near the source. The mobility of the holes in the source end of the channel of the asymmetric device is low compared with a PMOSFET with strained Si_{1-x}Ge_x everywhere in the channel. But this can be compensated by the kinetic energy enhancement due to the valence band offset at the source end in the asymmetric Si/Si_{1-x}Ge_x device. Figure 6 shows the electric field along the channel of the asymmetric device operated in the normal and reverse mode and for a Si control device. In the normal mode, due to the potential energy step in the channel, the device shows a larger field gradient near the source end of the channel (inset of figure 6). Especially at the step, where there is a jump in the electric field, the holes injected from the source into the channel will experience a velocity enhancement near the source end. At the same gate drive, the drive current for the asymmetric Si/Si_{1-x}Ge_x device is higher than the Si control device (figure 7). However, the off-state characteristics are almost the same for the two devices.

This work was supported in part by the Semiconductor Research Corporation, National Science Foundation-Science and Technology Center, and Department of Defense-Multi-Disciplinary University Research Initiative.

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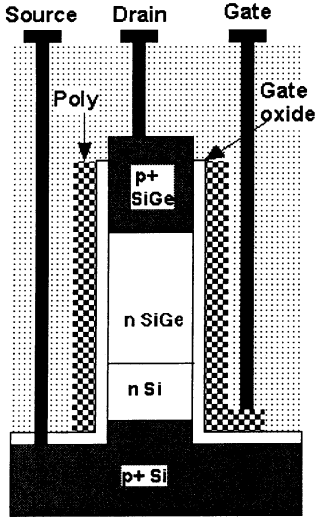


Figure 1. Schematic cross section of vertical asymmetric $\text{Si}_{1-x}\text{Ge}_x$ channel PMOSFET

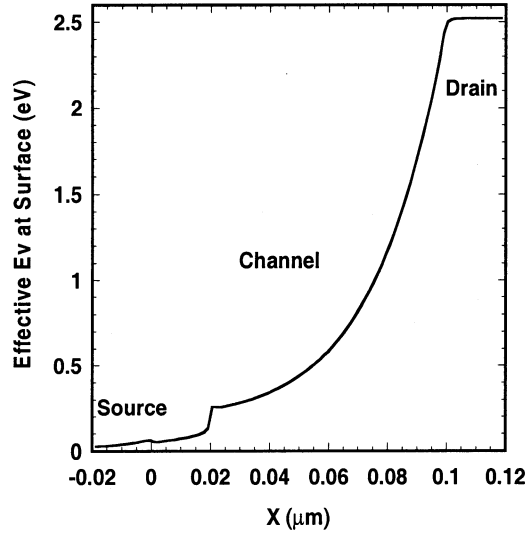


Figure 2. Energy band diagram of the device operated at $V_{DS}=V_G=-2\text{V}$.

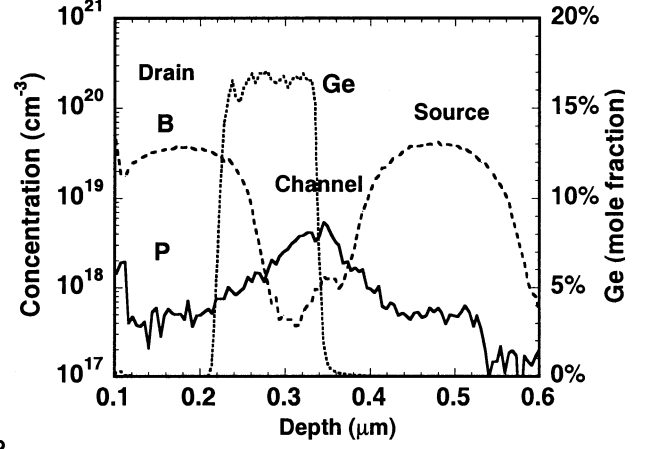


Figure 3. SIMS profile along the channel for the vertical asymmetric $\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ channel PMOSFET.

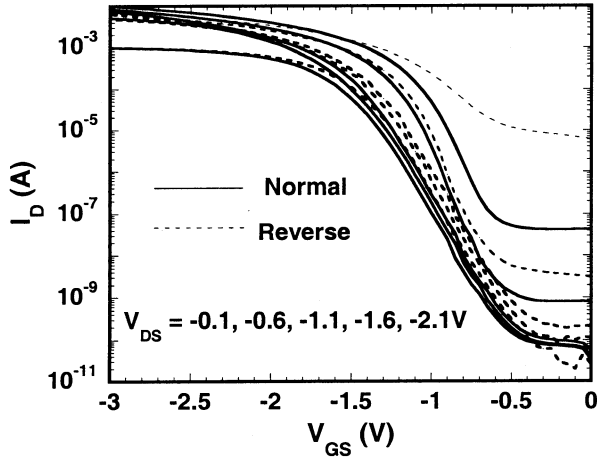


Figure 4. Subthreshold characteristics for the asymmetric $\text{Si}_{1-x}\text{Ge}_x$ channel PMOSFET measured in the normal and reverse mode.

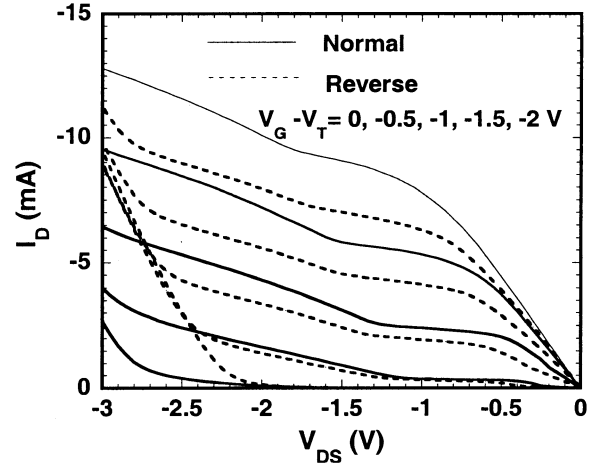


Figure 5. Output characteristics for the asymmetric $\text{Si}_{1-x}\text{Ge}_x$ channel PMOSFET measured in the normal and reverse mode.

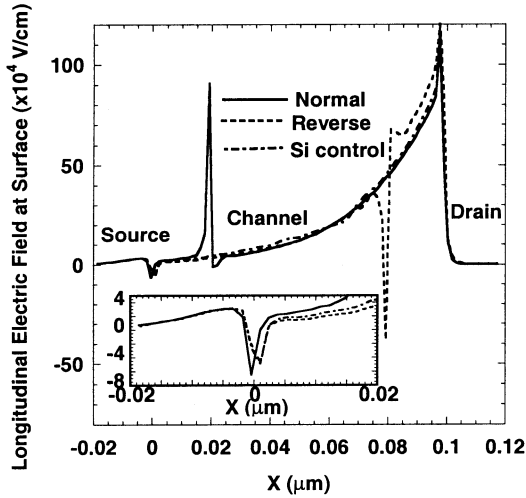


Figure 6. Longitudinal electric field along the channel at $V_{DS}=V_G=-2\text{V}$.

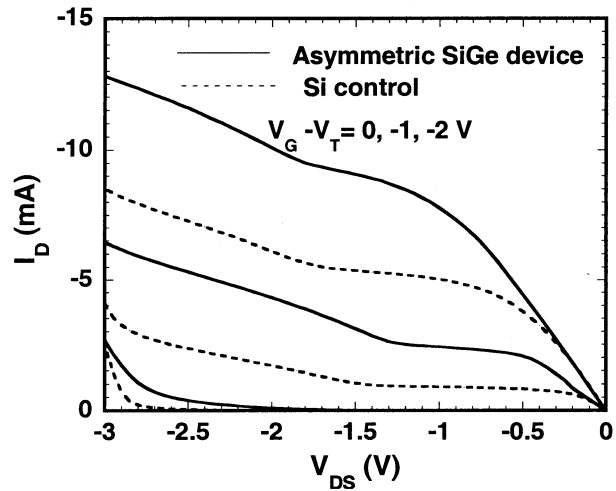


Figure 7. Output characteristics for the asymmetric $\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ channel PMOSFET and the Si control device.

III-V Devices and Sources

MONDAY PM, JUNE 25TH, 2001

Session Organizer: Colombo Bolognesi, Simon Fraser University

2:00 PM, II.B.-1 Invited

Optical Interconnections to Silicon Integrated Circuits: *David Miller*¹; ¹Stanford University, Stanford, CA 94305 USA

2:30 PM, II.B.-2

Temperature-Dependent Large Signal Modulation and Auger Recombination in $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ Quantum-Dot Lasers: *S. Ghosh*¹; P. Bhattacharya¹; E. Stoner¹; H. Jiang²; S. Nuttinck³; J. Singh¹; J. Laskar³; ¹University of Michigan, Solid State Electronics Laboratory, Department of Electrical Engineering and Computer Science, Ann Arbor, MI 48109 USA; ²Broadcom Corporation, 16215 Alton Parkway, Irvine, CA 92619 USA; ³Georgia Institute of Technology, Microelectronics Research Center, Department of Electrical Engineering, Atlanta, GA 30332 USA

2:50 PM, II.B.-3

ZnSe-Based Laser Diodes for the 560 nm Spectral Region: *M. Klude*¹; G. Alexe¹; C. Kruse¹; T. Passow¹; D. Hommel¹; ¹Institut für Festkörperphysik, Universität Bremen, 28359 Bremen, Germany

3:10 PM, II.B.-4

NpN InGaAsN-Based Heterojunction Bipolar Transistors with $f_{\text{max}}=60\text{GHz}$: *C. Monier*¹; A. G. Baca¹; F. Newman²; P. C. Chang¹; N. Y. Li²; H. Q. Hou²; E. Armour³; R. Stall³; ¹Sandia National Laboratories, Albuquerque, NM 87185 USA; ²Emcore Corporation, Emcore Photovoltaics, Albuquerque, NM 87123 USA; ³Emcore Corporation, Sommerset, NJ 08873 USA

3:30 PM Break

3:50 PM, II.B.-5

Noise Characteristics of Highly Strained InGaP/InGaAs p-HEMTs Grown on Patterned Substrates by Using Compound-Source MBE: *Jeong Hoon Kim*¹; Sung-June Jo¹; Jong-In Song¹; ¹K-JIST, Department of Information and Communications, 1 Oryong-dong Buk-gu, Kwangju, 500-712 Korea

4:10 PM, II.B.-6

A Flip-Flop Based on Monolithic Integration of InAs/AlSb/GaSb RITDs and InAlAs/InGaAs/InP HEMTs: *P. Fay*¹; Y. Xu¹; G. H. Bernstein¹; A. Gonzalez²; P. Mazumder²; D. H. Chow³; J. N. Schulman³; ¹University of Notre Dame, Department of Electrical Engineering, Notre Dame, IN 46556 USA; ²University of Michigan, Department of Electrical Engineering and Computer Science, Ann Arbor, MI 48109 USA; ³HRL Laboratories, Malibu, CA 90265 USA

4:30 PM, II.B.-7

Monolithic Integration of InAlAs/InGaAs Enhancement and Depletion (E/D)-Mode Metamorphic HEMTs on GaAs Substrate: *D. C. Dumka*¹; W. E. Hoke²; P. J. Lemonias²; R. Schwindt¹; G. Cueva¹; I. Adesida¹; ¹University of Illinois at Urbana-Champaign, Microelectronics Laboratory, Department of Electrical and Computer Engineering, 208 Wright Street, Urbana, IL 61801 USA; ²Raytheon RF Components, 362 Lowell Street, Andover, MA 01810 USA

Optical interconnects to silicon CMOS

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We currently use optics for nearly all long distance communications, and it is used increasingly at shorter distances. Optical data links are used inside large electronic systems to connect between frames of equipment and to connect to peripheral devices, such as storage. The concept of using optical interconnects to or on the silicon chip itself is, however, still a radical one. In this talk I will discuss why would we propose to make optical interconnects to the chip and how we might do so.

It is important first to understand some of the problems of electrical wiring, and the potential benefits of optics.[1] One key issue is the scaling of the number of bits per second that an electrical connection can support. With electrical wires, if a given wire cannot handle the data rate we need, we can make the wire thicker, reducing the resistance of the wire. But once we have filled all available space with wiring, we can no longer take that approach. Interconnections within high-performance electrical machines typically do fill much or all of the conveniently available space. In fact, once all space is filled with wiring, a simple scaling argument shows the size of the system makes no difference to the capacity of the electrical interconnect.

For a simple line limited by its resistance R and capacitance C , essentially we can send about one bit for every time RC . Most lines on silicon chips behave this way. Surprisingly, inductive-capacitive (LC) lines, such as coaxial lines or other impedance-matched lines used for high-speed signals, obey the same kind of scaling relation for reasons also related to their resistance. Even more surprisingly, per unit cross-sectional area of lines, for simple on-off signaling, such LC lines actually can carry less information than the RC lines, so changing to impedance-matched LC lines actually makes the scaling problem worse. (For high-speed digital systems, all signal lines behave as LC lines, except for lines on chips. The longer lines on chips are now also unavoidably starting to change towards LC lines.)

The consequence of this scaling argument is that, once all the available space becomes filled with wiring, suddenly there is a problem at all length scales in the system. We cannot solve the problem by miniaturization. Hence the need to consider optical interconnects at very short distance may occur much sooner than we would have guessed

based on the previous progressive trend. Of course, optical interconnects avoid this scaling limit because their physics is completely different.

Interconnects on silicon chips are arguably the best electrical interconnects we have, in terms of both performance and cost. Beyond 2006, the Semiconductor Industry Association predicts [2] that there is no known physical solution that allows interconnects at the chip level to continue to scale to keep up with the speed and integration level of the transistors on the chip. This scaling barrier discussed above is the underlying reason why even those on-chip interconnects themselves are starting to run into serious limits.

There are even greater problems for off-chip interconnects than on-chip ones. It is possible to break long, on-chip interconnects up using on-chip repeater amplifiers, but that approach is very inconvenient off of the chip. Consequently, off-chip interconnects are particularly attractive first implementation of optical interconnects to silicon chips.

Optical interconnects are interesting for many reasons other than this scaling argument.[3] They are immune to electromagnetic interference and crosstalk, they provide voltage isolation, they can have very low loss, and they allow use of free-space optics, imaging many light beams from one chip to another.

CMOS will be the dominant commodity electronics technology for the foreseeable future. Using CMOS therefore has the potential to reduce the cost of optical interconnects dramatically compared to expensive custom electronic approaches. The integration of the optoelectronic devices with CMOS can also improve the performance of the interconnect system substantially. Integrating the photodetectors with the CMOS can reduce their capacitance substantially compared to other approaches, such as wire bonding.

Historically, a great impediment to integrating optical interconnects with CMOS was the absence of suitable optical output devices. Fortunately there are now two devices that may be able to fill this role – quantum well modulator diodes, and vertical cavity surface emitting lasers (VCSELs). Of these, the quantum well diodes have been integrated in larger arrays, and have seen more systems work. They have the disadvantage that they need



Fig. 1. Array of quantum well modulator diodes bonded to a CMOS chip. The devices are bonded on 62.5 micron x 125 micron centers, for a total of 200 devices on this test chip. (Courtesy Gordon Keeler and Noah Helman, Stanford University)

an external laser source, but the advantages that the external source can have a well-controlled wavelength and can also be clocked to clock the interconnect itself.

Both the VCSEL and the quantum well modulator are made using III-V materials, such as GaAs and AlGaAs. As such, they require some integration technology to join them to the silicon circuits. The approach we have taken in our own work has been to solder-bond arrays of quantum well diodes to finished silicon CMOS chips, an approach pioneered at Bell Labs.[4] These devices can function both as detectors and as reflection modulators. They are intended to work with arrays of light beams perpendicular to the surface of the silicon chip. Fig. 1 shows a picture of bonded devices on a custom-designed CMOS chip. Using this technique, we have been able to demonstrate interconnection directly from one CMOS chip to another using light beams reflected off of modulators on one chip and received on photodiodes on another chip.

The use of optics for interconnects also opens up possibilities not available with electrical interconnect. It is possible to use a modulator-based system to remove skew and jitter from interconnects[5], for example, by reading the modulator out using short pulses. The timing of the signals then becomes that of the optical pulses, not the rising or falling edges of the electrical signal. Fig. 2 illustrates another possible concept in optical interconnects, which is to use wavelength division multiplexing to make a multichannel interconnect between chips over a single fiber.[6]

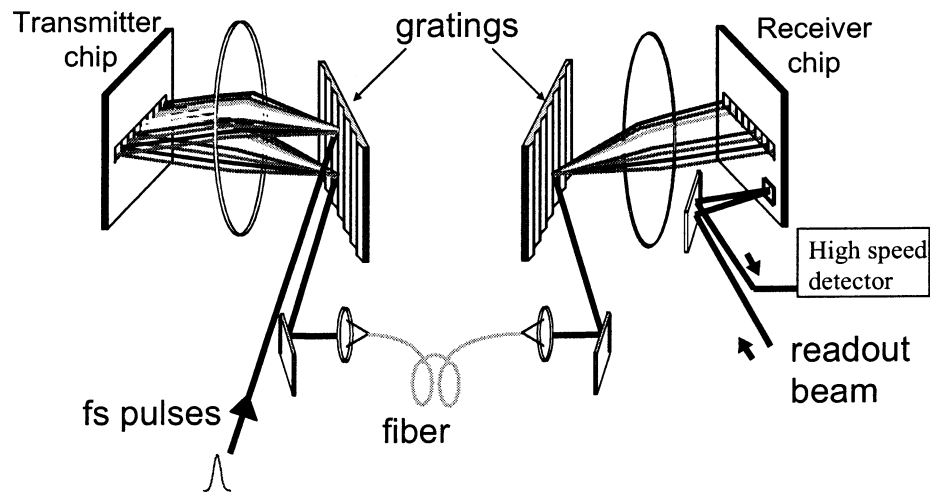


Fig. 2. Schematic illustration of a wavelength-division multiplexed optical interconnect experiment. A short pulse laser source generates a broad band of wavelengths. Separate bands of wavelengths are then individually modulated by the reflective quantum well modulators on the transmitter chip. The grating puts the wavelengths back together so they can be sent over one fiber to similar optics that then separates out the wavelengths so they can be individually read out by the receiver chip, giving a multichannel interconnect with only one laser and one fiber.[6]

Optical interconnects are the subject of much current research work, of which the work here is only a small example. For a collection of recent work in the field see Ref. [7].

Much work would remain to make the necessary technology a practical reality. There are some substantial device challenges. The photodetectors need to be well integrated with the electronics to minimize input capacitance. Such low capacitance (e.g., 10 fF) improves the system performance in several ways, reducing receiver power dissipation, improving receiver bandwidth, and reducing sensitivity to digital noise. Low voltages are required for the output devices (modulators or lasers), e.g., < 1 V swing, to match the power supply voltages of future generations of CMOS. The output devices must be fast (e.g., 10 GHz), and have low power consumption (e.g., < 1 mW). Devices that work at 1.5 microns wavelength would also be important to make the connection to optical networks, though short wavelength (e.g., 850 nm) devices could still be important useful for interconnects.

At this time, such optical interconnects to silicon CMOS are a research topic. When are they likely to be implemented? The problems with interconnects in high-performance electrical systems will become very severe later in this decade, and the need will be there for at least some substantial new approach to interconnects. Optics is arguably the only physical solution to such problems. Additionally, on about the same time frame, silicon CMOS will be running at clock rates (e.g., 10 GHz) that will make it fast enough to interface directly with optical channel bandwidths (e.g., 12.5 GHz wide spectral bands may soon be practically available for filling the entire optical fiber bandwidth). This creates the exciting prospect of the convergence of the silicon CMOS and optical networking communities – CMOS optical interconnects could become optical networks. Such a convergence is a speculative and radical goal, but the payoff could be substantial for both the electronics and photonics worlds.

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Temperature-Dependent Large Signal Modulation and Auger Recombination in $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ Quantum-Dot Lasers

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Self-organized $\text{In}(\text{Ga})\text{As}/\text{Ga}(\text{Al})\text{As}$ quantum dot interband lasers, operating at room temperature, have been extensively characterized in the past five years. Low threshold current, large modulation bandwidth, and low chirp and linewidth enhancement factor have been demonstrated in these devices.¹ Large-signal modulation of these lasers is important for optical communication applications. The non-radiative Auger recombination coefficients can also be measured from large signal modulation experiments by measuring the turn-on delay times of the laser output. The turn-on characteristics of the lasers have been theoretically investigated by Grundmann.² We report, to the best of our knowledge, the first experimental determination of the Auger coefficients in quantum dots.

$\text{In}_{0.4}\text{Ga}_{0.6}\text{As}/\text{GaAs}$ self-organized quantum dot separate confinement heterostructure (SCH) lasers were grown by MBE. The active region consists of five coupled quantum dot layers. Single-mode ridge waveguide lasers with ridge widths $3\mu\text{m}$, $5\mu\text{m}$, and $8\mu\text{m}$ and length $600\mu\text{m}$ were fabricated by standard photolithographic techniques and cleaving of the facets. The peak lasing wavelength was measured to be $1.06\mu\text{m}$ at room temperature, confirming lasing from ground state transitions. The lowest measured threshold current was 15 mA .

Large-signal modulation measurements were done at room temperature and lower temperatures in a closed cycle liquid helium cryostat with feedthru microwave probes and optical fiber. The lasers are pulse biased with a 10% duty cycle from $I=0$ to $I_{\text{final}}(> I_{\text{th}})$ with 100ps (20-80%) rise time electrical pulses. The output is detected with a 40 GHz InGaAs photodetector. The delay time between the electrical and optical signal is measured with a high-speed digital sampling oscilloscope, taking into account the delays due to the optical fiber, RF cables, the photodetector and low noise amplifier.

The temporal characteristics of the bias current pulse and the output optical pulse, with characteristic relaxation oscillations (RO) in the latter, are shown in Fig. 1. The RO frequency, ω_r , defines the intrinsic limit to the small-signal modulation frequency of the lasers. For example, from the data shown in Fig. 1, $\omega_r \cong 7\text{GHz}$, which agrees well with the result of small-signal bandwidth measurements.³ The measured turn-on delay times are plotted in Fig. 2 as a function of injection current density and temperature. The increase of delay time with increase in temperature, at a fixed current density, is shown more explicitly in Fig. 3. We believe this is a result of the increasing delay-time in the wetting layer and the fact that more dots of different size contribute to the lasing wavelength as the temperature increases.

To determine the Auger coefficients, the gain and spontaneous recombination rates are calculated with a 8-band $\mathbf{k}\cdot\mathbf{p}$ description of the bands and n_{th} is determined with a measured value of cavity loss using the multi-mode coupled rate equations. The inhomogeneous broadening is varied such that the experimental and calculated J_{th} are matched at each temperature. The Auger coefficient C_a is obtained by minimizing the RMS error between the theoretical and experimental delay times. A typical fit to the measured delay times at 300K is shown in Fig. 4 and the variation of C_a with temperature is shown in Fig. 5. Unlike bulk semiconductors, the value of C_a increases as the temperature decreases.

We believe that the variation of τ_d and C_a with temperature can be explained in terms of an Auger-like scattering process in the dot in which an electron in an excited state scatters with a ground state hole, thereby losing its energy.^{4,5} With increase in temperature, the thermal excitation of holes from the lowest quantum dot levels will decrease the rate of this process, since there are fewer holes for the electrons to recombine with. Auger recombination in the wetting layer also contributes to the process. These results will be discussed and presented.

The work is supported by ARO and NSF.

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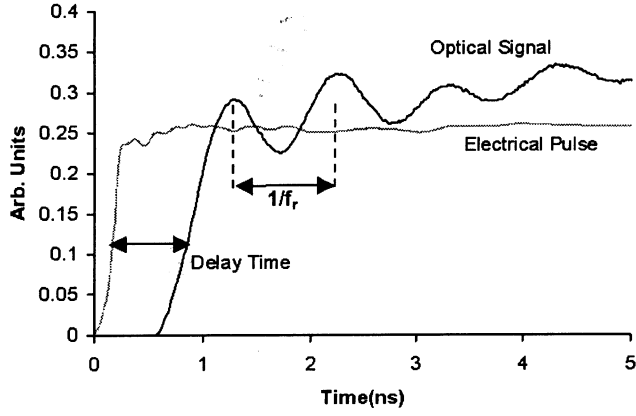


Fig. 1. Temporal characteristics of the pulsed bias current and the output optical pulse. The delay time is measured between the 50% points. Characteristic relaxation oscillations can also be seen.

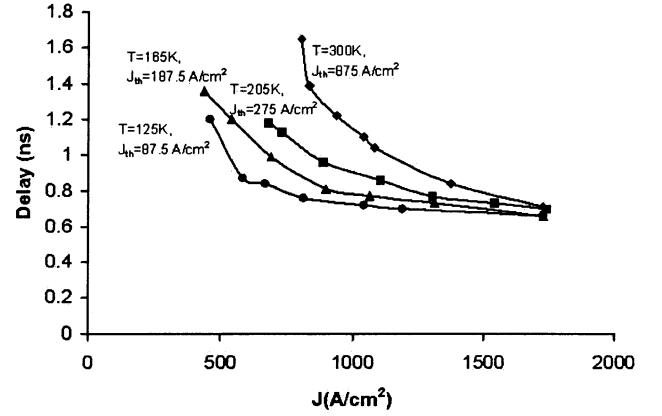


Fig. 2. The measured turn-on delay times as a function of injection current density and temperature.

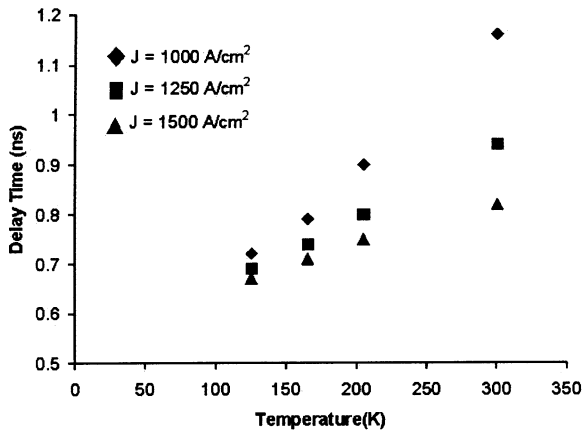


Fig. 3. The delay times as a function of temperature for fixed current densities.

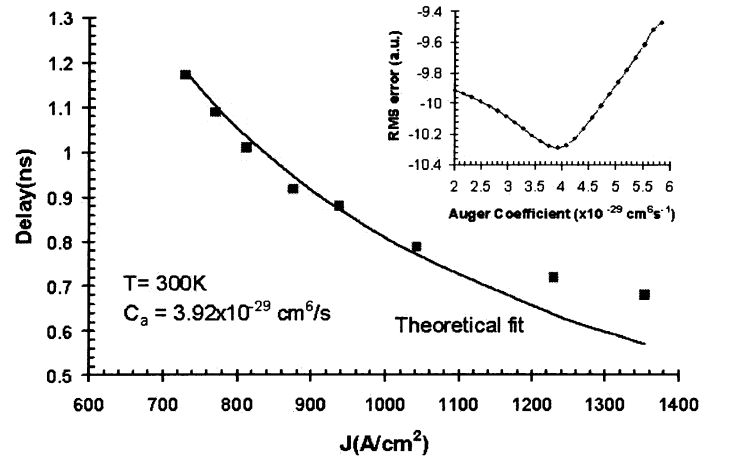


Fig. 4. A typical fit to the measured delay times at 300K. The inset shows a minimum in the RMS error at $C_a = 3.92 \times 10^{-29} \text{ cm}^6/\text{s}$.

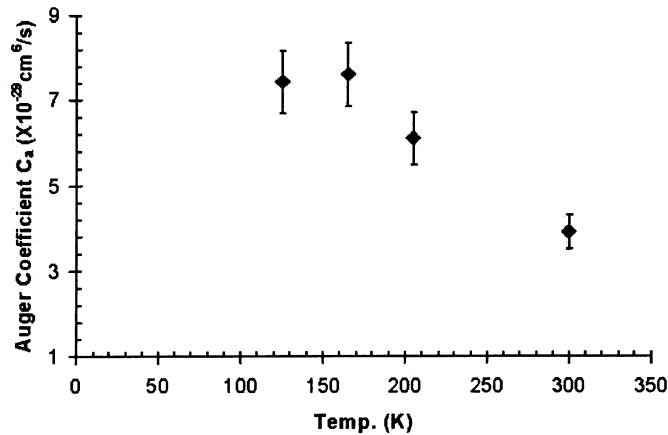


Fig. 5. Variation of the Auger coefficient C_a with temperature.

ZnSe-based laser diodes for the 560 nm spectral region

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Optical data transmission is one of the fastest growing markets today. It is dominated by the use of doped silica fibers. For short and medium range communication purposes plastic optical fibers (POF) with a polymethyl methacrylate (PMMA) core would suffice. But especially the medium range transmission is hampered by the degradation of the signal due to losses in the POF when using conventional III-V semiconductor, namely InP-based, light emitting and laser diodes as light source. These losses could be reduced by using a light source emitting around 560 nm where the PMMA transmission loss spectrum has its absolute minimum. However, the shortest wavelength realized with InP-based laser diodes so far is 614 nm [1]. A solution for this problem could be the use of II-VI semiconductor material. At present a number of groups worldwide are exploring this idea, employing a variety of different substrates such as ZnTe and InP, but they only achieved electroluminescence so far. In our approach we focus on standard ZnSe-based laser diodes grown on GaAs. Especially compared to InP these substrates are cheaper and thus can also provide cost reduction.

In this paper we report the fabrication, the optimization and the operational characteristics of ZnSe-based laser diodes with quaternary ZnCdSSe quantum wells (QWs), specially designed to operate around 560 nm. The conventional double heterostructure, separate confinement design of the laser structures is realized with ZnMgSSe cladding and ZnSSe wave guiding layers. To obtain lasing emission at the desired spectral region high Cd contents are required for the QWs. The photoluminescence spectrum of such a laser diode in Fig. 1 indicates that these QWs can be grown in high optical quality despite the large lattice mismatch between the QW and the rest of the structure. The full width at half maximum of the QW emission is only 13 meV, which is close to the theoretical value for a mixed crystal with 45% Cd. High resolution X-ray diffraction measurements confirm the high crystal quality of the structure, since no relaxation of the structures is found.

Fig. 1 also shows the stimulated emission around 558 nm of the laser diode while operated in pulsed and in continuous wave (cw) mode. The shift of 2 nm in emission wavelength between pulsed and cw mode corresponds to a temperature shift of 15 K indicating only moderate heating. The threshold current density of the device is 680 A/cm² and the operating voltage is less than 6 V at threshold. The external differential quantum efficiency was calculated to 68%.

Whereas the given device parameters are comparable to the conventional III-V laser diodes the lifetime in cw mode is at present less than a minute. As we have already shown, improvements can be expected from a more professional device processing technology [2]. Nevertheless the light output vs. current characteristic shown in Fig. 2 clearly demonstrates the principle stability of the devices even under high current injection. Above the threshold current of 68 mA the light output increases linearly. This linear behaviour is maintained up to the fivefold of the threshold current. The maximum output power is more than 930 mW, which is to the best of our knowledge the highest output power reported for ZnSe-based laser diodes so far.

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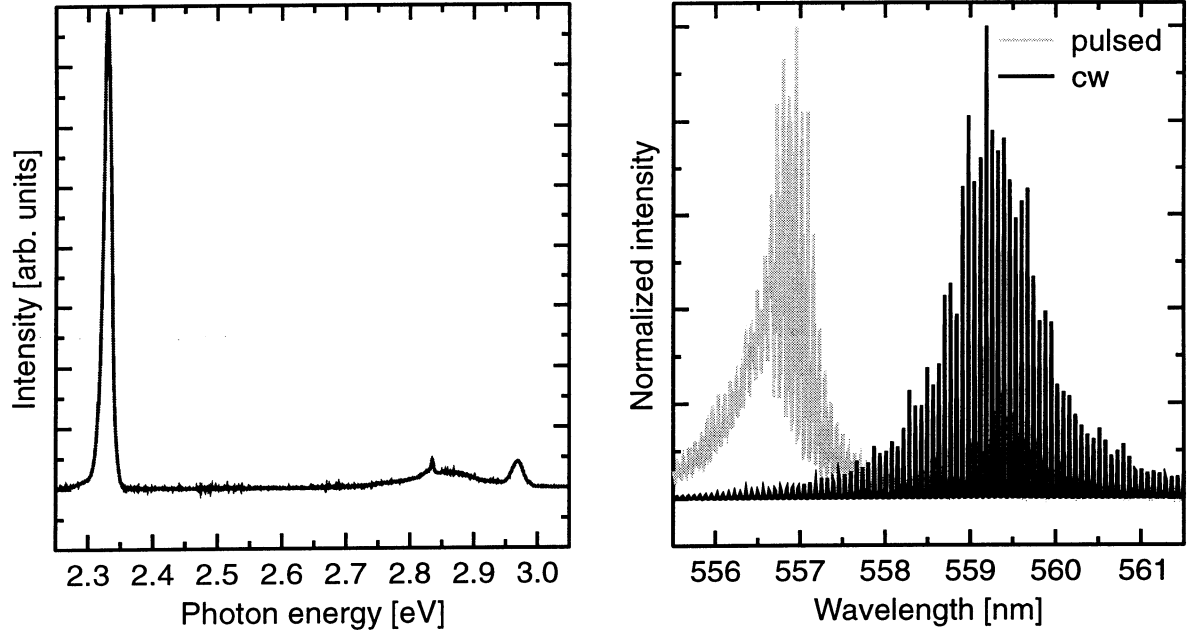


Figure 1: *Left part:* Photoluminescence spectrum of a laser diode recorded at 8 K. The quantum well emission clearly dominates the spectrum. The FWHM of 13 meV indicates a high quality of the quantum well. *Right part:* Electroluminescence spectra of the same device under pulsed and dc current injection at room temperature. The emission wavelength shift corresponds to a temperature increase of 15 K

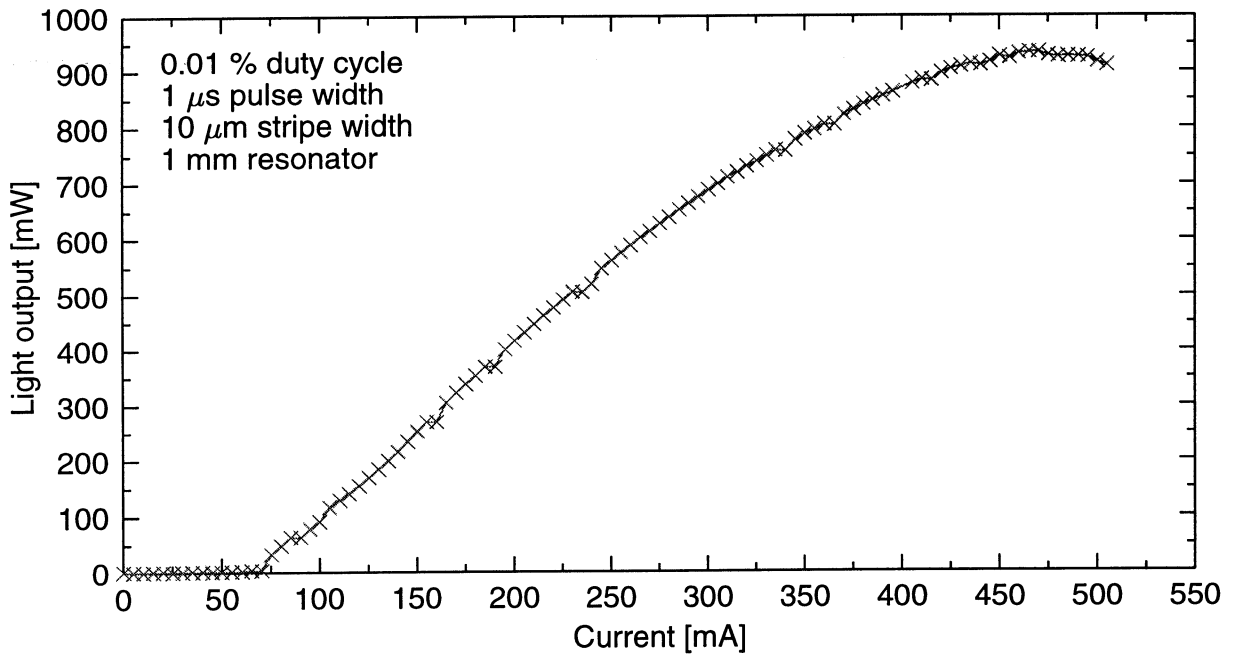


Figure 2: Light output vs. current characteristic of the laser diode in pulsed mode at room temperature. The threshold current is 68 mA, a maximum output power of 938 mW is measured.

***NpN* InGaAsN-based Heterojunction Bipolar Transistors with $f_{MAX} = 60$ GHz**

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Heterojunction Bipolar Transistors (HBT's) based on InP have demonstrated good potential for low-power electronic devices with the use of a small band-gap material in the base for an advantageous lower turn-on voltage V_{ON} but the high-cost InP technology has limited its commercial application. Progress in (In,Ga)(As,N) material quality has motivated the development of new bipolar transistors to produce cost-effective low-power devices. By incorporating a proper amount of N and In into GaAs simultaneously, a quaternary $In_xGa_{1-x}As_yN_{1-y}$ material lattice-matched to GaAs can be obtained with a significant reduction of the energy band-gap E_G .

Previous work on InGaAsN *Npn* HBT's has been concentrated on large area devices and initial DC results exhibit advantageous turn-on voltage reduction over the conventional InGaP/GaAs counterpart. This work reports DC and RF characteristics of small-area *NpN* InGaP/InGaAsN/GaAs Double HBT's (DHBT's) grown by metal organic chemical vapor deposition. The basic structure consists of a 500 Å *n*-InGaP emitter followed by a 700 Å *p*⁺-InGaAsN base and a 5000 Å *n*-GaAs collector. The $In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$ material is lattice-matched to GaAs with an E_G of approximately 1.2 eV. The band alignment of an abrupt InGaP/InGaAsN/GaAs double heterostructure is shown in Fig. 1. The large conduction band offset ($\Delta E_C \sim 0.32$ eV) at the base-emitter heterojunction gives rise to more energetic electron injection into the base but will also result in increasing the turn-on voltage of the transistor. A 0.2 eV conduction band offset at the base-collector heterojunction blocks the electron flow and prevents electron from being injected in the collector. For all these reasons, interfaces have been properly designed with the use of step grading and delta-doping layers to reduce the effect of the conduction band spikes on the electron transport at both heterojunctions. Self-aligned DHBT's were fabricated using a regular triple-mesa technology process. Pt/Ti/Pt/Au and Ge/Au/Ni/Au were e-beam evaporated to form the base and collector contacts while sputtered WSi served as the emitter metal.

Devices with an active emitter area of $3 \times 5 \mu m^2$ exhibit a DC current gain of 10. Despite recent progress in InGaAsN material quality, difficulties in producing base InGaAsN electron mobility and lifetime values comparable to the GaAs counterpart lead to non-optimized base transit time and increasing base current for a reduced DC current gain. The collector ideality factor is 1.05 and the base ideality factor is 1.31 (as low as 1.1 with non-self aligned devices), indicating high-quality InGaP/InGaAsN and InGaAsN/GaAs heterojunctions. The turn-on voltage (defined as the base-emitter voltage required to exceed a determined output collector current) of the *NpN* InGaAsN-based DHBT's is about 0.26 V lower than in a conventional *Npn* InGaP/GaAs HBT. The low turn-on voltage as well as advantageous offset voltage $V_{OFFSET} \sim 0.12$ V and knee voltage $V_{KNEE} \sim 0.3$ V provides an initial experimental indicator of the potential this novel technology can have for reducing power dissipation in GaAs-based transistors. Preliminary RF characteristics have been measured. Self-aligned devices exhibit a cut-off frequency $f_T = 29$ GHz currently limited by the base transport parameters. Despite a base sheet resistance around 1000 $\Omega/\square$, a maximum oscillation frequency f_{MAX} as high as 60 GHz is reported from the *NpN* InGaAsN DHBT. These promising high frequency characteristics have been demonstrated using a straightforward epitaxial design. Improvements are expected with particular consideration given to enhanced base transit time and reduced collector capacitance. Details on optimized InGaAsN-based HBT design will be presented.

In summary, microwave measurements from $3 \times 5 \mu m^2$ self-aligned *NpN* InGaAsN DHBT devices indicate that this low band gap material system can be successfully implemented in a GaAs-based HBT structure for lowering the turn-on voltage while attaining high-speed performances.

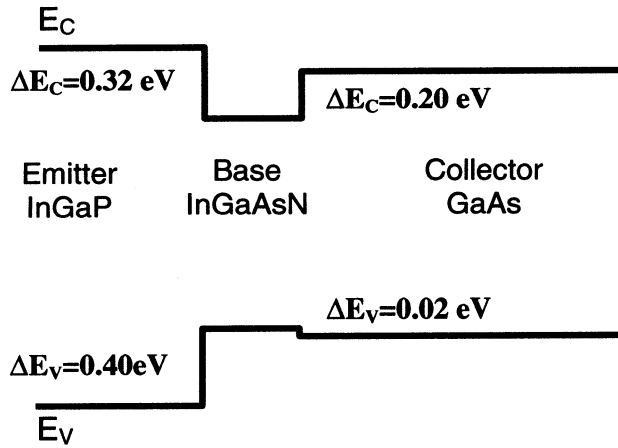


Fig. 1: Conduction and Valence band offsets of typical InGaP/InGaAsN/GaAs double heterojunction.

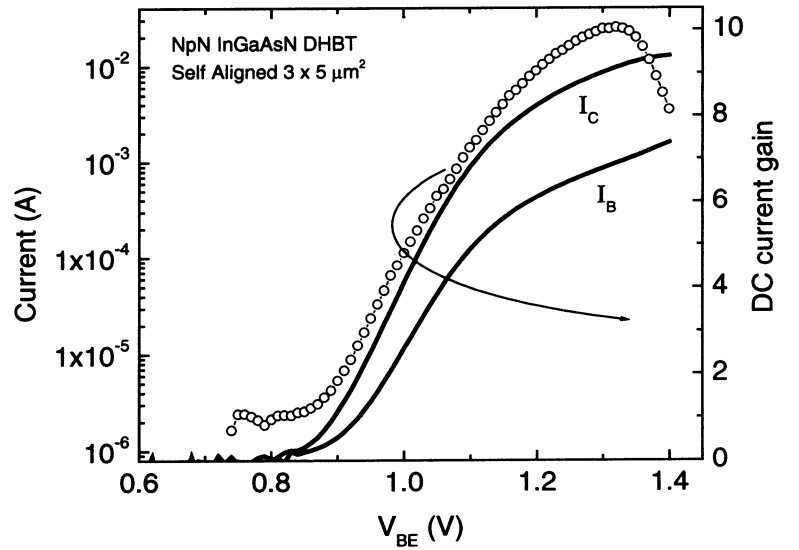


Fig. 2: Gummel plot characteristics and associated DC current gain of a self-aligned ($3 \times 5 \mu\text{m}^2$) NpN InGaAsN DHBT

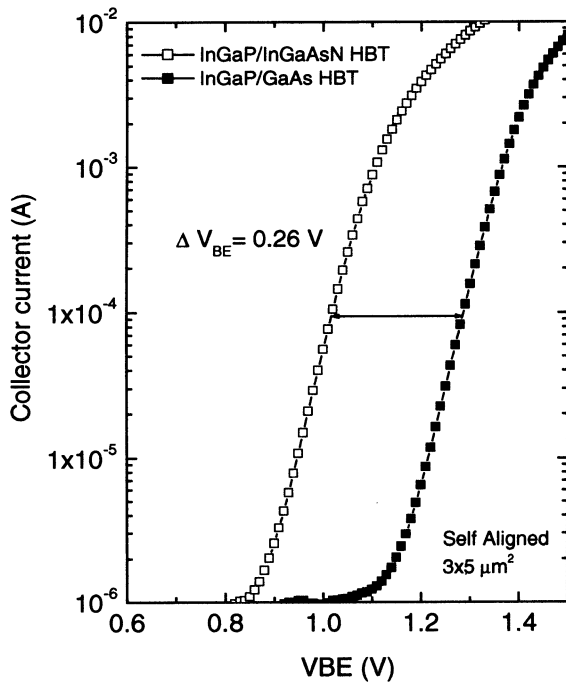


Fig. 3: Collector current comparison between traditional InGaP/GaAs HBT and the novel InGaAsN-based DHBT.

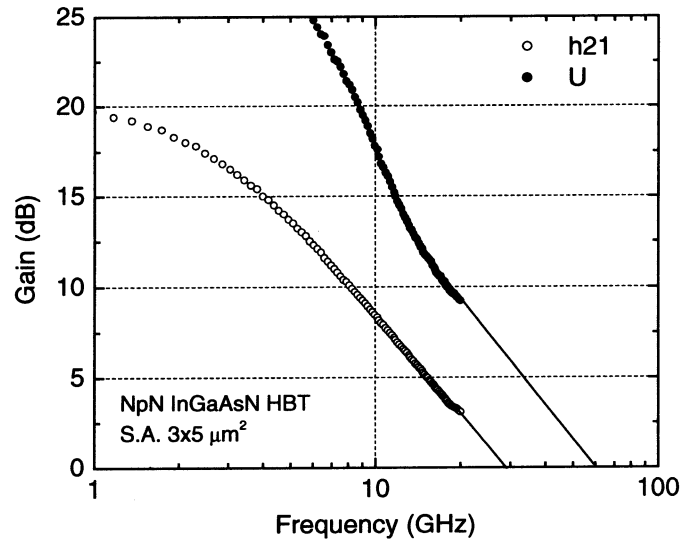


Fig. 4: Small-signal gain h_{21} and unilateral power gain U of a self-aligned $3 \times 5 \mu\text{m}^2$ InGaAsN DHBT with extrapolated cut-off frequency and maximum oscillation frequency of 29 and 60 GHz, respectively.

Noise Characteristics of Highly Strained InGaP/InGaAs p-HEMTs Grown on Patterned Substrates by Using Compound-Source MBE

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While the performance of InGaP/InGaAs pseudomorphic high electron mobility transistor (p-HEMT) can be improved by increasing the In composition of InGaAs channel layer due to the improved confinement and mobility of 2-dimensional electron gas, the In composition and the thickness of the InGaAs channel layer used for conventional GaAs-based p-HEMTs have been restricted below approximately 22% and 120 Å, respectively, due to the limitation of the critical layer thickness of the strained layer. P-HEMTs having an InGaAs channel layer thickness over the critical layer thickness showed a degraded performance due to the high misfit dislocation density [1]. Fitzgerald et. al. reported a patterned substrate growth of high-quality InGaAs layers, which are 10 times thicker than the critical layer thickness, having a reduced misfit dislocation density [2]. Using the patterned substrate growth, highly strained InGaP/In_{0.33}Ga_{0.67}As p-HEMTs having improved DC and microwave performances compared with those of conventional InGaP/In_{0.22}Ga_{0.78}As p-HEMTs have been successfully demonstrated [3]. In this paper, we report on the low-frequency and microwave noise characteristics of the highly strained InGaP/In_{0.33}Ga_{0.67}As p-HEMTs grown on patterned substrate and the conventional InGaP/In_{0.22}Ga_{0.78}As p-HEMTs grown on non-patterned substrate.

Highly strained InGaP/In_{0.33}Ga_{0.67}As and conventional InGaP/In_{0.22}Ga_{0.78}As p-HEMT structures, shown in Fig. 1, were grown on patterned and non-patterned GaAs substrates, respectively, using a compound-source MBE. Prior to the growth of the highly strained InGaP/In_{0.33}Ga_{0.67}As p-HEMT, 250nm high mesa patterns were formed on the semi-insulating GaAs substrates by dry etching. Transistors having a 1.5µm×50µm gate were fabricated using a conventional optical lithography. Fig. 2 shows the dependence of drain saturation current and transconductance of the p-HEMTs on the gate-source bias voltage. Fig. 3 shows the dependence of f_T and f_{max} of the p-HEMTs on the gate-source bias voltage.

Low-frequency input noise spectral densities of the p-HEMTs were measured for temperatures between 150 K and 440 K and frequencies between 1 Hz and 53 kHz. Fig. 4 shows the room-temperature low-frequency input noise spectral density of the p-HEMTs as a function of frequency measured at $V_{gs} = 0V$ and $V_{ds} = 2V$. The low-frequency noise of the p-HEMTs showed pure $1/f$ noise characteristics for most of the temperature investigated. Noise level and Hooge parameter of the highly strained InGaP/In_{0.33}Ga_{0.67}As p-HEMT were approximately an order of magnitude smaller than those of the conventional InGaP/In_{0.22}Ga_{0.78}As p-HEMT.

On-wafer microwave noise performance of the p-HEMTs was measured for different bias conditions. Fig. 5 shows the minimum noise figure and associated gain of the p-HEMTs as a function of frequency measured at $I_{ds} = 1.5mA$ and $V_{ds} = 1V$. Fig. 6 shows the drain current dependence of the minimum noise figure and associated gain of the p-HEMTs measured at $f = 2 GHz$ and $V_{ds} = 1V$. As can be seen in Fig. 5 and 6, the minimum noise figure of the highly strained InGaP/In_{0.33}Ga_{0.67}As p-HEMTs was lower than that of the conventional InGaP/In_{0.22}Ga_{0.78}As p-HEMT by more than 1 dB for most of the bias conditions.

In conclusion, substantial improvements in DC (drain saturation current and transconductance), microwave (f_T and f_{max}), and low-frequency and microwave noise characteristics of the InGaP/In_{0.33}Ga_{0.67}As p-HEMTs having a highly strained InGaAs channel layer (50% in excess of the critical layer thickness) are reported. The results indicate the potential of highly strained p-HEMTs grown on patterned substrates for use in high-performance device applications.

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GaAs	Cap	500 Å	8.0e18
In _{0.49} Ga _{0.51} P	Schottky	200 Å	5.0e17
In _{0.49} Ga _{0.51} P	doping	50 Å	1.0e19
Al _{0.24} Ga _{0.76} As	spacer	60 Å	Undoped
In _x Ga _{1-x} As (x=0.22, 0.33)	Channel	100 Å	Undoped
GaAs	Buffer	4000 Å	Undoped
Semi-Insulating GaAs Substrate			

Fig. 1. Layer structure of the highly strained and conventional InGaP/InGaAs p-HEMTs.

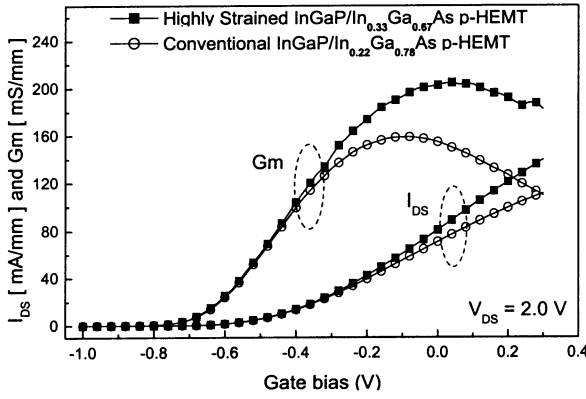


Fig. 2. Normalized drain saturation current and transconductance of the highly strained and conventional InGaP/InGaAs p-HEMTs.

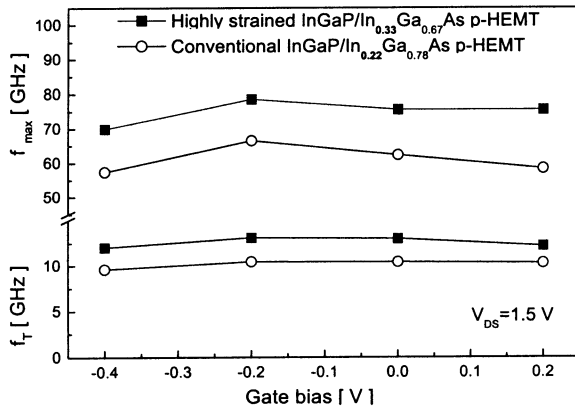


Fig. 3. Dependence of f_T and f_{max} of the highly strained and conventional InGaP/InGaAs p-HEMTs on the gate-source bias voltage.

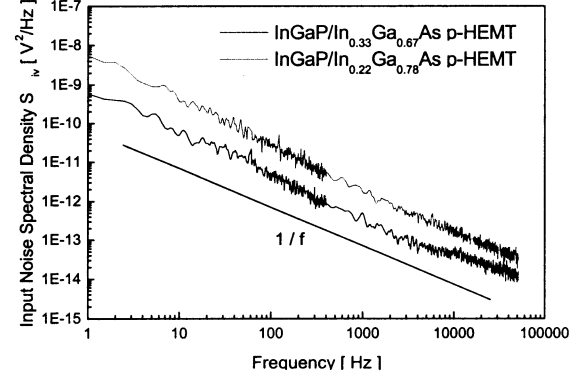


Fig. 4. Low-frequency input noise spectral density of the highly strained and conventional InGaP/InGaAs p-HEMTs measured at room temperature.

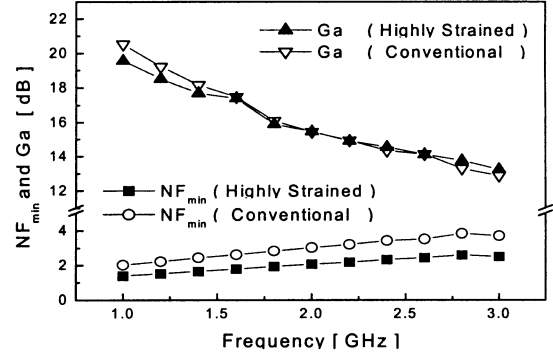


Fig. 5. Frequency dependence of minimum noise figure and associated gain of the InGaP/InGaAs p-HEMTs ($I_{ds} = 1.5\text{mA}$ and $V_{ds} = 1\text{V}$).

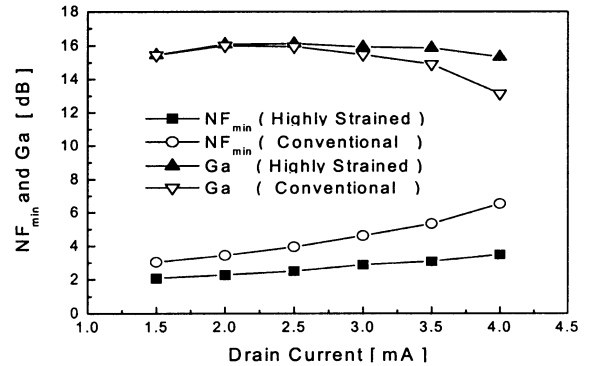


Fig. 6. Drain current dependence of minimum noise figure and associated gain of the InGaP/InGaAs p-HEMTs ($f = 2\text{GHz}$ and $V_{ds} = 1\text{V}$).

A Flip-Flop Based on Monolithic Integration of InAs/AlSb/GaSb RITDs and InAlAs/InGaAs/InP HEMTs

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Ultra-fast digital signal processing systems require both extremely high device speeds as well as compact topologies for implementing logic functions with low power dissipation. Circuits based on resonant tunneling diodes (RTDs) are a promising approach to achieve this goal. RTDs exhibit extremely high device speeds (switching times as low as 1.5 ps [1]) and the unique current-voltage characteristics of RTDs can be used to greatly reduce the circuit complexity required to realize logic functions [2-5]. Power consumption of RTD-based logic circuits can also be made small; InP-based RTD/HEMT logic circuits have been demonstrated experimentally with power dissipations of less than 2 mW/gate [6]. Even higher speed-power product performance can be expected from circuits based on InAs/AlSb/GaSb resonant interband tunneling diodes (RITDs), due to the unique broken-bandgap alignment present in this material system. As a consequence of this energy band configuration, considerably lower RITD peak voltages can be achieved. Circuits operating at lower supply voltages with correspondingly lower power consumption can thus be expected using RITDs.

We report for the first time the demonstration of logic circuits based on the monolithic integration of high-speed submicron gate length InAlAs/InGaAs/InP HEMTs with InAs/AlSb/GaSb RITDs. The epitaxial layers for the integrated RITD/HEMT device process were grown by molecular beam epitaxy (MBE) on unpatterned 2" semi-insulating InP substrates in a single uninterrupted growth run. The HEMT layers were grown first, followed by a strain-relaxed buffer layer and the RITD layers. A lattice-matched δ -doped InGaAs-channel HEMT heterostructure was employed. The RITDs had 1.5 nm AlSb barriers and a 6 nm GaSb quantum well. The RITD and HEMT layers were separated by a 50 nm thick layer of InGaAs (with lattice parameter matched to InP) followed by a 150 nm InAs buffer layer. Good electron transport properties were achieved in the HEMT channel, with a room-temperature sheet concentration of $2.1 \times 10^{12} \text{ cm}^{-2}$ and a mobility of $9800 \text{ cm}^2/\text{Vs}$. The IC fabrication process included mix-and-match optical and electron-beam lithography, mesa isolation for both HEMTs and RITDs, and low-k benzocyclobutene dielectric crossovers. HEMTs with $0.2 \mu\text{m}$ T-gates demonstrated -1.5 V pinchoff voltages, peak transconductance of 470 mS/mm , f_t 's of 127 GHz, and f_{max} 's of 183 GHz. The RITDs exhibited peak current densities of 12.3 kA/cm^2 .

An inverting D flip-flop was implemented using the MOBILE circuit architecture [5]. The top and bottom RITDs had areas of 115 and $108 \mu\text{m}^2$, respectively, and a $50 \mu\text{m}$ wide HEMT was used in parallel with the bottom RITD. Using a $0.6 \text{ V}_{\text{pp}}$ clock signal, output voltage levels of 0.54 V and 0.12 V were obtained for high- and low-outputs, respectively. The bistability inherent in the circuit architecture resulted in an effective inverting voltage gain in excess of 380. This effective gain is much greater than the g_m/g_o ratio of the HEMT (approximately 10), and is made possible by the negative differential resistance of the RITDs. No output hysteresis was detectable. The input logic threshold voltage was -1.15 V, and proper latching operation was maintained over the full range of input voltages from -1.5 V to 0 V. Power dissipation of 2.3 mW/gate was measured. Further decreases in power dissipation are expected from circuits with smaller area RITDs. High speed testing to determine the maximum switching speed, input sensitivity, and bit-error rate of the circuits is presently underway and will be presented at the conference.

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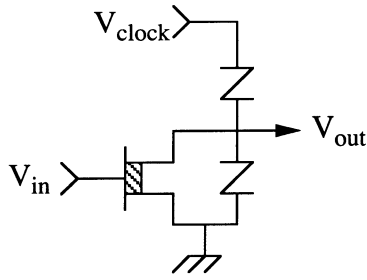
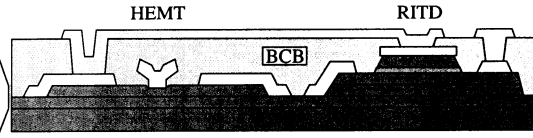


Figure 1. Circuit schematic of inverting D-flip flop.

HEMT layers:
 n⁺ InGaAs
 AlAs etch stop
 i-InAlAs
 Si δ -doping plane
 i-InAlAs
 i-InGaAs channel
 i-InAlAs buffer
 InP substrate



RITD layers:
 n⁺ InAs
 n-InAs
 i-InAs
 i-AlSb barrier
 i-GaSb quantum well
 i-AlSb barrier
 i-InAs
 n-InAs
 n⁺ InAs
 InAs buffer
 n⁺ InGaAs
 AlAs etch stop

Figure 2. Cross-sectional diagram of integrated RITD/HEMT process. Vertical dimensions are approximately to scale.

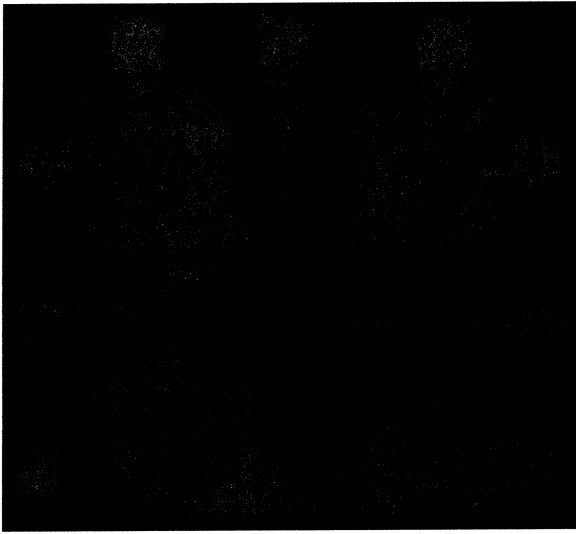


Figure 3. Die photograph of completed integrated circuit.

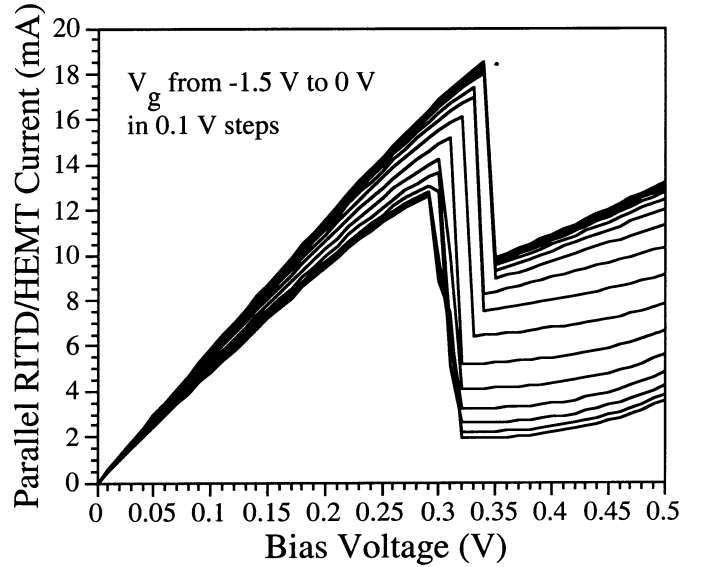


Figure 4. Measured current-voltage characteristic of parallel interconnected InP-based HEMT and InAs/AlSb/GaSb RITD. Peak current is modulated from 12.3 mA to 18.4 mA.

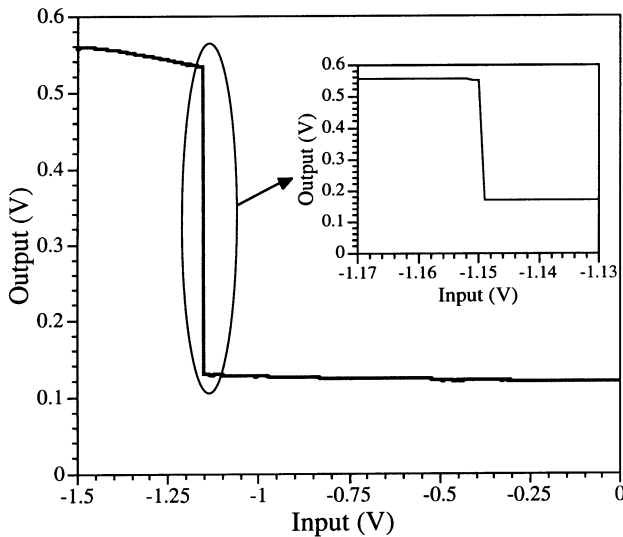


Figure 5. Measured voltage transfer characteristic for inverting D-flip flop. Exploded view of transition region is shown in inset. Circuit bistability provides effective voltage gain in excess of 380.

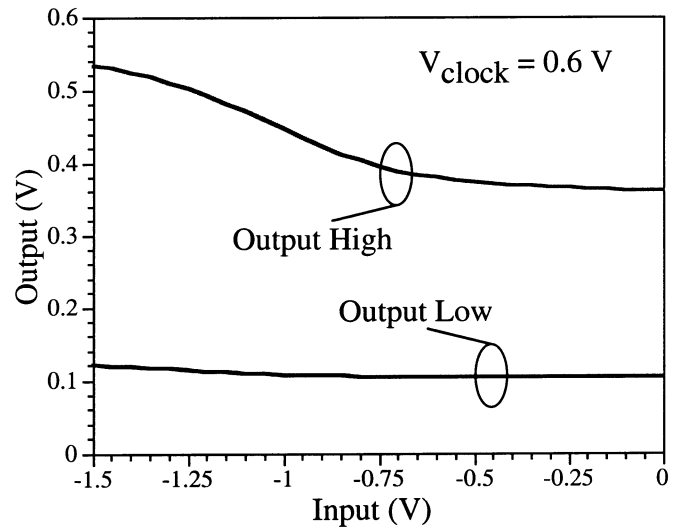


Figure 6. Measured output voltage in high and low latch states as a function of input voltage. Proper logic operation and preservation of latch state is maintained over full input range.

Monolithic Integration of InAlAs/InGaAs Enhancement and Depletion (E/D)-Mode Metamorphic HEMTs on GaAs Substrate

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Abstract

Metamorphic high electron mobility transistors (MM-HEMTs) utilizing InAlAs/InGaAs heterostructure for active device layers and GaAs as substrate have seen a remarkable and promising development in recent years. Although, InP-based InAlAs/InGaAs lattice-matched (LM) HEMTs show the best performance in terms of speed and noise, GaAs substrates, in view of their lower cost, easier handling, less fragility and more mature processing technology as compared to InP substrates, make MM-HEMT a very strong contender for commercial exploitation. Moreover, MM-HEMTs have been demonstrated with performance closely matching with InP-based HEMTs [1-2]. Except for a few studies on enhancement (E)-mode MM-HEMTs [3], most of the research studies so far however focused on depletion (D)-mode HEMTs. In view of excellent performance of D-mode devices, it is compelling to investigate E-mode devices as well. Moreover, once discrete devices are established, it becomes very much interesting to look into the monolithic integration of E- and D-mode devices as it finds an extensive application for ultra-high speed and low power digital circuits [4]. To the best of our knowledge, there are no published results on monolithic integration of metamorphic E/D HEMTs so far. In this paper, we present results on monolithically integrated metamorphic $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ E/D HEMTs on GaAs substrate with gate-lengths down to 0.13 μm .

Device layers are grown on 3-inch SI GaAs substrate using MBE. To accommodate the large lattice-mismatch strain between GaAs and InGaAs, a 1.5 μm -thick linearly-graded InAlGaAs buffer layer is employed [5]. Active device layers from buffer layer upward included a 200 Å-thick undoped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel, 40 Å-thick undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ spacer, Si delta-doping plane, 120 Å-thick undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ E-mode Schottky layer, 15 Å-thick undoped AlAs etch stop, 100 Å-thick undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ D-mode Schottky layer, and finally, 80 Å-thick doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ($N_D = 1 \times 10^{19} \text{ cm}^{-3}$) cap layer. Without the cap, a mobility of 9550 $\text{cm}^2/\text{V}\cdot\text{sec}$ and a sheet density of $1.12 \times 10^{12} \text{ cm}^{-2}$ are achieved at room temperature. Device fabrication started with mesa-isolation using wet-chemical etching. Ohmic contacts were formed by furnace alloying of evaporated AuGe/Ni/Au at 380 °C for 1 min. in N_2 ambient. Ohmic contact resistance was typically measured to be 0.12 $\Omega\cdot\text{mm}$. T-gates of E-mode devices were defined first using a tri-layer PMMA/P(MMA-MAA) resist with e-beam lithography and Pt/Ti/Pt/Au metallization. Gate-recess was performed by a citric acid: H_2O_2 solution. Overlay metallization on the ohmic contacts and measurement pads of E-mode devices was also deposited during gate formation. E-mode gate-anneal process was carried out in a furnace at 375 °C for 1 min to drive the bottom layer of Pt of the gate metal in the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layer. This buried Pt-layer was used to achieve a positive shift in the threshold voltage of the devices [6]. Finally, T-gates and overlay for D-mode devices were defined using e-beam lithography and Ti/Au metallization was employed for D-mode gates. D-mode gate-recess was carried out by a succinic acid: H_2O_2 solution. The gate-width of the devices was $2 \times 50 \mu\text{m}$ while the drain-source distance was 2.0 μm . Devices with gate-lengths down to 0.13 μm were fabricated.

DC and RF measurements were carried out for these devices. For E-devices, DC measurements were also recorded before gate-anneal. Excellent pinch-off characteristics were obtained for both E- and D-mode devices as shown in Fig. 1, and Fig. 2, respectively for 0.13 μm gate-length devices. As shown in Fig. 3, a maximum extrinsic transconductance (g_m) of around 650 mS/mm and a threshold voltage (V_T) of about 40 mV are recorded for E-devices after the gate-anneal. As evident in this figure, the gate-anneal process significantly shifts the V_T towards positive voltage as well as enhances the g_m of device. The g_m and V_T values for 0.13 μm D-mode devices were typically around 600 mS/mm and -350 mV, respectively. RF measurements were done using Cascade Microtech probes and HP8510B network analyzer in the frequency range of 1 to 35 GHz. Figures 5 and 6 show the measured current gain and maximum stable gain (MSG)/maximum available gain (MAG) derived from S-parameters for a typical E-mode and a typical D-mode device, respectively. Using a -20 dB/decade roll-off line, a unity current gain cut-off frequency (f_T) of 140 GHz and maximum oscillation frequency (f_{max}) of 200 GHz were obtained for E-mode devices and (f_T) of 135 GHz and f_{max} of 170 GHz were obtained D-mode devices. These results demonstrate the remarkable performance of metamorphic E/D HEMTs. Results of devices with other gate-lengths will also be reported.

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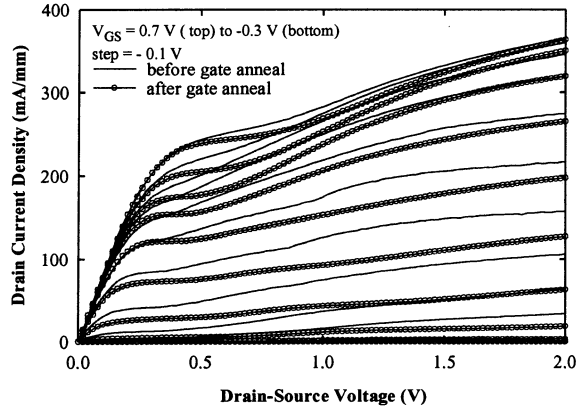


Fig. 1. Typically measured drain current characteristics of $0.13 \mu\text{m} \times 100 \mu\text{m}$ $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MM-EHEMTs on GaAs substrate before and after gate anneal

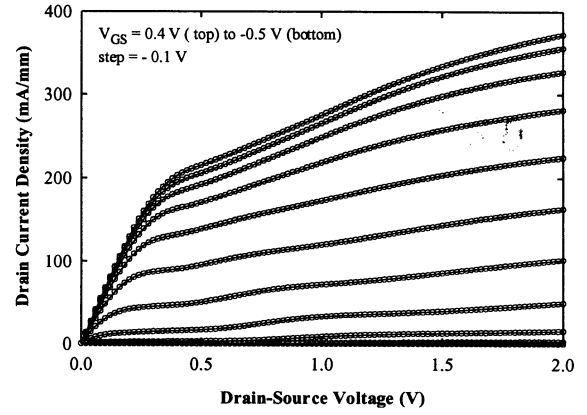


Fig. 2. Typically measured drain current characteristics of $0.13 \mu\text{m} \times 100 \mu\text{m}$ $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MM-DHEMTs on GaAs substrate

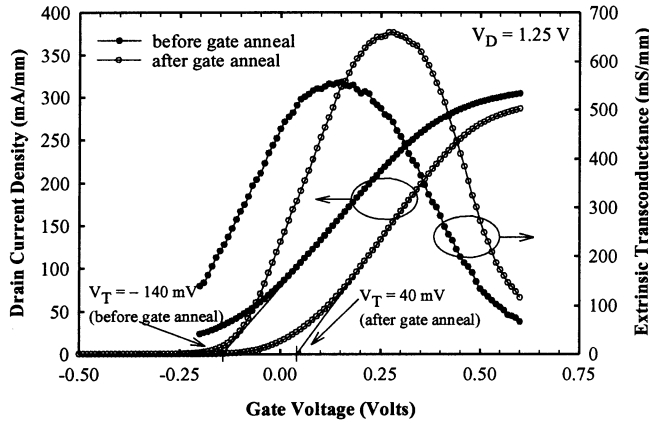


Fig. 3. Transfer characteristics of a typical $0.13 \mu\text{m} \times 100 \mu\text{m}$ $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MM-EHEMT at V_D of 1.25 V before and after gate anneal

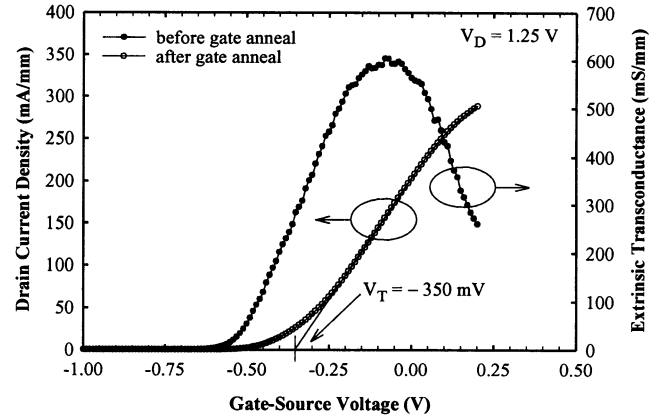


Fig. 4. Transfer characteristics of a typical $0.13 \mu\text{m} \times 100 \mu\text{m}$ $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MM-DHEMT at V_D of 1.25 V

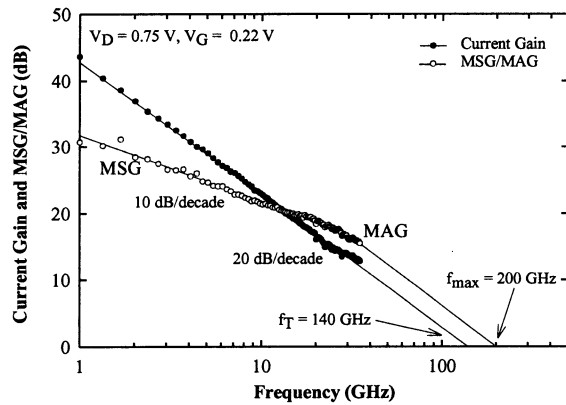


Fig. 5. RF gain characteristics of a typical $0.13 \mu\text{m} \times 100 \mu\text{m}$ $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MM-EHEMT

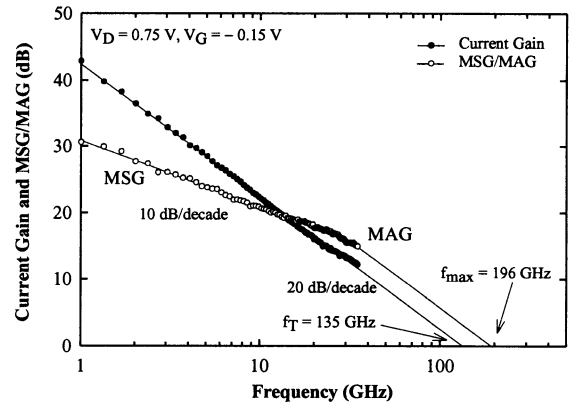


Fig. 6. RF gain characteristics of a typical $0.13 \mu\text{m} \times 100 \mu\text{m}$ $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MM-DHEMT

MONDAY PM, JUNE 25TH, 2001, 5:30 PM–8:00 PM

III.-1-Dual-Channel SOI LGBT with Improved Latch-Up and Forward Voltage Drop Characteristics: *Woo-Beom Choi*¹; Woong-Je Sung¹; Yong-Il Lee¹; Man Young Sung¹; ¹Korea University, Dept. of Elect. Eng., 1, 5-ka, Anam-dong, Sungbuk-ku, Seoul 136-701 Korea

III.-2-Chaos Generator MMIC's Using Resonant Tunneling Diodes: *K. Maezawa*¹; Y. Kawano¹; Y. Ohno¹; S. Kishimoto¹; T. Mizutani¹; ¹Nagoya University, Graduate Sch. of Eng., Furo-cho, Chikusa-ku, Nagoya-shi, 464-8603 Japan

III.-3-High Detectivity Solar Blind AlGaIn Metal-Semiconductor-Metal Detector: *Jean-Luc Reverchon*¹; Jean-Yves Duboz¹; Fabrice Semond²; Nicolas Grandjean²; Jean Massies²; ¹Laboratoire Central de Recherches, THALES, 91404 ORSAY, Cedex, France; ²CRHEA-CNRS, rue Bernard Gregory, Sophia Antipolis 06560 Valbonne, France

III.-4-Characterization of a 0.1 μ m MOSFET Using Cross-Sectional Scanning Tunneling Microscopy: *T. Okui*¹; S. Hasegawa¹; H. Nakashima¹; H. Fukutome²; H. Arimoto²; ¹Osaka University, The Institute of Scientific and Industrial Research, 8-1 Mihogaoka, Ibaraki, Osaka 567-0047 Japan; ²Fujitsu Laboratories Ltd., 10-1 morinosato-wakamiya, Atsugi, Kanagawa 243-0197 Japan

III.-5-Nanoscale MOSFETs Scaling: *Yehuda Naveh*¹; Victor Sverdlov¹; Konstantin Likharev¹; ¹State University of New York, Stony Brook, NY 11794-3800 USA

III.-6-50 nm Vertical Surround Gate MOSFET with S-Factor of 75mV/dec: *Ruigang Li*¹; Yaohui Zhang²; Yang Lu²; Daniel Sung Choi²; Marie Luo³; Kang L. Wang²; ¹University of California at Los Angeles, Elect. Eng. Dept., Rm. 56-125B ENGR IV, Los Angeles, CA 90095-1594 USA; ²University of California at Los Angeles, Elect. Eng. Dept., Los Angeles, CA 90095-1594 USA; ³Conexant Systems, Inc., 4311 Jamboree, Newport Beach, CA 92660 USA

III.-7-Hyperspectral Imaging of Breakdown in InAlAs/InGaAs HEMTs: A Comparative Study: *Mark Somerville*¹; Jon Rameau¹; Nii Moi Addo¹; ¹Vassar College, Dept. of Phys. and Astron., 124 Raymond Ave., Poughkeepsie, NY 12604 USA

III.-8-Extension of Safe-Operating-Area by Optimizing Body-Current in Submicron LDMOS Transistors: *S. K. Lee*¹; Y. C. Choi¹; J. H. Kim¹; C. J. Kim¹; H. S. Kang¹; C. S. Song¹; ¹Fairchild Korea Semiconductor Co. New Techn. Devel. Team, 82-3 Dodang-Dong, Wonmi-Ku, Puchon, Kyonggi-Do, Korea

III.-9-Computer Analysis of Geometry and Strain Effects in Silicon Nano-Crystal Floating-Gate Flash Memory Devices: *Aaron Thean*¹; Jean-Pierre Leburton¹; ¹University of Illinois, Beckman Institute for Advanced Science & Technology, Dept. of Elec. & Comp. Eng., Urbana, IL 61801 USA

III.-10-An Extension of McKelvey's One-Flux Method to Energy Space: *W. R. McKinnon*¹; ¹National Research Council, Ottawa, K1A 0R6, Canada

III.-11-Characterization of Midgap Tungsten Gate MOSFETs: *Huiling Shang*¹; Marvin H. White¹; Kathryn W. Gaurini²; Edward Cartier²; Paul Solomon²; ¹Lehigh University, EECS Dept., Sherman Fairchild Lab., Bethlehem, PA 18015 USA; ²IBM T. J. Watson Research Center, PO Box 218, Yorktown Heights, NY 10598 USA

III.-12-ESD Protection for High Voltage LDMOS with Sense FET: *Y. S. Choi*¹; J. J. Kim¹; C. K. Jeon¹; M. H. Kim¹; S. L. Kim¹; H. S. Kang¹; C. S. Song¹; ¹Fairchild Semiconductor, Process R&D Group, 82-3 Dodang-Dong, Wonmi-Ku, Puchon, Kyonggi-Do, 420-711, Korea

III.-13-Mixed Mode Double-Gate FET Model: *P. M. Solomon*¹; ¹IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA

III.-14-Low Programming Voltages and Long Retention Time in Metal Nanocrystal EEPROM Devices: *Zengtao Liu*¹; Venkat

Narayanan¹; Myongseob Kim¹; Gen Pei¹; Edwin C. Kan¹; ¹Cornell University, Elect. and Comp. Eng., Ithaca, NY 14853 USA

III.-15-High Performance AlGaIn/GaN HEMTs with Recessed Gate on Sapphire Substrate: *Y. Sano*¹; T. Yamada^{1,2}; J. Mita^{1,2}; K. Kaifu¹; H. Ishikawa³; T. Egawa³; M. Umeno³; ¹Oki Electric Industry Co., Ltd., Corp. Res. Lab., 550-5 Higashiawakawa, Hachioji, Tokyo 193-8550 Japan; ²Ultra-Low-Loss Power Device Technology Research Body; ³Nagoya Institute of Technology, Gokiso-cho, Showa-ku, Nagoya 466-8555 Japan

III.-16-A Comparison of Bulk and SOI Deep Sub-Micron MOSFET Small-Signal Behavior in the High-Frequency Regime Beyond 10GHz: *D. Goldman*¹; T. Gafron¹; C.-S. Kim¹; Q. Nguyen¹; F. Burke¹; B. Cheek¹; S. Parke¹; ¹Boise State University, Dept. of Elect. and Comp. Eng., Boise, ID 83725 USA

III.-17-Threshold Voltage Shift by Quantum Confinement in Ultra-Thin Body Device: *Yang-Kyu Choi*¹; Daewon Ha¹; Tsu-Jae King¹; Chenming Hu¹; ¹University of California at Berkeley, Dept. of Elect. Eng. and Comp. Scis., Berkeley, CA 94720 USA

III.-18-A New and Accurate Quantum Mechanical Compact Model for NMOS Gate Capacitance: *S. Mudanai*¹; L. F. Register¹; A. F. Tasch¹; S. K. Banerjee¹; ¹The University of Texas at Austin, Microel. Res. Ctr., Mail Code R9950, Austin, TX 78712 USA

III.-19-An Intrinsically Coupled HBT/RTD Device Enabling an Adjustable Peak-Current-Density: *P. Velling*¹; M. Agethen¹; W. Prost¹; G. Janssen²; R. M. Bertenburg²; F. J. Tegude¹; ¹Gerhard-Mercator University, Solid State Electr. Dept., 47057 Duisburg, Germany; ²IPAG-Innovative Processing AG, Lotharstrasse 55 (ZHO), 47057 Duisburg, Germany

III.-20-Excellent DC Characteristics of HEMTs on Semi-Insulating Silicon Carbide Substrate: *S. Arulkumaran*¹; T. Egawa¹; G. Zhao¹; H. Ishikawa¹; M. Umeno¹; ¹Nagoya Institute of Technology, Research Center for Micro-Struction Devices, Gokiso-cho, Showa-ku, Nagoya 466-8555 Japan

III.-21-A Quantum Dot FET-A Future Playground of Quantum State Manipulation: *Kanji Yoh*¹; Hironobu Kazama¹; Yoshito Katano¹; ¹Hokkaido University, Res. Center for Interface Quant. Elect., N 13, W8, Kita-ku, Sapporo, Hokkaido 060-8628 Japan

III.-22-Sub-40nm V-Groove MOSFETs: *J. Appenzeller*¹; R. Martel¹; Ph. Avouris¹; J. Knoch²; Y. Lu³; K. L. Wang³; J. Scholvin⁴; J. A. del Alamo⁴; P. Rice⁵; P. Solomon¹; ¹IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA; ²II. Physikalisches Institut, RWTH Aachen, Templergraben 55, 52056 Aachen, Germany; ³University of California at Los Angeles, Los Angeles, CA 90095 USA; ⁴Massachusetts Institute of Technology, 77 Massachusetts Ave., Cambridge, MA 02139 USA; ⁵IBM Almaden Research Center, San Jose, CA 95120 USA

III.-23-Terahertz Plasma-Wave Excitation in 80-nm Gate-Length GaAs MESFET by Photomixing Long-Wavelength CW Laser Sources: *Taiichi Otsuji*¹; Yoshihiro Kanamaru¹; Hajime Kitamura¹; Shin Nakae¹; ¹Kyushu Institute of Technology, Dept. of Control Sci. and Eng., Iizuka, Fukuoka, 820-8502 Japan

III.-24-Fabrication of InP DHBTs with 0.1 μ m Wide Emitter: *T. Arai*¹; H. Nagatsuka¹; Y. Miyamoto¹; K. Furuya¹; ¹Tokyo Institute of Technology, Dept. of Phys. Electr., 2-12-1 O-okayama, Meguro-ku, Tokyo 152-8552 Japan

III.-25-Characteristics of Submicron HBTs in the 140-220 GHz Band: *M. Urteaga*¹; D. Scott¹; T. Matthew¹; S. Krishnan¹; Y. Wei¹; M. Dahlstrom¹; M. Rodwell¹; ¹University of California at Santa Barbara, Dept. of ECE, Santa Barbara, CA 93106 USA

III.-26-A Quantum-Dot Cellular Automata Shift Register: *Ravi Kummamaru*¹; Aexei O. Orlov¹; John P. Timler¹; R. Ramasubramaniam¹; Craig S. Lent¹; Gary H. Bernstein¹; Gregory L. Snider¹; ¹University of Notre Dame, Dept. of Elect. Eng., Notre Dame, IN 46556 USA

Abstract

To improve latch-up and forward voltage drop properties of the silicon-on-insulator (SOI) lateral insulated gate bipolar transistor (LIGBT), a new dual-channel structure is proposed and fabricated in this paper. The dual-channel structure is employed to enable more electrons to flow into the n- drift layer and improve the latch-up characteristic. This dual-channel SOI LIGBT results in significant improvement in latch-up current density. Simulated results indicate that the latch-up current density is improved by 4 times compared to that of the conventional SOI LIGBT. The dual-channel SOI LIGBT's were fabricated using a high voltage CMOS fabrication process.

1. Introduction

The SOI LIGBT is a promising power device for use in high-voltage power integrated circuit applications, due not only to its superior isolation performance but also to good characteristics of lateral power devices on the SOI film. Many advantageous characteristics of the SOI LIGBT device, such as low on-state resistance, high input impedance, high breakdown voltage, dielectric isolation, high switching speed and high packing density, have been reported [1]. Unfortunately, the SOI LIGBT structure contains a parasitic thyristor. The device latch-up, which leads to loss of gate control, may occur at high current due to the existence of the parasitic thyristor. Since device failure due to latch-up prevents the SOI LIGBT to be used in practical applications, it is very important to improve the latch-up characteristic [2].

The purpose of this paper is to describe a new SOI LIGBT structure, which has the dual-channel structure and the improved latch-up and forward voltage drop characteristics as compared to the conventional SOI LIGBT device.

2. Device Structure and Operation

The simplified cross-sectional structures of conventional and proposed SOI LIGBT are shown in Figs. 1(a) and 1(b), respectively. To analyze the on-state and latch-up performance of the conventional and the proposed structure, detailed numerical simulations have been carried out using the two-dimensional device simulator TMA-MEDICI. The conventional SOI LIGBT has been also simulated to compare it with the proposed dual-channel device. The proposed device structure is identical with the conventional structure except its an additional channel and second cathode cell. The cathode cells are symmetrically formed by the self-aligned gate region for the proposed SOI LIGBT. The simulated results correspond to a SOI LIGBT with a 10 μm thick, n-type drift region of 40 μm length and $1 \times 10^{15} \text{ cm}^{-3}$ doping concentration; a 200 μm thick, p-type substrate with a concentration of $1 \times 10^{16} \text{ cm}^{-3}$; and a 2 μm thick isolation oxide layer. The surface doping concentrations of the p+ cathode well and p- base is $1 \times 10^{19} \text{ cm}^{-3}$ and $3 \times 10^{17} \text{ cm}^{-3}$, respectively.

3. Results and Discussion

The forward blocking characteristics of the conventional and the dual-channel device are simulated. As illustrated in Fig. 2, the simulated forward breakdown voltages of the two devices are almost same and about 115 V without the use of an n-buffer surrounding the p+ anode. For comparison, the simulated latch-up

characteristics of the conventional and proposed devices are shown in Fig. 3. At an on-state current density of 30 A/cm^2 and at a gate bias of 20 V, the forward voltage drop of the proposed device is reduced by 0.3 V in comparison with the conventional device. The simulation results on the latch-up current density are 34 A/cm^2 for the conventional structure and over 130 A/cm^2 for the proposed structure. The simulated latch-up current density of the proposed SOI LIGBT exhibits a 4 times improvement over the conventional SOI LIGBT. Fig. 4 shows the hole current vectors in the conventional and proposed structures at the on-state. The proposed structure with dual-channel shows better latch-up characteristics than the conventional device. Because the second cathode cell is located near the anode, a large number of holes flow through p-base of the second cathode electrode without passing through p-base underneath the n+ source region. As illustrated in Fig. 5, the dual-channel SOI LIGBT structure was fabricated on p-type substrate with a 10- μm thick n-type drift layer. Resistivities of the drift and the substrate are $7 \Omega\text{-cm}$ and $2 \Omega\text{-cm}$, respectively. After the p+ cathode well implantation and drive-in, the anode and cathode regions were formed by boron and phosphorous implantations, respectively. Fig. 6 shows the measured I-V characteristics of the proposed SOI LIGBT. Onset voltage of the device is at approximately 1.2V. The onset voltage is defined here as threshold at which the drain diode is turned on.

4. Conclusions

A new SOI LIGBT with dual channel structure was proposed. Its performance has been characterized. With the dual channel structure, holes can be collected by the second cathode effectively without causing latch-up even at high current level. The latch-up current densities for the proposed SOI LIGBT exhibit 4 times improvement over that of the conventional SOI LIGBT at the similar structure.

5. Acknowledgment

This work was financially supported by KEPCO through Electrical Engineering Science Research Institute under contract No. 99-007.

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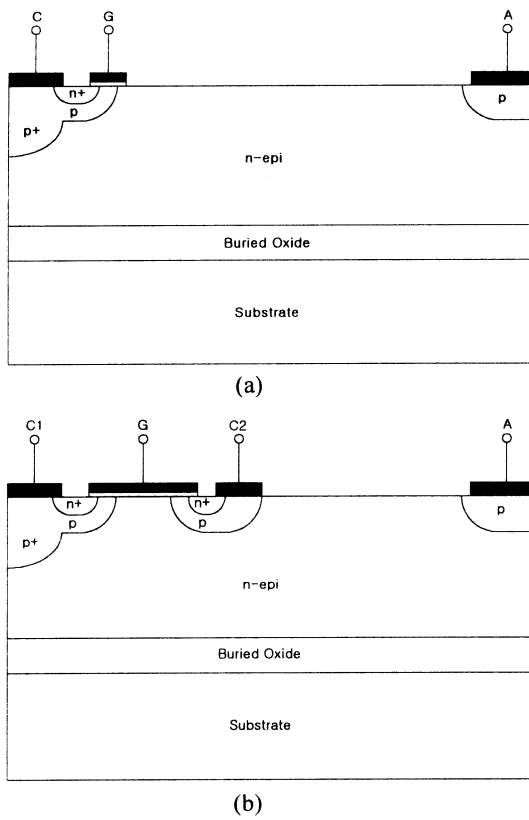


Figure 1. Schematic cross section of (a) the conventional SOI LIGBT and (b) the proposed SOI LIGBT.

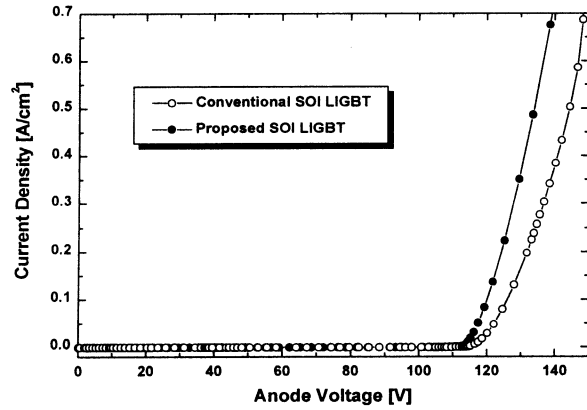


Figure 2. Simulated forward blocking characteristics of the conventional and proposed SOI LIGBT.

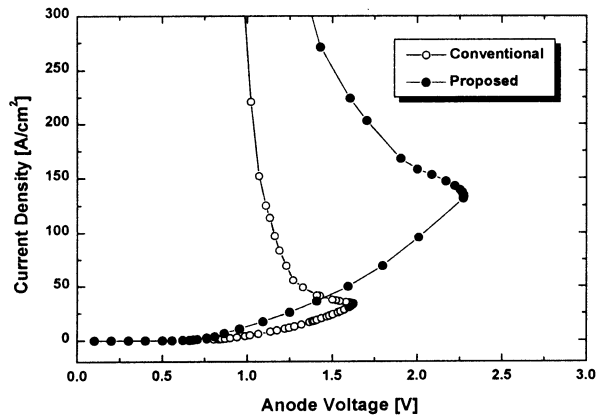
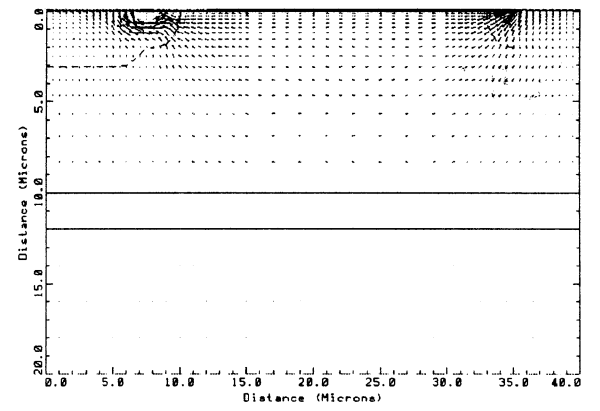
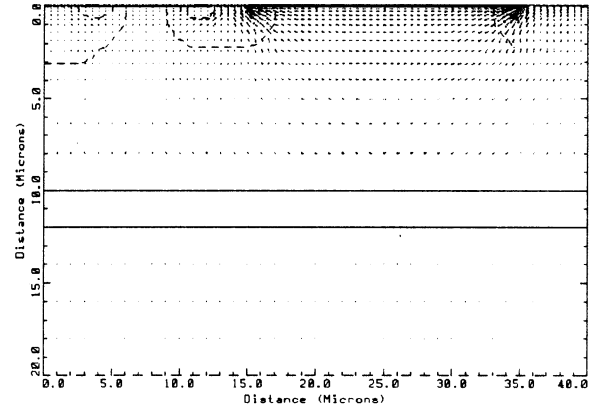


Figure 3. Simulated forward conduction characteristics of the conventional and proposed SOI LIGBT at on-state.



(a)



(b)

Figure 4. Hole current vectors at on-state of (a) the conventional SOI LIGBT and (b) the proposed SOI LIGBT.

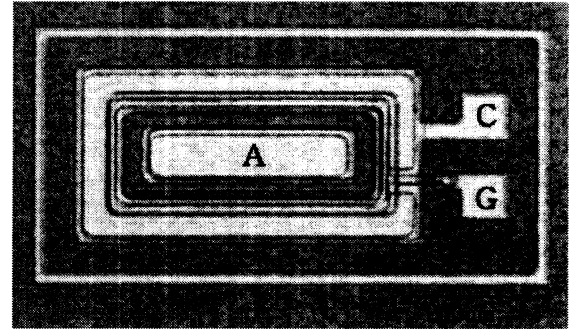


Figure 5. Fabricated dual-channel SOI LIGBT.

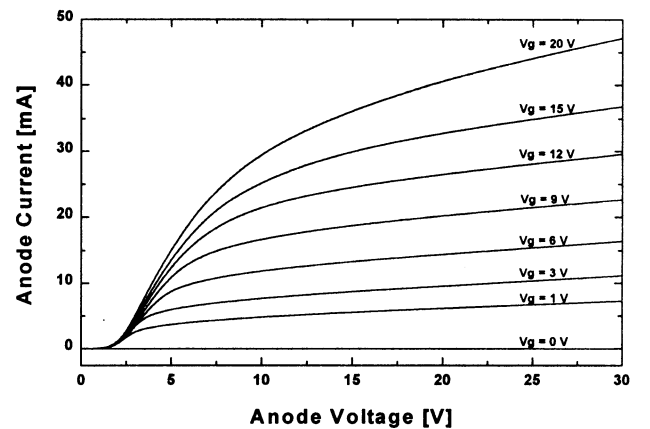


Figure 6. Experimental I - V characteristics of the proposed SOI LIGBT.

Chaos Generator MMIC's Using Resonant Tunneling Diodes

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Recently, applications of chaos, which is often observed in nonlinear circuits, have been studied intensively in the field of information processing and communication systems [1]. Using resonant tunneling devices to make such nonlinear circuits has many advantages, for example, simplicity in circuit, high operation frequency and low power consumption. In this paper, we report the demonstration of high-frequency operations of the chaos generator microwave monolithic ICs consisting of an RTD and a high electron mobility transistor (HEMT).

Figure 1 shows the configuration of the fabricated circuit. This chaos generator circuit consists of a resonant tunneling diode, an inductor L and a capacitor C . This circuit can be regarded as a van der Pol oscillator, and with oscillating input the circuit outputs various signal patterns including chaos [2]. The HEMT works as an open-drain output buffer, which is essential for high frequency operation since the measurement system disturbs the proper operation without it.

The circuits were fabricated using InP-based RTD/HEMT integration technology [3]. Figure 2 shows schematic cross section of the fabricated devices. The gate length of HEMT was 1.5 μm . The circuit parameters were varied in the range of $L = 1.15 - 5.9 \text{ nH}$, and $C_{\text{tot}} = 0.48 - 1.03 \text{ pF}$, so that the characteristic frequency $f_c (=1/2\pi(L C_{\text{tot}})^{1/2})$ was about 3.0 – 6.8 GHz. Here, C_{tot} is a sum of the capacitance C and the gate capacitance of the HEMT. The static current-voltage characteristics of the fabricated RTD are shown in Fig. 3. In this measurement, we used the negative voltage range of the RTD. The peak voltage of the RTD was about -0.25 V , the peak current density was $4.5 \times 10^4 \text{ A/cm}^2$, and the peak-to-valley current ratio was about 5 at room temperature.

The fabricated ICs were tested on a wafer with microwave probes. We have observed various signal patterns depending on the input signal frequency, its amplitude, and DC offset voltage. These patterns include 1/2, 1/3 frequency dividing signals, and chaos. Figure 4 shows the examples of the input and the output wave patterns at around 5.0 GHz for the device having the characteristic frequency of 3.0 GHz. It should be noted that these signal patterns can be chosen, even if the input frequency is fixed, by controlling input signal amplitude or offset bias voltage. This implies various applications including a variable-frequency divider. Moreover, we have observed a 1/2 frequency dividing signal at 12 GHz for the sample having the characteristic frequency of about 6.8 GHz as shown in Fig. 5. This demonstrates that the operation frequency increases in roughly proportion to the characteristic frequency f_c . Consequently, an extremely high operating frequency (much larger than 100 GHz) is expected with appropriate circuit parameters and design, because the characteristic frequency of the RTD can be much higher.

In summary, we have demonstrated the high-frequency operation of chaos generator circuits using a resonant tunneling diode. Various signal patterns including chaos were observed. Moreover, the 1/2 frequency dividing operation was obtained at 12 GHz, which demonstrated the potential of this circuit for ultrahigh-speed dynamic frequency divider applications.

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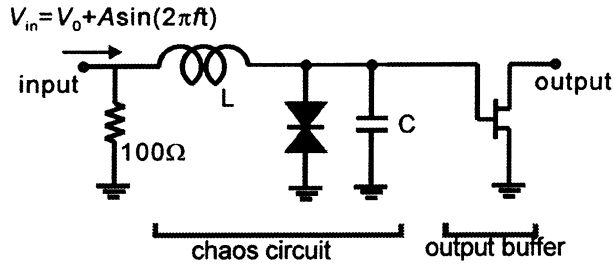


Fig. 1 Circuit configuration of the fabricated circuit

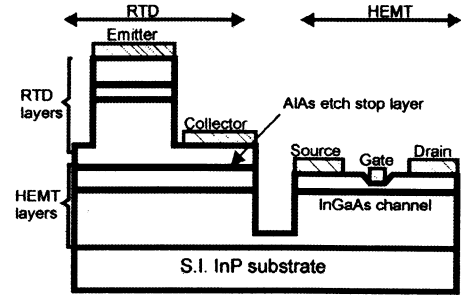


Fig. 2 Schematic cross-section of the fabricated devices

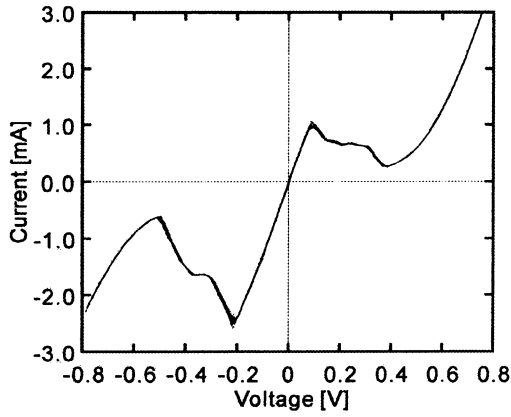


Fig. 3 Current-voltage characteristics of the fabricated RTD

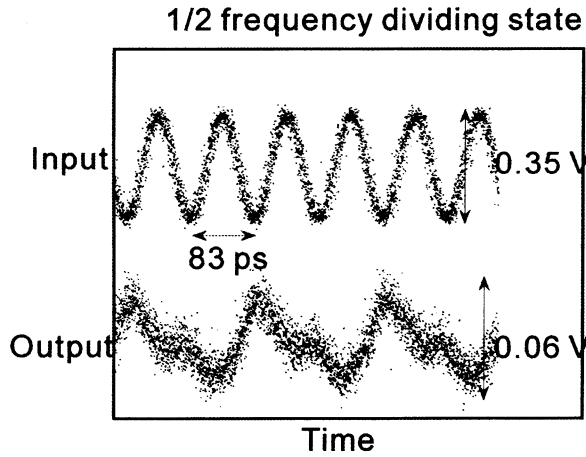
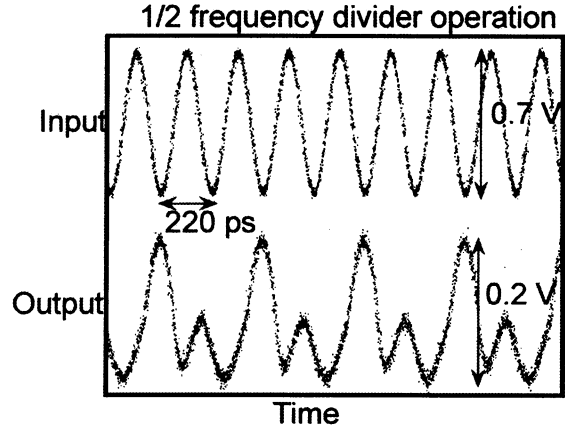


Fig. 5 Input and output waveforms of the circuit. A 1/2 frequency dividing signal at 12 GHz. The circuit parameters were $L=1.15$ nH and $C_{tot} = 0.48$ pF.

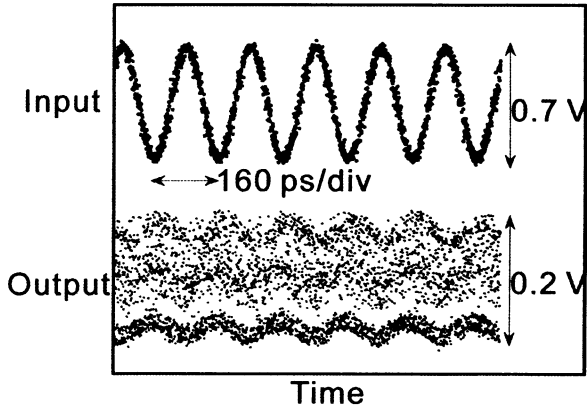


Fig. 4 Input and output waveforms of the circuit. The circuit parameters were $L=5.9$ nH and $C_{tot} = 0.48$ pF. (a) 1/2 frequency dividing signal at $f=4.5$ GHz, (b) chaos at 6.0 GHz.

High detectivity solar blind AlGaIn metal-semiconductor-metal detector

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GaN/AlGaIn/InGaIn materials are now widely used for LEDs, lasers, high power high frequency transistors and ultraviolet detectors. Concerning the latter, solar blind detectors are needed for various applications such as missile launching warning systems, fire and flame detection and medical monitoring of UVA and UVB radiations.

We have fabricated and characterized a solar blind detectors based on AlGaIn. The structure was grown on Si(111) by molecular beam epitaxy. After an AlN buffer, a GaN/AlN bilayer was grown, followed by a 1.6 μ m AlGaIn layer, with about 50% Al. The process includes an optical lithography and PtAu Schottky contact deposition, and lift off. Interdigitated finger were fabricated, with a finger width of 2 μ m and a spacing of 2 μ m between fingers. The total detector area is 100 μ m $\times$ 100 μ m. The current was extremely low, in the pA range for biases up to 50V. The photoresponse spectrum is shown in figure 1 : the cut-off wavelength is 280nm, making this detector solar blind. The cut-off is very sharp, with 3 decades near UV rejection, limited by the contribution of the GaN layer. Below 365 nm, the rejection is larger than 4 decades. At 20V the response is 22mA/W, and is 44mA/W at 40V, corresponding to 20% quantum efficiency. Figure 2 shows the bias dependence of the response : it increases first sublinearly, due to the electric field being mostly limited to the depletion region below the contacts, and then linearly when the field distribution becomes more homogeneous when the contacts start to inject more current. Figure 2 also shows the noise measurements. The noise is below our experimental limit (a few 10⁻¹⁵ A/ $\sqrt$ Hz) for biases up to 80V. At higher biases, current increases and noise is dominated by 1/f noise. The power spectral density of noise can be approximated by PSD=2eI+ β I²/f +constant, with β = 4 $\times$ 10⁻⁴. This allows to extrapolate the noise to lower currents. The constant was in a conservative approach set to 10⁻³⁰ A²/Hz, which obviously gives an upper limit for the noise. The detectivity deduced from the response and noise measurements is shown in figure 3. The value is below 10¹³ $\sqrt$ Hz/W for biases from 10 to 50V, but large uncertainties remain due to the difficult noise measurements. When replacing the measured noise by the extrapolated noise, the extrapolated detectivity reaches 2.5 $\times$ 10¹³ $\sqrt$ Hz/W. As the noise for low biases is white and the response fast, this detectivity is obtained at any frequency ; in particular, at 50Hz, the detectivity D =2.5 $\times$ 10¹³ / $\sqrt$ 50= 3.5 $\times$ 10¹² /W is obtained, corresponding to a noise equivalent power of 0.3 pW. This performance represents the state of the art for solar blind MSM detectors based on AlGaIn, and is very promising for applications. It also shows that extremely high quality AlGaIn/GaN layers can be grown on Si(111).

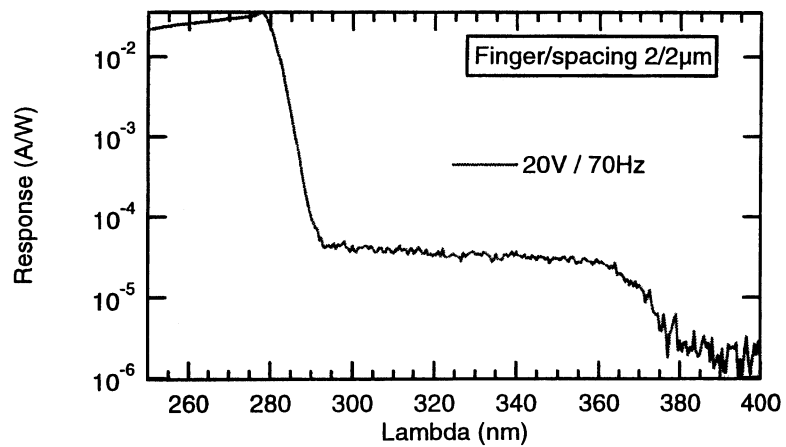


Figure 1

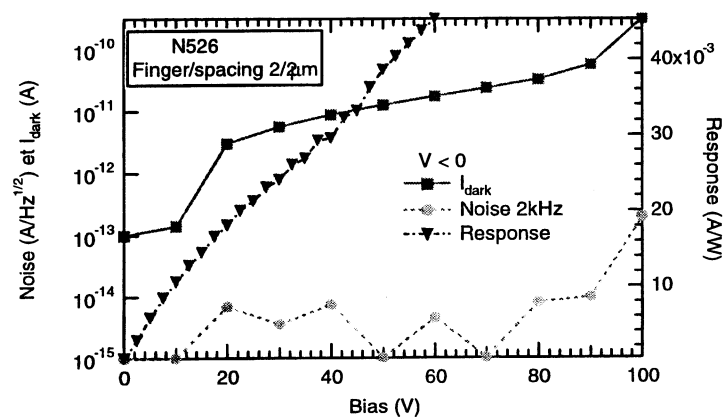


Figure 2

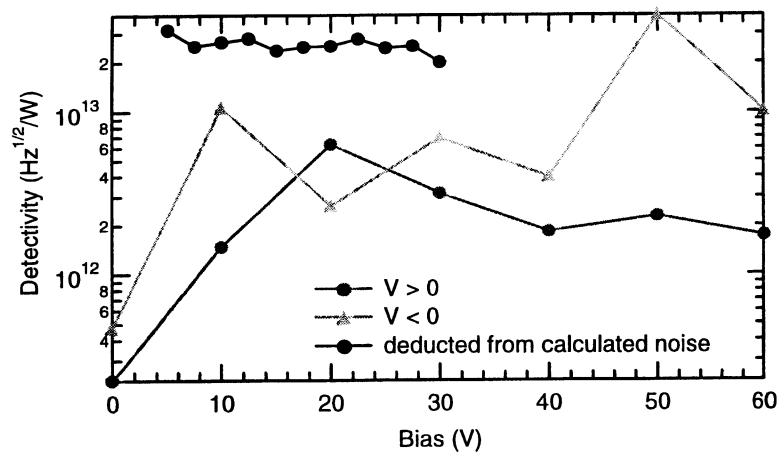


Figure 3

Characterization of a 0.1 μm MOSFET using cross-sectional scanning tunneling microscopy

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Since MOS structures are now getting smaller, it has become more important to directly evaluate their structures. We have used scanning tunneling microscopy/scanning tunneling spectroscopy (STM/STS) to characterize the structural and electrical properties of Si nano *pn* junction. We have reported that three different *n*-type, *p*-type, and depleted regions can be visualized through the H-terminated surface with STM.[1] It is required to get properties such as channel length, carrier concentration in the channel region, and the width of depleted regions around source/drain (S/D). In this work, we visualize a 0.1 μm -scaled MOSFET structure on a nanometer scale using cross-sectional STM.

An *n*-channel MOSFET structure was fabricated by an electron beam lithographic technique and As ion implantation on Si(001). After patterning of lines evenly spaced with periodicity of 300 nm, poly-Si gates deposition and As ion implantation for shallow S/D was performed, then poly-Si was deposited as a protective cap layer. Rapid thermal annealing was carried out at 1000 °C. The (100) and (110) cross sections were polished to realize smooth surfaces. Samples were dipped into a solution (HF : HCl = 1 : 19) to remove oxide and leave hydrogen-terminated surfaces. STM measurement was performed in a constant current mode.

Figure 1 shows a topographic STM image of the MOSFET observed through a H-terminated (100) cross section. This image was taken at a sample bias voltage of 6 V and a tunneling current of 0.2 nA. In the middle of the image, S/D regions are clearly seen as shown in a schematic illustration (Fig. 2). It is estimated that the depth of the S/D regions is approximately 65 nm. A bright area at the top indicates a gate, while notably dark regions beside the gate do the spacer oxide. The STM image also shows the dark region in the *p*-type substrate surrounding the S/D. The dark contrast means that the tip approaches to the surface to keep the tunneling current constant. It is considered that the dark region shows the depleted region of the MOSFET. Thus, the local carrier concentration can be roughly obtained. The channel region of the MOSFET can be seen between the source and the drain. The length of the channel region is approximately 90 nm in the STM image. The actual channel length is estimated to be about 64 nm because the cross section is realized by cutting at an angle of 45° with the direction along the lines and spaces. In the STM image of (110) cross section (Fig. 3), even the thin gate oxide is observed as a dark line under the gate. It reveals high spatial resolution and the great ability to characterize device structures by STM.

A MOSFET structure was visualized in a nanometer scale using STM. Topographic STM images show the S/D regions, the poly-Si gate, and the very thin gate oxide layer on a nanometer scale. The results show that STM is a powerful technique to determine the depth of the S/D, the channel length, and the local carrier concentration.

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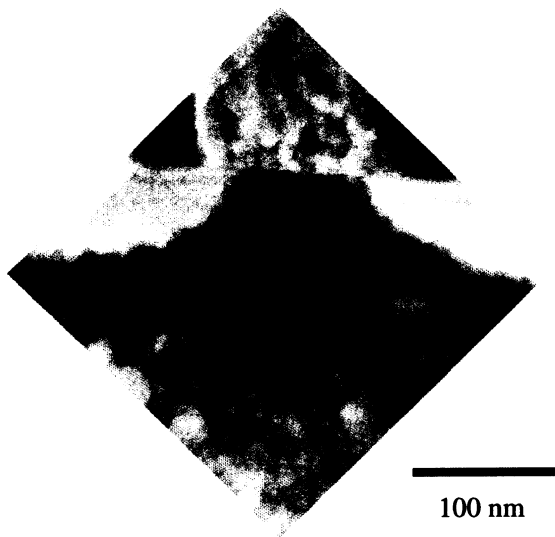


Fig. 1: Cross-sectional STM image of the MOSFET taken at $V_s = 6$ V and $I_t = 0.2$ nA.

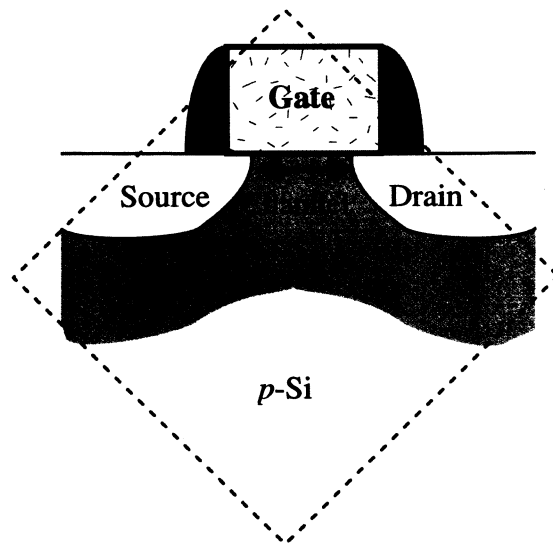


Fig. 2: Schematic illustration of the observed area.

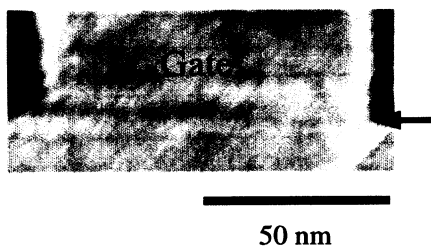


Fig. 3: Cross-sectional STM image of the gate oxide taken at $V_s = 4$ V and $I_t = 0.2$ nA.

Nanoscale MOSFETs Scaling

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Prospects of MOSFET scaling deep into nanoscale region, beyond the projections of the International Technology Roadmap for Semiconductors [1] are of a primary importance for the future of the industry and information technology.

We have carried out numerical modeling of room-temperature operation of silicon, dual-gate SOI MOSFETs with ultra-thin, intrinsic (undoped) channel connecting bulk, n^+ -doped source and drain (Fig. 1). If the channel length L is of the order of 10 nm, electron-phonon and surface roughness scattering inside the channel may be neglected, and electron transfer is ballistic [2, 3]. Nevertheless, this transfer still may be well controlled by gate voltage, at small but practical thickness of gate oxide (t_{ox}) and channel (t). In contrast with the preliminary analytical model [4], in our present work the device electrostatics including band bending in source, drain and gate, has been treated explicitly using a numerical Poisson solver, and quantum-mechanical electron tunneling along the channel (under the maximum of the electrostatic potential created by the gate) has been taken into account self-consistently.

The results show that the current saturation in very short MOSFETs is due to the transport bottleneck at the electron entrance into the channel, due to electron confinement both in energy and the spatial direction across the channel. Due to this effect, room-temperature devices as short as 8 nm still have high transconductance (Fig. 2), relatively small DIBL effect (Fig. 3) and acceptable voltage gain (Fig. 4). This is why they seem quite suitable for nearly all digital applications, though rather high gate voltage threshold roll-off [3] may make the device reproducibility and VLSI circuit yield rather challenging.

We have also used our results to study power scaling of logic circuits based on nanoscale MOSFETs, using a simple phenomenological model in which the total power consumption P is the sum of dynamic power CV_{DD}^2f and static power proportional to $J_{OFF}V_{DD}$. (C is the total effective interconnect capacitance and V_{DD} is the voltage swing.) The results (Fig. 5) show that in contrast to the situation in the drift-diffusion mode, in the ballistic regime both minimum value of P and the corresponding optimum V_{DD} increase as the channel length decrease. This fact may have substantial implications for the development of nanoscale CMOS technology.

At the meeting we will also address other characteristics of nanoscale ballistic MOSFETs, including their high-frequency properties (internal switching speed, f_i and f_{max}) and current noise.

Helpful discussions with D. Frank, C. Hu, S. Laux, M. Fischetti, M. Lundstrom, S. Luryi, J. Palmer, P. Solomon, Y. Taur, S. Tiwari, and H.-S. P. Wong are gratefully acknowledged. The work was supported in part by DARPA via ONR and by SRC.

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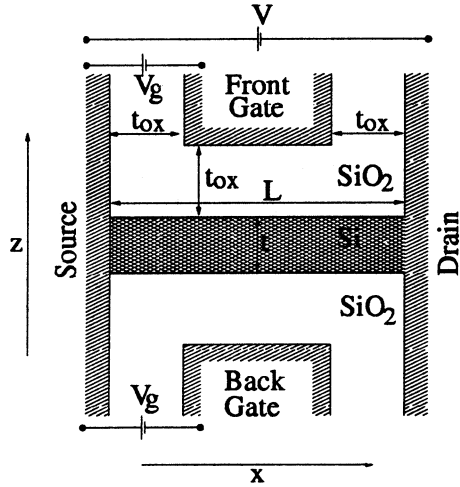


Figure 1. The model of dual-gate MOSFET, used in this work.

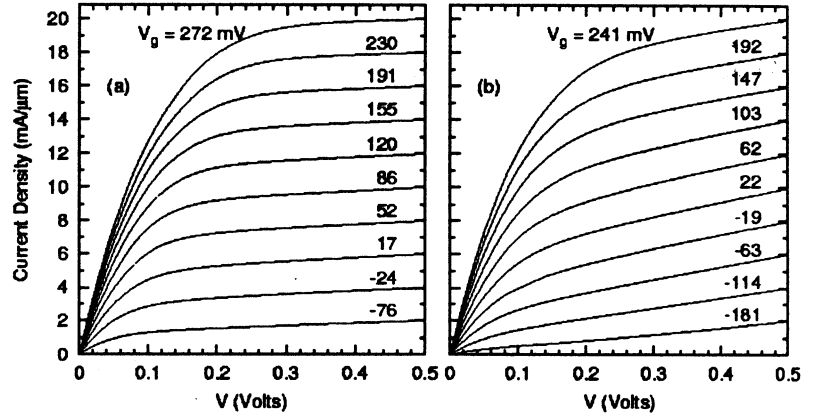


Figure 2. Source-drain I - V curves of transistors with (a) $L = 12$ nm and (b) $L = 8$ nm, for 10 values of gate voltage, at room temperature. Here $t_{ox} = 1.5$ nm; $t = 2$ nm, $T = 300$ K.

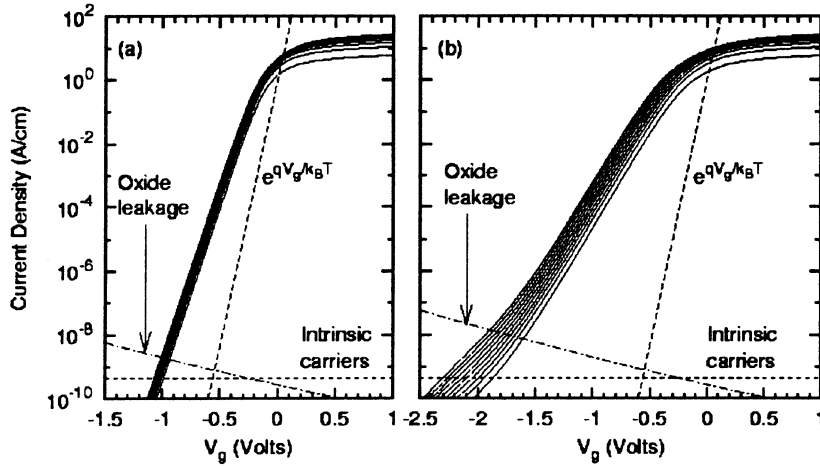


Figure 3. Subthreshold curves of the almost the transistors as in Fig. 2, but with $t_{ox} = 2.5$ nm, for 10 values of source-drain voltage V . Almost-vertical dashed lines: the 60-mV-per-decade slope of an ideal transistor with classical charge transfer. Horizontal dashed lines: the limit below which our disregard of intrinsic carriers is no more valid. Dot-dashed lines: the gate oxide current. $T = 300$ K.

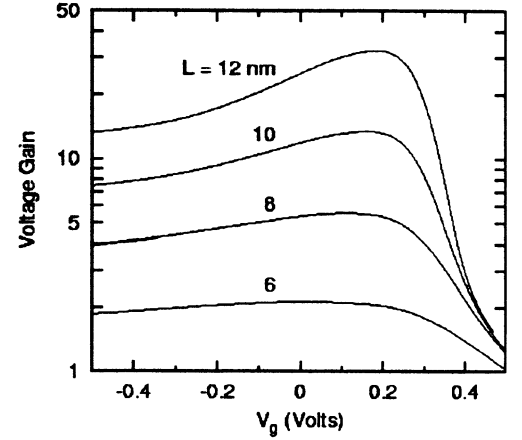


Figure 4. Voltage gain $G_V \equiv \partial V / \partial V_g|_{I = \text{const}}$ as a function of gate voltage for various channel lengths at $T = 300$ K and $V = 0.3$ V. $t = 2$ nm, $t_{ox} = 1.5$ nm.

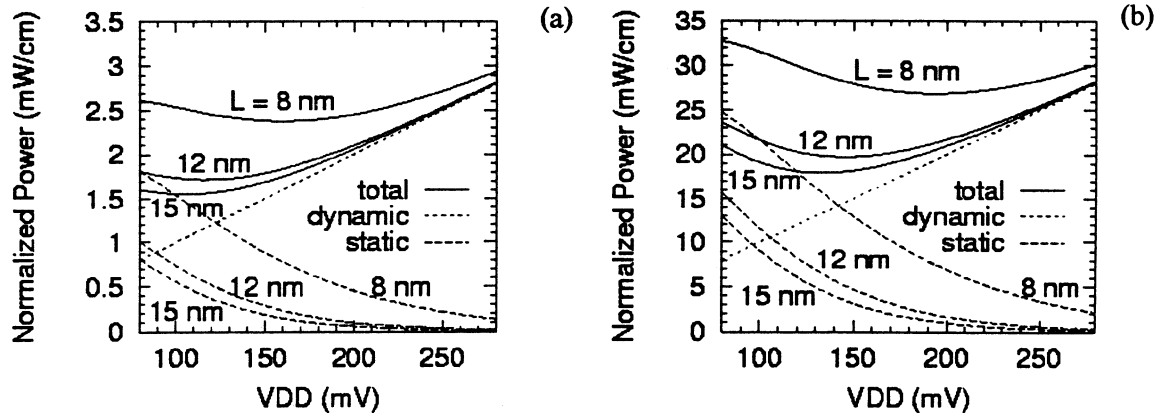


Figure 5. Total power per unit transistor width as a function of V_{DD} for (a) $J_{ON} = 0.1$ A/cm and (b) $J_{ON} = 1.0$ A/cm for various channel lengths at $T = 350$ K. $t = 2$ nm, $t_{ox} = 1.5$ nm. The on-current level determines the circuit speed. For circuits with $\sim 10^9$ transistors per cm^2 , the former level corresponds to ~ 10 GHz clock frequency.

50 nm Vertical Surround Gate MOSFET with S-factor of 75mV/dec

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ABSTRACT

Vertical MOSFETs (VMOS) have a potential to improve short channel effects and to increase the integration density [1,2]. The vertical replacement-gate (VRG) MOSFET with 50 nm channel length on 300 nm Si wall [3] and the vertical sub-100 nm MOSFETs on MBE Si island by electric field tailing [4] were reported. In the previous work, the Si island was not fully depleted and thus S factor remains large (90-140 mV/dec). In this paper, we report the fabrication and device characteristics along with simulation results of **fully depleted** vertical MOSFETs.

The I_{ds} vs V_{gs} curves and the threshold voltage roll-off simulated with a revised charge-sharing. The threshold voltage roll-off is shown to be critically governed by the Si wall thickness t_{Si} and as the Si wall becomes thicker than 200 nm, there are no major advantages of the threshold voltage roll-off over the conventional planar MOSFET. For the surround gate MOSFETs with Si wall thickness less than 50 nm, however, it need only a 10 mV surface potential to fully deplete the channel (or 5 mV for half of the channel) if the channel doping is around 10^{17} cm^{-3} . In this case, the subthreshold swing approaches the ideal value (60 mV/dec) of fully depleted SOI and the channel length may be reduced to 20 nm for the vertical device with gate oxide thickness of 2 nm, instead of 50 nm for planar device since the short channel effects are attenuated. The relative g_m may also be increased to 2.3 S/mm and 1.3 S/mm and f_T may reach to 265 GHz and 150 GHz, for n channel and p channel, respectively when the carrier over shoot effect is included.

A self-aligned process was developed for fabricating VMOS on extremely thin 50 nm Si islands with current manufacturing tools. Using a 248 nm stepper combining with the antireflective coatings (ARC) technology, 200 nm wide and 570 nm thick photoresist patterns were fabricated as RIE masks. With RIE undercut control, uniform 50 nm thick Si wall arrays with an aspect ratio of more than 50 were fabricated reproducibly for subsequent VMOS process. The bottom drain was formed by self-aligned n^+ implantation shown in Fig. 1-e. The surround gate and the top source were doped at the same time by self aligned n^+ implantation after CMP of poly Si and etching back (Fig. 1-g). A subsequent LPCVD SiO_2 deposition for isolation was followed by CMP planarization and via hole etching to form the structure for contact (Fig. 1-h) and the top source, surrounding gate and bottom drain were exposed for self aligned silicide and metal deposition. The SEM micrograph of the completed VMOS exposed by focus ion microbeam milling is shown in Fig. 2. The device was fabricated on a 50 nm thick, 600 nm high and $2 \mu\text{m}$ long vertical Si wall. The footprint of each device is only $0.1 \mu\text{m}^2$. The device has a 280 nm gate length, $4 \mu\text{m}$ gate width ($2 \mu\text{m}$ Si wall length) and 20 nm gate oxide. From the I-V characteristics of Fig. 3 and 4, a subthreshold S-factor of 75 mV/dec close to the ideal SOI value was obtained, indicating fully depleted SOI islands. Minimal short channel effects were also seen. Because of the large ohmic contact resistance on nano top source and scattering in the reversion layer caused by roughness of the vertical channel surface, the transconductance g_m was low (40 mS/mm) and these may be improved by the using cobalt silicide and by smoothing the channel surface with oxidation. Design of a novel VMOS structure was also accomplished in order to improve the device speed/frequency performance by minimizing the overlap capacitance of the gate and the source.

A single VMOS integrated with bi-stable quantum tunneling diodes may be used to form low power (40× lower), high density (comparable to that of DRAM) SRAM. Likewise, the integration density for vertical standard macro cells can be increased by a factor of >10, >6 and >30 for inverter, NAND and SRAM, respectively, when compared with planar technology.

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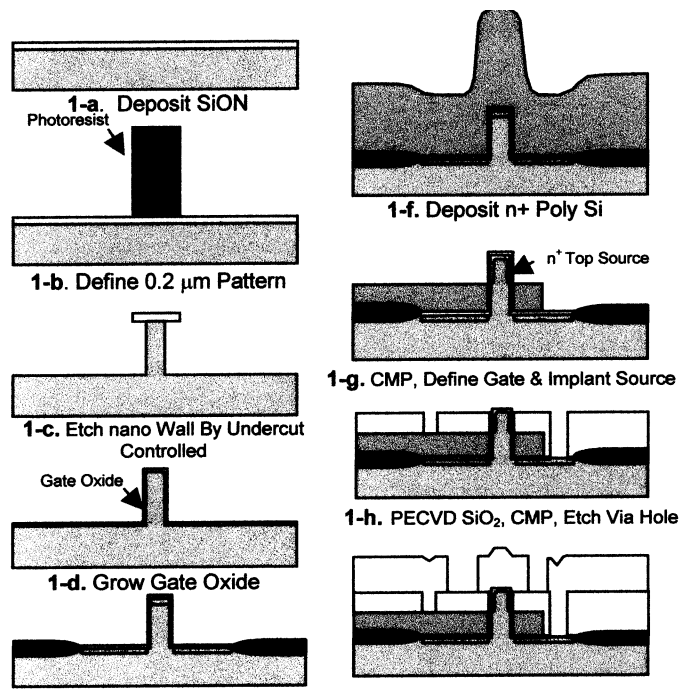


Fig. 1. Process flow for vertical NMOSFET. **1-a** SiON deposition is for antireflective coatings (ARC) and a later oxidation process; **1-b**. 200 nm wide photoresist patterns are used as RIE masks with a 248 nm stepper; **1-c**. With RIE undercut control, 50 nm vertical Si wall can be obtained; **1-d**. Oxidation is employed for annealing damages, smoothing surface roughness and gate oxide processing. **1-e**. The As implantation energy is 150 keV, and the dose is $3 \times 10^{15} \text{ cm}^{-2}$ to form the bottom drain; **1-f**. Deposition of n+ poly Si should be thicker than the height of the Si wall in order to CMP and etching back. **1-g**. After CMP planarization, the gate length may be controlled by poly Si etching. Poly Si gate is used as the implantation mask to realize the self align for gate and top source doping; **1-h**. LPCVD SiO_2 is for the isolation between the surround gate and top source. For metal contact, the top source is exposed by CMP, the gate and bottom drain by via hole etching; **1-i** Cobalt silicide may improve nano size ohmic contact.

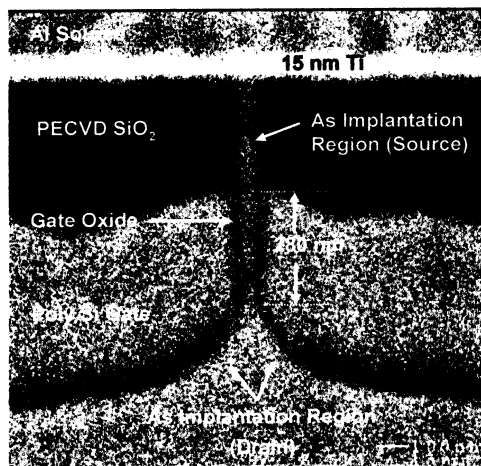


Fig. 2. SEM image of a vertical MOSFET on a 50nm Si wall exposed by focus ion microbeam milling.

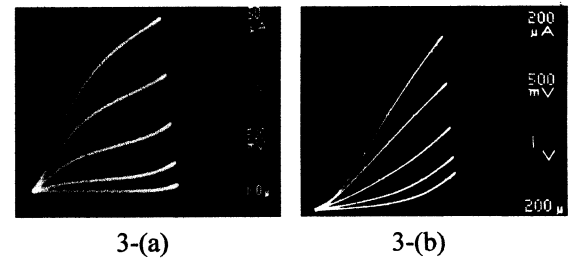


Fig. 3. (a) I-V characteristics of the device on the 50 nm thin Si wall and (b) on 1μm thick Si wall. Both devices have a 280 nm gate length, 4 μm gate width (2 μm Si wall length) and 20 nm gate oxide. For fully depleted VMOS, short channel effects were minimized.

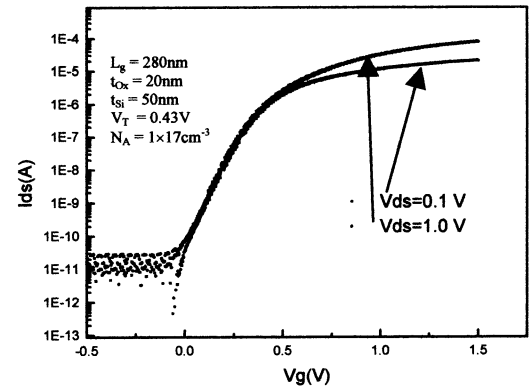


Fig. 4. 75mV/dec of S-factor for VMOS on the 50nm thick Si wall, approaching the close ideal value of fully depleted SOI. For a device fabricated on a 80 nm wide Si wall, a larger S value of 81 mV/dec was obtained.

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Hyperspectral Imaging of Breakdown in InAlAs/InGaAs HEMTs: a Comparative Study

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Although InAlAs/InGaAs HEMTs offer promise for high-speed, high power applications, both off-state and on-state breakdown voltages in this material system tend to be poor. One promising avenue for understanding breakdown is the study of photon emission. Previous examinations of emission in this material system and in the AlGaAs material system have generally been limited to investigations of a single device.[1]-[3] In this work we will present a comparative investigation of emission at breakdown in a set of InAlAs/InGaAs HEMTs that includes devices with a wide range of doping levels. Such a comparison allows us to understand better the tradeoffs in device design, as well as helping us to identify when/if different breakdown mechanisms may be at play.

In order to track photon emission at breakdown, we have developed a computer-controlled system which allows hyperspectral imaging of photon emission (fig. 1). The device set studied consists of three high performance InAlAs/In_{0.67}Ga_{0.33}As HEMTs.[4] All have $L_G \approx 0.1 \mu\text{m}$ as well as nominally identical insulator and channel thicknesses of 200 Å. The only major difference is sheet carrier concentration, which ranges from $2.82 \times 10^{12} \text{ cm}^{-2}$ (low n_s) to $3.66 \times 10^{12} \text{ cm}^{-2}$ (high n_s). These different doping levels lead to substantially different breakdown voltages: off-state breakdown voltages range from $BV_{DG} = 6.1 \pm 0.1 \text{ V}$ for the low n_s device to $BV_{DG} = 3.5 \pm 0.3 \text{ V}$ for the high n_s device.

The devices exhibit significant emission both in off-state and in on-state breakdown (see fig. 2 for an example of visible emission). As has been observed in other devices, visible emission is from the drain edge, and is not entirely homogeneous along the gate edge nor between the two fingers. Using the imaging spectroscopy capabilities of our system, we are also able to extract information about the energy distribution of emitted photons. In fig. 3 we plot a typical spectrum. Note that due to our use of the imaging spectrograph, we can easily extract information about each gate finger independently. Both gate fingers on this device yield a similar energy distribution of photons; we observe (1) a small peak around 1.5 eV, which presumably corresponds to some real-space transfer and subsequent recombination in the InAlAs, and (2) a highly Maxwellian energy distribution for energies greater than about 1.6 eV. This feature allows us to define an effective carrier temperature for high energy carriers in the device.

Previous work comparing off-state and on-state breakdown in AlGaAs HEMTs has shown that higher electron temperatures are often associated with off-state breakdown.[1] In figure 4 we present a comparison of temperatures at off-state and on-state breakdown for three devices. Two interesting features emerge: first, the lightly doped device exhibits higher temperatures both in the off-state and in the on-state than the devices with higher n_s . Second, while the low n_s device shows the expected drop in temperature in the on-state, the devices with higher doping exhibit slightly *higher* temperatures in on-state breakdown.

The disparity between the low n_s device and the other devices is particularly interesting, as it suggests that breakdown mechanisms in this device may be different from the mechanisms in devices with higher carrier concentration. For example, we have previously suggested that in many InAlAs/InGaAs HEMTs, breakdown in the off-state is largely due to thermionic field emission from the gate. However, recent measurements suggest that impact ionization may play some role in lightly doped devices, probably due to the greater spatial extent of the high field region in such devices (see fig. 5). Such increased spatial extent of the field could lead to increased electron heating in the off-state. These results may help explain why improved off-state breakdown, which is often achieved through wide recesses or reduced doping, does not always correlate strongly with improved reliability.[5]

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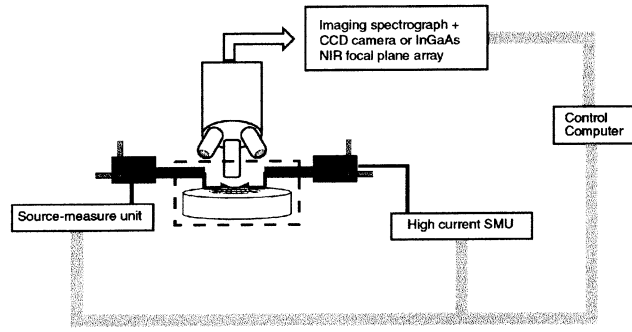


Fig. 1 - Schematic diagram of system used in this work. Emitted photons are collected by the microscope, and fed to an imaging spectrograph that is equipped with a mirror grating as well as gratings blazed for the visible and for the NIR. For imaging in the visible, a scientific CCD camera is placed at the exit port of the spectrograph; for NIR imaging, an InGaAs focal plane array is used.

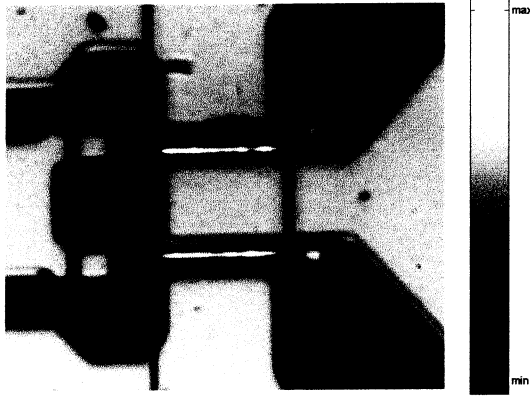


Fig. 2 - Typical image of emission at on-state breakdown ($n_s = 3.66 \times 10^{12} \text{ cm}^{-2}$, $I_D = 300 \text{ mA/mm}$, $I_G = -1 \text{ mA/mm}$, $V_{DG} = 2.3 \text{ V}$).

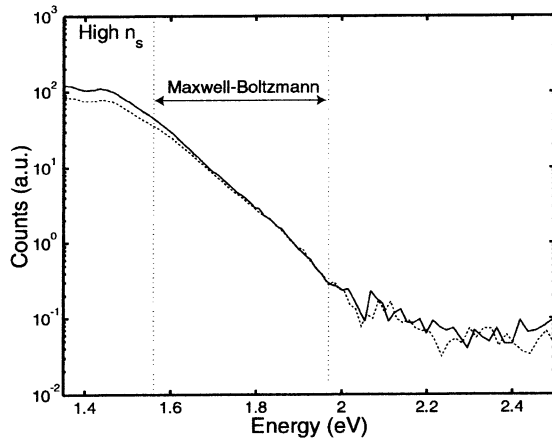


Fig. 3 - Typical spectrum of emitted photons (each line corresponds to emission from one of the fingers). The energy distribution is Maxwellian over a large range.

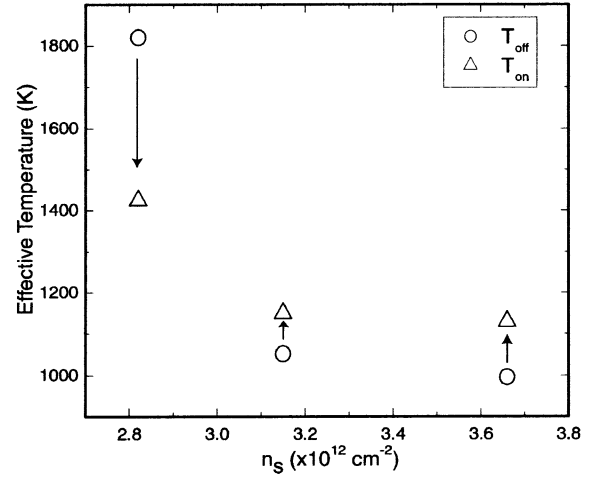


Fig. 4 - Comparison of effective carrier temperatures at both on-state and off-state breakdown as a function of doping level.

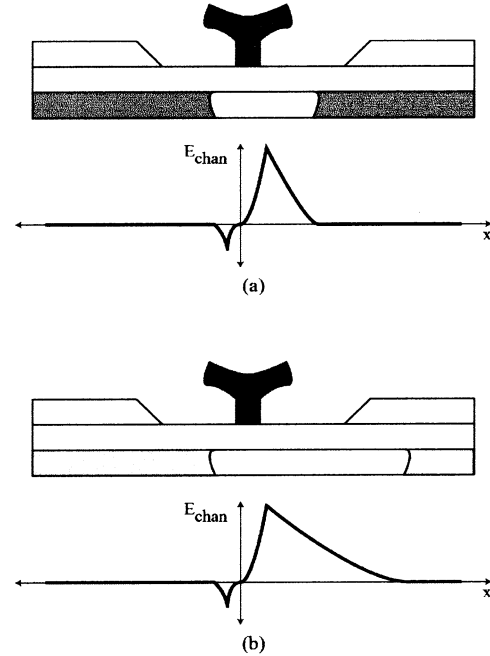


Fig. 5 - Model for the higher carrier temperatures observed in the low n_s device in off-state breakdown. (a) shows the a highly doped device and the corresponding field within the channel ; (b) shows a more lightly doped device. If breakdown is largely determined by the peak field, then breakdown in a more lightly doped device should correspond to higher carrier temperatures, as the spatial extent over which heating can occur is increased.

Extension of Safe-Operating-Area by Optimizing Body-Current in Submicron LDMOS Transistors

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We present the extension of Hot-Electron-Limited SOA and Electrical SOA by optimising the two peaks of body current in 20V LDMOS Transistors. The LDMOS has two peaks of body current and the origin of two peaks can be explained through hot carrier injection phenomenon. The first peak shows the appearance of weakly impact ionization related to the device degradation and the second peak shows the occurrence of snap-back phenomenon predicting device destruction, respectively.

The indicating numbers in Fig. 2 and Fig. 3 show the extended H-E SOA by optimizing of body current. The number 1 indicated the extension when the first peak is lower and the number 2 indicated the extension when the second peak occurs later. The body current depends on the p-body diffusion (n-channel device) and the n-type drift region doping concentration. From the process design point of view, the first peak of body current must be lower to increase device on-state breakdown voltage and the second peak must occur later to prevent device destruction by snap-back phenomenon.

Using the above analysis, we simulated 40V LDNMOS transistor through optimization of p-body and drift doping concentration. Fig. 4 and Fig. 5 show that the shift of the maximum impact ionization position and the change of maximum value were caused by Kirk effect. At high V_{gs} the drain current is higher and the charge of moving carriers compensates for the drift region with n-type dope, involving a shift of potential lines toward the high concentration drain. Therefore, the body current showed the increased value very steeply because of the increased ionization coefficient due to the higher drain current and the increased drain-edge electric field. The higher body current makes parasitic-npn operating possible and leads to the snap-back phenomenon, and finally results in unfavorable device destruction. Fig. 6 shows the simulation results after optimizing doping concentration in drift region. We found that the impact ionization rate is distributed all over n-type drift region and maximum peak value is lower despite of higher V_g . Fig. 7 and Fig. 8 show the change of body current and I-V characteristics after optimizing.

Through the above simulation, we confirm that if the first peak is lower the device on-state breakdown voltage increases, and if the second peak occur later the snap-back phenomenon occur later.

It is noteworthy that the first peak must be lower and the second peak later for the best results even though there is a trade-off relationship between them. Therefore, we have to optimize carefully the process design to improve the SOA of LDMOS transistors. Finally, we obtained the optimal process design for the extended SOA in 20V/40V LDMOS transistors that the p-body concentration is moderately lower and the n-drift concentration is higher.

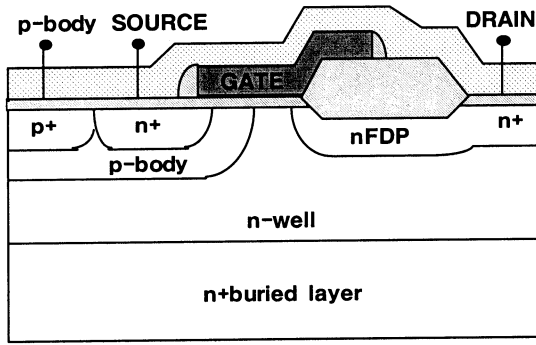


Fig. 1: Schematic of the cross-section in 20V LDMOS

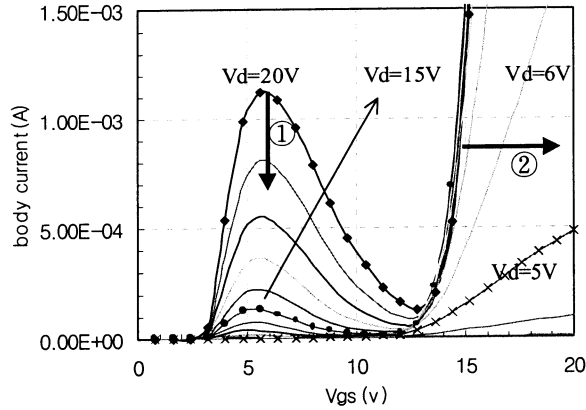


Fig. 2: P-body currents measured at drain voltages of each step

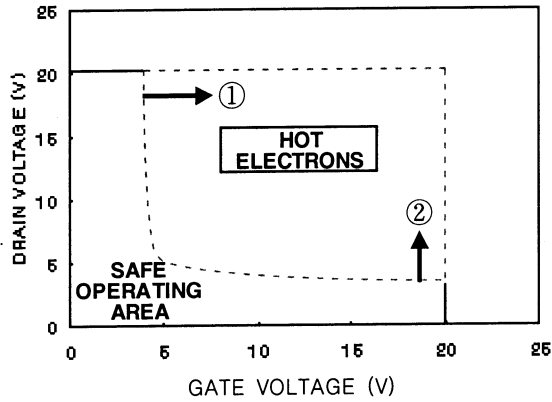


Fig. 3: Hot-carrier-limited safe operating area of a 20V LDMOS

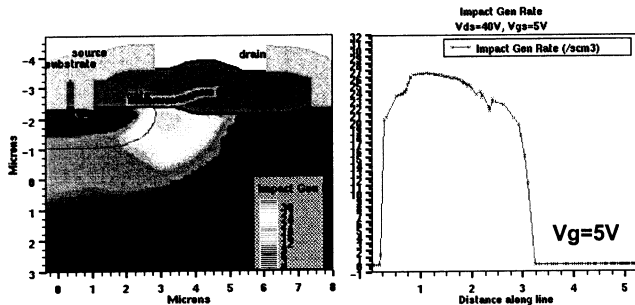


Fig. 4: Impact-ionization rate of LDMOS at $V_d=40V$ and $V_g=5V$

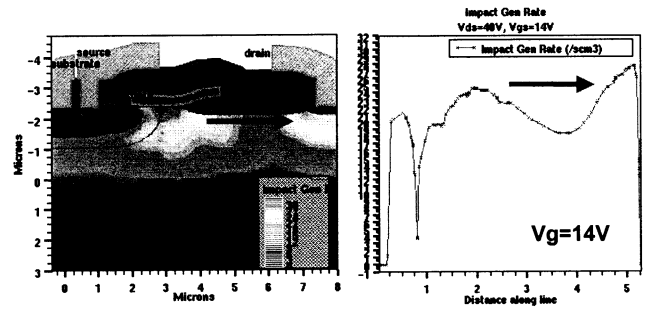


Fig. 5: Impact-ionization rate of LDMOS at $V_d=40V$ and $V_g=14V$

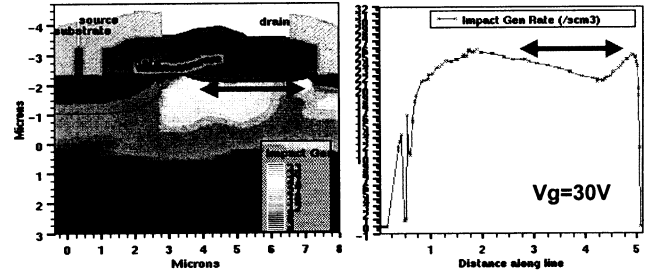


Fig. 6: Impact-ionization rate at $V_d=40V$ and $V_g=30V$ After optimizing

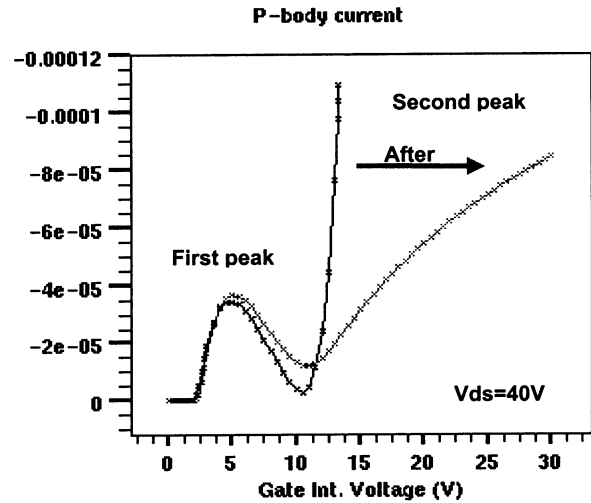


Fig. 7: Body-current after optimizing

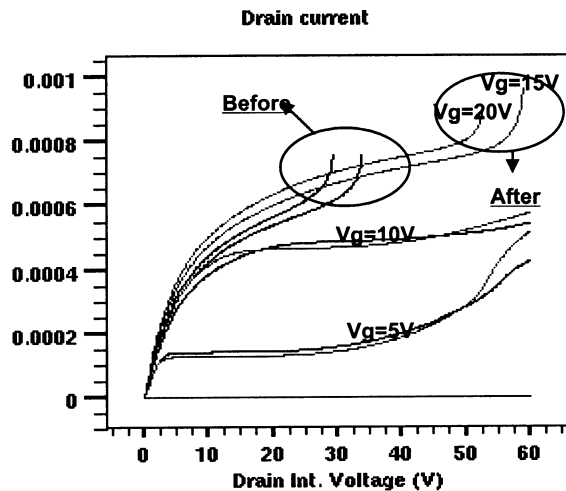


Fig. 8: I-V characteristics after optimizing

Computer Analysis of Geometry and Strain Effects in Silicon Nano-Crystal Floating-Gate Flash Memory Devices

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Non-volatile memory devices based on nano-crystal floating-gate technology have shown great promise for ultra-dense high-endurance memories for low-power applications[1]. The device operation is based on single-electron charging while the low-voltage write and erase operation is the result of direct quantum-mechanical tunneling of electrons or holes through the thin oxide. The possibility of producing nano-crystals of different sizes and shapes, ranging from hemisphere to sphere, has been demonstrated [1],[2].

We use advanced device modeling based on self-consistent 3D Schrödinger and Poisson equations to investigate the detailed operation of nano-crystal memory transistors, focusing on the following:

- The quantization of the many-valley electronic structure and single-electron charging of nano-crystals.
- Effects of simple geometry changes on the nano-crystal electronic states, write voltage and retention time of the device.
- Influence of strain due to SiO₂/Si lattice-mismatch on the nano-crystal electronic states.

The electronic energy levels within the quantum-dot(QD) are obtained by solving three 3-D eigenvalue Kohn-Sham equations, corresponding to the three two-fold-degenerate valley bandstructure($v=X,Y,Z$)(Fig. 1). The possibility of intervalley splitting is not considered here,

$$\nabla M_v^{-1} \nabla \psi_v(r) + \{-q\phi(r) + \Delta E_c(r) + \epsilon_{xc}(n(r))\} \psi_v(r) = E_v \psi_v(r). \quad (1)$$

In Eq. 1, $\Delta E_c(r)$ is the material band offsets between the silicon nano-crystals and the silicon dioxide insulator which provides the hard-wall confinement in the QD. M_v is the electron effective mass tensor that describes different effective masses arising from the anisotropy of the Si bandstructure. The electron-electron interaction in nano-crystal QDs is treated within the density functional theory, with the exchange-correlation potential, $\epsilon_{xc}(n)$, computed from the local density approximation(LDA)[4]. We compute the inhomogeneous strain field at every point according to the continuum strain model by minimizing the elastic energy of the system[5]. The strain energy modifies the electronic potential energies according to the deformation potential theory originating from a first-order bulk strain perturbation Hamiltonian[5] given by,

$$\begin{aligned} \delta E^{(100)} &= \Xi_d^{(100)} (\epsilon_{xx} + \epsilon_{yy} + \epsilon_{zz}) + \Xi_u^{(100)} \epsilon_{xx} \\ \delta E^{(010)} &= \Xi_d^{(100)} (\epsilon_{xx} + \epsilon_{yy} + \epsilon_{zz}) + \Xi_u^{(100)} \epsilon_{yy} \\ \delta E^{(001)} &= \Xi_d^{(100)} (\epsilon_{xx} + \epsilon_{yy} + \epsilon_{zz}) + \Xi_u^{(100)} \epsilon_{zz} \end{aligned} \quad (2)$$

where ϵ_{xx} , ϵ_{yy} and ϵ_{zz} are the position-dependent strain tensor components in the x, y and z directions, respectively. δE are the valley-dependent strain energy contribution to the electronic potential energy for the conduction band valleys along different crystal axes and Ξ are the deformation potential parameters.

We show the sensitivity of nano-crystal electronic spectra to nano-crystal geometry and the resulting in a 60meV variation in the program voltage of the device (Fig. 2). In addition, changes in quantum-mechanical coupling between unbound channel states and bound nano-crystal states due to differences in QD shapes(Fig. 3) can result in retention time variation of several orders of magnitude(Table I). Finally, our investigation of strain effects in the nano-crystal shows subtle geometrical-dependent influence on the QD electronic spectrum with varying degree of sensitivity to the strain(Fig. 4). Further details of the simulation and its results will be discussed at the conference.

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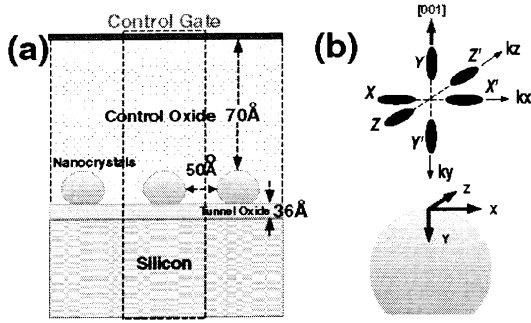


Fig. 1 (a) Schematic of the simulated unit cell of the Metal-Oxide-Semiconductor (MOS) structure with a silicon nanocrystal quantum-dot (QD) embedded in the SiO_2 . (b) Illustration showing the orientation of the nanocrystal QD and the six doubly-degenerate conduction band valleys considered in our model. The valleys are labeled with respect to the orientation of their principle axis in k -space.

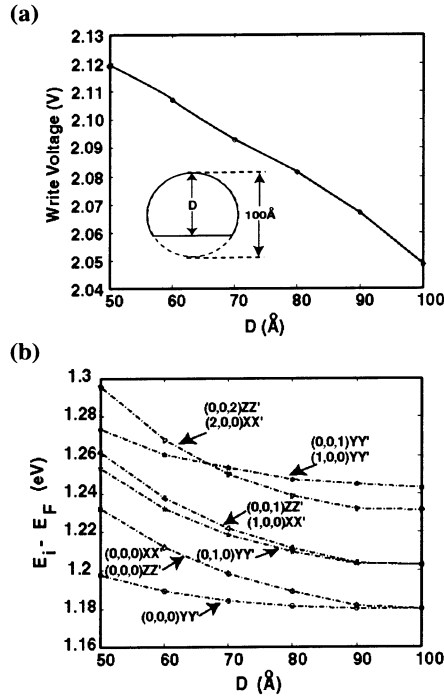


Fig. 2 (a) Write voltage variation with nano-crystal height, D . (b) Variation of first ten quantized electronic levels with nano-crystal height.

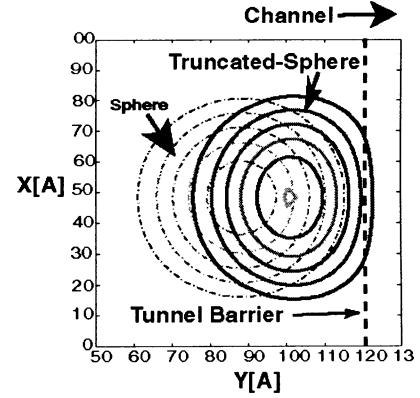


Fig. 3 Contour plots showing the real components of the ground-state wavefunctions for the truncated-sphere and the spherical nanocrystals

SHAPES	RETENTION TIME
Hemisphere	11 Days
Truncated Sphere	3 Months
Sphere	10 Years

Table I. Retention times for a 7-nm-diameter silicon nanocrystals of on a 3.5nm thick tunnel oxide, under flat-band condition of the device.

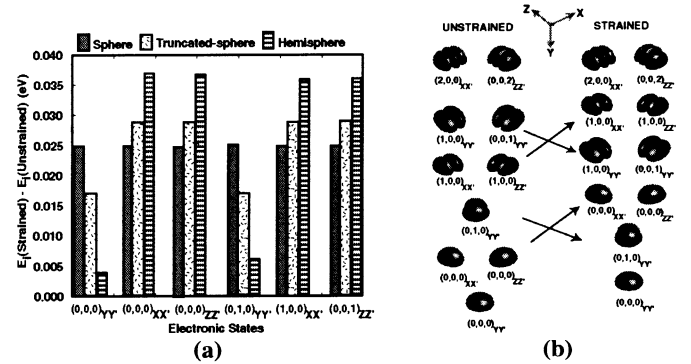


Fig. 4 (a) Energy level difference between the first six quantum states of three differently-shaped strained and unstrained nanocrystals. (b) 3D Iso-surface plots of the first ten wavefunctions in the unstrained and strained hemispherical QD.

An extension of McKelvey's one-flux method to energy space

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McKelvey *et. al.* [1] introduced the one-flux method, based on left-going and right-going fluxes of particles, as an alternative to the drift-diffusion method in describing semiconductor devices. The one-flux method received little attention after Shockley [2] showed its relation to drift-diffusion, until Tanaka and Lundstrom revived it and applied it to HBTs [3]. Recently, Lundstrom [4] has used the one-flux method to discuss the ultimate limitations of FETs.

One assumption in the one-flux method is that carriers move at the thermal velocity. This is not true in the collector of an HBT or the channel of an FET, and yet the one-flux method accurately predicts the fraction of electrons backscattered from those high-field regions [4]. Lundstrom [4] argued that the one-flux method is successful because the backscattered electrons do not penetrate deeply into the high-field region, and so never gain more than an energy kT from the field. Monte Carlo simulations for Si support this argument. But is the argument always true, or does it depend on the semiconductor's material parameters?

To study the limitations of the one-flux method, I propose an extension of the method to account for the energy of the particles. This extension, based on Bringuier's Fokker-Planck approach to the Boltzmann equation [5], [6], reduces the Boltzmann equation from momentum space to energy space. In the continuous-flux method presented here, the left-going and right-going fluxes are considered to be functions of energy and position, so that heating or cooling of the distributions can be treated.

The continuous-flux method is based on the following pair of equations:

$$\frac{\partial}{\partial t} n^\pm \pm \frac{\partial j^\pm}{\partial x} \pm qF \frac{\partial j^\pm}{\partial E} = \pm \left[\left(w_p + \frac{qF}{p} \right) n^- - w_p n^+ \right] - \frac{\partial}{\partial E} (An) + \frac{1}{2} \frac{\partial^2}{\partial E^2} (Bn)$$

Here $n^\pm(x, E)$ are the density of right-going (+) and left-going (−) particles of energy E , $n = n^+ + n^-$ is the total density, $j^\pm(x, E) = n^\pm(x, E)v(E)/2$ is the flux, $v(E)$ and $p(E)$ are the velocity and momentum, and qF is the force on the particle, assumed to be in the positive direction. The coefficients w_p , A , and B , all functions of energy, are related to the scattering mechanisms through the Boltzmann equation. The equations are written for isotropic scattering, but can be extended to anisotropic scattering.

The assumptions underlying the method will be discussed and the method applied to the backscattering of particles from a high-field region. For illustration, the scattering is described by analytical expressions [6], with the energy lost in an inelastic scattering event as a parameter. The backscattered fraction in the continuous-flux method reduces to the one-flux result when this loss parameter is large. In the opposite limit of small energy loss, the backscattered particles penetrate more deeply into the high-field region and gain energy much higher than kT , and the backscattered fraction falls off more slowly with field than in the one-flux result.

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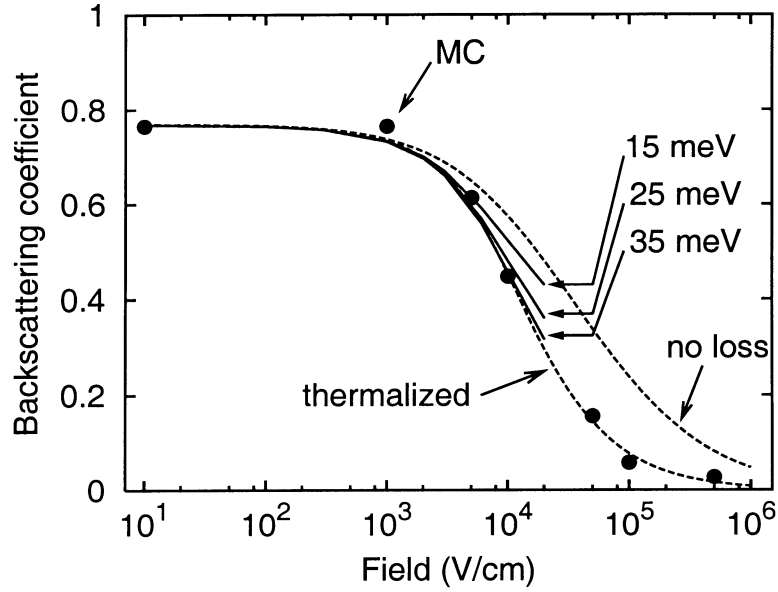


Fig. 1. Backscattering coefficient versus electric field for electrons injected into a Si slab $0.1 \mu\text{m}$ thick. The points are from Monte Carlo simulations in [4]. The lower dashed line is from the one-flux method, and the upper dashed line from an approximate analytical expression based on the continuous flux method, assuming negligible energy loss per inelastic scattering event. The solid curves are for three values of the energy lost per inelastic scattering event, and lie between the limits set by the dashed lines. (The solid curves stop at a field where the numerical solution of the continuous-flux equations becomes inaccurate.)

Characterization of Midgap Tungsten Gate MOSFETs

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Tungsten is one of the most promising candidates for metal gate CMOS technology because of its low resistivity and near ideal mid-gap workfunction. The refractivity of tungsten permits process integration in the very early stages of the standard CMOS technology. Although a low Si/SiO₂ interface trap density D_{it} could be achieved when tungsten is deposited by the magnetron sputtering, the leakage current density for a gate oxide thinner than 6nm becomes unacceptable because of the sputtering damage [1]. For ultra-thin dielectrics, the chemical vapor deposition (CVD) is the preferred method to produce low resistivity thin tungsten films [2]. However, with the high D_{it} in CVD tungsten gate MOS devices, the degradation of mobility of these devices is expected because of the relationship: $\mu_{eff} = 1/(1+\alpha D_{it})$ [3]. We show the mobility of thin oxide CVD tungsten gate MOSFETs can be greatly improved by applying a layer of aluminum on the top of a tungsten gate electrode.

A cross-section of the fabricated tungsten gate MOSFETs is shown in Fig. 1. The starting material for our bulk silicon devices is a p-type, 20 $\Omega\cdot\text{cm}$, (100) silicon substrate. The S/D regions are first defined and implanted with phosphorous through a pad oxide layer. Second, the channel region is defined. The overlap between the gate and the S/D regions is either 5 μm or 10 μm , depending on the particular device structure. Next, a 4.5nm thick gate oxide is grown and the gate material is deposited. For one set of samples, only tungsten is CVD deposited for gate electrode, while for another set of samples aluminum is e-beam deposited after tungsten is deposited to form the Al+W gate electrode. Finally, aluminum is used for interconnects and the devices are annealed in forming gas for 30 min at 400°C.

The I_D - V_G characteristics are taken at a very low drain bias $V_{DS}=10\text{mV}$, which are shown in Fig. 2. The extracted parameters (effective mobility μ_{eff} , surface roughness θ_s , interface trap density D_{it}) [4] are self-consistent, as shown in Fig. 3. For the bulk substrate case, we find the mobility is improved from 258cm²/V-sec for the CVD tungsten gate MOSFETs to 343cm²/V-sec for the Al+W gate MOSFETs. The subthreshold slope is also improved from 100mV/dec to 84mV/dec when aluminum is applied on the top of the tungsten gate electrode. This improvement is attributed to the reduction in Si/SiO₂ interface trap density in the Al+W gate MOS devices. The mechanism we believe is that the water vapor trapped between aluminum and tungsten provides a source of active hydrogen for the passivation to take place. This reduction offers promise for tungsten gate technology as a gate electrode material for future CMOS technology.

Acknowledgements:

The authors would like to thank researchers at IBM T.J. Watson Research Center: S. Guha and L. Ragnarsson for device mask design, C. T. Black and R. Sandstrom for providing lab access, P. Saunders for phosphorous implantation, and H-S Philip Wong for his encouragement and support. This work is supported by DARPA under contract number N66001-97-1-8908.

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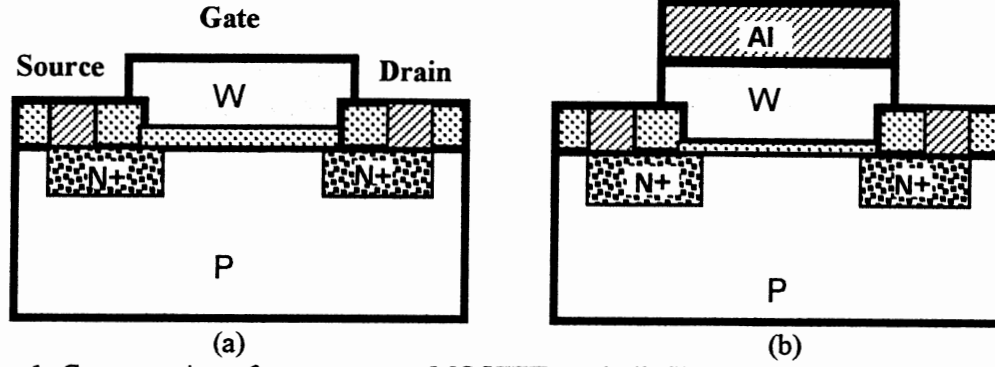


Figure.1: Cross-section of tungsten gate MOSFETs on bulk Si (a) W only (b) Al+W gate.

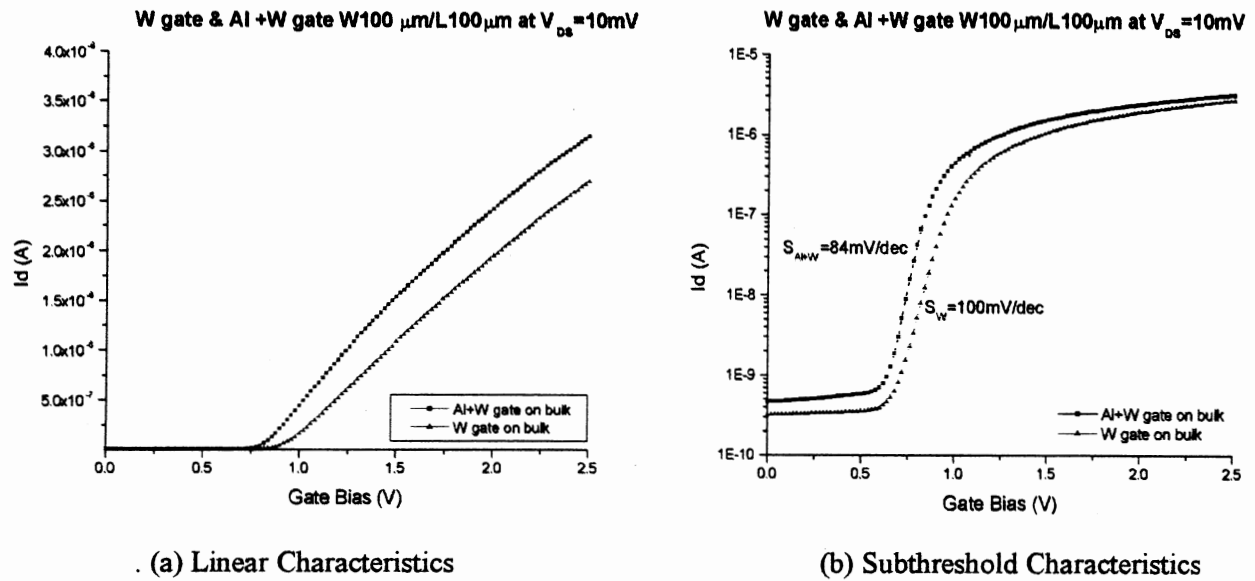


Figure 2: The I_D - V_G characteristics of Al+W and W Gate MOSFETs on bulk Si substrate

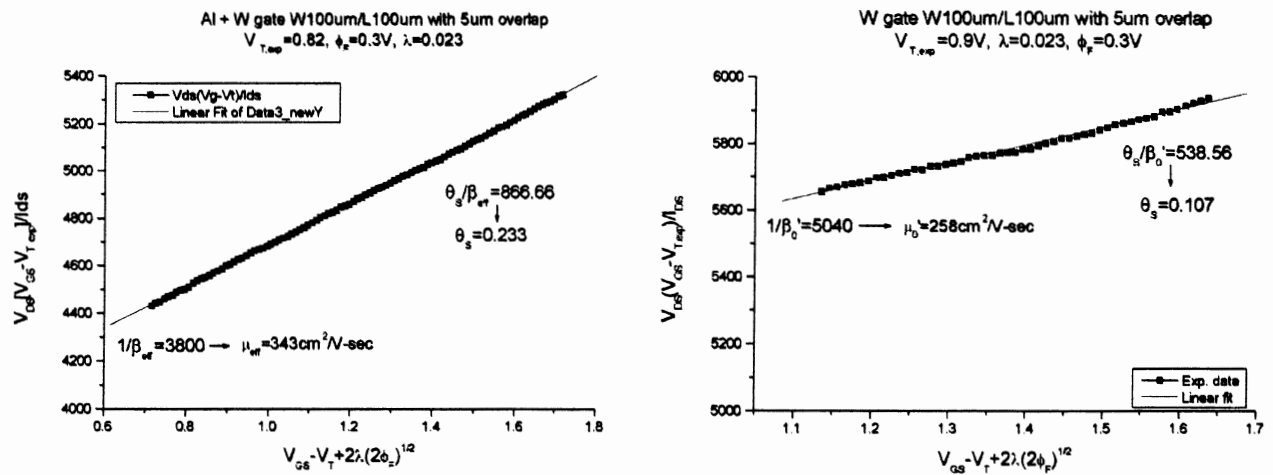


Figure 3: Mobility extraction for Al+W and W Gate MOSFETs on bulk Si substrate.

ESD Protection for High Voltage LDMOS with Sense FET

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The Power LDMOS that is commonly used in SPS one chip has two sources with one drain in order to make the current ratio of main source to sense source. Main source is directly connected to ground and sense source is connected to ground via sense resistor. In the application this current of sense source induces the voltage drop (V_s), which operate OCP (Over Current Protection) circuit for blocking all current of MOSFET. When a positive ESD pulse is applied to the drain, LDMOS can be immune to ESD if induced high current of ESD pulse is discharged through main source. A schematic of the ESD current flow is shown in Fig.1. When ESD pulse was applied, the ESD current must be transmitted through Route1 to substrate. However the change of route for current flow affected on sense source with serious. Because Route2 was more susceptible to such an ESD pulse than Route1 and also the ratio of main source area to sense source area is 100 to 1. Fig.2 shows SEM pictures of the sources. We can see the holes in silicon surface due to filament induced by metal spike. Because poly resistor has larger delay time than that of ESD pulse, poly resistor interferes with the current flow. It looks like having a parasitic npn transistor because the current is discharged by way of main source like the collector of npn transistor.

Analysis, using both electrical device simulation and measurement, reveals some solutions for main causes of failure as follows. First is a general method using I/O protection cell. When ESD pulse is applied for sense source of SPS one chip IC without connecting poly resistor, there not only isn't spiked to sense source but also little variation of sensing voltage (V_s). And the induced current of ESD stress is discharged to substrate. However, as it can be seen from Fig.1, Fig.3(a) and Fig.3(b), when ESD pulse is applied for poly resistor added to the path of ground, the metal of sense source is spiked because poly resistor interferes with the current flow by introducing an RC time constant. Also, the current tends to concentrate in the surface of the region of drift for LDMOS like the current crowding as shown in Fig.3(b). Fig.3(a) depicts lattice temperature at the metal of resistor. This simulation results were coincident with the cause of failure in Fig.2 as mentioned previous. In order to solve the ESD problem, we propose the circuit as shown in Fig.4(a) which includes the protection diode with collector-base shorted emitter of npn transistor. In Fig.4(b) and Fig.4(c), simulation results show that it is possible to add NPN CB diode in the form of parallel circuit for relieving ESD impact without generating melting point of metal. Secondly, the method for inducing a delay in the ESD pulse. The ESD current approaches the main source itself ahead of the sense source to discharge the current at the substrate. Fig.4(d) shows the top view of an SPS one chip IC including our proposed Sense FET. We exchange the layout for keeping a distance between the drain pad and the sense source. Additionally, insert a deep P+ layer between the main source and the sense source in order to prevent a parasitic NPN Transistor. The key point of layout is that the distance between the drain pad and the sense source must be long enough to induce a delay time in the ESD current.

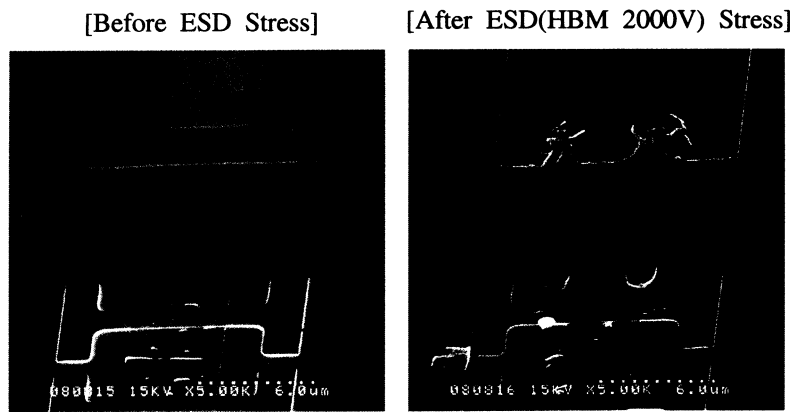
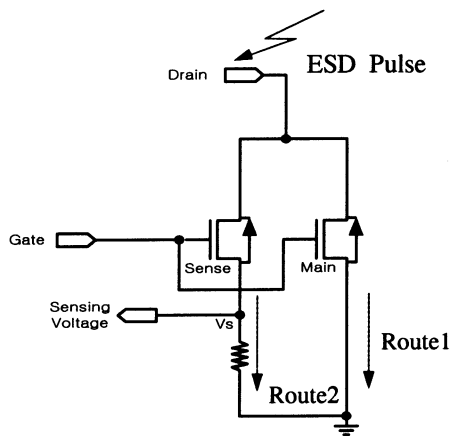
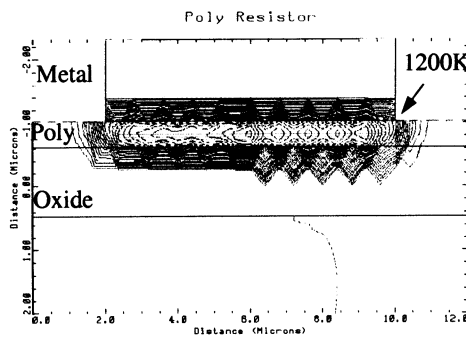
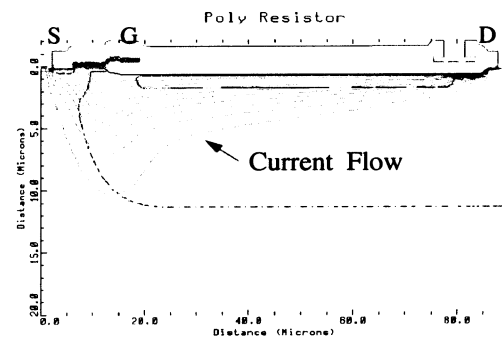


Fig.1 Schematic of the current flow of ESD Fig.2 SEM photograph of Sources showing filament between the Sense and Main Source due to severe ESD damage

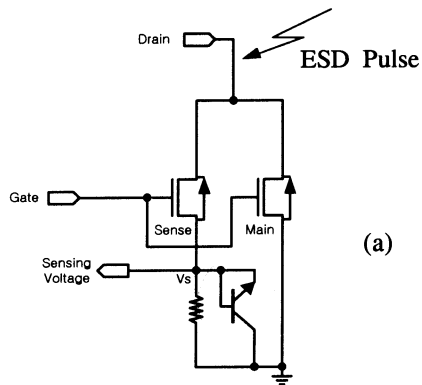


(a)

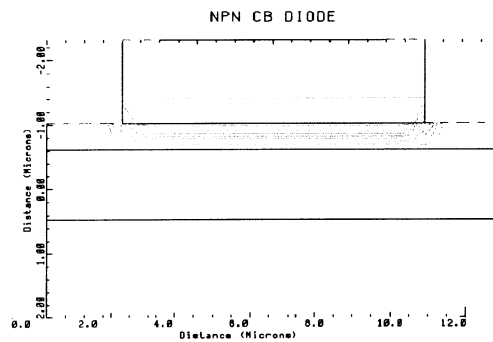


(b)

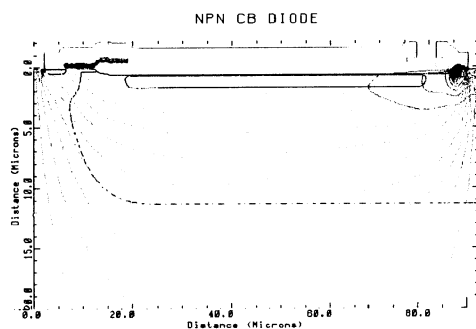
Fig.3 (a) Cross section of Poly resistor showing current flow and Lattice Temperature at the metal after ESD Stress (b) Cross section of LDMOS showing current flow for a positive ESD Stress



(a)



(b)



(c)

(d)

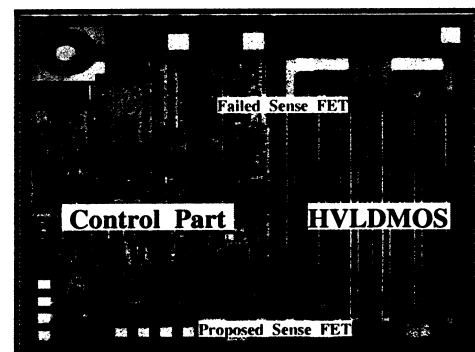


Fig.4 (a) Schematic of a protection scheme, using NPN CB Diode. (b) Cross section of Poly resistor showing current flow. There is no Lattice Temperature at the metal. (c) Cross section of LDMOS showing current flow after ESD stress (d) Variation of Design for increasing delay time with SPS one chip IC

Mixed Mode Double-Gate FET Model.

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As silicon approaches its scaling limit the double gated FET (DGFET) is looking increasingly attractive as a way to achieve a smaller gate length for the same oxide thickness [1]. Uses are proposed where the gates are either tied together [2] or varied independently for threshold voltage control [3].

The DGFET (Fig. 1) exhibits many modes of operation as the voltages on the two gates are varied with the channel being sometimes at the front, back or at both interfaces, and the channel configuration may change with position along the channel. We present here, for the first time, a compact model powerful enough to model such complex behavior. The heart of the model is the *mixed-mode* algorithm which, under appropriate bias conditions, transforms the DGFET into two single gate FETs (SGFET) in series. The single gate FET model itself uses a new treatment of the space charge region, extending Suzuki's [5] model, allowing the DGFET to be realistically simulated well into the punch-through regime. Sub-threshold and short-channel effects are included, and an effective perpendicular electric field, modified by the short-channel charge, is derived for the DGFET and used in mobility calculations. Additional mobility terms can be added to account for scattering at either interface. In addition to currents, voltage dependent capacitances are also derived, including sub-threshold gate to gate capacitances, enabling realistic simulations of coupled circuit noise to be undertaken.

The physics behind the *mixed-mode* algorithm is illustrated in Fig. 2b, where, under certain conditions (compound mode), two conducting channels are present near the source and only one near the drain in what. The transition from dual to single channel mode occurs at a point along the channel where the weaker channel is pinched off by the body potential. In the algorithm the FET is replaced by two series FETs with the potential between them corresponding to the pinch-off condition. The operating regions, mapped on simulated FET drain characteristics, are illustrated in Fig. 4. Simulated gate characteristics (see Fig. 4) show the sub-threshold

region including the change in slope on transition from front to back channel conduction.

The model was implemented as a FORTRAN™ subroutine accessed by an ASX™ circuit simulator. Average running time on a RS6000™ 355MHZ processor was 30ms per point. Voltage, current and capacitance wave forms on the 4-6th stages of a 0.1μm gate length CMOS inverter chain are shown in Fig. 5, showing that the model can deal smoothly with the wide variety of conditions encountered in a typical transient simulation.

The compound mode allows the case of a mobility modulated FET [5] to be handled. In this case the front interface has a much lower mobility than the back, so that the overall mobility decreases as the front channel becomes populated. For an abrupt mobility transition (solid curves in Fig. 6) the mobility does not change abruptly over the entire device because the channel concentration is a function of position along the channel, and this is captured by the mixed mode model.

In summary, a general purpose DGFET model is presented capable of handling a wide variety of DGFET configurations and arbitrary potentials on its four terminals.

This work was supported by DARPA grant N66001-97-8908.

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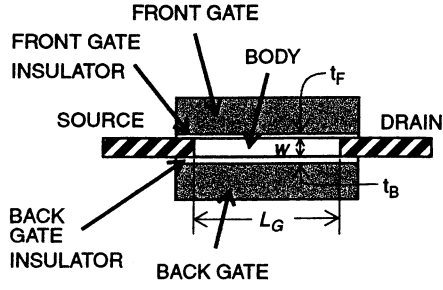


Fig. 1. Schematic cross-section of the DGFET including definition of principal dimensions.

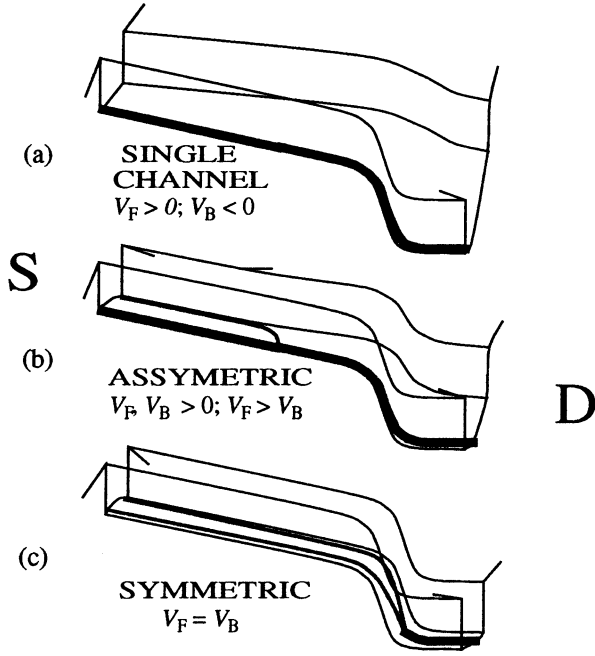


Fig. 2. Visualizations of potential along the channel of a double gate FEL showing the current paths in a) single channel, b) compound and c) dual channel modes.

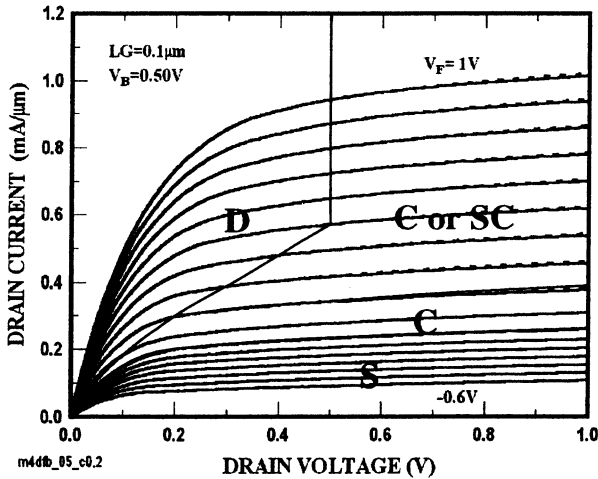


Fig. 3. Drain characteristics of DGFET showing operation in single (S), compound (C), dual (D) and simplified compound (SC) modes.

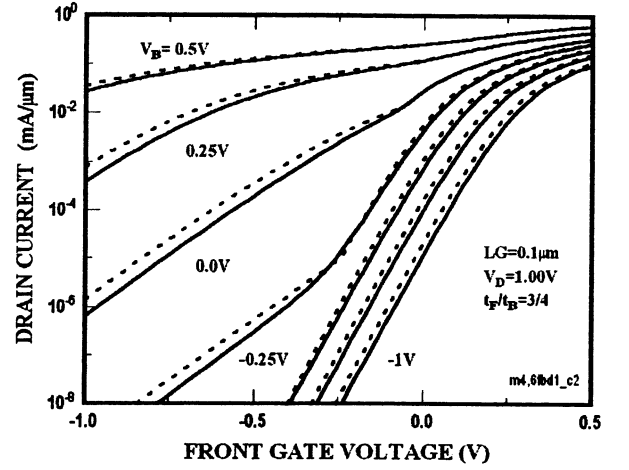


Fig. 4. Drain current vs. gate voltage, including the sub-threshold region, for asymmetrical FET ($t_F/t_B=3\text{nm}/4\text{nm}$).

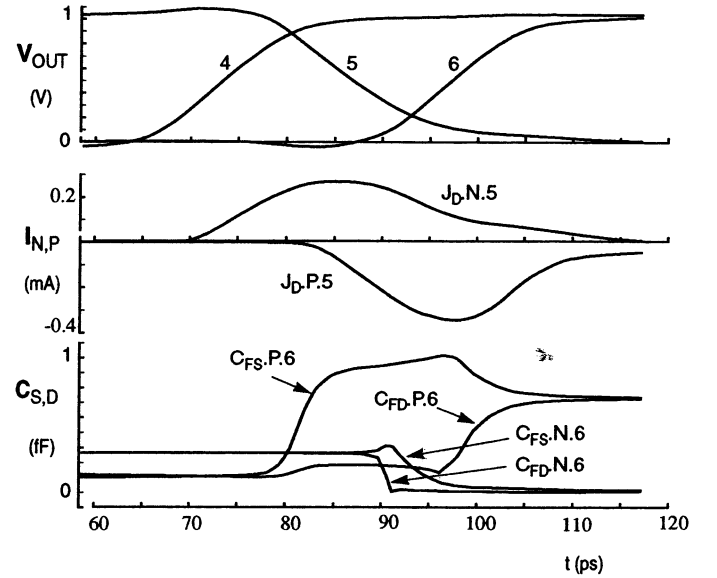


Fig. 5. Simulation of 0.1μm DGFET inverter delay chain.

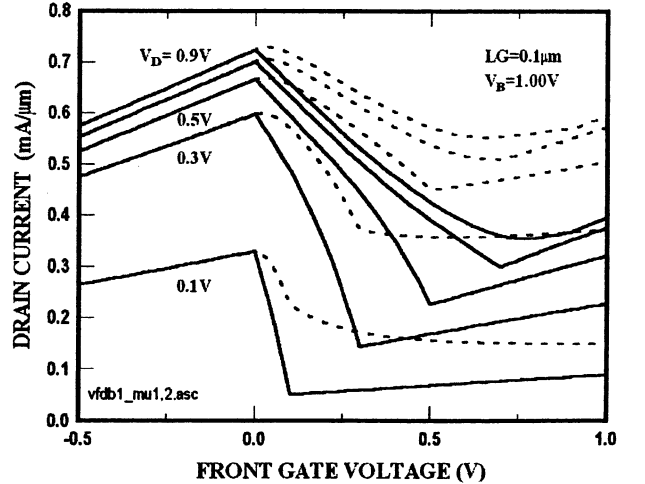


Fig. 6. Asymmetric mobility DGFET with $\mu_F=50$ and $\mu_B=3000\text{ cm}^2/\text{V}\cdot\text{s}$. Solid lines are for abrupt, and dashed lines for a charge weighted case.

LOW PROGRAMMING VOLTAGES AND LONG RETENTION TIME IN METAL NANOCRYSTAL EEPROM DEVICES

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Abstract

Conventional Si/Ge nanocrystal EEPROM devices have several advantages over conventional EEPROM with continuous floating gate [1]. However, to maintain good retention characteristics the programming voltages (write and erase) cannot be scaled down easily. Interface and dopant fluctuations at the Si/Ge nanocrystal interface also cause device design difficulty [2]. In this work, we demonstrate for the first time that metal nanocrystal EEPROM can have much lower programming voltages by careful choice of the metal floating-gate work function. Interface fluctuations is at a minimum due to the metal density of states. The retention characteristic for metal nanocrystals is similar to that of Si nanocrystals in view of Coulomb blockade. Process integration of the metal floating gate on thin tunneling oxide is greatly improved by the self-assembly step of nanocrystal formation. Energy minimization during self assembly will relax the interface stress and stabilize the metal structure to avoid penetration and contamination [3]. Together with Schottky contact injection improvement [4], introduction of metal nanocrystals can push deep submicron CMOS and EEPROM scaling for more technology generations.

I. Introduction

Nanocrystal EEPROM devices were proposed for low-power and low-voltage operations by utilizing direct tunneling, floating gate sparsity and Coulomb blockade [1, 2]. The floating gate was composed of Si or Ge nanocrystals due to process compatibility. Even with the enhancement, voltage scaling was still rather limited by design trade-off between programming voltages and retention characteristics. Metal nanocrystals with size of 2-40nm can also be reliably formed on tunneling oxide through self-assembly or Ostwald ripening [3]. After formation, the metal nanocrystals are much more thermodynamically stable and can be easily integrated with less possibility to damage or contaminate the device with thin oxide. In principle, most metals can be used as the nanocrystal floating gates, which gives a new degree of design freedom from the choices of work function and thermal budget. Careful choice of floating gate work function can result in useful asymmetry between the programming and retention stages, and hence can dramatically enable aggressive voltage scaling while maintaining good retention characteristics. Our preliminary experiments have clearly shown this scaling improvement by comparing metal and Si nanocrystal devices with very similar process flow. We are able to decrease the EEPROM programming voltage from around 20V to 4V. Due to facility limitation, we have still observed some anomalous I-V characteristics in metal nanocrystal EEPROM devices, which can be

explained physically and will not become a serious limitation in production-grade facilities.

II. Metal nanocrystal process integration

To form the self-assembled metal nanocrystals as floating gates, a wetting layer of metal of 2-10nm is evaporated or deposited on top of 4-8nm thermal oxide. Then a RTA process with short temperature peaks close to but lower than the bulk eutectic temperature is performed. Undulation of dot patterns is the result of energy minimization among the surface and elastic energies and various long-range forces [5]. Dots in a more regular pattern and with minimal separation can be obtained if the electrical-double-layer force [6] as shown in Fig. 1, is a significant contributor. We have carefully characterized the various metal and Si (as control devices) nanocrystals by SEM (Fig. 2), AFM (Fig. 3) and electrical measurements in the following.

III. Nanocrystal EEPROM IV characteristics

The test EEPROM cells have a gate oxide of around 6nm (from IV and CV), CVD control oxide around 20nm and height of nanocrystals ranges from 8 to 20nm. To determine that individual isolated dots have been formed instead of a continuous polycrystalline thin film at the floating gate, both Si and metal nanocrystal devices were subject to hot-carrier injection condition and showed similar asymmetrical IV characteristics on source/drain reversal (Fig. 4). Interface effective mobility (Fig. 5) is monitored to evaluate Si channel quality. Charging and erasure characteristics of the control Si nanocrystal devices from control gate current injection are shown in Fig. 6. At higher control gate biases, current ripples correspond to single-charge events to the nanocrystals [1,2]. Fig. 7 shows Au-nanocrystal IV under gate current injection. Both Si and Au cases have floating-gate charging retention time much longer than 500 hours. Tunneling into Au nanocrystals is much more efficient in evidence of the low writing voltage and the potential pocket shown in Fig. 8. The initial attempt at an electrical erase of Au samples shows a clear change in subthreshold slope, instead of V_{th} shift. This phenomenon can be explained by the inhomogeneous charge states of the metal nanocrystals [2] resulted from the low negative control bias, where the channel can be better approximated with the equivalent circuits in Fig. 9 with relative strengths strongly dependent on the nanocrystal sparsity. After 20 days of storage, there is little redistribution and leakage of the nanocrystal charge. The channel leakage is larger probably owing to lack of passivation. Notice that the gate current is still very low here and stress-induced leakage current is very small. The Au-dot charge can be fully erased through UV exposure.

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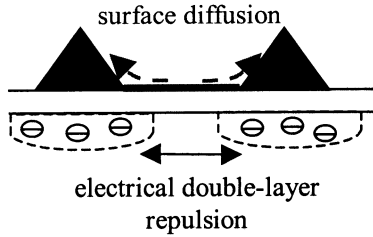


Fig. 1. Formation of nanocrystals from surface diffusion of deposited wetting layers. If the substrate is doped and extrinsic, the electrical double-layer repulsion will enlarge dot spacing.

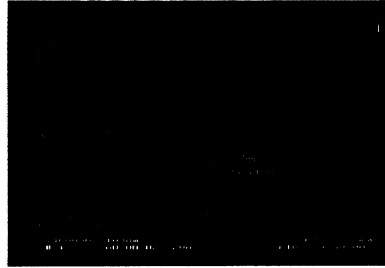


Fig. 2. Au nanocrystals on SiO₂ formation after 2-min RTA of 550°C. The initial wetting layer thickness is 2nm. Both dot size and spacing are around 13nm with 5nm deviation.

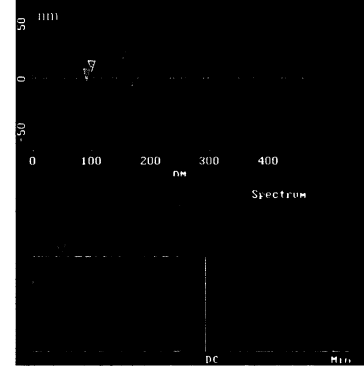


Fig. 3. AFM analysis of metal nanocrystals. Features are subject to 2-3nm error in the contact mode.

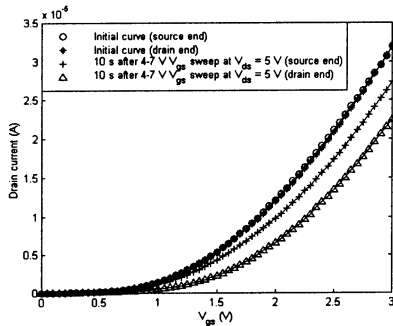


Fig. 4. Asymmetrical drain current characteristics from source/drain reversal measurements (similar for Si and Au cases).

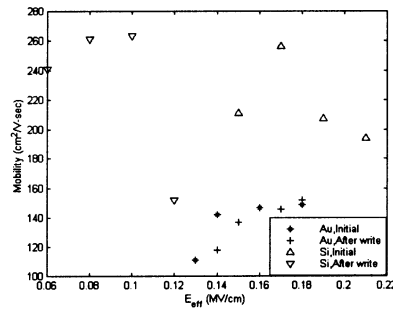


Fig. 5. MOSFET interface mobility monitoring channel quality. The distribution is within measurement errors.

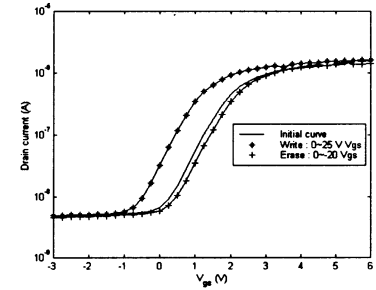


Fig. 6. Charging and erasing of Si nanocrystal EEPROM cells from control gate current injection around 20V.

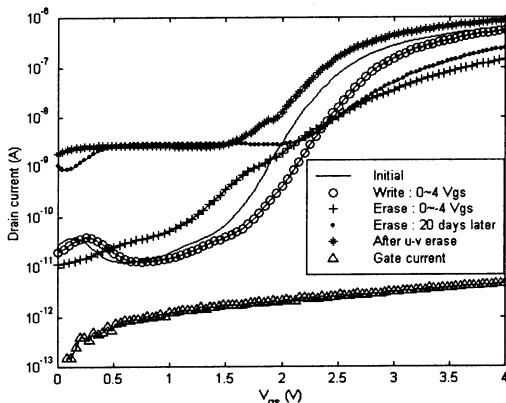


Fig. 7. Charging and erasing of Au nanocrystal EEPROM cells from control gate current injection. For acceptable retention time, the programming voltage can be dramatically lowered to around 4V.

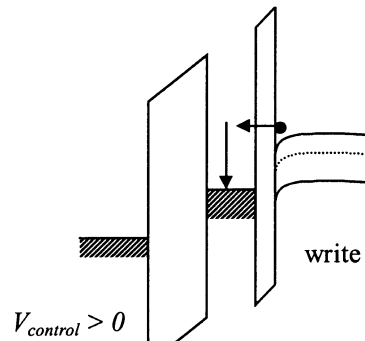
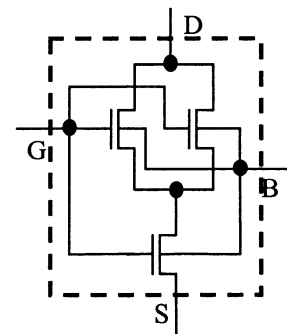


Fig. 8. Band diagrams of mid-gap metal nanocrystal charging with respect to control bias. Notice that the electrons are easier to tunnel in but much more difficult to tunnel out. Holes may participate during negative control bias.



Fitting parameters:
 $V_{th1}, V_{th2}, V_{th3}, t_{ox1}, t_{ox2},$
 $W_1, W_2, W_3, L_1, L_2, L_3$

Fig. 9. Equivalent circuit models to account for dot sparsity and charge inhomogeneity.

High Performance AlGaIn/GaN HEMTs with Recessed Gate on Sapphire Substrate

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High performance AlGaIn/GaN high electron mobility transistor (HEMT) with recessed gate was successfully fabricated on sapphire substrate, as shown in Fig. 1. In order to realize high performance HEMT, it is very important not only to improve 2-dimensional electron gas (2DEG) but also to reduce the parasitic resistance. However, the increase of aluminum content in AlGaIn to get high density 2DEG results in poor ohmic contact, as well known. Fig. 2 shows the comparison of contact resistances to GaN and AlGaIn. Contact resistance was $8 \times 10^{-6} \Omega \text{cm}^2$ in case of n-GaN ($1 \times 10^{19} \text{cm}^{-3}$), and as high as $7 \times 10^{-5} \Omega \text{cm}^2$ in case of n-AlGaIn ($1 \times 10^{18} \text{cm}^{-3}$). In our recessed gate structure, ohmic contact with low resistivity can be formed on n-GaN with high electron density which is grown on AlGaIn layer with high aluminum content [1].

The substrate used here consists of a 30-nm-thick GaN nucleation layer, a 2.5- μm -thick undoped GaN layer, a 10-nm-thick $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ spacer layer, a 20-nm-thick n- $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ ($1 \times 10^{18} \text{cm}^{-3}$) layer and a top 20nm-thick n⁺-GaN ($1 \times 10^{19} \text{cm}^{-3}$) layer on sapphire substrate grown by MOCVD. Electron density and electron mobility of 2DEG were $1 \times 10^{13} \text{cm}^{-2}$ and $736 \text{cm}^2/\text{Vs}$, respectively.

Drain and source ohmic contacts were formed with Ti (15nm)/ Al (250nm) and annealed at 550°C for 1 min. Gate recess etching was done by reactive ion etching (RIE) in a Cl_2/H_2 plasma and gate metal (Ni/Au) was deposited on recessed area.

The HEMT with 0.5 μm gate length showed excellent current saturation property without no kink effect and no current degradation, as shown in Fig.3. The maximum trans-conductance was as high as 327 mS/mm. Fig. 4 shows the short circuit current gain (h_{21}) and maximum stable gain / maximum available gain (MSG/MAG) curve measured in the 1-50GHz range at $V_{\text{ds}} = 4\text{V}$. An extrinsic current gain cutoff frequency (f_T) of as high as 32.3GHz and a maximum frequency of oscillation (f_{max}) of 39GHz were obtained. Resistances, so called source resistance (R_s), between source and gate were also measured.

These characteristics were compared with that of non-recessed 0.75 μm gate HEMT which has same hetero structure with no n⁺-GaN top layer, as shown in Table 1. R_s of recessed gate HEMT was smaller than one third of that of non-recessed gate HEMT. This will be the reason why the trans-conductance (g_m) of recessed gate HEMT is three times larger than that of non-recessed gate HEMT. The $g_m \times$ gate-length product and $f_T \times$ gate-length product were also compared. In the recessed gate HEMT, these products were greatly improved and also nearly equal to that of the highest achieved for GaN-HEMT[2][3] without the use of extremely short gate length[2] or high performance 2DEG[3].

To evaluate effective electron velocity in the channel, we deleted the influence of pad parasitic capacitance to the measured f_T by F-matrix calculation. Amended f_T , which is considered to be nearly intrinsic, was 43.0 GHz and the effective electron velocity calculated from this was $1.4 \times 10^7 \text{cm/s}$. This is the highest value reported to date for GaN-HEMT.

In conclusion, it can be said that AlGaIn/GaN HEMT with recessed gate is a promising device for high power and high frequency applications.

This work was performed under the management of FED as a part of the MITI New Sun Shine Program (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

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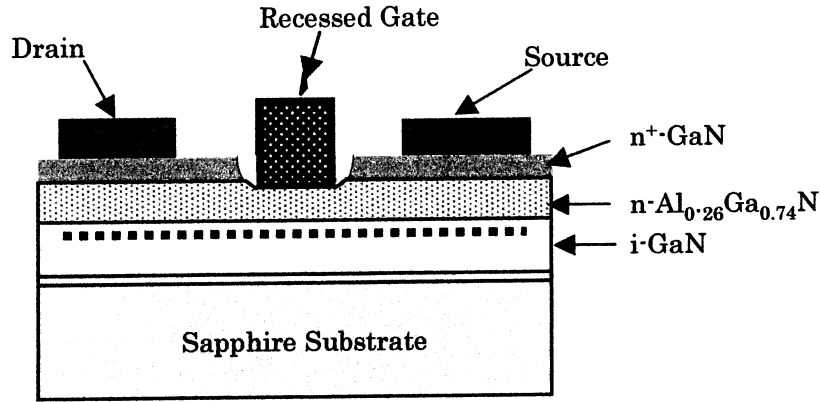


Fig. 1 AlGaN/GaN HEMTs with Recessed Gate.

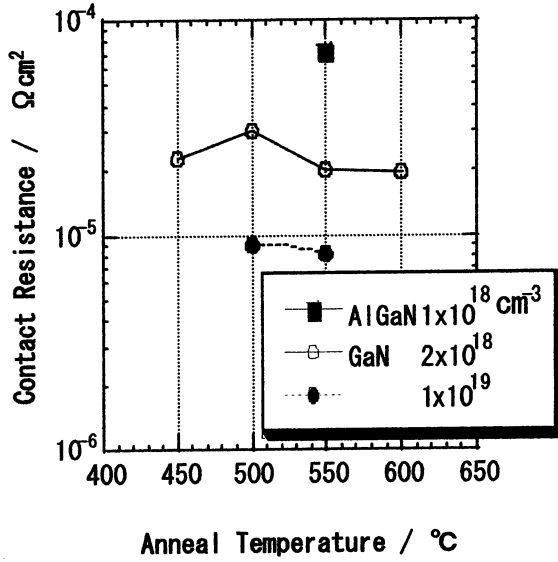


Fig. 2 Anneal temperature dependence of contact resistance.

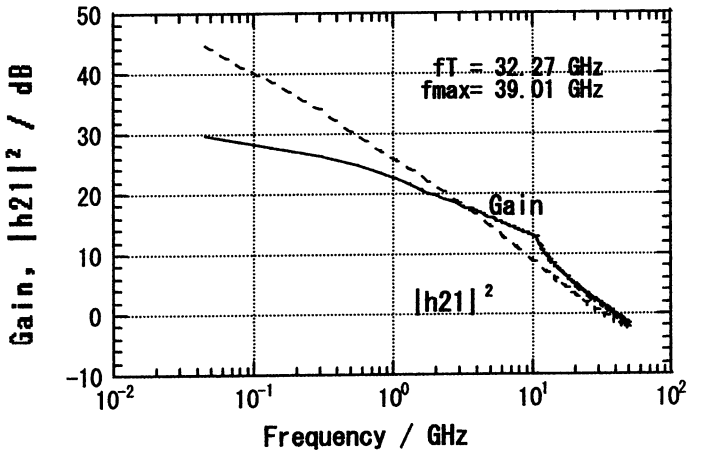


Fig. 4 Current Gain $|h_{21}|^2$ and MSG/MAG(Gain) of HEMT.

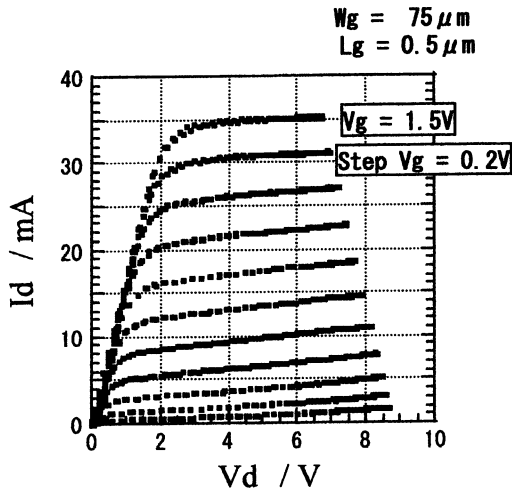


Fig. 3 DC I V characteristics of AlGaN/GaN HEMT.

Gate structure	Non-Recessed	Recessed (This work)
Gate Length (μm)	0.75	0.5
R_s (Ωmm)	7.2	2.1
g_m (mS/mm)	110	327
f_T (GHz)	6.0	32.3
f_{max} (GHz)	25.5	39.0
$g_m \times L_g$ ($\mu\text{m-mS/mm}$)	83	164
$f_T \times L_g$ ($\mu\text{m-GHz}$)	4.5	16.2

Table 1 Comparison of characteristics between Non-recessed and recessed gate HEMT.

A Comparison of Bulk and SOI Deep Sub-Micron MOSFET Small-Signal Behavior in the High-Frequency Regime Beyond 10GHz

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Abstract

This paper investigates the small-signal behavior of SOI CMOS devices. The small signal parameters include: power gain, transconductance, input resistance, output resistance, input and output capacitance. These characteristics were compared to Bulk CMOS at RF frequencies above 10GHz. Analysis of these results, show great reduction in the negative impacts of both the parasitic S/D resistance and parasitic BJT floating-body effects on RF circuits at 10GHz regime.

Introduction

By scaling MOSFET channel lengths to nearly a tenth micron, CMOS is rapidly becoming a serious option for many low-power, wireless RF applications that were previously considered to be the exclusive domain of more expensive SiGe BICMOS and GaAs technologies. Affordable, handheld wireless devices are now soon incorporating RF-CMOS discrete chips. However, there are several limitations to achieving RF, baseband, and digital signal processing integration on a single CMOS chip. Fortunately, SOI offers solutions to several of these integration problems, including reduced power dissipation, reduced substrate coupling and losses, improved inductor Q factor, improved short-channel behavior, and reduced parasitic capacitance. However, floating-body PDSOI devices must contend with non-linearity, excess $1/f$ noise, and reduced output resistance in baseband analog applications, due to the parasitic bipolar action in the body. As SOI devices are considered for use at RF system frequencies of 2.4GHz (Bluetooth) and beyond, it is imperative to understand their basic small-signal behavior as compared to bulk, and whether or not these analog baseband limitations still exist at RF frequencies [1-5]. Only a few small signal PDSOI MOSFET results have been published to date [2-5].

Process/Device description

The devices used in this work are the fastest digital SOI-CMOS reported to date, with <8psec ring oscillator delays [6]. Table 1 shows the process and device parameters used in this work. SIMOX wafers, shallow S/D extensions, retrograde body, and halo implants were used to improve short-channel behavior and reduce parasitic BJT action. Dual poly gates and S/D junctions were silicided. Bulk and PDSOI devices were processed in the same run with identical structures and dimensions.

Characterization method

The measured devices are interdigitated, n-type MOSFET with sixteen $4\mu\text{m}$ wide fingers, embedded in a coplanar waveguide structure with $L_{\text{eff}}=0.22\mu\text{m}$ (Fig. 2). Characteristics were measured in saturation with $V_G=V_D=1.5\text{V}$. Table 2 shows the test frequency range from 1GHz to 20GHz. For each measured frequency, a de-embedding and calibration procedure is applied using an on-wafer open structure and off-wafer load, short, and thru structures. Measurements were

made on-wafer with an HP8510C network analyzer, 3.5-mm waveguide, and a pair of air coplanar probes, ACP40 S-G, and a manual Cascade Microtech Summit Microwave Probe Station. Care is taken to ensure the pressure and angle of the probe tips is consistent during de-embedding, calibration, and measurement.

Results & Discussion

Small signal parameters power gain ($|h_{21}|$), transconductance (g_m), input resistance (R_{in}), output resistance (R_{out}), input capacitance (C_{in}), and output capacitance (C_{out}) were obtained versus frequency by transformation of the S-parameters (Fig. 1). Analyzing the extracted $|h_{21}|$, the approximate f_t is 33GHz for SOI, while the bulk gain rolls-off early at 23GHz (Fig. 3). g_m of the bulk device was 20% higher and rolled off steeper than SOI above 10GHz (Fig. 4). As expected, both C_{in} and C_{out} were lower for the SOI than bulk devices, due to smaller junction capacitance. However, C_{in} is dominated by C_{gs} and is somewhat independent of frequency. The increase of C_{in} above 10GHz is yet to be explained (Fig. 5). C_{out} falls off rapidly with frequency for SOI, resulting in an increased performance advantage over bulk at higher frequencies (Fig. 6). R_{in} is higher for SOI than bulk, most likely due to higher S/D sheet resistance, but this effect also decreases above 10GHz (Fig. 7). R_{out} for SOI is only half the bulk value at low frequencies, due to parasitic bipolar action (Fig. 8). However, as the operating frequency increases into the non-quasi-static regime, this floating body effect is mitigated. In fact, the SOI R_{out} converges with the bulk value at 15GHz, thereby completely eliminating this floating body gain degradation.

Conclusion

The convergence of bulk and PD-SOI R_{in} and R_{out} characteristics at frequencies in the 10GHz regime greatly reduces the negative impact of both the parasitic S/D resistance and the parasitic BJT floating-body effect on the small-signal behavior of RF circuits. In particular the R_{out} , gain, bandwidth, and linearity are found to be comparable for bulk and PDSOI devices at frequencies beyond 10GHz, while the C_{in} , C_{out} , and other well-known advantages of SOI for SOC integration are retained at these frequencies as well. These results demonstrate the practicality of using PDSOI devices for RF-CMOS applications in the future.

Acknowledgment

The authors would like to thank Dr. Fari Assaderaghi of IBM for providing the samples. This project is supported by National Science Foundation Grant EPS-9977454.

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SIMOX PDSOI Parameters	
Tox	3.5 nm
Leff	0.22 μm
Nfinger	16
Wfinger	4 μm
Vt	0.4 V
Rsd	220 $\Omega\text{-}\mu\text{m}$
Ion	550 $\mu\text{A}/\mu\text{m}$
Ioff	1 nA/ μm

Table 1: Process and Device Parameters

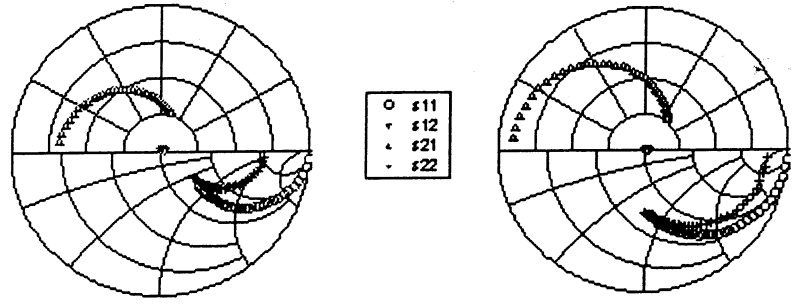


Fig. 1: S-Parameters (Smith/Polar). SOI (left), BULK (right)

Test Parameters	
Wafer	SOI and BULK
Device	NMOS-AB structure
Test	$V_g = V_d = 1.5 \text{ V}$
Conditions	$V_s = 0 \text{ V}$
Sweep	1 GHz to 20 GHz

Table 2: Test Parameters for both SOI and BULK

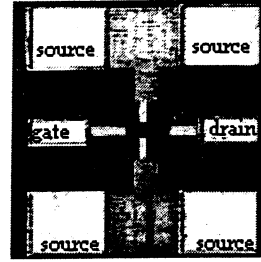


Fig. 2: Coplanar waveguide structure, contact pads defined

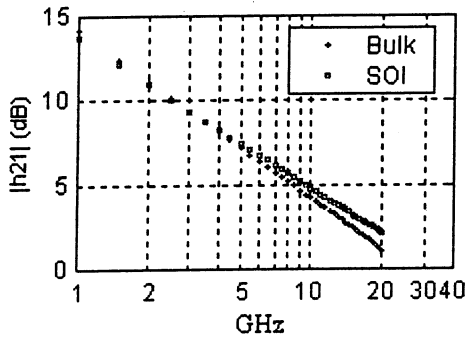


Fig. 3: Power gain versus frequency

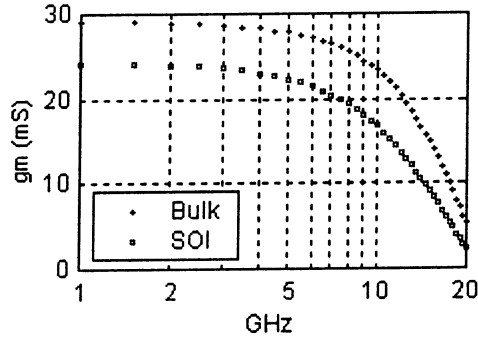


Fig. 4: g_m versus frequency

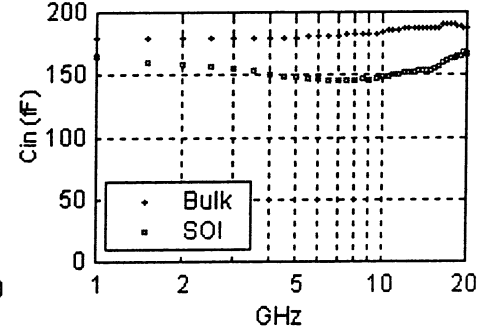


Fig. 5: C_{in} versus frequency

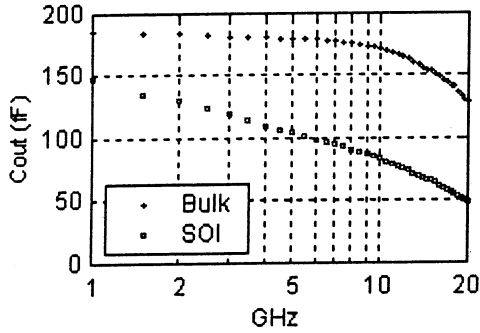


Fig. 6: C_{out} versus frequency

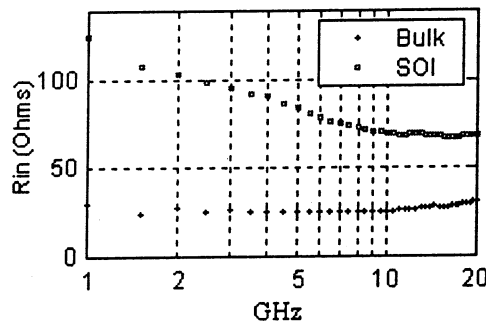


Fig. 7: R_{in} versus frequency

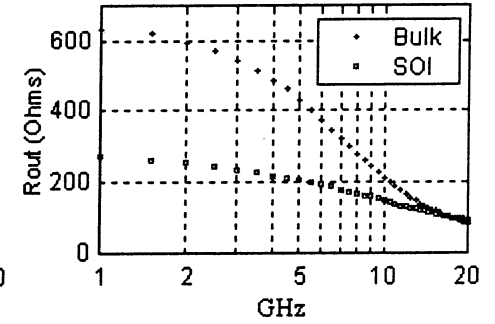


Fig. 8: R_{out} versus frequency

Threshold Voltage Shift by Quantum Confinement in Ultra-thin Body Device

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Introduction

Ultra-thin body (UTB) single or double gate MOSFET with raised S/D was proposed to suppress the short-channel effects in future CMOS device [1][2][3]. Any potential well can cause sub-band splitting (between 2-fold and 4-fold valleys of the conduction band, light and heavy hole bands of the valence band) when the quantum confinement happens [4][5]. The sub-band splitting results in a smaller density of states so that more energy-band bending is required to attain a desired inversion-charge density as compared to a thicker body device. The increase in threshold voltage has been observed in thin-body structure device [7][8]. Previous works calculated the threshold voltage shift numerically [7][8] and treated the quantum effect with the effect of a high-doping concentration [4][5]. A simple analytical model is desirable for understanding the experimental data and providing quick guide to the threshold voltage adjustment for UTBFET.

Modeling

The inversion charge has been numerically analyzed with Poisson equation and Schrodinger equation solved self-consistently or analytically solved for a high body-doping bulk device with a triangular potential approximation (see Fig. 2a) [3][4][5][6]. However, the potential shape in UTB device is closer to rectangular because of a light body-doping (Fig. 2b). Light doping improves mobility and reduces the doping fluctuation effect. Even heavy-doping would not be effective for the threshold voltage adjustment due to the thin thickness. A closed analytical model with the rectangular and triangular potential approximation is developed and compared with the measured data instead of numerical calculation in this work. While the threshold voltage is usually defined as $\phi_s = 2\phi_B$ in the classical mode, it is appropriate to define the threshold voltage as the gate voltage when the same amount of charge is acquired in the quantum mechanical mode [6]. A closed from expression for the threshold voltage shift vs. UTB thickness (T_{si}) can be shown to be

$$\Delta V_t^{QM} = (1 + 3T_{ox} / T_{si}) \cdot kT / q \cdot \ln(h^2 N_{c,v} / [4\pi q \epsilon_s \sum_{i,n} g_i m_{di} e^{-E_{in}/kT}]) \text{ where } E_{in} = h^2 n^2 / 8m_{zi} T_{si}^2$$

E_{in} are energy-eigen values while $E_{in} = (3hq\epsilon_s / 4\sqrt{2m_{zi}} \cdot (n + 3/4))^{2/3}$ for the triangular well.

The threshold voltage is measured at 100nA/um of drain current [2] and the UTB thickness is measured with NanoSpec/DUV at each point and calibrated with TEM pictures. Fig. 1 shows the TEM picture of a 3nm ultra-thin body SOI device. The threshold voltage difference is taken to be $\Delta V_t = V_t^{QM}(\text{thin body}) - V_t^{QM}(\text{thick body})$ in UTB device. The rectangular well model is closer to the measured data than the triangular well model as shown in Fig. 3a and 3b. Fig. 4 shows opposite trends of the threshold voltage shift for UTB and bulk device. More shift in bulk device is at a higher body-doping concentration because the confinement is stronger. The threshold voltage shift is caused by the confinement effect of the thin body in the UTB device. A higher body-doping makes the threshold voltage of the thick-body UTB device larger due to sub-band splitting. Therefore the threshold voltage *shift*, effect of reduction of the UTB body thickness, is reduced (even though the threshold voltage is larger). The threshold voltage shift is predicted to be larger in double gate device than single gate device for the same argument.

Conclusion

The threshold voltage shift caused by quantum confinement in UTB is observed experimentally. An analytical model is proposed and shows a good agreement with the experimental data of both PMOSFET and NMOSFET. It predicts a larger threshold voltage shift for a lighter body-doping, which is opposite to the trend in the bulk device. This threshold voltage shift must be taken into account in the design of UTB device, including the double gate MOSFET.

Acknowledgement

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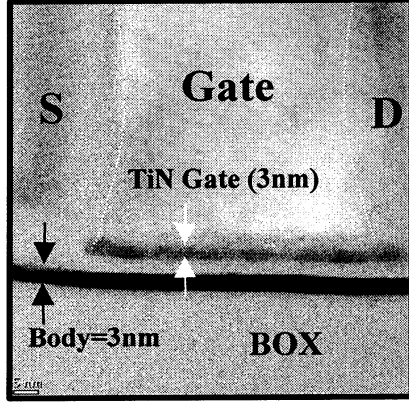
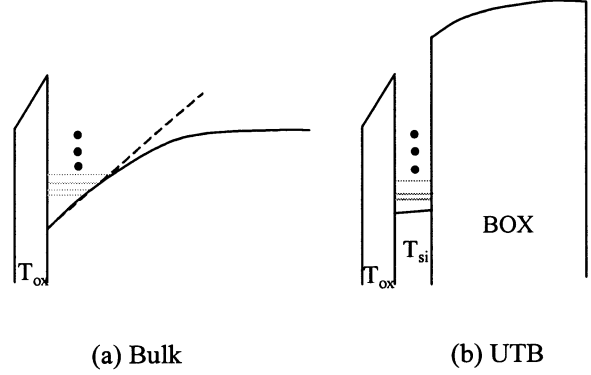


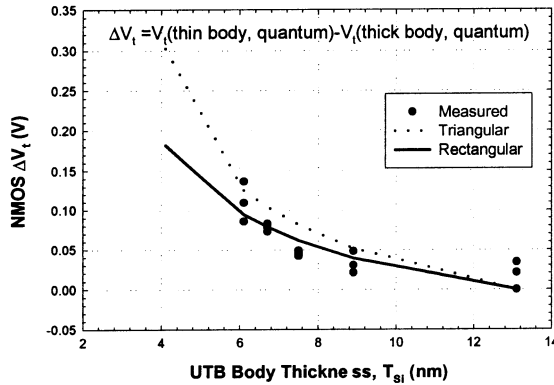
Figure 1. TEM picture of ultra-thin body (3nm) SOI device.

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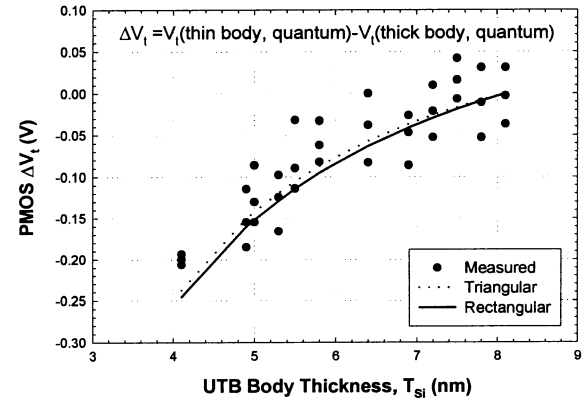


(a) Bulk

(b) UTB

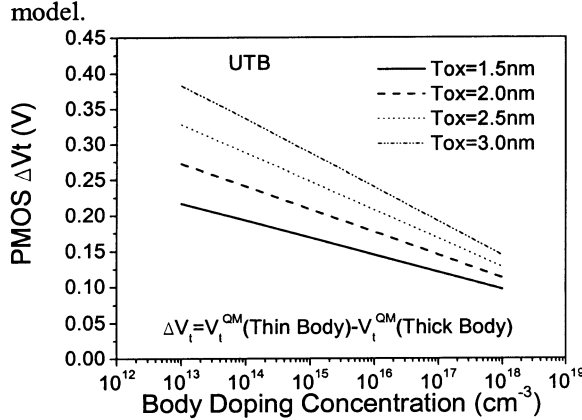


(a) NMOS

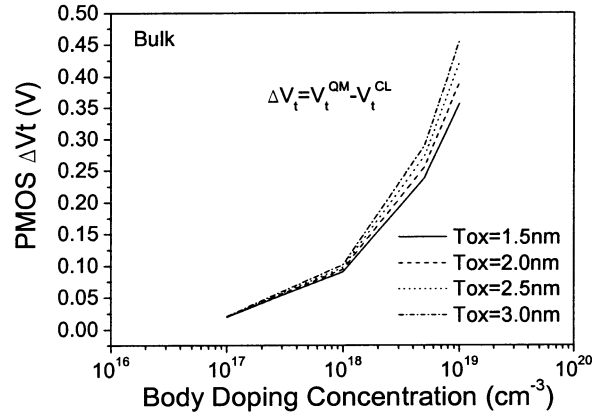


(b) PMOS

Figure 3. Comparison of analytical model and measurement data of UTBFET for (a) NMOS and (b) PMOS. The rectangular potential well model matched the measured data better than the triangular potential well model.



(a) UTB



(b) Bulk

Figure 4. Threshold voltage shift vs. body-doping concentration in (a) UTB device and (b) bulk device. Larger threshold voltage shift is predicted for lighter body-doping UTB and heavier body-doping bulk device.

A New and Accurate Quantum Mechanical Compact Model for NMOS Gate Capacitance

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Introduction: Traditional gate capacitance models involve the solution of the surface potential for a given gate bias, obtained assuming a charge sheet model [1]. The quantum mechanical (QM) effects are usually accounted for by using a simple Van Dort like model and the poly-depletion effects are calculated using a simple depletion model [2]. In this work, a novel and accurate approach has been developed to calculate the surface potential for a given oxide field and to generate a complete sweep of the CV curve, accounting for poly-depletion and QM effects via a first principles approach.

Approach: For a given oxide field, F_{ox} , the induced surface charge is known. In accumulation, the induced carriers fill up the various subbands, each with an approximately constant density of states, raising the Fermi level. In strong inversion, the situation is similar except that the depletion layer charge must be subtracted out. Comprehensive self-consistent solutions of Schrödinger's and Poisson equations using UTQUANT [3], which account for wave function penetration into the gate dielectric, show that the lowest energy subband—the ground state subband of the heavy-hole band for holes and the ground-state subband of the interface-normal conduction band valleys for electrons—contribute the principal fraction of charge, and a fraction which is only weakly dependent on the field: approximately 80% for holes in accumulation and 70% for electrons in strong inversion at 300K, for example. These simulations also show that the energies of these subband follow simple power-law relations with the oxide field F_{ox} analogous to that used in [4] but more precisely obtained here: $F_{ox}^{0.64}$ for holes and $F_{ox}^{0.6}$ for electrons independent of doping, as shown in Figs 1 and 2, respectively. This information is used to obtain a simple yet accurate explicit analytic expression for the Fermi level, *and thus the band-bending*, using the lowest subband as a function of the oxide field in inversion and accumulation, as per the examples of Figs. 3 and 4. A simple quadratic model for the band-bending prior to the onset of strong inversion was used to model the depletion layer. By adding in the potential drop across the oxide and the flat-band voltage, the gate voltage vs. oxide field/stored charge relation is readily obtained. From this latter relationship, the CV curve can be readily swept out, as per the example of Fig 5 for a metal gate device with a substrate doping $1e17\text{ cm}^{-3}$.

The simple depletion model works well except for when low fields, where the depletion width is smaller than the Debye length of the semiconductor, and high doping must be considered simultaneously. Under these conditions, the self-consistent simulations show the depletion layer voltage drop to vary only linearly with field rather than quadratically, consistent with a simple triangular potential barrier model developed for this purpose, as shown in Fig. 6. This latter model is critical for accurate modeling of low field poly-depletion effects, as shown in Fig. 7.

Conclusions: The simple explicit analytic model developed can be used to generate an accurate sweep of the CV curve from the oxide field. The quantum mechanical effects are intrinsically included in the estimation of the subband energies. Neither the substrate potential nor the polysilicon potential are pinned at any arbitrary value. So far only NMOS device have been explicitly treated; the model will be extended to PMOS devices in the future. Work is also ongoing to allow band-bending and capacitance to be calculated directly as a function of voltage.

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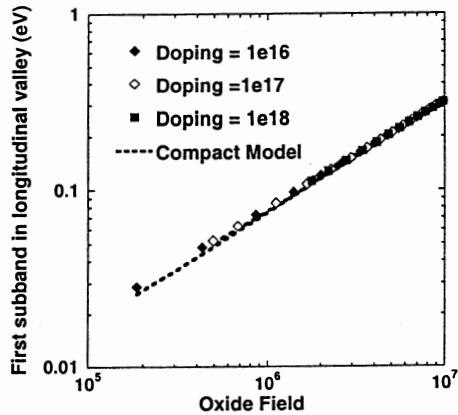


Figure 1: Electron subband energy calculated (broken line) compared with self-consistent results (symbols) at 300K.

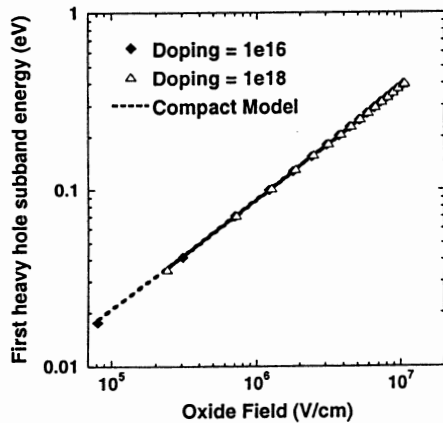


Figure 2: Hole subband energy calculated (broken line) compared with self-consistent results (symbols) at 300K.

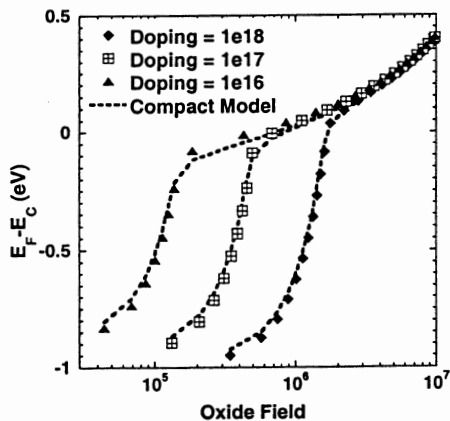


Figure 3: Fermi-level prediction (broken lines) compared with self-consistent result (symbols) in the inversion region at 300K.

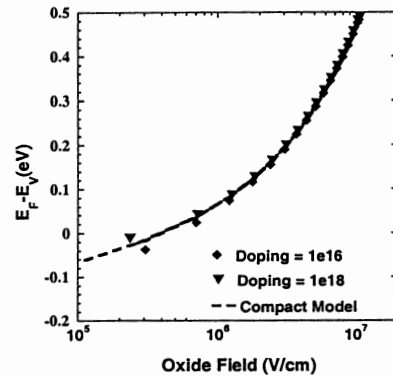


Figure 4: Fermi-level prediction (broken lines) compared with self-consistent result (symbol) in the accumulation region at 300K.

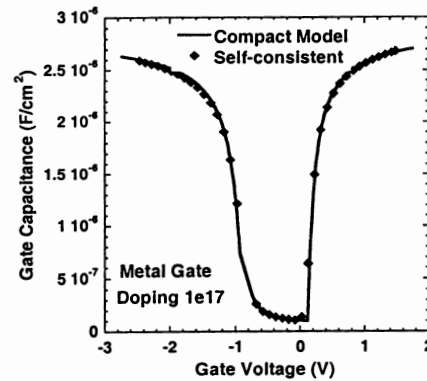


Figure 5: CV from the compact model compared against self-consistent result at 300K.

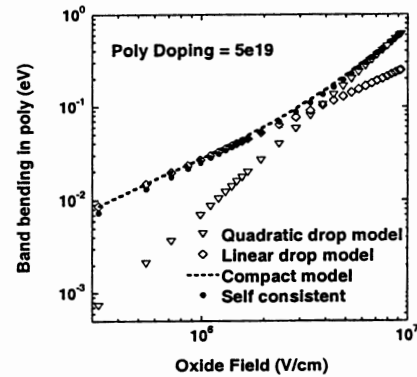


Figure 6: A detailed study of the polysilicon potential drop.

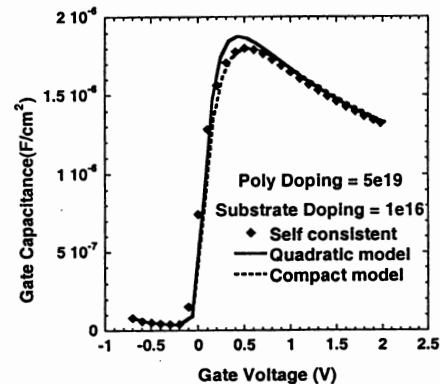


Figure 7: Comparison of CV with and without the low field depletion model correction at 300K.

An intrinsically coupled HBT/RTD device enabling an adjustable Peak-Current-Density

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Abstract

For the two terminal Resonant-Tunneling-Diode (RTD) the device functionality is dominated by the epitaxially grown layer sequence consisting of very thin layers. I. e. a variation of the barrier layer thickness shows an exponential impact on the RTD peak-current density. This is a major drawback for the use of RTD devices for circuit applications and has to be compensated by novel circuit architectures like the MOOnostable BIstable Logic Element (MOBILE) [1]. The operation principle of a MOBILE, shown in figure 1, is based on the comparison of the absolute RTD peak-current scaled by the RTD device area [2]. By this method the exponential impact of epitaxial growth variations are reduced to less critical lateral scaling rules. But the design of programmable and/or multiple-valued logic functions is inhibited because the current is defined by the RTD area, only. In this work a novel HBT/RTD device is presented with a controllable peak-current density S_{Peak} .

The proposed intrinsically coupled HBT/RTD device enables a direct adjustment of the peak-current-density by the B/E input voltage and simplifies the MOBILE circuit topology as shown in figure 1c). The RTD layer sequence is integrated inside the collector of the HBT directly at the B/C junction (cf. fig. 2). By this way the charge accumulation n_{BC} at the RTD structure can be controlled by the bipolar effect which results in an intrinsically coupled device structure ($n_{\text{BC}} = f(V_{\text{BE}})$, see fig 2). An increase of V_{BE} results in a charge accumulation n_{BC} at the RTD layer sequence while V_{CE} acts on the B/C depletion region and by this way on the adjustment of the RTD resonance level W_1 to the conduction band of the base. The exact control of RTD features like peak-current-density S_{Peak} or Negative-Differential-Resistance (NDR) by two voltages enables a more flexible circuit design with reduced restriction caused by limits in reproducible layer growth and device fabrication.

Figure 3a) shows the common-emitter dc-output characteristics of the coupled RTD/HBT device (RTD inside the collector) while figure 3b) corresponds to a more conventional RTD/HBT combination with a RTD inserted in the HBT emitter branch. The coupled RTD/HBT device shows the adjustable peak-current-density at a low peak-voltage $V_{\text{Peak}} = 320 \text{ mV}$ and also a current-blocking-effect at $V_{\text{CE}} > V_{\text{Peak}}$ which is known for D-HBT like structures. This device behavior is in strong contrast to the 'series-circuit' like behavior of the RTD/HBT device with a RTD inserted in the emitter branch given in fig. 3b) and will be discussed in detail.

The growth of the InP/(InGa)As:C HBT and (InAl)As/(InGa)As RTD structures (cf. fig. 2) is carried out in a commercial MOVPE system using a non-gaseous-source configuration while device fabrication is based on wet chemical etching and optical lithography [3]. The differences in electrical behavior of the combined RTD/HBT devices and the corresponding RTD and HBT single devices will be addressed while state-of-the-art performance is achieved for InP/(InGa)As:C HBT ($\beta = 400$, $f_T = 150 \text{ GHz}$).

The applicability of the RTD/HBT device combinations to circuit concepts based on programmable MOBILE threshold and boolean gates and multiple-valued-logic will be discussed. For multiple-valued-logic applications and programmable XNOR, XOR, NAND, NOR logic gates the achieved low RTD peak-voltages are of major importance while enabling level compability.

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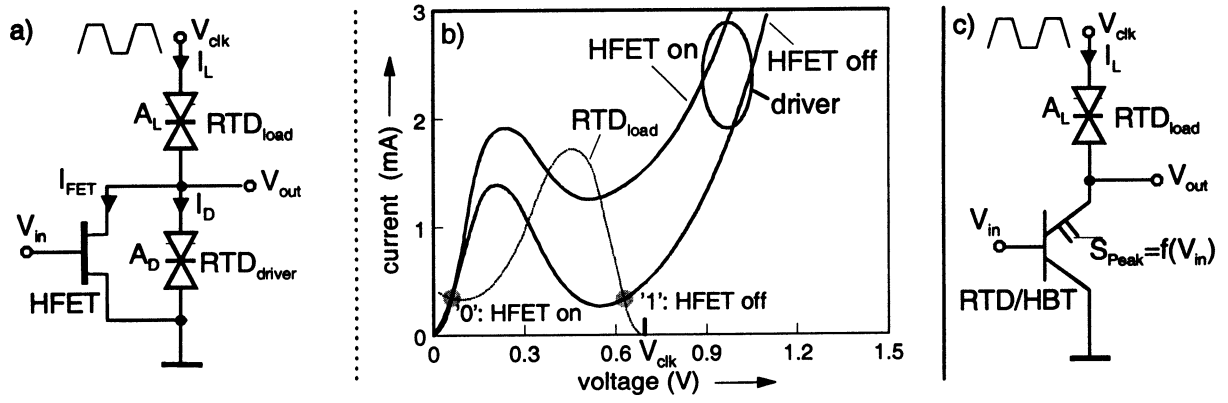


Figure 1: Fig. 1a) shows a MOBILE which can base on HFET/RTD or HBT/RTD devices while Fig. 1b) shows the corresponding switching behavior. The coupled RTD/HBT devices enables a direct control of S_{Peak} by input voltage V_{in} resulting in a simplified basic cell topology for MOBILE operation (see Fig. 1c)).

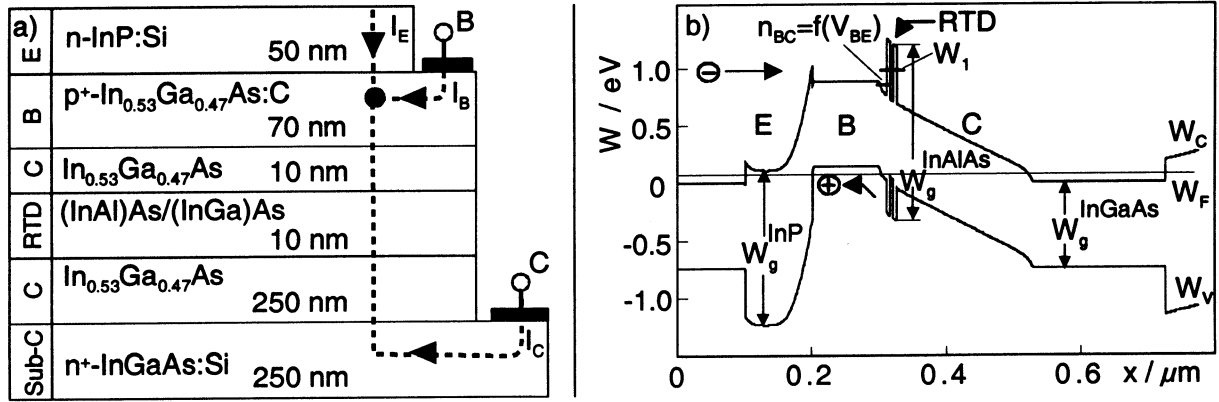


Figure 2: Fig. 2a) shows the layer stack of the coupled RTD/HBT device including the principle three mesa topology while in Fig. 2b) the corresponding band diagram for thermoelectric equilibrium is given.

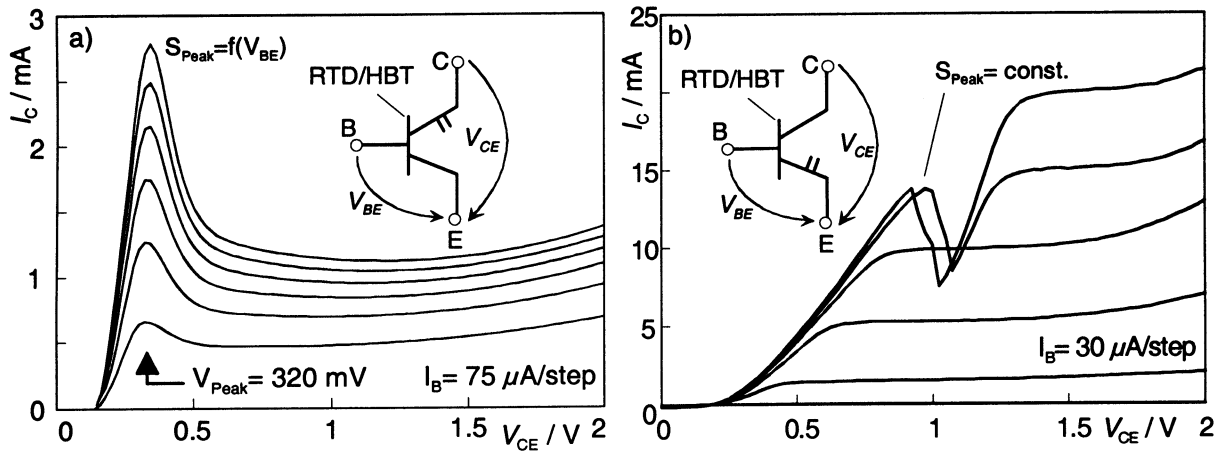


Figure 3: Fig. 3a) shows the common emitter dc-output characteristics of the proposed coupled RTD/HBT device while a RTD is integrated inside the collector near to the B/C-junction (see fig. 2) enabling an adjustable peak-current density $S_{Peak} = f(V_{BE})$. In contrast in fig. 3b) the RTD is inserted in the emitter path and the resulting device operates like a 'series-circuit' of HBT and RTD exhibiting a constant S_{Peak} dominated by the RTD layer sequence.

Excellent DC characteristics of HEMTs on semi-insulating silicon carbide substrate

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Abstract: The epitaxial layers of $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}/\text{GaN}$ were grown by MOCVD with a good uniformity and carrier mobility of $1281 \text{ cm}^2/\text{Vs}$ at room temperature. High electron mobility transistor (HEMT) have been fabricated using AlGaN/GaN heterostructure on semi-insulating silicon carbide substrate. The fabricated $2.2\mu\text{m}$ gate length $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}/\text{GaN}$ HEMTs exhibited high transconductance 287 mS/mm with high drain current density 857 mA/mm . This is the first report with highest transconductance so far achieved for $2.2\mu\text{m}$ gate length AlGaN/GaN HEMTs.

The $\text{Al}_{0.26}\text{Ga}_{0.74}/\text{GaN}$ layers were grown by atmospheric pressure MOCVD on (0001)-oriented semi-insulating 4H-SiC substrates using the following growth conditions. The device structure consists of 3 nm un-doped AlGaN barrier layer, 15 nm silicon doped AlGaN supply layer, 7 nm un-doped AlGaN spacer layer, 3000 nm insulating GaN (i-GaN) layer and a 200 nm AlN buffer on top of the SiC substrate. Aluminium content of the all AlGaN layers was 26%. The device isolation was accomplished by mesa dry etching down to the i-GaN by BCl_3 plasma reactive ion etching. The ohmic contact was performed by the deposition of a $\text{Ti}/\text{Al}/\text{Ti}/\text{Au}$ (25/100/45/55 nm), which was subsequently alloyed at 770°C for 60 s in N_2 atmosphere. The gate metals of $\text{Pd}/\text{Ti}/\text{Au}$ (40/40/80 nm) were performed optically defined $2.2 \mu\text{m}$, $3.0 \mu\text{m}$ and $5 \mu\text{m}$ long gates using optical lithography through conventional lift-off method. The DC characteristics were measured in dark using HP4145B semiconductor analyser.

Good $I_{\text{DS}}\text{-}V_{\text{DS}}$ characteristics (Figure 1) of a $2.2 \mu\text{m}$ gate length and $15 \mu\text{m}$ gate width HEMT, yielding a maximum current density of 867 mA/mm and a record extrinsic transconductance of 287 mS/mm for the gate voltage of 0.2 V . From the transfer characteristics (figure 2), the observed maximum drain-source current density is 1100 mA/mm for the gate and drain voltage of 3.8 and 10 V . The $I\text{-}V$ characteristic is noteworthy for its minimal current decrease at large dissipation levels due to self-heating. Owing to the excellent thermal conductivity of the SiC substrate, the current density decreases during the sweep (857 mA/mm to 833 mA/mm) by only 2.8% when the drain bias is increases to 20 V . The self-heating effect is high for sapphire based device structures.

In summary, we have demonstrated for the first time, high transconductance

$\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}/\text{GaN}$ based $2.2\mu\text{m}$ gate HEMTs with good I-V characteristics grown on semi-insulating SiC substrates. These HEMTs exhibited a high transconductance and drain current density of 287 mS/mm and 857 mA/mm , respectively. The fabricated high transconductance AlGaIn/GaN HEMTs on semi-insulating SiC substrates will be very much suitable for high power and high frequency applications.

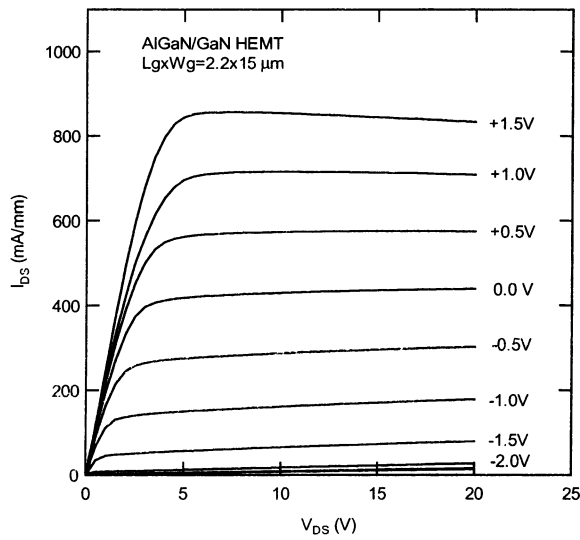


Figure 1. $I_{\text{DS}}\text{-}V_{\text{DS}}$ characteristics of HEMT for $L_g/W_g=2.2/15\text{ }\mu\text{m}$. V_{GS} is $+1.5\text{ V}$ to -3.0 V in steps of 0.5 V .

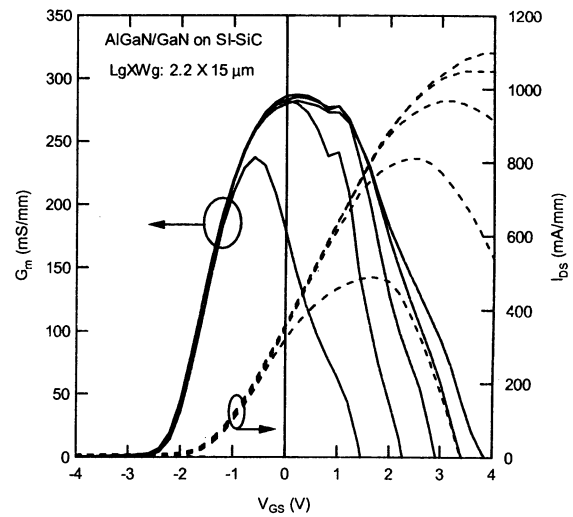


Figure 2. Transfer characteristics of HEMT for $L_g/W_g=2.2/15\text{ }\mu\text{m}$. V_{DS} is 2 V to 10 V in steps of 2 V .

A Quantum Dot FET

- A Future Playground of Quantum State Manipulation -

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We report a novel functional transistor which yields drain current peaks according to a dot-confined energy-states (shell structures) by scanning gate voltage and/or external magnetic field by controlling the interplay between charging energy and the dot confined energy states. Remarkable result is that the average "single-dot" energy states were resolved despite the inhomogeneous variations of the quantum dot ensemble. It would lead to an FET which manage to control quantum states in a "average quantum dot" state by normal FET operation of gate and drain voltage control.

The d-doped channel transistor structure was formed in adjacent to the InAs dots in a heterostructure shown in Figs.1 and 2. The average size of the InAs dots were 25Å in height and 170Å in diameter. The average number of dots under the 3µm x 10µm gate is estimated to be approximately 6,600. The charging states of the dots under the gate can be monitored by the current peaks due to threshold voltage shift caused by the spontaneous charging of dots when the Fermi level crosses the dot confined states as shown in Fig.3. The energy separation generally consist of confinement energy and charging energy. The evidences of observing the "single dot" state are (i) the energy separation of the almost equally spaced three pairs of peak curves range from 20meV (s-shell) to 16meV (p-shell), which is well accounted for by the charging energy of the dots, (ii) the slope of the "s-shell" peak in B² dependence in Fig.4 yields average electron cloud extent, $\langle x^2 \rangle$, to be 90Å, which is consistent with the estimation from the lateral dot size, (iii) the slope difference of the pairs of "p-shell" curves is well understood by the orbital splitting of the p-state electrons and the splitting in linear scale fits to 2.21meV/T which in turn yields 0.052m₀ [1][2] for the effective mass in the InAs dots.

The critical issues for the success which are different from the previously reported works[3][4] are: (i) the appropriate structural design to be able to monitor dot energy states as low as the ground state, (ii) complete elimination of dopants from the barrier layers, (iii) large enough energy spacing between dot-confined sublevels to be resolved without smearing due to size distribution of the quantum dots, (iv) device operation with low drain bias (V_d=300µV) so that the quantum dots under the gate electrode equally contribute to the total charging effect. The advantage of the present structure is that the "single dot" state level can be resolved using "ensemble of dots" through semiconductor channel current. Furthermore, the "quantum-dot-state" is read and written by the transistor current. Now that the read/write operation of a "single" dot is in hand, the most promising application would be semiconductor-based "qubit " in solid-state quantum computer. Combination with the spin-polarized electron injection technique would constitute an example of a "qubit " in a future solid-state quantum computer.

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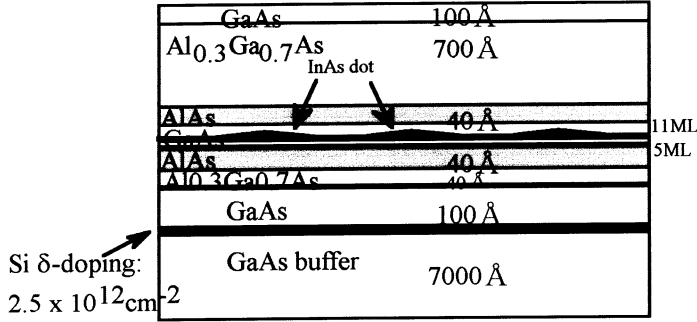


Fig.1 The heterostructure of the δ -doped channel structure. Self-assembled InAs dots were formed 200 Å apart in adjacent to the channel.

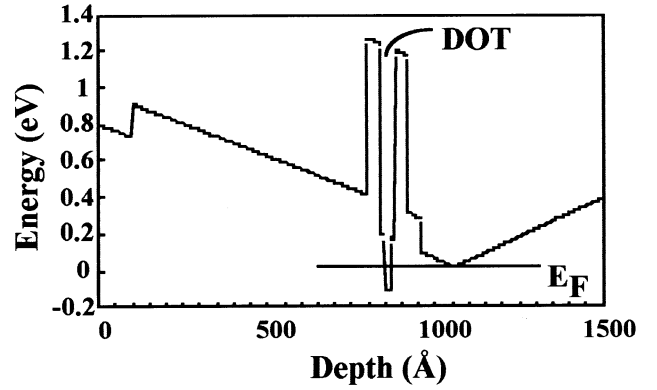


Fig.2 The energy band diagram of the device structure.

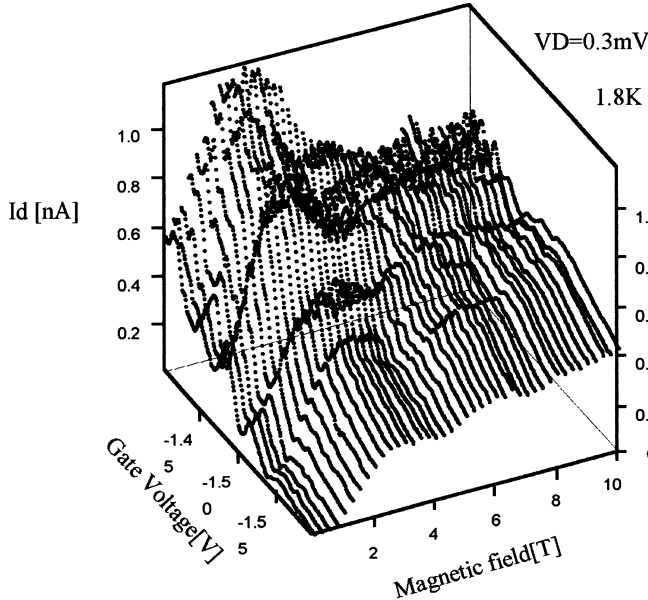


Fig.3 The current-voltage characteristics at low current region. Magnetic field is applied perpendicular to the surface up to 10 Tesla.

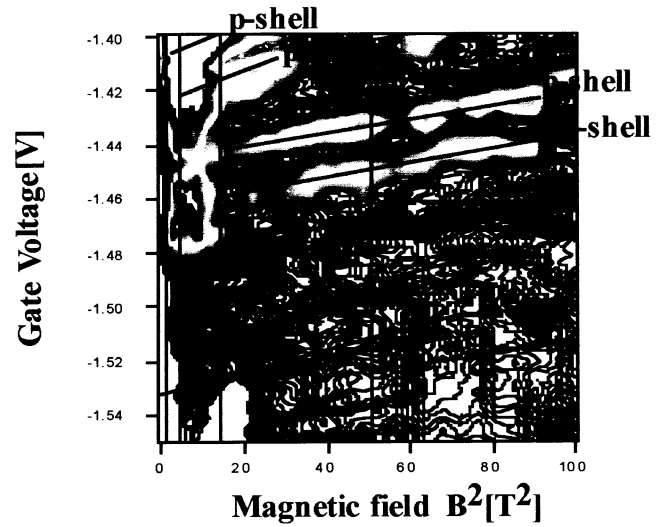


Fig.4 Contour plot of drain current of the same sample as in Fig.3. This is a reproduction of Fig.3 with the horizontal axis revised to B^2 .

Sub-40nm V-groove MOSFETs

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In past years opinions about the ultimate scaling limits of MOSFETs have often been revised, and experimentalists have proven that aggressive scaling results in high performance devices in the sub-50nm channel length regime.¹⁻⁵ The question of how far the reduction of MOSFET size can be driven - while obtaining improved device characteristics - remains open.

In a previous article,⁶ we showed that a V-groove design can be used to achieve sub-0.1 μ m MOSFETs. A thick raised source/drain structure of highly n-doped silicon on top of an ultra-thin p⁻ silicon channel (see Fig. 2) combines the advantages of low contact resistances with the suppression of short channel effects. Here, we present most recent results on V-groove MOSFETs with a source/drain separation down to $L_g = 36$ nm exhibiting state of the art electrical characteristics.^{4,5} We therefore demonstrate that the V-groove MOSFET has potential for sub-40nm operation.

Using an anisotropic etch, V-grooves can be generated in silicon with the flanks of the groove defined by the {111} silicon planes. Combining this with an MBE grown, highly Sb-doped n⁺⁺ region ($\approx 10^{20}\text{cm}^{-3}$, grown at 600°C) on top of a 15nm lightly p-doped ($5 \times 10^{14}\text{cm}^{-3}$) channel layer (being part of an SOI structure), allows one to define source, drain and an ultra-short channel in a single step. Provided that the V-groove opening is chosen according to the doped silicon thickness, the V-groove can be engineered such that the n-doped layer is fully cut through - thus defining source and drain - while leaving the p⁻ channel layer untouched. Since no annealing step is necessary for the definition of source and drain, an extremely abrupt doping profile results. Using an electron beam patterned etch mask as shown in Fig. 1, MOSFETs with nominal V-groove openings L_0 varying from 100nm to 160nm and a channel width of $W_0 = 700$ nm have been fabricated. A typical cross section for the smallest V-groove opening is shown in Fig. 2. The channel length L_g for this device is 36nm, much smaller than the actual lithographic pattern defining L_0 . (Due to the processing details the final V-groove opening is approximately 40% larger than the nominal design.). After source/drain and channel definition a low-temperature gate oxide of $\approx 26\text{\AA}$ was grown and a tungsten metal gate is defined.

Fig. 3 shows the output characteristic of a 36nm V-groove MOSFET (100nm V-groove opening). Figs. 4 and 5 illustrate the corresponding sub-threshold and transfer characteristics (straight black lines) as well as the characteristics for 110nm and 120nm V-groove openings. For our smallest devices we find a sub-threshold slope of 150mV/dec, $I_d = 415\mu\text{A}/\mu\text{m}$ and a specific transconductance value of around $1000\mu\text{S}/\mu\text{m}$ (both for $V_{gs} = V_{ds} = 1\text{V}$). From the output conductance data of Fig. 6, we calculate an intrinsic output resistance of only $500\Omega\cdot\mu\text{m}$. In total, we characterized four transistors with sub-40nm gate length and similar electrical behavior. Comparing these results with recent publications^{4,5}, we find that our transconductance value for the same gate voltage over-drive is state of the art, in particular, taking into account that both, the gate oxide ($\approx 26\text{\AA}$) and the p⁻ layer (15nm) are rather thick. The large channel layer thickness also is responsible for the slope of the sub-threshold swing. Reduction of p⁻ thickness is expected to significantly improve the device performance in terms of DIBL.

Figs. 4 and 5 also contain our results on wider V-groove openings of 110nm (dotted black lines) and 120nm (straight gray lines) again for a nominal channel width of $W_0 = 700$ nm. For V-groove openings beyond 120nm no transistor action was observed. This is the case since for large values of L_0 the channel layer gets fully consumed. Drain currents and transconductances (G_m) decrease very strongly with V-groove opening, as shown in Figs. 4 and 5, for openings of 100nm, 110nm and 120nm. Clearly part of this is caused by an increase in channel length, as supported by the improved sub-threshold characteristics shown in Fig. 4, but the increased opening also has an impact on the channel width. At larger L_0 the p⁻ layer gets partly consumed by the etch due to non-uniformities, resulting in a decreased effective channel width. The critical dimensions of these devices will be determined, by destructive analysis, once all electrical measurements are done.

In conclusion, we have demonstrated that a V-groove MOSFET concept is capable of generating high performance transistor characteristics of sub-40nm MOSFETs.

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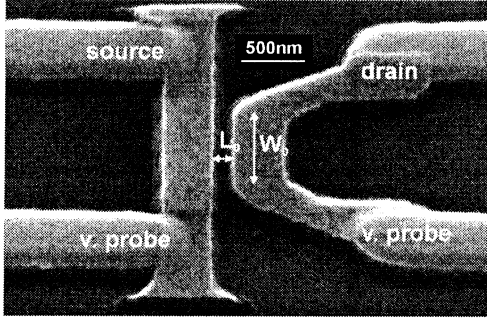


FIG. 1. SEM top view of a V-groove MOSFET before gate oxidation and gate metal deposition. L_0 is the V-groove opening, W_0 the nominal transistor width of around 700nm. Two source and two drain contacts are connected to allow to perform four-terminal measurements.

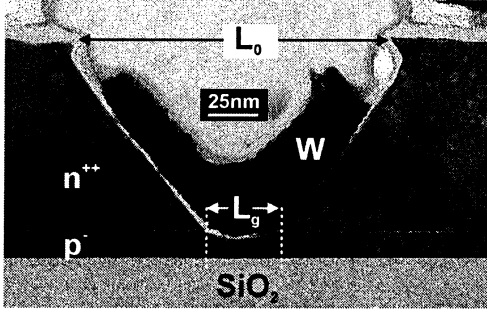


FIG. 2. TEM image of a 36nm MOSFET V-groove device. Tungsten (W) is used as a metal gate in our approach. Mention the flat bottom part of the V-groove allowing for optimum transport conditions in the channel of length L_g in the p^- region.

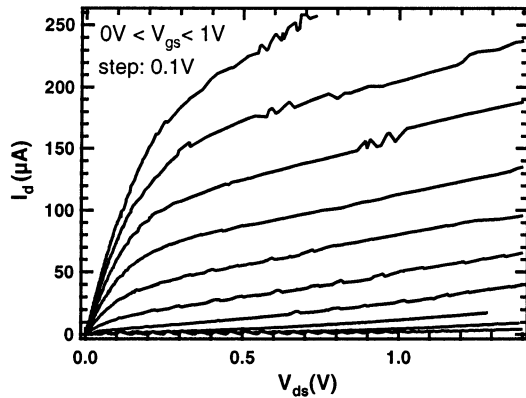


FIG. 3. Output characteristics of a 36nm ultra-short channel lengths MOSFETs (Corresponding to a nominal V-groove opening of 100nm.). The jogs in the output characteristics resulted from the interpolation of our four-point measurements.

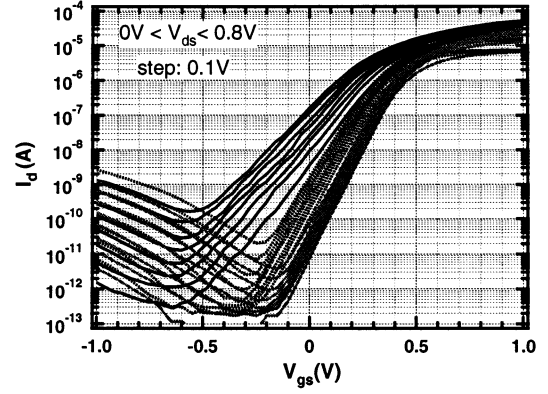


FIG. 4. Sub-threshold characteristics for V-groove openings of 100nm (straight black), 110nm (dotted black) and 120nm (straight gray).

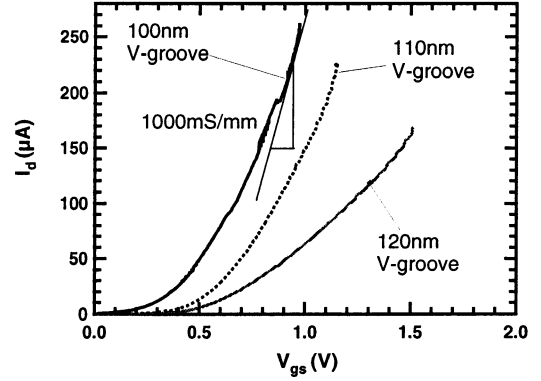


FIG. 5. Transfer characteristics of the three device classes under investigation. Line types as in Fig. 4. As in Fig. 3, the jogs result from the interpolation of our data.

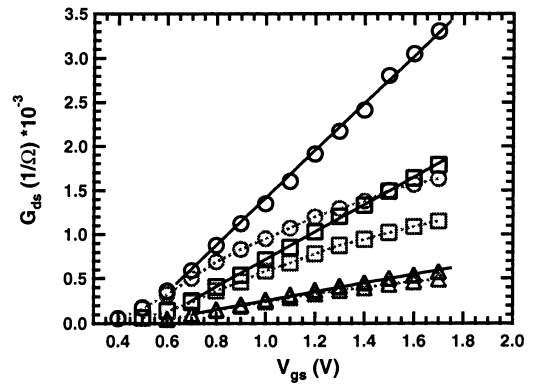


FIG. 6. Conductance in the linear output region for the three device classes under investigation (circles: 100nm, squares: 110nm, and triangles: 120nm nominal V-groove opening). The straight black lines are the result of subtracting a constant 310Ω spreading resistance due to the n^{++} contact regions.

Terahertz Plasma-Wave Excitation in 80-nm Gate-Length GaAs MESFET by Photomixing Long-Wavelength CW Laser Sources

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Emerging information technologies necessitate further extension of operating frequency bands in electronic systems to beyond terahertz (THz). Conventional semiconductor device technologies, which rely upon real-carrier transport, however, face to the substantial limit of operation in the THz region. New operating principles should be appreciated to establish novel THz device technology for the real applications.

Two-dimensional electron plasma in the electron channel of submicron FET's can make resonant oscillation in the THz range. Dyakonov and Shur formulated the 2-dimensional plasma dynamics as a function of device parameters and applied gate bias voltages V_{gs} (offset from the threshold) [1]. The THz radiation can be coherently absorbed via inter-subband transitions of conduction electrons if the electrons are transversely well confined in the channel. The resonant intensity increases with the plasma coherency, or equivalently with $v_p \tau / L$, where v_p the plasma-wave velocity, τ the plasma relaxation time, L the gate length. The resonance frequency is given by the standing-wave condition, proportional to v_p / L . The resonance frequency can be externally controlled by V_{gs} , since v_p is a function of V_{gs} , which offers the tunability of oscillation. The THz plasma resonant phenomena, however, has only been measured by illuminating a AlGaAs/GaAs HEMT with a single 2.5-THz gas laser source [2], and there has been no experimental reports on the resonance frequency dependence on V_{gs} . This paper demonstrates the first experiment on it.

Experimental setup is shown in Fig. 1. A pair of wavelength-tunable CW laser sources having a 100-nm band around 1550 nm was prepared for. The terahertz excitation was performed by photomixing the two sources in a manner of difference-frequency generation. The plasma resonance effects modulate the DC drain-source potential, which is originated from even-mode harmonic resonance components. Thus, the modulated DC drain-source components ($O[100 \mu V]$) were precisely measured by using a lock-in amplifier. An 80-nm gate-length GaAs MESFET [3] was selected as a sample. The gate width is 100 μm (12.5 $\mu m \times 8$ sections). The photomixed laser beam was linearly polarized along the channel axis and illuminated onto one section of the channel as shown in Fig. 2. The difference frequencies were set at 0.96, 1.55, and 2.55 THz.

In general, the semi-insulating GaAs material is transparent to the photon in the 1550-nm range. However, because of the deep trap centers produced by Cr and O doping for defect compensation, significant photocurrent was generated under both single-laser and photomixed-laser illuminations (see Fig. 3). In order to discriminate the effect of the plasma resonance from the background, the measured DC drain-source voltages (initially biased at +0.2 V) under single-laser illumination were subtracted from those under photomixed-laser illumination, which is hereafter denoted as DC drain-source modulation component ΔV_{ds} . V_{gs} dependence of ΔV_{ds} was measured under each difference-frequency condition. Figs. 4 (a) and (b) plots the measured and simulated results. The vertical axis $\Delta V_{ds} \cdot V_{gs}$ corresponds to the plasma resonance intensity. The results clearly indicate the occurrence of plasma resonance at the peak points of $\Delta V_{ds} \cdot V_{gs}$. In the simulation, the plasma-wave velocity v_p was accurately calculated taking the V_{gs} dependence of the density of electrons in the MESFET channel into account. Compared the measured results to the simulated ones, as shown in Fig. 5, the V_{gs} dependence of the resonance frequency well coincides with the simulated results. In summary, although the measurement is an indirect observation, it was verified for the first time that the plasma resonance frequency is controlled externally by V_{gs} in a wide terahertz range.

The authors thank Dr. Eiichi Sano and Koichi Narahara at NTT Laboratories for their valuable discussion and providing the GaAs MESFET wafer samples. This work is partially supported by NTT Laboratories and Ministry of Public Management, Public Affairs, Posts and Telecommunications, Japan.

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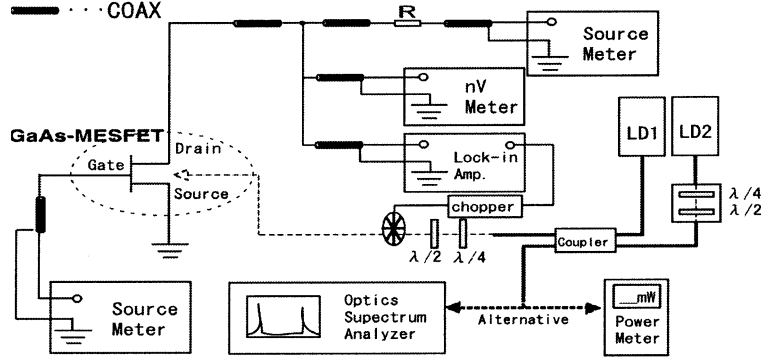
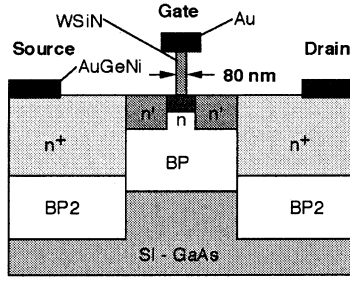
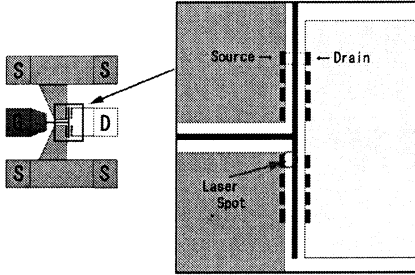


Fig. 1 Experimental setup.



(a) Cross sectional view.



(b) Pad layout and illumination point.

Fig. 2 80-nm gate-length GaAs MESFET.

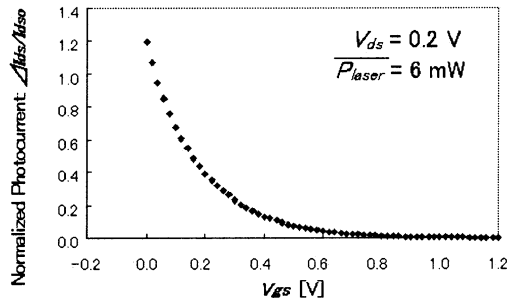


Fig. 3 Measured photocurrent ΔI_{ds} vs. V_{gs} . The vertical axis is normalized by original drain current I_{dso} .

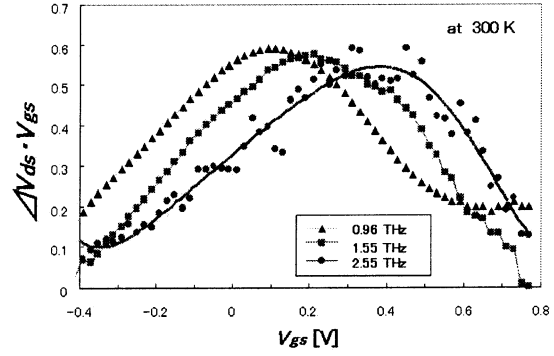


Fig. 4(a) Measured resonance intensity vs. V_{gs} .

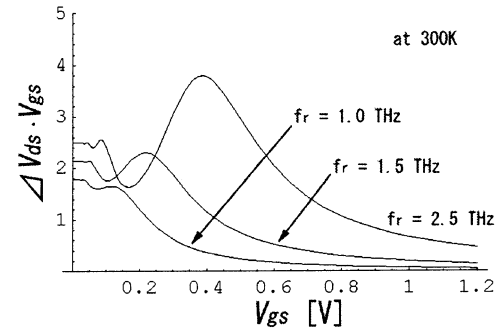


Fig. 4(b) Simulated resonance intensity vs. V_{gs} .

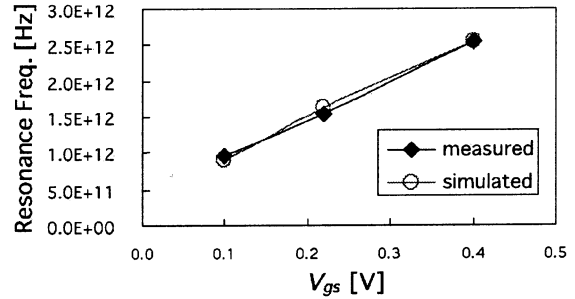


Fig. 5 Resonance frequency vs. V_{gs} .

Fabrication of InP DHBTs with 0.1 μm wide emitter

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InP based double heterojunction bipolar transistors (DHBTs) with emitter width of 0.1 μm were reported. Emitter mesa with vertical facet was formed by combination of CH_4/H_2 -reactive ion etching (RIE) and wet etching using two different HCl based solutions. Self-aligned base electrode was formed with 0.1 μm thick InP emitter layer, by control of the lateral extent of undercut etching less than 0.1 μm .

In HBTs, size reduction of emitter is significantly effective for high-speed operation when extrinsic base-collector capacitance can be reduced [1,2]. We previously reported fabrication process of a 0.1- μm -wide emitter by wet etching [3]. Because undercut etching of InP layer on $\langle 010 \rangle$ facet was fast, thin InP emitter must be used. As a result, we could not make a self-aligned base metal. Moreover, the smallest width of the operated transistor was 0.5 μm at the previous report.

In this report, fabrication process of a 0.1- μm -wide emitter for a self-aligned base metal is described. By combination of dry etching and wet etching, 0.12 μm -height emitter mesa could be fabricated. DC characteristics of HBTs with 0.1- μm -wide emitter are also reported.

Used epitaxial structure was shown in Table 1. After formation of emitter electrode (Ti/Pt/Au/Ti = 20/25/200/20 nm) by electron beam lithography and liftoff technique, GaInAs and InP layers were etched by CH_4/H_2 -RIE. Although RIE showed the advantage in anisotropic etching, the disadvantages were low selectivity of material and damage of etched facet. Etched surface after 100 nm-etching had roughness with diameters of 10-20 nm. Thus additional wet etching was essential.

Remained thickness of the InP layer after RIE was adjusted to 10 nm. $\text{HCl}:\text{H}_3\text{PO}_4=1:1$ at 1-2°C (etchant A) and $\text{HCl}:\text{H}_3\text{COOH}=1:4$ at 5-7°C (etchant B) were used in InP wet etching. When we used etchant A, obtained surface was smooth, but a tilted facet was observed partially as shown in Fig. 1. When we used etchant B, emitter mesa with vertical facet was formed, but some residuals of InP were observed on GaInAs surface as shown in Fig. 2, when the lateral extent of undercut etching was limited to 0.1 μm . Thus, we used combination of two etchant. The etchant A formed smooth surface while subsequent etching by etchant B formed vertical facet. The lateral extent of undercut etching could be suppressed to 0.1 μm . As a result, a 0.1- μm -wide emitter mesa was formed using a 0.3- μm -wide emitter electrode as shown in Fig. 3.

Combination of two wet etching was also effective for a narrow base mesa to reduce a base-collector capacitance [4]. By etchant A, the lateral extent of undercut etching was controlled, while vertical facet was formed by etchant B. Figure 4 shows the dummy sample of base mesa. A 0.3- μm -wide collector was confirmed, while the lateral extent of undercut etching was controlled to 1.5 μm .

HBT with emitter area of $0.1 \times 10 \mu\text{m}^2$ was fabricated. For interconnection of the fine emitter, wet-etched undercut air-bridge was used [5]. Figure 5 shows the SEM image of HBT after collector metallization. Width of the emitter mesa and the collector layer were 0.1 μm and 0.3 μm , respectively. A self-aligned base electrode was observed. Figure 6 shows the typical common-emitter I-V characteristic. Current gain was 12 at $V_C=5\text{V}$ and $I_C=60\mu\text{A}$. When we apply this process to fabricate HBT with the structure to reduce base-collector capacitance [1,2], high-speed operation of HBT can be expected.

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Table 1. Epitaxial layers of HBTs.

Layer	Material	Thickness [nm]	Doping [cm^{-3}]
Contact	n-GaInAs	20	2×10^{19}
Emitter	n-InP	10	2×10^{19}
Emitter	n-InP	90	5×10^{17}
Base	p-GaInAs	50	2×10^{19}
Collector	i-GaInAs	60	---
	n-InP	5	2×10^{17}
	i-InP	200	---
Subcollector	n-GaInAs	600	1×10^{19}
Buffer	i-InP	100	---

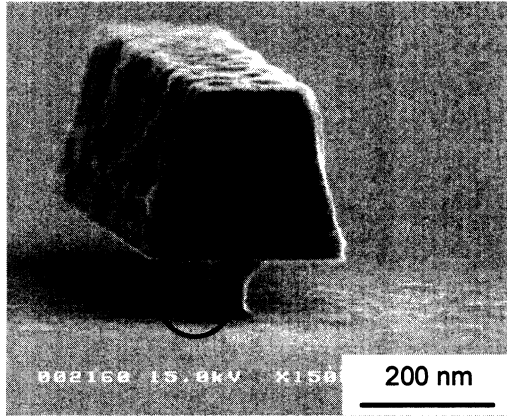


Figure 1. Test structure of emitter etched by CH_4/H_2 -RIE and $\text{HCl}:\text{H}_3\text{PO}_4=1:1$ solution. A circle shows a tilted facet.

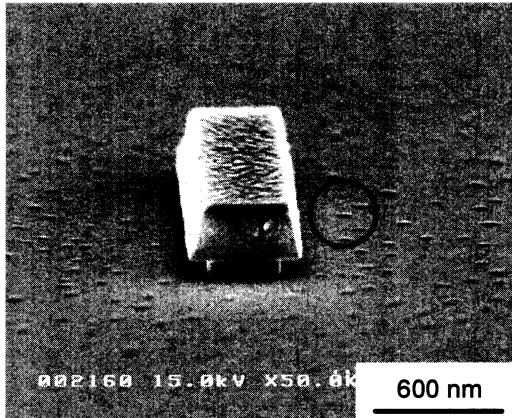


Figure 2. Test structure of emitter etched by CH_4/H_2 -RIE and $\text{HCl}:\text{H}_3\text{COOH}=1:4$ solution. A circle shows residuals of InP.

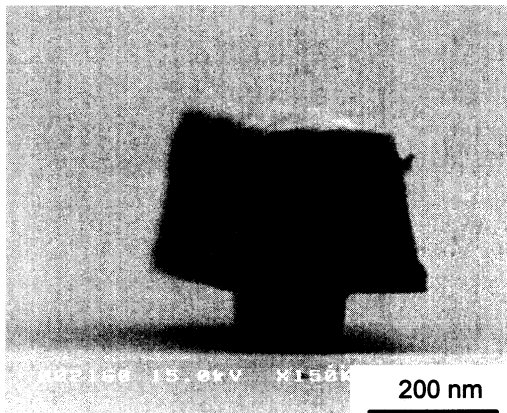


Figure 3. Test structure of emitter etched by CH_4/H_2 -RIE, $\text{HCl}:\text{H}_3\text{PO}_4=1:1$ and $\text{HCl}:\text{H}_3\text{COOH}=1:4$.

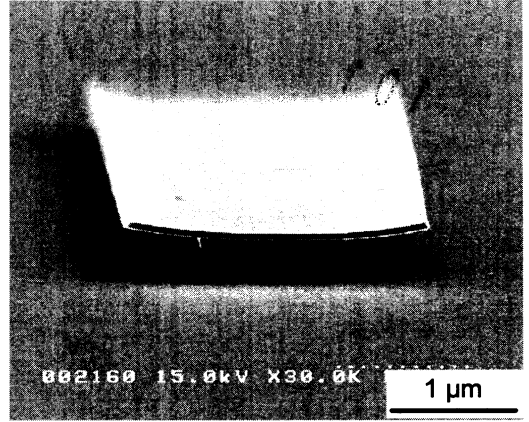


Figure 4. Test structure of base mesa without emitter. Width of collector layer was $0.3 \mu\text{m}$.

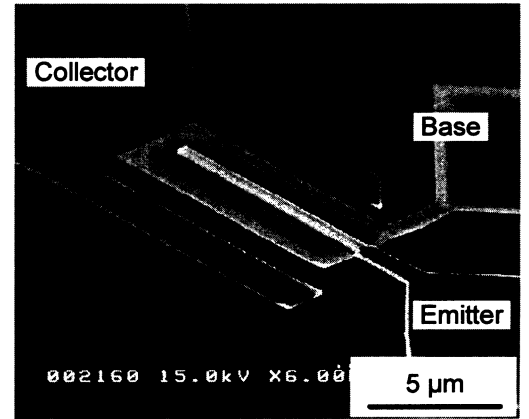


Figure 5. Fabricated HBT with emitter area of $0.1 \times 10 \mu\text{m}^2$.

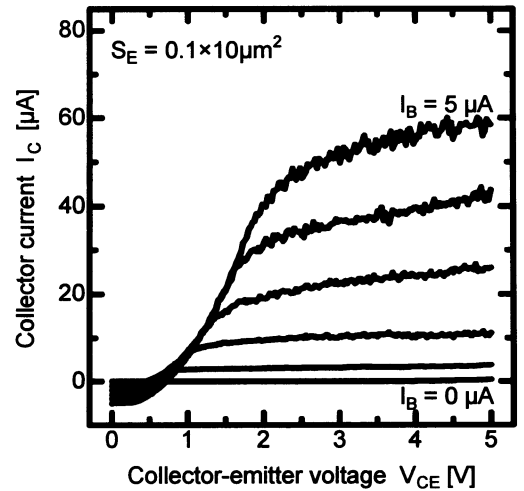


Figure 6. Measured common-emitter collector I-V characteristics.

Characteristics of Submicron HBTs in the 140-220 GHz Band

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We report the measurement of submicron transferred-substrate InGaAs/InAlAs heterojunction bipolar transistors (HBTs) in the 140-220 GHz frequency band. We believe this is the first reported characterization of HBTs above 110 GHz. Previous measurements of transferred-substrate HBTs have predicted record values of power gain cutoff frequency f_{max} by extrapolating at -20 dB/decade the unilateral power gain measured at 110 GHz [1]. Due to uncertainties associated with our measurement techniques, the unilateral power gain could not be determined for higher-gain devices. Additionally, transistor S-parameters measured in the 140-220 GHz band do not correlate well with a hybrid- π model derived from measurements at lower (6-45 GHz) frequencies.

The MBE layer structure and fabrication process are similar to those described in [2]. Electron-beam lithography was used to define submicron emitter and collector stripes. Two layer structures were considered. One layer structure consisted of a 40 nm base and a 300 nm collector. This layer structure was representative of that used for previously reported high f_{max} transistors [1]. The second layer structure had a 30 nm base, and a 150 nm collector. Devices on this layer structure were expected to have higher current gain cutoff frequencies f_T , and a lower $f_{max}:f_T$ ratio.

On-wafer measurements used an HP8510C network analyzer with Oleson Microwave Labs frequency extenders, connected to GGB Industries wafer probes via short WR-5 waveguides. Calibration used on-wafer Line-Reflect-Line (LRL) standards with extended reference planes for reduced probe coupling. The standards were measured after calibration to partially verify the calibration accuracy. The measurement of the through line standard showed the magnitude of S_{11} and S_{22} to be < -30 dB, and S_{21} had < 0.2 dB variation in amplitude and $< 3^\circ$ variation in phase. Measurement of the open standard showed an amplitude variation of < 0.1 dB and a phase variation $< 3^\circ$. Fig. 1 shows the measurements of the reflection coefficients for the through and open standards after calibration. Also shown on the graph is S_{21} for a long 50Ω line that was not used in the calibration. The measurement shows smooth amplitude and phase variation, as expected of a well-calibrated measurement.

Fig. 2 shows the unilateral power gain (U), the maximum stable gain (MSG), and the short circuit current gain ($h_{21} \sim f_T/jf$) for a device measured from 6-45 GHz and 140-220 GHz. The device was fabricated on 300 nm collector material, and had emitter and collector stripe widths of $0.4 \mu\text{m}$ and $0.7 \mu\text{m}$, respectively. The unilateral gain is not plotted in the 140-220 GHz band because measurements showed large variations in the parameter. At spurious intervals in the band the calculated U increases to infinity and then becomes negative. This effect is due to the very high transistor output impedance. At high frequencies the HBTs have low series input resistance ($\sim R_{bb}$) and extremely low shunt output conductance $G_{22} \approx j2\pi f C_{cb} h_{21}$, with the latter parameter being largely responsible for the high HBT power gain. Because of this very low G_{22} , $\|S_{22}\|$ is very close to unity, and small variations in the measured S_{22} result in large variations in the measured G_{22} and U. Extrapolating U from the 6-45 GHz measurements at -20 dB/decade predicts an f_{max} of ~ 600 GHz.

The measured S_{12} shows a rapid increase in magnitude over the 140-220 GHz range, increasing much more rapidly than expected given a fixed and frequency-independent collector-base capacitance C_{cb} . Consequently, the measured $MSG = \|S_{21} / S_{12}\| \sim 1 / \omega C_{cb} [R_{ex} + \kappa l / qI]$ decreases more rapidly than the theoretical -10 dB/decade. The anomalous S_{12} may be due to spurious probe-probe coupling or coupling between transistor input and output transmission-lines through substrate electromagnetic modes.

A hybrid- π model was derived from the 6-45 GHz measurements. The model is shown in Fig. 4, and the simulated S-parameters are included in Fig. 3. The modeled S_{11} and S_{22} are in poor agreement with measurements in the 140-220 GHz band. However, measurements of a single-stage amplifier using these devices were found to be in close agreement with simulations using the measured transistor S-parameters [3]. Measured amplifiers exhibit > 6 dB gain per transistor at 180 GHz, which is consistent with high transistor available power gain [4].

Fig. 5 and Fig. 6 show the measured gains and S-parameters for a transistor with a 150 nm collector. The device had emitter and collector stripe widths of $0.7 \mu\text{m}$ and $1.0 \mu\text{m}$. The thinner collector results in a higher C_{cb} , and thus a larger output conductance. The measurement of U appears well-behaved, decreasing at ~ -20 dB/decade. The f_{max} and f_T of the device are estimated to be ~ 220 GHz and ~ 200 GHz, respectively. 140-220 GHz measured parameters of this HBT are again not consistent with that of a hybrid- π model developed from 6-45 GHz measurements.

We believe this work represents the first attempt to accurately characterize transistors of any type in the 140-220 GHz band. The measured devices show evidence of high transistor power gain at submillimeter-wave frequencies. However, at this time, the measurement uncertainty is too large to accurately quantify the device performance in this band. This work was supported by the ONR under grant no. N0014-99-1-0041.

[1] Q. Lee *et al.*, 1999 IEEE Device Research Conference, Santa Barbara, CA. (postdeadline)

[2] Q. Lee *et al.*, 1999 IPRM, Davos, Switzerland.

[3] M. Urteaga *et al.*. To be presented 2001 MTT-S, Phoenix, AZ.

[4] M. Urteaga *et al.*. To be submitted.

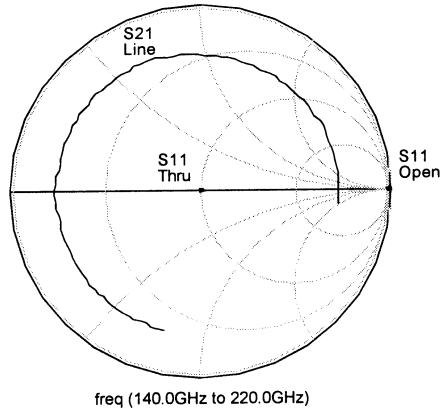


Fig. 1. Measurements of calibration standards after LRL calibration.

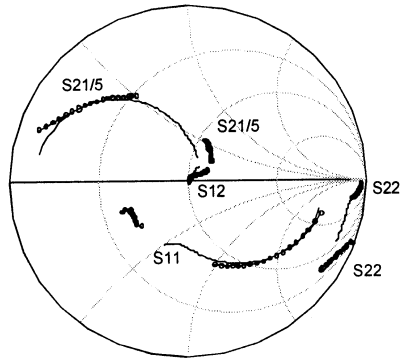


Fig. 3. Measured device S-parameters from 6-45GHz and 140-220 GHz for the transistor with a 300 nm collector. The solid line represents the equivalent circuit model derived from the low frequency measurements.

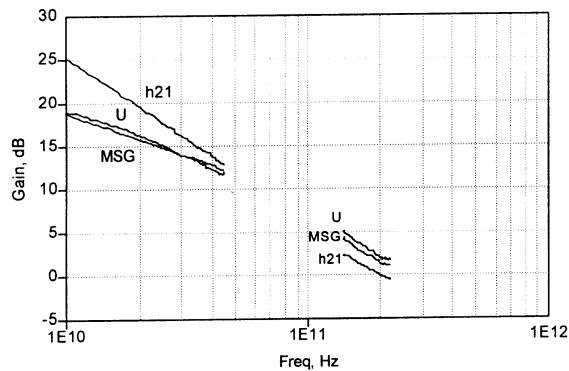


Fig. 5. Gains of $0.7 \times 6 \mu\text{m}^2$ emitter and $1.0 \times 6.4 \mu\text{m}^2$ collector HBT with a 150 nm collector. Bias conditions are: $I_C = 3.0 \text{ mA}$ and $V_{CE} = 1.0 \text{ V}$.

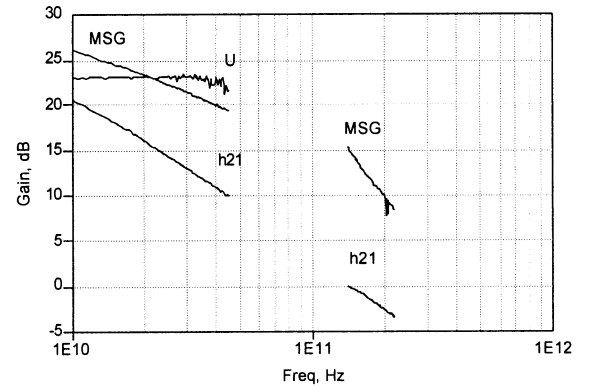


Fig. 2. Gains of $0.5 \times 6 \mu\text{m}^2$ emitter and $0.7 \times 6 \mu\text{m}^2$ collector HBT with a 300 nm collector. Bias conditions are: $I_C = 3.6 \text{ mA}$ and $V_{CE} = 1.2 \text{ V}$.

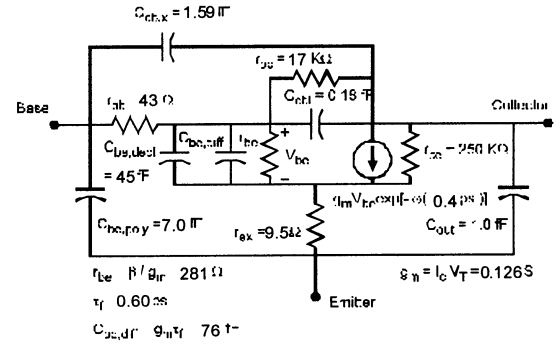


Fig. 4. Device equivalent circuit model for transistor with 300 nm collector. Bias conditions are: $I_C = 3.6 \text{ mA}$ and $V_{CE} = 1.2 \text{ V}$.

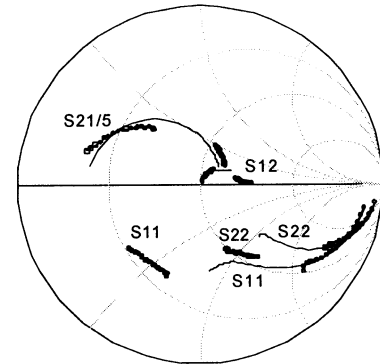


Fig. 6. Measured device S-parameters from 6-45GHz and 140-220 GHz for the transistor with a 150 nm collector. The solid line represents the equivalent circuit model derived from the low frequency measurements.

A QUANTUM-DOT CELLULAR AUTOMATA SHIFT REGISTER

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Quantum-dot Cellular Automata (QCA) is a computational paradigm [1] where the position of single electrons within cells, composed of coupled quantum dots, is used to encode and process binary information. In the past few years the basic QCA devices were experimentally tested and good agreement with theoretical predictions was demonstrated [2]. In the early asynchronous devices, pipelining was not possible due to lack of control over electron switching and power gain was not possible since the only source of energy was the input signal. To overcome these obstacles clocked control over the QCA circuitry was proposed [3,4]. In clocked QCAs, energy is supplied to the cells by the clock lines, rather than by inputs alone. As a result, in contrast to the edge driven cellular architectures, power gain, reduced power dissipation and pipelining can be achieved in clocked QCA systems. Recently, a functional clocked cell [5] and a QCA latch [6] were fabricated and tested.

Here we present a more advanced device in the family of clocked QCA systems - a two cell shift register. The device consists of two capacitively coupled QCA latches L_1 and L_2 (Fig. 1). The QCA latch [6] consists of three micron-sized aluminum islands, or dots (D_1 - D_3 for L_1 , and D_4 - D_6 for L_2), separated by tunnel junctions. Both L_1 and L_2 are leadless, i.e. they are not connected to any external charge reservoirs. Multiple tunnel junctions are used between dots to increase the charge retention time of the latches. Two single-electron electrometers measure the state of the shift register (E_1 reads the state of L_1 , and E_2 reads the state of L_2). The layout of the device is shown in Fig. 2.

Figure 3 demonstrates the operation of the device. To operate the shift register, a differential input signal V_{IN} is applied to the inputs V_{IN}^+ and V_{IN}^- at t_1 (Fig. 3 A). L_1 and L_2 remain in the neutral state until the first clock is applied (t_2 in Fig. 3 B). When the clock CLK_1 is applied to L_1 (t_2 in Fig. 3 C), an electron is switched and locked in the direction defined by the input signal. Once L_1 is set (i.e. an electron is locked on one of the end dots), input signal is removed (t_3 in Fig. 3 A) and the state of L_1 does not change. When the second clock CLK_2 is applied to L_2 (t_4 in Fig. 3 D), it switches in the direction defined by the state of the first latch (t_4 in Fig. 3 E). The state of L_2 remains unchanged when CLK_1 is removed and L_1 turns off (t_5 in Fig. 3 B & C), as long as CLK_2 is applied (t_6 in Fig. 3 E). As can be seen in Fig. 3 for the input signal of reversed polarity, the switching direction is reversed. An interesting feature of this design is that the propagation of the information can be reversed by changing clocking sequence and input gates, so the QCA shift register is a logically reversible device [7].

The current prototype operates at a temperature of 70 mK. However, future generations of the QCA devices based on new technologies are expected to work at liquid nitrogen (metal nanocluster QCA) and room temperatures (molecular QCA).

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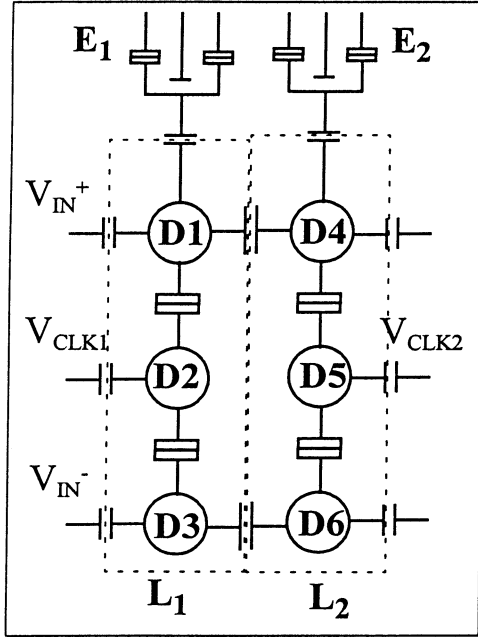


Figure 1. Schematic Diagram of a QCA shift register.

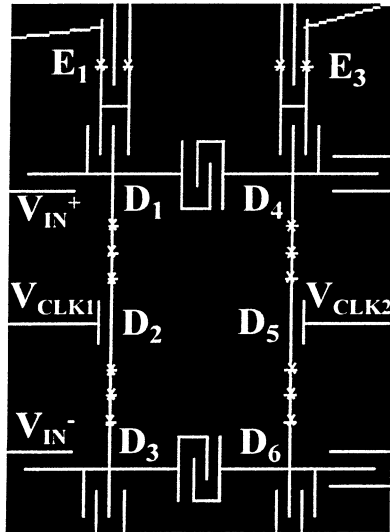


Figure 2. Layout of the device. Lines represent aluminum islands and leads and '*'s represent tunnel junctions.

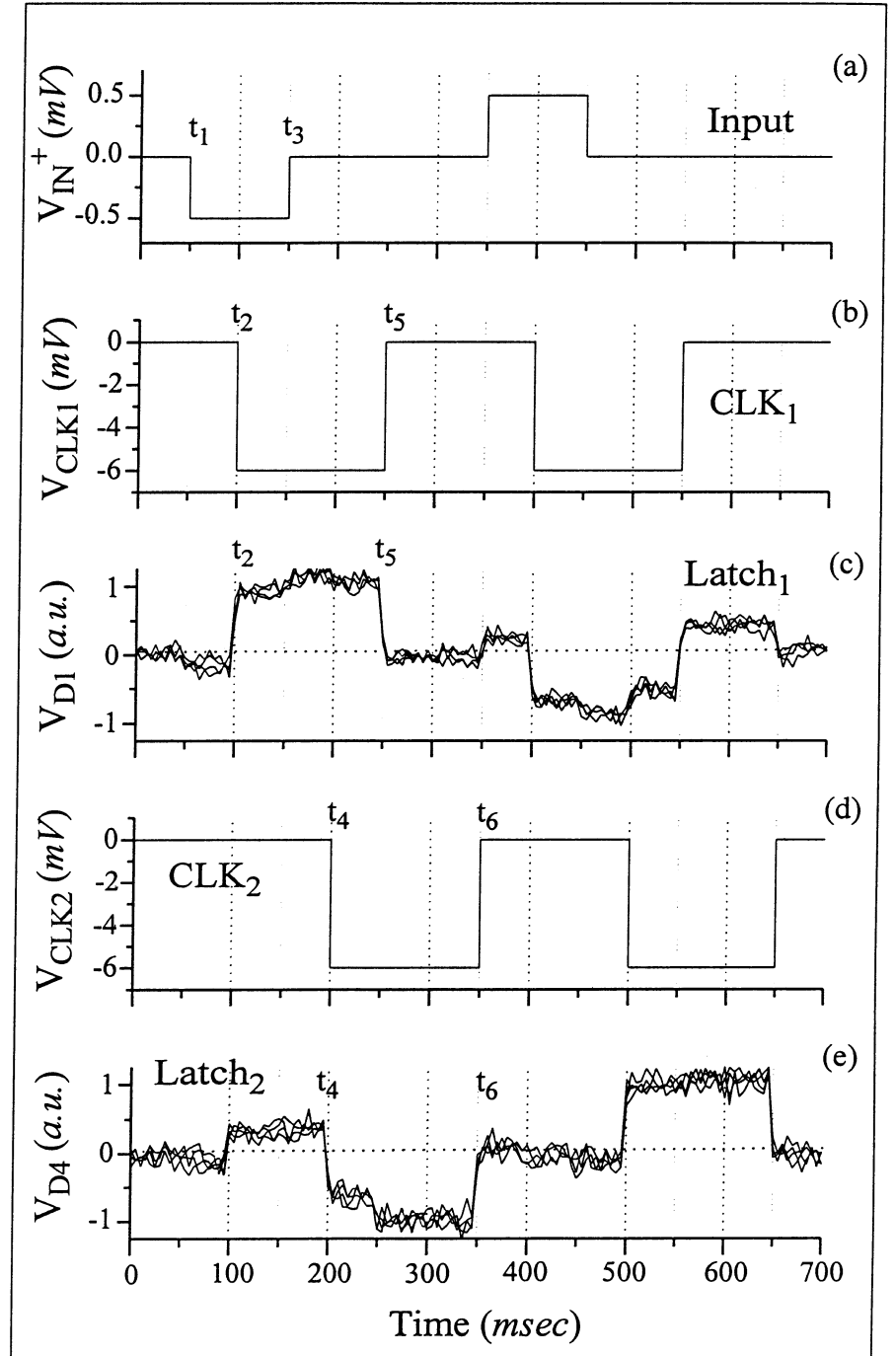


Figure 3. Operation of a shift register (a) Differential input signal ($V_{IN}^+ = -V_{IN}^-$) (b) Clock signal applied to latch L_1 (c) Potential on dot D_1 in arbitrary units (d) Clock signal applied to latch L_2 (e) Potential on dot D_4 in arbitrary units

Emerging Technologies

TUESDAY AM, JUNE 26TH, 2001

Session Organizer: Sanjay Banerjee, The University of Texas at Austin

9:00 AM, IV.-1 Invited

Nanotube Nanoelectronics: *Paul L. McEuen*^{1, 2}; J. Park^{2, 3}; A. Bachtold^{2, 3}; M. Woodside^{2, 3}; M. S. Fuhrer^{2, 3}; M. Bockrath^{2, 3}; L. Shi⁴; A. Majumdar⁴; P. Kim^{2, 3}; ¹Cornell University, Laboratory of Atomic and Solid State Physics, Ithaca, NY 14853 USA; ²University of California, Department of Physics, Berkeley, CA 94720 USA; ³University of California, Materials Sciences Division, Lawrence Berkeley National Laboratory, Berkeley, CA 94720 USA; ⁴University of California, Department of Mechanical Engineering, Berkeley, CA 94720 USA

9:30 AM, IV.-2 Invited

Molecule/Metal and Molecule/Semiconductor

Heterostructures for Electronic Devices: *David B. Janes*¹; Purdue University, School of Electrical and Computer Engineering, W. Lafayette, IN 47907 USA

10:00 AM, IV.-3 Invited

Integrated RF Passive Components - Discrete vs. Distributed:

*J. N. Burghartz*¹; K. T. Ng¹; N. P. Pham¹; B. Rejaei¹; P. Sarro¹; ¹Delft University of Technology, EC TM-DIMES, Feldmannweg 17, 2600 GB Delft, The Netherlands

10:30 AM Break

10:50 AM, IV.-4 Invited

Photonic Crystal Cavities and Waveguides: *A. Scherer*¹; O.

Painter¹; J. Vuckovic¹; M. Loncar¹; D. Dapkus²; I. Kim²; T. Pearsall³; ¹Caltech, MC 200-36, Pasadena, CA 91125 USA; ²University of Southern California; ³CERF Corning, Avon France

11:20 AM, IV.-5 Invited

Electronic Detection of DNA: Robust Platform for Integrated

Devices: *Robert H. Terbruggen*¹; Yin-Peng Chen¹; Hau Duong¹; Dan Farkas¹; K. M. Millan¹; Gary T. Olsen¹; Nathan Swami¹; Hai Wang¹; Handy Yowanto¹; C. J. Yu¹; Gary F. Blackburn¹; Jon Faiz Kayyem¹; ¹Motorola Clinical Micro Sensors, 757 South Raymond Avenue, Pasadena, CA 91105 USA

Nanotube Nanoelectronics

Paul L McEuen^{1,2}, J. Park^{2,3}, A. Bachtold^{2,3}, M. Woodside^{2,3}, M.S. Fuhrer^{2,3},
M. Bockrath^{2,3}, L. Shi⁴, A. Majumdar⁴, and P. Kim^{2,3}

(1) Laboratory of Atomic and Solid State Physics, Cornell University, Ithaca NY 14853

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(3) Department of Physics, University of California, Berkeley, CA 94720

(4) Dept. of Mechanical Engineering, University of California, Berkeley, CA 94720

Single walled carbon nanotubes (SWNTs) are emerging as the prototypical one-dimensional conductor. Since their discovery in the 90's, they have been the subject of amazingly intense study. Here we will review our group's work in this field -- the creation of tiny nanoelectronic devices with nanotubes as the active element. As we will see, some nanotubes are semiconductors, and can be used to construct devices that are the 1D analogs of the MOSFET. Other nanotubes behave as nearly perfect metallic conductors, and are proving to be a new laboratory for studying the physics of electrons in 1D. Both kinds of devices may have significant technological applications.

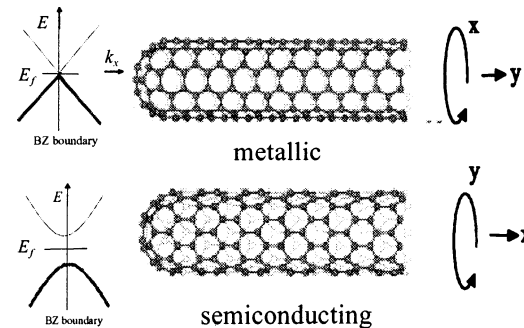


Figure 1

The remarkable electrical properties of SWNTs stem from the unusual electronic structure of the 2D material – graphene – from which they are constructed. It is called a semimetal (or zero bandgap semiconductor) since it is metallic in some directions in k -space and semiconducting in the others. When graphene is wrapped up to form a tube (see Fig. 1), the momentum of the electrons moving around the circumference of the tube is quantized. This quantization results in tubes that are either one-dimensional metals or semiconductors, depending on how the allowed momentum quantization values compare to the preferred directions for conduction. Nanotubes can be thus be either metals or semiconductors, depending on how the tube is rolled up. This remarkable theoretical prediction has been verified using a number of measurement techniques.

To create a device, tubes are either grown on the surface using CVD or deposited on the surface from a solvent. Lithography is used to pattern metallic electrodes that make contact to a single nanotube or nanotube bundle. A typical device and schematic is shown in Figure 2.

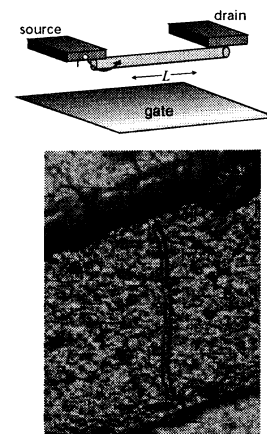


Figure 2

In addition to the source and drain electrodes, a third gate terminal is employed to electrostatically tune the carrier density on the tube. When tubes are measured, two types of behavior are observed, corresponding to metal and semiconducting tubes. Figure 3 shows the conductance of a semiconducting tube as the gate voltage is varied. The tube can be turned on by applying a negative bias to the gate and turned off with a positive bias, as first observed by the DELFT group. This device is analogous to a p-type MOSFET, with the nanotube replacing Si as the material that hosts charge carriers. The tube is intrinsically p-type due to doping by the Au electrodes as well as chemical species adsorbed on the tube. Tubes can also be doped n-type using dopants such as Potassium that donate electrons to the tube or by applying large positive voltages to the gate.

This semiconducting nanotube transistor is remarkable in many ways. For one, it has a width of only 1 nm. There has been a great deal of work to create ultrasmall semiconducting devices from bulk semiconductors, but these have always been plagued by surface states – electronic states that arise when the three dimensional crystal is interrupted by a boundary. These surface states generally degrade the operating properties of the device, and controlling them is one of the key technological challenges to device miniaturization. The nanotube solves the surface state problem in an elegant fashion. First, it begins with a 2 dimensional material whose surface is part of its inherent nature. It then rids itself of the problem of edges by using a topological trick – a cylinder has no edges.

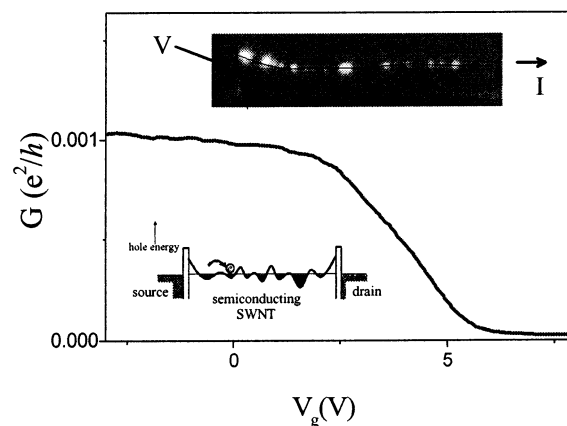


Figure 3

Looking more closely at the conductance in Fig. 3, we see that it initially rises linearly with V_g , conducting better as additional holes are added to the nanotube. The conductance is limited by any barriers that the holes see as they traverse the tube. This is schematically illustrated in Figure 3, where the potential landscape seen by the holes is a series of peaks and valleys. The holes must hop through this landscape in order for the tube to conduct. The resistance of the tube will be dominated by the highest barriers in the tube. Recent experiments by the Berkeley and DELFT groups confirm this simple picture. They use a scanning probe microscope tip to identify the major scattering sites. One such measurement is shown in the inset to Fig. 3. The bright spots correspond to places where the AFM tip affected the conductance of the sample, producing a map of the barriers to conduction.

At higher gate voltages, the conductance stops increasing and instead is constant. This limiting conductance is due to the contact resistance between the metallic electrodes and to the tube. In this device, this contact resistance is quite substantial. The value of this contact resistance can vary by orders of magnitude from device to device, probably due to mundane issues like surface cleanliness. Many groups are working to improve the quality of these contacts, with significant success.

We now turn our attention to the second type of tube. Figure 4 shows the conductance of another nanotube sample as a function of V_g at a variety of temperatures. Let us first concentrate on the behavior near room temperature. In dramatic contrast to the semiconducting nanotube, the conductance is not noticeably affected by the addition of a few carriers. This is typical of metals, where the number of carriers is large and the addition of a few more does not alter the conducting properties significantly.

The conductance of the metallic sample is also quite large in comparison to the semiconducting device. Indeed, a number of groups have measured tubes whose conductance is within a factor of a few of the value, $G = 4e^2/h$, predicted for a *ballistic* nanotube, i.e. one where the electrons are perfectly transmitted through the tube. This indicates that electrons can travel over micron length scales down the tube without scattering. A number of other measurements support this conclusion, including scanned probe experiments by our group.

These long scattering lengths are in striking contrast to the behavior observed in traditional metals like copper, where scattering lengths are typically on the order of 10^8 of nm at room temperature. The main reason is that acoustic phonons, the long wavelength lattice vibrations present at room temperature, do not have enough momentum to reverse the direction of the speeding electron in the nanotube. The same is not true for optic phonons, but these are too high in energy to be present at room temperature. Recent experiments by the DELFT group has shown that at high voltages, the electrons can emit optic phonons and therefore scatter. This leads to a dramatic reduction of the conductance at high biases and a saturation of the current. This saturation value is ~ 25 μA for a single nanotube, which is still a remarkably macroscopic current to be carried by such a nanoscopic system!

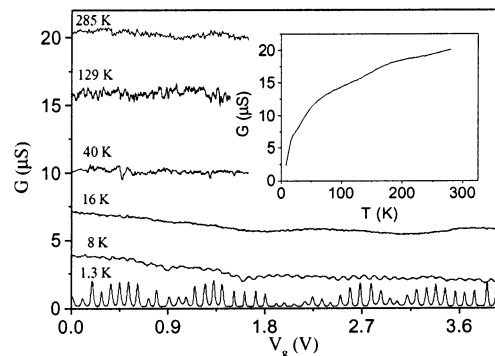


Figure 4

Further evidence for the near-perfect nature of these tubes comes from the low-T behavior seen in Fig. 4. The conductance is observed to oscillate as a function of gate voltage. These are called Coulomb oscillations, and occur each time an additional

electron is added to the nanotube. In essence, the tube is acting like a long box for electrons, often called a quantum dot. The electronic and magnetic properties of these nanotube quantum dots reveal a great deal about the behavior of electrons in nanotubes. For example, the fact that the oscillations are quite regular and periodic indicates that the electronic states are extended along the entire length of the tube. If there was significant scattering in the tube, the states would become localized at various locations along the overall tube length and the Coulomb oscillations would be less regular. Tube quantum dots as long as 10 μm exhibit these well-ordered oscillations, again indicating that the mean free path can be very long.

While the above experiments demonstrate that many of the basic properties of SWNTs are now understood, there are an almost limitless number of new geometries and topics to be explored. For example, many groups have now created free-standing nanotube devices, and the interactions between the mechanical and electronic degrees of freedom are beginning to be investigated. In addition, devices consisting of multiple nanotubes are being studied by our group and others. The thermal properties of tubes are also being actively investigated, and measurements by our group indicate that the thermal conductivity can be extremely high. Fabrication techniques are also rapidly improving. By growing tubes on prefabricated structures, by pushing them around with AFM tips, and by a host of other new techniques creatively combining lithography, chemistry, and nanomanipulation, many new structures are being created. It is remarkable how far the field has come since the first measurements in 1997, and it shows no signs of slowing.

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Molecule/Metal and Molecule/Semiconductor Heterostructures for Electronic Devices

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The field of molecular electronics involves using organic or biological molecules as electronic components, typically in the form of metal/molecule/metal structures in which each molecule is nominally connected to a contact at each end. Recently, interesting functionalities have been demonstrated in molecular devices, including negative differential resistance devices with large peak-to-valley ratios, memory devices with nearly nonvolatile storage, and control of conductivity via molecular doping [1-3]. Although the exact mechanisms responsible for the non-monotonic current-voltage relationships and memory effects are not yet known, it appears that the mechanisms are different from those that dictate conventional semiconductor device behavior. Overall, there are a number of interesting molecular properties that could serve as the basis for novel electronic devices, including oxidation/reduction events, in which the molecules exchange electrons with contacts, structural reconfigurations and selective optical absorption/emission. For most of the molecular systems studied to date, the nature of the interface between the molecular layers and the contacts has not been well controlled or well understood. Development of suitable electronic components based on these properties will require the development of well-understood molecular/metal heterostructures. In addition, the development of molecular/semiconductor heterostructures would allow direct integration with well-established semiconductor devices and circuits. Just as well-understood semiconductor heterostructures have enabled a number of high-performance electronic and optoelectronic devices, molecular based heterostructures would represent an enabling technology for new classes of devices.

This presentation will discuss the experimental and theoretical work at Purdue aimed at developing and understanding molecular heterostructures. These studies include measurements of electrostatic surface potentials of self-assembled monolayers (SAMs) on metal and semiconductor surfaces, current-voltage spectroscopy of molecular systems and modeling of the conductivity of metal/molecule/metal systems. One of the fundamental issues involved in understanding and modeling the conduction properties of these systems is the relative position of the molecular states with respect to the Fermi level. This band alignment, along with the broadening of molecular states associated with bonding to the metal, determines the low-field conductivity as well as the turn-on voltage of metal/molecule/metal systems[4]. Knowledge of these quantities allows the prediction of band line-ups in much the same fashion as in semiconductor heterostructures or metal-semiconductor (Schottky) junctions. In contrast to typical semiconductor layers, there is no "bulk" region in the molecular systems, so bulk molecular properties such as electron affinity do not provide complete information. The electrostatic surface potential of the molecular layer with respect to that of the metal substrate is a key parameter in determining the nature of the molecule/metal junction, since it provides information

about the charge transfer between the molecule and metal. The current studies involve an integrated experimental and theoretical effort to characterize and model these systems.

Toward the goal of integrated molecular/semiconductor devices, we have also developed and characterized nanoscale molecule/semiconductor heterostructures. The approaches employ directed self-assembly techniques, in which chemical affinities are used to organize pre-formed elements into highly ordered networks of nanostructures and resist-free patterning techniques are used to realize the specific structures needed for interconnect lines or substructures for devices. This effort has led to the demonstration of low-resistance nanoscale ohmic contacts [5] and to the development of self-assembly techniques for well ordered nanoscale metal islands with strong electronic coupling to semiconductor device layers [6].

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Integrated RF Passive Components – Discrete vs. Distributed

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Passive components have been recognized as performance as well as cost limiting elements of integrated radio-frequency (RF) systems [1]. While the integration of high-quality (Q) capacitors at small area appears feasible, those requirements are not easily met for inductors [2]. The frequency range, at which discrete spiral inductors can efficiently be used, is limited at around 1 GHz by size and at about 15 GHz by the controllable minimum inductance value (Fig.1). Distributed networks on silicon substrates appear feasible for frequencies above 35 GHz, at which the length of a $\lambda/4$ –transmission line becomes smaller than 1 mm. In the intermediate frequency range from 15 GHz to 35 GHz neither discretely nor distributed elements can easily be applied. Here, periodic structures, consisting of discrete components and transmission line sections and operating in slow-wave mode, can provide practical solutions [3].

Discrete spiral inductors can be designed on silicon with a nearly constant inductance over a wide frequency range, but Q is quite frequency dependent (Fig.2). With ohmic losses in the spiral coil dominating at low frequencies and substrate losses being most severe at high frequencies, Q develops a distinct maximum [2]. It is desired to shift that maximum to the operating frequency of the circuit. Here, one can take advantage of the availability of multi-level interconnects in silicon process technology and use either stacked metal layers to reduce the ohmic losses in the metal or omit the lowest metal layers to reduce the capacitive RF leakage through the substrate (Fig.2). The result of this optimization concept is shown in Fig.3a, where in a given lateral coil layout the vertical design is used to shift $Q_{\max}$ over a range of roughly 3 GHz. It also seems favourable to use stacked metal layers in large inductors, while omitting the lower metal layers for substrate loss reduction appears more effective in small inductors (Fig.3b). In spite of those means of optimization, large inductors typically have lower $Q_{\max}$'s than small inductors (Fig.4). Higher Q may also come from an improvement in process technology, either by replacing aluminum (Al) by copper (Cu) as metallization (Fig.4) or by low-loss substrates [2].

Transmission lines are preferably integrated as microstrips instead of coplanar wave guides, since those use less chip area. Microstrips, however, cannot be built at low losses by using multi-level interconnects, because the available vertical spacing between signal and ground planes is too small. This leads to a microstrip structure with a ground plane built in the silicon substrate at a spacing of about 150 μm beneath the wafer surface, as shown in Fig.5d. Such a microstrip can be fabricated in post-processing (Fig.5a-d; Fig.6) after the standard silicon processing is finished [4]. Microstrips with a loss as low as 3-dB/cm at 17 GHz can be fabricated provided, that a high-resistivity silicon substrate is used (Fig.7). The main constraints are coming then from the always present parasitic surface layer, which results from contamination of the field oxide and the dc bias of the signal line. Microstrips appear to have lower loss and bias dependence than coplanar wave guides, if built on high-resistivity silicon substrates [5].

While there is currently still much activity on optimization of integrated RF passives, one should already look ahead to integrated transmission line structures at micro- and millimeter waves and combinations of both for periodic structures in the intermediate frequency range.

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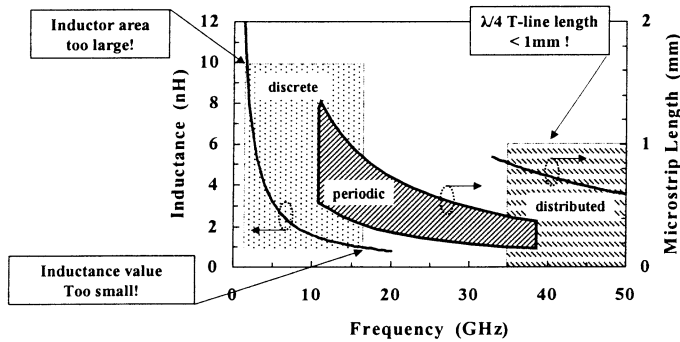


Fig.1 Frequency dependencies of discrete inductors at 50 Ω impedance, $\lambda/4$ transmission lines, and periodic slow-wave structures with 2x-5x size reduction.

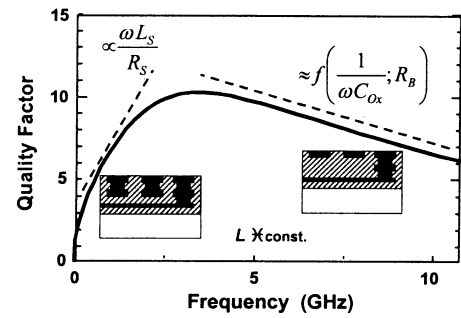


Fig.2 Quality factor of a spiral inductor on a silicon substrate as function of frequency with illustration of ohmic losses and substrate losses at low and high frequencies, respectively, and coils with stacked and omitted metal layers for optimization of Q [2].

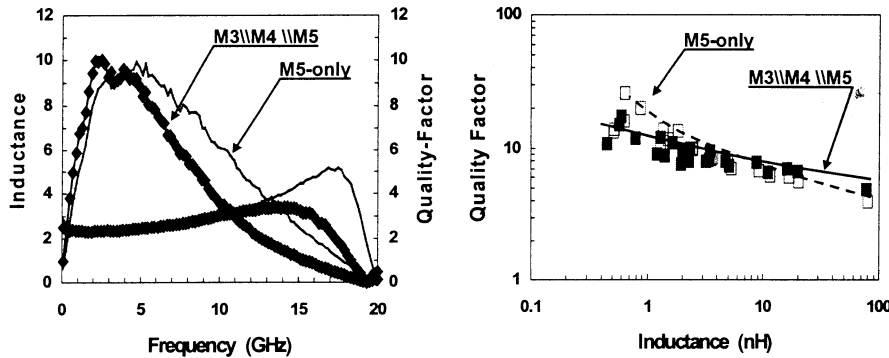


Fig.3 Dependencies of (a) inductance and Q on frequency for inductors with stacked metal layers and using only the top metal layer and (b) of Q on inductance for inductors ranging from 0.5 nH to 90 nH [2]

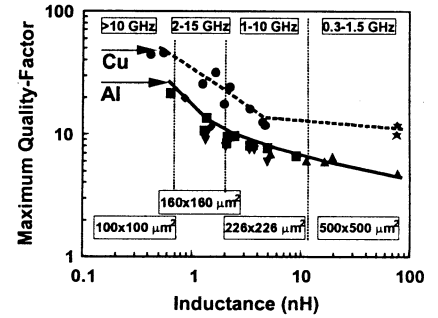


Fig.4 Maximum Q vs. inductance of spiral inductors on 15-ohm-cm silicon in the range 0.5 nH and 90 nH with Al and Cu metallization [1],[2].

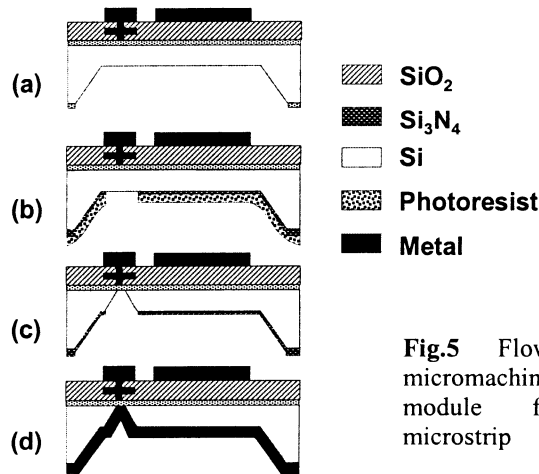


Fig.5 Flow of the bulk-micromachining post-process module for optimized microstrip integration on

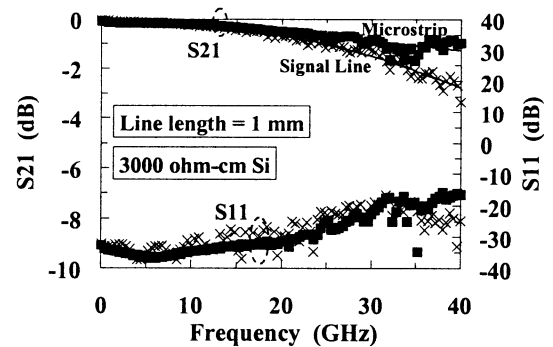


Fig.7 Microstrip on 3-kohm-cm silicon.

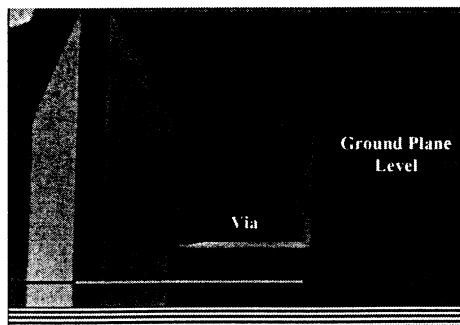


Fig.6 Plan view of a section of a wafer after application of the steps a-c of the post-process module illustrated in Fig.5.

Photonic Crystal Cavities and Waveguides

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Recently, it has also become possible to microfabricate high reflectivity mirrors by creating two- and three-dimensional periodic structures. These periodic “photonic crystals” can be designed to open up frequency bands within which the propagation of electromagnetic waves is forbidden irrespective of the propagation direction in space and define photonic bandgaps [2,3]. When combined with high index contrast slabs in which light can be efficiently guided, microfabricated two-dimensional photonic bandgap mirrors provide us with the geometries needed to confine and concentrate light into extremely small volumes and to obtain very high field intensities [4,5]. Here we show the use of these “artificially” microfabricated crystals in functional nonlinear optical devices, such as lasers, modulators, and waveguides.

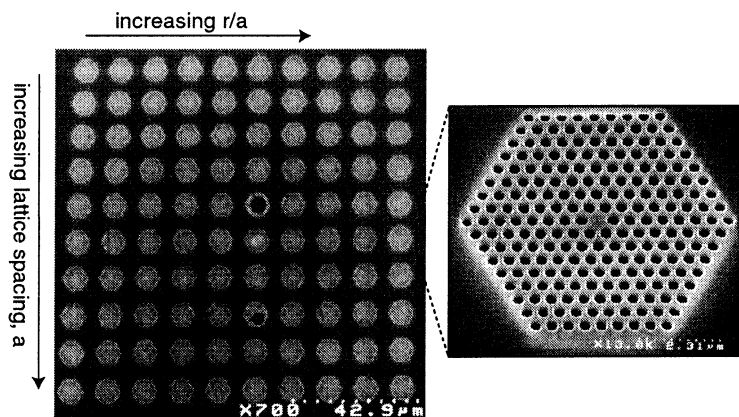
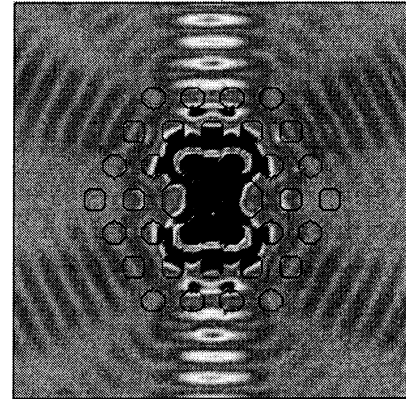


Figure 2. 10x10 multi-wavelength laser array within a 100x100 micron area. Each laser emits at a lithographically controlled optical components and leads to their integration in large numbers, much in the same way

In-Plane emission (FDTD simulation)



Vertical Emission (cut through slab)

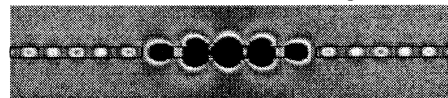


Figure 1. Field Intensity of light leakage from a single defect surrounded by 3 periods of photonic crystal and slightly enlarged holes in the horizontal direction. Light preferentially emits in the y dipole.

Sub-wavelength nano-optic cavities can be used for efficient and flexible control over both emission wavelength and frequency. Similarly, nanofabricated optical waveguides can be used for efficient coupling of light between devices. This new capability allows the reduction of the size of

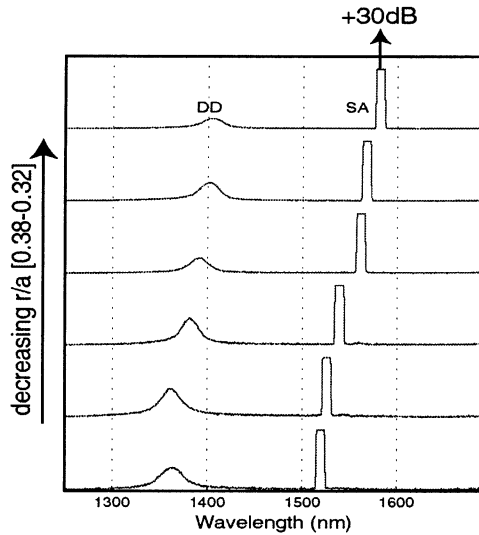


Figure 3. Sample spectra taken from lasers defined within the 10x10 array

smallest optical cavities [6], with mode volumes down to $2.5 (\lambda/2n_{\text{slab}})^3$, or $0.03 \mu\text{m}^3$ in InGaAsP emitting at $1.55 \mu\text{m}$. We have also been able to tune the emission wavelength of these lasers from 1450nm to 1620nm within a 10x10 laser array in an area of $100 \mu\text{m} \times 100 \mu\text{m}$ by local lithographic modification of the cavity lengths. As the mode volumes of nano-cavities are decreased, the coupling efficiency between the spontaneous emission within the cavity and the lasing mode can be significantly improved [7]. We have calculated spontaneous emission coupling factors (β) above 85% for optimized photonic crystal lasers constructed in active quantum well material [8]. This spontaneous emission coupling efficiency can be even higher if the linewidth of the semiconductor emission is narrowed, as will be the case when using quantum dot active material. Therefore, single

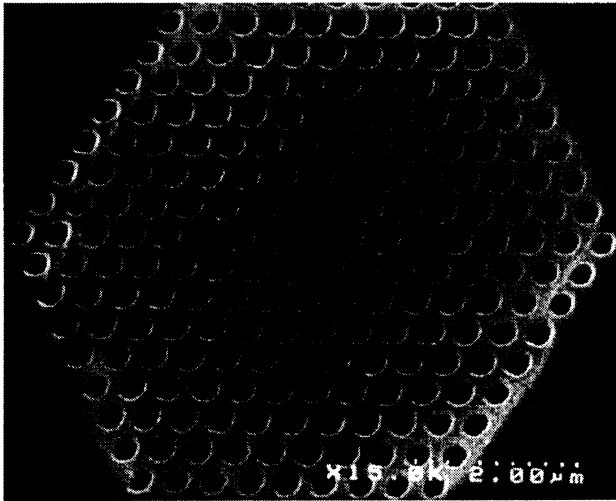


Figure 4. Multiple cavities fabricated on a Si wafer.

negligible diffraction losses. Photonic crystals are also the perfect medium for constructing what have been termed “photonic molecules”, or interconnected cavities that

as electronic components have been integrated for improved functionality to form microchips. As high-Q optical and electronic cavity sizes approach a cubic half-wavelength the spatial and spectral densities (both electronic and optical) increase to a point where the light-matter coupling becomes so strong that spontaneous emission is replaced by the coherent exchange of energy between the two systems.

The lithographic control over the wavelength and polarization supported within photonic crystal cavities can also be used to construct compact nanophotonic laser and detector arrays, as well as all-optical gates and routers. We have already demonstrated room temperature lasing in the

defect photonic crystal lasers represent in many ways the ultimate evolution of VCSELs, since control over both vertical and lateral spontaneous emission is possible. With most of the spontaneous emission funneled into a single optical mode, the photonic crystal laser can be modulated at much higher frequencies even close to threshold. The photonic crystal provides us with the unique opportunity of coupling light emitted by one cavity, and using it to optically pump another with

can share and exchange photons. Finally, we have shown that the emission wavelength of light from these photonic crystal lasers can be varied by simple adjustments of the lithographic pattern during their fabrication. Thus, single mode lasers emitting at 1450nm can be fabricated only microns apart from lasers emitting at 1600nm, and could share the same waveguide slab. Photonic crystals provide us with the opportunity of constructing very compact laser sources with designed frequencies (Figure 3) and polarization as well as wavelength and polarization sensitive detector arrays. Moreover, they can form very flexible platforms for connecting optical sources, detectors, routers, modulators, polarizers and filters in very compact microfabricated systems.

At $\sim 1.5\mu\text{m}$ wavelengths, it is possible to use silicon as a low-absorption waveguide material, and to leverage from the extensive fabrication and wafer preparation experience of the microelectronics industry. In particular, semiconductor on insulator (SOI), such as Smartcut and SIMOX structures lend themselves well to fabrication of single mode waveguides from high index silicon and the fabrication of passive 2-D photonic crystal structures. In one commercially available SOI process, called Smartcut, it is possible to form a well-defined silicon dioxide layer underneath a thin slab of single crystal silicon layer at the surface (Figure 6). When designed properly, this slab can serve as a high index optical waveguide, and can easily be patterned to define 2-D PBG material.

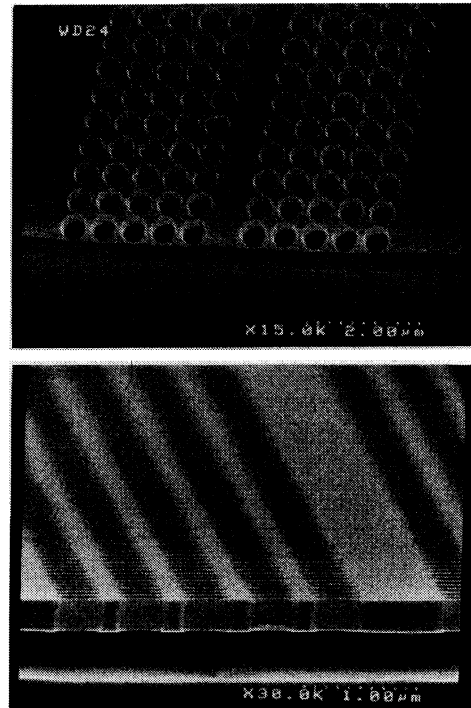


Figure 5. Angle view and crosssection through a suspended photonic bandgap waveguide fabricated from SOI silicon.

Photonic crystal waveguides play a crucial role in photonic crystal integrated circuits. These waveguides are responsible for transferring light throughout the integrated circuit as well as for the coupling of light into and out of the integrated circuit. Therefore, a careful investigation of the properties of these waveguides is an important of our research. Our goal is to combine theoretical analysis and optimization with experimental techniques to develop a systematic method for design of the waveguides and control of the properties of the waveguide modes to obtain the optimum performance for the desired application.

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Electronic Detection of DNA: Robust Platform for Integrated Devices

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Sample-to-answer devices that both amplify and detect nucleic acid targets will find use in health-care, agricultural, forensic medicine, military applications, environmental monitoring and animal husbandry. Ideally, these devices will be able to start with almost any sample input, be inexpensive to manufacture, utilize portable instrumentation, and require no user intervention. In practice, developing devices that meet these criteria are difficult due to limitations imposed by the enzymatic amplification procedures, and the DNA detection platform. Motorola's Clinical Micro Sensors division has recently developed and commercialized an electronic nucleic acid detection platform that simplifies the process for building sample-to-answer devices.

This electronic detection platform utilizes self-assembled monolayer chemistry (Figure 1) coupled with alternating current voltammetry (ACV) to produce a robust sensor that is capable of detecting low levels of bound target. Electronic DNA detection has been implemented into a variety of different substrates including printed wiring board, ceramic and silicon. The sensors are prepared on metallic gold surfaces that have been prepared using standard processing techniques developed for the electronics and semiconductor industries. Compared to nucleic acid sensors that utilize fluorescence detection, electronic detection offers comparable sensitivity with the added advantage of low cost instrumentation, and the ability to detect the DNA without subsequent washing steps following hybridization (homogeneous detection). Other aspects of the electronic detection platform are the ability to detect DNA without time consuming labeling steps via use of presynthesized ferrocene labeled oligonucleotide probes that bind target through a sandwich configuration. The electronic detection is a non-destructive technique allowing for continuous monitoring of the binding process (Figure 2), and the quantitative nature of the measurement allows for determination of target abundance. Electronic detection has been shown to be a versatile platform upon which to develop molecular diagnostics and protocols for carrying out common diagnostics assays like genotyping and gene expression monitoring have been developed.

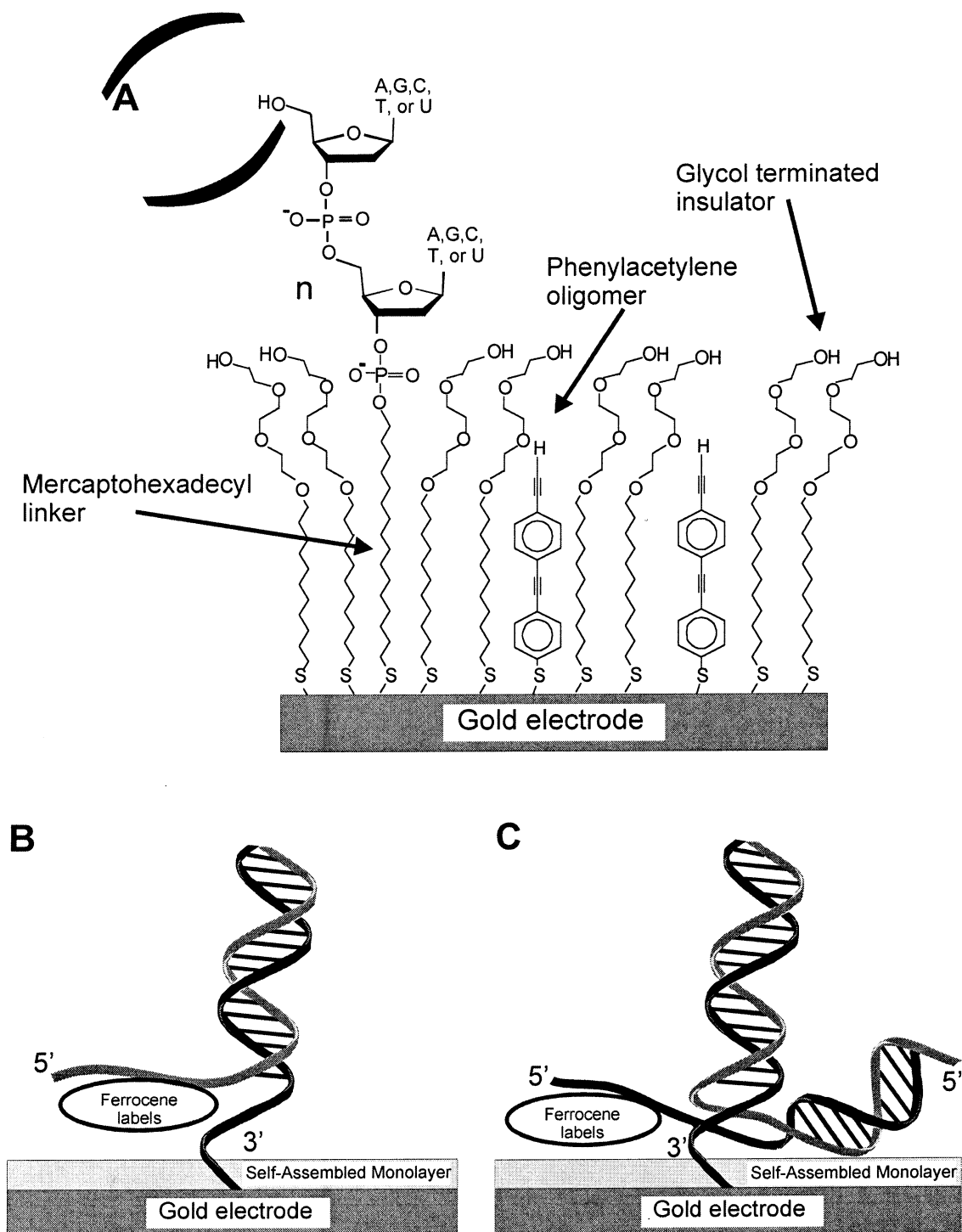


Figure 1

Figure 1. Electrode surface and labeling strategies. (A) Schematic representation of the capture surface. The sensor surface is a multi-component SAM that contains a glycol-terminated insulating molecule, a conjugated phenyleneacetylene thiolate, and alkane thiol-linked single-stranded DNA attached via the 3'-end. (B) Illustration of a labeled target captured on the sensor electrode. (C) Illustration of a "sandwich" assay. The

ferrocene-labeled signaling probe hybridizes to the region of the target that is proximal to the capture sequence. The ferrocene labels are incorporated immediately 5' to the signaling probe recognition sequence.

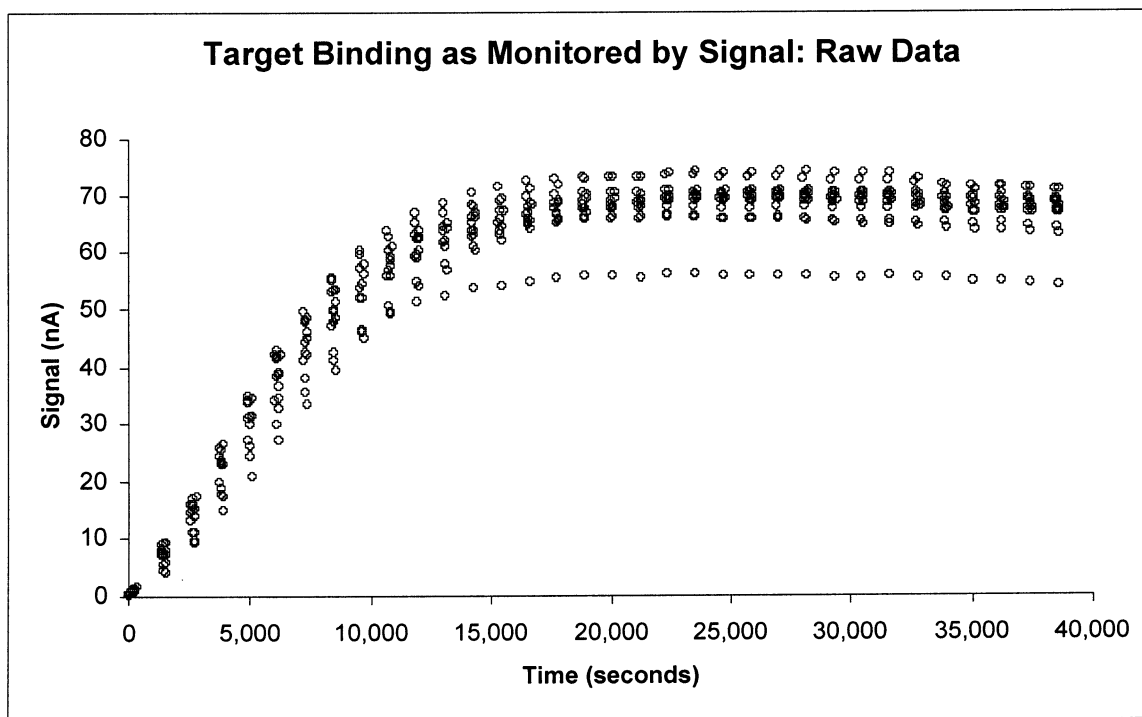


Figure 2. Plot of the raw signal as a function of time for 14 individual electrodes modified with the same capture surface. Target is labeled via the sandwich configuration as illustrated in figure 1C.

Novel Devices

TUESDAY PM, JUNE 26TH, 2001

Session Organizers: Rick Kiehl, University of Minnesota

2:00 PM, V.A.-1 Invited

Tunable Two-Electron Spin States in Quantum Dot Structures and the Applicability for Making Spin Qubits: *S. Tarucha^{1,3}; K. Ono²; D. G. Austing³; S. Sasaki³; T. Fujisawa³; Y. Tokura³; L. P. Kouwenhoven⁴; ¹ERATO Mesoscopic Correlation Project & ²Department of Physics, University of Tokyo, 7-3-1 Bunkyo-ku, Hongo, 7-3-1 Tokyo 113-0033, Japan; ³NTT Basic Research Laboratories, Morinosato Wakamiya, Atugi-shi, Kanagawa 243-0198, Japan; ⁴ERATO Mesoscopic Correlation Project, & Department of Applied Physics, Delft University of Technology, P.O. Box 5046, 2600 GA Delft, The Netherlands*

2:30 PM, V.A.-2

A Multiple-Valued SRAM with Combined Single-Electron and MOS Transistors: *Hiroshi Inokawa¹; Akira Fujiwara¹; Yasuo Takahashi¹; ¹NTT Basic Research Laboratories, 3-1 Morinosato Wakamiya, Atsugi-shi, Kanagawa Pref., 243-0198 Japan*

2:50 PM, V.A.-3

Binary-Decision-Diagram Quantum Circuits Based on Schottky Wrap Gate Control of GaAs Honeycomb Nanowires: *Seiya Kasai¹; Hideki Hasegawa¹; ¹Hokkaido University, Research Center for Interface Quantum Electronics and Graduate School of Electronics and Information Engineering, N-13, W-8, Kita-ku, Sapporo 060-8628 Japan*

3:10 PM, V.A.-4

Single Electron Transistors with Sidewall Depletion Gates on a Silicon-On-Insulator Quantum Wire: *D. H. Kim¹; K. R. Kim¹; S.-K. Sung¹; B. H. Choi^{2,3}; S. W. Hwang^{2,3}; D. Ahn²; J. D. Lee¹; B.-G. Park¹; ¹Seoul National University, Inter-University Semiconductor Research Center (ISRC) and School of Electrical Engineering, San 56-1, Shinlim-dong, Kwanak-gu, Seoul 151-742, Korea; ²University of Seoul, Institute of Quantum Information Processing and Systems (iQUIPS), Seoul 130-743, Korea; ³Korea University, School of Electrical Engineering, Anamdong, Sungbukku, Seoul 136-701 Korea*

3:30 PM Break

3:50 PM, V.A.-5

A Semiconductor GMR Device: *Kanji Yoh¹; T. Doi¹; Y. Katano¹; S. Abe²; H. Ohno²; K. Sueoka²; K. Mukasa²; ¹Hokkaido University, Research Center for Interface Quantum Electronics, N 13, W8, Kita-ku, Sapporo, Hokkaido 060-8628 Japan; ²Hokkaido University, Graduate School of Electronics and Information Technology, N 13, W8, Kita-ku, Sapporo, Hokkaido 060-8628 Japan*

4:10 PM, V.A.-6

Digital Thin Film Non-Volatile Optical Memory: *Robert C. J. Chi¹; A. J. Steckl¹; ¹University of Cincinnati, Nanoelectronics Laboratory, Cincinnati, OH 45221-0030 USA*

4:30 PM, V.A.-7

Modeling and Design Study of Nanocrystal Memory Devices: *Min-She¹; Ya-Chin King²; Tsu-Jae King¹; Chenming Hu¹; ¹University of California at Berkeley, Department of Electrical Engineering and Computer Sciences, Berkeley, CA 94720 USA; ²National Tsing-Hua University, Department of Electrical Engineering, Hsinchu, Taiwan*

4:50 PM, V.A.-8

Quasi-Magnetic Fields Revisited: Second-Order Transport Effects in Graded Semiconductors: *William R. Frensley¹; ¹University of Texas at Dallas, Richardson, TX 75083 USA*

Tunable two-electron spin states in quantum dot structures and the applicability for making spin qubits

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and L.P. Kouwenhoven⁴

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The electronic configuration in a quantum dot is determined in such a way as to minimize the total energy associated with the quantum mechanical and interaction effects. The spin state thus determined, usually takes a total spin, $S = 0$, when the number of electrons in the dot, N , is even, and $S = 1/2$ for odd N . S can be greater than $1/2$ when the spin-related interaction is strong. The spin configuration is then tunable with various parameters such as number of electrons, strength of confinement and magnetic field, and this provides a good potential for applications to quantum computing and spintronics.

Electron spin is a most natural candidate for the spin-qubit since every spin $1/2$ encodes exactly one qubit. It is theoretically shown that the spin qubit located in quantum-confined systems satisfies all requirements necessary for a scalable quantum computer [1]. According to the Loss-DiVincenzo scheme [1], a double quantum dot structure operates as a two-level system consisting of a spin singlet and triplet. The singlet and triplet are made out of two-electrons, and the exchange interaction between the spins is controlled by gate electrodes to produce the fundamental quantum XOR operation [2]. On the other hand, experimentally there are still technical difficulties in preparing well defined two-electron states in quantum dot structures. We have recently fabricated single and double quantum dot structures with a tunable number of electrons, starting from $N = 0$, and identified the two-electron spin states. In this paper we review the experiments conducted to characterize the electronic properties of the two-electron spin states, such as the tunability of singlet and triplet states, the time scale for spin relaxation, and the modulation of exchange coupling, which are vital for making spin qubits.

We prepare a single dot with a circular, disk-shape, and a double dot structure by vertically stacking two disk-shaped dots (Fig. 1). For the single dot, we show that the configuration, which is either a singlet or a triplet, is tunable as a function of magnetic field (B -field) and gate voltage. We use a pulsed gating technique [3] to measure the spin-flip relaxation time from the excited to the ground state. For a double dot structure, we focus on the singlet-triplet splitting associated with the lowest bonding and antibonding states. We use a B -field to modulate the exchange coupling between the two spins [4].

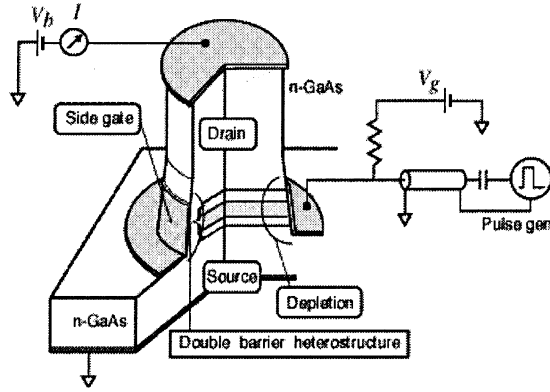


Fig.1 Device configuration for a single quantum dot and the set-up for a pulsed gating measurement. The double barrier structure consists of a 12-nm $\text{In}_{0.05}\text{Ga}_{0.95}\text{As}$ as well as two (7.5- and 9-nm) $\text{Al}_{0.22}\text{Ga}_{0.78}\text{As}$ barriers.

Tunable spin singlet and triplet states in a single quantum dot

Our quantum dot is located in a cylindrical mesa of a resonant tunneling double barrier structure with a Schottky gate on the side of the mesa (Fig.1) [5]. The electrons in the dot are strongly confined by the heterostructure barriers in the vertical direction, and laterally confined by the 2D harmonic potential. This lateral confinement leads to sets of degenerate states consisting of orbitals of 1s, 2p, In the presence of a B -field perpendicular to the 2D plane of the dot the eigen states evolve like the Fock-Darwin (FD) states (Fig. 2). The orbital degeneracy at $B = 0$ T is lifted on initially increasing B . As B is increased further, new crossings or new degeneracies can occur. Near $B = 0$ T the two-electron ground state is a singlet having two antiparallel spins both in the 1s orbital, and the first excited state is a triplet having parallel spins in the 1s and 2p orbitals. As the B -field is increased, the ground state undergoes a transition from the singlet to triplet due to increased interactions (Fig. 2)[6]. The same singlet-triplet transition is observed for general two-electron filling at each crossing point in the Fock-Darwin diagram [7]. This indicates that a singlet-triplet transition can be manipulated by tuning the orbital degeneracy.

For quantum computing, it is essential to realize systems with a weak coupling to their environment, and therefore slow dephasing. A dephasing time over 100 nsec, which is much longer than the energy relaxation time, has previously been measured for n- GaAs bulk material, using a time-resolved Faraday rotation technique [8]. For our quantum dot, spin-orbit coupling and hyperfine coupling to nuclear spins in the host material are possible mechanisms to cause spin-flips of conducting electrons. Recent calculations [9] including spin-orbit coupling predict an unusually long spin-flip time, although the contribution of nuclear spins is not yet clear. The spin flip is assisted by electron-phonon scattering, which accompanies energy relaxation. We have studied the relaxation of a two-electron state from the excited (triplet) to the ground (singlet), using a pulsed gating technique (Fig.1). In this measurement, we have only obtained a lower bound of the relaxation time, which is 100 μsec . Note that what is measured is the energy relaxation time with a spin-flip. In contrast, in our previous experiment [3] on a planar quantum dot holding many electrons, the time of relaxation without a spin-flip is shorter than nsec, which

is due to the high electron-phonon scattering rate. So the unusually long relaxation time ($> 100 \mu\text{sec}$) obtained in the present measurement, indicates that the bottleneck in the relaxation is the slow spin-flip rate. Such a long spin relaxation time will be essential for integrating a large number of qubits ($> 10^4$) to implement realistic computation.

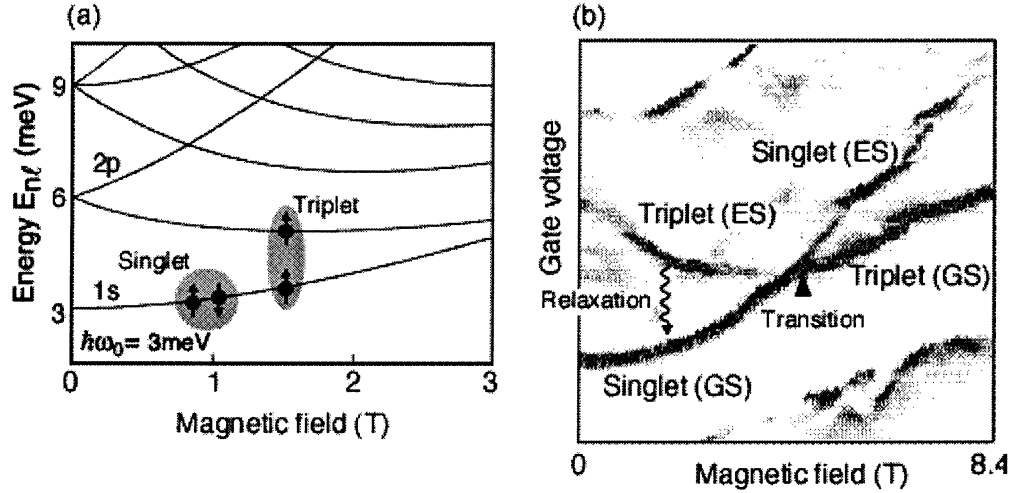


Fig.2 (a) Fock-Darwin diagram calculated for a 2D harmonic confinement whose characteristic energy $\hbar\omega_0 = 3 \text{ meV}$.

(b) Two-electron ground state (GS) and first excited state (ES) (dark lines) measured for a single dot. Relaxation from the first excited to the ground state for $B < 5 \text{ T}$ is accompanied by a spin-flip.

Tunability of a singlet and triplet states in a double quantum dot

In a double quantum dot a spin singlet and triplet state form the two levels where the exchange interaction between the spins is controlled by the gate electrodes. The exchange coupling, J , is given by $J = 4t^2/U - V(B)$, where t , U and V are the extended-hopping matrix element, on-site Coulomb repulsion and a B -field induced energy, respectively. J is equivalent to the singlet-triplet splitting, so in the absence of a B -field J is always positive, and independent of the coupling strength between two dots, indicating that a singlet is the ground state. J becomes negative as a function of B -field, leading to a transition in the ground state from a singlet to a triplet.

We use a triple barrier structure instead to a double barrier structure to fabricate a vertically coupled two-dot device, and study the influence of B -field on the exchange coupling. The vertical quantum mechanical coupling gives rise to a set of a bonding and an antibonding states (Fig. 3), each of which consists of 2D harmonic states confined by the common Schottky gate. The two-electron ground state is a singlet having antiparallel spins both in the bonding-1s orbital, and the excited state is a triplet

having parallel spins in the bonding-1s and antibonding-1s orbitals. We apply a B -field parallel to the 2D plane of the dot to modulate the exchange coupling, and observe a switching between the singlet and triplet state. In our vertical device we only use the B -field to modify the exchange coupling (t and V). On the other hand, in a lateral device we will be able to change the sign of the exchange coupling as a function of gate voltage under B -field. We discuss the necessary conditions for realistic quantum gate operation in both the vertical and lateral devices.

A double quantum dot is also a candidate for making spin injectors or filters. We have recently prepared a weakly coupled double quantum dot to demonstrate the operation of spin filtering. Associated with the spin-dependent transport through the two-electron ground state we have observed a spin diode like operation [10].

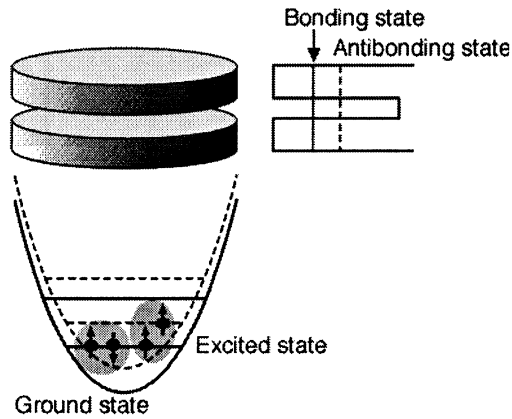


Fig.3 Configuration for a double quantum dot.

1. D. Loss and D.P. DiVincenzo, Phys. Rev. A **57**, 120 (1998).
2. A. Barenco et al., Phys. Rev. A **52**, 3457 (1995).
3. T. Fujisawa et al., Phys. Rev. B **63**, 81303 (2001).
4. G. Burkard et al., Phys. Rev. B **56**, 2070 (1999); M.N. Leuenberger and D. Loss, cond-mat/0010434.
5. D.G. Austing *et al.*, Japn. J. Appl. Phys. **34**, 1320 (1995); *ibid*, Semicond. Sci. Technol. **11**, 388 (1996).
6. L.P. Kouwenhoven et al., Science, **278**, 1788 (1997).
7. S. Tarucha et al., Phys. Rev. Lett. **77**, 3613 (1996); *ibid*, **84**, 2485 (2000).
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10. K. Ono et al., presented in ICPS25 (Osaka, 2000).

A Multiple-Valued SRAM with Combined Single-Electron and MOS Transistors

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We report here a new type of "single-electron" memory that works as a multiple-valued SRAM.

A schematic of the proposed memory is shown in Fig. 1. The source of a MOSFET with fixed gate bias V_{gg} is connected to the drain of a single-electron transistor (SET), and the SET drain voltage is kept nearly constant around $V_{gg}-V_{th}$, where V_{th} is the threshold voltage of the MOSFET. This $V_{gg}-V_{th}$ is set low enough to sustain the Coulomb-blockade condition. By connecting the SET gate to the MOSFET drain, the I_d-V_{gs} (3-terminal) characteristics of the SET are converted to the $I-V$ (2-terminal) characteristics of the combined SET-MOSFET circuit. With a proper choice of load device, the periodic nature of the $I-V$ characteristics results in a number of stability points, and this realizes the multiple-valued memory operation.

The SET is fabricated by pattern-dependent oxidation (PADOX) [*], in which a one-dimensional Si wire patterned in silicon on insulator (SOI) is converted into a small Si island with a small tunnel capacitor at each end. Figure 2 shows the I_d-V_{gs} characteristics of a SET. Periodic drain-current peaks are clearly seen along with an effect of tunnel resistance modulation by the gate voltage. From this figure and a Coulomb diamond plot, gate capacitance, source/drain capacitance, and tunnel resistance are calculated to be 0.3 aF, 2.7 aF, and 80~220 k Ω , respectively.

PADOX is highly compatible with CMOS fabrication process since the area other than one-dimensional Si wire can be used as an ordinary MOSFET channel. Figure 3 shows the I_d-V_{gs} characteristics of a MOSFET on the same SOI wafer. The effective channel width, length, and gate oxide thickness are 12 μm , 14 μm , and 90 nm, respectively. The requirements for the present application, such as small off-state leakage and steep subthreshold slope, are met by this MOSFET.

Figure 4 shows the $I-V$ characteristics of the combined SET-MOSFET circuit. The current increases and decreases periodically, reflecting the I_d-V_{gs} characteristics of the SET (Fig. 2). If a current source of 4.5 nA is connected to the circuit, stability points a~f should appear. Note that the number of stability points is infinite in principle, but is practically limited by the breakdown voltage of the MOSFET drain or SET gate and the deviation from the ideal SET characteristics.

The multiple-valued memory operation was verified by current sweep measurements. If the current starts from stability point a and increases, the voltage jumps up when the current exceeds the second peak in the $I-V$ characteristics (Fig. 4). If the current sweep is reversed at this moment, stability point b can be reached. Other stability points, c~e, can also be reached by choosing higher current-sweep reversal points. Note that stability point f cannot be attained by this current-mode operation, because the last peak in the $I-V$ characteristics (Fig. 4) is lower than the previous one.

Figure 6 proposes a four-transistor memory cell for large-scale applications. A depletion-mode grounded-gate MOSFET M1 is used to sustain the SET drain voltage around the absolute threshold voltage of M1. Another depletion-mode MOSFET, M2, with its gate and source shorted serves as a current source, and pass-transistor M3 controls the access to the cell. In write operation, the voltage applied to BL is transferred through M3, and is quantized to a stability point after M3 is cut off. It should be noted that any stability point can be directly reached by this voltage-mode operation.

In summary, we have devised a novel multiple-valued SRAM comprised of a SET and a MOSFET, and the basic operation is verified with devices fabricated on the same SOI wafer. The result opens up the possibility of dramatically increasing the memory density of future scaled-down CMOS.

[*] Y. Takahashi et al., IEEE Trans. Electron Devices, Vol. 43, pp. 1213-1217, 1996.

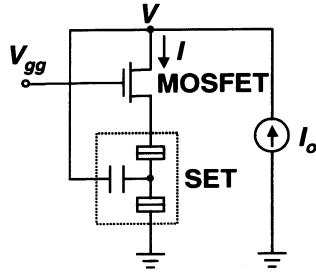


Fig. 1 The proposed multiple-valued static memory comprised of a SET, a MOSFET and a constant-current source I_o . By connecting the SET gate to the MOSFET drain, the I_d - V_{gs} (3-terminal) characteristics of the SET are converted to the I - V (2-terminal) characteristics.

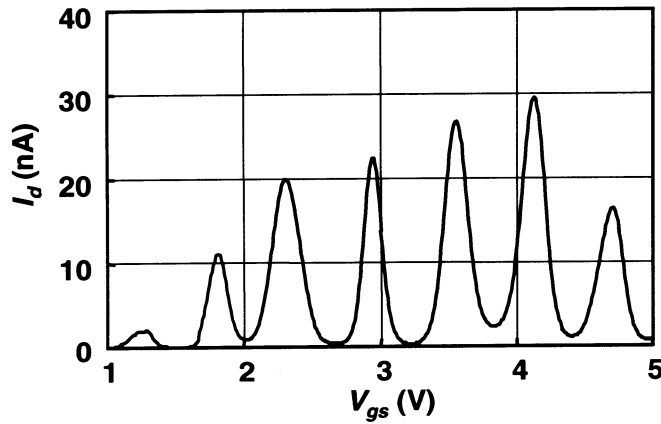


Fig. 2 I_d - V_{gs} (3-terminal) characteristics of a SET fabricated by PADOX, measured at 27 K and 10 mV of V_{ds} .

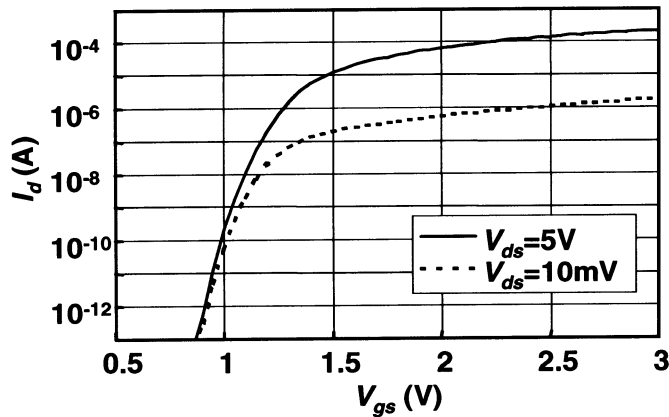


Fig. 3 I_d - V_{gs} (3-terminal) characteristics of a MOSFET fabricated on the same SOI wafer for the above SET, measured at 27 K.

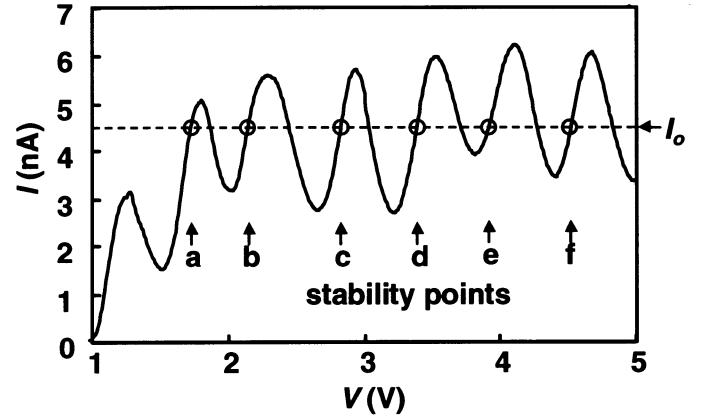


Fig. 4 I - V (2-terminal) characteristics of the proposed circuit measured at 1.08 V of V_{gg} . Stability points (a~f) expected for the current load of 4.5 nA are also shown.

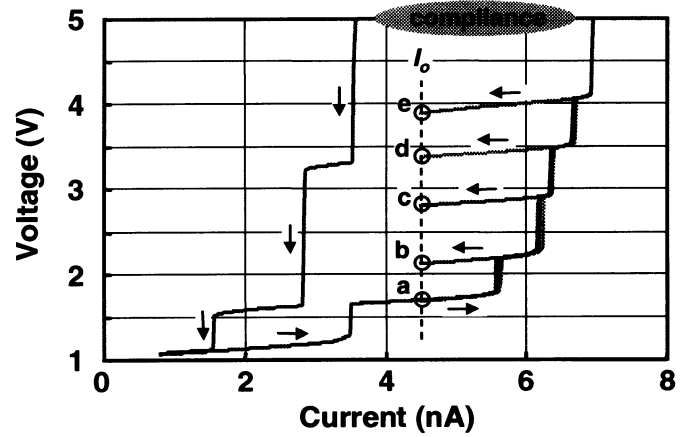


Fig. 5 Current sweep measurements of the proposed circuit. The compliance of the current source is 5 V.

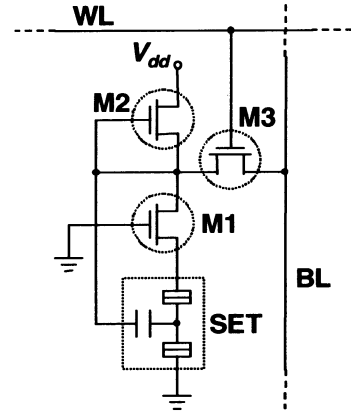


Fig. 6 A multiple-valued "single-electron" SRAM cell with two depletion-mode MOSFETs (M1 and M2) and one enhancement-mode MOSFET (M3).

BINARY-DECISION-DIAGRAM QUANTUM CIRCUITS BASED ON SCHOTTKY WRAP GATE CONTROL OF GaAs HONEYCOMB NANOWIRES

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Rapid progress of the network-dominated information society demands creation of nanoelectronics beyond the Si C-MOS scaling limit. Rapid penetration of nano-technology into areas of chemistry and biology also requires nanoelectronics as the workhorse for sensing, information processing and control. However, in spite of research over 25 years, no realistic prospect for high-density integration of quantum devices seems to exist.

This paper proposes and investigates a novel realistic approach for quantum integrated circuits which implements a binary-decision-diagram (BDD) logic architecture[1] by a quantum device architecture based on Schottky wrap gate (WPG) control of GaAs honeycomb nanowire arrays. The WPG structure shown in **Fig.1** has features of tight gate control, strong electron confinement, device design flexibility and a simple lateral structure suitable for planar integration.

In the BDD architecture, a logic function is realized by connecting many node devices as shown in **Fig.2(a)**. The function of the node device is to switch the path of the signal messenger such as a single electron or a few electrons into 0- or 1-branch depending on input as shown in **Fig.2(b)**. Here, no output-to-input connection is required in contrast to the conventional logic gate architecture. Thus, no large voltage gain, no precise input-output voltage matching, no large fan-in and fan-out numbers, and no large current drivability are required. It is a good architecture for quantum devices operating near the quantum limit of delay-power product. For hardware implementation, we note the basic three-fold branch symmetry of the node device and propose a device architecture based on Schottky WPG control of honeycomb nanowire arrays.

Various types of WPG BDD node devices using quantum wire transistors (QWRTrs) and single electron transistors (SETs) are shown in **Fig.3**. Previously, we demonstrated a successful operation of a 3-WPG single electron node device shown in **Fig.3(a)**. [2] However, small and uniform dot sizes are difficult to realize with this device. Thus, new node devices shown in **Figs.3(b)** and **(c)**, having one QWRTr or one SET on each of the exit branch, respectively, were fabricated as shown in **Fig.4**. Each branch of the node device showed clear conductance quantization and oscillations as shown in **Fig.5**. With these, clear path switching characteristics were obtained.

To investigate the feasibility of integration, a two-bit adder using the device in **Fig.3(c)** was designed and fabricated. Careful design efforts led to a honeycomb layout design without wire cross-over as shown in **Fig.6**. **Figure 7** shows the fabricated quantum WPG BDD 2-bit adder. In spite of large feature sizes, high-density integration over 10^6 node devices/cm² has been already achieved. The result of a probe-test done by picking up a "OR logic function block" on the chip is shown in **Fig.8**. It showed clear correct operation. Correct operation was seen at least up to 120 K by bias adjustments. This is because the circuit shows gradual transitions with temperature increase from the single electron quantum regime to a few electron quantum regime, and finally to the many electron classical regime. Full function test is being done, and will be presented. Wire size reduction should lead to room temperature operation in the single electron quantum regime.

[1] N.Asahi, M.Akazawa and Y.Amemiya, IEEE Trans. Electron Devices **42** (1995) 1999.

[2] S.Kasai, Y.Amemiya and H.Hasegawa, Tech. Dig. 2000 IEDM (2000) 585.

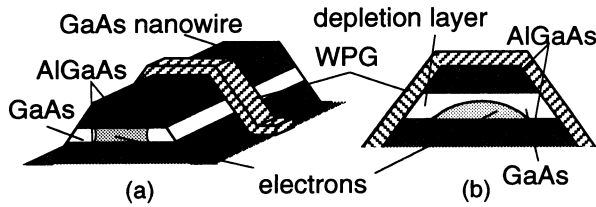


Fig.1 Schottky WPG structure.

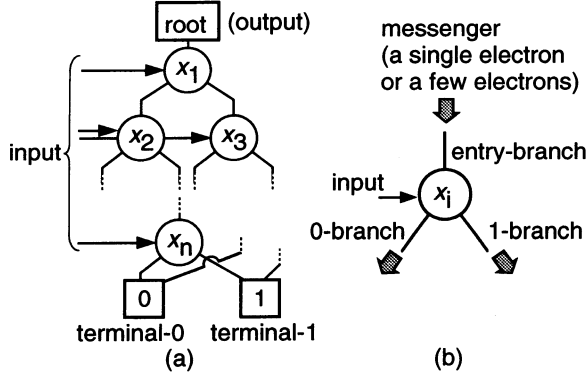


Fig.2 (a) BDD logic architecture and (b) BDD node device.

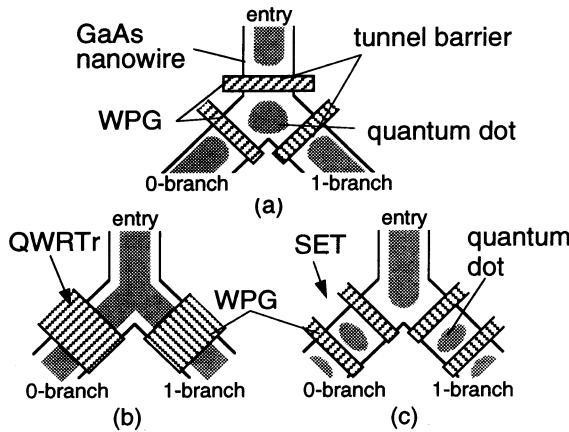


Fig.3 WPG quantum BDD node devices with (a) 3-WPGs with a QD, (b) QWRTrs and (c) WPG SETs.

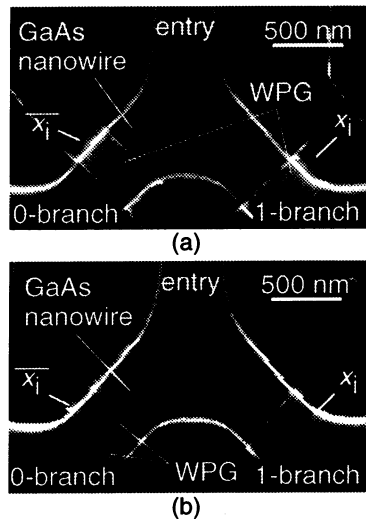


Fig.4 (a) WPG QWRTr- and (b) SET-based BDD node devices.

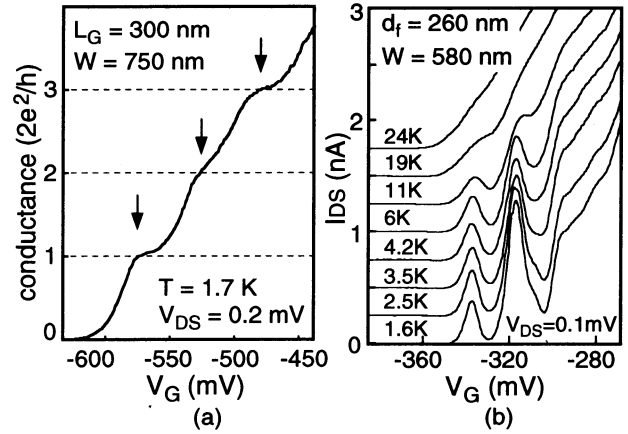


Fig.5 Conductance characteristics of exit branches in (a) WPG QWRTr- (b) SET-based BDD node devices.

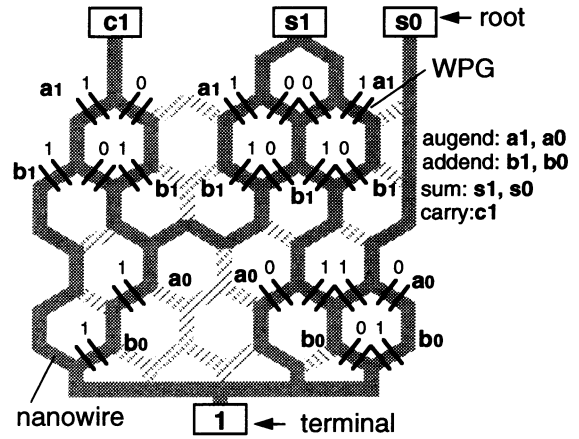


Fig.6 Circuit diagram of a BDD 2-bit adder.

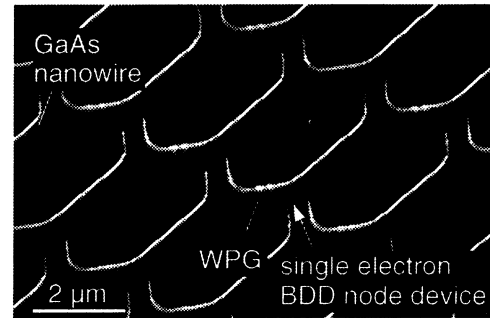


Fig.7 Fabricated WPG quantum BDD 2-bit adder.

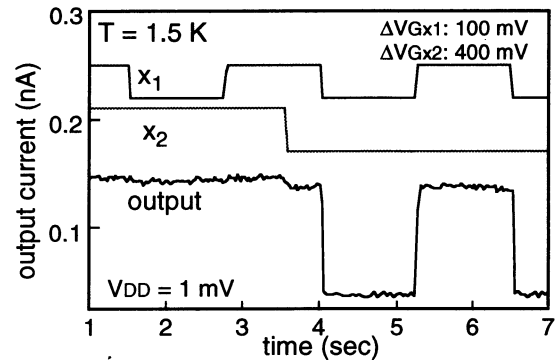


Fig.8 Input/output waveform of WPG BDD OR logic function block.

Single Electron Transistors with Sidewall Depletion Gates on a Silicon-On-Insulator Quantum Wire

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For practical application to multi-functional nanoelectronic devices, single electron transistors (SETs) should have controllable and reproducible characteristics. For high temperature operation, recently proposed SET structures have depended on somewhat contingent phenomena such as unintentional potential barriers in quantum wires [1], e-beam irregularity [2] or randomly distributed nanocrystal arrays [3], so that their device characteristics couldn't be predicted. In this work, SETs with sidewall depletion gates on a silicon-on-insulator (SOI) quantum wire have been fabricated by the combination of conventional lithography and VLSI technology, and their properties were investigated.

Figure 1 shows a schematic of the fabricated device. Inversion layer in a p-type 45nm-thick SOI quantum wire channel is formed by the back gate bias (V_{BG}), and two tunnel junctions are formed by the sidewall depletion gate bias (V_{SG}). The charge of electrically formed quantum dot is controlled by the control gate bias (V_{CG}). A uniform 30 nm-wide SOI quantum wire was formed by sidewall patterning method [4] as shown in Fig. 2(a), which effectively suppressed unintentional potential barriers. Figure 2(b) and 2(c) show the n-type doped polycrystalline silicon sidewall gates on Si wire, which were formed by the sequential LPCVD and the reactive ion etching of polycrystalline silicon on nitride groove. The separation between two sidewall gates (S_{SG}) was designed to be 37 nm (SET1) and 185 nm (SET2), for the high temperature operation and high voltage gain, respectively. Sidewall depletion gate structure has the merit in that it can implement a feature size smaller than the limit of e-beam lithography [5].

Figure 3 shows the control gate dependence of the drain current and the differential conductance of SET1 at 77 K. Clear multiple Coulomb oscillation peaks are obtained with the period (ΔV_{CG}) of 600 mV. This characteristic is superior to the recently published Si based high temperature SETs [2, 6] in that many peaks are observed at 77K, and I_{ON}/I_{OFF} value is maintained as the control gate voltage increases. Gate capacitance of 0.27 aF extracted from ΔV_{CG} is consistent with that of 0.24 aF estimated from the device geometry. Moreover, ΔV_{CG} is constant as V_{CG} increases. These characteristics stem from the strong controllability of tunnel barriers by V_{SG} , which can be attributed to the 3-dimensional structure of the sidewall depletion gate wrapping Si channel. This is confirmed by 3-dimensional device simulation, as shown in Fig. 4. The size of electrostatically defined quantum dot is invariant in sweeping V_{CG} . Considering that, in many cases of previous reports, electrically formed quantum dots were too sensitive to gate bias conditions to maintain the reliable multiple switching performance and showed just a small number of peaks only in a subthreshold region [5, 7], the fabricated SETs are much improved and comparable to SETs by physically formed quantum dot [6]. Figure 5 shows the drain voltage dependence of the drain current of SET1 at 77 K. Coulomb gap is clear and modulated by V_{CG} . Maximum gap was about 20mV. This suggests an extremely low voltage gain, because quantum dot is weakly coupled to the control gate.

In the case of SET2 with S_{SG} of 185 nm, the area of quantum dot increases, so that the control gate capacitance and the voltage gain increase. Figure 6 shows the drain current contour of SET2 at 15 K. Clear rhombus shape and high voltage gain of 1.3 are observed. Extracted capacitances are: control gate capacitance (C_{CG})=2.13 aF, drain junction capacitance (C_D)=1.64 aF, source junction capacitance (C_S)=1.42 aF, and total capacitance (C_T)=8 aF.

In summary, reliable operation of Si based SETs fabricated by conventional VLSI technology was successfully demonstrated at 77K. Improving the performance of the suggested SETs will make the designable and reproducible high temperature SETs possible.

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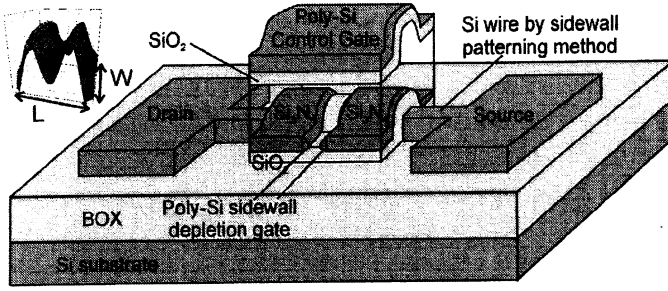


FIG. 1. Schematic diagram of the fabricated SET. Starting material was a 45nm thick SOI film. The inset shows the electron potential profile in SOI wire calculated by 3-dimensional device simulation.

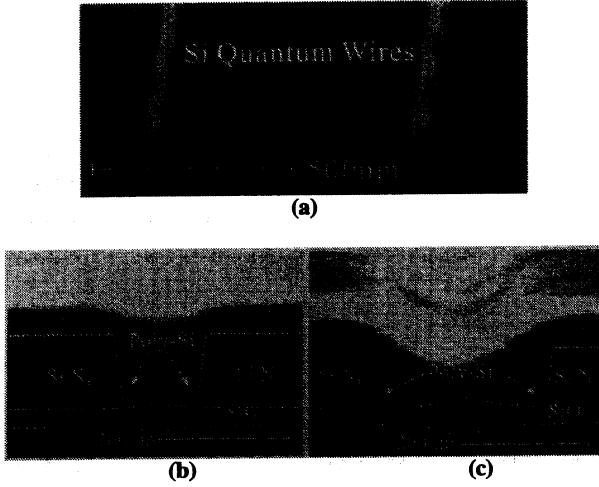


FIG. 2. (a) SEM image of Si wire formed by sidewall patterning method after the gate oxidation. Final line width was 23 nm. (b) SEM image of polycrystalline silicon sidewall depletion gates of SET1 ($S_{SG}=37$ nm). (c) SEM image of polycrystalline silicon sidewall depletion gates of SET2 ($S_{SG}=185$ nm).

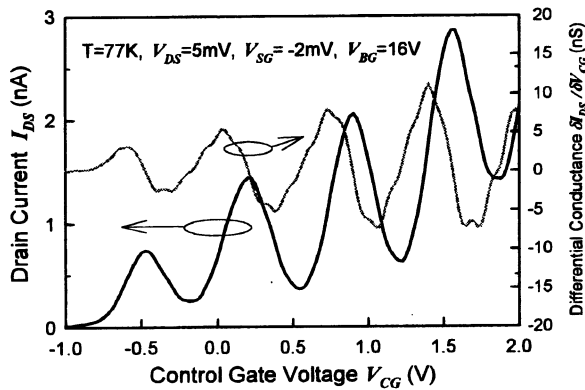


FIG. 3. Control gate dependence of the drain current and the differential conductance of SET1 at 77 K. Multiple Coulomb oscillation peaks are clearly observed. Oscillation period (ΔV_{CG}) is 600mV, which corresponds to the control gate capacitance (C_{CG}) of 0.27 aF. ΔV_{CG} is constant as V_{CG} increases.

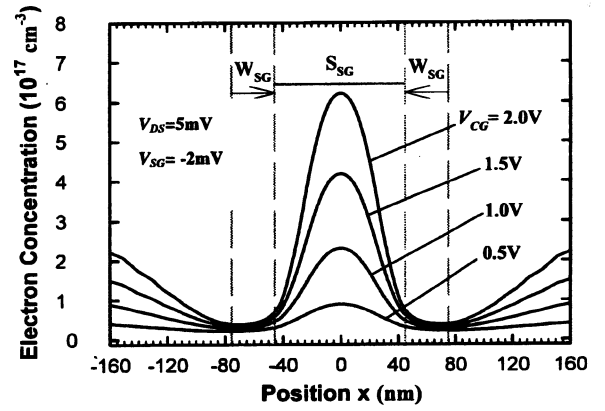


FIG. 4. Electron concentration along an SOI wire length direction at 7nm depth beneath Si/SiO₂ interface. Poisson equation is solved by 3-dimensional device simulator.

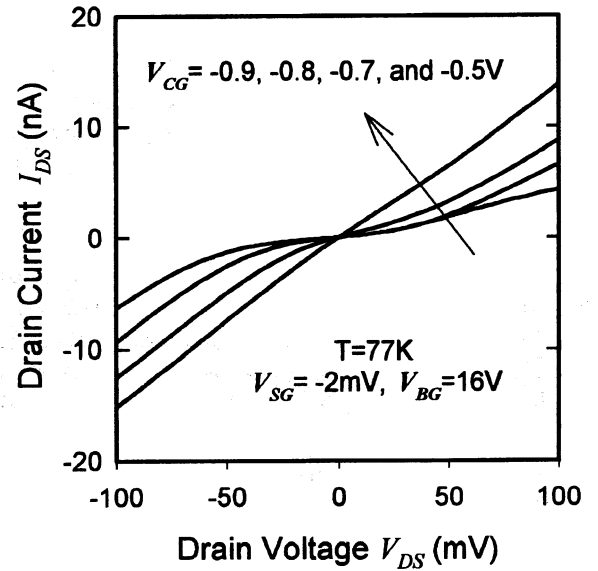


FIG. 5. Drain voltage dependence of the drain current of SET1 at 77 K. Coulomb gap is clear and modulated by V_{CG} .

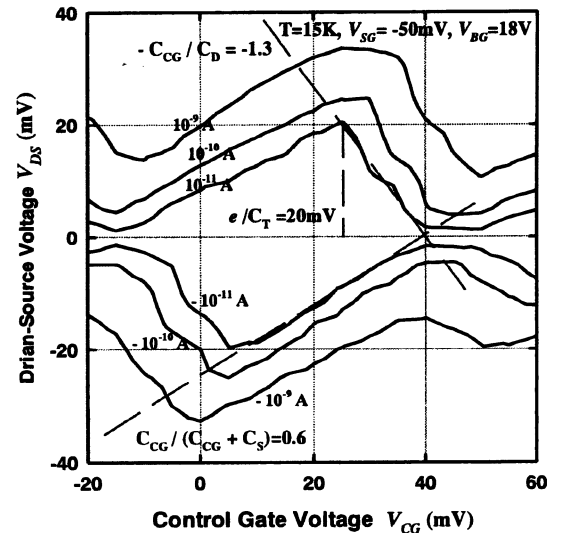


FIG. 6. Contour plot of drain current as a function of control gate voltage (V_{CG}) and drain voltage (V_{DS}) of SET2 at 15 K. The voltage gain of 1.3 is obtained.

A Semiconductor GMR Device

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We propose and report on a narrow-gap semiconductor interband-tunneling device whose magnetoresistance varies more than five orders of magnitude at 2K. The operational principle of the novel GMR device is based upon the magnetic field modulation of the tunnel barrier thickness thereby changing the tunnel resistance of the new version of "Esaki diode" characteristics. The depletion layer thickness, i.e., tunnel barrier thickness, is determined by the difference between the bottom of the Landau level and the Fermi level of the collector (p-InAs). The metallic GMR device[1] which utilizes spin scattering properties[2] exhibits resistance variation of 10 - 50 %, whereas the present semiconductor GMR device was found to exhibit a wide range of resistance ratio of over 10^5 .

The structure consists of p^+ -InAs substrate, $1\mu\text{m}$ of p^- -InAs layer, $500\text{\AA}$ of undoped InAs, and $80\text{\AA}$ of InAlAs barrier layer. Ti/Au electrode is deposited on top of the InAlAs barrier and the AuZn alloy is used as a contact metal to the bottom of the device. Lateral size of the top electrode is $20\mu\text{m}$ square. Thus, the quantum "Esaki diode" consists of surface inversion layer, lightly doped p-depletion layer, p- charge neutral layer and p^+ substrate. The p- charge neutral layer is the most sensitive layer to the external magnetic field in the present device structure. The Fermi level at 2K is only 1.9meV and the bottom of the Landau level can easily exceed the Fermi level as the magnetic field (perpendicular to the surface) exceeds 1T in the present doping condition. Unlike conventional Esaki diode, the emitter is not n-type semiconductor, but 2DEG surface inversion layer[3] induced in nominally undoped region. The critical field can be designed by appropriate heterostructure design. The advantages of the present structure include (i) extremely wide range of terminal resistance (200Ω @0T to $200\text{M}\Omega$ @7T), (ii) simple and solid two terminal device structure. Disadvantages are related with its operating conditions : (i) high magnetic field ($B > 1\text{T}$) and (ii) low temperature ($\approx 2\text{K}$). Optimization of the heterostructures may well increase the operational temperature range to higher temperature and magnetic field range to lower fields. However, the novel operating principle of the present semiconductor-based GMR device may provide an opportunity to develop a variety of useful applications in the integrated sensors.

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Correspondence: yoh@rciqe.hokudai.ac.jp

InAlAs	80Å
InAs	500Å
p-InAs	1μm ($1 \times 10^{17} \text{cm}^{-3}$)
p ⁺ -InAs	sub strate

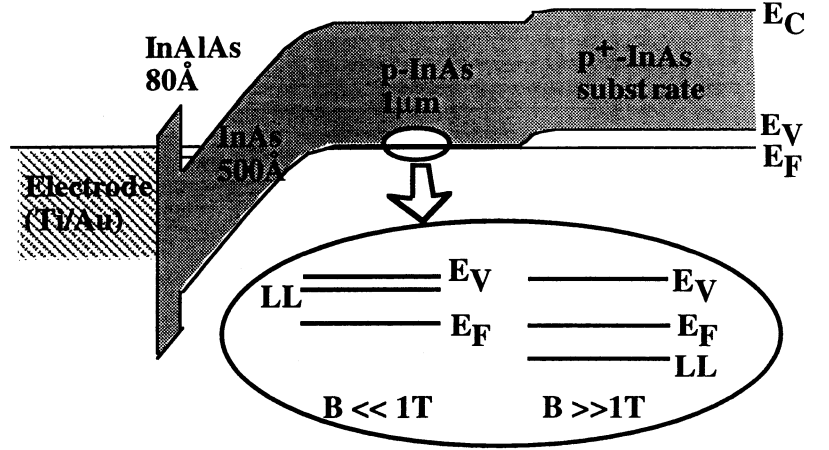


Fig.1 Heterostructure of the device

Fig.2 Energyband diagram

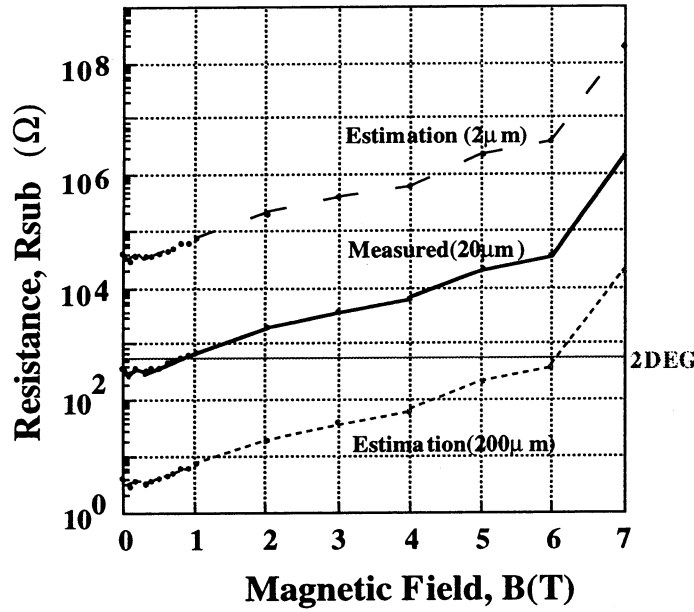


Fig.3 Two terminal resistance (surface-to - substrate) dependence on external magnetic field perpendicular to surface.

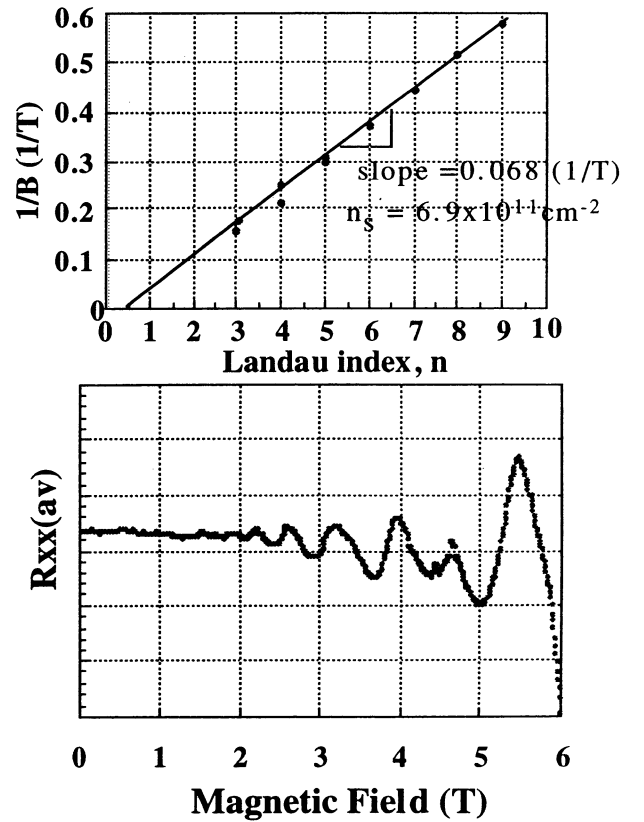


Fig.4 Shubnikov de Haas oscillation of the surface inversion layer.

Digital Thin Film Non-Volatile Optical Memory

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Abstract

Optical memory devices are conventionally fabricated by laser beam processing. In this paper, we report on the use of a Ga^+ focused ion beam to “write” data on a SiO_2 film grown on Si. The use of FIB milling has the advantage of creating smaller data storage elements and higher data density (than current DVD devices) since the ion beam can be focused into a much smaller spot size (as small as 8nm in diameter) than that of lasers. The FIB-written data has a sub-micron structure with multiple bit capacity per physical location and can be read by far-field optical detection. The extended lifetime of data stored on a robust material such as SiO_2/Si produces a data storage option with excellent survival under harsh environment such as high temperature, radiation, etc.

This promising optical memory device utilizes a novel concept of dielectric digital thin-film (DTF) interference. The “write” process is performed by 30kV Ga^+ FIB milling with 1nA beam current. The conversion from electronic data to FIB pixel pattern is generated by a software program created in LabVIEW. FIB milling is capable of creating different depth levels with step height of 50nm or smaller. The “read” process uses vertical optical interference established locally by the remaining SiO_2 layer thickness. This interference effect creates distinguishable color pixels that can be decoded. As an example, optical ROM devices with 16 different colors (equivalent to 4 bits per memory pixel) have been fabricated using the DTF structures on a 800 nm SiO_2 thin film. Depending on the need of different applications, the pixel size can be as large as several microns or as small as several tens of nanometer. A memory device with pixel pitch of 700nm (for far-field optical detection) has been fabricated to display 16 different colors. These devices contain a bit density of 5 Gbit/in² which is roughly double the current storage density of a DVD. We have also fabricated DTF devices with 256 milling levels, equivalent of 8 bits per memory pixel, on the 800nm SiO_2 film. We estimate that the DTF color optical memory devices have the potential of reaching 2 Terabits per square inch, providing that near-field optical detection techniques are utilized. This huge density potential and the durability of the DTF structure have created a very attractive new approach for optical data storage devices.

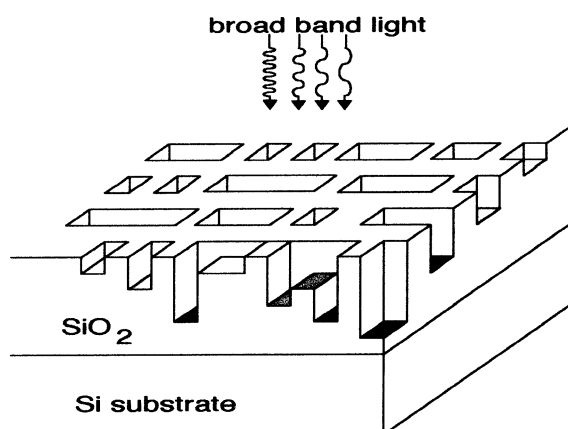


Fig. 1 Schematic diagram for the DTF memory device structure.

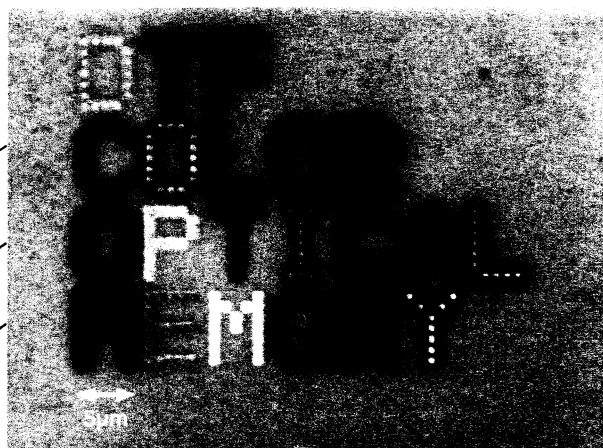


Fig. 2 Optical image of a pixel array with distinct colors created by FIB milling in SiO_2/Si layer.

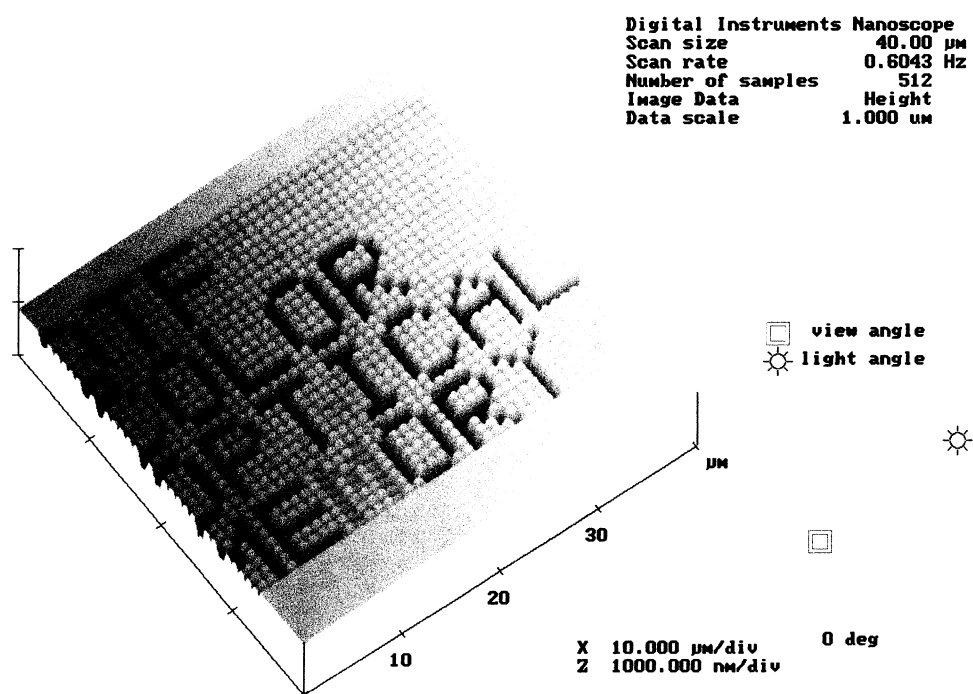


Fig. 3 AFM image of a high density array of data pixels in SiO_2/Si layer. Pixel pitch is $0.7\mu\text{m}$.

Modeling and Design Study of Nanocrystal Memory Devices

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I. Introduction

Semiconductor memory for the future demand high density/low cost and low power consumption cell design. Compared with DRAM, flash memory with floating gate structure consume less power and they can also achieve much high array density. However, the tunnel oxide must be less than 25Å in order to achieve 100 ns write/erase time for a reasonable programming voltage (<10 V) [1]. Unfortunately, the retention time of a floating-gate device with 20Å tunnel oxide is less than 1ms, as shown in Fig. 1.

To achieve a better retention/programming time ratio, semiconductor memory with nanocrystal embedded in the gate dielectric was proposed [2,3,4]. Although nanocrystal memory device has been experimentally investigated, no theory is available to guide its design or to predict its performance limits, especially the nanocrystal size scaling limit.

In this paper, the write/erase and retention time of semiconductor nanocrystal memory devices at room temperature are modeled using single-charge tunneling theory with quantum confinement and Coulomb blockade effects [5]. The impact of nanocrystal size and tunnel-oxide thickness are studied, and the suitability of nanocrystal memory devices for nonvolatile memory and DRAM applications is discussed.

II. Device Modeling

The nanocrystal memory device structure is shown in Fig.2 with the writing/erasing process. The control oxide thickness is fixed at 50Å. The tunneling current density during writing/erasing process can be expressed by the

Golden Rule:
$$J = \frac{2e}{\hbar} \int_0^{\infty} T(E) \eta_s(E) \eta_d(E) [f_s(E) - f_d(E)] dE \quad (1)$$

Here, $T(E)$ is the tunneling probability between energy levels across the tunnel oxide, η_s and η_d are the densities of states in the substrate (channel) and in a nanocrystal, respectively. f is the electron distribution function. The tunneling probability is calculated using the WKB approximation. When one electron is stored in the nanocrystal, the system energy will be raised by the electrostatic charging energy $e^2/2C$, where C is the nanocrystal capacitance. The quantum confinement energy becomes significant when the nanocrystal size shrinks to the nanometer range, which causes the conduction band in the nanocrystal to shift to higher energy [6]. Ge nanocrystal is studied here.

The conduction band shift for 5, 3, 2 nm nanocrystal is taken as 0.15, 0.5 and 1 eV respectively [7]. During retention, the electrons inside the nanocrystal can't be stored in the conduction band. Since the conduction band edge inside the nanocrystal is higher than that of substrate, electrons will tunnel back to the channel very easily. This is not consistent with the long retention time observed in the published experimental data [2,4]. Generally there are a lot of deep trap states in the nanocrystal such as P_b center[8], where the trap energy level is always 0.3 eV below the conduction band which is already shifted upward. Since electron wavefunction in the trap states is localized so the tunneling between channel and traps during write/erase is neglected. After electron is injected into the nanocrystal it will fall into the trap states through scattering mechanism. During erase, electrons will be de-trapped to the conduction band thermally and then tunnel back to the channel.

III. Results and Discussion

Fig. 3 shows the write/erase (W/E) time as a function of gate voltage for various tunnel-oxide thicknesses d , for 3 nm-diameter spherical nanocrystals. The retention reaches 10 years around $d=30\text{\AA}$ while achieving μs W/E time at 10V and ms W/E time at 6V. Fig. 4 shows that the retention time can be adjusted over a wide range by changing the tunnel-oxide thickness, to achieve quasi-nonvolatile memory operation with a tradeoff between programming speed and voltage. The nanocrystal memory device can achieve at least 10^6 times long retention time than floating-gate memory, for a given programming speed. It is consistent with experimental observation published.

The impact of nanocrystal dot size D on device performance is shown in Fig. 5. Larger D favors electron charging due to larger tunneling probability and less quantum confinement/Coulomb-charging effects. Quantum confinement effects dominate for D smaller than 5 nm. Fig. 5a shows that it is difficult to obtain 10 ns write time at low voltage (3V), no matter what the nanocrystal diameter is. The quantum confinement effect in 2 nm nanocrystals is very strong so that the retention time is lower and write time is longer. Fig. 5b shows that 10 ns write/erase times can be achieved with 10Å tunnel oxide, but then the refresh time would not be much longer than that of DRAM. Larger programming voltages (e.g. 10 V) can be used to improve write/erase speed, of course.

IV. Conclusion

The nanocrystal memory device would seem to work better as a flash-EEPROM memory device as opposed to a DRAM device. Nanocrystal size around 5nm is preferred to achieve fast programming speed and longer retention time and the size should not be scaled below that. Nanocrystal memory devices can provide 10^6 times larger retention-time to write-time ratio than conventional floating-gate devices.

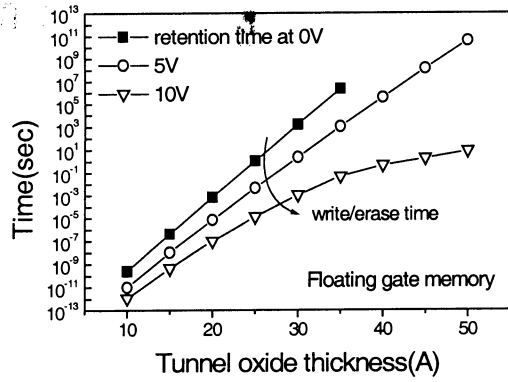


Figure 1: Retention and write/ erase time versus various tunnel oxide thickness at various gate voltage with conventional floating gate memory.

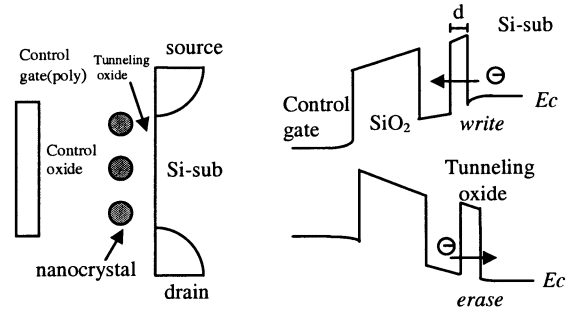


Figure 2: nanocrystal memory device structure and Illustration of write/erase process on/off the nanocrystal.

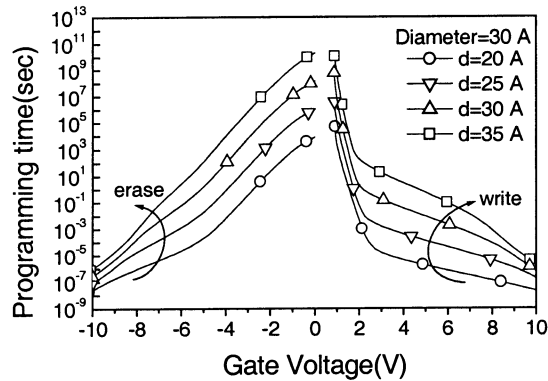


Figure 3: As a nonvolatile memory, nano-trap device can achieve 10 years retention and μ s write and erase time. The retention time can be extracted at zero gate bias during erase.

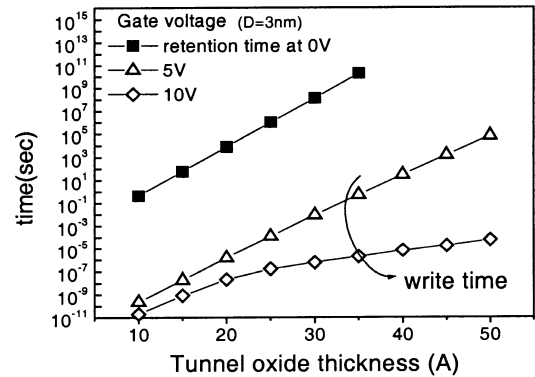
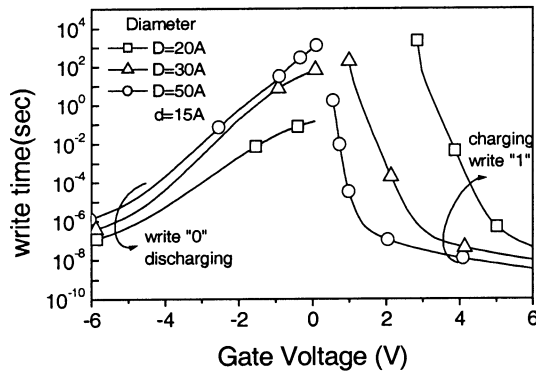
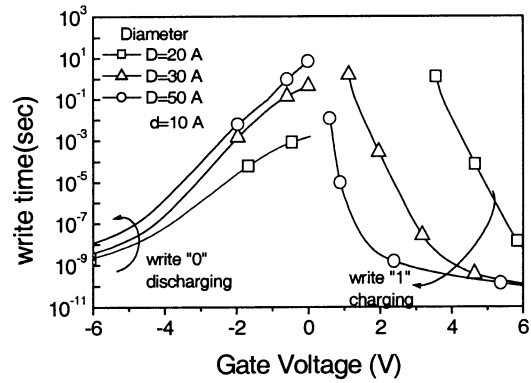


Figure 4: At least 10^6 longer retention time can be obtained with nano-trap than floating-gate at the same W/E speed.



(a)



(b)

Figure 5: Dependence of write and erase characteristics on nanocrystal size. The tunnel oxide is fixed at (a) 15 Å, DRAM writing time (~ 10 ns) can not be obtained at low voltage (b) 10 Å, the refreshing time (intercept of write "1" and write "0") is not impressive.

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Quasi-Magnetic Fields Revisited: Second-Order Transport Effects in Graded Semiconductors

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Richardson, Texas, 75083, USA

When Kroemer¹ introduced the concept of quasi-electric fields to describe the effects of graded semiconductors on carrier transport, he also discussed a “quasi-magnetic field” effect which occurs if the energy-band minimum shifts within the Brillouin zone as the alloy composition is varied. As heterostructure technology has developed in the subsequent forty years, such behavior of the energy-band structure has not been observed, and the quasi-magnetic field concept has largely been forgotten.

However, a careful rederivation of the heterostructure drift-diffusion equation from the Boltzmann transport equation reveals another quasi-magnetic field effect in the second order. Using a simple relaxation-time approximation, we find that the electron particle current density is given by

$$\mathbf{j}_n + \tau n \frac{d\mathbf{v}}{dt} = -D_n N_c \nabla \left(\frac{n}{N_c} \right) - \mu_n n (\mathcal{E} + \nabla E_c / q) - \frac{\mu_n n}{2q} \mathbf{v} \times \mathbf{v} \times \nabla m^*,$$

where $\mathbf{v}$ is the drift velocity. The effect of the last term is similar to that of a magnetic field proportional to $\mathbf{v} \times \nabla m^*$. Presuming that any effective-mass gradient would be in the epitaxial direction z , the effect would be largest for carrier drift parallel to the surface, let us say in the direction x . If the carrier motion in the z direction is confined, then an electric field will be developed to counteract motion in this direction, as happens with the Hall effect. (Call this the “quasi-Hall effect.”) The direction of the field will be such as to push the carriers toward the lower m^* region. The magnitude of this field will be

$$\mathcal{E}_z = \frac{v^2 \nabla m^*}{2q}$$

If m^* changes by $0.1 m_0$ in 100 nm, and v is 10^6 cm/s, the magnitude of this field will be 300 V/cm, which would typically be detectable but not significant. For carrier velocities of 10^7 cm/s, the field would be 3×10^4 V/cm, which is more likely to cause significant effects in devices.

Of present device structures, only the graded-bandgap base heterojunction bipolar transistor is so configured as to demonstrate this quasi-magnetic field effect. Lateral currents flowing in the base will redistribute base majority carriers to produce a longitudinal electric field by the quasi-Hall effect. If the effective mass varies approximately in proportion to the band gap (as is true of the direct-gap semiconductors) the quasi-Hall field will oppose minority-carrier motion in the forward direction.

The identification of a transport effect which depends upon the gradient of m^* in semiconductor alloys suggests that the effective mass and its dependence on alloy composition would be a worthy subject of experimental investigation in the technologically important alloys.

¹H. Kroemer, “Quasi-Electric and Quasi-Magnetic Fields in Nonuniform Semiconductors,” *RCA Review* **18**, 332-42 (1957)

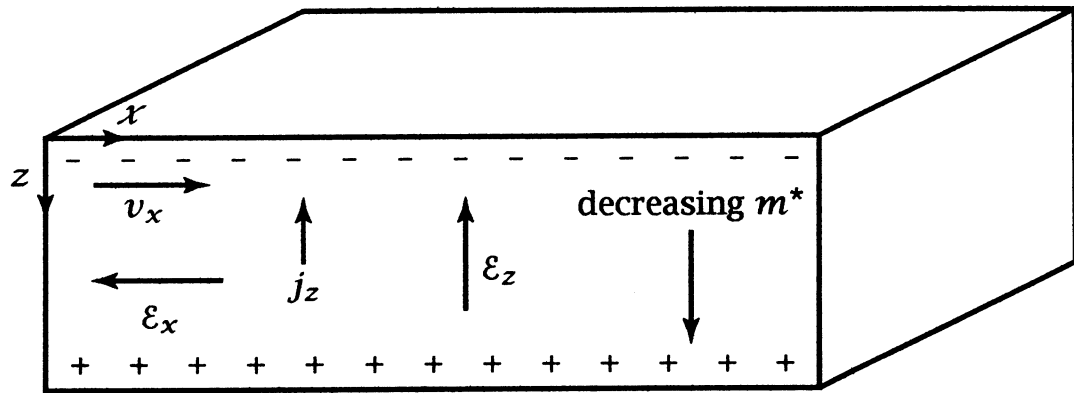


Figure 1: Geometry of the quasi-Hall effect in an n-type graded semiconductor layer.

Detectors

TUESDAY PM, JUNE 26TH, 2001

Session Organizer: Pallab Bhattacharya, University of Michigan

2:00 PM, V.B.-1 Invited

Single Electron Transistors as Far-Infrared Photon Detectors: *O. Astafiev*¹; V. Antonov¹; T. Kutsuwa¹; S. Komiyama²; ¹Department of Basic Science, University of Tokyo, Komaba 3-8-1, Meguro-ku, Tokyo 153-8902, Japan; ²Japan Science and Technology Corporation (JST) Kawaguchi-shi, Saitama 332-0012, Japan

2:30 PM, V.B.-2

High-Speed Waveguide Avalanche Photodetectors: *Geoffrey Kinsey*¹; R. Sidhu¹; A. L. Holmes, Jr.¹; J. C. Campbell¹; ¹The University of Texas at Austin, Microelectronics Research Center, MER 1.608B/R9900, Austin, TX 78712 USA

2:50 PM, V.B.-3

200-Gbit/s Monolithic Photodiode-Electroabsorption Modulator (PD-EAM) Optical Gate: *S. Kodama*¹; T. Ito¹; N. Watanabe¹; S. Kondo¹; H. Takeuchi¹; H. Ito¹; T. Ishibashi¹; ¹NTT Photonics Laboratories, Morinsato-Wakamiya 3-1, Atsugi-shi, Kanagawa 243-0198, Japan

3:10 PM, V.B.-4

A CMOS-Compatible High-Speed Silicon Lateral Trench Photodetector: *Min Yang*²; Ken Rim¹; Dennis Rogers¹; Jeremy Schaub¹; Jeffrey Welsch¹; Daniel Kuchta¹; Diane Boyd²; ¹IBM T. J. Watson Research Center, P. O. Box 218, Yorktown Heights, NY 10598 USA; ²IBM Microelectronics, Hopewell Junction, NY 12533 USA

3:30 PM Break

3:50 PM, V.B.-5

High-Temperature Operation of Mid-Infrared ($\lambda=4\text{--}5\mu\text{m}$) Vertical and Lateral InAs/GaAs/AlGaAs Quantum Dot Infrared Photodetectors: *A. D. Stiff*¹; S. Krishna¹; P. Bhattacharya¹; S. Kennerly¹; ¹University of Michigan, Solid State Electronics Laboratory, Department of Electrical Engineering and Computer Science, Ann Arbor, MI 48109-2122 USA; ²Army Research Laboratory, Sensors and Electron Devices Directorate, Adelphi, MD 20783 USA

4:10 PM, V.B.-6

Normal-incident $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}/\text{GaAs}$ Quantum Well Infrared Photodetector Employing a p-i-n-i-p Camel Diode Structure: *Heesoo Son*¹; Jinsung Park¹; Songcheol Hong¹; Sung-June Jo²; Jong-In Song²; ¹KAIST, Department of Electrical Engineering and Computer Science, Taejeon 305-701, Korea; ²K-JIST, Department of Information and Communications, Kwangju 500-712, Korea

4:30 PM, V.B.-7

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Single electron transistors as far-infrared photon detectors

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The single electron transistor (SET) [1] is able to detect polarization within small objects caused by individual electrons. This property can be utilized to realize high sensitive detection of electromagnetic waves reaching single photon counting level, if individual photons affect on an electron distribution within tiny devices capacitively coupled to SET. The best candidates for the detection are quantum dots (QDs) in two-dimensional electron gas (2DEG). Here, we explore far infrared (FIR) detectors based on two photo-excitation mechanisms in 2DEG: (i) cyclotron resonance (CR) absorption in high magnetic fields [2] and (ii) collective mode excitations at a characteristic frequency of the parabolic confinement potential in the absence of magnetic fields. The devices are fabricated by lithographic techniques in GaAs/Al_xGa_{1-x}As heterostructure crystals with 2DEG of 80 m²/Vs mobility and a sheet carrier density of $n_s = 2.6 \times 10^{15} \text{ m}^{-2}$ at 4.2 K. Experiments are carried out in a dilution refrigerator at a temperature of 70 mK. As a FIR-source we use 2DEG Hall-bar CR-emitter with continuously tuned wavelengths over range of $1 \text{ mm} < \lambda < 0.05 \text{ mm}$ [3]. The schematic views for the two types of the devices are shown in Fig. 1 (a) and Fig. 2 (a). Metal gates deposited on the top of GaAs/Al_xGa_{1-x}As laterally define QDs.

In the first device type (Fig. 1 (a)), QD is situated in a high magnetic field. The energy spectrum of electrons in QD is split into Landau levels (LLs) (here we neglect weak spin splitting). The magnetic field is chosen so that the lowest Landau level (LL1) is filled while the second Landau level (LL2) is partially filled by electrons as it is illustrated on Fig. 1 (b). Conductive ring and conductive core are formed by electrons of LL1 and LL2 at the Fermi level separated by completely filled area of LL1 with electrons below the Fermi level. A current between upper and lower reservoirs of Fig. 1(a) flows through the ring of QD when the electrochemical potential of the ring lines up with the electrochemical potentials of the reservoirs. When the QD is illuminated by FIR at nearly CR frequency, each absorbed photon excites electron-hole pair as it is shown on Fig. 1 (b). Just after the excitation, the electron and hole quickly lose their excess energies via phonon interaction and eventually go down and up, respectively, along LLs. Thus, the photon absorption results finally in one electron transfer from the ring to the core and can be detected as the conductance drop because of shift out of the resonance. Fig. 1 (c) demonstrates typical time-trace of the conductance through QD under illumination when the ground state is in the transport resonant conditions. When QD is illuminated by an extremely weak FIR radiation, random switches are appeared with switching rate strongly dependent on the intensity and wavelength of the incident radiation. With this sample we achieve the single photon detection counting in magnetic field range $3.4 \text{ T} < B < 4.15 \text{ T}$, which corresponds to detected wavelength range $0.17 \text{ mm} < \lambda < 0.21 \text{ mm}$. In properly adjusted conditions, “dark” switches are completely suppressed and from 10 to 100 photons per hour coming through an effective antenna area of extended metal gates are sufficient to detect the signal. Estimated from this, noise equivalent power (NEP) reaches the order of $10^{-22} \text{ W/Hz}^{1/2}$.

In the second device (Fig. 2 (a)), two capacitively coupled QDs are formed by negatively biased metal gates. Adjacent to the first QD (D1) that forms SET, the second QD (D2) is placed and capacitively coupled to D1. D2 is coupled to incident FIR by a planar dipole antenna. As depicted in Fig.2 (b), if an electron in D2 gains an excess energy through the excitation by FIR, the excited electron escapes either to D1 or to the electron reservoir adjacent to D2 so that the number of electrons in D2 decreases by one. The electron then rapidly releases its excess energy (via phonon emission or electron-electron interaction) relaxing to the Fermi level. The potential barriers, in turn, prevent the “cold” electron from returning to D2, thereby realizing a relatively long lifetime of the

ionized state of D2. Fig. 2 (c) demonstrates the time trace of the conductance near conductance resonance when weak illumination is applied in a rectangular waveform. The conductance exhibits short positive spikes, which become much more dense when radiation is tuned on. We ascribe the spikes to individual excitation events. The photo-response spectrum exhibits resonance with maximum at 0.6 mm wavelength and half-width of 0.1 mm. The resonance exactly corresponds to a characteristic frequency of the parabolic bare confinement potential within D2. We find out that the conductance spikes do not completely vanish in the dark conditions, probably, because the sample is not perfectly shielded against the 4.2K-black-body radiation in the present work. An estimated NEP for the sample to be of the order of 10^{-17} W/Hz^{1/2}.

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Figure captions:

Fig. 1. (a) Schematic view of QD in a high magnetic field. (b) Mechanism of internal polarization within QD caused by photon absorption at CR frequency. (c) Conductance time-trace when FIR-illumination is applied in rectangular waveform.

Fig. 2. (a) Schematic view of double-QD device. (b) Mechanism of photo-excitation. (c) Conductance time-trace when FIR is applied in a rectangular waveform.

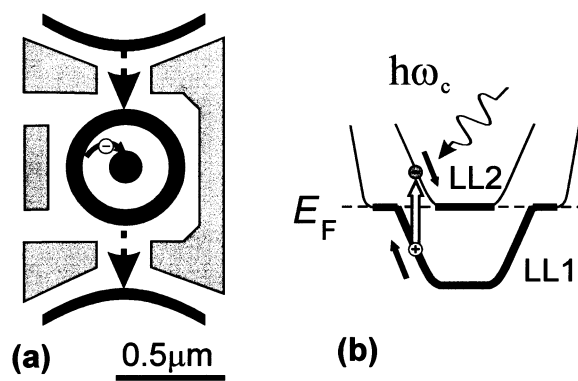


Fig. 1

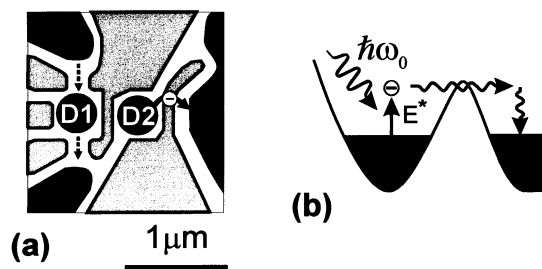
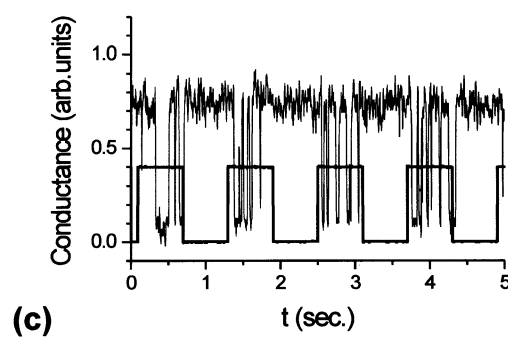
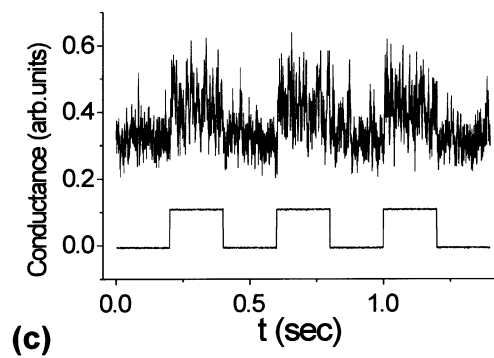


Fig. 2



High-Speed Waveguide Avalanche Photodetectors

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Avalanche photodetectors are becoming increasingly attractive as a means to boost sensitivity in optical communications systems. An edge-coupled waveguide configuration allows the absorption region to be thinned in order to reduce carrier transit times without compromising sensitivity. An AlGaAs/GaAs waveguide avalanche photodetector (WG-APD) was demonstrated with a maximum bandwidth of 32GHz and a gain-bandwidth product of 110GHz. An InGaAs/InAlAs waveguide avalanche photodetector was demonstrated with a bandwidth of 28GHz at low gains and an external quantum efficiency of 16% at 1.55 μ m. The gain-bandwidth product of 320GHz is the highest reported for an APD.

The AlGaAs/GaAs WG-APD was grown by solid-source molecular beam epitaxy on n-type GaAs (Fig. 1). The InGaAs/InAlAs WG-APD was grown by metal organic vapor phase epitaxy on n-type InP (Fig. 2).

The gain-bandwidth product of several AlGaAs/GaAs WG-APD devices, obtained from frequency response measurements, was approximately 110GHz (Fig. 3). The maximum optical bandwidth was 32GHz. The InGaAs/InAlAs WG-APDs had a thin multiplication layer of 150nm. The resulting gain-bandwidth product was 320GHz, based on a calculated gain at punchthrough of 1.28 (fig. 4). The maximum optical bandwidth was 28GHz.

Noise measurements were made on the InGaAs/InAlAs WG-APD material using an ultra-violet laser and a HP8970B noise meter at a frequency of 300MHz and a bandwidth of 4MHz. As shown in Fig. 4, an equivalent k value of ~ 0.15 was obtained for multiplication up to 23.

A thin InGaAs absorption layer was used in the InGaAs/InAlAs WG-APD to improve the carrier transit time and reduce the dark current. The quantum efficiency was measured using a tungsten-halogen light source, a spectrometer, and a lock-in amplifier. A beam waist approximately 4 μ m in diameter made for poor coupling with the relatively thin 200nm InGaAs core and 100nm InAlGaAs guiding layers. Scanning electron microscope images revealed that a rough, slightly beveled facet produced by the reactive ion etching compounded the coupling problem. For an uncleaved 10 μ m $\times$ 10 μ m device, the external quantum efficiency was less than 5% at 1.55 μ m. Higher coupling efficiencies were achieved with a manually cleaved device 40 μ m in length. The external quantum efficiency was 16% at 1.55 μ m.

In conclusion, we report an AlGaAs/GaAs waveguide avalanche photodiode with a unity-gain bandwidth of 32GHz and a gain-bandwidth product of 110GHz. An InGaAs/InAlAs waveguide avalanche photodetector demonstrated a low multiplication excess noise corresponding to $k=0.15$ and an external quantum efficiency of 16% at 1.55 μ m. The 320GHz gain-bandwidth product is the highest reported for an APD.

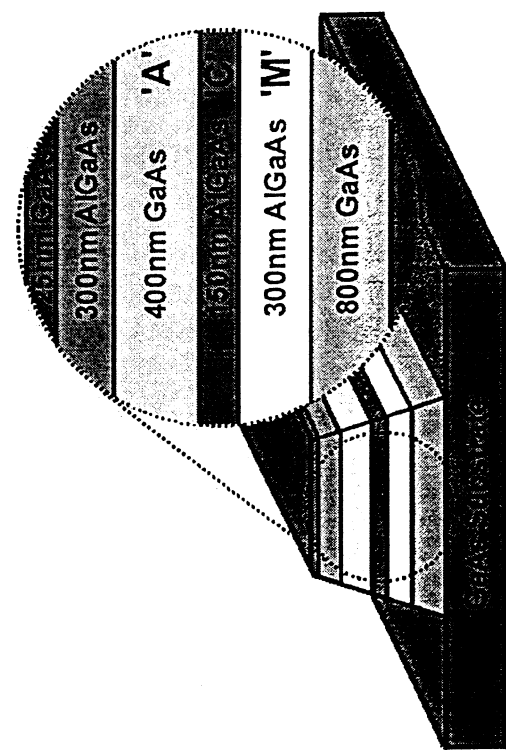


Figure 1. Cross section of the AlGaAs/GaAs WG-APD.

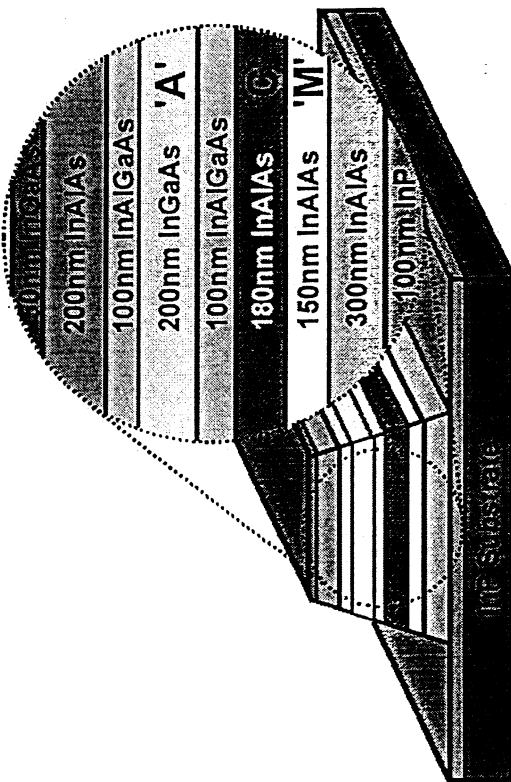


Figure 2. Cross section of the InGaAs/InAlAs WG-APD.

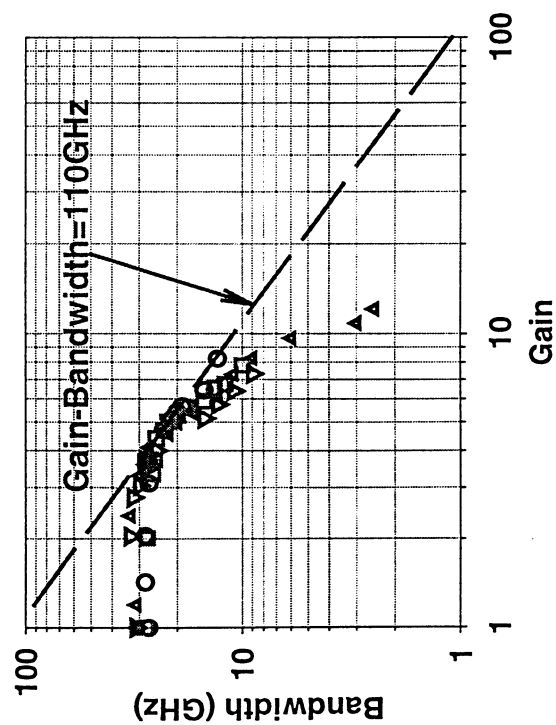


Figure 3. Gain-bandwidth product of several AlGaAs/GaAs WG-APDs.

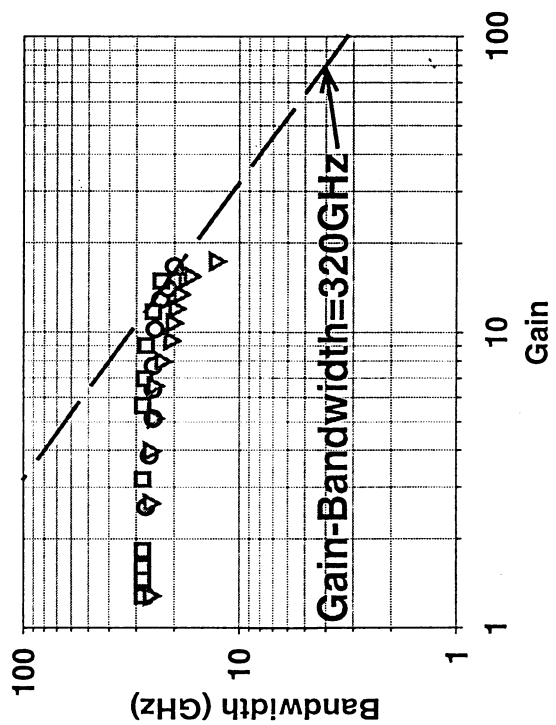


Figure 4. Gain-bandwidth product of several InGaAs/InAlAs WG-APDs.

200-Gbit/s Monolithic Photodiode-Electroabsorption Modulator (PD-EAM) Optical Gate

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This paper presents optical demultiplexing (DEMUX) operation of a novel ultrafast optical gate that monolithically integrates a uni-traveling-carrier photodiode (UTC-PD) [1] and an electro-absorption modulator (EAM). Adopting a traveling-wave (TW) design for the EAM together with the effective use of the nonlinear extinction characteristics of the EAM, the demultiplexing of optical RZ signals corresponding to a 200 Gbit/s data rate has been achieved with an extinction ratio of 18.6 dB.

Ultrafast optical gates (or switches) have attracted attention as key devices for future optical communication systems with high bit-rate TDM channels (≥ 100 Gbit/s). Among them, a device based on semiconductor technology is favorable because of its compactness and easier system insertion. To date, the semiconductor optical amplifier-based symmetric Mach-Zehnder (SOA-MZ) all-optical switch has been investigated intensively [2]. On the other hand, electro-optic (EO) switches, which can be further advantageous in terms of operation simplicity over all-optical ones, also have high potential. The realization of ultrafast EO-switches has actually been limited by the bandwidth of driver amplifiers and the electrical interconnections. To overcome these problems, we have proposed a monolithic optical gate configured of a UTC-PD and an EAM in which the PD directly drives the EAM without electrical amplifiers (monolithic PD-EAM) [3]. We have also demonstrated its operation with a gate opening time of 2.3 ps [3]. In this work, the DEMUX operation of the PD-EAM is studied.

The equivalent circuit and photograph of the fabricated monolithic PD-EAM are shown in Figs. 1(a) and (b), respectively. It consists of a back-illuminated InP/InGaAs UTC-PD, a TW-EAM with InAlGaAs/InAlAs multiple-quantum-wells (MQWs), two bias capacitors, and a matched resistor (R_T) for the electrical termination of the EAM waveguide. The PD anode is connected to the signal line (anode) of the TW-EAM, and thus an optical input (photocurrent) generates a positive signal to the EAM, constructing the transmission gate. The EAM ridge waveguide has a 200- μm -long active part and two 100- μm -long passive parts on either side of the active part. The junction area of the UTC-PD is 50 μm^2 and its 3-dB bandwidth is around 80 GHz. Chip size is 1 mm x 0.4 mm.

In testing for DEMUX operation of the PD-EAMs, the optical output signal was detected using a cross-correlation technique. The input RZ-data pulses to the EAM (5-ps period), corresponding to 200 Gbit/s, were prepared by multiplexing a 1.55- μm optical pulse generated by a passive mode-locked fiber laser (ML-FL) with an FWHM of 800 fs and repetition rate of 32.6 MHz. The same initial pulse from the ML-FL was compressed to an FWHM of 240 fs in order to provide the PD and the cross-correlator with clock (control) and probe pulses, respectively. The optical energy of the input signal fed to the EAM was fixed at 0.1 pJ/pulse. The EAM bias voltage for the gate-off state was -3.5 V.

Figures 2(a) and (b) show the input data pulses (observed through the EAM transmission) and each output pulse for each time slot, respectively. It is clear that every input data pulse is demultiplexed by adjusting the timing between the input data pulses and the control pulse. Figure 3 shows the on/off ratio of the PD-EAM gating under 200-Gbit/s DEMUX operation. Here, to characterize interchannel crosstalk, the on/off ratio is defined as the peak intensity ratio between the on-level and the adjacent off-level [Fig. 3(a)]. A good on/off ratio of 18.6 dB was obtained at a control pulse energy of 8.6 pJ/pulse, as shown in Fig. 3(b). At a smaller control pulse energy of 3.9 pJ/pulse, the on/off ratio remains as high as 16.7 dB.

We have investigated the demultiplexer function of the monolithic PD-EAM at a data-rate corresponding to 200-Gbit/s and demonstrated a high extinction ratio (low interchannel crosstalk). Design optimization of each device element should further improve the PD-EAM performance.

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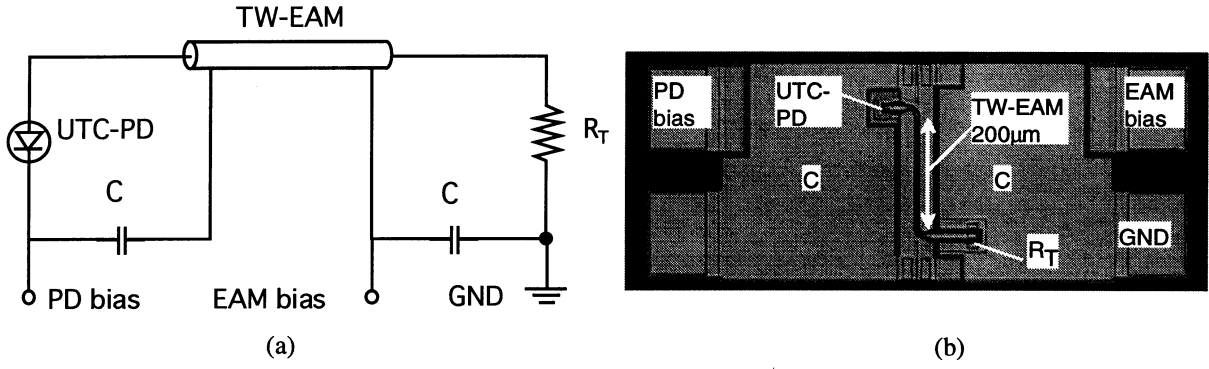


Fig. 1 (a) Equivalent circuit and (b) photograph of a fabricated monolithic PD-EAM optical gate.

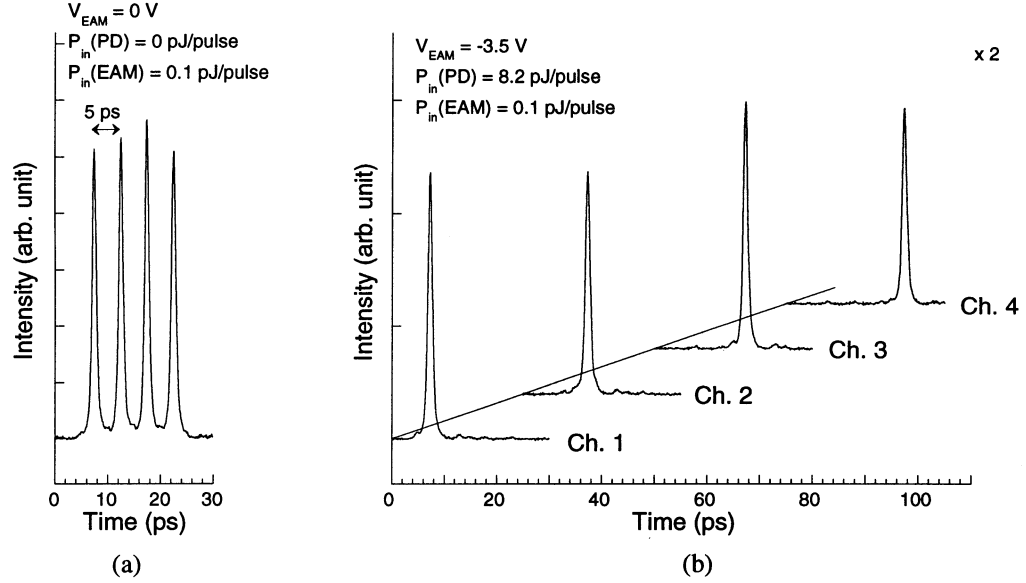


Fig. 2 200-Gbit/s demultiplexing operation of PD-EAM. (a) Input and (b) output data. Both (a) and (b) are observed by cross-correlation.

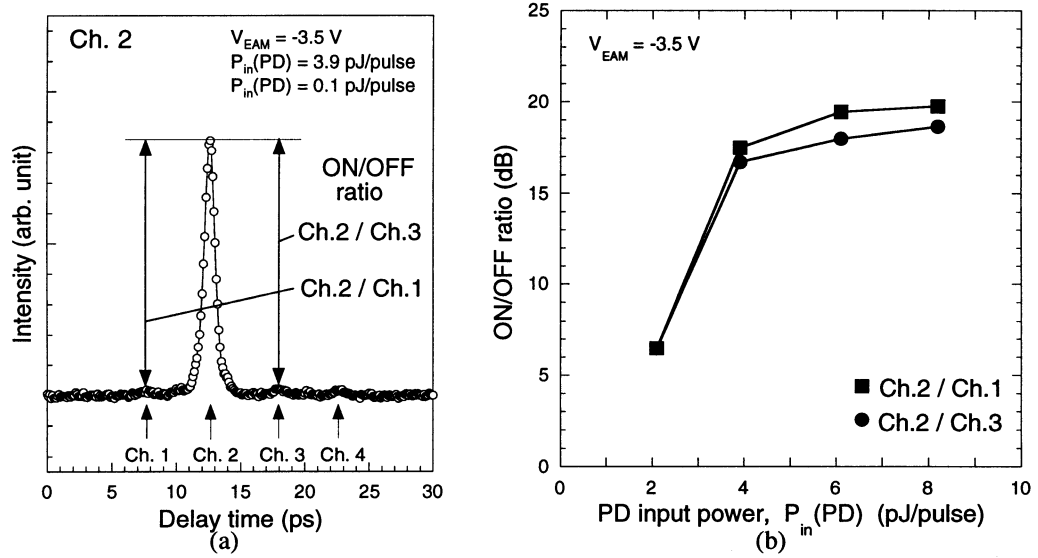


Fig. 3 (a) Definition of the on/off ratio and (b) measured on/off ratios under 200-Gbit/s operation of the monolithic PD-EAM optical gate.

A CMOS-Compatible High-Speed Silicon Lateral Trench Photodetector

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Introduction

Silicon-based photodetectors (Fig.1a) have difficulty in achieving both high bandwidth and high responsivity due to the long absorption depth of silicon (15 μ m) at 850nm. Metal-semiconductor-metal (MSM) detectors have been demonstrated on SOI with very high bandwidth gained at the expense of low responsivity [1]. Using a trench MSM structure, higher responsivity has been reported [2]. Lateral p-i-n photodiodes on SOI substrates have demonstrated 1-2GHz bandwidths and 18-25% peak external quantum efficiencies at 3V [3, 4].

In the present work, we have fabricated fully CMOS-compatible silicon lateral p-i-n photodiodes with deep trenches to enhance the collection of deep photocarriers (Fig.1b). The devices exhibit a bandwidth of 2.5GHz at 670nm and a 3V bias. Successful operation at 2.5Gb/s and 845nm has been achieved at 3.3V. The responsivity is 0.45A/W at 845nm, corresponding to an external quantum efficiency of 66%. To the authors knowledge, these devices have the best overall function (highest speed-responsivity at low bias) among silicon-based photodetectors.

Device Structure and Fabrication

The lateral trench photodetectors (LTDs) were fabricated on a p-type (100) silicon substrate with a resistivity of 11-16 Ω -cm. The detailed process flow is shown in Fig.2. The 0.35 μ m wide and 8 μ m deep trenches were formed by reactive ion etching (Fig.2a). The trenches were laid out in interdigitated finger patterns with a spacing of 3.3 μ m. The device area looking from the top was a circle with a diameter of 75 μ m (Fig.3). Borosilicate glass (BSG) was then deposited as a sacrificial trench fill material, and the surface was planarized by chemical-mechanical-polishing (CMP). A hard mask layer was then deposited (Fig. 2b). Using the patterned hard mask, BSG was stripped off from every other trench (Fig.2c). Fig.4a shows the cross-sectional SEM picture of a device at this point of fabrication. In-situ phosphorus-doped polysilicon ($\sim 10^{20}$ cm⁻³) was then deposited to fill the empty trenches. The top of the trenches were exposed by a polysilicon CMP (Fig.2d). The BSG in the remaining trenches was then stripped off, the cross-sectional SEM being shown in Fig.4b. In-situ boron-doped polysilicon ($\sim 10^{18}$ cm⁻³) was deposited and the structure was planarized by CMP (Fig.2e). The devices were annealed at high temperature to drive in the dopant so as to move the junctions away from silicon/polysilicon interface. Fabrication of CMOS devices can resume at this point for a fully integrated receiver. In this work, only discrete photodetectors with silicide and metal contact on top of each trench were fabricated. No anti-reflection coating was used.

Experimental Results

Fig.5 shows the reverse I-V characteristics of a fabricated LTD. Extremely low dark currents of 1.5pA were observed at 5V. The breakdown voltage was 27V.

Fig.6 shows the small-signal frequency response of the LTD. At a wavelength of 670nm, the 3dB bandwidth is 2.5GHz. Higher bandwidth is expected for smaller finger spacing. A low frequency tail ($f < 100$ MHz) was observed at 845nm (Fig 6b). For $f > 100$ MHz, the signal dropped by 3dB (electrical) at 2GHz. At this wavelength, about half of the light is absorbed in the silicon below the trenches. Of these carriers, some transport via diffusion in the undepleted silicon and some transport slower due to relatively low electrical fields. The low frequency response can be improved by using deeper trenches. The responsivity is 0.45A/W ($\eta = 66\%$) at 845nm.

A discrete LTD was then wire-bonded to a BiCMOS transimpedance amplifier to form a receiver. The measured eye-diagram using an 845nm wavelength laser source modulated with a 2.5Gb/s, 2⁷-1 pseudo-random-bit-sequence (PRBS) input is shown in Fig.7. The receiver exhibits excellent performance in spite of the elevated low frequency response. At a BER of 10⁻⁹ and a bias of 3.3V, the sensitivity was -16.1dBm at 2.5Gb/s. This is the highest sensitivity of any silicon-based optical receiver at this data rate. With a fully integrated LTD and amplifier, we expect to obtain an even higher sensitivity.

Conclusion

Novel silicon lateral trench photodetectors that are compatible with CMOS processing have been demonstrated. The trench structure decouples the carrier transit distance from the light absorption depth. The LTDs exhibit high-speed, high responsivity and excellent operation at 2.5Gb/s and 3.3V bias for light source at 845nm wavelength. The performance and the process compatibility of the silicon LTD make possible the fabrication of silicon monolithic receivers for fiber-optic data links.

Acknowledgments

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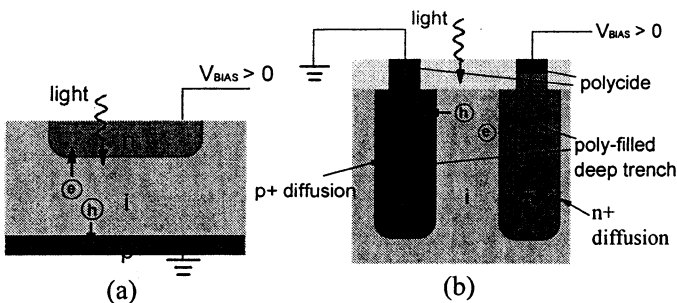


Fig 1. Cross-section of silicon based photodiodes: (a) vertical p-i-n diode (b) lateral trench detector (LTD).

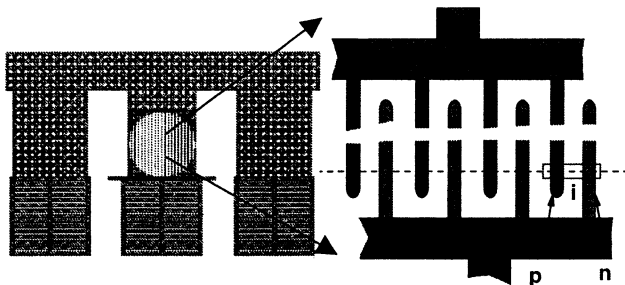


Fig. 3 The top-down view of a LTD. The trenches are interdigitated patterns with spacing of 3.3 μm. The whole area is a circle with a diameter of 75 μm.

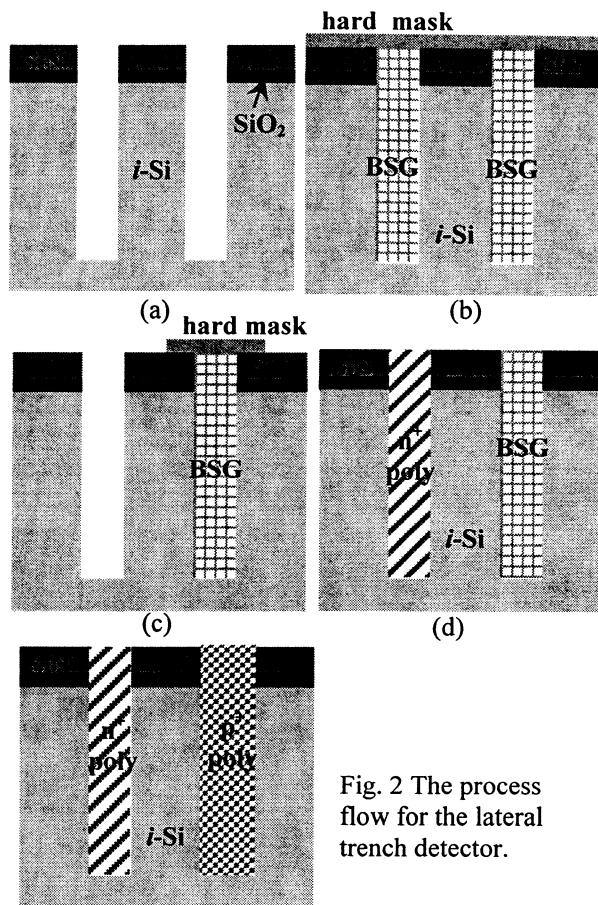


Fig. 2 The process flow for the lateral trench detector.

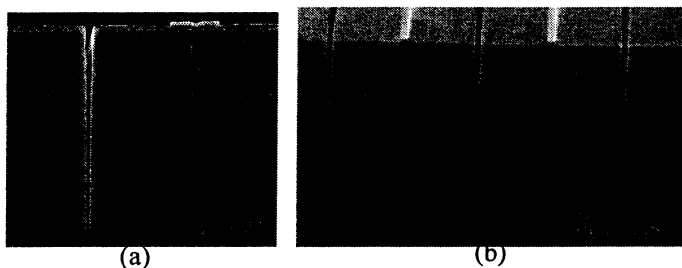


Fig. 4 SEM pictures of LTD when (a) BSG was stripped from every the other trench (b) BSG was stripped from the rest of the trenches after n^+ polysilicon deposition and CMP.

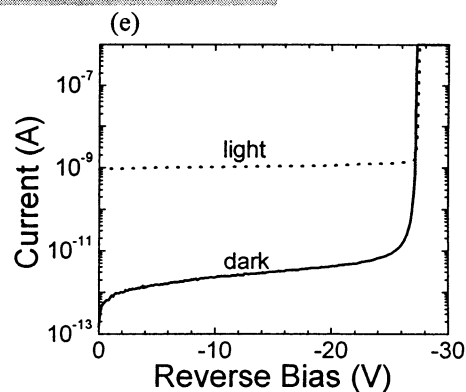


Fig.5 Measured dark and light current from the LTD at reverse bias. The breakdown voltage is 27V.

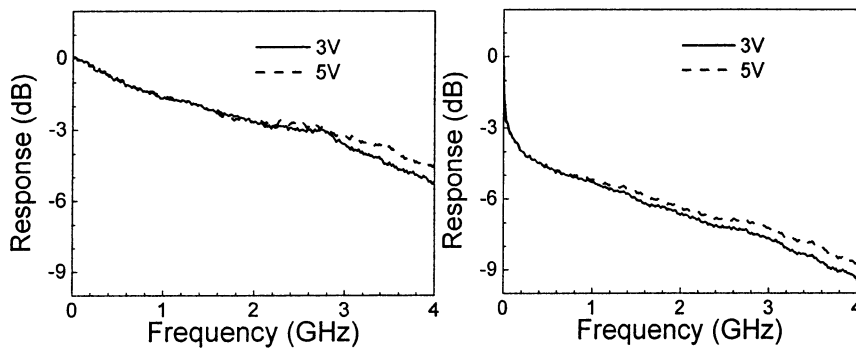


Fig. 6 Frequency response of the LTD at (a) 670nm and (b) 850nm.

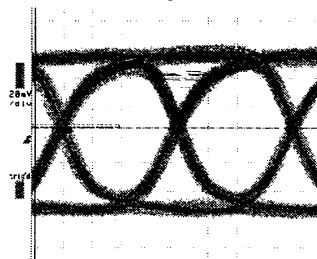


Fig.7 Eye diagrams of a discrete LTD wired to a BiCMOS amplifier at 3.3V bias and 2.5Gb/s rate. The light source is 845nm.

High-Temperature Operation of Mid-Infrared ($\lambda=4-5\ \mu\text{m}$) Vertical and Lateral InAs/GaAs/AlGaAs Quantum Dot Infrared Photodetectors

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Abstract

Infrared (IR) detection has sundry applications from military targeting systems to the observation of stellar phenomena to professional photography. State-of-the-art IR photon detection is dominated by mercury cadmium telluride (MCT) detectors and quantum well infrared photodetectors (QWIPs). While these devices can yield specific detectivities (D^*) on the order of $10^{11}\ \text{cmHz}^{1/2}/\text{W}$ (Jones), they generally require an operating temperature of 80K or less¹. Therefore, it is desirable to develop a high temperature IR photon detection technology, which would lend itself more readily to lightweight, compact, inexpensive IR cameras.

Intersubband quantum dot infrared photodetectors (QDIPs) have great promise for providing high-temperature normal incidence operation in the mid- and far-infrared ranges due to the favorable dynamics of hot carriers in quantum dots². In this paper, we present state-of-the-art results on vertical and lateral mid-infrared ($\lambda=4-5\ \mu\text{m}$) InAs/GaAs/AlGaAs QDIPs. To our knowledge, the vertical detector we have characterized has the lowest reported dark current for such a device ($I_{\text{dark_vertical}}=125\text{nA}$ at $V_b=0.5\text{V}$ for $T=300\text{K}$)^{3,4}. The lateral detector, which also has an extremely low dark current ($I_{\text{dark_lateral}}=27\text{pA}$ at $V_b=0.5\text{V}$ for $T=100\text{K}$), also has one of the highest operating temperatures (100K) to be reported for such a device⁵. Both of these detectors deliver D^* values in the 10^8 Jones range at an operating temperature of 100K. These D^* measurements are accurately obtained using a calibrated blackbody source.

Vertical QDIPs (VQDIPs), which operate by means of vertical transport of carriers through directly doped quantum dot layers, have been grown and fabricated with symmetric and asymmetric AlGaAs barriers. Schematics of the heterostructure and the conduction band diagram are shown in Fig. 1. These AlGaAs barriers, on either side of each dot layer, impede the collection of free carriers between the top and bottom contacts, thus reducing the dark current (Fig. 2). While this also reduces the amount of photogenerated current that can be collected, the thickness and composition of the AlGaAs barrier can be engineered to optimize the responsivity (R) of the detector. As shown in Fig. 3, the maximum values for peak detectivity and peak responsivity at $T=100\ \text{K}$ are 1.2×10^8 Jones and $1.4\ \mu\text{A}/\text{W}$, respectively. The inset to Fig. 3 shows the spectral response for this device, which peaks at $4.1\ \mu\text{m}$. We believe this peak arises from an electron bound state to continuum transition in the quantum dot.

The lateral QDIP (LQDIP) operates by lateral transport of carriers between two top contacts. In this case, the AlGaAs barriers are used to modulation-dope the quantum dots and to provide a high mobility collection channel at the GaAs/AlGaAs interface, much like a FET structure. The heterostructure and conduction band diagram are shown in Fig. 4. Since the major component of the dark current arises from interdot tunneling and hopping conduction, the dark current is extremely low in these devices (Fig. 5). The maximum peak detectivity and responsivity at $T=70\text{K}$ are 4.4×10^8 Jones and $9.9\text{mA}/\text{W}$, respectively (Fig. 6). The peak spectral response occurs at $5.05\ \mu\text{m}$, as shown in the inset to Fig. 6.

Further work is in progress to optimize the design of these detectors and to obtain higher values of D^* and R at higher temperatures. These design considerations will also be presented and discussed.

This work is supported by ARO and DARPA.

¹ M.Z. Tidrow, Mat. Sci. and Engin. B, **74**, 45 (2000).

² J. Phillips, P. Bhattacharya, S.W. Kennerly, D.W. Beekman, and M. Dutta, IEEE J. Quant. Elect., **35**, 936 (1999).

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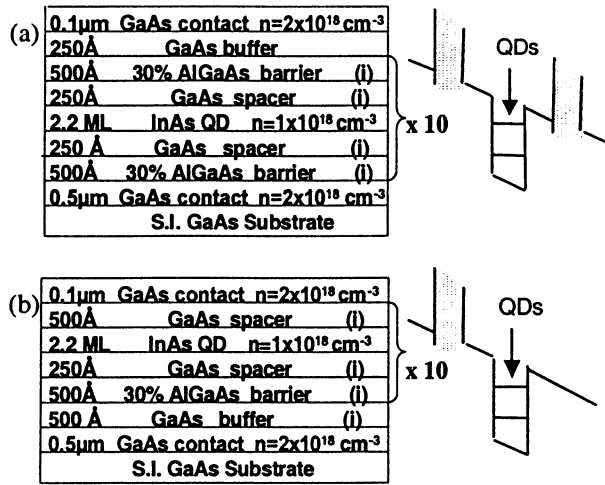


Figure 1. Vertical QDIP with (a) symmetric barrier and (b) asymmetric barrier

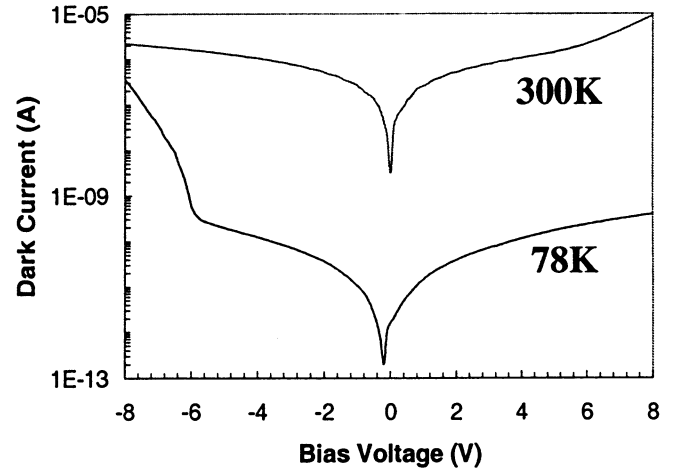


Figure 2. Dark current for vertical QDIP with asymmetric AlGaAs barrier

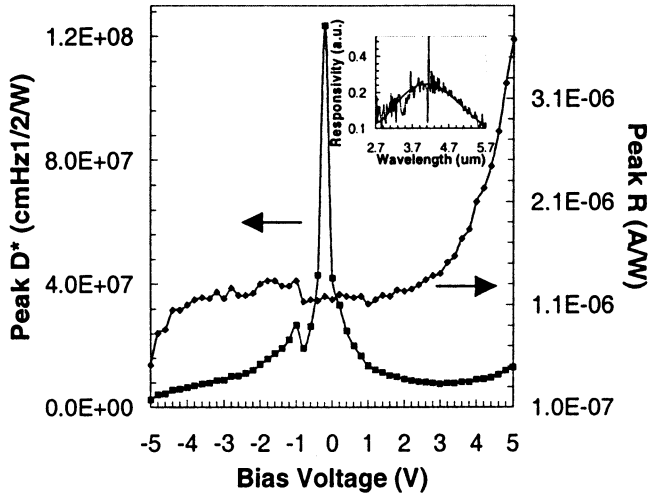


Figure 3. Peak D^* and R for vertical QDIP with asymmetric AlGaAs barrier, spectral response shown as inset

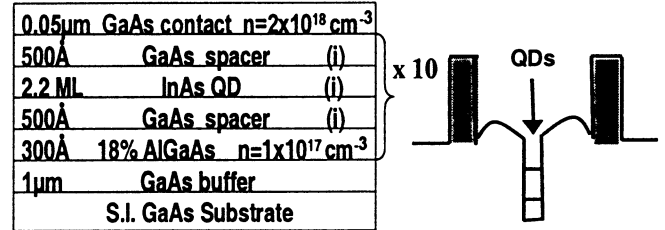


Figure 4. Lateral QDIP with 18% AlGaAs barrier

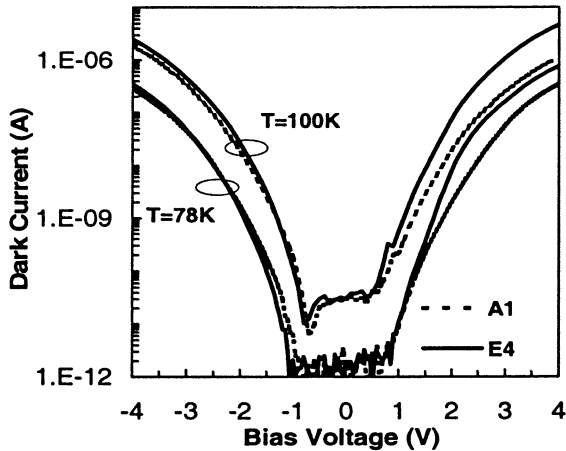


Figure 5. Dark current for lateral QDIP with 18% AlGaAs barrier

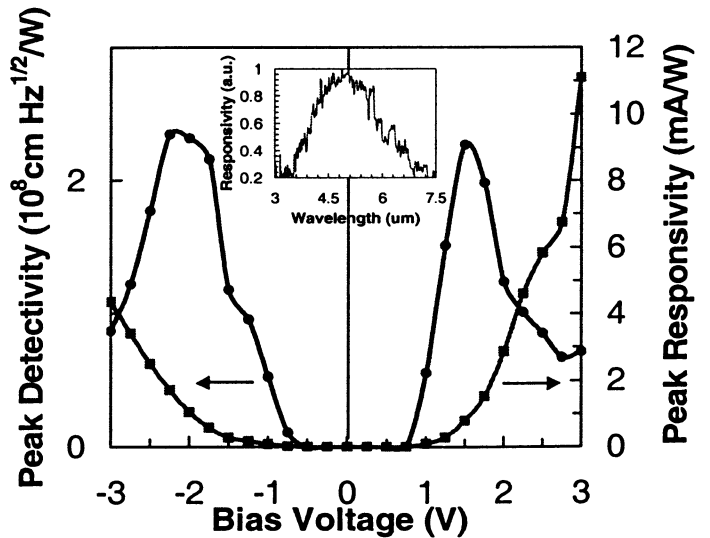


Figure 6. Peak D^* and R for lateral QDIP with 18% AlGaAs barrier, spectral response shown as inset

Normal-incident $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}/\text{GaAs}$ Quantum Well Infrared Photodetector Employing a p-i-n-i-p Camel Diode Structure

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Quantum well infrared photodetectors (QWIPs) utilizing intersubband transitions have been widely used for detecting far-infrared optical signals having wavelengths of 3-5 μm or 8-12 μm within the atmospheric transmission windows. It is well known that QWIPs utilizing the electron intersubband transition has a limitation since normal-incident absorption is forbidden. The use of hole intersubband transitions allows the normal-incident absorptions due to the hole-band mixing in quantum wells. However, due to the large effective mass of hole, the absorption coefficient and thus the detectivity of the QWIPs utilizing the hole intersubband transitions are generally lower than those of QWIPs utilizing the electron intersubband transitions [1]. Chu et al. reported the normal-incident p-i-p QWIPs having detectivities as high as 0.14 ~ 1.07 $\text{cm Hz}^{1/2}/\text{W}$ by using p-doped compressive-strained InGaAs quantum wells [2]. In this paper, we report on a normal-incident QWIP having an improved detectivity that is achieved by reduction in dark current by employing a p-i-n-i-p camel diode structure.

The epitaxial layer structure of the p-i-n-i-p QWIP, shown in Fig. 1, was grown on a semi-insulating GaAs (100) substrate. The schematic cross-section of the device and the energy band diagram are shown in Fig. 2. Unlike the conventional p-i-p QWIP layer structure, the QWIP employing a p-i-n-i-p camel diode structure has an 8 nm n^+ δ -doped region just below the active region. As can be seen in Fig. 2, the n^+ δ -doped layer generates a potential barrier for hole (ϕ_{bo}) that plays a role of inhibiting the dark current and thus improving the detectivity.

QWIPs having a $75 \times 75 \mu\text{m}^2$ active area were fabricated. Fig. 3 shows dark currents of the detector as a function of bias voltage with the temperature as a parameter. The dark current of the conventional p-i-p QWIP, reported in ref [2], having a similar active area ($50 \times 50 \mu\text{m}^2$) measured at 77 K is also shown for comparison. Unlike the conventional p-i-p QWIP, I-V characteristics of the QWIP utilizing the p-i-n-i-p camel diode structure showed an unsymmetrical behavior. The dark current of the p-i-n-i-p QWIP was more than 5 orders of magnitude lower than that of the conventional p-i-p QWIP at operating bias voltages ($V_D < 0\text{V}$). Fig. 4 and 5 show the 10 K PL spectra and the temperature dependent absorption photocurrent spectra for interband transitions, respectively. Fig. 6 shows the bias dependent intersubband absorption photocurrent spectra measured at 10 K. The peak at $\sim 3 \mu\text{m}$ is ascribed to the transition between the first heavy hole state and continuum states. The detectivity estimated from the photocurrent response and the dark current measurements was approximately $4.4 \times 10^{10} \text{ cm Hz}^{1/2}/\text{W}$.

In conclusion, a normal-incident QWIP utilizing the hole intersubband transitions having the detectivity as high as $4.4 \times 10^{10} \text{ cm Hz}^{1/2}/\text{W}$ has been demonstrated. The improvement in the detectivity is ascribed to the reduction in the dark current achieved by using a p-i-n-i-p camel diode structure. Further improvement in detectivity is expected by increasing the responsivity of the detector, which can be achieved by doping the quantum wells with a p-type dopant and increasing the period of MQW [2].

[1] B.F. Levine, *J. Appl. Phys.* vol. 74, no. 8, p. R1, 1993.

[2] J. Chu and S. S. Li, *IEEE J. Quantum Electron.*, vol. 33, p. 1104, 1997.

p ⁺ In _{0.2} Ga _{0.8} As	5x10 ¹⁸ /cm ³	10 nm
p ⁺ GaAs	2x10 ¹⁸ /cm ³	500 nm
GaAs	undoped	30 nm
In _{0.2} Ga _{0.8} As/GaAs QW (10 periods)	undoped	5/20 nm
GaAs	undoped	50 nm
n ⁺ GaAs	2x10 ¹⁸ /cm ³	8 nm
GaAs	undoped	20 nm
p ⁺ GaAs	2x10 ¹⁸ /cm ³	400 nm
GaAs Buffer	undoped	300 nm
Semi-insulating GaAs Substrate		

Fig. 1. Epitaxial layer structure of the QWIP employing a p-n-p camel diode structure

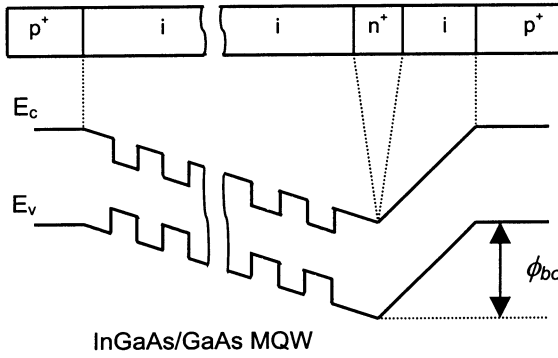


Fig. 2. Schematic cross-section and energy band diagram of the QWIP employing a p-n-p camel diode structure.

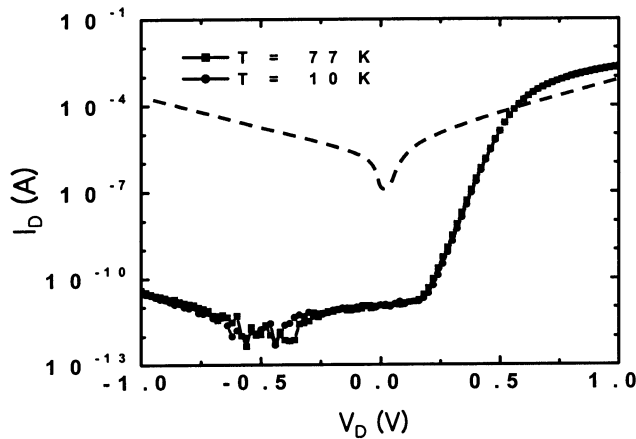


Fig. 3. Temperature dependent I-V characteristics of the QWIP employing a p-n-p camel diode structure. The dashed line shows I-V characteristics of the conventional p-i-p QWIP reported in ref. [2] measured at 77 K.

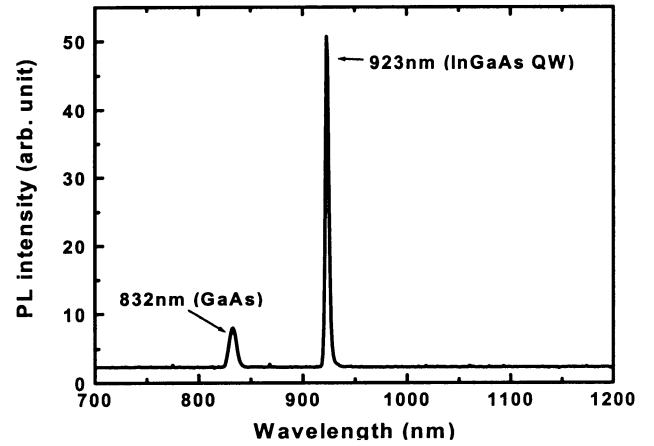


Fig. 4. Photoluminescence spectra of the QWIP employing a p-n-p camel diode structure measured at 10 K.

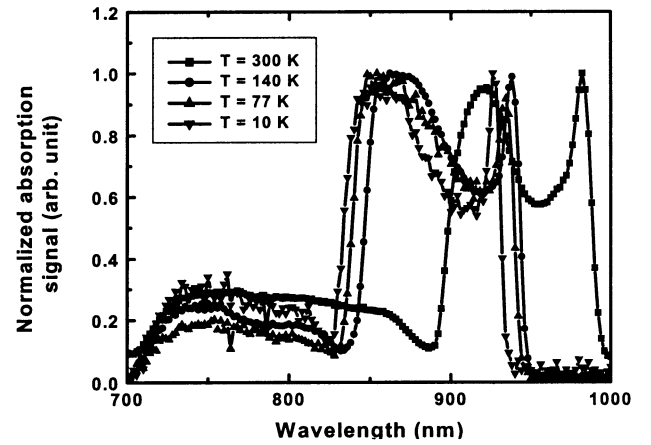


Fig. 5. Temperature dependence of interband absorption photocurrent spectra.

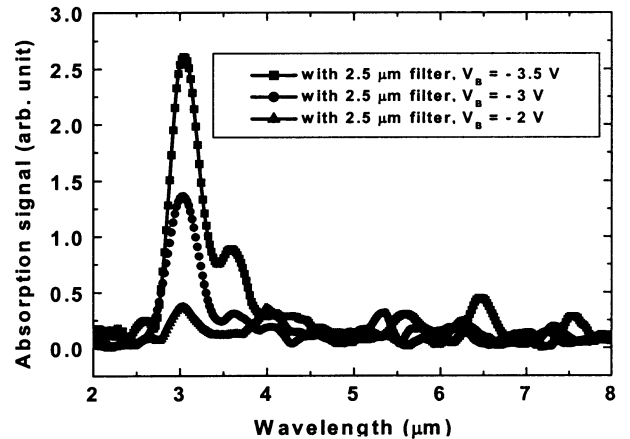


Fig. 6. Bias dependence of intersubband absorption photocurrent spectra measured at 10 K.

High Efficiency, Large Area, InGaAs/InPAs Thermophotovoltaic Cells

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Thermophotovoltaic (TPV) cells are a class of photovoltaic devices designed to convert radiant heat energy ($\lambda > 1.5 \mu\text{m}$) to electrical power through the use of low bandgap ($\sim 0.5 \text{ eV}$) semiconductor material systems. Efficiencies in a TPV system may be enhanced by matching the spectral output of the radiator to the cell and by reflecting photons with energy $h\nu < E_g$ to help maintain heat in the radiator. In this paper, we present an InGaAs/InPAs double heterostructure TPV cell that has achieved a power conversion efficiency of **13.8 %** and a power density of **0.54 W/cm²** for a graphite radiator operating at 995°C and a cell temperature of 27.8°C. This represents the best performance of a TPV device for these operating conditions to date.

The 0.6 eV InGaAs/InPAs structures are being grown on 3" semi-insulating InP substrates by MOCVD¹. Lattice mismatched growth of InGaAs and InPAs active layers is achieved by first growing a three step, compositionally graded InPAs buffer scheme. A lateral conduction layer of n-type InGaAs serves as the internal contact layer for the cell. In order to use a p-type base region with an n-type lateral conduction layer, a p++/n++ tunnel diode is implemented with InGaAs. The InGaAs/InPAs double heterostructure, which forms the cell, is grown next. Finally an n+ contact layer to the topside of the cell is accomplished with InGaAs material.

These devices are made as a Monolithic Interconnected Module (MIM) to permit the fabrication of large area cells². Presently, 30 interconnected diodes on the semi-insulating InP substrate comprise a TPV device with a die area of 4 cm². Each cell is 2 cm long by 600 μm wide, which results in an active area of approximately 3.6 cm² for the 30-diode cell. Wet etches are used to isolate each diode, and contact to the topside and backside of the cell is made with a Cr/Au or Ti/Au metalization process. On the back of the InP substrate, silicon nitride and Au form a reflector to reflect the light not absorbed on the first pass and to recuperate below bandgap light at the radiator. A silicon nitride layer on the front of the cell serves as an anti-reflection coating.

Cells are electrically evaluated using a quartz-halogen lamp assembly for open circuit voltage (V_{oc}), short circuit current (I_{sc}), fill factor (FF) and maximum power ($P_{max} = V_{oc} * I_{sc} * FF$). Typically, at a short circuit current of 100 mA and a cell temperature of 25°C, these high efficiency 30-diode cells deliver a V_{oc} of 9.4 V, FF of 61 % and P_{max} of 580 mW. The TPV cells are optically evaluated for quantum efficiency and reflectance over the spectral range of interest. Individual MIMs are mounted in ceramic saddles for in-vacuum efficiency measurements using a graphite gray body radiators heated to temperatures as high as 1000°C. The ceramic saddle containing the cell is affixed atop a thermo-electric cooled copper pedestal permitting the absorbed power (P_{abs}) to be measured by monitoring a drop in temperature across the pedestal. Thus, the efficiency defined as the percentage P_{max}/P_{abs} may be calculated for various radiator and cell temperatures. At a graphite radiator temperature of 882°C and a cell temperature of 22.2°C, the TPV cells were 10.6 % efficient and produced a power density of 0.26 W/cm². Increasing the radiator temperature to 995°C, a power conversion efficiency of 13.8 % and a power density of 0.54 W/cm² were measured for a cell operating at 27.8°C.

1. C. S. Murray, N. Fatemi, M. Stan, B. Wernsman, and R. J. Wehrer, "Growth, Processing, and Characterization of 0.55 eV n/p/n Monolithic Interconnected Modules," 28th IEEE Photovoltaic Spec. Conf., Anchorage, Ak, Sept. 15-22, 2000.
2. D. M. Wilt, E. B. Clark, M. B. Clevenger, C. S. Murray, and R. J. Wehrer, "0.55 eV n/p/n MIM TPV Cell Development," 28th IEEE Photovoltaic Spec. Conf., Anchorage, Ak, Sept. 15-22, 2000.

Si ₃ N ₄ Anti-reflection Coating	
n++ InGaAs Contact	
n InPAs Window	
n+ InGaAs Emitter	} Double heterostructure cell
p InGaAs Base	
p InPAs Back Surface Field	
p++ InGaAs	
n++ InGaAs	} Tunnel junction
n+ Lateral Conduction Layer	
Undoped InPAs Buffer	
Semi-insulating InP Substrate	
Si ₃ N ₄ Reflector	
Gold Back Surface Reflector	

Fig 1. Cross-section of the double heterostructure MIM device.

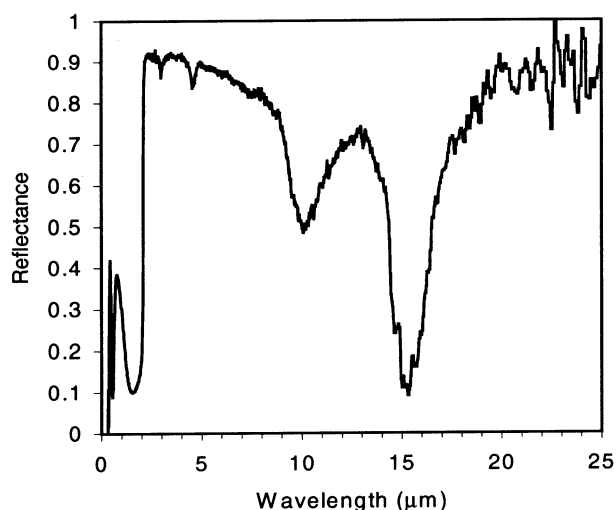


Fig. 3. Measured reflectance of a 0.6 eV MIM.

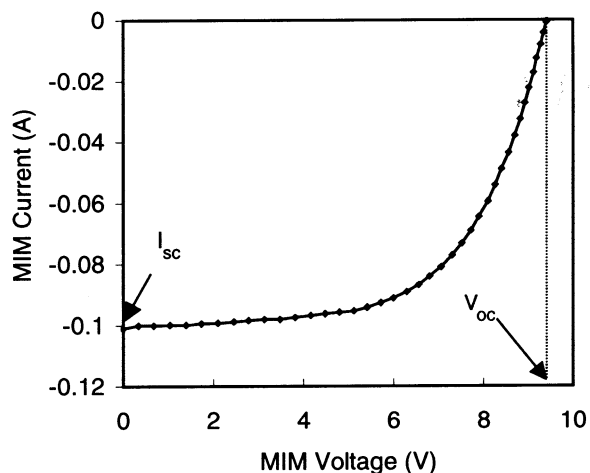


Fig. 2. Measured illuminated I-V showing Voc and Isc values.

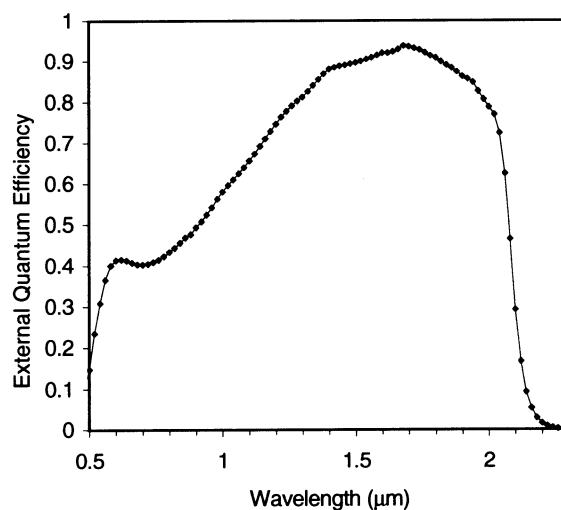


Fig. 4. Measured external quantum efficiency.

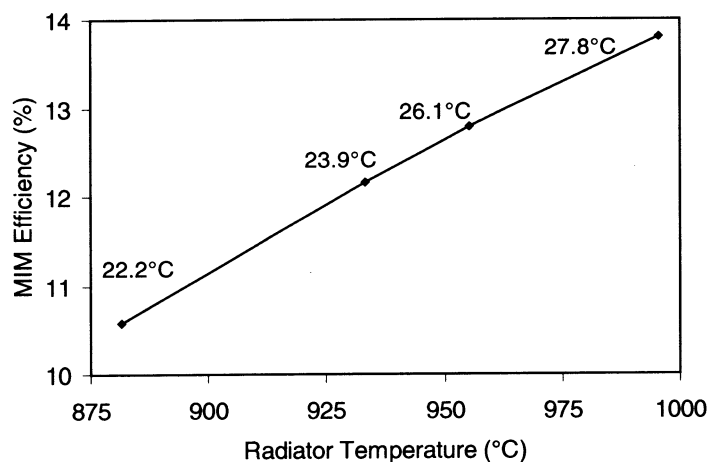


Fig. 5. Measured in-vacuum MIM efficiency using a graphite radiator. The cell temperature is indicated on the graph.

Nanostructure Modeling

WEDNESDAY AM, JUNE 27TH, 2001

Session Organizers: Frank Register, The University of Texas at Austin; Supriyo Bandyopadhyay, University of Nebraska

10:00 AM, VI.A.-1

Spin-Orbit Interaction of 2° in InAlAs/InAs Hetero-structures: *Kanji Yoh*¹; Toshihiro Doi¹; Shin-ichiro Abe²; Yoshito Katano¹; Hiroshi Ohno²; Kazuhisa Sueoka²; Koichi Mukasa²; ¹Hokkaido University, RCIQE, N13, W8, Kita-ku, Sapporo, Hokkaido 060-8628 Japan; ²Hokkaido University, Grad. Sch. of Eng., N13, W8, Kita-ku, Sapporo, Hokkaido 060-8628 Japan

10:20 AM (Student), VI.A.-2

Thermal Conductivity in Semiconductor Thin Films and Nanowires: *Jie Zou*¹; Alexander A. Balandin¹; ¹University of California at Riverside, Dept. of Electl. Eng., Riverside, CA 92521 USA

10:40 AM (Student), VI.A.-3

Quantum Mechanical Calculation of QCA Molecule Properties: *Christopher J. Russo*¹; *Craig S. Lent*¹; ¹University of Notre Dame, Electl. Eng., 275 Fitzpatrick, Notre Dame, IN 46556 USA

11:00 AM, VI.A.-4

Nano-Transistor Modeling: Two Dimensional Green's Function Method: *A. Svizhenko*¹; M. P. Anantram¹; T. R. Govindan¹; B. Biegel¹; ¹NASA, Ames Rsrch. Ctr., MS T27A-1, Moffett Field, CA 94035-1000 USA

11:20 AM, VI.A.-5

A Coupled Schrödinger/Monte Carlo Technique for Quantum-Corrected Device Simulation: *Brian Winstead*¹; Umberto Ravaioli¹; ¹University of Illinois at Urbana-Champaign, Beckman Inst., Urbana, IL 61801 USA

11:40 AM, VI.A.-6

Quantitative Prediction of Threshold Voltage Fluctuations in Sub-100 nm MOSFETs by a New Dopant Model: *Hiroyuki Yamamoto*¹; Yos-himitsu Okada¹; Nobuyuki Sano¹; ¹University of Tsukuba, Inst. of Appl. Phys., 1-1-1 Tennoudai, Tsukuba, Ibaraki, 305-8573 Japan

Spin-Orbit Interaction of 2° in InAlAs/InAs Heterostructures

Kanji Yoh¹; Toshihiro Doi¹; Shin-ichiro Abe²; Yoshito Katano¹; Hiroshi Ohno²; Kazuhisa Sueoka²; Koichi Mukasa²; ¹Hokkaido University, RCIQE, N13, W8, Kita-ku, Sapporo, Hokkaido 060-8628 Japan; ²Hokkaido University, Grad. Sch. of Eng., N13, W8, Kita-ku, Sapporo, Hokkaido 060-8628 Japan

Spin-orbit interaction of electrons in surface inversion layers is known to be pronounced in mid-narrow gap semiconductors such as InAs or InSb. However, investigation of those materials suffer from substrate leakage current due to interband tunneling because of their narrow bandgap. Here we report the transport characterization of $\text{In}_{0.8}\text{Al}_{0.2}\text{As}/\text{InAs}$ heterostructures grown on p-type InAs substrate⁽¹⁾. Shubunikov de Haas oscillation of the InAs surface inversion layer was successfully measured by improved heterointerface quality and reduced interband tunneling current. As a result, spin-orbit interaction was estimated through Rashba oscillation. The heterointerface of arsenic-based material system was achieved by growing strained thin InAlAs barrier on top of undoped InAs channel layer. The molecular beam epitaxially grown heterostructure is composed of p⁺-InAs substrate, 1 μm of p-InAs buffer layer, 500Å of InAs and 80Å of InAlAs. The surface electrode of Ti/Au was deposited on top of the surface so that the ohmic contact to the surface inversion layer was taken through the tunneling barrier. The current voltage characteristics with wide voltage bias revealed that 2° saturation characteristics dominates at relatively low bias (-1V to +1V) and the substrate leakage current dominates at higher bias (>1.5V). At low current region, the Shubunikov de Haas oscillation was successfully obtained at 4K. The carrier concentration at the inversion layer was estimated to be $6.9 \times 10^{11} \text{cm}^{-2}$. The spin-orbit coupling constant⁽²⁾ of $\alpha_{\text{zero}} = 27 (\times 10^{-12} \text{eVm})$ or 12meV in spin split energy at Fermi level. The estimation decreases if we replace the effective mass of the bulk InAs value with higher value taking into account of the non-parabolicity of the energy band. However, the separate direct measurement of the spin split of the same sample exhibit band split energy of 14meV which is not so far from the estimation by Rashba oscillation. The present spin-orbit result is comparable to the number obtained in the strain relaxed $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}/\text{In}_{0.75}\text{Al}_{0.25}\text{As}$ heterostructure⁽³⁾. ⁽¹⁾ D.C. Tsui, Phys. Rev. B 4, 4438 (1971) ⁽²⁾ Th. Schaeppers et al, J. Appl. Phys. 83, 4324 (1998) ⁽³⁾ S. Yamada et al, 4th International Workshop on Quantum Functional Devices (Kanazawa, 2000)

Thermal Conductivity in Semiconductor Thin Films and Nanowires

Jie Zou¹; Alexander A. Balandin¹; ¹University of California at Riverside, Dept. of Electl. Eng., Riverside, CA 92521 USA

As the device feature dimensions continue to shrink toward nanometer scale, thermal properties of semiconductor low-dimensional structures are beginning to attract significant attention [1]. Downscaling trend in electronic and optoelectronic devices leads to an increase in power dissipation (per unit area) despite the reduction of the power supply voltage [2]. A variety of size effects that manifest themselves at nanoscale may adversely affect the removal of excessive heat. At the same time, these effects are very interesting from the fundamental-science point of view [3]. In this talk we present a self-consistent model for calculating the lattice thermal conductivity in semiconductor thin films and nanowires. The model is based on the solution of phonon Boltzmann equation. It rigorously takes into account modification of the acoustic phonon dispersion in low-dimensional structures with the lateral feature size of 10 nm - 30 nm, and change in the non-equilibrium phonon distribution due to partially diffuse scattering from rough boundaries and interfaces. It will be shown that the presence of distinctive boundaries in such structures leads to a transformation of the acoustic branches of phonon dispersion to quasi-optical branches characterized by a low group velocity and different cut-off frequencies. This transformation affects both in-plane and cross-plane thermal conduction in low-dimensional structures. In this talk we also analyze three-phonon Umklapp scattering processes in thin films and nanowires and compare them with those in bulk semiconductors. The predictions of the thermal conductivity values based on our model are in good agreement with available experimental data for silicon thin films and nanowires. The described changes in phonon transport in semiconductor thin films and nanowires bear important consequences for nanostructure and device simulation since neither Fourier heat theory nor Debye approximation are accurate at nanometer length scale. The observed modification of the thermal resistance of the low-dimensional structures has to be taken into account in simulation of thermal transport in deep-submicron devices since it strongly affects the electrostatic discharge voltage (EDS) and other reliability characteristics. The change in the acoustic phonon dispersion and group velocity may be partially responsible for the experimentally observed drop of EDS in devices based on thin-film silicon-on-insulator (SOI) wafers. [1]. G. Chen, *Int. J. Therm. Sci.* 39, 471 (2000) [2]. International Technology Roadmap for Semiconductor Industry, 1999. [3]. J. Zou and A. Balandin, Phonon heat conduction in a semiconductor nanowire, to appear in *J. Appl. Phys.*, 2001.

Quantum Mechanical Calculation of QCA Molecule Properties:

*Christopher J. Russo*¹; *Craig S. Lent*¹; ¹University of Notre Dame, Electl. Eng., 275 Fitzpatrick, Notre Dame, IN 46556 USA

Current computer architecture based on integrated silicon CMOS technology is rapidly approaching fundamental limits of scalability, primarily as a result of energy dissipation considerations. In the search for a new paradigm to achieve speeds and densities well beyond the foreseen limits of CMOS, a new model of device design using charge state and Coulomb interaction for information storage and propagation has been proposed. This paradigm of computation, based on Quantum Cellular Automata (QCA), provides a natural approach to the design of molecules that can encode and propagate binary information in their charge configurations. We investigate the properties of potential QCA molecules, using quantum mechanical calculations in the local density approximation. Specifically, the switching of a two-state cell with an appropriate driver charge is shown. Calculations of experimentally accessible molecular properties are investigated, and further details of molecular cell bistability are explored.

Nano-transistor modeling: Two dimensional Green's function method

A. Svizhenko, M. P. Anantram, T. R. Govindan and B. Biegel

NASA Ames Research Center, Mail Stop:T27A-1, Moffett Field, California 94035-1000, U.S.A

Two quantum mechanical effects that impact the operation of nanoscale transistors are inversion layer energy quantization and ballistic transport. While the qualitative effects of these features are reasonably understood, a comprehensive study of device physics in two dimensions is lacking (SIA Roadmap). Our work addresses this shortcoming and provides: (a) a framework to quantitatively explore device physics issues such as the source-drain and gate leakage currents, DIBL, and threshold voltage shift due to quantization, and b) a means of benchmarking quantum corrections to semiclassical models (such as density-gradient and quantum-corrected MEDICI).

We have developed physical approximations and computer code capable of realistically simulating 2-D nanoscale transistors, using the non-equilibrium Green's function (NEGF) method. This is the most accurate full quantum model yet applied to 2-D device simulation. Open boundary conditions and oxide tunneling are treated on an equal footing. Acoustic phonon scattering is included, causing transport to deviate from ballistic in a realistic manner. Electrons in the ellipsoids of the conduction band are treated within the anisotropic effective mass approximation. Self consistent solution of Poisson-NEGF equations is numerically intensive because of the number of spatial and energy coordinates involved. This makes the use of parallel/distributed computing imperative. For the self consistent calculations presented here, parallelization is performed by distributing the solution of NEGF equations to various processors, energy wise. The calculations were performed on a SGI Origin 2000 at the NAS computing facility located at the NASA Ames Research Center.

We present simulation results for the "benchmark" MIT 25nm and 90nm MOSFETs [1]. We compare our results (labeled "quantum") to those from the PROPHET (classical) drift-diffusion simulator (labeled "DD") and the quantum-corrected MEDICI results (labeled "Medici") available in [1]. In the 25nm MOSFET, the channel length is less than ten times the electron wavelength, and the electron scattering time is comparable to its transit time. Our main results are: (i) Simulated subthreshold and drain current characteristics are shown in Fig. 1 (a,b) where the potential profiles are calculated self-consistently by the corresponding simulation methods. The current predicted by our quantum simulation has smaller subthreshold slope of the V_g dependence which results in higher threshold voltage. (ii) Quantum mechanically calculated electron density is much smaller than the background doping density in the poly silicon gate region near oxide interface. This creates an additional effective gate voltage (Fig. 2). Different ways to include this effect approximately will be discussed. (iii) We have developed a method to calculate the gate-oxide leakage current (tunnel current) within the context of the NEGF method. Fig. 3 compares the drain and gate-oxide leakage current for the MIT 25 nm MOSFET, and for the same device with a 25nm gate length, for gate-oxide thickness of 1.5nm. There is an important difference in that the shorter gate length device has twenty times smaller current at zero gate bias than the longer gate length device, while the on-current at large gate voltages are comparable. This trend is true for a wide range of oxide thicknesses (Fig. 3 b) and should be a device consideration.

[1] *The well tempered MOSFET information at <http://www-mtl.mit.edu:80/Well>*

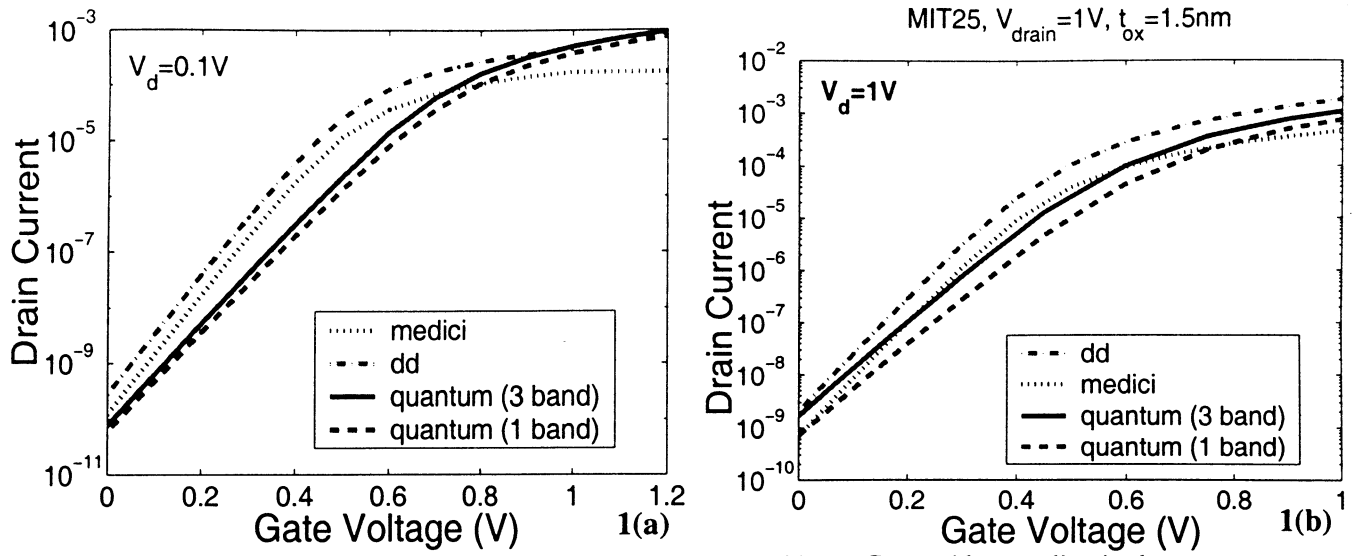


Fig.1. Drain current versus gate bias for (a) small and (b) large drain biases. Gate-oxygen tunneling is absent.

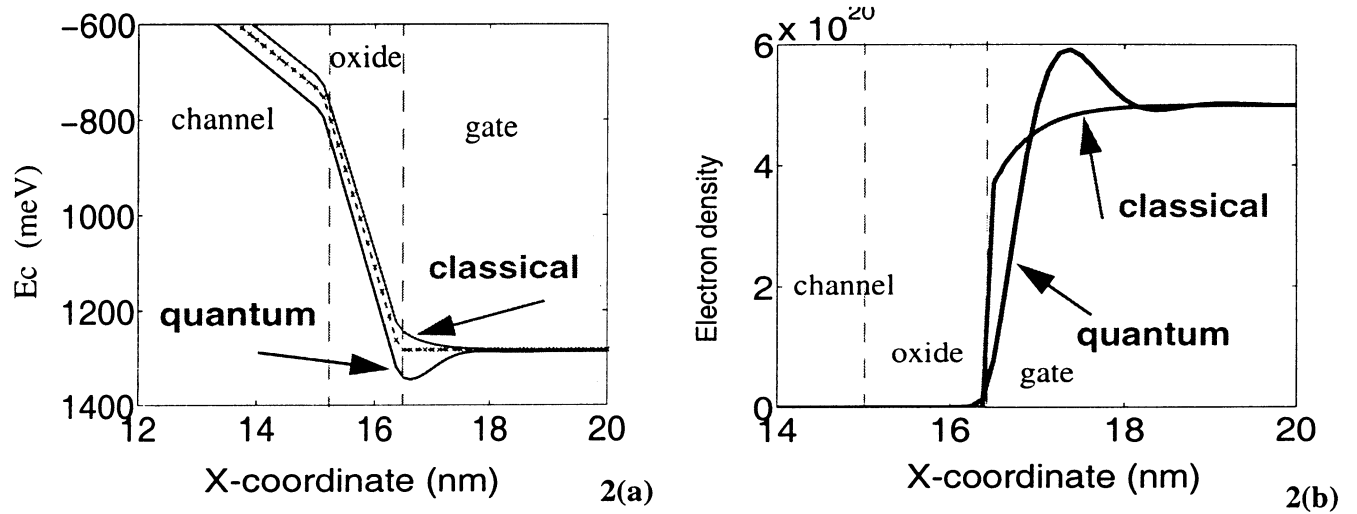


Fig. 2. Classical (DD) and quantum mechanically calculated potential profiles (a). The latter is lower than the former due to decay of electron density into the oxide (b).

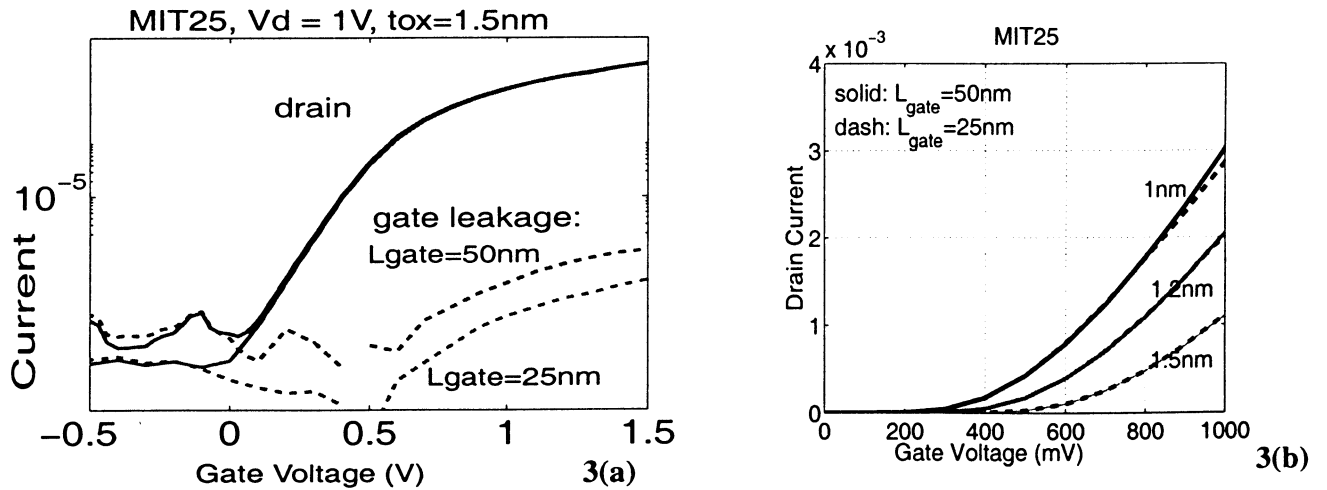


Fig. 3. Drain and gate leakage currents (a) for the MIT-25nm device with 25 and 50 nm gate lengths. Gate leakage is decreased by an order magnitude, while on-currents at $V_g = 1V$ are comparable (b).

A COUPLED SCHRÖDINGER/MONTE CARLO TECHNIQUE FOR QUANTUM-CORRECTED DEVICE SIMULATION

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As silicon MOSFETs are scaled below 100 nm, quantum effects become a critical consideration. The development of accurate and practical full quantum transport models for these devices is a daunting task. Fortunately, quantum coherence along the transport path is not expected to become significant for room temperature operation until extremely scaled lengths in the sub-10 nm regime. Thus for practical device simulation, a natural prescription is to try to retain the very mature semi-classical techniques as much as possible. To do this, the essential quantum effects such as tunneling and quantization can be captured as corrections to the semi-classical model. Physically based models such as full-band Monte Carlo are a useful starting point to add quantum corrections because they adequately describe the non-equilibrium and hot carrier phenomena which dominate today's devices, and can be used to calibrate lower levels of the simulation hierarchy such as drift-diffusion.

Quantum extensions to semi-classical simulation comprise an active area of research and recent Monte Carlo models have been developed based on approximations to the Wigner transport equation[1] and on the Feynman effective potential[2] In addition, quantum corrections based on approximate or exact 1-D Schrödinger solutions have been developed for drift-diffusion by several authors[3][4] Here we present a new model for quantum-corrected full-band Monte Carlo device simulation which accounts for quantum repulsion at the silicon/gate-insulator interface through a self-consistent coupling with the Schrödinger equation.

In a coupled Monte Carlo-Schrödinger simulation, the Schrödinger equation is periodically solved along 1-D slices of a 2-D domain. The quantum concentration slices are regarded as envelope functions for the Monte Carlo solution, and the Monte Carlo potential is corrected to reflect their shape. The correction is formulated in such a way that it is not a function of the particular magnitude of the quantum concentration, and thus there is no problem posed by the absence of the fermi level concept in a Monte Carlo model. In this work, the Monte Carlo-Schrödinger method is applied to a MOS capacitor for a wide range of biases, and is compared to self-consistent Schrödinger-Poisson calculations for validation. Preliminary results for a 2-D MOSFET simulation are also presented.

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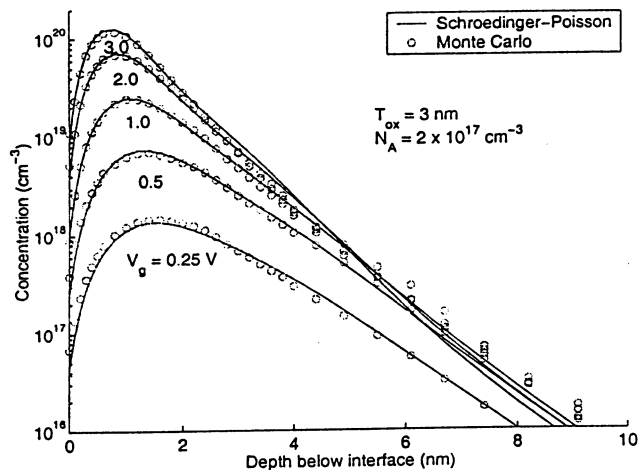


Figure 1: Electron concentration in an inverted MOS capacitor.

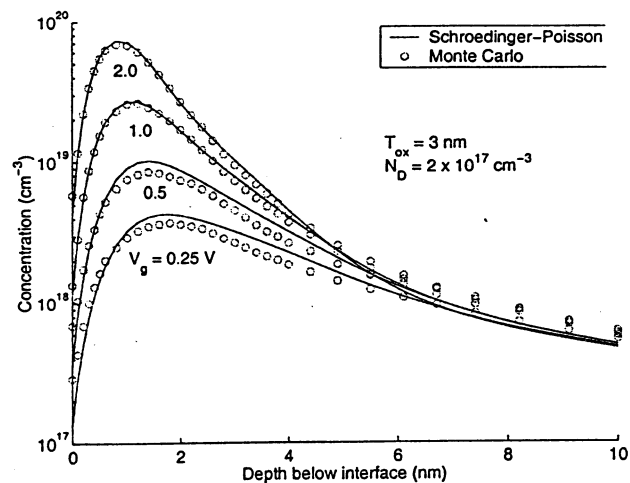


Figure 2: Electron concentration in an accumulated MOS capacitor.

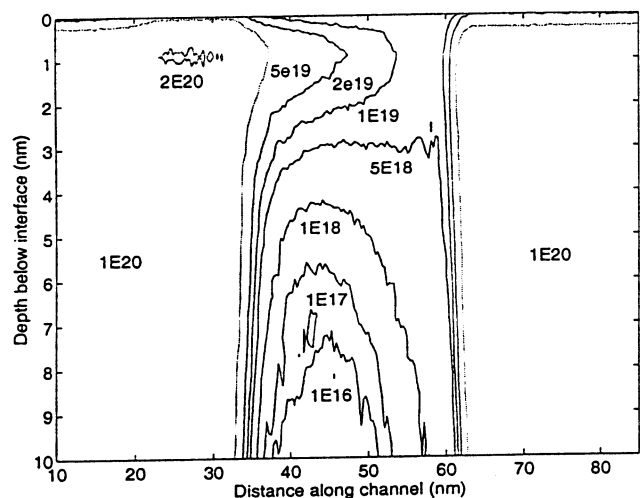


Figure 3: Electron concentration from a quantum-corrected Monte Carlo simulation of the MIT 25-nm "Well-Tempered" MOSFET (see <http://www-mtl.mit.edu/Well/>).

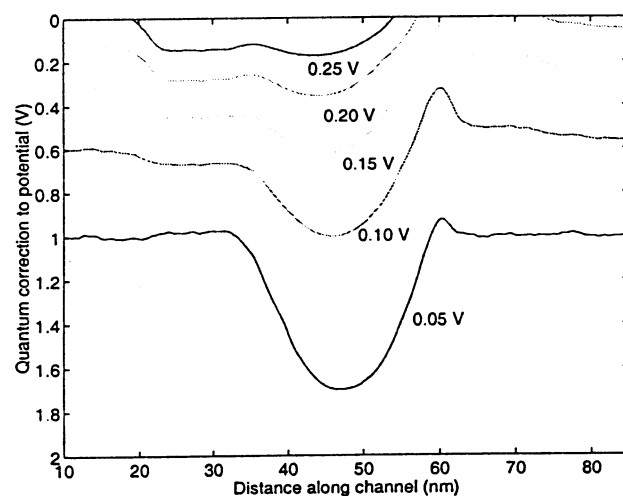


Figure 4: Quantum correction to the potential for the 25-nm MOSFET simulation.

Quantitative Prediction of Threshold Voltage Fluctuations in Sub-100 nm MOSFETs by a New Dopant Model

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1. Introduction

Threshold voltage (V_{th}) fluctuation associated with the discreteness of random dopants in the substrate is becoming a real and serious problem for future large-scale integrations of ultra-small MOSFETs. This problem has been theoretically investigated by the conventional 3-D and/or 2-D Drift-Diffusion (DD) simulations [1-3]. However, it has been pointed out that a naive application of the conventional dopant model to the extreme 'atomistic' situations, which is the case for most studies carried out so far, is physically incorrect and that the separation of the long-range and short-range parts of the Coulomb potential of the dopant is crucial in modeling the random discrete dopants [4]. Therefore, quantitative investigations of V_{th} variations with a reliable dopant model are of great importance. In the present paper, V_{th} fluctuations in sub-100 nm MOSFETs are studied in a predictable manner by employing a new dopant model that explicitly splits the long-range and short-range potentials of dopants.

2. Dopant Model and Simulation Method

A device structure employed for the present 3-D DD simulations is a simple n-MOSFET with (macroscopically) uniform acceptors (10^{18} cm^{-3}) and the oxide thickness of $t_{ox} = 2 \text{ nm}$. The DD simulator is conventional except the dopant model that explicitly incorporates the long-range part of the Coulomb potential and eliminates the short-range part [4], as schematically drawn in Fig. 1. It should be noted that the short-range part of the Coulomb potential represents the impurity scattering via screened dopants which is responsible to attain the local equilibrium and, thus, implicitly included in the current continuity equations in the DD simulator. In the present simulations, only acceptors in the substrate are treated as random dopants and the donors are treated as continuous jellium.

3. 3-D DD Simulation Results

In order to demonstrate the validity of the present dopant model, statistical analyses are carried out for relatively large MOSFETs with $L_g = 200 \text{ nm}$ and $W = 500 \text{ nm}$ so that the microscopic variations of electron current paths caused by the inhomogeneity of dopants are washed out. The simulation results are shown in Fig. 2, in which the I_d - V_g characteristics of 10 MOSFETs are plotted. The standard deviation $\sigma_{V_{th}}$ of V_{th} and the relative magnitude of the deviation with respect to V_{th} are, respectively, 5.5 mV and 1.8 %. The statistical fluctuation is very small and the off-currents I_{off} nearly coincide with the I_{off} characteristic of the 2-D simulation with uniform acceptor doping. Therefore, the present dopant model can correctly reproduce the previous simulation results for large devices in which the microscopic dopant variations in the substrate could be ignored.

Figure 3 shows the I_d - V_g characteristics of 100 MOSFETs with the gate length $L_g = 50 \text{ nm}$ and the device width $W = 50 \text{ nm}$. The spatial distribution of acceptors in each MOSFET is generated at random so that there is no correlation among the acceptors. Throughout this work, V_{th} is defined as the gate voltage at

which I_{off} is 10 nA. The standard deviation $\sigma_{V_{th}}$ is found to be about 33 mV, which is, *by accident*, similar to the values obtained from the previous 'atomistic' dopant approaches [2-3]. The relative magnitude of the deviation with respect to V_{th} is about 13 %. In practice, however, V_{th} variation is expected to be larger than this value because of the graininess of donors which also induces pn-junction fluctuations at the source and drain edges. Also, notice that I_{off} averaged over all discrete doping results does not show a large shift, but rather it is very close to that of 2-D DD simulation with uniform doping. This is a sharp contrast to the results previously reported. We believe that the present result is more reasonable because the dopant number in the substrate fluctuates around the expected value from the macroscopic dopant density and, therefore, there is no reason to expect that the averaged I_{off} deviates from that of the uniform doping. The histogram of the V_{th} deviation for the same 100 MOSFETs is shown in Fig. 4. The solid curve represents the Gaussian distribution with the standard deviation $\sigma_{V_{th}}$ found above and it approximates the simulation results quite well.

Figure 5 shows the correlation coefficients in MOSFETs with $L_g = 50 \text{ nm}$ and $W = 50 \text{ nm}$ between V_{th} and the dopant number N_d included in the channel regions underneath the gate oxide with the thickness of 5, 10, 35, and 100 nm. The correlation coefficient has a peak around 35 nm and this is consistent with the fact that the thickness of the depletion region is expected to be about 35 nm. The correlation plots between V_{th} and N_d in the channel regions are also shown in Fig. 6. Since V_{th} increases along with N_d , a slight positive correlation between V_{th} and N_d is observed in Fig. 6 (b), whereas no significant correlation in the other cases is found. The correlation in Fig. 6 (b) is, however, not quite strong compared with the spreading of the correlation plots.

4. Conclusions

Threshold voltage fluctuations in sub-100 nm MOSFETs have been investigated by the 3-D Drift-Diffusion simulations with a new dopant model that explicitly splits the long-range and short-range parts of the Coulomb potential of localized dopants. After demonstrating the validity of the present dopant model, the standard deviation of threshold voltages for sub-100 nm MOSFETs has been reliably estimated.

Acknowledgments

The authors would like to thank K. Matsuzawa, M. Mukai, and N. Nakayama for discussions. This work was supported in part by the Semiconductor Technology Academic Research Center (STARC).

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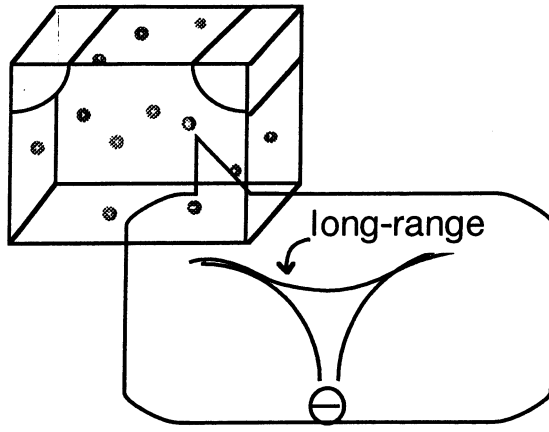


Fig. 1: Discrete dopant model used in DD simulations. The long-range-part of the Coulomb potential of each dopant is explicitly incorporated.

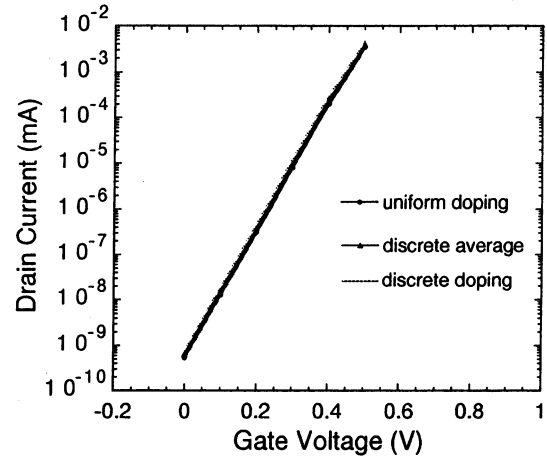


Fig. 2: Subthreshold characteristics of 10 MOSFETs with $L_g = 200$ nm and $W = 500$ nm obtained from the 3D-DD simulations with the present model. The solid line with dots represents the result from the conventional 2-D simulation with uniform doping.

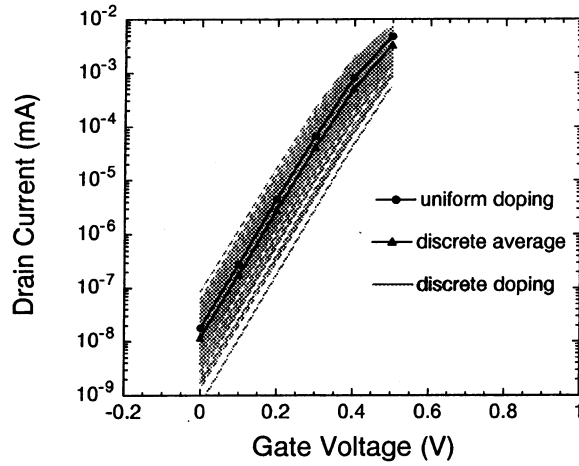


Fig. 3: Subthreshold characteristics of 100 MOSFETs with $L_g = 50$ nm and $W = 50$ nm obtained from the 3D-DD simulations with the present model. The solid line with dots represents the result from the conventional 2-D simulation with uniform doping.

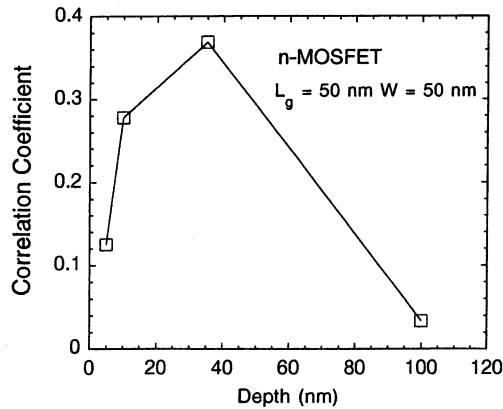


Fig. 5: Correlation coefficients between V_{th} and N_d in the channel regions underneath the gate oxide as a function of the depth from the oxide interface.

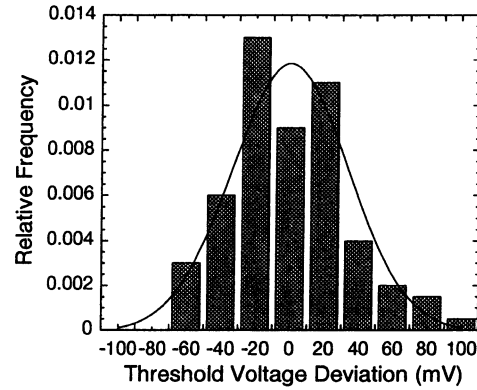


Fig. 4: Histogram of the V_{th} deviations of the same 100 MOSFETs in Fig. 3. The solid line represents the Gaussian distribution.

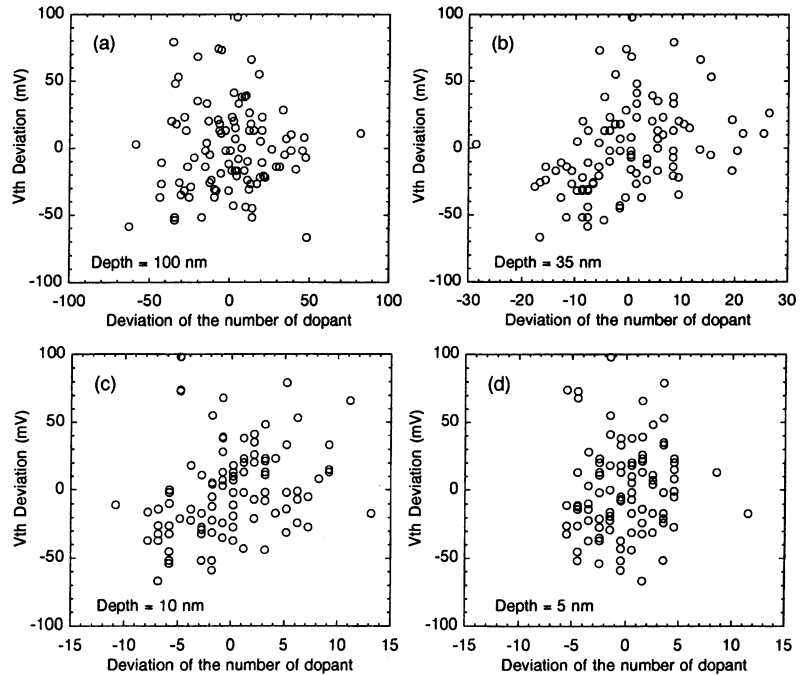


Fig. 6: Correlation plots between V_{th} and N_d in the channel regions underneath the gate oxide with the depths of (a) 100 nm, (b) 35 nm, (c) 10 nm, and (d) 5 nm.

Displays

WEDNESDAY AM, JUNE 27TH, 2001

Session Organizer: Tayo Akinwande, MIT

10:10 AM, VI.B.-1 Invited

High Gamma Coatings for Plasma Display Panels: A Comparison: *P. K. Bachmann*¹; V. Van Elsbergen¹; C. McGrath¹; ¹Phillips Research Laboratories, Weissshausstrasse 2, D-52066 Aachen, Germany

10:40 AM, VI.B.-2

Rare-Earth Doped GaN Electroluminescent Devices for Robust Flat Panel Displays: *J. Heikenfeld*¹; A.J. Steckl¹; ¹University of Cincinnati, Nanoelectronics Lab, Cincinnati, OH 45221-0030 USA

11:00 AM, VI.B.-3

Novel Three-Color Polymer Light-Emitting Devices for Passive-Matrix Flat Panel Displays: *Ke Long*¹; Min-Hao Lu¹; Florian Pschenitzka¹; J. C. Sturm¹; ¹Princeton University, Department of Electrical Engineering, Center for Photonics and Optoelectronic Materials (POEM), Princeton, NJ 08544 USA

11:20 AM, VI.B.-4

Flexible Liquid Crystal Displays Driven by Organic Thin Film Transistors on Polymeric Substrates: *C. D. Sheraw*¹; L. Zhou¹; J. R. Huang¹; L. Jia¹; J. A. Nichols¹; C. C. Kuo¹; D. J. Gundlach¹; T. N. Jackson¹; M. G. Kane²; I. G. Hill²; M. S. Hammond²; J. Campi²; B. K. Greening²; J. Franc³; J. West³; ¹The Pennsylvania State University, Center for Thin Film Devices, University Park, PA 16802 USA; ²Sarnoff Corporation, Solid State Display Laboratory, Princeton, NJ 08543 USA; ³Kent State University, Liquid Crystal Institute, Kent, OH 44242 USA

Invited Paper:

High Gamma Coatings for Plasma Display Panels: A Comparison

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D-52066 Aachen, Germany

Summary:

Today, plasma display panels (PDPs) are based on high-frequency dielectric barrier discharges that are ignited and maintained between electrodes that are embedded in glass [1]. The cross section of a typical discharge cell with a co-planar electrode arrangement is shown in Fig. 1 (left). Optimum performance, lifetime, and energy efficiency of such panels require optimization of the operating conditions of the dielectric barrier discharge. This includes minimization of the plasma firing voltages, maximization of UV-light generation and protection of the glass surfaces against plasma-induced damage. Minimization of the firing voltage requires coatings with a high ion-induced secondary electron emission coefficient (high gamma coefficient), i.e., surfaces that release as many electrons as possible per rare gas ion arriving at the plasma-solid interface [2]. Band-gap energy, electron affinity of the dielectric surface layer, as well as the ionization energy of the gas inside the discharge cells are relevant for the gamma coefficient [3]. Magnesium oxide is commonly applied as a high gamma protective coating inside PDP discharge cells. Because of their potentially low electron affinity, diamond and a number of other wide band-gap materials, e.g. AlN, ta-C or cBN are particularly interesting. Moreover, diamond is ideal for testing the influence of various parameters on ion-induced emission because it is fairly simple to change its electron affinity from negative (H-terminated) to positive (O-terminated) [4] and to study the corresponding gamma changes.

This contribution describes the basic operation principles of plasma display panels and the role of ion-induced secondary electron emission in igniting and sustaining plasmas in PDP cells. A reliable and reproducible method to measure gamma coefficients under panel-like conditions is explained [5]. Gamma measurements for polycrystalline MgO films [5], MgO single crystals [6], NEA and PEA diamond (Fig.1, right) [7], ta-C [7] and AlN are compared and discussed in the framework of a simple ion-induced electron emission model based on band-gap and electron affinity of the participating surfaces and on the ionization energies of the rare gases Ne, Ar, and Xe used in our experiments. The potential of diamond, AlN, and ta-C as PDP cell coating alternatives to MgO is discussed.

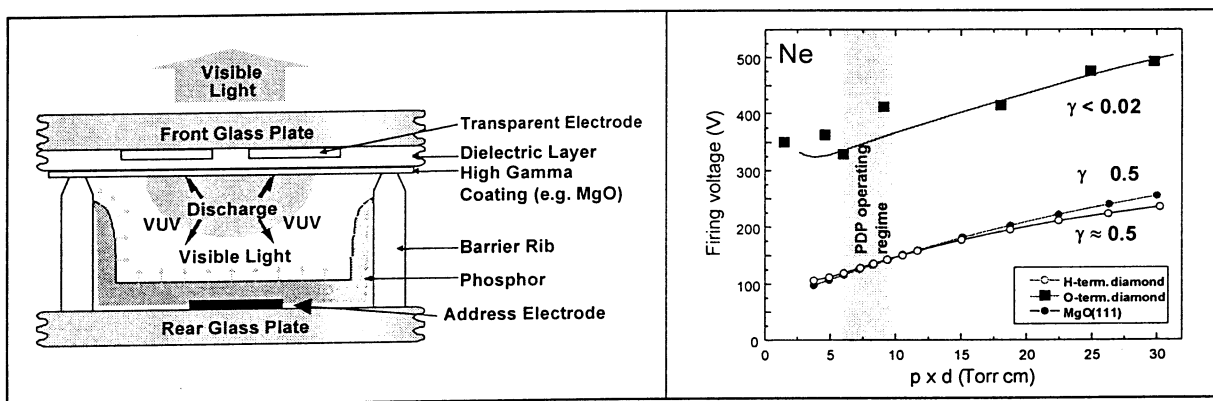


Fig. 1: Cross section of a plasma panel discharge cell (left) and measured firing voltages vs. pxd for H-terminated NEA diamond, O-terminated PEA diamond and a MgO (111) single crystal (right).

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Rare-Earth Doped GaN Electroluminescent Devices for Robust Flat Panel Displays

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Red, green, and blue light emission has been obtained from alternating current electroluminescent display devices (AC-ELDs) on Si and glass substrates using rare earth (RE)-doped GaN phosphors¹. The AC-ELDs are attractive for use in flat panel displays (FPDs) due to excellent emission chromaticity and a very simple device structures. These capacitive AC-ELD structures are biased with inexpensive (~\$2 US) drivers which supply high bipolar voltages (+/- 120-240 V) at low current (frequencies of 100Hz-1kHz) for loads up to 100's of nF (1-100 in² display size). GaN:RE phosphors deposited at < 600 °C are now compatible with standard flat panel display glass substrates. Furthermore, we have developed a novel fabrication technique which results in low-cost, high-yield, and high-capacitance (performance) AC-ELDs on glass substrates.

Ideal for a full-color FPD, AC-ELDs exhibit very narrow emission line-widths which are well-aligned with red, green, and blue color requirements. GaN:Eu AC-ELDs at peak wavelengths emit red light at 622 nm with a C.I.E chromaticity coordinates of (x=0.69, y=0.31), GaN:Er green at 537/558 nm (x=0.30, y=0.69), and GaN:Tm blue at 477 nm (x=0.10, y= 0.10). ELDs have also been developed with two phosphor layers doped with either Er or Eu. These dual phosphor devices have the capability of generating red, orange, yellow or green light by varying only the electrical bias conditions on a single electrode.

The devices show a much improved brightness of 3X-8X over previous reports. For example, GaN:Eu AC-ELDs exhibit a maximum red brightness of ~40 cd/m² at 1 kHz excitation. Alloying the GaN:RE phosphor with ~10% AlN is shown to further improve the device brightness by >30%. For phosphors with short emission lifetimes such as 537/538 nm emission from GaN:Er (~10 μs), the brightness increases linearly with frequency up to 10's of kHz. The GaN:RE phosphors are much more chemically stable (moisture resistant) than commercial ZnS-based phosphors. The GaN:RE phosphors exhibit optical turn-on voltages (<100 V) which are significantly lower than those of other chemically stable (oxide-based) phosphors (>200 V). Initial AC-ELD devices operated in a 40% humidity environment have exhibited 50% brightness decay lifetimes >1000 hours. Due to the chemical stability of a nitride-based phosphor, the GaN:RE AC-ELDs have the potential for extremely long operational lifetimes (> 50,000 hrs).

We will discuss the improvements required to make GaN:RE AC-ELDs overtake ZnS-based AC-ELDs and possibly other FPD devices. Similar to the potential of other AC-ELD technologies², advances in GaN:RE AC-ELDs could be strongly considered for applications such as flat TVs.

¹ A. J. Steckl, J. Heikenfeld, M. Garter, R. Birkhahn, and D. S. Lee, *Compound Semiconductor* 6 (1), 48 (2000).

² S. Grossman, *Electronic Design*, p. 25, May 1 (2000).

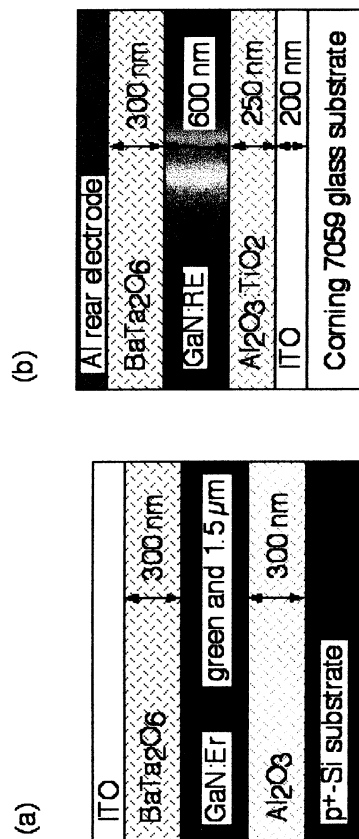


Fig. 1 Schematic diagrams of GaN:RE AC-ELDs formed on Si substrates (a) and glass substrates (b). The device in (a) can also be utilized as a 1.5 μ m emitter on Si.

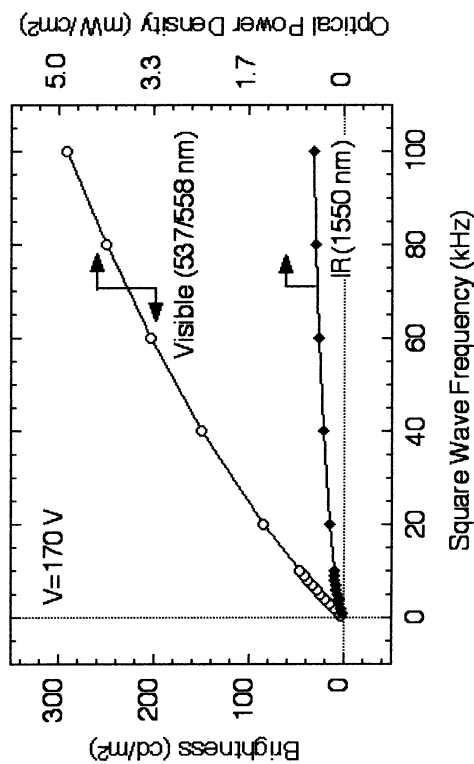


Fig. 3 Brightness (green emission at 537/558 nm) and optical power (green and IR emission at 1550 nm) from an AC-ELD operated at 170 V_p as a function of square wave frequency.

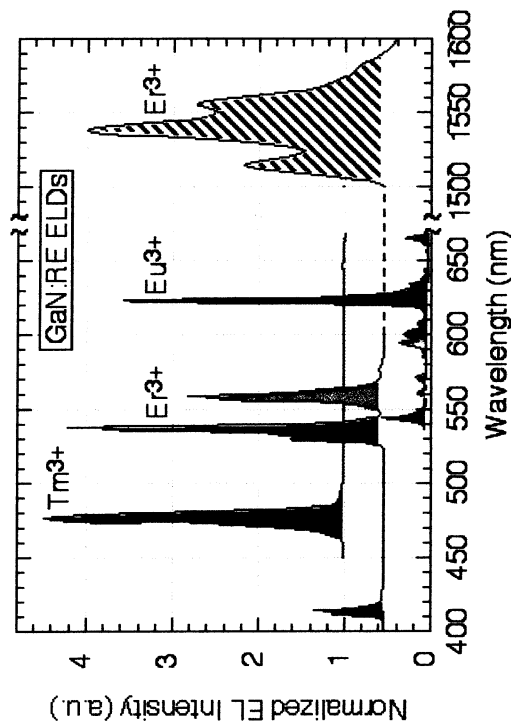


Fig. 2 The emission spectra of Tm, Er, and Eu-doped GaN ELDs showing the visible and IR wavelengths of interest.

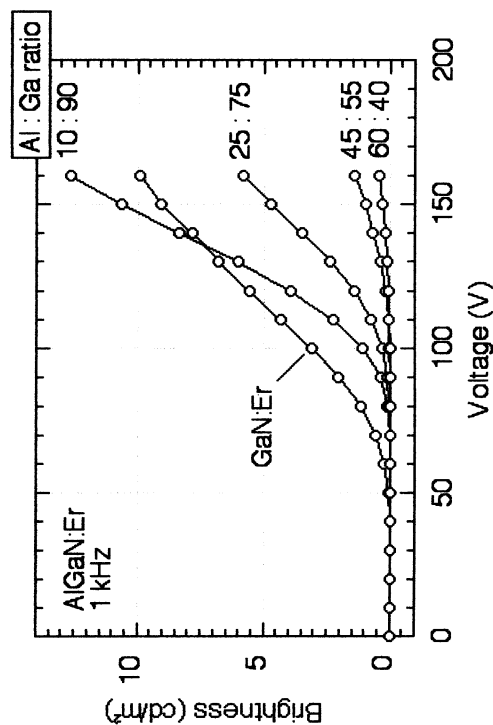


Fig. 4 Brightness vs. square wave voltage for a GaN:Er AC-ELD and AlGaIn:Er AC-ELDs.

Novel Three-Color Polymer Light-Emitting Devices for Passive-Matrix Flat Panel Displays

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With polymer-based organic LED's, patterning of the polymer to achieve color is a critical issue. A locally dye-doped polymer film is attractive for realization of multi-color devices on a single substrate. Different dyes may be locally added either by ink-jet-printing^{1,2} or by masked dye diffusion³ onto a previously spin-coated polymer film to get R,G,B subpixels. However, high leakage and low efficiency of these single-layer doped polymer LEDs limit their applications in passive matrix displays⁴. Both of these problems can be solved by adding an electron transport layer (ETL) over the polymer layer after dyes have been applied. The ETL Alq suppresses hole tunneling to reduce reverse leakage current, moves the cathode away from the emissive dyes to reduce cathode-quenching of the excitons via dipole interaction, and balances electron and hole transport to raise efficiency. However, due to the low exciton energy in the Alq ($E_{\text{exciton}}=2.3\text{eV}$), excitons formed in the polymer layer will migrate to the Alq layer, so that the dye in the polymer does not control the emission color (Figure 1,2(a)). In this paper, we introduce a thin exciton blocking layer (EBL) between the doped-polymer layer and the ETL, to confine the excitons within the polymer layer, yet still allow electrons to pass through, so that multi-color polymer-based devices can be realized (Figure 2(b)). The fabricated red, green, blue polymer LEDs using this novel tri-layer structure have higher efficiency and reverse leakage current two orders of magnitude lower than the single-layer devices.

The devices (Figure 2(b)) begin with a 100 nm thick polymer blend layer using poly(9-vinylcarbazole) (PVK) as a hole transport polymer, 2-(4-biphenyl)-5-(4-tert-butyl-phenyl)-1,3,4-oxadiazole (PBD) as an electron transport molecule and fluorescence dye (Nile red for red devices, Coumarin 6 for green devices, Bimane for blue devices) as an emission material, which is deposited on top of ITO layer by spin coating. A thin 6 nm 2,9-dimethyl-4,7-diphenyl-1,10-phenanthroline (BCP) layer as an exciton blocking layer ($E_g=3.6\text{eV}$) and a 40 nm thick 8-hydroxyquinoline aluminum (Alq) layer as an electron transport layer are deposited continuously by thermal evaporation. At last a 150 nm thick Mg:Ag (10:1)/Ag layer is deposited as the OLED cathode.

Figure 3 shows the electroluminescence spectra of the fabricated blue, green, and red tri-layer devices, with peak wavelengths of 436 nm, 500 nm and 590 nm respectively. Compared with the single-layer devices, there is negligible increase in operation voltage from the extra layers (Figure 4). The rectification ratio of the tri-layer devices, defined as the ratio of forward current to reverse current at the same bias, is improved drastically: For a bias of $\pm 10\text{V}$, the rectification ratio for the blue device is increased from $1.5\text{e}4$ to $2.4\text{e}6$; for the green device from $1.3\text{e}3$ to $1.3\text{e}6$; for the red device from $7.4\text{e}3$ to $8.7\text{e}5$. In addition to the high rectification ratio, the tri-layer devices have higher efficiencies than the single-layer devices (Table 1). In conclusion, we demonstrated three-color organic light-emitting devices with very high rectification ratio and improved quantum efficiency. The fabricated devices are well suited for full-color passive matrix OLED displays. Further research is being done in fabricating a full-color passive matrix display using these novel devices.

1. T. R. Hebner et al., *Appl. Phys. Lett.*, **73**, 1775 (1998)
2. J. Bharathan and Y. Yang, *Appl. Phys. Lett.*, **72**, 2660 (1998)
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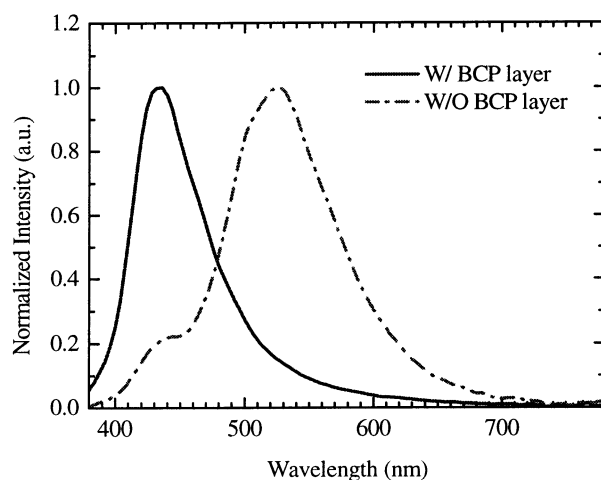


Figure 1. Spectra of the blue devices with and without exciton blocking layer BCP: without the BCP layer, Alq emission (peak @ 524nm, green) dominates; with the BCP layer, only Bimane emission (peak @ 436nm, blue) remains.

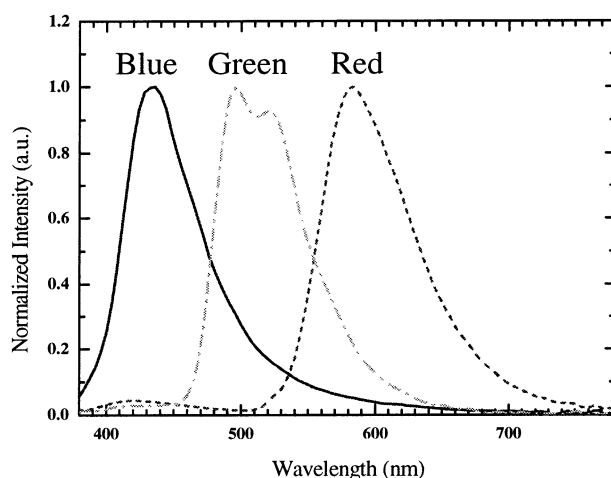


Figure 3. Electroluminescence spectra of the blue, green, and red tri-layer devices. Different emission colors depend on the corresponding dye dopants in the polymer layer: Blue: Bimane; Green: Coumarin 6; Red: Nile red

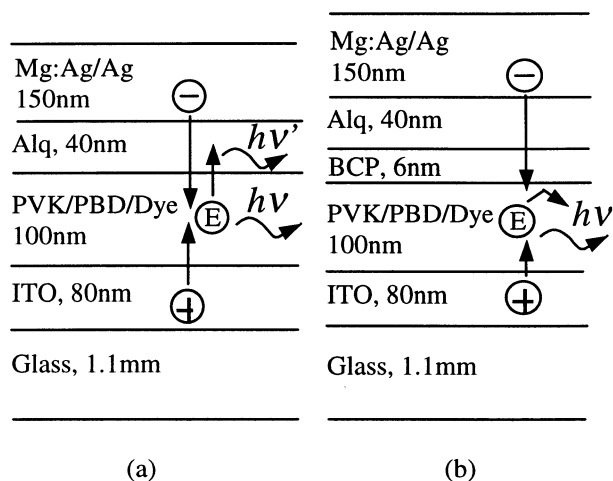


Figure 2. Schematic cross section of the OLEDs: (a) without EBL layer; (b) with EBL layer. Motion of the electrons, holes and excitons is shown.

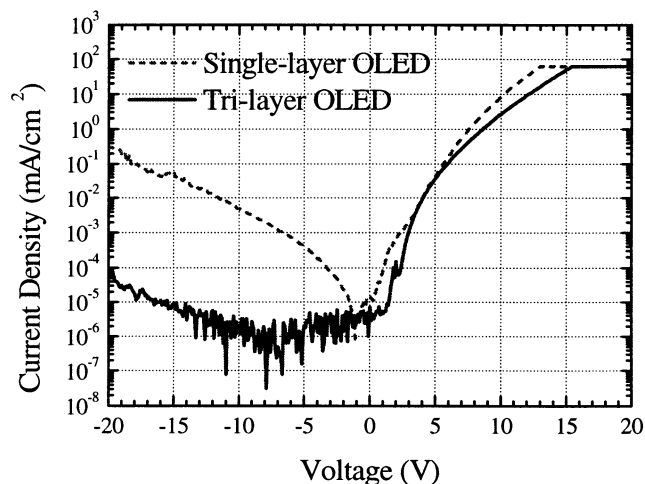


Figure 4. Typical I-V characteristics of the single-layer and tri-layer OLEDs

Table 1. Comparison of the single-layer and tri-layer devices

		Blue (Bimane)	Green (Coumarin 6)	Red (Nile red)
η_{ext} (%)	Single-layer	0.13%	0.70%	0.61%
	Tri-layer	0.34%	1.1%	0.95%
Rectification ratio @ $\pm 10\text{V}$	Single-layer	1.5e4	1.3e3	7.4e3
	Tri-layer	2.4e6	1.3e6	8.7e5

Flexible Liquid Crystal Displays Driven by Organic Thin Film Transistors on Polymeric Substrates

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Organic thin film transistors (OTFTs) have become very attractive for a variety of low-cost electronic applications such as smart cards, RF identification tags and flat panel displays. OTFTs have the inherent advantage that they can be processed at much lower temperatures than a-Si:H and poly-Si TFTs, making them compatible with inexpensive, lightweight, and flexible polymeric substrates. The integration of OTFTs with organic light emitting diodes or liquid crystals on polymeric substrates allows flexible active matrix displays. Recently, researchers at Philips Research Laboratories reported the first OTFT-driven liquid crystal display on a glass substrate [1]. We report here the first active matrix liquid crystal display fabricated using OTFTs on a flexible polymeric substrate.

Our display test chip was designed for use with polymer-dispersed liquid crystals (PDLC) and includes four types of 16×16 , 250- μm -pitch pixel arrays, with clear aperture between 38% and 58%, as well as analog and digital OTFT circuits, a 1- cm^2 200-OTFT parameter test array (density limited by test probe structure), and discrete OTFTs. The OTFT and pixel structure is shown in Fig. 1. Transparent, colorless polyethylene naphthalate (PEN) film, 125 μm thick, was used as the substrate. Prior to device processing, the PEN substrates were mounted to glass carriers for mechanical support and pre-shrunk at 150 °C for 2 hours to improve thermal dimensional stability; the maximum temperature used for device processing is 110 °C. Nickel was used as the gate electrode. A bilayer consisting of room-temperature PECVD deposited silicon nitride and a low-temperature ion-beam deposited silicon dioxide was used as the gate dielectric to improve crossover yield. Palladium was used for the source/drain contacts and transparent indium tin oxide (ITO) was used for the pixel electrode. The pentacene organic active layer was deposited by thermal evaporation at a rate of ~ 0.5 Å/s. During pentacene deposition, the substrate was held at 60°C to improve molecular ordering in the pentacene film for increased carrier mobility and improved device characteristics. The silicon dioxide gate dielectric surface was vapor-treated with octyldecyltrichlorosilane prior to pentacene deposition. After deposition, the pentacene active layer was patterned using a water-based photosensitized polyvinyl alcohol (PVA) photolithographic process. An additional layer of PVA was used to protect the organic TFTs from the liquid crystal and polymer materials. Fig. 2 shows a completed display test chip before liquid crystal assembly. Test displays were completed using optically-cured PDLC, 16 μm plastic spacers, and ITO coated Mylar[®] film. Fig. 3 shows a pixel array with $> 98\%$ pixel yield displaying two fixed patterns. The display was operated using QVGA display waveforms with data voltages of $\pm 20\text{V}$ at 30Hz, a select voltage of -30V, and a deselect voltage of +25V, with a 69 μs line time.

Discrete OTFTs, the 200 OTFT array, and OTFT circuits were measured prior to display assembly. Electrical TFT performance is the best reported to date for OTFTs on flexible substrates. Discrete devices have carrier field-effect mobility as large as 1.2 $\text{cm}^2/\text{V}\cdot\text{s}$ and on/off current ratio $> 10^7$. Fig. 4 shows the electrical characteristics of a discrete pentacene TFT on PEN film with channel width of 200 μm , channel length of 10 μm , and oxide thickness of 450 nm. Results from the 200 OTFT array show high device yield ($> 99\%$) and excellent uniformity with 0.81 $\text{cm}^2/\text{V}\cdot\text{s}$ average mobility and +1.8V average threshold voltage and standard deviations of 0.05 $\text{cm}^2/\text{V}\cdot\text{s}$ and 0.8 V for mobility and threshold voltage, respectively. OTFT ring oscillators with propagation delay < 40 μs /stage and frequency dividers operating at a clock frequency of 1.1kHz were also measured.

[1] Philips Research Laboratories, "Plastic transistors drive for 64×64 -pixel display," EETIMES.com, URL: <http://www.eetimes.com/story/OEG20000911S0037>, Sept. 11, 2000.

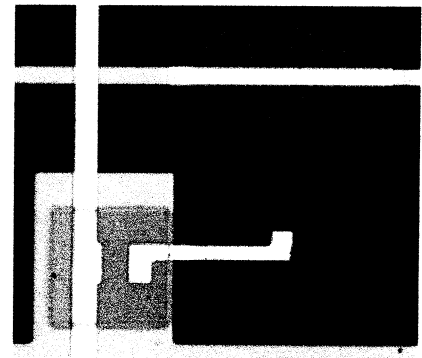
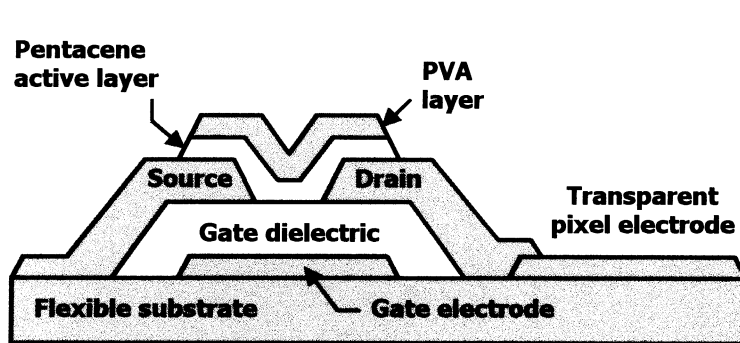


Fig. 1. Cross section (left) and optical micrograph (right) of an AMLCD pixel with pentacene TFT on flexible polyethylene naphthalate (PEN) film.



Fig. 2. OTFT test chip on PEN film before display assembly.

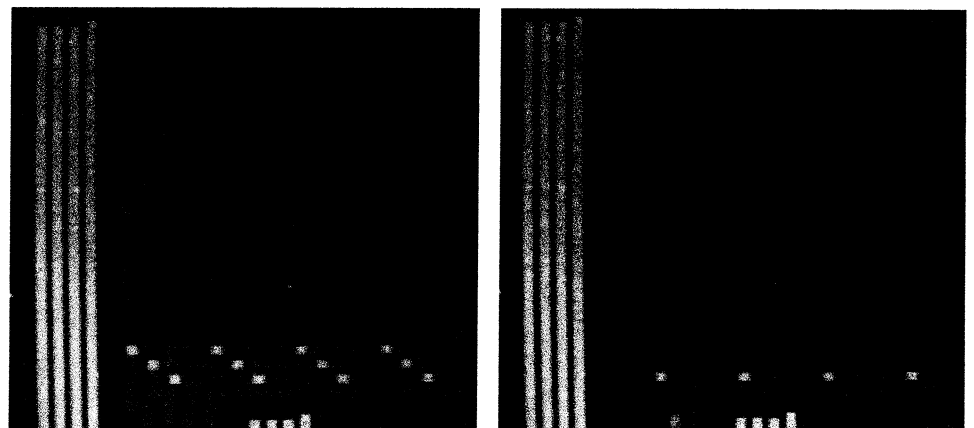


Fig. 3. Pentacene OTFT-driven 16×16 pixel active matrix PDLC display on flexible PEN film.

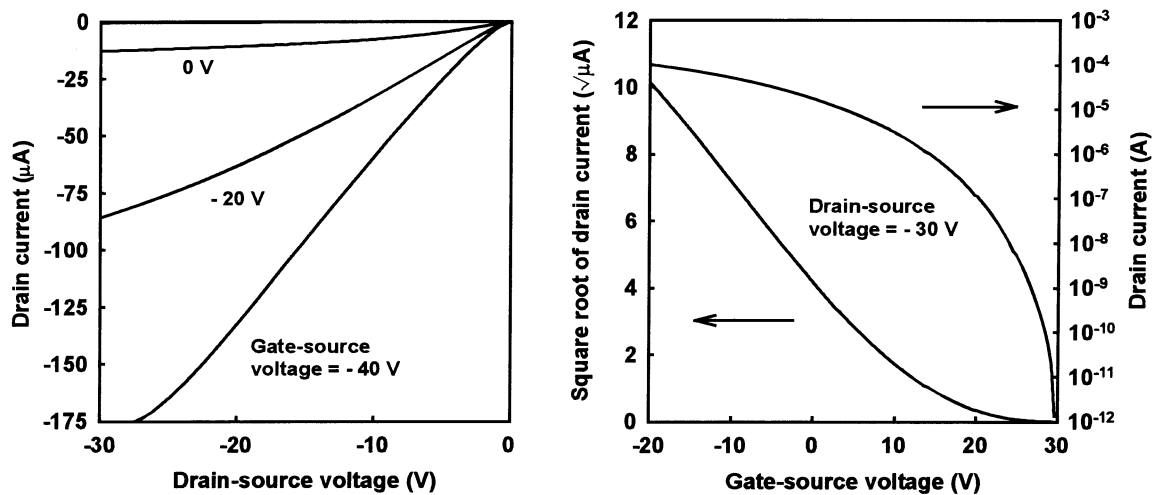


Fig. 4. Electrical characteristics of a pentacene TFT on flexible PEN film.

TFTs

WEDNESDAY PM, JUNE 27TH, 2001

Session Organizer: Hagen Klauk, Infineon Technologies

2:00 PM, VII.A.-1 Invited

Organic-Inorganic Electronic Devices Based on Hybrid Perovskites: *D. B. Mitzi*¹; C. D. Dimitrakopoulos¹; L. L. Kosbar¹; ¹IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA

2:30 PM, VII.A.-2

CMOS Polysilicon Circuits on Flexible Steel Substrates: *Ming Wu*¹; Sigurd Wagner¹; ¹Princeton University, Department of Electrical Engineering, Princeton, NJ 08544 USA

2:50 PM, VII.A.-3

High-Performance Thin-Film Transistor Fabricated on Poly-Si Films Prepared by Metal Imprint Technology: *Kenji Makihira*¹; Masahito Yoshii¹; Tanemasa Asano¹; ¹Kyushu Institute of Technology, Center for Microelectronic Systems, 680-4 Kawazu, Iizuka, Fukuoka 820-8502, Japan

3:10 PM, VII.A.-4

Excimer Laser Annealed, Poly-Si Thin Film Transistors for Flat Panel Imager Application: *J. P. Lu*¹; K. Van Schuylenbergh¹; J. Ho¹; Y. Wang¹; P. Nylén¹; J. B. Boyce¹; R. A. Street¹; ¹Xerox Palo Alto Research Center, 3333 Coyote Hill Road, Palo Alto, CA 94304 USA

3:30 PM Break

3:50 PM, VII.A.-5

Amorphous Si TFTs on Plastically-Deformed Substrates with 3-D Shapes: *P. I. Hsu*¹; H. Gleskova¹; Z. Suo¹; S. Wagner¹; J. C. Sturm¹; ¹Princeton University, Center for Photonics and Optoelectronic Materials (POEM), Princeton, NJ 08544 USA

4:10 PM, VII.A.-6

Gate Control in Ultra-Short Channel Double-Gate MOSFETs Accounting for 2D and Quantum Confinement Effects: *M. Mouis*²; F.-N. Genin¹; A. Poncet¹; ¹Laboratoire de Physique de la Matière, UMR-CNRS n° 5511, INSA-Lyon 20, Avenue Albert Einstein, F-69621 Villeurbanne, France; ²CEA-Grenoble, LETI/DTS/CPMA, 17 rue des Martyrs, 38054 Grenoble Cedex 9 France

Organic-Inorganic Electronic Devices Based on Hybrid Perovskites

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Organic-inorganic materials enable the integration of useful organic and inorganic characteristics within a single molecular-scale composite. Organic materials have the key advantage of potentially simple and low-temperature thin-film processing using techniques such as spin coating, ink jet printing or stamping. In addition, the flexibility of organic chemistry enables the formation of organic molecules with useful luminescent and conducting properties. Inorganic materials enable the design of materials with better thermal / mechanical stability and higher electrical mobility, as a result of the stronger covalent and ionic bonding. Combining these and other characteristics within a molecular-scale composite is expected to provide unique opportunities for electronic device components [1].

Hybrid perovskites [2] are one interesting family of crystalline organic-inorganic hybrid, combining extended metal halide sheets with layers of organic cations (Figure 1). In the current systems, the metal halide sheets consist of two-dimensional networks of corner-sharing tin(II) or lead(II) halide octahedra, while the organic cations are protonated aromatic amines. An organic-inorganic light-emitting device (OLED), based on a hybrid perovskite with dye-containing organic cations and lead(II) halide inorganic sheets, has recently been reported [3]. An organic-inorganic thin film transistor (OITFT) has also been demonstrated [4], employing the hybrid perovskite $(\text{C}_6\text{H}_5\text{C}_2\text{H}_4\text{NH}_3)_2\text{SnI}_4$ as the channel material. The organic-inorganic hybrid channel enables the integration of simple processing (self assembly) associated with organic materials and the higher carrier mobilities of inorganic compounds.

The first hybrid perovskite OITFTs provided mobilities of $\sim 0.6 \text{ cm}^2/\text{V}\cdot\text{sec}$ (comparable to that of a-Si) and the ability to solution process the channel layer at near ambient temperatures [1,4]. In the current study, by further refining the device preparation, we demonstrate saturation-regime mobilities as high as $1.4 \text{ cm}^2/\text{V}\cdot\text{sec}$ (Figure 2). An on-off ratio of $>10^5$ and current densities of $>400 \text{ A}/\text{cm}^2$ can regularly be achieved. The field-dependence of the mobility is, however, substantial in the spin-coated perovskite channels, presumably as a result of traps within the hybrid [5]. The electronic properties of the hybrid semiconductor making up the channel layer in the OITFTs can be fine-tuned using the organic cation layer. This control arises from the steric constraints provided by the organic molecule and the specific hydrogen bonding interaction between the organic cation and the inorganic framework [6]. One example of this control is provided by a series of tin(II) iodide-based hybrids with fluorine-substituted phenethylammonium cations [6]. The position of the fluorine substitution on the phenyl ring is used to control the optical and electrical properties of the hybrid (Figure 3). In addition, we are exploring the electronic properties of hybrid perovskites with a larger number of inorganic sheets sandwiched between the organic layers [7] to see if better device characteristics can be achieved.

In summary, the organic-inorganic perovskites provide an ideal opportunity to combine useful properties in a hybrid composite that can be processed using simple solution or evaporation-based thin film techniques. Since these techniques are performed at ambient temperature, it is envisioned that the hybrid materials are likely to be compatible with a range of potential applications, including those that may require flexible plastic substrates. Besides the OITFT and OLED devices discussed here, organic-inorganic hybrids may also provide novel possibilities for thermoelectric, dielectric, photoconductive and magnetic applications. In each case, the possibilities afforded by the hybrid systems are only beginning to be considered.

[1] D. B. Mitzi, K. Chondroudis, C. R. Kagan, *IBM J. Res. Develop.* **45**, 29 (2001).

[2] D. B. Mitzi, *Prog. Inorg. Chem.* **48**, 1 (1999).

[3] K. Chondroudis, D. B. Mitzi, *Chem. Mater.* **11**, 3028 (1999).

[4] C. R. Kagan, D. B. Mitzi, C. D. Dimitrakopoulos, *Science* **286**, 945 (1999).

[5] Dimitrakopoulos, C. D.; Purushothaman, S.; Kyymissis, J.; Callegari, A.; Shaw, J. M., *Science* **283**, 822 (1999).

[6] D. B. Mitzi, C. D. Dimitrakopoulos, L. L. Kosbar, *Chem. Mater.*, submitted.

[7] D. B. Mitzi, C. A. Feild, W. T. A. Harrison, A. M. Guloy, *Nature* **369**, 467 (1994).

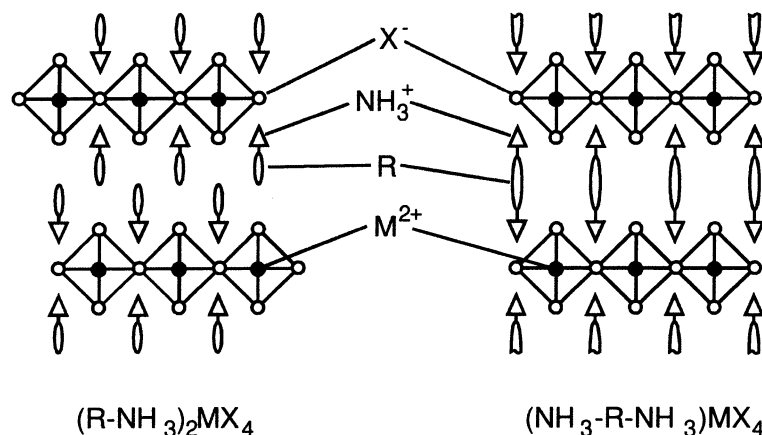


Figure 1. Schematic representation of single-layer hybrid perovskites with monoammonium (R-NH_3) or diammonium ($\text{H}_3\text{N-R-NH}_3$) cations. In each case, “R” represents an organic moiety and “X” is a halogen.

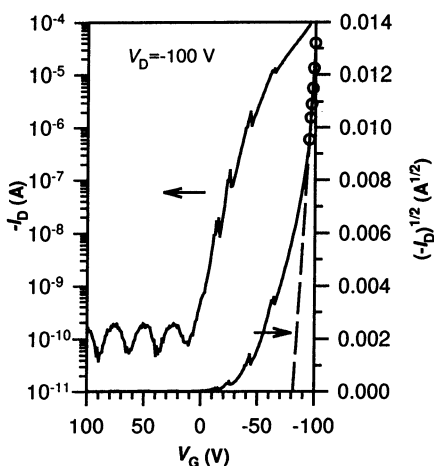


Figure 2. Plots of I_D and $I_D^{1/2}$ versus V_G at constant $V_D = -100$ V, used to calculate current modulation, $I_{\text{on}}/I_{\text{off}}$, and field-effect mobility, μ , for a TFT with a spin-coated (phenethylammonium) $_2\text{SnI}_4$ channel of length $L = 15.4$ μm and width $W = 1500$ μm . The gate dielectric is 5000 Å of SiO_2 .

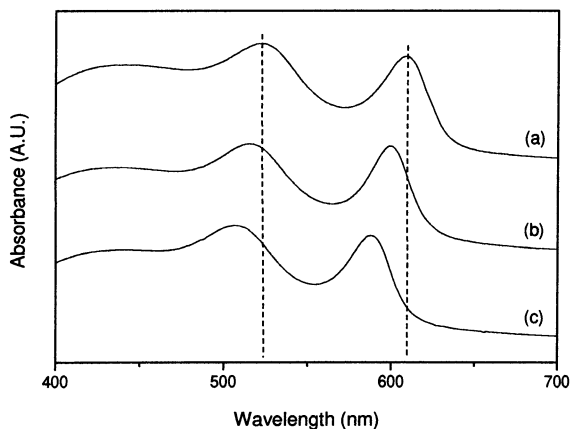


Figure 3. Room temperature UV-vis absorption spectra for spin-coated thin films of (a) (4-fluorophenethylammonium) $_2\text{SnI}_4$, (b) (3-fluorophenethylammonium) $_2\text{SnI}_4$, and (c) (2-fluorophenethylammonium) $_2\text{SnI}_4$. The dashed lines are guides for the eye to highlight the shift in position of the band edge and exciton peak for each system.

CMOS Polysilicon Circuits on Flexible Steel Substrates

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We present results of a new technique for fabricating polycrystalline silicon (polysilicon) circuits on a flexible substrate. The polysilicon film is formed by thermally annealing amorphous silicon films deposited on steel foil substrates. The high temperature tolerance of steel allows furnace crystallization at 750°C in 2 minutes.

Figure 1 shows the self-aligned TFT structure. 200 μ m thick stainless steel was planarized with spin-on-glass and plasma enhanced chemical vapor deposited (PECVD) silicon oxide without prior finishing. A precursor amorphous silicon (a-Si:H) film was deposited by PECVD at 150°C, and then annealed in a furnace at 750°C for 2min. The polysilicon layer then was defined into individual TFT islands by Reactive Ion Etching (RIE). 150nm SiO₂ and 200nm intrinsic a-Si:H were deposited by PECVD at 350°C and 250°C as gate dielectric and gate electrode. The a-Si:H was patterned by RIE to form the eventual gate, SiO₂ was wet etched to open source and drain, boron/phosphorus was implanted into source and drain for p-/n- channel TFTs respectively, and implant damage was annealed out at 700°C for 30 minutes. 1-hour hydrogenation at 350°C was used to passivate defects. 200nm passivation SiO₂ was deposited by PECVD at 250°C, contact holes were opened by wet etch, and 200nm Al was thermally evaporated and patterned into gate and source/drain electrodes and interconnections. Finally the transistors were annealed in forming gas at 250°C for 30minutes.

Figure 2 shows the transfer characteristics of p- and n- TFTs made with polysilicon on steel. Both transistors have well-behaved electrical properties. The ON currents at $V_{GS} = 40V$ and $V_{DS} = 5V$ are in the ~10mA range for both transistors. The hole and electron mobilities in the linear regions are 11 and 16 cm²/Vs, the off currents of p- and n- channel TFTs are 1.2pA/ μ m and 23pA/ μ m of channel width, and the drain current ON/OFF ratios are 10⁷ and 10⁶ for p- and n- channel TFTs, respectively.

Figure 3 shows the output curve of a CMOS polysilicon inverter on steel. Here, the p- and n- channel TFTs have channel width $W = 60\mu$ m and length $L = 6\mu$ m. Both the output voltage and power are plotted vs. input voltage. Supply HIGH voltage V_{DD} was set from 10V to 26V with supply LOW voltage $V_{GND} = 0$. This inverter shows a full rail-to-rail swing and a full-range abrupt voltage transfer characteristic with a gain of ~25 at $V_{DD} > 18V$. The maximum output power $P_{MAX} = 18\mu$ W at $V_{DD} = 26V$.

Figure 4 shows the characteristic of a CMOS inverter operating at 1MHz at a supply voltage $V_{DD} = 30V$. This inverter is composed of n- and p- channel TFTs with channel width $W = 60\mu$ m and length $L = 2\mu$ m. The fall and rise times are 270ns and 322ns (90% peak-peak amplitude swing), respectively. These values are consistent with the RC time constant of the transistor and a 1pF parasitic capacitance, which is the capacitance of the output metal pad to the steel substrate. Figure 5 shows the output signal from a 5-stage CMOS ring oscillator oscillating at 1.03MHz at a supply voltage $V_{DD} = 30V$. The p- and n- channel TFTs have channel width $W = 60\mu$ m and length $L = 4\mu$ m.

These complementary polysilicon thin film transistor circuits on steel foil demonstrate a new route to large-area, flexible TFT backplanes with the performance required for driver circuits of displays, sensor arrays, and mechatronic materials.

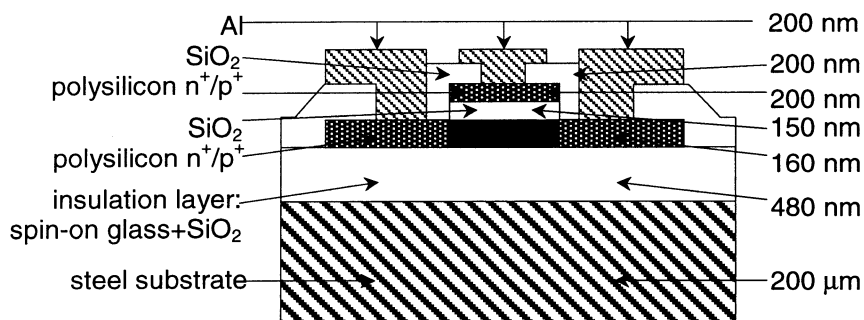


Figure 1. Schematic cross-section of self-aligned polysilicon TFT on steel.

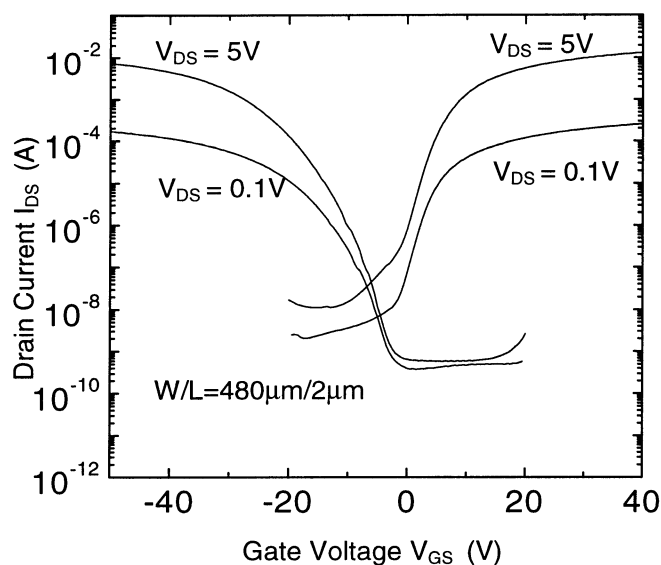


Figure 2. Transfer characteristics of n- and p- channel polysilicon TFTs on steel.

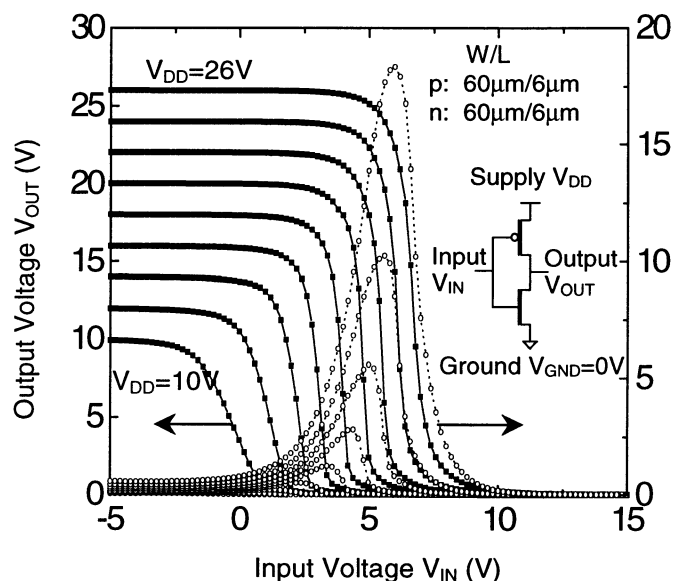


Figure 3. Output characteristics of CMOS polysilicon inverter on steel.

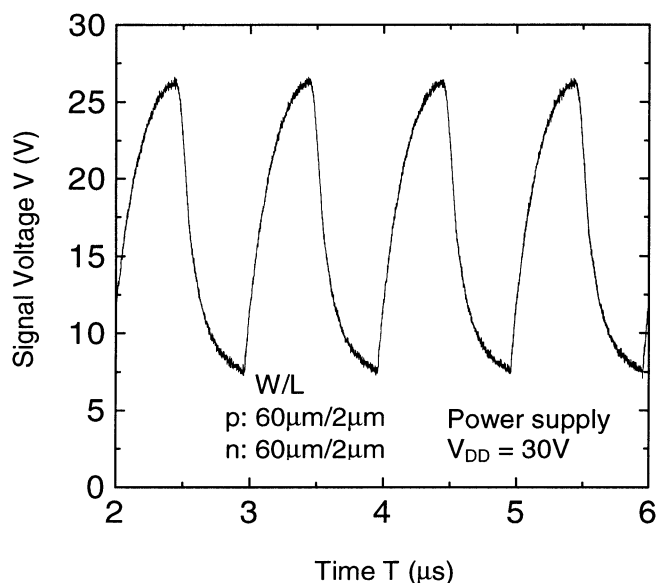


Figure 4. CMOS polysilicon inverter on steel operating at 1 MHz.

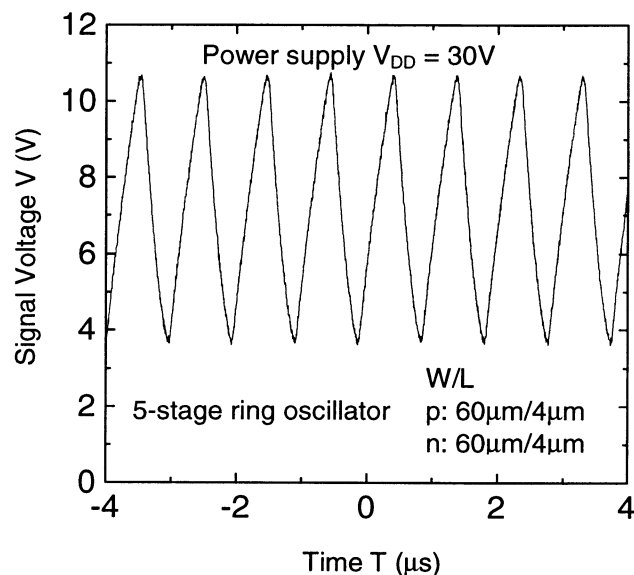


Figure 5. 5-stage CMOS polysilicon ring oscillator oscillating at 1.03 MHz.

High-Performance Thin-Film Transistor Fabricated on Poly-Si Films Prepared by Metal Imprint Technology

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1. Introduction

One promising approach for fabricating high-performance poly-Si TFTs is to place entire channel within a single grain of poly-Si films. To realize these devices, large grains must be formed at controlled positions. In solid phase crystallization (SPC) of amorphous Si, there have been proposed methods such as ion implantation¹⁾ and metal imprint technology²⁾ to induce nucleation at desired sites. In this work, we demonstrate TFTs fabricated in single-grains of poly-Si films prepared by the metal imprint technology. It is shown that the single-grain TFTs have superior performance in terms of switching behavior and uniformity in characteristics to those fabricated on conventional SPC poly-Si films.

2. Experiments

Process sequence of imprint method is as follows. A tip-array coated with a Ni film is faced down to an a-Si film and pressed at the pressure of about 0.15MPa. After removing the tip-array substrate, a-Si is annealed to crystallize at 560°C or 590°C in an N₂ ambient.

Al-gate n-channel TFTs were fabricated and characterized. In order to place TFT channel region within the single grain, the position of imprinted grains and the positions of channels were aligned each other (Fig. 1). Gate length and gate width were 5 μ m and 5 μ m. Source/drain was formed by phosphorus ion implantation. Gate oxide was formed using dry oxidation and its thickness was 40nm. The thickness of active layer was 80nm. No plasma hydrogenation was performed to characterize intrinsic performance of TFTs.

3. Results and Discussion

Figure 2 shows a SEM image of a Si film imprinted with the Ni-coated tip array and annealed at 590°C for 7 hours. We can see that crystal grains appear only at the sites imprinted with the tips which was arrayed in a square grid pattern. From the results of TEM observation, the grain is found to be <111>-oriented single crystal. We have observed many grains induced by the Ni imprint. Almost all of the grains were <111>-oriented single crystal.

The results of isothermal annealing experiments (Fig. 3) clearly demonstrate that, with the Ni imprint, nucleation takes place almost coincidentally at the imprinted sites, while the conventional SPC is a result of spontaneous nucleation. The grain growth rate and TEM results indicate that the growth mechanism of the imprint technology is different from the metal-induced lateral crystallization.³⁾ The average grain sizes obtained with Ni imprint by annealing at 560°C and 590°C were 10 μ m and 5 μ m, respectively.

The transfer characteristic of TFTs fabricated using the imprint technology was superior to those of TFTs fabricated on poly-Si films grown by the conventional SPC in terms of on-current, subthreshold swing and cut-off current (Fig. 4). We have not observed any detrimental effect of the use of Ni. Carrier mobility analysis was performed on a number of TFTs. The results clearly demonstrated that mobility of Ni-imprinted TFTs is higher than that of the conventional-SPC TFTs. The field effect mobility up to about 400cm²/V-s was obtained when TFT was fabricated in a single-grain grown using the Ni-imprint at 560°C (Fig. 5).

In case of TFTs fabricated on Ni-imprinted poly-Si films, we observed that the mobility increases with decreasing annealing temperature. As mentioned above, the average grain size (10 μ m) of Ni-imprinted poly-Si films grown at 560°C is large enough to cover the whole channel, while the average grain size (5 μ m) of films grown at 590°C suggests that most of TFTs fabricated in the films contains grain boundaries in the channel region. These results indicate that the presence of grain boundaries in the channel significantly degrades the mobility of n-channel TFT.

The dispersion in threshold voltage and subthreshold slope of Ni-imprinted TFT was about half that of the conventional-SPC TFTs. The dispersion in mobility was, however, not improved significantly. This is considered to be owing to the fact that distribution in grain size becomes large with increase in grain size.

4. Conclusion

In conclusion, the metal imprint technology is effective in preparation of large Si grains at controlled sites. n-channel TFTs fabricated on poly-Si film grown at 560°C showed the field effect mobility up to 400cm²/V-s. The uniformity in characteristics is improved by fabricating the channel in a single-grain. The results suggest that performance of TFTs can be further improved by reducing crystalline defects in grains.

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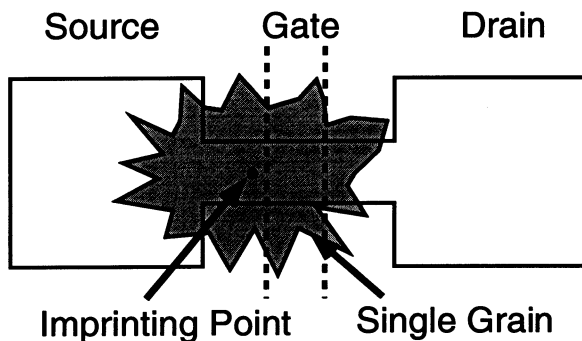


Fig. 1. The relative position between the TFT channel region and the Ni imprinted point.

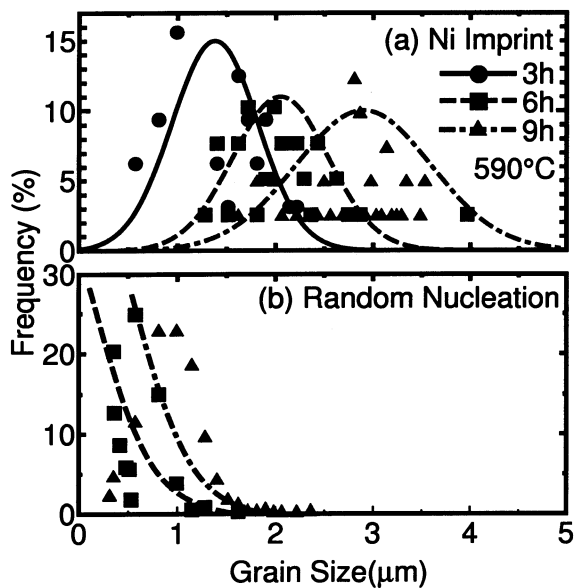


Fig. 3. Change with annealing time of distribution of grain size of Si films.

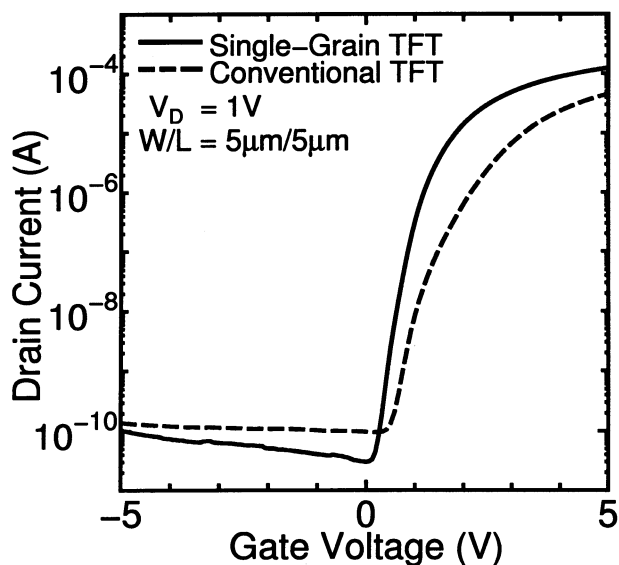


Fig. 4. Typical subthreshold characteristics of n-channel TFTs.

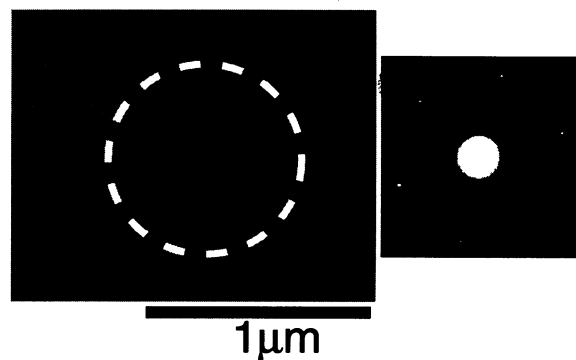


Fig. 2. SEM image of Si grains grown using imprint with a Ni-coated tip array. The sample was annealed at 590 °C for 7 h. TEM image and diffraction pattern taken from a grain are also shown.

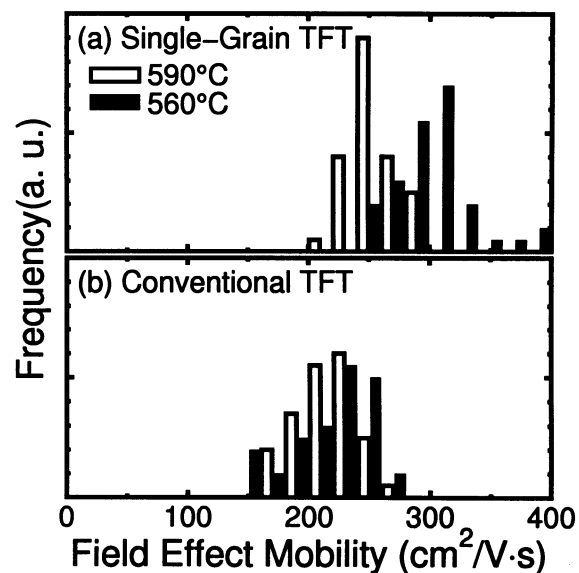


Fig. 5. (a): Distribution of field effect mobility obtained from single-grain TFTs. (b): Distribution of the mobility obtained from conventional-SPC poly-Si TFTs.

EXCIMER LASER ANNEALED, POLY-SI THIN FILM TRANSISTORS FOR FLAT PANEL IMAGER APPLICATION

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Pulsed Excimer-Laser Annealed (ELA) poly-Si Thin Film Transistor (TFT) technology has become an important technology for large area electronic applications. The much-improved performance of these poly-Si TFTs over the conventional hydrogenated amorphous Si TFTs has attracted much attention because of the possibility of building high quality active matrix displays based on either LCDs or organic LEDs. In addition to display applications, ELA poly-Si TFT technology enables the opportunity of building next generation flat panel imagers with higher-level integration and better noise performance. Both the on-glass integration of peripheral driver electronics to reduce the cost of interconnection and the integration of pixel level amplifier to improve the noise performance of large area imagers have attracted much interest and are under development based on this new technology.

In this talk, we will report the progress and current status of our effort in building advanced flat panel imagers based on poly-Si TFT technology. Compared to typical display applications, TFTs used in flat panel imagers have much more stringent requirement on off-state leakage current. With our low leakage current ($2\text{fA}/\mu\text{m}$), high performance (mobility $> 100\text{ cm}^2/\text{Vs}$) poly-Si TFT process, we have successfully demonstrated a prototype imager (384×256 pixels) using poly-Si TFTs as pixel switches, driven by on-glass poly-Si electronics. Good image quality (see Fig. 1) and good uniformity have been achieved as a result of the low and narrow distribution of TFT leakage current. Figure 2 shows the histogram of leakage current of 384×256 poly-Si TFT pixel switches. Integrated peripheral driver electronics have been designed with high tolerance of process variations. On-glass, integrated gate-line drivers including 256 stages static shift registers and buffers for driving high capacitive load have been realized and have been shown to run the prototype imagers successfully without using external gate-line electronics. Poly-Si TFT process, integrated peripheral circuits, and performance of the poly-Si prototype imager, as well as the development of pixel level electronics and preliminary results of radiation hardness study of poly-Si TFTs will be discussed.



Figure 1 Image captured by a prototype imager with 384x256 pixels based on ELA poly-Si TFT technology.

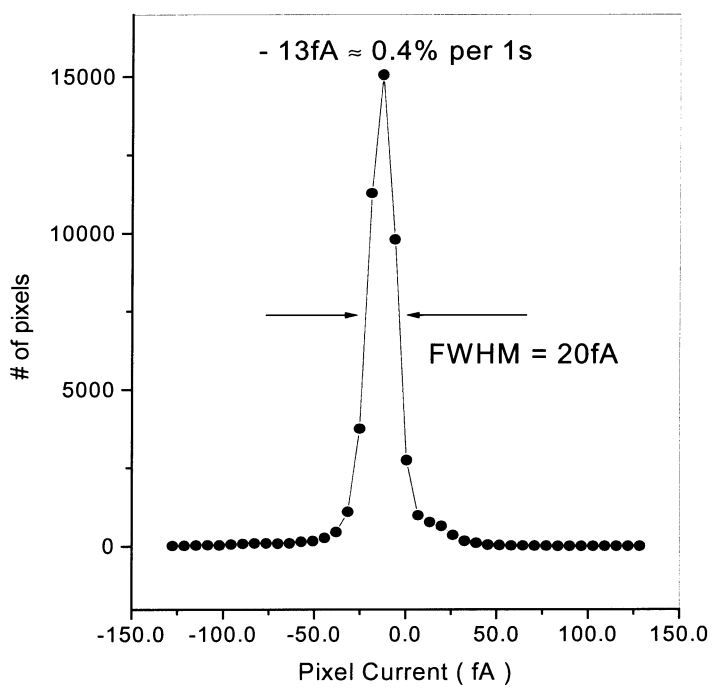


Figure 2 Histogram of pixel switch leakage current of a 384x256 pixel, poly-Si prototype imager.

Amorphous Si TFTs on Plastically-Deformed Substrates with 3-D Shapes

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Current generations of electronic and optoelectronic products are fabricated on the surface of flat, rigid semiconductor or glass substrates. For large-area electronics applications such as displays, large-area sensor arrays (e.g. X-ray imaging plates), and eventually intelligent furniture, clothes, etc, it is highly desirable that they be lightweight and deformable. Previous work [1,2] has demonstrated that transistors on thin metal or plastic foil substrates can be rolled into cylindrical shapes down to a 0.5mm radius of curvature with no adverse effects. With such cylindrical shapes, the strain on the surfaces (where the devices are) can be kept low by using thin substrates. However, to form arbitrary 3-D electronic surfaces, there is no way to avoid a large strain in the substrate. In this paper we report the first transistors fabricated on a substrate that is then plastically deformed. Using amorphous silicon (α -Si) device islands on a polyimide substrate, TFTs can withstand an average substrate strain of 6%, as the substrate is deformed into a spherical cap shape subtending angles as large as 66° (1 steradian solid angle).

In this work, the α -Si TFTs are made on patterned silicon nitride islands on a polyimide (Kapton®) substrate (Fig. 2, 3). To achieve a spherical cap subtending 1 steradian ($\sim 66^\circ$ field of view), the average strain in the substrate can be shown by geometrical considerations [3] to be $\sim 6\%$ (Fig. 1). This leads to permanent plastic deformation of the plastic or metal substrates, and cracks uniform inorganic device films (, which can withstand $\sim 1\%$ strain at most). Previous results [3] have shown that by patterning hard (and brittle) silicon and silicon nitride layers (without devices) into isolated islands on soft polyimide substrates, the semiconductor islands can remain crack-free despite average strain in the substrate in excess of 5%. Most of the deformation takes place in the inter-island region and the substrate flows underneath the hard islands. The strain in the semiconductor island is therefore reduced. In this work, the maximum amorphous silicon island size is about $100\text{ }\mu\text{m}$. To create electronics on a deformed curved substrate, we first fabricate α -Si TFTs on a silicon nitride buffer on a flat plastic or metal foil. The maximum process temperature is 150° . The foil is then plastically deformed into the final desired shape after the nitride and α -Si are patterned.

Fig. 4 shows TFTs' characteristic curves before and after the substrate was deformed into a 1 steradian spherical dome. After fabrication, the curves are well behaved with $\mu_{n, \text{linear}} = 0.2\text{ cm}^2/\text{V.s}$, $V_T = 1.8\text{ V}$, and $I_{\text{ON}}/I_{\text{OFF}} \sim 10^6$. After deformation, devices are still well behaved, with mobility and threshold voltage nominally unchanged (within device to device variations). The leakage current increase is thought to be due to heating to $\sim 150^\circ\text{C}$ during deformation (to soften the polyimide substrate) as opposed to the deformation itself. Further work is underway to complete circuits and increase island sizes with novel geometries.

This work was supported by ONR/DARPA N60001-98-1-8916.

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- [2] H. Gleskova and S. Wagner, Failure Resistance of Amorphous Silicon Transistors Under Extreme In-plane Strain, *Appl. Phys. Lett.*, **75**, 3011 (1999).
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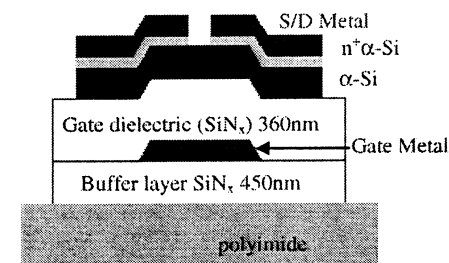
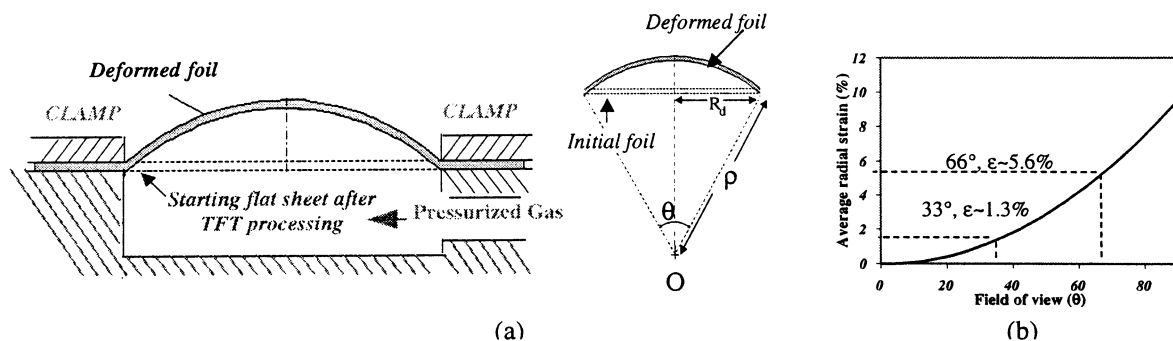


Figure 2. TFT structures

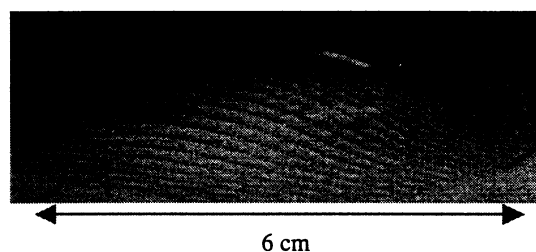
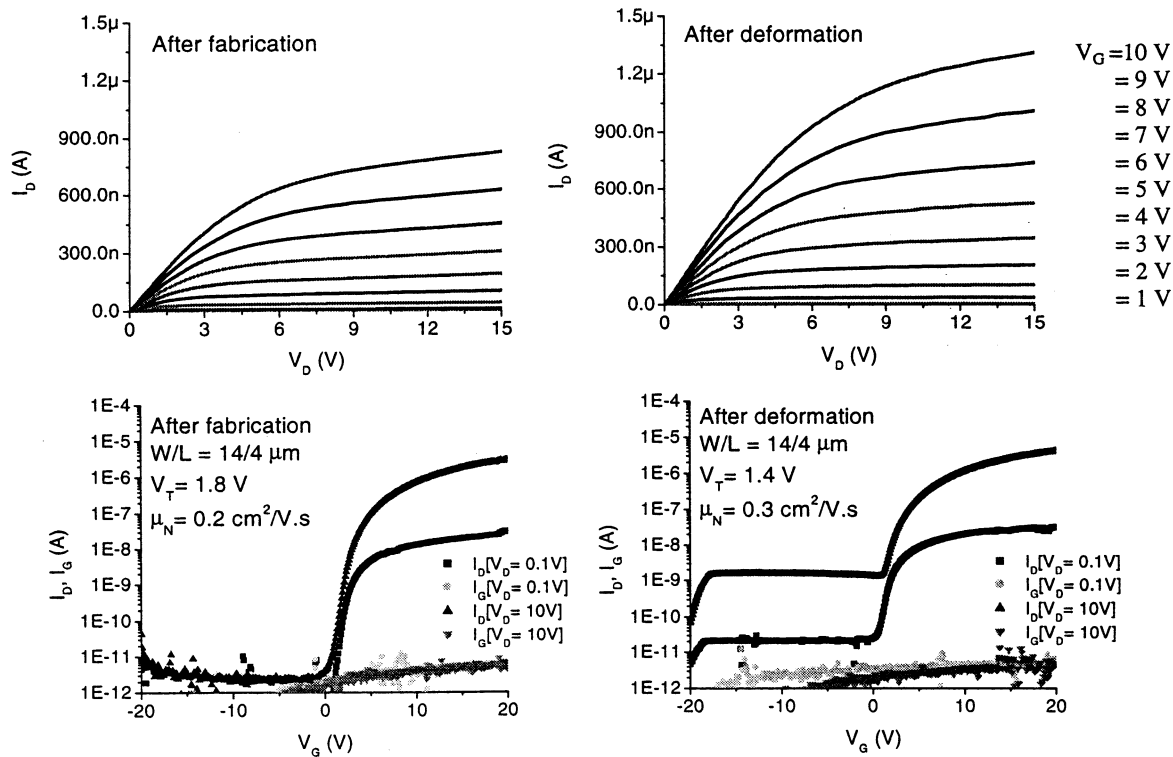


Figure 3. Polyme foil with a-Si/Si₃N₄ islands after deformation to a spherical cap shape with a $\sim 66^\circ$ field of view (~ 1 steradian).



Gate Control in Ultra-Short Channel Double-Gate MOSFETs accounting for 2D and Quantum Confinement Effects

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1- Objectives

Double-gate MOSFETs (DG-MOSFETs) are among the best candidates for the realization of ultra-short gate length MOSFETs due to their low sensitivity to short-channel effect, at least if the inter-gate distance is small. At these dimensions, confinement effects are playing a dominant role but a simple 1D resolution [1] may not be sufficient. Only few attempts have been done so long to account for the lateral variation of quantum confinement along the channel of an MOS transistor. [2, 3] We establish here for the first time how 2D effects are affecting carrier confinement and gate control in the channel of ultra-short gate DG-MOSFETs by solving the Poisson and Schrödinger equations self-consistently in the 2D section of a device. The results are discussed in reference to what is obtained from a 2D classical simulation (no confinement : Poisson equation with a bulk statistics) and from a 1D quantum simulation (confinement effects in a long gate device).

2- Numerical method

The specific features of our method have been already presented.[3] This method is especially well suited to the simulation of arbitrary shaped structures and shows rapid and robust convergence. The meshing was strongly refined near the gates (around 0.1 nm mesh size) : note that this is even more important when confinement effects are neglected as the carrier concentration shows then sharper profiles.

In the quantum simulations, we accounted for the 6-fold degeneracy of the conduction band in silicon. The ellipsoidal symmetry of each valley was described by means of a mass tensor. We assumed the usual values for the longitudinal and transverse effective mass in silicon (longitudinal and transverse being defined here with respect to the valley axis) : $m_l = 0.19 m_0$, $m_t = 0.9 m_0$. A 3 eV barrier was assumed at the interface between oxide and silicon.

Simulations were done under quasi-equilibrium conditions ($V_{DS} = 0$ V). Accounting for drain voltage influence requires coupling with carrier transport : this is a tough physical and numerical work which is presently under way and will represent the next step of this study. Gate charge control was evaluated by integrating the electron concentration across the channel. We checked from classical 2D drift-diffusion simulations that the variation of the integrated charge n_i as a function of V_{GS} was giving the correct subthreshold slope and threshold voltage.

3- Results

3.1 Sensitivity to inter-gate distance variation

We have first simulated structures where the inter-gate distance d_{GG} was varied (from 40 down to 2 nm) while channel length L_{ch} was kept equal to 40 nm (50 nm gate length). As DG-MOSFETs are less sensitive to volume leakage, a low substrate doping has been used (10^{16} cm^{-3}). The oxide thickness was 1 nm.

Figures 1-2 compare the electron concentration profiles calculated with the same surface electrostatic potential, in the strong inversion regime, with and without confinement effects. Neglecting quantum effects gave increasingly wrong results as d_{GG} decreased. The difference was especially evident below 10 nm, where classical simulation still found two separate gate channels whereas they were in fact already merging. Note that the distance at which channels merge depends on gate voltage. A simple 1D quantum simulation would not give the right profile either, as it would over-estimate quantum confinement effects (Fig. 5).

Variation of the integrated electron concentration (n_i) with the gate surface potential (Ψ_G) is shown on Figs 3 (2D classical) and 4 (2D quantum). Classical simulation gave a rather correct estimation of the inter-gate distance above which short-channel effects were appearing. But the set of characteristics strongly differed for small d_{GG} due to strong coupling between the two interfacial wells. From these curves, we extracted the subthreshold slope (S), the electrostatic potential on the gate at threshold (Ψ_T , taken at $n_i = 10^9 \text{ cm}^{-2}$) and the electron sheet concentration in strong inversion (n_{inv}). Both quantum and classical simulations gave a very similar estimation of S (Fig. 5). This is consistent with the fact that S is a good indicator of the presence of 2D leakage effects. Classical simulation gave a correct estimation of Ψ_T as well, provided that d_{GG} was larger than 10 nm. Below this distance, confinement effects became too strong to be neglected. The 1D quantum simulation gave better results (as a 40 nm channel length could then be considered as "long"). Finally, it should be noted that whatever d_{GG} , quantum confinement strongly reduced the maximum inversion charge (Fig. 8). Therefore, I_{ON} values deduced from a 2D classical simulation should be taken with care (even apart from any carrier transport consideration).

3.1 Sensitivity to channel length shrinking

In a second set of simulations, we maintained 10 nm between the gates and reduced L_{ch} from 40 to 10 nm. The maximum inversion charge was rather insensitive to channel shrinking (in the explored range of gate lengths). Extracted values of S and Ψ_T are given on Table 1. Classical simulation under-estimated their degradation at short gate length. This was correlated to tunneling between source and drain, with wave functions showing a significant contribution in a region of the channel where the sub-band minimum was up to 100 meV below the conduction band (for $L_{ch} = 10$ nm).

Table 1 : Influence of L_{ch} shrinking (1st number for 2D quantum, 2nd number for 2D classical simulation)

L_{ch} (nm)	40	30	20	10
S (mV/dec)	61/61	63/63	69/70	114/104
Ψ_T (V)	0.3/0.3	0.3/0.3	0.25/0.24	0.07/0.09

4- Conclusions

We found that classical simulation strongly over-estimated the inversion charge, even in large structures. It gave a rather correct estimation of the presence of 2D effects in the subthreshold regime, as long as inter-gate distance and channel length remained higher than 10 and 20 nm. If d_{GG} or L_{ch} was shorter than these values, it was necessary to account for confinement effects, even in the subthreshold regime. Noteworthy, confinement enhanced then the degradation of the sub-threshold characteristic with gate shrinking and its sensitivity to inter-gate distance variation. With a 10 nm channel length (and probably for longer channels with a bias voltage applied on the drain), tunneling between source and drain has been evidenced and correlated to the subthreshold characteristics degradation.

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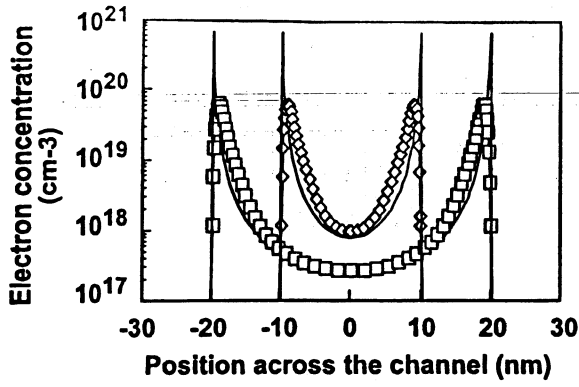


Fig. 1 : Electron profile across the channel as calculated from 2D quantum simulation (symbols) and 2D classical simulation (solid lines) for large d_{GG} values (40 and 20 nm). The profiles are taken at mid-distance between source and drain. $\Psi_S = 1.4$ V

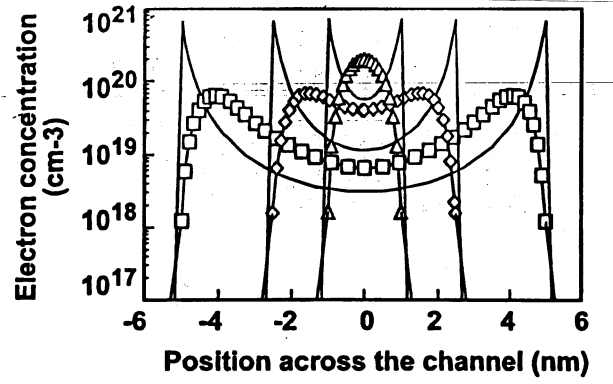


Fig. 2 : Same as Figure 1 for small d_{GG} values (10, 5 and 2 nm).

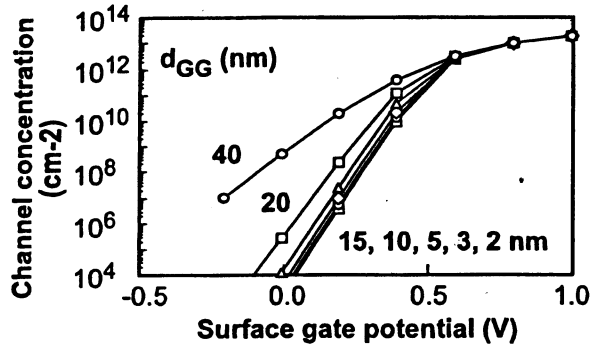


Fig. 3 : Gate charge control as calculated from 2D CLASSICAL simulation for different inter-gate distances ($d_{GG} = 40, 20, 10, 5, 3$ and 2 nm)

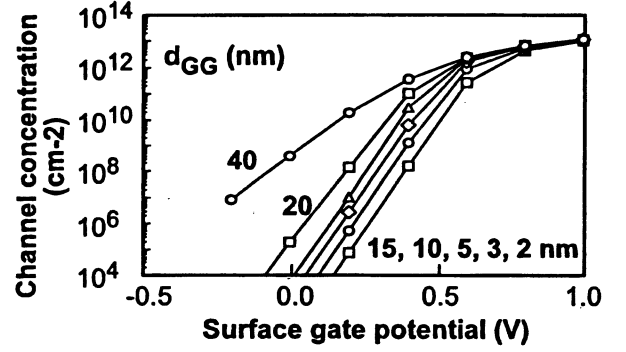


Fig. 4 : Gate charge control as calculated from 2D QUANTUM simulation for different inter-gate distances ($d_{GG} = 40, 20, 10, 5, 3$ and 2 nm)

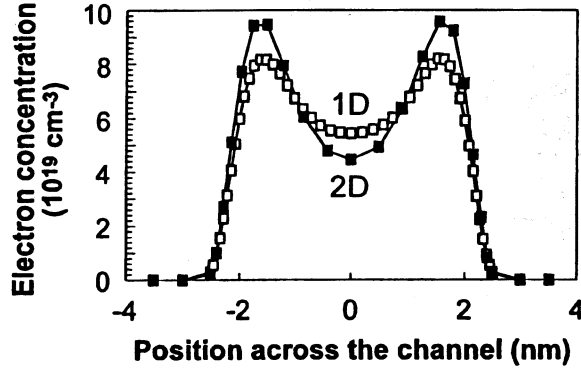


Fig. 5 : Electron profiles after 1D simulation ($L_{ch} = \infty$) and after 2D QUANTUM simulation ($L_{ch} = 40$ nm) for $d_{GG} = 5$ nm ($\Psi_S = 1.6$ V)

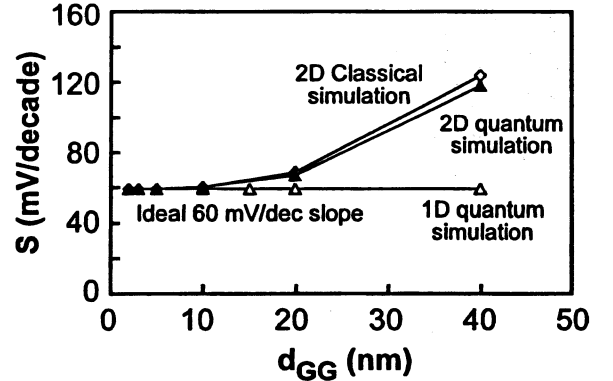


Fig. 6 : Subthreshold slope as a function of d_{GG} ($L_{ch} = 40$ nm)

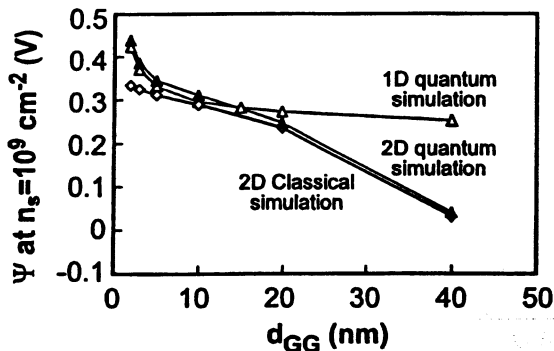


Fig. 7 : Threshold voltage Ψ_T as a function of d_{GG} ($L_{ch} = 40$ nm)

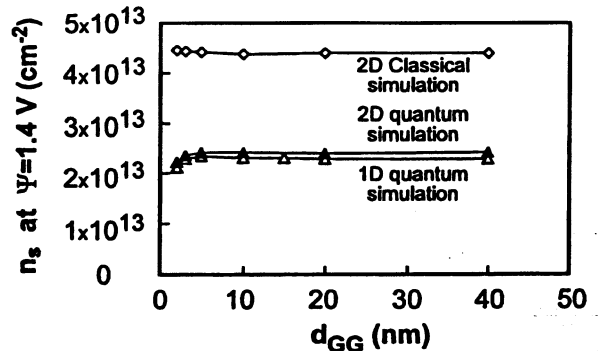


Fig. 8 : Strong inversion channel concentration as a function of d_{GG} ($L_{ch} = 40$ nm and $\Psi_S = 1.4$ V)

Wide Bandgap Semiconductors

WEDNESDAY PM, JUNE 27TH, 2001

Session Organizer: Anant Agarwal, CREE

2:00 PM, VII.B.-1 Invited

K-Band GaN Power HFET's with 6.6 W/mm CW Saturated Output Power Density and 35% Power Added Efficiency at 20 GHz: *Miro Micovic*¹; Jeong S. Moon¹; Ara Kurdoghlian¹; Paul Hashimoto¹; Danny Wong¹; Loren McCray¹; Tahir Hussain¹; Paul Janke; ¹HRL Laboratories LLC, 3011 Malibu Canyon Road, Malibu, CA 90265 USA

2:30 PM, VII.B.-2

Linearity of High Al-Content AlGaIn/GaN HEMTs: *T. Jenkins*¹; L. Kehias¹; P. Parikh²; Y.-F. Wu²; P. Chavarkar²; M. Moore²; U. Mishra²; ¹Air Force Research Laboratory, 2241 Avionics Circle, Wright-Patterson AFB, OH 45433 USA; ¹Cree Lighting Company, 340 Storke Road, Goleta, CA 93117 USA

2:50 PM, VII.B.-3

Demonstration of Push-Pull Operation of AlGaIn/GaN HEMTs on SiC: *Jong-Wook Lee*¹; Sungjae Lee¹; Keven J. Webb¹; ¹Purdue University, School of Electrical and Computer Engineering, West Lafayette, IN 47907 USA

3:10 PM, VII.B.-4

On Development of 600-850 V 6H-SiC LDMOS Transistors Using Silane-Ambient Implant Anneal: *I. Sankin*¹; J. B. Casady¹; J. B. Dufrene¹; W. A. Draper¹; J. Kretchmer²; J. Vandersand¹; V. Kumar¹; M. S. Mazzola¹; S. E. Saddow¹; ¹Mississippi State University, Electrical & Computer Engineering Department, Box 9571, Mississippi State, MS 39762-9571 USA; ²General Electric Corporate Research & Development Center, Schenectady, NY USA

3:30 Break

3:50 PM, VII.B.-5

An X-Band Silicon Carbide IMPATT Diode: *Luo Yuan*¹; Michael R. Melloch¹; James A. Cooper, Jr.¹; Kevin J. Webb¹; ¹Purdue University, School of Electrical and Computer Engineering, West Lafayette, IN 47907 USA

4:10 PM, VII.B.-6

The Effect of Emitter Implant and Anneal on High-Voltage 4H-SiC BJTs: *Yi Tang*¹; Jeffrey B. Fedison¹; T. Paul Chow¹; ¹Rensselaer Polytechnic Institute, Center for Integrated Electronics and Electronic Manufacturing, Troy, NY 12180 USA

4:30 PM, VII.B.-7

Diamond Surface Channel FET with $f_{\max}$ Above 30 GHz: *A. Aleksov*¹; A. Denisenko¹; U. Spitzberg¹; E. Kohn¹; ¹University of Ulm, Dept. of Electron Devices and Circuits, Albert-Einstein-Allee 45, D-89081 Ulm, Germany

K-Band GaN Power HFET's with 6.6 W/mm CW Saturated Output Power Density and 35% Power Added Efficiency at 20 GHz

Miro Micovic, Jeong S. Moon, Ara Kurdoghlian, Paul Hashimoto, Danny Wong,
Loren McCray, Tahir Hussain, Paul Janke

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AlGaIn/GaN heterostructure field effect transistors (HFET's) grown on SiC substrates are currently the most powerful three-terminal microwave solid state devices. While the power performance of these devices is well documented at X-band frequencies[1- 2], there is growing interest in these devices at higher frequencies. In this study we characterize the power performance of GaN HFET's at 20 GHz. The epitaxial GaN/AlGaIn HFET layers were grown by plasma assisted MBE on semi-insulating SiC wafers. The layer sequence (starting at the substrate) consists of an AlN/AlGaIn nucleation layer, a 2 μm thick GaN layer and a strained AlGaIn Schottky barrier layer. This HFET structure consistently yields a room temperature 2DEG Hall effect mobility of over 1300 cm^2/Vs and an electron sheet charge density of $1.3 \times 10^{13} \text{ cm}^{-2}$. A Ti/Al/Ni/Au metalization process is used to form source and drain contacts. The source-drain separation of the devices is 2 μm . The ohmic contact resistance extrapolated from TLM patterns is 0.5 $\Omega\text{-mm}$. The 0.15 μm long T-shaped gate fingers were defined using e-beam lithography. Mesa isolation was achieved by chlorine reactive ion etching. The on-wafer DC measurements were carried out using a HP4155 semiconductor parameter analyzer. A two terminal reverse-bias gate-to-drain breakdown voltage of 50 V was measured at a gate current density of 1 mA/mm. The transfer characteristics of a 2x50 μm dual gate device are shown in Figure 1. A peak g_m of 280 mS/mm was measured at 7 V V_{ds} . The common source I-V characteristics of the same device are shown in Fig.2. The maximum drain current density of the device is 1.7 A/mm at 10 V V_{ds} . This is one of the highest current densities ever reported for a microwave field effect transistor. The small signal RF performance was measured over the 0.5 to 40 GHz frequency range using a HP8510 network analyzer. Figure 3 shows small signal frequency response from a 0.15 μm x 200 μm device measured at $V_{ds} = 10 \text{ V}$, $V_{gs} = -5.5 \text{ V}$. From S-parameter data, an extrinsic current-gain cutoff frequency (f_r) of 85 GHz and a maximum frequency of oscillation (f_{max}) of more than 100 GHz are extrapolated. On-wafer power measurements at 20 GHz were performed using an active load-pull system. The power performance of a 0.1 mm (2x50 μm) device biased at $V_{ds} = 20 \text{ V}$ and $I_d = 80 \text{ mA}$ is shown in Figure 4. The device has a gain of 10.7 dB in its linear region and a gain of 6.3 dB at peak efficiency. The measured continuous wave (CW) output power density of 6.6 W/mm and associated power added efficiency (PAE) of 35% are, to the best of our knowledge, the highest reported to date for a field effect transistor at this frequency. This result is also the best combination of the output power density and PAE reported for a GaN HFET in the K-band.

In summary, we have demonstrated state of the art performance of GaN HFET's at 20 GHz. Our results clearly show that GaN HFET's have strong potential for power applications at K-band frequencies and beyond.

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 - [2] Y.-F. Wu, et al., "High Content AlGaIn/GaN HEMT's on SiC Substrates with Very-High Power Performance", *IEDM Technical Digest*, Washington D. C., 927-927, Dec. 5-8 1999.

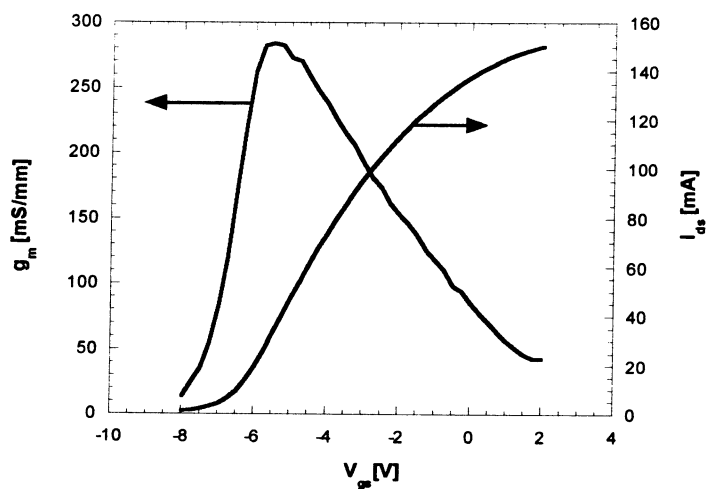


Fig 1. DC transfer characteristics of a 0.15 μm x 100 μm GaN HFET at 7V drain bias.

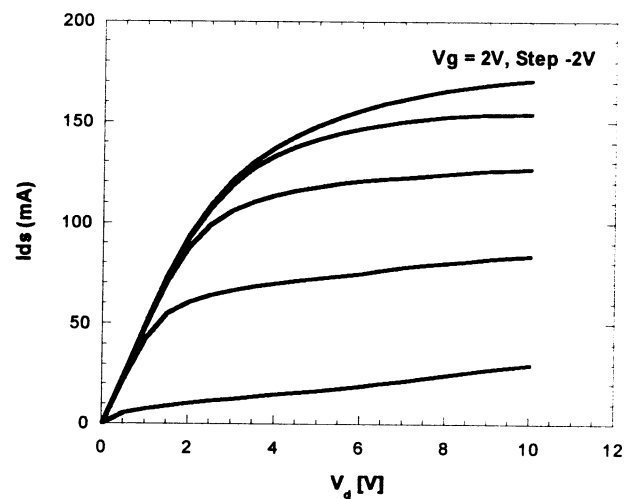


Fig. 2. Common source I-V characteristics of a 0.15 μm x 100 μm GaN HFET.

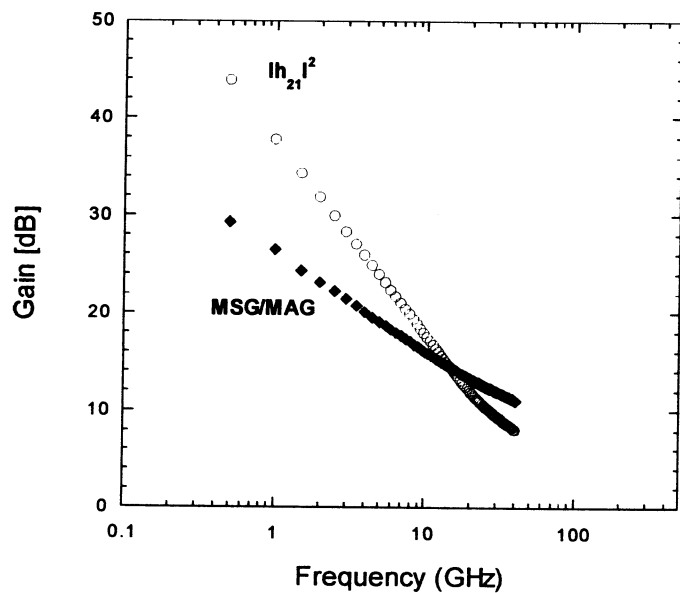


Fig. 3. Small signal current gain ($|h_{21}|$) and maximum stable/available gain (MSG/MAG) of a typical 0.15 μm x 200 μm GaN HFET measured at $V_{ds} = 10$ V, and $V_{gs} = -5.5$ V.

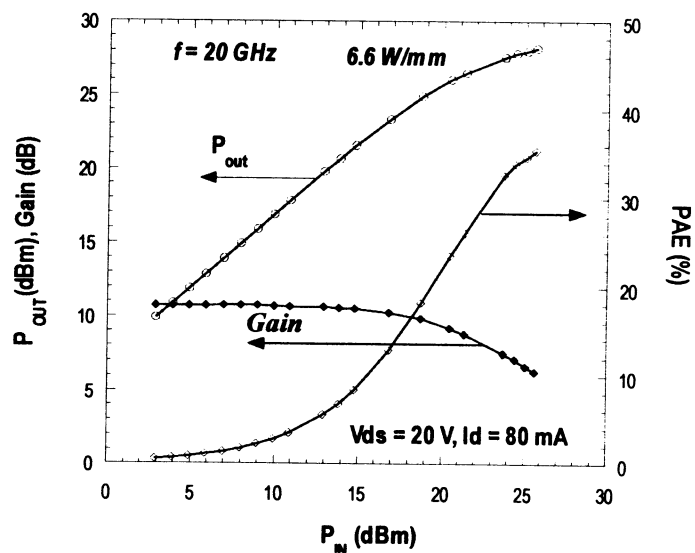


Fig. 4. Power performance of a 0.1 mm (2x50 μm) GaN HFET at 20 GHz. The device was biased at $V_{ds} = 20$ V with $I_{ds} = 80$ mA.

Linearity of High Al-Content AlGaIn/GaN HEMTs

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This work will address the advancements in the linearity of AlGaIn/GaN HEMTs. This is the first reported linearity result for high-Al content devices, and it is the first reported result of linearity for nitride-based HEMTs under both transmitter and receiver types of conditions. When the device technology matures, it will have commercial and military applications in wireless base stations, satellite communications, and radar.

The power handling capability of AlGaIn/GaN HEMTs continues to improve. For example, a power density of 9.1 W/mm with PAE of 47% at 8.2 GHz was achieved for small-periphery devices, while large-periphery devices yielded an amplifier with greater than 50 W output power at 6 GHz using a single 8-mm HEMT chip.^[1] However, advanced modulation and coding techniques require linear amplifiers. At the device level, excess output power capability is specified to ensure that sufficient linearity is achieved at the required minimum output power under backed-off conditions. Alternatively, complex circuit techniques and shunting of multiple devices are used. In the receiver, linearity is required for fidelity and robustness to hostile signals or interference, while still providing adequate detection of the minimum signals at low dissipated powers.

This novel work will present recent advancements in the promising linearity of high Al-content AlGaIn/GaN HEMTs scaled for transmitter and receiver applications. The device structures were grown by MOCVD on semi-insulating SiC substrates. A modulation-doped AlGaIn layer, with greater than 30% Al, was grown on the insulating GaN buffer that was used for the channel. The gate lengths were 0.5-0.6 μm . The devices were fabricated using a process that was previously discussed.^[2] Single-tone and two-tone (CW) performance was measured using a Maury Microwave load pull system with passive electromechanical tuners. The single-tone and carrier frequencies were 10 GHz. The second tone was offset from the carrier by 100 kHz, and the third-order intermodulation product was measured at the output. Carrier-to-intermodulation ratio (C/I) was used to characterize linearity in saturated power conditions, such as peak PAE. The output third-order intercept (OIP3) was used to evaluate the device linearity under linear power conditions.

Evaluation of linearity for insertions in output power amplifiers involved devices with 1-mm periphery, which were flip-chip bonded to carriers for reduced source inductance and improved thermal management. Linearity was characterized with respect to bias, efficiency, and total power. A difference between single-tone and two-tone performance was observed and will be explained. At 15 V, -18 dBc was obtained at peak PAE. At P_{1dB} , the C/I was -27 dBc. An OIP3 greater than 44 dBm was observed under Class-A operation. The AlGaIn/GaN HEMTs were also compared to 1.2-mm periphery GaAs-based pHEMTs. Causes of the differences in linearity between the pHEMTs and the nitride-based HEMTs will be discussed.

The linearity of devices for robust receiver applications was characterized using smaller periphery (150 μm) HEMTs. These devices yielded a better trade-off between optimum input noise match and gain match while simultaneously exhibiting high breakdown voltage. These devices were tested on-wafer using low power and low drain current appropriate for low-noise amplifiers. The 150- μm devices yielded an OIP3 of 28.6 dBm at $V_{\text{DS}}=10\text{V}$ and $V_{\text{GS}}=-2.75\text{V}$, if a 3:1 slope is extrapolated. However, the measured slope of the third-order intermodulation was greater than 3:1.

While several challenges and issues remain concerning the insertion of nitride technology into applications, the linearity results are promising. Further investigation of the device design towards improved linearity should prove fruitful.

Acknowledgement: The linearity measurements and analysis were done at AFRL. The AlGaIn HEMT device work for robust receivers was support by ONR under contract # N0001400C0175 and the work on high power transmitters was supported by BMDO with the contract monitored by ONR (contract #N0001499C0656).

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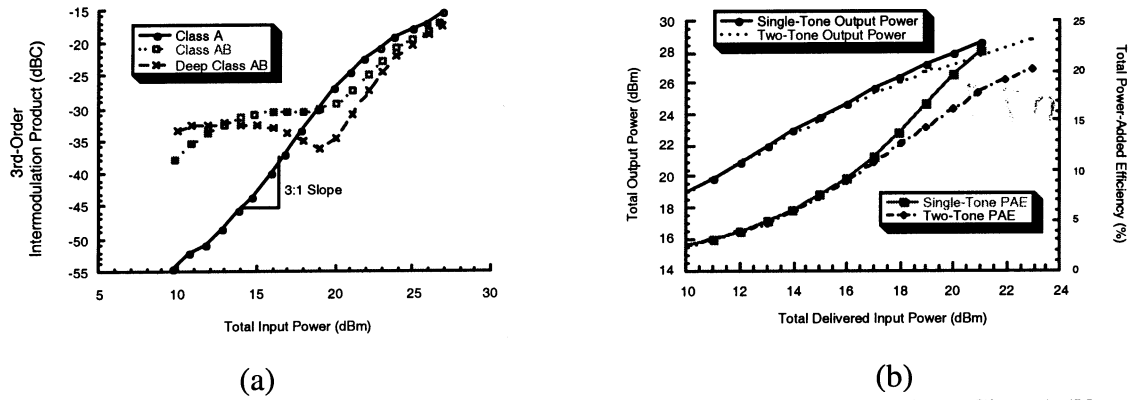


Figure 1. Power performance of 1-mm AlGaIn/GaN HEMT. (a) Intermodulation with $V_{DS}=15V$ at Class-A ($V_{GS}=-2.5V$), Class-AB ($V_{GS}=-3.75V$) and deep Class-AB ($V_{GS}=-4V$) biases. (b) Comparison of output power and efficiency for single-tone and two-tone input power at $V_{DS}=10V$ and $V_{GS}=-3V$. Carrier and second tone frequencies were 10 GHz and 10.0001 GHz, respectively.

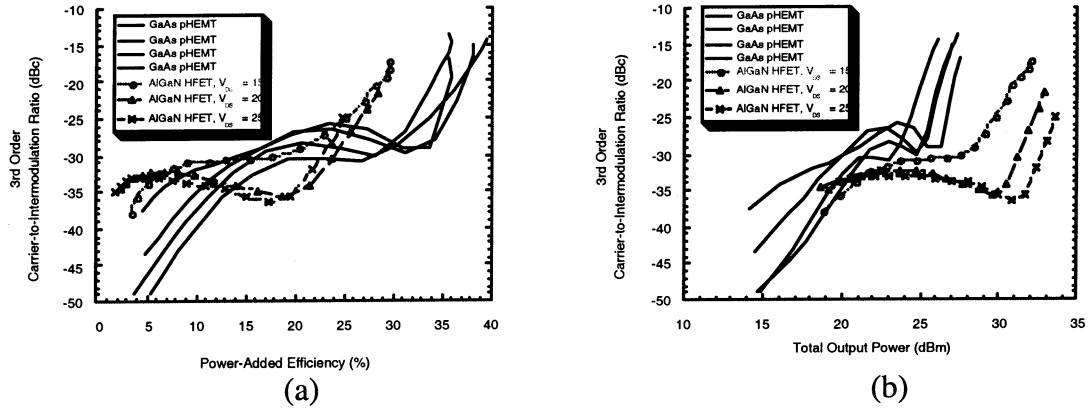


Figure 2. Comparison of 1-mm AlGaIn/GaN HEMTs and 1.2-mm III-V pHEMTs with respect to (a) the total efficiency and (b) to the total output power. The gate and drain biases of pHEMT were varied over the safe-operating area, while the gate bias of AlGaIn HEMT was fixed at -3.75 V and drain bias was varied.

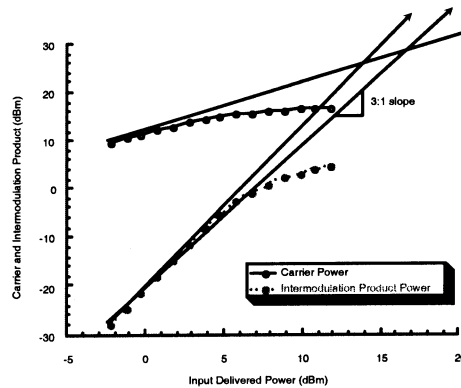


Figure 3. Third-order intercept (OIP3) of the 150- μm AlGaIn/GaN HEMT. The bias conditions were those used for noise characterization with $V_{DS}=10V$ and $V_{GS}=-2.75V$.

Demonstration of Push-Pull Operation of AlGaIn/GaN HEMTs on SiC

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AlGaIn/GaN on high thermal conductivity SiC transistors have demonstrated power densities of 6.9 W/mm at 10 GHz and 9.1 W/mm at 8.2 GHz [1], [2], making them candidates for compact, light-weight, high power amplifier systems. These power densities have been measured in small periphery devices. To achieve this level of power density in large periphery devices requires good thermal management. The requirements on thermal dissipation will be further exacerbated for GaN transistors on lower thermal conductivity Si [3].

We report the first demonstration of Class B push-pull operation of GaN HEMTs, thereby taking advantage of lower thermal dissipation while achieving linear operation and allowing higher power density in large-area devices. This lower thermal dissipation can be achieved because of the potentially higher power-added-efficiency (PAE) of Class B operation, relative to Class A operation.

The epilayers for the AlGaIn/GaN HEMTs were grown using MOCVD on semi-insulating 4H-SiC. The epilayer structure is similar to that in [1]. The 0.25 mm device with $L_G=0.35\ \mu\text{m}$ showed more than 800 mA/mm drain current, 220 mS/mm transconductance, and more than 60 V breakdown voltage. A 1.5 mm ($12 \times 125\ \mu\text{m}$) device, measured in a $50\ \Omega$ system, produced 13.5 dB gain at 10 GHz, an f_T of 26 GHz and a f_{max} of 45 GHz, as shown in Fig. 1. Using the device geometry and typical measured DC characteristics, a thermal model that has been developed for AlGaIn/GaN on SiC HEMTs produced the simulated temperature rise versus drain bias voltage of Fig. 2, for Class A and B operation. For each drain bias, the maximum output power is assumed. Although single-ended Class B operation is nonlinear, the lower temperature rise from reduced power dissipation is evident. Figure 3 shows the measured power sweep of a $0.35\ \mu\text{m}$ gate length, 1.5 mm wide device in Class B mode, biased at $V_{DS}=15\ \text{V}$. For saturated power input at 4 GHz, the output power was 2.4 W and the thermal dissipation in Class B operation was 2.7 W in a $50\ \Omega$ system. For comparison, using a 15 V bias in Class A mode and a peak current of 800 mA, and assuming the maximum output power condition, results in 4-5 W of dissipated power. A PAE of 46 % was measured in Class B mode without input and output matching, with 12 dB small signal gain.

Class B push-pull operation was achieved using a new broadband balun for input/output phase shifting. This balun was implemented with three symmetric coupled lines and showed excellent loss of less than 0.5 dB per balun over 5-11 GHz (3 dB bandwidth was 4-12 GHz) [4]. The fabricated amplifier is shown in Fig. 4. The balun and matching network were fabricated on a high thermal conductivity AlN substrate ($\epsilon_r=8.5$). Small-signal S-parameter measurements at $V_{DS}=15$, $V_{GS}=-3.4\ \text{V}$ showed 8 dB gain at 5 GHz (for the amplifier including input and output baluns) with 25 % PAE, and 31 % PAE with the balun loss de-embedded, as shown in Fig. 5 and Fig. 6. The 3 dB bandwidth of this amplifier is 3.5-10.5 GHz. The increase in I_{DS} with input power in Fig. 6 is characteristic of Class B operation.

Acknowledgments: This work is supported by ONR under N00014-98-1-0371 and N00014-99-C-0172 (John Zolper). The devices were fabricated by Cree Inc. under ONR contract N00014-99-C-0172 (John Zolper).

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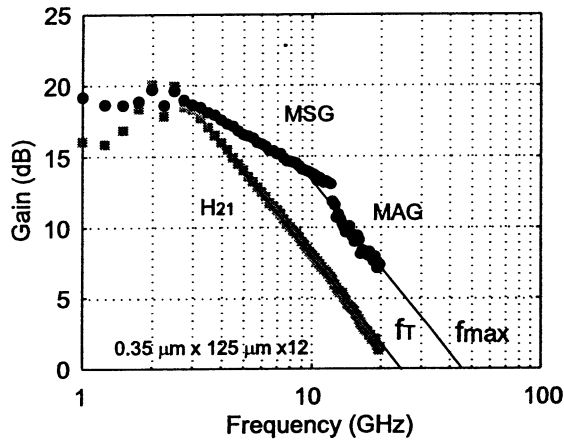


Fig. 1. Measured current gain ($|H_{21}|$) and power gain versus frequency of a $0.35 \mu\text{m}$ gate-length, 1.5 mm AlGaIn/GaN HEMT on SiC

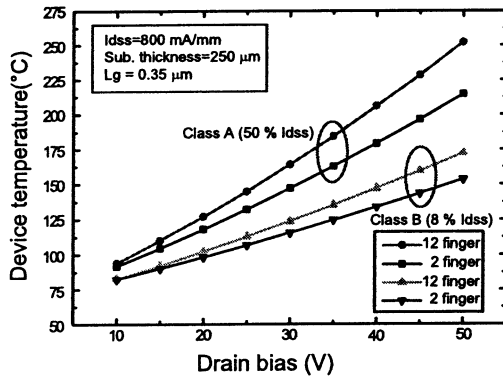


Fig. 2. Temperature rise versus drain bias voltage for 2 finger ($250 \mu\text{m}$) and 12 finger (1.5 mm) AlGaIn/GaN HEMT on SiC in Class A and Class B (AB) mode operation.

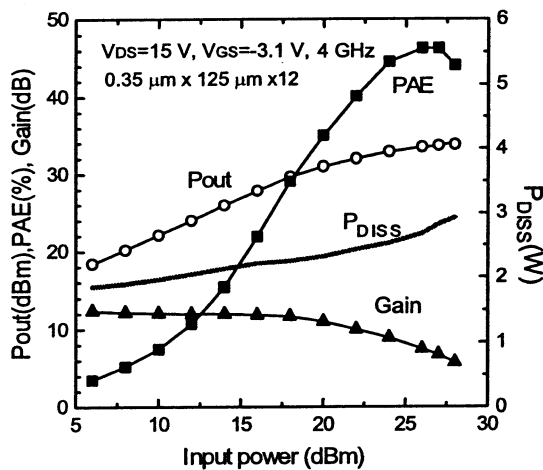


Fig. 3. Measured power sweep of 1.5 mm AlGaIn/GaN HEMT on SiC at 4 GHz with $V_{DS} = 15 \text{ V}$, $V_{GS} = -3.1 \text{ V}$ (Class B (AB) bias).

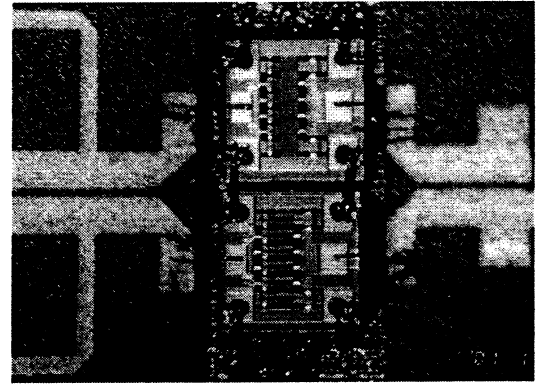


Fig. 4. Photograph of the fabricated amplifier.

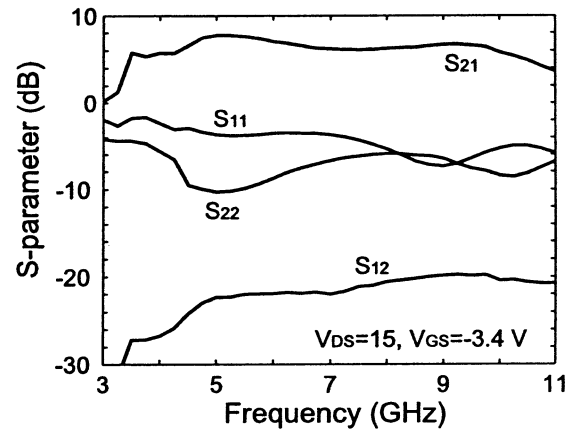


Fig. 5. Measured small-signal S-parameters for the push-pull amplifier ($V_{DS}=15 \text{ V}$, $V_{GS}=-3.4 \text{ V}$).

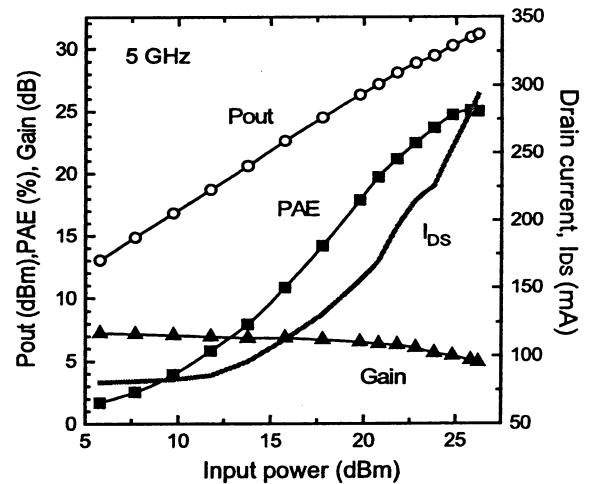


Fig. 6. Power output of Class B push-pull amplifier biased at $V_{DS}=12 \text{ V}$, $V_{GS}=-3.1 \text{ V}$.

On Development of 600 - 850 V 6H-SiC LDMOS Transistors Using Silane-ambient Implant Anneal

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In this work, we report on development of 600 - 850 V SiC LDMOSFET's, which for the first time utilize silane-overpressure implant annealing, in comparison to earlier works [1-3]. A 2-D model using Medici™ software from Avant! Corporation was used to optimize the structure, and a modified implant anneal with silane overpressure was used to improve the surface morphology of implanted regions. Further, drain and gate electrode extensions were used to increase the blocking voltage.

One of the major issues in growing the p-type epitaxy is controlling background contamination from the reactor at 1600°C growth temperature, and control of the dopant introduction. Ten μm layers were grown uniformly doped in the range of $2\text{-}7 \times 10^{16} \text{ cm}^{-3}$ across the four wafers, which explains the blocking voltage for such devices (600-850V). These layers were grown in a horizontal cold-wall system capable up handling up to 75 mm diameter single wafers without the use of active trimethylaluminum (TMA), and the full process has been reported in detail elsewhere [4].

Looking for the optimal structure of lateral n-channel 6H-SiC MOSFET shown in Figure 1, we pursued two competing goals: minimize $R_{\text{on,sp}}$ and maximize V_B . To do so, a reduction of surface field, by choosing optimal doping and thickness of drift region, is done. For the drift region depth of 0.4 μm , donor concentration of the drift region can be optimized as a function of acceptor concentration in p-epi and target blocking voltage by using 2-D simulation (see Figure 2). However, even for the optimal drift region concentration, the potential distribution across the surface is not linear, but rather of a parabolic shape. There still remain two points of peak electric field at the edge of the gate electrode and at the corner of the drain region. To reduce this problem we used gate and drain electrodes extension over the field oxide as shown in Figure 1. Such overlaps give more homogeneous distribution (see Figure 3) of surface potential, which means significant improvement of blocking voltage.

One way to reduce channel component of $R_{\text{on,sp}}$ is to reduce channel length, although it risks punch-through when high V_D is applied. Another way to lower on-resistance is to improve the ion implant anneal, and lower the surface step-bunching on the surface of the annealed SiC. Annealing at 1600°C for to activate the N_2 source/drain and drift regions, we have experimental evidence from AFM (see Figure 4) that wafers annealed in a silane over-pressure reduces the surface roughness. The process has been reported before [5], but here we make the first quantitative comparisons in channel mobility between Ar and silane ambient annealed wafers. Comparisons with a control wafer using Ar-ambient implant activation and silane over-pressure activation showed relatively small differences between the average values of the effective channel mobility (μ_{eff}) at room temperature (30.4 $\text{cm}^2/(\text{V}\cdot\text{s})$ and 40.6 $\text{cm}^2/(\text{V}\cdot\text{s})$ respectively). However, measurements performed at elevated temperatures, revealed the μ_{eff} did not decrease as rapidly for those devices fabricated on silane-annealed wafers. There were no differences in breakdown voltage among the single-finger test devices (a top-view of such a device is shown in Figure 5 with 700 V blocking result shown in Figure 6). Larger area 20 finger devices exhibited blocking voltage up to 600 V, with 0.6 A current in the forward direction. 600 V blocking was obtained on devices with drift regions as short as 9 μm .

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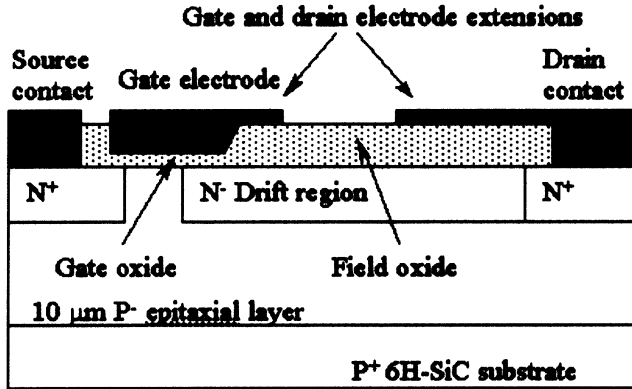


Figure 1: Cross-section of a 6H-SiC LDMOSFET. Drift region varied from 9 to 18 μm .

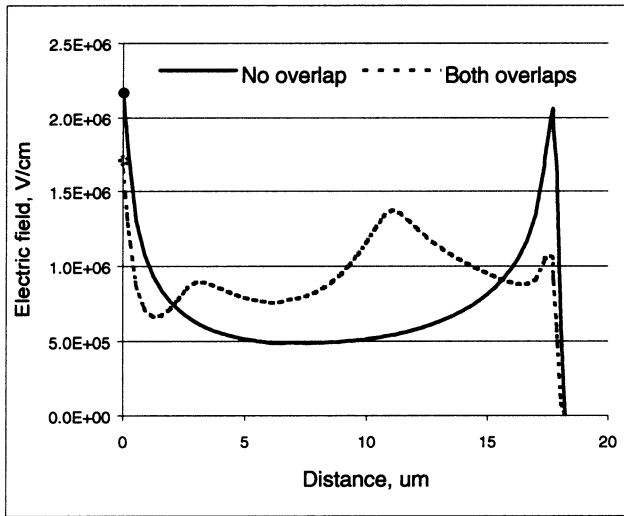


Figure 3: Simulated electric field distribution at the surface between gate and drain with and without using field plates at $V_{ds}=1000\text{V}$.

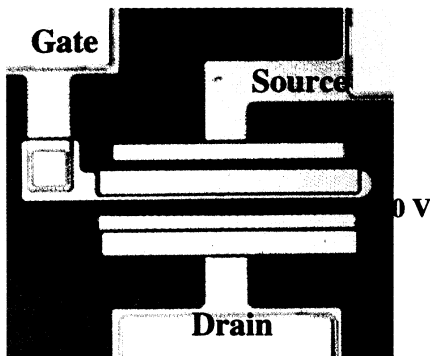


Figure 5: Top-view of single-finger test MOSFET used to measure breakdown voltage.

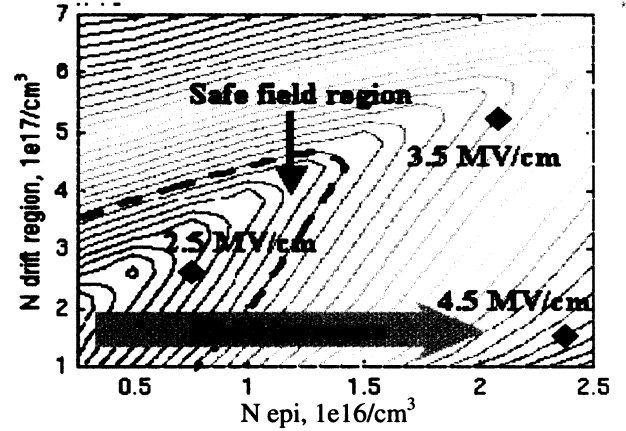


Figure 2: Simulated maximum electric field in the device bulk as a function of drift region and epi doping at $V_{ds}=1.2\text{ kV}$.

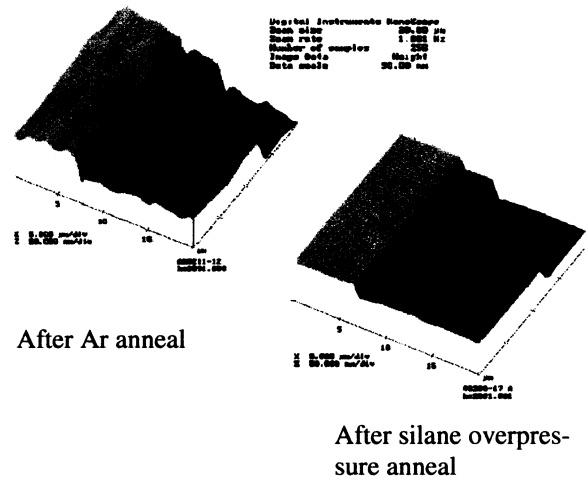


Figure 4: Atomic force microscopy of the surface of the drift and drain regions after ion implantation and subsequent 1600°C annealing in argon and silane ambient conditions.

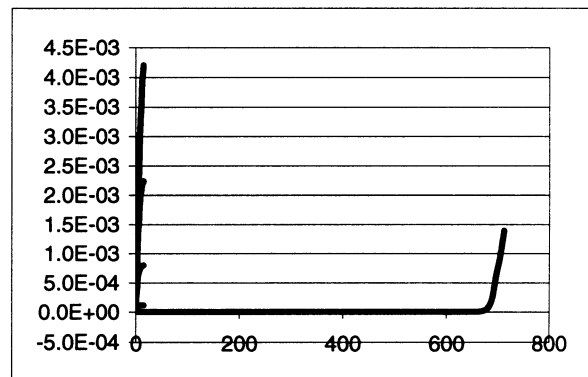


Figure 6: Typical blocking characteristic of a single-finger MOSFET with $5\text{ }\mu\text{m}$ channel length and $112\text{ }\mu\text{m}$ channel width. Drift region length was $12\text{ }\mu\text{m}$.

An X-band Silicon Carbide IMPATT Diode

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IMPact-ionization-Avalanche-Transit-Time (IMPATT) diodes are widely used as microwave sources in transmitters in pulsed radar systems. Under pulsed conditions, the peak output power of an IMPATT diode at a given frequency is limited by its underlying material properties. Due to the high breakdown field and high electron saturation velocity of silicon carbide (SiC), a SiC IMPATT diode is expected to produce microwave power at least 100 times higher than Si or GaAs IMPATT diodes [1]. We reported the first demonstration of a SiC IMPATT diode last year [2]. In this work, the microwave characteristics of the diode are presented.

The cross section of the X-band SiC IMPATT diode is shown in Fig. 1. The fabrication process steps are: mesa isolation, top- and back-side ohmic contacts, and overlaying gold layers. The measured reverse breakdown characteristic of the SiC IMPATT diode is shown in Fig. 2. The breakdown voltage is about 800V. It is found that sustainable avalanche breakdown, which is the pre-requisite for IMPATT operation, is achieved on the device.

IMPATT diodes operate in the reverse breakdown regime, which results in a substantial power dissipation. To avoid excessive heating, the SiC IMPATT diode is biased in pulsed mode. The block diagram of the pulse measurement system used for SiC IMPATT testing is shown in Fig. 3. Two pulse current waveforms are shown in Fig. 4. The large current transients at the turn-on and turn-off of the pulses are due to capacitive charging and discharging. The avalanche current decreases with time over the pulse duration because of device heating. The peak bias current, which is ~ 0.15 A and ~ 0.2 A for the two biasing conditions, is achieved near the onset of breakdown. The device area is 1.227×10^{-4} cm².

The spectral output of the SiC IMPATT diode is shown in Fig. 5. The bias (pulse) current waveforms used for obtaining the spectra are similar to those in Fig. 4, except that the pulse length is reduced to ~ 200 ns for both waveforms. The periodic structures due to the finite pulse duration are clearly visible in the pulse spectra. It can also be seen that the peak oscillation occurs at a higher frequency when the bias current increases, which is a characteristic of 'current tuning' effect in IMPATT operation [3].

A 50 GHz digital sampling oscilloscope is used to obtain the envelope of the microwave oscillation in the time domain. Knowing the voltage amplitude at any moment, the instantaneous microwave power can be calculated and correlated to the diode current. The results are shown in Fig. 6, which plots the instantaneous microwave power versus the diode current for the two bias current waveforms shown in Fig. 4. We observe that the microwave power is a function of the bias current. The maximum power of 15 dBm (32 mW) is attained at a bias current of 0.2 A. The threshold current required to initiate the microwave oscillation is about 0.1 A. Note that, in Fig. 6, the slight difference in the instantaneous power on the two curves at the same bias current is related to device heating.

In summary, we report the experimental performance of the first SiC IMPATT oscillators. The work paves the way for further development of SiC IMPATT diodes in realizing their full potential in high-power microwave applications.

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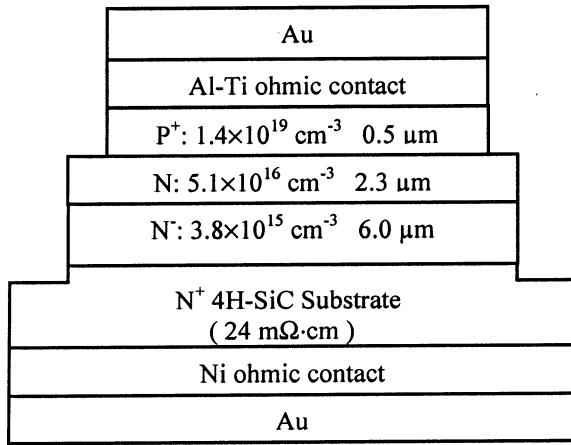


Fig. 1. Schematic cross section of X-band SiC IMPATT diodes.

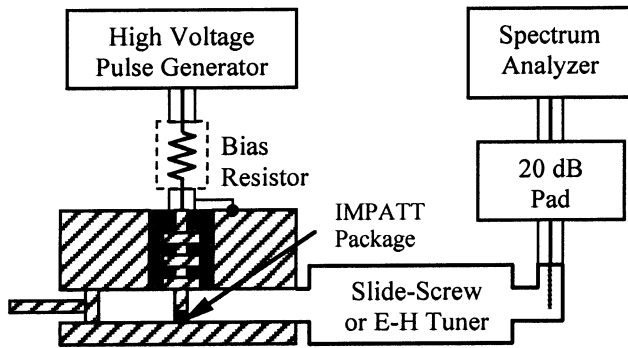


Fig. 3. Schematic diagram of the pulse measurement system for SiC IMPATT diode characterization. The bias current is monitored by a current probe outside the waveguide cavity.

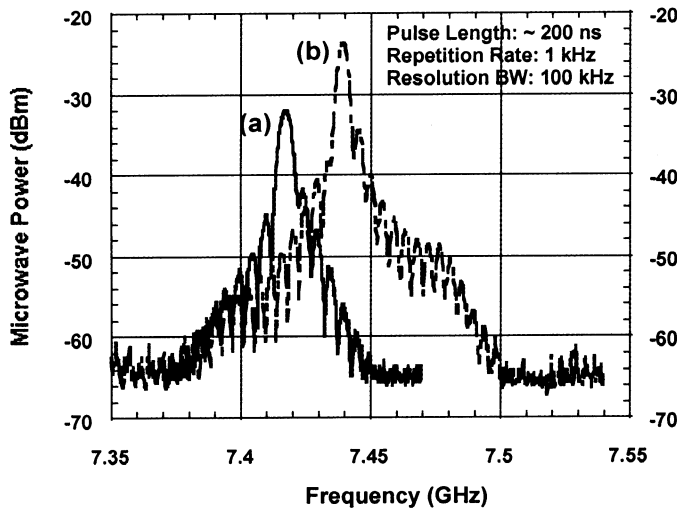


Fig. 5. Spectral output of an X-band SiC IMPATT diode under two biasing conditions. (a): peak bias current ~ 0.15 A and (b): peak bias current ~ 0.2 A.

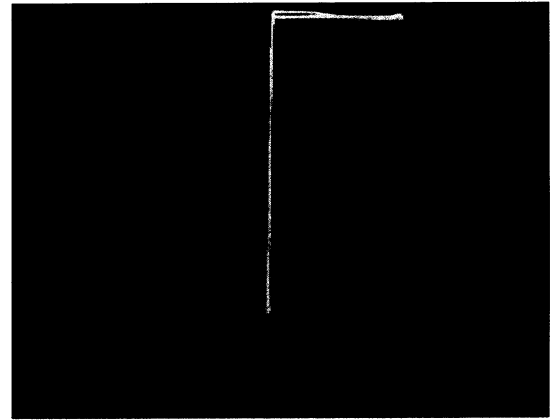


Fig. 2. Reverse breakdown characteristic of an X-band SiC IMPATT diode. Horizontal scale: 200 V/div. Vertical scale: 200 μ A/div.

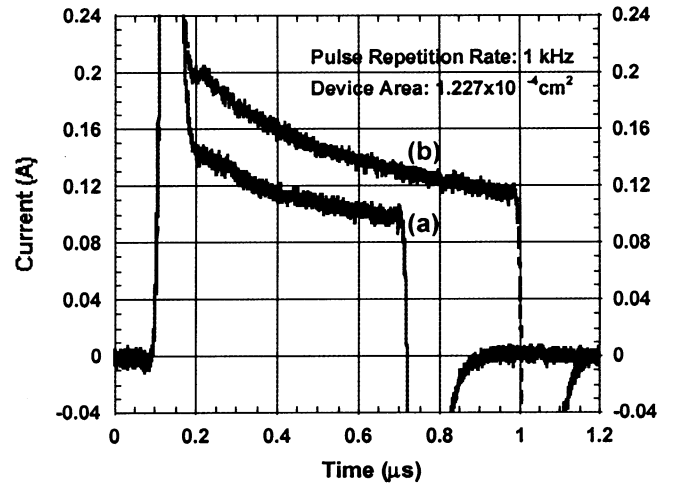


Fig. 4. Bias current waveforms for an X-band SiC IMPATT diode. The peak current is ~ 0.15 A in (a), and ~ 0.2 A in (b).

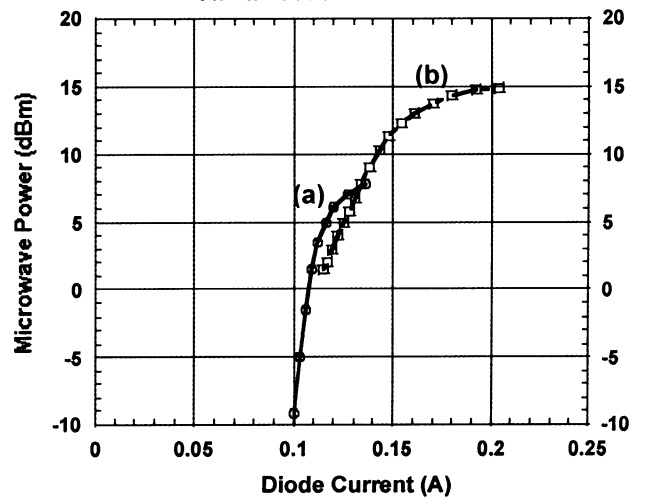


Fig. 6. Instantaneous microwave power vs. bias current for the X-band SiC IMPATT diode. (a): peak bias current ~ 0.15 A and (b): peak bias current ~ 0.2 A.

The Effect of Emitter Implant and Anneal on High-Voltage 4H-SiC BJTs

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In recent years, significant progress has been made in SiC bipolar junction transistors, most of which on epi-emitter bipolar transistors [1-3]. Recently, an 1800 V, 3.8 A epi-emitter bipolar transistor was reported in 4H-SiC by Cree Inc.[2]. The implanted-emitter BJTs are of interest because it offers process flexibility and is an important building block of bipolar devices such as IGBT, MGT, GTO, etc. We reported the first implanted-emitter bipolar transistor in 4H-SiC [3]. The device showed a record-high common emitter current gain of 40, and forward drop of 1V at forward current density of 50A/cm². The open-base breakdown voltage was less than 60V due to the very small base width (<0.2μm).

In this work, improved epi-base, implanted-emitter, npn bipolar junction transistor is reported with increased base width and improved emitter anneal. The devices showed a blocking voltage of 500V and maximum common emitter current gain of 8. Negative temperature coefficient is observed.

The device cross-section is shown in Fig. 1. The nominal thickness and the doping of the P-epi layer and N-drift layer are 1μm, 2×10^{17} cm⁻³, and 12 μm, 4×10^{15} cm⁻³, respectively. The emitter implantation was done at 600°C with different implantation species and annealing cycles, but with the same dose of 3×10^{15} cm⁻². The implantation splits and the measured sheet resistances are shown in Table 1. Previous study has shown that low sheet resistance can be obtained for phosphorus and arsenic at annealing temperature as low as 1200°C [4,5]. Previous lot used phosphorus as the implantation material, but the implantation tail reduced the actual base width and caused the low open-base breakdown voltage [3]. Here we have decreased the emitter trench depth to make the base width bigger than the previous attempt.

The distribution of the common emitter current gain of the four samples and their medians are shown in Fig. 2. At room temperature, maximum common emitter current gain of 8 was measured on 300 μm×300 μm devices of phosphorus 1600°C annealed sample, as shown in Fig. 2. Sample A with nitrogen implantation and 1600°C anneal also gives similar current gain. Comparing to the previous lot, the current gain is much smaller which we attribute to the increased base width for improving blocking characteristics.

Fig. 3 illustrates the effect of temperature on β. In the base region, the background carrier concentration increases with temperature due to increased ionization of deep level acceptors. As a result, β decreases with temperature. This negative temperature coefficient makes this device attractive for paralleling and for preventing thermal run-aways. This feature was also observed in the previous samples [3].

The correlation between open-base breakdown and open-emitter breakdown of the phosphorus 1200°C sample and the previous devices are shown in Fig. 4. The two samples have the same implantation and annealing cycles and went through the same process except that the new sample has a wider base width. The BV_{CEO} is greatly improved from the previous results, and it ranges from below BV_{CBO} to BV_{CBO}/4. The BV_{CBO} limitation is due to the base punch-through. The base width and doping need to be further optimized so as to achieve BV_{CBO} limited by termination design or avalanche breakdown without current gain degradation. The distribution of the BV_{CEO} of the four samples are shown in Fig. 5. The As sample does not show a high blocking voltage, which is attributed to the implantation damage. The other samples show an open-base breakdown voltage ranging from 100V to 500V, the highest blocking being 550V. The increase of the breakdown voltage and the decrease of the current gain are both due to the increase of the base width.

In summary, among the implantation species studied, the phosphorus 1600°C annealed sample shows the lowest sheet resistance, highest current gain and good blocking characteristics.

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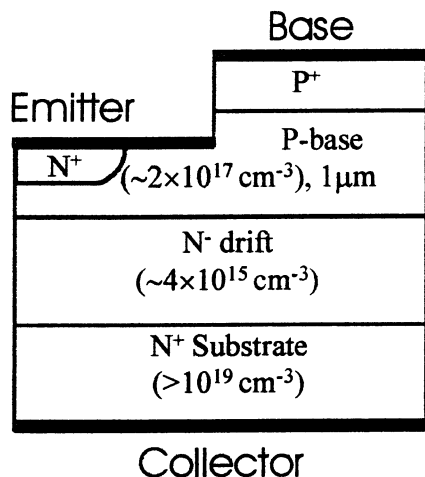


Fig.1 Schematic cross-section of implanted-emitter 4H-SiC BJT studied in this work

Emitter implant species	Annealing temperature (°C)	Annealing time (min)	Sheet resistance (Ω/sq)
phosphorus	1200	30	1200
phosphorus	1600	15	230
arsenic	1200	30	3400
nitrogen	1600	15	3000

TABLE I Emitter implantation splits and measured sheet resistance

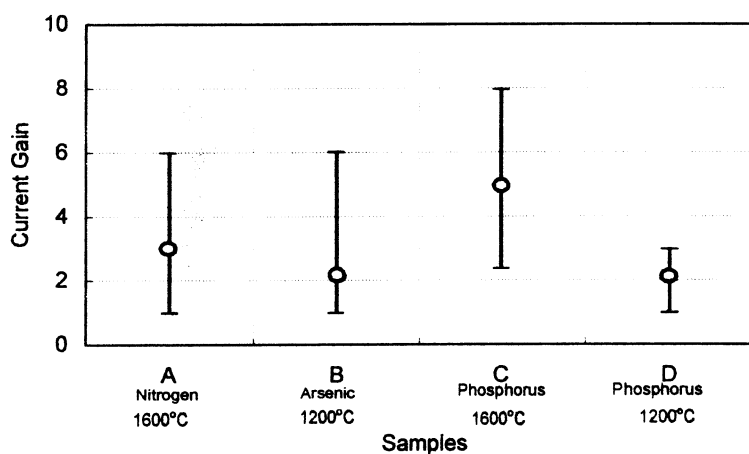


Fig.2 Distribution and median of maximum common emitter current gain at $V_{CE}=10V$

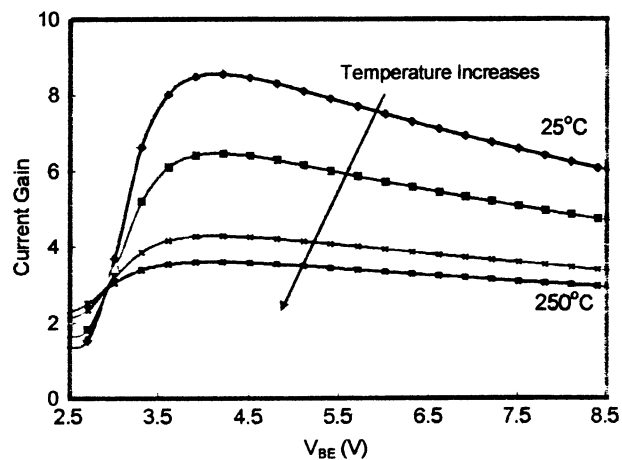


Fig.3 Temperature effect on common emitter current gain of phosphorus 1600°C sample

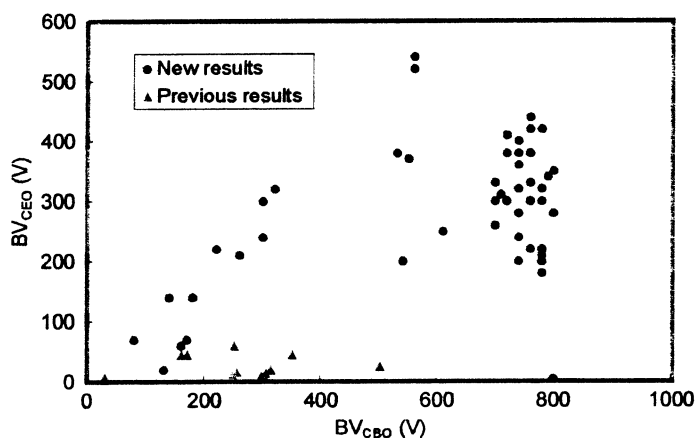


Fig.4 Improvement of open-base breakdown voltage and open-emitter breakdown voltage

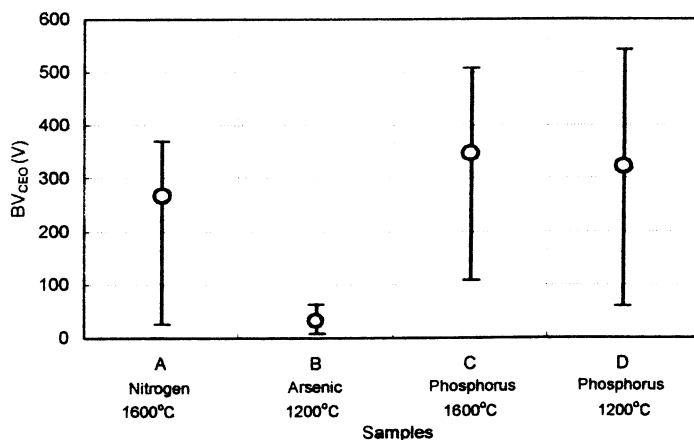


Fig.5 Distribution and median of open-base breakdown voltage

Diamond surface channel FET with $f_{\max}$ above 30GHz

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Diamond FETs are attractive candidates for power applications mainly due to the high breakdown field despite the fact that doping of diamond is only possible for p-type FET devices, however with a high sheet charge density above 10^{13} cm^{-2} and mobilities of 100 to $350 \text{ cm}^2/\text{Vs}$. In this case a hydrogen induced surface channel FET structure was used, in which a sub-surficial hole channel is created by hydrogen plasma treatment. In the micrometer gate length regime such structures have shown excellent breakdown characteristics and have thus been used to evaluate the power handling capability of diamond FETs [1].

In this study the gate length performance between $5.0 \mu\text{m}$ and $0.2 \mu\text{m}$ was investigated, using an experimental self-aligned symmetric gate technology, where the gates were realized by a 3-level e-beam lithography process. Substrates used were synthetic (100) oriented nitrogen doped semi-insulating crystals. The cross section of this device is shown in fig. 1 indicating that the structure is planar with a self aligned source-gate and gate-drain distance of $1.0 \mu\text{m}$ independent of the gate length.

The DC output characteristics of the $0.2\mu\text{m}$ gate length device is displayed in fig. 2. The surface channel FETs are enhancement mode devices. The gate built-in potential of 0.9V (Al) is sufficient to pinch off the sheet charge of $1.35 \cdot 10^{13} \text{ cm}^{-2}$ (see fig. 4). The maximum output current approx. 200mA/mm at a (forward) gate bias of -2.4V despite the high drain saturation voltage of -5V indicating the influence of parasitic resistances. The maximum transconductance g_m reaches 107mS/mm with the g_m/g_{DS} voltage gain still being 10^2 . Also shown in fig. 2 is the bias point for maximum f_T . The cut-off frequencies f_T and $f_{\max}(\text{MAG})$ and $f_{\max}(\text{U})$ were directly extracted from the gain plots as shown in fig. 3. The values for $f_T = 11.8 \text{ GHz}$ and $f_{\max}(\text{MAG}) = 30.6 \text{ GHz}$ and $f_{\max}(\text{U}) = 33.0 \text{ GHz}$ are the highest values obtained for diamond FET devices up to now. The high $f_{\max}/f_T$ ratio is mainly due to the high voltage gain.

The gate length dependence of the current gain cut-off frequency f_T is shown in fig. 4. Again plotted are the maximum f_T values obtained from each FET structure. As expected f_T increases inversely with the gate length. To evaluate the dependence at short gate lengths the relationship is fitted to a analytical MISFET model including field dependant mobility after [2]. For the fit used were $p_s = 1.35 \cdot 10^{13} \text{ cm}^{-2}$, $\mu_0 = 125 \text{ cm}^2/\text{Vs}$, $v_{\text{sat}} = 1.1 \cdot 10^7 \text{ cm/s}$ and a gate capacitance of $C_i = 885 \text{ nF/cm}^2$, where mobility and the sheet charge density are in good agreement with Hall-measurements. Due to the bias point at moderate current levels (see fig. 2) parasitics are basically taken into account by a parasitic gate capacitance and source series resistance.

By extrapolating to even shorter gate lengths performance in the mm-wave regimes may be feasible despite the rather moderate mobility.

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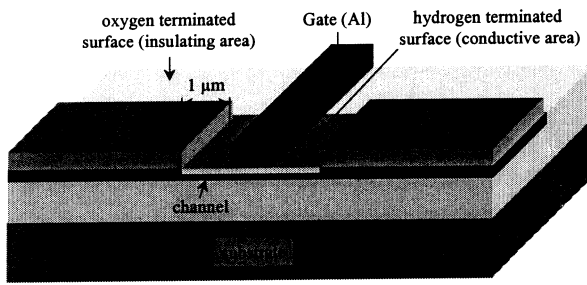


Fig. 1: FET cross section indicating planar device structure. The gate is symmetrically self aligned between source and drain.

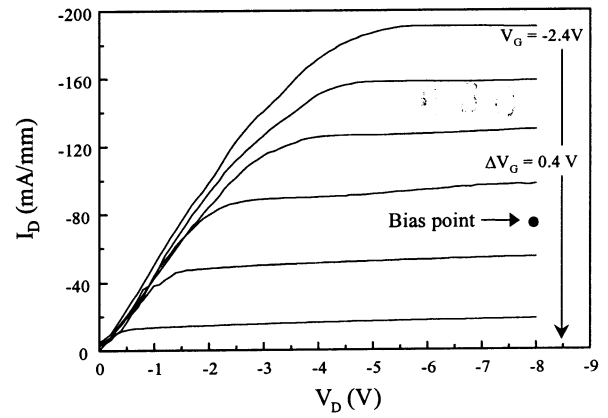


Fig. 2: DC-output characteristics of 0.2 μm gate length device

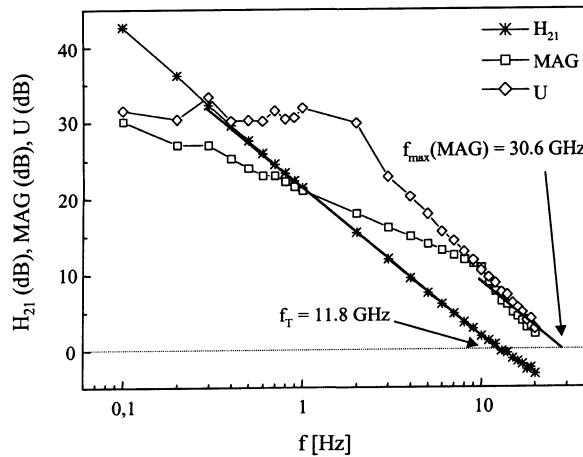


Fig. 3: Frequency dependance of H_{21} , MAG, and U, with extracted values for f_T and $f_{\max}(\text{MAG})$ for the 0.2 μm gate length FET

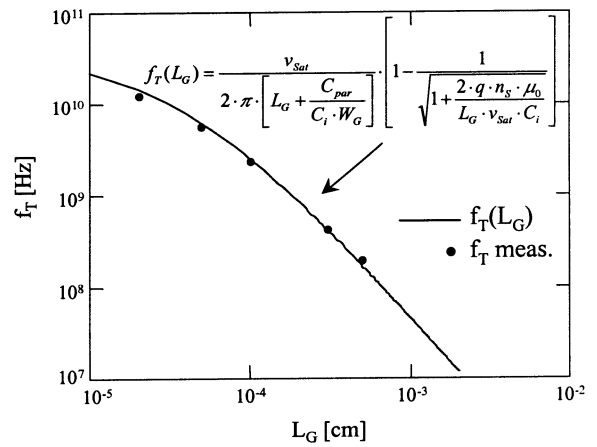


Fig. 4: Gate length dependence of f_T ; measured values and fitting curve according to the given expression. Fitting parameters are $C_i = 885 \text{ nF/cm}^2$ and $v_{\text{sat}} = 1.1 \times 10^7 \text{ cm/s}$. Derived values are $\mu_0 = 125 \text{ cm}^2/\text{Vs}$ and $p_s = 1.35 \times 10^{13} \text{ cm}^{-2}$.

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