Schedule of Events

60TH DEVICE RESEARCH CONFERENCE

SUNDAY PM, JUNE 23RD, 2002

Registration 4:00PM–9:00PM
Location .....University Center/Multicultural Lounge

Welcoming Reception 6:00PM–8:00PM
Location ..... Lagoon Plaza

MONDAY AM, JUNE 24TH, 2002

Registration 7:30AM–5:00PM
Location .....University Center/Multicultural Lounge

Plenary Session 8:30AM
Location ..... Corwin Pavilion

MONDAY PM, JUNE 24TH, 2002

Session II.A. Nitride Electronic Devices 1:40PM
Session II.B. Si-Based Devices 1:30PM
Session III. Poster Session..... 5:30PM–8:30PM

Poster Session Reception 5:30PM–8:30PM
Location .....Lagoon Plaza

TUESDAY AM, JUNE 25TH, 2002

Registration 7:30AM–5:00PM
Location .....University Center/Multicultural Lounge

Session IV. Emerging Technologies 8:30AM

TUESDAY PM, JUNE 25TH, 2002

Session V.A. Optical Devices 2:00PM
Session V.B. Nanoscale & Tunneling Devices 2:10PM

Conference Picnic 6:00PM–8:00PM
Location .....Goleta Beach

Rump Session 8:00PM–10:30PM
Location ..... Corwin East & Corwin West

WEDNESDAY AM, JUNE 26TH, 2002

Registration 7:30AM–1:00PM
Location .....University Center/Multicultural Lounge

Joint Plenary Session with EMC 8:20AM
Session VI.A. III-V Devices 10:00AM
Session VI.B. Late News Papers..... 10:00AM

WEDNESDAY PM, JUNE 26TH, 2002

Session VII.A. Column IV Power Devices 2:00PM
Session VII.B. MOS Dielectrics..... 2:10PM

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SESSION IV. EMERGING TECHNOLOGIES 111–132

(Corwin Pavilion)

Plenary Session

MONDAY AM, JUNE 24TH, 2002

Session Organizer: Sanjay Banerjee, The University of Texas at Austin

Session Chair: Jeffrey Welser, IBM Microelectronics

8:30 AM, Welcoming Remarks
Presentations: IEEE Fellows and Best Student Paper Award

9:00 AM, I.-1 Plenary
From Electron Tubes to Nanostructures: 60 Years of Electron Device Research: *H. Kroemer*[1]; [1]University of California at Santa Barbara, Dept. of Electl. & Compu. Eng., & Dept. of Matls., Santa Barbara, CA 93106 USA

9:50 AM Break

Special MEMS Session

10:15 AM I.-2 Invited
RF MEMs for Wireless Applications: *C. T.-C. Nguyen*[1]; [1]University of Michigan, Ctr. for Wireless Microsys., Ann Arbor, MI 48109 USA

10:45 AM I.-3 Invited
Advanced MEMs for Photonics: M. C. Wu[1]; P. R. Patterson[1]; D. Hah[1]; M. C.M. Lee[1]; S. Huang[1]; J.-C. Tsai[1]; [1]University of California at Los Angeles, Electl. Eng. Dept. & California NanoSystem Inst. (CNSI), Los Angeles, CA 90095 USA

11:15 AM I.-4 Invited
Bio-MEMs: The Impact of MEMs on Biotechnology in the 21st Century: *M. Madou*[1]; C. Gurtner[1]; [1]Nanogen, 10398 Pacific Ctr. Ct., San Diego, CA 92121 USA

Session II.A. *(Corwin East)*

Nitride Electronic Devices

MONDAY PM, JUNE 24TH, 2002

Session Organizer: Bobby Brar, Rockwell Scientific Company

Session Chair: Chanh Nguyen, GCS Corp

1:40 PM II.A-1
Submicron Enhancement-Mode AlGaN/GaN HEMTs: *J. S. Moon*[1]; D. Wong[1]; T. Hussian[1]; M. Micovic[1]; P. Deelman[1]; M. Hu[1]; M. Antcliffe[1]; C. Ngo[1]; P. Hashimoto[1]; L. McCray[1]; [1]HRL Laboratories, LLC, 3011 Malibu Canyon Rd., Malibu, CA 90265 USA

2:00 PM II.A-2
p-GaN/AlGaN/GaN High Electron Mobility Transistors: *R. Coffie*[1]; S. Heikman[1]; D. Buttari[1]; S. Keller[1]; A. Chini[1]; L. Shen[1]; N. Zhang[1]; A. Jimenez[1]; D. Jena[1]; U. K. Mishra[1]; [1]University of California, Dept. of ECE, Santa Barbara, CA 93106 USA

2:20 PM II.A-3
3.2 W/mm, 71% PAE AlGaN/GaN HEMT Operation at 20GHz: *R. Sandhu*[1]; M. Wojtokwicz[1]; I. Smorchkova[1]; M. Barsky[1]; R. Tsai[1]; J. W. Yang[2]; H. Wang[2]; M. A. Khan[2]; [1]TRW, Elect. & Tech. Div., One Space Park, Redondo Beach, CA 90278 USA; [2]University of South Carolina, Dept. of Electl. Eng., Columbia, SC 29208 USA

2:40 PM II.A-4
p-Channel GaN/AlGaN Heterostructure Junction Field Effect Transistor: *A. Koudymov*[1]; M. Shatalov[1]; G. Simin[1]; J. Zhang[1]; V. Adivarahan[1]; M. Asif Khan[1]; [1]University of South Carolina, Dept. of Electl. Eng., Columbia, SC 29208 USA

3:00 PM Break

3:20 PM II.A-5
AlGaN/GaN Current Aperture Vertical Electron Transistors: *I. Ben-Yaacov*[1]; Y.-K. Seck[1]; S. Heikman[1]; S. P. DenBaars[1]; U. K. Mishra[1]; [1]University of California, ECE Dept., Santa Barbara, CA 93106-9560 USA

3:40 PM II.A-6
AlGaN/GaN HEMTs Grown by MBE on Semi-Insulating HVPE GaN Templates: *N. G. Weiman*[1]; M. J. Manfra[1]; J. W.P. Hsu[1]; L. N. Pfeiffer[1]; K. W. West[1]; D. V. Lang[2]; R. J. Molnar[3]; [1]Lucent Technologies Bell Laboratories, Murray Hill, NJ 07974 USA; [2]Agere Systems, Murray Hill, NJ 07974 USA; [3]MIT Lincoln Labs, Lexington, MA 02420 USA

Session II.B. *(Corwin West)*

Si-Based Devices

MONDAY PM, JUNE 24TH, 2002

Session Organizer: Ed Nowak, IBM Microelectronics

Session Chair: David Fried, Cornell University

1:30 PM II.B-1 Invited
Strained-Si- and SiGe-On-Insulator (Strained-SOI and SGOI) MOSFETs for High Performance/Low Power CMOS Application: *S. Takagi*[1]; [1]Toshiba Corporation, MIRAI Project, MIRAI-ASET; Adv. LSI Tech. Lab., 1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki 210-8582 Japan

2:00 PM II.B-2
Performance-Augmented CMOS Using Back-End Uniaxial Strain: *R. E. Belford*[1]; W. Zhao[2]; J. Potashnik[2]; Q. Liu[2]; A. Seabaugh[2]; [1]Belford Research, Inc., Hilton Head, SC 29926 USA; [2]University of Notre Dame, Dept. of Electl. Eng., Notre Dame, IN 46556 USA

2:20 PM II.B-3
Electron Inversion Layer Mobility in Strained-Si *n*-MOSFETs with High Channel Doping Concentration Achieved by Ion Implantation: *H. M. Nayfeh*[1]; J. L. Hoyt[1]; C. W. Leitz[2]; A. J. Pitera[2]; E. A. Fitzgerald[2]; D. A. Antoniadis[1]; [1]Massachusetts Institute of Technology, Microsys. Tech. Lab., 60 Vassar St., MIT 39-617, Cambridge, MA 02139 USA; [2]Massachusetts Institute of Technology, Dept. of Matls. Sci. & Eng., 60 Vassar St., Cambridge, MA 02139 USA

2:40 PM II.B-4
Nano-Scale Implantless Schottky-Barrier SOI FinFETs with Excellent Ambipolar Performance: *H.-C. Lin*[1]; M.-F. Wang[2]; F.-J. Hou[1]; J.-T. Liu[1], F.-H. Ko[1]; H.-L. Chen[1]; G.-W. Huang[1]; T.-Y. Huang[1]; S. M. Sze[1]; [1]National Nano Device Laboratories, 1001-1 Ta-Hsueh Rd, Hsin-Chu, Taiwan; [2]National Chiao-Tung University, Inst. of Elect., Hsin-Chu, Taiwan

3:00 PM Break

3:20 PM II.B-5
Demonstration of FinFET CMOS Circuits: *B. A. Rainey*[1]; D. M. Fried[1]; M. Ieong[2]; J. Kedzierski[3]; E. J. Nowak[1]; [1]IBM Microelectronics Division, Essex Junction, VT, USA; [2]IBM Semiconductor Research and Development Center, E. Fishkill, NY, USA; [3]IBM Research Division, Yorktown Heights, NY, USA

3:40 PM II.B-6
High Performance Sub-100nm Si Thin-Film Transistors by Pattern-Controlled Crystallization of Thin Channel Layer and High Temperature Annealing: *J. Gu*[1]*;* W. Wu[1]; S. Y. Chou[1]; [1]Princeton University, NanoStructure Lab., Dept. of Electl. Eng., Princeton, NJ 08544 USA

4:00 PM II.B-7
Proposal of N-Channel Heterostructure Dynamic Threshold-Voltage MOSFET (HDTMOS) with P-Type Doped SiGe Body: *T. Kawashima*[1]; T. Takagi[1]; Y. Hara[1]; Y. Kanzawa[1]; A. Inoue[1]; H. Sorada[1]; K. Nozawa[1]; A. Asai[1]; T. Ohnishi[1]; M. Kubo[1]; [1]Matsushita Electric Industrial Company, Ltd., Adv. Tech. Rsrch. Lab., 3-1-1, Yagumo-Nakamachi, Moriguchi, Osaka 570-8501 Japan

4:20 PM II.B-8
90 GHz F_t SiGe HFET with Fully Optical Self-Aligned Sub-100nm Gate: *M. Zeuner*[1]; A. Fox[2]; T. Hackbarth[1]; D. Behammer[3]; U. Konig[1]; [1]Daimler Chrysler Research Center Ulm, Wilhelm-Runge-Str. 11, Ulm D-89081 Germany; [2]IHP, Im Technologiepark 25, D-15236 Frankfurt(0der); [3]United Monolithic Semiconductors GmbH, Wilhelm-Runge-Str. 11, Ulm D-89081 Germany

III.-1
Reliability and ESD for High Voltage LDMOS with SenseFET: *Y. S. Choi*[1]; J. J. Kim[1]; C. K. Jeon[1]; M. H. Kim[1]; S. L. Kim[1]; H. S. Kang[1]; C. S. Song[1]; [1]Fairchild Semiconductor, 82-3, Dodang-Dong, Wonmi-Ku, Puchon, Kyonggi-Do 420-711 Korea

III.-2
A Novel Variational Approach for Modeling Sub-0.1 Micron MOS Devices Including Quantum Mechanical Interface Charge Confinement Effects: *N. G. Gunther*[1]; A. A. Mutlu[1]; M. Rahman[1]; [1]Santa Clara University, Dept. of Electl. Eng., Santa Clara, CA 95053-0569 USA

III.-3
Nickel Induced Crystallization of a-Si Gate Electrode at 500°C and Gate Oxide Reliability: *A. R. Joshi*[1]; K. C. Saraswat[1]; [1]Stanford University, CIS 006, 420 Via Ortega, Stanford, CA 94305-4070 USA

III.-4
Stable Breakdown Characteristics of 600V LDMOS by Extended P-Bottom Region: *S. L. Kim[1];* C. K. Jeon[1]; J. J. Kim[1]; Y. S. Choi[1]; M. H. Kim[1]; H. S. Kang[1]; C. S. Song[1]; [1]Fairchild Semiconductor, New Tech. Dvpt. Team, Puchon, Kyonggi-Do 420-711 Korea

III.-5
Symmetry Realization of BSIM Model with Dynamic Reference Method for Circuit Simulation: *X. Xi*[1]; K. Cao[1]; J. He[1]; H. Wan[1]; M. Chan[1]; C. Hu[1]; [1]University of California, Dept. of Electl. Eng. & Compu. Sci., Berkeley, CA 94720 USA

III.-6
Newly Designed Isolated RESURF LDMOS Transistor for 60V BCD Process Provides 20V Vertical NPN Transistor: *T. H. Kwon*[1]; Y. S. Jeoung[1]; S. K. Lee[1], Y. C. Choi[1]; C. J. Kim[1]; H. S. Kang[1]; C. S. Song[1]; [1]Fairchild Korea Semiconductor Process Development Group, 82-3, Dodang-Dong, Wonmi-Ku, Puchon, Kyunggi-Do, Korea

III.-7
High Performance 40-GHz Bandpass Filters on Si Using Proton Implantation: *K. T. Chan*[1]; C. Y. Chen[1]; A. Chin[1]; J. C. Hsieh[2]; J. Liu[2]; T. S. Duh[3]; W. J. Lin[3]; [1]National Chiao Tung University, Dept. of Elect. Eng., Hsinchu, Taiwan; [2]United Microelectronics Cooperation, Hsinchu, Taiwan; [3]Institute of Nuclear Energy Research, Taoyuan, Taiwan

III.-8
RF Noise in Deep Sub-µm MOSFETs and Proposed Solution: *C. H. Huang*[1]; C. H. Lai[1]; J. C. Hsieh[2]; J. Liu[2]; A. Chin[1]; [1]National Chiao Tung University, Dept. of Elect. Eng., Hsinchu, Taiwan; [2]United Microelectronics Cooperation, Hsinchu, Taiwan

III.-9
An Enhanced Compact Waffle MOSFET for RF Integrated Circuits: *S. Lam*[1]; W. H. Ki[1]; P. K. Ko[1]; M. Chan[1]; [1]Hong Kong University of Science & Technology, Dept. of Electl. & Elect. Eng., Hong Kong

III.-10
Improved MOSFET Electron Mobility for Advanced Gate Dielectric Stacks: *I. Polishchuk*[1]; K. J. Yang[1]; T.-J. King[1]; C. Hu[1]; [1]University of California, Dept. of Electl. Eng. & Compu. Scis., Berkeley, CA 94720 USA

III.-11
Speed Advantage of Optimized Metal S/D in 25 nm Dual-Gate Fully-Depleted CMOS: *D. Connelly*[1]; D. Grupp[1]; D. Yergeau[2]; [1]Acorn Technologies; [2]Stanford University, CA, USA

III.-12
Normal Incidence Long-Wave Infrared InAs/In0.15Ga0.85As DWELL Detectors Operating at 8.2µm: *S. Krishna*[1]; S. Raghavan[1]; B. Fuchs[1]; A. Stintz[1]; K. Malloy[1]; C. Morath[2]; D. Le[2]; D. A. Cardimona[2]; [1]University of New Mexico, Ctr. for High Tech. Matls., EECE Dept., Albuquerque, NM 87106 USA; [2]Air Force Research Lab (AFRL/VSSS) 3550 Aberdeen Ave. S.E., Bldg. 426, Kirtland AFB, NM 87117 USA

III.-13
High Luminous Flux Mirror-Substrate AlGaInP Large-Area Emitters: *R. H. Horng*[1]; D. S. Wuu[2]; S. H. Huang[1]; C. R. Chung[3]; [1]National Chung Hsing University, Inst. of Precision Eng., Taichung 402 Taiwan; [2]National Chung Hsing University, Dept. of Matls. Eng., Taichung 402 Taiwan; [3]Da-Yeh University, Inst. of Electl. Eng., Chang-Hwa 515, Taiwan

III.-14
SiGe-Channel 0.1-µm pMOSFETs with Super Self-Aligned Ultra-Shallow Junction Formed by Selective In-Situ B-Doped SiGe CVD: *D. Lee*[1]; M. Sakuraba[1]; T. Matsuura[1]; J. Murota[1]; T. Tsuchiya[2]; [1]Tohoku University, Lab. for Elect. Intelligent Sys., Res. Inst. of Elect. Comm., 2-1-1 Katahira, Aoba-ku Sendai 980-8577 Japan; [2]Shimane University, Interdisciplinary Fac. of Sci. & Eng., Matsue, Shimane 690-8504 Japan

III.-15
Multiple Delta-Doped Layer Structures for Silicon Power MOSFETs: *C. Tolksdorf* [1]; J. Schulze[1]; T. Sulima[1]; I. Eisele[1]; G. Deboy[2]; [1]Universitat der Bundeswehr Munich, Inst. of Physics, Fac. EE & IT, Werner-Heisenberg-Weg 39, Neubiberg 85577 Germany; [2]Infineon Technologies AG Munich, Balanstrasse 73, Munchen 81541 Germany

III.-16
GaAs Schottky Varactor Diode Optimization for High-Performance Nonlinear Transmission Lines: *D. Sawdai*[1]; D. Ko[1]; M. Kintis[1]; S. Maas[2]; X. Zhang[1]; S. Valdes[1]; E. Garber[1]; G. Barber[1]; E. Quach[1]; J. Newman[1]; F. Fong[1]; [1]TRW, Inc., Space & Elect. Grp., One Space Park, D1/1302, Redondo Beach, CA 90278 USA; [2]Nonlinear Technologies, Inc.

III.-17
A Novel Horizontal Current Bipolar Transistor (HCBT) for Vertical BiCMOS Integration: T. Suligoj[1]; P. Biljanovic[2]; K. L. Wang[1]; [1]University of California at Los Angeles, Device Rsrch. Lab., Dept. of Electl. Eng., Los Angeles, CA 90095 USA; [2]University of Zagreb, Fac. of Electl. Eng. & Computing, Unska3, Zagreb HR-10000 Croatia

III.-18
The Effect of Scattering on Drive Current of Nanotransistors: *A. Svizhenko*[1]; M. P. Anantram[1]; [1]NASA Ames Research Center, MS T27A-1, Moffett Field, CA 94035-1000 USA

III.-19
Optoelectronic Conversion through 850nm Band Single Mode Si_3N_4 Photonic Waveguides for Si-On-Chip Integration: *T. Matsuura*[1]; A. Yamada[1]; J. Murota[1]; E. Tamechika[2]; K. Wada[3]; L. C. Kimerling[3]; [1]RIEC Tohoku University, Katahira, Aoba-ku, Sendai 980-8577 Japan; [2]NTT Photonics Laboratories, Atsugi 243-0198; [3]MIT, Microph, Ctr., MA 02139 USA

III.-20
InP Hot Electron Transistor with a Buried Metallic Gate for Electron Emission: *Y. Miyamoto*[1]; R. Yamamoto[1]; H. Maeda[1]; K. Takeuchi[1]; L.-E. Wernersson[2]; K. Furuya[1]; [1]Tokyo Institute of Technology, Dept. of Electl. & Elect. Eng., 2-12-1 O-okayama, Meguru-ku, Tokyo 152-8552 Japan; [2]Lund University, Solid State Physics/Nanometer Structure Consortium, Box 118, Lund S-22100 Sweden

III.-21
Memory Device Based on a Ferroelectric Tunnel Junction: *J. Rodriguez Contreras*[1,3]; J. Schubert[2]; H. Kohlstedt[1]; R. Waser[1]; [1]Institut fur Festkorperforschung, Julich 52425 Germany; [2]Institut fur Schichten und Grenzflachen, Julich 52425 Germany

III.-22
Thermal Management and Device Failure Assessment of High-Power AlGaN/GaN HFETs: *M. Kuball*[1]; S. Rajasingam[1]; A. Sarua[1]; J. M. Hayes[1]; M. J. Uren[2]; T. Martin[2]; R. S. Balmer[2]; B. T. Hughes[2] ; K. P. Hilton[2]; [1]University of Bristol, H. H. Wills Physics Lab., Bristol BS8 1TL UK; [2]QinetiQ Ltd., St. Andrew's Rd., Malvern, Worcs WR14 3PS UK

III.-23
Room Temperature Grown Zirconia/SiO_2 Dielectric Stacks with 1 nm EOT: *S. Ramanathan*[1]*;* P. C. McIntyre[1]; [1]Stanford University, Dept. of Matls. Sci. & Eng., Stanford, CA 94305 USA

III.-24
Graph-Based Quantum Integrated Circuits Using III-V Multi-Branch Nanowire Networks and their Nano-Schottky Gate Control: S. Kasai[1]; M. Yumoto[1]; T. Fukushi[1]; T. Muranaka[1]; H. Hasegawa[1]; [1]Hokkaido University, Rsrch. Ctr. for Integrated Quantum Elect. & Grad. Sch. of Elect. & Info. Eng., N-13, W-8, Kita-ku, Sapporo 060-8628 Japan

III.-25
Tunneling through Multi-Layer Gate Dielectrics-An Analytical Model: *I. Polishchuk*[1]*;* Y.-C Yeo[1]; T.-J. King[1]; C. Hu[1]; [1]University of California, Dept. of EECS, Berkeley, CA 94720 USA

III.-26
Ultra High Fmax InP/InGaAs/InP Transferred Substrate DHBTs: *S. Lee*[1]; M. Urteaga[1]; Y. Wei[1]; Y. Kim[1]; M. Dahlström[1]; S. Krishnan[1]; M. Rodwell[1]; [1]University of California, Dept. of ECE, Santa Barbara, CA 93106 USA

III.-27
Simulation of Quantum and Scattering Effects Along the Channel of Ultra-Scaled Si-Based MOSFETs: *W. Chen*[1]; L. F. Register[1]; S. K. Banerjee[1]; [1]University of Texas at Austin, Microelect. Rsrch. Ctr., R9950, Austin, TX 78758 USA

Session IV. *(Corwin East)*

Emerging Technologies

TUESDAY AM, JUNE 25TH, 2002

Session Organizer: Jeffrey Welser, IBM Microelectronics

Session Chair: Hagen Klauk, Infineon Technologies

8:30 AM IV.-1 Invited
Hybrid-Gate Suspended Field-Effect Transistors for Gas Sensing: *I. Eisele*[1]; M. Zimmer[1]; [1]Universität der Bundeswehr München, Inst. of Physics, Fac. of Electl. Eng. & Info. Tech., Neubiberg 85577 Germany

9:00 AM IV.-2 Invited
Manipulation of Ferromagnetism in Magnetic Semiconductor Field Effect Transistors: *H. Ohno*[1]; [1]Tohoku University, Rsrch. Inst. of Electl. Comm., Katahira 2-1-1, Aoba-ku, Sendai 980-8577 Japan

9:30 AM IV.-3 Invited
Molecular-Scale Transistors Based on Self-Assembled Monolayers: *J. H. Schön*[1]; [1]Bell Laboratories, Lucent Technologies, 600 Mountain Ave., Murray Hill, NJ 07974 USA

10:00 AM Break

10:20 AM IV.-4 Invited
Designing In-Vitro Patterned Neuronal Network: *B. C. Wheeler*[1]; [1]University of Illinois at Urbana-Champaign, Electl. & Compu. Eng. Dept. & Beckman Inst., 405 N. Mathews Ave., Urbana, IL 61801 USA

10:50 AM IV.-5 Invited
Structured Cold Point Thermoelectric Coolers: *U. Goshal*[1]; [1]Austin Research Laboratory, IBM Rsrch., 11400 Burnet Rd., Austin, TX 78758 USA

11:20 AM IV.-6 Invited
The Second Revolution–Mixed-Technology Integrated Microsystems: *T. E. Zipperian*[1]; [1]Sandia National Laboratories, Microsys. Sci., Tech. & Components, PO Box 5800, Albuquerque, NM 87185-1077 USA

Session V.A. *(Corwin East)*

Optical Devices

TUESDAY PM, JUNE 25TH, 2002

Session Organizers: Kent Choquette, University of Illinois at Urbana-Champaign

Session Chair: Tom Zipperian, Sandia National Laboratories

2:00 PM V.A-1 Invited
Quantum Dot Lasers: Temperature Insensitive Operation and the Prospect for High Speed Modulation: *D. G. Deppe*[1]; O. B. Shchekin[1]; [1]University of Texas at Austin, Microelect. Rsrch. Ctr., Austin, TX 78712 USA

2:30 PM V.A-2
Quantum Dot Tunnel Injection Lasers with Large Modulation Bandwidth at Room Temperature: *S. Ghosh*[1], P. Bhattacharya[1]; Z-K. Wu[1]; T. Norris[1]; J. Singh[1]; B. Kochman[1]; [1]University of Michigan, Dept. of Elect. Eng. & Compu. Sci., Ann Arbor, MI 48109-2122 USA

2:50 PM V.A-3
A 1.5 µm GaInNAs(Sb) Laser Grown on GaAs by MBE: *W. Ha*[1]; V. Gambin[1]; S. Bank[1]; M. Wistey[1]; H. Yuen[1]; S. Kim[1]; J. S. Harris, Jr.[1]; [1]Stanford University, Solid State & Photonics Lab., CISX B113-3, Via Ortega, Stanford, CA 94305 USA

3:10 PM Break

3:30 PM V.A-4
Technology and Performance of Submicron Metal-Semiconductor-Metal GaN Ultraviolet Detectors: *T. Palacios*[1]; E. Monroy[1,2]; F. Calle[1]; F. Omnes[3]; [1]Universidad Politecnica de Madrid, ISOM & Dpto. Ingenieria Electronica, ETSI de Telecomunicacion, Ciudad Universitaria, s/n Madrid 28040 Spain; [2]CEA, Dept. De Recherchce Fondamentale sur la Matiere Condensee, Grenoble Cedex 9, 38054 France; [3]Centre de Recherche sur l'Hetero-Epitaxie et ses Applications, CNRS, Valbonne 06560 France

3:50 PM V.A-5
GaAlAs/GaAs Micromachined Tunable Vertical Filter with Low Tuning Voltage Below 5 Volts: *T. Amano*[1]; F. Koyama[1]; T. Hino[1]; M. Arai[1]; A. Matsutani[1]; [1]Tokyo Institute of Technology, Microsys. Rsrch. Ctr., Precision & Intelligence Lab., 4259 Nagatsuta, Midori-ku, Yokohama 226-8503 Japan

4:10 PM V.A-6 Invited
Polymer LEDs and LASERs for Integrated Optics: *M. D. McGehee*[1]; [1]Stanford University, Dept. of Matls. Sci. & Eng., Bldg. 550, Stanford, CA 94305 USA

Session V.B. *(Corwin West)*

Nanoscale & Tunneling Devices

TUESDAY PM, JUNE 25TH, 2002

Session Organizer: Vivek Subramanian, University of California at Berkeley

Session Chair: Nick Lindert, Intel

2:10 PM V.B-1
Contact Printing with Nanometer Resolution: *Y. L. Loo*[1]; R. L. Willett[1]; K. W. Baldwin[1]; J. A. Rogers[1]; [1]Bell Laboratories, Lucent Technologies, 600 Mountain Ave., Murray Hill, NJ 07974 USA

2:30 PM V.B-2
Charge Retention Characteristics of SiGe Quantum Dot Flash Memories: *D.-W. Kim*[1]; F. E. Prins[1]; T. Kim[1]; D.-L. Kwong[1]; S. Banerjee[1]; [1]University of Texas at Austin, Microelect. Rsrch. Ctr., Austin, TX 78712 USA

2:50 PM V.B-3
Multilayer Tunneling Barriers for Nonvolatile Memory Applications: *P. Blomme*[1,2]; B. Govoreanu[1,2]; M. Rosmeulen[1,2]; J. Van Houdt[1]; K. DeMeyer[1,2]; [1]IMEC, STDI Div., Kapeldreef 75, Leuven 3001 Belgium; [2]ESAT, KU Leuven, Kasteelpark Arenberg 10, Leuven 3001 Belgium

Break 3:10 PM

3:30 PM V.B-4
A Resonant Tunneling Permeable Base Transistor with Al-Free Tunneling Barriers: E. Lindstrom[1]; I. Pietzonka[1]; W. Seifert[1]; L. E. Wernersson[1]; [1]Lund University, Solid State Physics/Nanometer Consortium, Box 118, S-22100 Sweden

3:50 PM V.B-5
Room Temperature Negative Differential Resistance in AIN/GaN Double Barrier Resonant Tunneling Diodes Grown by RF-Plasma Assisted Molecular Beam Epitaxy: *A. Kikuchi*[1]; R. Bannai[1]; K. Kishino[1]; [1]Sophia University, Electl. & Elect. Eng., 7-1, Kioi-cho, Chiyoda-ku, Tokyo 102-8554 Japan

4:10 PM V.B-6
A Novel Frequency-Doubling Device Based on Three-Terminal Ballistic Junction: *I. Shorubalko*[1]; H. Q. Xu[1]; I. Maximov[1]; D. Nilsson[1]; P. Omling[1]; L. Samuelson[1]; W. Seifert[1]; [1]Lund University, Solid State Physics & the Nanometer Consortium, Box 118, Lund SE-22100 Sweden

Session VI.A. *(Corwin East)*

III-V Devices

WEDNESDAY AM, JUNE 26TH, 2002

Session Organizers: Yasuyuki Miyamoto, Tokyo Institute of Technology

Session Chair: Aaron Oki, TRW

10:00 AM VI.A-1 Invited
InP-Based HEMTs with a Cutoff Frequency Higher than 450 Ghz: *K. Shinohara*[1]; Y. Yamashita[2]; A. Endoh[2]; K. Hikosaka[2]; T. Matsui[1]; T. Mimura[2]; S. Hiyamizu[3]; [1]Communications Research Laboratory, 4-2-1 Nukui-kitamachi, Koganei, Tokyo 184-8795 Japan; [2]Fujitsu Laboratories, Ltd, Kanagawa, Japan; [3]Osaka University, Osaka, Japan

10:30 AM VI.A-2
Suppression of Drain Conductance Frequency Dispersion in InP-Based HEMTs by Eliminating Hole Accumulation: *T. Arai*[1]; K. Sawada[1]; N. Okamota[1]; K. Makiyama[1]; T. Takahashi[1]; N. Hara[1]; [1]Fujitsu Laboratories, Ltd., 10-1 Morinosato-Wakamiya, Atsugi, Kanagawa 243-0197 Japan

10:50 AM VI.A-3
Thermal Performance of Metamorphic Double Heterojunction Bipolar Transistors with InP and InAlP Buffer Layers: *Y. M. Kim*[1]; M. Dahlström[1]; M. J.W. Rodwell[1]; A. C. Gossard[1]; [1]University of California, Dept. of ECE, Santa Barbara, CA 93106 USA

11:10 AM VI.A-4
InAlAs/InGaAs/InP DHBTs with Polycrystalline InAs Extrinsic Emitter Regrowth: *D. Scott*[1]; H. Xing[1]; S. Krishnan[1]; M. Urteaga[1]; N. Parthasarathy[1]; M. Rodwell[1]; [1]University of California, Dept. of ECE, Santa Barbara, CA 93106 USA

Session VII.A. *(Corwin East)*

Column IV Power Devices

WEDNESDAY PM, JUNE 26TH, 2002

Session Organizer: Jeff Casady, Mississippi State University

Session Chair: Jesse Tucker, General Electric Corporate R&D

2:00 PM VII.A-1 Invited
High Power Hybrid and MMIC Amplifiers using Wide-Bandgap Semiconductor Devices on Semi-Insulating SiC Substrates: *S. T. Sheppard*[1]; R. P. Smith[1]; W. L. Pribble[1]; Z. Ring[1]; T. Smith[1]; S. T. Allen[1]; J. Milligan[1]; J. W. Palmour[1]; [1]Cree, Inc., 4600 Silicon Dr., Durham, NC 27703 USA

2:30 PM VII.A-2
A Silicon Carbide Self-Aligned and Ion Implanted Static Induction Transistor (SAI-SIT) for 150 Watt S-Band Operation: *T. J. Knight*[1]; R. C. Clarke[1]; R. R. Barron[1]; J. A. Ostop[1]; B. A. Morick[1]; J. R. Gigante[1]; W. J. Malkowski[1]; A. W. Morse[1]; G. C. DeSalvo[1]; K. J. Petrosky[1]; W. R. Curtice[2]; [1]Northrup Grumman Corporation, Baltimore, MD 21090 USA; [2]W. R. Curtice Consulting, Washington Crossing, PA 18977 USA

2:50 PM VII.A-3
First Diamond FET RF Power Measurement on Diamond Quasi-Substrate: A. Aleksov[1]; M. Kubovic[1]; N. Kaeb[1]; U. Spitzberg[1]; I. Daumiller[1]; Th. Bauer[2]; M. Schreck[2]; B. Stritzker[2]; E. Kohn[1]; [1]University of Ulm, Dept. of Electron Devices & Circuits, Albert-Einstaein-Allee 45, Ulm D-89081 Germany; [2]Universitaet Augsburg, Inst. fuer Physik, Augsburg D-86135 Germany

3:10 PM Break

3:30 PM VII.A-4
4H-SiC Power Bioplar Transistors with Common Emitter Current Gain > 50: *C.-F. Huang*[1]; J. A. Cooper, Jr.[1]; [1]Purdue University, Sch. of ECE, W. Lafayette, IN 47907-1285 USA

3:50 PM VII.A-5
Self-Aligned Extended-Drain with Compensating Ion-Implantation for Extended-SOA in 30V Lateral MOS: *S. K. Lee*[1]; C. J. Kim[1]; Y. C. Choi[1]; T. H. Kwon[1]; Y. S. Jung[1]; H. S. Kang[1]; C. S. Song[1]; [1]Fairchild Korea Semiconductor Process Development Group, 82-3, Dodang-Dong, Wonmi-Ku, Puchon, Kyunggi-Do, Korea

Session VII.B. *(Corwin West)*

MOS Dielectrics

WEDNESDAY PM, JUNE 26TH, 2002

Session Organizer: Leonard Franklin Register, University of Texas at Austin

Session Chair: Jack Lee, University of Texas at Austin

2:10 PM VII.B-1
Direct Evidence for Multiple Vibrational Excitation of Si-H/D Bonds for Hot-Carrier Degradation of MOS Transistors: *Z. Chen*[1]; P. Ong[1]; [1]University of Kentucky, Dept. of Electl. & Computer Eng. & Ctr. for Micro-Magnetic & Elect. Devices, Lexington, KY 40506 USA

2:30 PM VII.B-2
Ultrathin High-K Gate Dielectric Technology for Germanium MOS Applications: *C. O. Chui*[1]; S. Ramanathan[2]; B. B. Triplett[2]; P. C. McIntyre[2]; K. C. Saraswat[1]; [1]Stanford University, Dept. of Electl. Eng., Stanford, CA 94305 USA; [2]Stanford University, Dept. of Matls. Sci. & Eng., Stanford, CA 94305 USA

2:50 PM VII.B-3
High Quality MOSFETs Fabrication with HfO_2 Gate Dielectric and TaN Gate Electrode: *R. Choi*[1]; K. Onishi[1]; C. S. Kang[1]; R. Nieh[1]; S. Gopalan[1]; H.-J. Cho[1]; S. Krishnan[1]; J. C. Lee[1]; [1]The University of Texas at Austin, Microelect. Rsrch. Ctr., R9950, Dept. of Electl. & Computer Eng., Austin, TX 78758 USA

3:10 PM Break

3:30 PM VII.B-4
Impact of NH_3 Pre-Treatment on the Electrical and Reliability Characteristics of Ultra Thin Hafnium Silicate Films Prepared by Re-Oxidation Method: *S. Gopalan*[1]; R. Choi[1]; K. Onishi[1]; R. Nieh[1]; C. S. Kang[1]; H-J Cho[1]; S. Krishnan[1]; J. C. Lee[1]; [1]University of Texas at Austin, Microelect. Rsrch. Ctr., MC R9950, Austin, TX 78758 USA

3:50 PM VII.B-5
A Comparative Study of RF Noise Characteristics of Different Submicron SOI MOSFET Structures on SIMOX Technology: *S. Lam*[1]; H. Wang[1]; W.-K. Lee[1]; P. K. Ko[1]; M. Chan[1]; [1]Hong Kong University of Science & Technology, Dept. of Electl. & Elect. Eng., Hong Kong

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