2001 EMC At-A-Glance
Wednesday Morning, June 27, 2001

8:20 AM EMC PLENARY LECTURE/STUDENT AWARDS

Room: Washington Hall

Plenary Speaker: Nick Holonyak, Jr.,
University of Illinois at Urbana–Champaign, Electrical Engineering Research Laboratory
& Center for Compound Semiconductor Microelectronics, Urbana, IL 61801 USA

Topic: "From the Transistor to the Light Emitting Diode and Laser"

Break: 9:20 AM–10:00 AM

Session A: Epitaxy for Devices

10:00 AM A1 (Student), AlInAs/GaAs$_{0.51}$Sb$_{0.49}$ /GaInAs Heterojunction Bipolar Transistors Grown by Solid Source Molecular Beam Epitaxy
..... *Changhyun Yi*

10:20 AM A2 (Student), Characterization of GaAsSb 1.3µm QW Heterostructures Grown by Metalorganic Chemical Vapor Deposition
..... *Min-Soo Noh*

10:40 AM A3 (Student), Growth and Properties of Lattice-Matched and Mis-Matched InGaAs Tunnel Junctions for Mid-Infrared Devices Grown on Graded InAlAs/InP Substrates
..... *Ojin Kwon*

11:00 AM A4 (Student), Growth and Characterization of Low-Oxygen Content AlAs/AlGaAs DBRs and InAlP Cladding Layers
..... *Richard Dean Heller*

11:20 AM A5 (Student), Monolithic Integration of a Heat Pump and a Laser Diode in a Single Epitaxial Growth
..... *Jizhi Zhang*

Session B: Joint EMC & DRC Session on Modeling of Materials and Nanostructures

10:00 AM B1, Spin-Orbit Interaction of 2° in InAlAs/InAs Hetero-structures
..... *Kanji Yoh*

10:20 AM B2 (Student), Thermal Conductivity in Semiconductor Thin Films and Nanowires
..... *Jie Zou*

10:40 AM B3 (Student), Quantum Mechanical Calculation of QCA Molecur Properties
..... *Christopher J. Russo*

11:00 AM B4, Nano-Transistor Modeling: Two Dimensional Green's Function Method
..... *A. Svizhenko*

11:20 AM B5, A Couple Schrödinger/Monte Carlo Technique for Quantum-Corrected Device Simulation
..... *Brian Winstead*

11:40 AM B6, Quantitative Prediction of Threshold Voltage Fluctuations in Sub-100 nm MOSFETs by a New Dopant Model
..... *Hiroyuki Yamamoto*

Session C: Contacts to Wide Bandgap Semiconductors - I

10:00 AM C1 (Student), Impact of Material Defects on SiC Schottky Barrier Diodes
..... *Dallas T. Morisette*

10:20 AM C2 (Student), Chemically-Dependent Traps and Polytypes at Pt/Ti Contacts to 4H and 6H-SiC
..... *Sergey P. Tumakha*

10:40 AM C3, Influence of Semiconductor Surface Properties on the Ohmic Contact Characteristics for p-Type Silicon Carbide
..... *T. Worren*

11:00 AM **C4 (Student), Ohmic Contact Formation on Inductively Coupled Plasma (ICP) Etched 4H-Silicon Carbide Using Sputtered Titanium Tungsten**
..... *Sang-Kwon Lee*

11:20 AM C5, Reliability of Ti/TaSi$_2$/Pt Ohmic Contacts on 4H- and 6H-SiC After 1000 Hours in Air at 600°
..... *Robert S. Okojie*

11:40 AM C6 (Student), The Role of Titanium in Ti/Al Contacts to p-Type 4H-SiC
..... *Brian J. Johnson*

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Session D: Materials Integration: Mismatched Epitaxy

10:00 AM D1 (Student), Development of Cross-Hatch Morphology in Lattice Mis-matched Layers
Aaron Maxwell Andrews

10:20 AM D2, Lattice-Mismatched Heteroepitaxy of GaInAs on InP
S. P. Ahrenkiel

10:40 AM D3, Island and Pit Nucleation in InGaAs/GaAs Films
Joanna Mirecki Millunchick

11:00 AM D4 (Student), Engineered SiGe/Si Substrates for Coplanar Integra tion of III-V Semiconductors and Strained Si Electronics with Silicon
Arthur J. Pitera

11:20 AM D5 (Student), Visible LED Materials Based on Relaxed, Graded InGaP: Engineering High Performance in the Presence of Defects
Lisa M. McGill

11:40 AM D6, Lattice-Mismatched GaInP/ GaInAs Devices on Ge Substrates: Bulk Lifetime, Interface Recombination, Sublattice Disorder, and Photovoltaic Efficiency
Richard R. King

Session E: Nanoscale Characterization

10:00 AM E1 (Student), Cross-Sectional Scanning Tunneling Microscopy Studies of Phase Separation in InAlAs Alloys
B. Shin

10:20 AM E2 (Student), Atomic Force Microscope I-V Measurements of Polycarbonate Membrane Template-Synthesized Nanowires
Lili Jia

10:40 AM E3 (Student), Potential Imaging of Pentacene Organic Thin Film Transistors
Jonathan A. Nichols

11:00 AM E4 (Student), Effect of Cantilever on Electrostatic Potentials Measured by Scanning Kelvin Probe Micros copy
Hemant R. Bhangale

11:20 AM E5 (Student), Experimental and Modeling Studies of Schottky Contacts to Low-Temperature-Grown GaAs in Ex-Situ Structures
Saurabh Lodha

11:40 AM E6 (Student), Properties of Surface States on Clean and Si-Deposited GaAs(001)-c(4x4) Surfaces Studied by Scanning Tunneling Microscopy and Spectroscopy
Noboru Negoro

Session F: Advanced Gate Dielectrics – I

10:00 AM F1 Invited, Functionality of Epitaxial Ferroelectric Heterostructures and Possibilities for Integration with Silicon
Charles Ahn

10:40 AM F2 (Student), In-Plane Anisotropic Dielectric Properties of Epitaxial Barium Titanate Thin Films
Brent H. Hoerman

11:00 AM F3 (Student), Studies of Liquid Source Misted Chemical Deposited Strontium Tantalate ($SrTa_2O_6$) as MOS Gate Oxide
Dong-Oh Lee

11:20 AM F4 (Student), Platinum and Iridium High Temperature Etching Character istics
Stefan Schneider

11:40 AM F5 (Student), The Thickness Dependent Gate Oxide Integrity Degradation by Cu Contamination
Yih Hsia Lin

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Session G: IR Quantum Devices and Materials

1:20 PM **G1, Long Wavelength Infrared Negative Luminescence from MCT Diodes**
..... *Tim Ashley*

1:40 PM **G2 (Student), GaInSb Quantum Well Lasers Grown on AlInSb Metamorphic Buffer Layers**
..... *Edwin Pease*

2:00 PM **G3, Linewidth of Terahertz Intersubband Plasmons in Quantum Wells**
..... *Carsten A. Ullrich*

2:20 PM **G4 (Student), InAs Quantum Dot Lasers Grown on AlGaAsSb Metamorphic Buffers on GaAs Substrate**
..... *Y.-C. Xin*

2:40 PM **G5, Normal Incidence InAs/ InAlGaAs Quantum Dot Infrared Photodetectors with Undoped Active Region**
..... *Zhonghui Chen*

3:00 PM **Break**

3:20 PM **G6 (Student), Tuning InAs/ InAlGaAs Quantum Dot Structures for Infrared Photodetectors**
..... *Eui-Tae Kim*

3:40 PM **G7, Near 1.5 µm Infrared Detectors Based on Ge Quantum Dots on Si Substrate**
..... *Song Tong*

4:00 PM **G8 (Student), Stable Growth of AlInAsSb Quaternaries Using a Digital Alloy Technique**
..... *Leslie G. Vaughn*

4:20 PM **G9, Thermal and Optical Characteristics of MBE Grown InAs/AlSb Superlattices**
..... Dapeng Xu

4:40 PM, **G10, Late News**

Session H: Special Topical Session on Bioelectronic Materials and Biological/Electronic Interfaces

1:20 PM **H1 Invited, Nanoscale Optoelectronic Photosynthetic Devices**
..... *Elias Greenbaum*

2:00 PM **H2 Invited, Protein-Based 3D Memories and Associative Processors**
..... *J. A. Stuart*

2:40 PM **H3, Enzyme Electrode Based on Nano-Patterned Alumina**
..... *Juan Jiang*

3:00 PM **Break**

3:20 PM **H4 Invited, Semiconductor Nanocrystal Quantum Dots: From Scaling Laws to Biological Applications**
..... *A. Paul Alivisatos*

4:00 PM **H5 Invited, Constructed Networks of Dissociated Rat Hippocampal Neurons Cultured on Microelectrode Arrays**
..... *Conrad D. James*

4:40 PM **H6 Invited, Chemical Sensors Based on Modulation of Work Function**
..... *J. Janata*

Session I: Growth and Properties of Quantum Wires

1:20 PM **I1 Invited, Epitaxial Growth and Transport Properties of Step Quantum Wires and Planar Superlattice Structures**
..... *H. Sakaki*

2:00 PM **I2, Ultrahigh Quality AlGaAs/GaAs Quantum Wires Grown by Flow Rate Modulation Epitaxy Using Tertiarybutylarsine**
..... *Xue-Lun Wang*

2:20 PM **I3, Exciton Scattering by Auger Processes in a Single Quantum Wire**
..... *Valia Voliotis*

2:40 PM **I4, Magnetic and Structural Properties of Electrochemically Self-Assembled Fe/Co Quantum Wires**
..... *Latika Menon*

3:00 PM **Break**

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Session J: Self-Assembled Nanostructures

3:20 PM **J1 (Student), Structural Investigation of Wurtzite GaN Nanowires Fabricated Via Direct Reaction of Ga and Ammonia**
..... Randolph N. Jacobs

3:40 PM **J2 (Student), Template Directed Vapor-Liquid-Solid Growth of Silicon Nanowires**
..... Kok-Keong Lew

4:00 PM **J3, Nucleation and Heteroepitaxy Processes in Self-Assembly of Si Nanostructures**
..... Elena A. Guliants

4:20 PM **J4, Synchronized Pinning Due to Commensurability Between the Vortex Lattice in a Niobium Film and an Underlying Self-Assembled Periodic Magnetic Quantum Dot Array**
..... Latika Menon

4:40 PM **J5, Cl2/Ar/H2-Inductively-Coupled-Plasma-Reactive Ion Etching of InP/InGaAsP Nanostructures**
..... Sean L. Rommel

Session K: Contacts to Wide Bandgap Semiconductors – II

1:20 PM **K1, Correlation Between I-V Characteristics and Dislocations for Au/Ni/n-GaN Schottky Contacts**
..... Kenji Shiojima

1:40 PM **K2, Characterization of Metal/p-GaN Schottky Interfaces by I-V-T Measurements**
..... Takayuki Sawada

2:00 PM **K3 (Student), Thermal and Environmental Aging of the Au/Ni/p-GaN Ohmic Contact Annealed in Air**
..... Sammy H. Wang

2:20 PM **K4 (Student), Low Resistance Pd/Ru Ohmic Contacts to p-GaN**
..... Ja-Soon Jang

2:40 PM **K5 (Student), $TiAl_3$-Based Contacts to n-GaN**
..... Christopher M. Pelto

3:00 PM Break

3:20 PM **K6 (Student), Characterization of Schottky Contacts on n-Type AlxGa1-xN**
..... L. Zhou

3:40 PM **K7, Ohmic Contacts to AlGaN with High Al Content**
..... Suzanne E. Mohney

4:00 PM **K8 (Student), Microstructural Analysis of Ti/Al/Ti/Au Ohmic Contacts to n-AlGaN/GaN**
..... Jiang Chen

4:20 PM, K9, Late News

4:40 PM, K10, Late News

Session L: III-N Growth

1:20 PM **L1 (Student), Growth of InN by Molecular Beam Epitaxy**
..... Hai Lu

1:40 PM **L2 (Student), Properties of High-Quality AlGaN/GaN Superlattices Grown by Metalorganic Chemical Vapor Deposition**
..... Uttiya Chowdhury

2:00 PM **L3 (Student), Growth and Characterization of AlN/GaN Heterostructures Using Low-Pressure Organometallic Vapor Phase Epitaxy**
..... Seth Martin Hubbard

2:20 PM **L4, Growth and Characterization of Epitaxial AlGaN/GaN on Single-Crystal Aluminum Nitride Substrates**
..... Leo J. Schowalter

2:40 PM **L5, Enhanced Ultraviolet Light Emission From Quaternary AlInGaN Grown by Atomic Layer Epitaxy**
..... Jianping Zhang

3:00 PM **Break**

3:20 PM **L6, Cantilever Epitaxy and its Potential for GaN Substrates with Whole-Wafer Dislocation Densities Below 10^7/cm^2**
..... Carol I. H. Ashby

3:40 PM **L7, Crystallographic Tilting in Pulsed Metalorganic Chemical Vapor Deposited GaN**
..... Qhalid Fareed

4:00 PM **L8 (Student), Epitaxial Lateral Overgrowth of GaN Layer on Si(111) Substrate**
..... Jeong Wook Lee

4:20 PM **L9, Al1-xSixN Ternary Alloy Epitaxial Growth and its Spontaneous Ridge Formation**
..... Makoto Kasu

4:40 PM **L10, Growth and Characterization of InGaN/GaN Multi-Quantum Wells Selectively Grown on Hexagonal GaN Microstructures**
..... Chang-Hee Hong

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Session M: Advanced Gate Dielectrics – II

Wednesday Afternoon, Cont.

1:20 PM M1 Invited, Si-Compatible Gate Dielectrics with High K, High Optical Bandgap, and Their Epitaxy on Silicon
..... Darrell G. Schlom

2:00 PM M2 (Student), Measurement of the Optical Bandgap of High K Candidate Materials for MOSFETs by Far UV Ellipsometry
..... Seung-Gu Lim

2:20 PM M3, Atomic Scale Chemistry and Structure of Alternative Gate Oxides
..... Susanne Stemmer

2:40 PM M4 (Student), Electrical and Structural Characteristics of Zirconium Oxynitride Prepared by Nitrida tion of Zirconium Oxide
..... Sanghun Jeon

3:00 PM Break

3:20 PM M5 Invited, Materials Research for Alternate Gate Dielectrics: Challenges and Achievements
..... J. Raynien Kwo

4:00 PM M6, Dependence of Thermal Stability of $ZrO_2/SiO_2/Si$ Layered Structure on Ambient Oxygen
..... Heiji Watanabe

4:20 PM M7 (Student), Electrical Properties of HfO2 Gate Dielectric on SiGe
..... Tat Ngai

4:40 PM M8 (Student), Investigation of Aluminum Oxynitride as Replacement Dielectric for SiC Devices
..... William Leroy Rose

Session N: Mixed III-V-N and Novel IR Materials

8:20 AM N1 (Student), Nitrogen Incorporation in GaInNAs for Long Wavelength Opto-Electronic Devices
..... Vincent Gambin

8:40 AM N2 (Student), Local Ordering in Vibrational Spectra of InGaAsN Alloys
..... Alexander M. Mintairov

9:00 AM N3 (Student), Deep Levels and Their Impact on Current Generation in MOCVD-Grown GaAs/InGaAsN Heterostructure Devices
..... Robert J. Kaplar

9:20 AM N4 (Student), Distribution of Nitrogen Atoms in GaAsN and InGaAsN Alloys Determined by Scanning Tunneling Microscopy
..... H. A. McKay

9:40 AM N5 (Student), Novel Interface Properties of Metastable (GaIn)(NAs)/(GaAs)-Heterostructures
..... Siegfried Nau

10:00 AM Break

10:20 AM N6, Infrared Absorption of Thermally Annealed GaInNAs
..... Takeshi Kitatani

10:40 AM N7, GaInTlAs Layers Grown on InP by Low Temperature Molecular Beam Epitaxy: Structural and Optical Properties ..
..... Guy R. Hollinger

11:00 AM N8, Theoretical Study of the Effects of Isovalent Co-Alloying of Bi and N in GaAs
..... Su-Huai Wei

11:20 AM N9 (Student), A Dislocation-Free and Lattice-Matched $Si/GaP_{0.971}N_{0.029}/Si$ Structure
..... Kenji Momose

11:40 AM N10 (Student), A Dislocation-Free $GaAs_yP_{1-x-y}N_x/GaP_{0.98}N_{0.02}$ Quantum Well Structure Lattice-Matched to Si Substrate
..... Yasuhiro Fujimoto

Session O: Molecular and Organic Electronics

8:20 AM O1 (Student), Electrostatic Surface Potential of Conjugated Molecules on Au(111) Using Electrostatic Force Microscopy
..... Stephen W. Howell

8:40 AM O2, Progress Towards Molecular Quantum-Dot Cellular Automata
..... Marya Lieberman

9:00 AM O3 (Student), Can Organic Molecules Be Ohmic? Modifying Conductance of Molecular Nanostructures By Doping
..... Andre P. Labonte

9:20 AM 04 (Student), Growth Characteristics of Carbon Nanotubes Grown Using Carbon Monoxide by Plasma Enhanced Chemical Vapor Deposition
..... Jae-hee Han

9:40 AM O5, Study on Emission Property of Field Emission Display with the Density of Carbon Nanotube
..... Ha Jin Kim

10:00 AM Break

10:20 AM 06 (Student), Napthacene Organic Thin Film Transistors
..... David J. Gundlach

10:40 AM O7, Orientation of Pentacene Films Using Surface Alignment Layers and its Influence on Thin Film Transistor Characteristics
..... Michele Swiggers

11:00 AM O8, Polymer Encapsulation of Screen Printed Organic Thin Film Transistors
..... Jianna Wang

11:20 AM O9 (Student), Organic Thin Film Transistors with Improved Linear Region Performance Using Chemically-Modified Source and Drain Contacts
..... David J. Gundlach

11:40 AM, O10, Late News

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Session P: Quantum Dot Device Structures

8:20 AM **P1 (Student), Electric Field Dependent Spectroscopy of Quantum Dot Molecules**
..... B. D. Gerardot

8:40 AM **P2 (Student), Resonant Tunneling with High Peak-to-Valley Ratios Observed in InAs/InP Quantum Dot Stacks**
..... Magnus Lars Borgstrom

9:00 AM **P3, Enhanced Intraband Stark Effects in Stacked InAs/GaAs Self-Assembled**
..... Weidong Sheng

9:20 AM **P4 (Student), Charging Kinetics and Charging Saturation Mechanisms of 2D Array Si Nanocrystals Embedded in a MOS Structure**
..... Christophe Busseret

9:40 AM **P5, Red Light Emitting InP/GaInP Quantum Dot Lasers: How the Mechanism of Operation Influences Their Performance**
..... Thomas Riedl

Session Q: Materials Integration: Wafer Bonding and Alternate Substrates

8:20 AM **Q1 (Student), Dislocation Dynamics of SiGe Film Relaxation on Silicon on Insulator Substrates**
..... Eric M. Rehder

8:40 AM **Q2 (Student), Modeling of In-Plane Expansion and Buckling of SiGe Islands on BPSG**
..... Haizhou Yin

9:00 AM **Q3 (Student), High Quality Heteroepitaxial InGaAs Layers Grown on Strain Relaxed Seed Membranes Using the 'Paramorphic' Approach**
..... Mouloud Boudaa

9:20 AM **Q4, Silicon on Sapphire Substrates Formed by Wafer Bonding**
..... P. D. Moran

9:40 AM **Q5 (Student), GaAs/GaN Diodes Wafer-Fused at 500°C**
..... Sarah Marie E. Monteith

10:00 AM **Break**

10:20 AM **Q6 (Student), GaN MSM Photodetectors on Lithium Gallate: Demonstration of Performance and Integration Onto Si**
..... Sa Huang

10:40 AM **Q7, The Integration of Continuous-Wave InGaN Multiple-Quantum-Well Laser Diodes with Copper and Diamond Substrates by Laser Lift-Off**
..... William S. Wong

11:00 AM **Q8, Formation of Hybrid SiC/Si and SiC/SiO2/Si Wafers by Oxygen Implantation, Wafer Bonding and Etching**
..... J. T. Torvik

11:20 AM **Q9, Wafer Bonding Fabrication of High Voltage Power Electronic Devices**
..... K. D. Hobart

11:40 AM **Q10, Electrical and Optical Characterization of Wafer-Bonded 4H/6H-SiC and SiC/Si N-p Heterojunction Diodes**
..... John T. Torvik

Session R: Doping and Defects in Group III-Nitrides and ZnO

8:20 AM **R1, Sub-Micron Scale Photoluminescence Images of Epitaxially Laterally Overgrown GaN at a Low Temperature**
..... Masahiro Yoshimoto

8:40 AM **R2, Dislocation Electrical Activity in GaN Films Grown By Molecular Beam Epitaxy**
..... Julia W. P. Hsu

9:00 AM **R3, Phosphoric Acid Decoration Etch of Defects in HVPE and MOVPE GaN**
..... X. Xu

9:20 AM **R4, Deep Centers With Anomalous Capture Behavior in Free-Standing GaN**
..... Zhaoqiang Fang

9:40 AM **R5, Polarity Dependence of Nitrogen-Doping into ZnO Layers Grown on GaN Templates by Plasma-Assisted Molecular Beam Epitaxy**
..... Hang-Ju Ko

10:00 AM **Break**

10:20 AM **R6, Controlled n-Type Doping Using Oxygen in GaN Grown by rf PlasmaMolecular Beam Epitaxy**
..... Gerald Lucovsky

10:40 AM **R7 (Student), Optical Memory Effects and Yellow Luminescence in GaN**
..... Y. C. Chang

11:00 AM **R8 (Student), Point Defect Distributions and Interdiffusion at AlGaN/GaN HEMT Structures**
..... Shawn T. Bradley

11:20 AM, R9, Late News

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Session S: Si-Based Heterojunction Growth and Characterization

Thursday Morning, Cont.

8:20 AM **S1 (Student), Investigating Hole Mobility Enhancements in Surface Strained Si/SiGe Heterostructures**
..... Christopher W. Leitz

8:40 AM **S2, Growth and Stabilization of Sub 100-nm Vertical n-Channel MOSFET's**
..... David C. Paine

9:00 AM **S3 (Student), Improvement of SiO2/SiGe Interface of SiGe pMOSFETs Using Water Vapor Annealing**
..... Tat Ngai

9:20 AM **S4 (Student), Monte Carlo Modeling of Ion Implantation into SiGe**
..... Gaurav Shrivastav

9:40 AM **S5, Growth of $Ca_xCd_{1-x}F_2$ Alloy on Si Substrates Using Very Thin CaF_2 Buffer Layer**
..... Kazuo Tsutsui

10:00 AM **Break**

10:20 AM **S6 (Student), Annealing Effect on Properties of $Si_{0.2}Ge_{0.8}/Si_{0.7}Ge_{0.3}$/ Si(001) p-Type Modulation Doped Heterostructures Studied by Magnetotransport Measurements and Raman Spectroscopy**
..... Maksym Myronov

10:40 AM **S7, Diffusion of Ion Implanted N-Type Dopants in Silicon Germanium Alloys**
..... Satoshi Eguchi

Session T: Spin-Dependent (or Spintronic) Electronic Materials

1:20 PM **T1 (Student), Characterization and Spin Transport Across the Fe_xCo_{1-x} / GaAs(100) Interface**
..... Brian D. Schultz

1:40 PM **T2, Spin-Polarized Transport in Mn-Containing Dilute Magnetic III-V Semiconductors**
..... Leeor Kronik

2:00 PM **T3 (Student), Growth of the Dilute Magnetic Semiconductor (Ga,Mn)P by Gas Source MBE**
..... M. E. Overberg

2:20 PM **T4, Spontaneous Anisotropic Magnetoresistance in GaMnAs**
..... David V. Baxter

2:40 PM **T5, Molecular Beam Epitaxy Growth of Heusler Alloy Ni_2MnGe Thin Films on GaAs(001)**
..... J. Lu

3:00 PM **Break**

3:20 PM **T6 (Student), MBE Growth of Ferromagnetic Ni_2MnIn Thin Films on InAs (001)**
..... J. Q. Xie

3:40 PM **T7, Influence of Material and Device Parameters on Spin Effects in Quantum Dots**
..... Philippe Matagne

4:00 PM **T8 (Student), The Effect of Mn Ions on the Formation of CdSe Self-Assembled Quantum Dots**
..... Luba Titova

4:20 PM **T9, Electron Spin Dynamics in III-V Quantum Wells**
..... Wayne H. Lau

4:40 PM, **T10, Late News**

Session U: Growth and Properties of Quantum Dot Structures

1:20 PM **U1, Growth of InAs and InAsSb Quantum Dots by Metal-Organic Chemical Vapor Deposition**
..... J. G. Cederberg

1:40 PM **U2 (Student), InP Self-Assembled Quantum Dots Embedded in In0.49(AlxGa1-x)0.51P Grown by Metalorganic Chemical Vapor Deposition**
..... Jae-Hyun Ryou

2:00 PM **U3, Matrix Effect on the Stacking Behavior of InAs Nanostructures Grown on InP (001) Substrates**
..... Hanxuan Li

2:20 PM **U4 (Student), Fermi-Level Effect on the Interdiffusion of InAs and InGaAs Quantum Dots**
..... Oleg B. Shchekin

2:40 PM **U5, Self-Ordered Structures and Compositional Modulations on the Atomic Scale in (Cd,Zn,Mn)Se and In(Sb,As) Quantum Dot Structures**
..... Peter Moeck

3:00 PM Break

3:20 PM **U6, Spontaneous Emission Modification in Single InAs Quantum Dots Using a Three-Dimensional Cavity**
..... G. S. Solomon

3:40 PM **U7, Pyramidal Three-Dimensional Optical Microcavities with High Resonance Q Values in Short-Wavelength Region**
..... Ikuo Suemune

4:00 PM **U8 (Student), Lateral Conductivity and Large Negative Magnetoresistance in Self-Organized Quantum Dots**
..... Boaz Kochman

4:20 PM **U9, Phonon Emission by Individual InAs/GaAs Quantum Dots**
..... Andrei Yu Silov

4:40 PM **U10 (Student), Temperature Dependence of Carrier Relaxation and Dynamics in InAs QDs: Experimental and Model**
..... Chuanshun Cao

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Session V: SiC Growth and Characterization

1:20 PM **V1, High Quality Step-Flow Growth of Homoepitaxial 6H-SiC**
..... William V. Lampert

1:40 PM **V2, Lateral Growth of Thin Cantilevers from Atomically Flat 4H- and 6H-SiC Mesa Surfaces**
..... Philip G. Neudeck

2:00 PM **V3 (Student), In-Situ Etching of SiC Prior to Epitaxial Growth Using H2/O2 Gas Mixtures**
..... Ishwara Bhat

2:20 PM **V4, Al Doping (>1e20 cm-3) of SiC by Liquid Phase Epitaxy and Resulted Ohmic Contacts**
..... Alexander L. Syrkin

2:40 PM **V5 (Student), Growth and Doping of SiC Thin Films on Low-Stress, Amorphous Si_3N_4/Si Substrate for Robust MEMS Applications**
..... Lin Cheng

3:00 PM **Break**

3:20 PM **V6 (Student), Nucleation of Threading Dislocations in Sublimation Grown SiC**
..... M. Skowronski

3:40 PM **V7 (Student), Evidence of Basal Plane Slip During Sublimation Growth of Silicon Carbide**
..... Seoyong Ha

4:00 PM **V8, EPR Study of the Interaction Between Intrinsic Defects and N/B Impurities in Semi-Insulating SiC**
..... Valery V. Konovalov

4:20 PM **V9 (Student), Observations of Deep Levels in 4H-SiC Using Optoelectronic Modulation Spectroscopy**
..... Chi-Hsin Chiu

4:40 PM, **V10, Late News**

Session W: Non-Destructive Testing and In-Situ Monitoring and Control

1:20 PM **W1 (Student), Emissivity and Sample Temperature Variations During Growth on Silicon on Insulator Substrates**
..... Eric M. Rehder

1:40 PM **W2 (Student), Monitoring of Ultra-Thin Oxide Processing Using Non-Contact Surface Photovoltage Method**
..... J. Wang

2:00 PM **W3, Angle Dependent Surface Photovoltage Spectroscopy Study of GaAs/GaAlAs Vertical Cavity Surface Emitting Laser Structures**
..... Y. S. Huang

2:20 PM **W4, Characterization of Subsurface Damage in Nano-Patterned GaAs Using Micro-Raman**
..... Kurt G. Eyink

2:40 PM **W5 (Student), Contactless Characterization of Multi-Epitaxial Wafer by Depth-Resolved Cathodelumine-scence**
..... Fumitaro Ishikawa

3:00 PM Break

3:20 PM **W6, Chemical Imaging of an InGaN Multi-Quantum Well Structure on Fully Coalesced Lateral Epitaxial Overgrown GaN**
..... Thomas H. Myers

3:40 PM **W7 (Student), Optical Characterization of InGaN/GaN Multiple Quantum Wells with Si-Doped Barriers**
..... Mee-Yi Ryu

4:00 PM **W8, Precise AlGaN Layer Thickness Determination of GaN/AlGaN HEMT Structures by X-ray Diffraction**
..... Abbas Torabi

4:20 PM, **W9, Late News**

4:40 PM, **W10, Late News**

Session X: III-V Nitride Processing and Devices

1:20 PM **X1 (Student), A Comparison of Sidewall Recombination in Photoelectrochemical and Dry Etched InGaN/GaN Quantum Well Probes**
..... E. D. Haberer

1:40 PM **X2, Plasma Damage in GaN Schottky Structures-Effect of PARIE**
..... Zoulikha Mouffak

2:00 PM **X3, Surface Passivation of GaN/AlGaN Heterostructure Using ECR-CVD SiNx Film and Ultrathin Al_2O_3 Layer**
..... Tamotsu Hashizume

2:20 PM **X4, Effects of High Density Plasma Etching on Contacts to GaN and $Al_xGa_{1-x}N$**
..... Rajwinder Singh

2:40 PM **X5 (Student), Effect of a MBE Grown AlN Surface Layer on the DC and RF**
..... Jeonghyun Hwang

3:00 PM **Break**

3:20 PM **X6, Fabrication and DC Characteristics of Various Al-Content MOCVD Grown AlGaN/GaN HEMTs on Sapphire Substrate**
..... S. Arulkumaran

3:40 PM **X7 (Student), GaN and AlGaN High-Voltage Rectifiers Grown by Metalorganic Chemical Vapor Deposition**
..... Ting Gang Zhu

4:00 PM **X8, Responsivity Spectra of GaN Based Schottky Barrier UV Detectors Using Synchrotron Radiation**
..... Atsushi Motogaito

4:20 PM **X9, Device Characteristics of a Pt-Ga2O3(Gd2O3)-GaN Capacitor**
..... T. S. Lay

4:40 PM, **X10, Late News**

2001 EMC At-A-Glance

Friday Morning June 29, 2001

Session Y: Heteroepitaxy on Si

8:20 AM **Y1, Growth of InP and InP-based InGaAsP Heterostructures on Silicon Substrates by Solid-Source Molecular Beam Epitaxy**
..... Clifton G. Fonstad

8:40 AM **Y2, Molecular Beam Epitaxy of CaF_2 on Si(111)**
..... Karl R. Hofmann

9:00 AM **Y3 (Student), Epitaxial Growth of BeZnSe on CaF_2/Si(111) Substrate**
..... Takeo Maruyama

9:20 AM **Y4, Selective Growth of CdF2/ CaF2 Resonant Tunneling Diode Nanostructure on Si**
..... Masahiro Watanabe

9:40 AM, **Y5, Late News**

10:00 AM **Break**

Session Z: Erbium Doping and Ordering

10:20 AM **Z1, Erbium Doping in GaP and GaNP Grown by MOMBE**
..... Ikuo Suemune

10:40 AM **Z2 (Student), Optimum Er Concentration for In-Situ Doped GaN Visible and IR Luminescence**
..... Dong-Seon Lee

11:00 AM **Z3 (Student), Flat Panel Display Material Issues and Options for Rare Earth-Doped GaN Electroluminescent Phosphors**
..... Jason C. Heikenfeld

11:20 AM **Z4 (Student), Sinusoidally-Modulated III-V Semiconductor Superlattices by Molecular Beam Epitaxy**
..... Xinyu Liu

11:40 AM **Z5, Anomalous Properties of Triple-Period-A (TP-A) Type Ordering in GaInP with Sb Added During Growth**
..... Tohru Suzuki

Session AA: Nanoscale Fabrication and Self-Assembled Systems

8:20 AM **AA1, Room Temperature Infra-Red Absorption in Electrochemically Self-Assembled 3.5 nm CdS Quantum Dots**
..... Supriyo Bandyopadhyay

8:40 AM **AA2, Electrochemical Self-Organization of Nanopores on Anodized Aluminum Oxide**
..... Sunil K. Thamida

9:00 AM **AA3, Template Based Electrochemical Fabrication of Nanstructured Materials and Their Applications**
..... Michael Crouse

9:20 AM **AA4 (Student), Gas-Phase Generated Nanocrystals with Self-Adjusted Sub-µm Film Feature Size**
..... Frank Otten

9:40 AM **AA5, Self-Assembled ZnO Nanostructures Within a Diblock Copolymer Matrix on Si and SiO2 Surfaces**
..... Agis A. Iliadis

10:00 AM **Break**

10:20 AM **AA6, Room Temperature Coulomb Diamond Characteristic of Single Electron Transistor**
..... Y. Gotoh

10:40 AM **AA7 (Student), Single Crystalline Si Formed on Amorphous Substrate at Low Temperature by NanoPatterning and Nickel Induced Lateral Crystallization**
..... Jian Gu

11:00 AM **AA8, Temperature-Dependent Ordering Process of Self-Assembled Ge Islands in the Multi-Layer Structures**
..... Yasuhiro Shiraki

11:20 AM **AA9 (Student), Fabrication of Germanium Dots on Different Dielectric Substrates**
..... Dong-Won Kim

11:40 AM **AA10 (Student), The Influence of a Buried Misfit Dislocation Network on the Pyramid-to-Dome Transition Size in Ge Self-Assembled Quantum Dots on Si(001)**
..... Hyung-Jun Kim

2001 EMC At-A-Glance

Friday Morning June 29, 2001

Session BB: SiC Processing and Characterization

8:20 AM **BB1 (Student), Comparative Hall Measurements on "Wet and Dry" Oxidized 4H-SiC MOSFETs**
..... *Kiran Chatty*

8:40 AM **BB2 (Student), Low Damage Etching of Silicon Carbide Using Cl2 Based Plasmas**
..... *Farid Ahmed Khan*

9:00 AM **BB3 (Student), Mesa Isolation with Good Edge Acuity by Electron Cyclotron Resonance Plasma Etching of SiC Using Cl_2, CH_4, Ar_2, and a Resist Mask**
..... *C. I. Thomas*

9:20 AM **BB4 (Student), Optimization of Carbon-Face SiC Metal Oxide Semiconductor Structures Using Low Temperature Oxidation and Post Oxidation Annealing**
..... Chun Wang

9:40 AM **BB5, Defect Density at the SiC/ SiO2 Interface During HighTemperature Gas Exposure**
..... *Peter Tobias*

10:00 AM **Break**

10:20 AM **BB6 (Student), Characterization and Modeling of Low-Voltage 4H-SiC Schottky and PN Diodes**
..... *Malay Trivedi*

10:40 AM **BB7, Spectroscopy of Light Emission Due to Electron-Hole Recombination in 4H and 6H SiC MOSFETs** .
..... *P. J. Macfarlane*

11:00 AM **BB8, The Effects of Defects on SiC PIN Diode Operation Examined by Light Emission**
..... *R. E. Stahlbush*

11:20 AM **BB9, Bipolar Silicon Carbide Power Diodes Realized by Aluminum Implantations and High Temperature rf-Annealing**
..... *M. Lazar*

11:40 AM **BB10, Low-Dose Boron and Aluminum P-Type Implants in 4H- and 6H-SiC**
..... *Nelson Saks*

Session CC: Characterization of Wide Bandgap Semiconductors

8:20 AM **CC1, UV Optical Gain in GaN Layers and GaN/InGaN Multiple Quantum Wells**
..... *Edmundas Kuokstis*

8:40 AM **CC2, Large Field Emission from Heavily Si-Doped AlN and AlxGa1-xN (0.4<x<1)**
..... *Makoto Kasu*

9:00 AM **CC3, Recombination Mechanisms in AlGaN and Their Effects on the Response of Ultraviolet Detectors**
..... *Jean-Luc Reverchon*

9:20 AM **CC4 (Student), Characterization of Nitrides by Scanning Kelvin Probe Microscopy**
..... *Goutam Koley*

9:40 AM, **Late News**

10:00 AM **Break**

10:20 AM **CC6, Valence-Band Discontinuities in p-InGaN/n-GaN Heterojunction Diodes**
..... *Toshiki Makimoto*

10:40 AM **CC7, Measurement of Carrier Transport in GaN Using GaN Homojunction and AlGaN/GaN Heterojunction p-i-n Diodes**
..... *M. Wraback*

11:00 AM **CC8 (Student), Nonlinear Piezoelectricity in InGaN/GaN Quantum Wells with Si Doped Barriers**
..... *G. O. Vaschenko*

11:20 AM **CC9 (Student), Advancement in the Electrical Characteristics of AlGaN/ GaN Heterostructures Grown by MBE on LiGaO2 Substrates**
..... *Sangbeom Kang*

11:40 AM **CC10, Transport and Low Frequency Noise Properties of Thin Highly Doped GaN Layers**
..... *Remis Gaska*

Session DD: Semiconductors: Processing and Oxidation

8:20 AM **DD1 (Student), Lateral Oxidation of $AlAs_xSb_{1-x}$ Compounds**
..... *Aaron Maxwell Andrews*

8:40 AM **DD2 (Student), Protection of Compliant $In_{0.25}Ga_{0.75}As$/GaAs Structures During Lateral Oxidation Using an Amorphous InGaP Layer**
..... *Gregory W. Pickrell*

9:00 AM **DD3 (Student), Structural Instability of Wet Oxidized GaP and $Al_{0.4}Ga_{0.6}P$**
..... *Kuo-Lih Chang*

9:20 AM **DD4, Properties of InAlP Native Oxides Supporting MOS Inversion-Layer Behavior**
..... *Pedro J. Barrios*

9:40 AM **DD5, Deep Oxidation of AlGaAs Heterostructures for Strongly-Confined Optical Waveguides**
..... *Douglas C. Hall*

10:00 AM **DD6 (Student), Microwave Annealing for Ultra-Shallow p+-n Junctions**
..... *Taras Kirichenko*

2001 Electronic Materials Conference

TECHNICAL PROGRAM

University of Notre Dame · Notre Dame, Indiana · June 27–29, 2001

Wednesday, June 27, 2001

EMC PLENARY LECTURE/STUDENT AWARDS

Ceremony: 8:20 AM

Room: Washington Hall

Session Chairman: M. R. Melloch, Purdue University, School of Electrical and Computer Engineering, West Lafayette, IN 47907 USA

Plenary Speaker: Nick Holonyak, Jr.
University of Illinois at Urbana–Champaign, Electrical Engineering Research Laboratory & Center for Compound Semiconductor Microelectronics, Urbana, IL 61801 USA

Topic: From the Transistor to the Light Emitting Diode and Laser

Break: 9:20 AM-10:00 AM

Session A: Epitaxy for Devices

Wednesday AM Room: 129
June 27, 2001 Location: University of Notre Dame

Session Chair: Mike Tischler, ATMI, Mesa, AZ 85210 USA

10:00 AM (Student)
A1, AlInAs/GaAs$_{0.51}$Sb$_{0.49}$/GaInAs Heterojunction Bipolar Transistors Grown by Solid Source Molecular Beam Epitaxy: *Changhyun Yi*[1]; Tong-Ho Kim[1]; April S. Brown[1]; [1]Georgia Institute of Technology, Sch. of Electl. & Comp. Eng., Microelect. Rsrch. Ctr., Atlanta, GA 30332 USA

InP-based GaAs$_{0.51}$Sb$_{0.49}$-base HBTs exhibit significant performance and manufacturing advantages over "conventional" GaInAs-base HBTs with InP or AlInAs emitters[1]. These advantages include the high valence band discontinuity (GaAsSb/AlInAs = 0.64 eV), and the ability to exploit an abrupt emitter-base junction due to the type-II nature of the AlInAs-GaAsSb junction and the absence of a conduction band spike affecting the transport of electrons from base to emitter. These effects should lead to high gain and low turn on voltage with high breakdown (for an InP collector). Key issues to address in these structures are the achievement of low resistivity bases, high quality mixed anion interfaces, and control of the alloy composition of the base. The high performance results reported recently[1] are for structures grown by MOCVD with C doping. Herein, we report the growth and characteristics of AlInAs/GaAsSb/GaInAs heterojunction bipolar transistors using solid source MBE (As and Sb cracker cells) and Be doping. We have utilized an AlInAs emitter to minimize the number of dissimilar anions at the emitter-base junction, and to add a slight (10 meV) energy launch to electrons entering the base. The AlInAs/GaAsSb/GaInAs HBTs were grown on InP substrates at a substrate temperature of 500°C. 300K Hall measurements were used to assess the electronic properties of p-type GaAsSb. As-grown undoped GaAs$_{0.51}$Sb$_{0.49}$ layer shows p-type conductivity with a background concentration of 3.2x10^{16} cm^{-3}. Si and Be were used as n- and p-type dopants, respectively. Structures with 100x100 µm^2 emitters were fabricated with a fully self-aligned triple mesa process. A base doping level (Be) of 3x10^{19} cm^{-3} was used. The measured turn-on voltage was V_{BE} = 0.36 V at J_C = 1 A/cm^2. This turn-on voltage is approximately 50% lower than that of an abrupt AlInAs/GaInAs HBT. The typical turn-on voltage of InP-based abrupt HBT is 0.6 ~ 0.7 V in current literature. The collector emitter offset voltage ($V_{CE\text{-}offset}$) was 0.23 V while that of the abrupt AlInAs/GaInAs HBT is approximately 0.45 V. The collector emitter breakdown voltage BV_{CEO} was 3 ~ 4 V at I_C = 5x10^{-4} A/cm^2. For the 100x100 µm^2 emitter size, the dc current gain was 25 ~ 30 with collector current ideality factor η_C = 1.02 and base current ideality factor η_B = 1.1 compared to AlInAs/GaInAs SHBT with η_C = 1.2 and η_B = 1.45. [1]M. W. Dvorak, O. J. Pitts, S. P. Watkins, C. R. Bolognesi, "Abrupt Junction InP/GaAsSb/InP Double Heterojunction Bipolar Transistors with F_T as High as 250 GHz and BV_{CEO} > 6 V", 2000 IEDM, pp. 178 ~ 181.

10:20 AM (Student)
A2, Characterization of GaAsSb 1.3µm QW Heterostructures Grown by Metalorganic Chemical Vapor Deposition: *Min-Soo Noh*[1]; Jae-Hyun Ryou[1]; Laura Giovane[2]; Sheila Mathis[2]; Robert Weissman[2]; Frederick A. Kish[2]; Ying-Lan Chang[3]; Russell D. Dupuis[1]; [1]The University of Texas at Austin, Microelect. Rsrch. Ctr., 10100 Burnet Rd., Austin, TX 78758 USA; [2]Agilent Technologies, Network Solutions Div., 370 Trimble Rd., San Jose, CA 95131 USA; [3]Agilent Technologies, Corp. Rsrch. Lab., 3500 Deer Creek Rd., Palo Alto, CA 94304 USA

Lasers emitting at ~1.33µm or 1.55µm are one of the most important optoelectronic devices for optical fiber communication systems. Recently, Vertical Cavity Surface Emitting Lasers (VCSELs) operating at 1.3µm have been attracting great interest for high-performance communication system applications. The conventional material for 1.33µm laser operation is InGaAsP grown on InP substrates. However, InGaAsP/InP VCSEL structures lack suitable high refractive index contrast Distributed Bragg Reflector (DBR) pairs. Alternately, it is desirable to grow long-wavelength VCSELs on GaAs substrates because this would permit the use of well-developed GaAs-based laser technologies like large-area processing, oxidation-compatible material systems, and good DBR pair materials. Recently, GaAsSb materials have been studied for this application. Strained GaAsSb QW heterostructures grown on GaAs substrates can be good candidates for this purpose in spite of the large miscibility gap expected for typical growth conditions and the expected Type-II band alignment of the GaAsSb/GaAs heterojunction. In this work, GaAs$_{1-x}$Sb$_x$ QW heterostructures were grown by low pressure MOCVD using various growth parameters such as the growth temperature (Tg), V/III ratio, gas-phase Sb mole fraction of the Group V elements, and various QW barrier materials. The structures were analyzed by X-ray diffraction, transmission electron microscopy, secondary ion mass spectrometry, photoluminescence (PL), and cathodoluminescence (CL). Control of the fundamental growth parameters, e.g., Tg and the V/III ratio, was very important to achieve good crystalline quality of the QW. As the Sb mole fraction of the Group V elements increases, the solid composition also increases up to x=0.33 but the optical properties become dramatically poorer. To explore the band alignments, GaAsSb dual-quantum well separate-confinement heterostructures (DQW-SCHs) were grown using GaAs, AlGaAs, InGaP, and InGaAs waveguide/barrier structures with Al$_{0.40}$Ga$_{0.60}$As cladding layers. The Type I band-to-band and Type-II transitions were studied using PL at room temperature and at 4K and CL at 10K. At 4K, the PL spectra for GaAsSb/GaAs QWs taken under variable-excitation CW conditions show no multiple peaks due to the expected Type-II band alignment. However, we could conclude indirectly that these samples had a Type-II band alignment because a shorter PL wavelength is observed with higher Eg waveguide materials. Furthermore, variable excitation CL studies clearly show both Type-I and Type-II luminescence transitions. For the GaAsSb/InGaAs case, we have obtained Type-II PL emission at

~1.3µm at 300K. From the 4K variable-excitation PL spectra, the heterojunction band alignments and the conduction-band offsets for the various waveguide materials were calculated. We also fabricated broad-area laser diodes with a GaAsSb/GaAs SQW-SCH structure. These devices lased at λ=1.1µm at 300K in a pulsed mode (50µm stripe and 500µm cavity length) at a threshold current density of ~2.7kA/cm^2. We will describe the results of the heterojunction studies and the corresponding device results.

10:40 AM (Student)

A3, Growth and Properties of Lattice-Matched and Mis-Matched InGaAs Tunnel Junctions for Mid-Infrared Devices Grown on Graded InAlAs/InP Substrates: *Ojin Kwon*[1]; Steven A. Ringel[1]; M. M. Jazwiecki[1]; [1]The Ohio State University, Dept. of Electl. Eng., 2015 Neil Ave., Columbus, OH 43210 USA

Lattice-matched and lattice-mismatched $In_xGa_{1-x}As$ materials grown on GaAs and InP substrates are receiving considerable attention due to their enabling potential for achieving ultra-high speed electronic devices and a wide range of infrared optoelectronic devices. The small electron effective mass, the wide range of bandgaps spanned by this alloy system, and the fact that bandgap engineered heterostructures involving the InGaAlAsP materials are together allowing the enhancement and/or development of devices such as metamorphic HEMT's, quantum cascade lasers, multiple wavelength detectors and thermophotovoltaic (TPV) devices. One application of great interest for infrared TPV devices and multi-wavelength detectors is the use of $In_xGa_{1-x}As$ for electrical interconnects between series-connected optical sub-elements. Here, $In_xGa_{1-x}As$ tunnel junctions are explored, which can act as quasi-ohmic, low-resistance interconnects. For these optoelectronic applications, the tunnel junction must provide an ultra-low resistance "quasi-ohmic" interconnect, and must not act as an optical parasitic element via optical absorption. Hence, highly-doped, ultra-thin tunnel junctions are needed in order to simultaneously limit both electrical and optical parasitics so that maximum device performance can be realized. Moreover, the composition of the $In_xGa_{1-x}As$ comprising the tunnel junction must be chosen so that lattice-matching is preserved between the various devices being interconnected together, which themselves may be mismatched with respect to the substrate to achieve the desired bandgap profile. Hence, this paper explores the growth, material properties and device characteristics of ultra-thin $In_xGa_{1-x}As$ tunnel junctions grown by solid source molecular beam epitaxy (MBE) on InP and graded InAlAs/InP substrates for lattice matched (x = 0.53, Eg = 0.74eV), and lattice-mismatched (x = 0.69, Eg = 0.60eV and x = 0.75, Eg = 0.55eV) compositions. Extremely thin (200Å total device thickness), lattice-matched $In_{0.53}Ga_{0.47}As$ and lattice-mismatched $In_{0.69}Ga_{0.31}As$ tunnel junctions have been grown by MBE on InP substrates. Carbon was used to achieve p-type doping for these compositions. An extremely high maximum peak current density of over 5900 A/cm^2 and very low specific resistivity of $5.22x10^{-5}$ A/cm^2 were obtained for the 0.60 eV bandgap $In_{0.69}Ga_{0.31}As$ tunnel junction. In addition, a beryllium-doped, lattice-mismatched 0.55eV bandgap $In_{0.75}Ga_{0.25}As$ tunnel junction was grown which demonstrated a peak current density of 1350A/cm^2 as well as a low resistivity of $1.36x10^{-4}$ A/cm^2 at zero applied bias. Based on X-ray analysis, the $In_xGa_{1-x}As$ compositions of lattice-mismatched tunnel junction layers were within approximately 0.5% of intentional indium composition. Carbon-doped p-type junction layers analyzed by secondary ion mass spectroscopy (SIMS) showed less carbon diffusion with steeper doping profile compared to beryllium-doped layers. Dependence of the current-voltage results on composition, bandgap, strain state, dopant type (carbon vs. beryllium) and concentration will be discussed by correlating with SIMS and triple axis X-ray diffraction analyses that have recently been completed.

11:00 AM (Student)

A4, Growth and Characterization of Low-Oxygen Content AlAs/AlGaAs DBRs and InAlP Cladding Layers: *Richard Dean Heller*[1]; David A. Kellogg[2]; Gabriel Walter[2]; Nick Holonyak[2]; Ravi Kanjolia[3]; Barry Leese[3]; Russell D. Dupuis[1]; [1]The University of Texas at Austin, Microelect. Rsrch. Ctr., 10100 Burnet Rd., Bldg. 160, Austin, TX 78758 USA; [2]University of Illinois at Urbana–Champaign, Ctr. for Compd. Semicond. Microelect., 208 N. Wright St., Urbana, IL 61801 USA; [3]Epichem, Inc., 26 Ward Hill Ave., Haverhill, MA 01835-0739 USA

The InAlGaP and AlGaAs III-V material systems are of great technological interest and are employed in many applications in the fields of optoelectronics and high-speed electronic devices. Of particular current interest are the wide-bandgap compound semiconductors grown lattice-matched to GaAs substrates such as high-aluminum mole fraction $Al_xGa_{1-x}As$ (x>0.5) and $In_xAl_{1-x}P$ (x~0.5) layers. For example, AlAs and $Al_{0.98}Ga_{0.02}As$ layers are widely used in vertical-cavity surface emitting lasers as the low-index layer in a distributed Bragg reflector mirror and for oxidized current controlling layers. AlGaAs and InAlP are also potentially useful for native-oxidize DBRs thereby dramatically reducing the number of pairs of lower- and higher-index materials needed to increase the reflectivity to ~99%. We have grown and characterized AlAs/AlGaAs DBRs and InAlP cladding layers for use in native-oxide confined $Al_yGa_{1-y}As/In_{0.5}(Al_xGa_{1-x})_{0.5}P$ quantum-well heterostructure lasers and optimized the growth for low-oxygen and low unintentional impurity content. These structures were grown by low-pressure MOCVD in a modified EMCORE GS3200 UTM reactor at a pressure of 60 Torr using adduct-purified trimethylindium, trimethylaluminum, triethylgallium, AsH_3, and PH_3 as sources and purified H_2 as a carrier gas. Diethylzinc and bis(cyclopentadienyl)magnesium were used as the Zn and Mg p-type dopants, respectively. The lattice matching conditions for the AlGaAs, InGaP, InAlGaP alloys were established using X-ray rocking curve and photoluminescence characterization of ~500 nm thick layers. Impurity concentrations were measured using electrochemical profiling. The oxygen, silicon, and carbon impurity levels were measured using SIMS. For AlGaAs DBRs, we have measured the [O] in AlAs layers to be as low as ~5E16 cm^{-3} and silicon levels to be ~3E16 cm^{-3} using SIMS. The background impurity level is dependent on source quality and growth conditions, e.g., V/III ratio, growth temperature. Furthermore, in InAlP:ud structures we have measured the [O] level to be ~9E16 cm^{-3}, the [Si] level to be ~3E16 cm^{-3}, and the [C] level to be ~3E16 cm^{-3}. SIMS measurements of the oxygen, silicon, and carbon impurity levels for Mg and Zn doped InAlP layers were made to determine the impurities introduced by these sources. For InAlP:Mg, the oxygen, silicon, and carbon levels appear to be ~8E16 cm^{-3}, 2E16 cm^{-3}, and 2E16 cm^{-3}, respectively. The [O] level is the only impurity that appears to be increased by the Mg source. For InAlP:Zn, the oxygen, silicon, and carbon levels appear to be ~7E16 cm^{-3}, 2.5E16 cm^{-3}, and 6E16 cm^{-3}, respectively. The [C] level is the only impurity that appears to be increased by the Zn source. Broad-area InGaP quantum well laser diodes using these InAlP layers have lased at 300K under pulsed conditions at threshold current densities around 500-800 A/cm^2 at wavelengths from 630 to 650 nm. We will report the details of the growth and the doping characteristics of these structures.

11:20 AM (Student)

A5, Monolithic Integration of a Heat Pump and a Laser Diode in a Single Epitaxial Growth: *Jizhi Zhang*[2]; Kei May Lau[1]; Neal G. Anderson[2]; [1]Hong Kong University of Science & Technology, EEE Dept., Clear Water Bay, Kowloon, Hong Kong; [2]University of Massachusetts–Amherst, ECE Dept., Amherst, MA 01003 USA

As an alternative to thermoelectric (TE) cooling, it is very attractive to epitaxially integrate a cooler with a laser diode for thermal management. Recently, a single-stage cooling of 1°C was reported using a thermionic (TI) cooler[1]. The TI cooler is very suitable for integration comparing to TE cooler. Although the cooling of a TI cooler has not shown to be very effective, it may be useful as a heat pump to help heat dissipation. In this paper, we propose and report preliminary results of a monolithically integrated heterostructure tunneling-junction heat pump and a 980nm GRIN-SCH laser diode grown in single run of low pressure MOCVD. The test structure of this concept is a regular GRIN-SCH followed by a Zener diode. On a n++ GaAs substrate, a 1.2µm lower cladding layer of 6.7E17 cm-3 n-Al0.38Ga0.62As was grown at 800°C. Followed was the regular GRIN-SCH grown at 700°C, comprised of two undoped 10nm GaAs barriers, an 8nm undoped In0.22Ga0.78As quantum well, and two undoped GRIN layers with Al composition grading from 0.06 to 0.38. Then a 500nm 5E17 cm-3 p-Al0.38Ga0.62As layer was deposited at 700°C for the first part of upper cladding layer. After that, a 50nm carbon-doped p++-GaAs layer was deposited at 550°C to a level of 1.2E20 cm-3, followed by a 50nm 6.9E18 cm-3 n+-GaAs layer deposited at 700°C forming a tunneling junction. Right after is a 700nm 1.0E17 cm-3 n-Al0.38Ga0.62As grown at 800°C. Finally a 100nm 6.9E18 cm-3 n-GaAs layer was grown at 700°C for contact. In this integrated structure, when the active layer of the laser is forward biased, the p++n+ GaAs tunneling junction is reverse-biased. Electrons in the valence band of the p++-GaAs layer tunnel through to the n+-side, then thermally excited and transported to the n-AlGaAs layer of high band gap. This thermionic

emission is a process of energy absorption and heat dissipation. The holes in the reversed-biased Zener diode are driven to the p-AlGaAs layer on the other side. Broad area lasers with stripe width of 100µm and cavity length of 500µm were fabricated and mounted epi-side up on a heat sink for testing. They were characterized under 100Hz pulsed current with a duty cycle of 1/1000. The laser diode with the integrated heat pump has a threshold current density (Jth) of 210A/cm2 in contrast to 150A/cm2 for our conventional laser without the heat pump at 290K. The increased threshold current density is a result of the additional structures and potential Franz-Keldysh effect in this junction. However, the T0 of the integrated laser diodes remains constant at 290K up to a test temperature of 410K, while that of our conventional laser diodes increases after the test temperature reaches 360K. These preliminary results suggest that the concept of heat pumping in laser diodes may be viable using the proposed technique. [1]A. Shakouri, et al, Appl. Phys. Lett. vol. 74, No.1, pp 88-89, 1999.

Session B: Joint EMC & DRC Session on Modeling of Materials and Nanostructures

Wednesday AM Room: 102
June 27, 2001 Location: University of Notre Dame

Session Chair: Supriyo Bandyopadhyay, University of Nebraska–Lincoln, Dept. of EE, Lincoln, NE 68588-0511 USA

10:00 AM

B1, Spin-Orbit Interaction of 2° in InAlAs/InAs Heterostructures: *Kanji Yoh*[1]; Toshihiro Doi[1]; Shin-ichiro Abe[2]; Yoshito Katano[1]; Hiroshi Ohno[2]; Kazuhisa Sueoka[2]; Koichi Mukasa[2]; [1]Hokkaido University, RCIQE, N13, W8, Kita-ku, Sapporo, Hokkaido 060-8628 Japan; [2]Hokkaido University, Grad. Sch. of Eng., N13, W8, Kita-ku, Sapporo, Hokkkaido 060-8628 Japan

Spin-orbit interaction of electrons in surface inversion layers is known to be pronounced in mid-narrow gap semiconductors such as InAs or InSb. However, investigation of those materials suffer from substrate leakage current due to interband tunneling because of their narrow bandgap. Here we report the transport characterization of $In_{0.8}Al_{0.2}As/InAs$ haterostructures grown on p-type InAs substrate(1). Shubunikov de Haas oscillation of the InAs surface inversion layer was successfully measured by improved heterointerface quality and reduced interband tunneling current. As a result, spin-orbit interaction was estimated through Rashba oscillation. The heterointerface of arsenic-based material system was achieved by growing strained thin InAlAs barrier on top of undoped InAs channel layer. The molecular beam epitaxially grown heterostructure is composed of p^+-InAs substrate, 1µm of p-InAs buffer layer, 500Å of InAs and 80Å of InAlAs. The surface electrode of Ti/Au was deposited on top of the surface so that the ohmic contact to the surface inversion layer was taken through the tunneling barrier. The current voltage characteristics with wide voltage bias revealed that 2° saturation characteristics dominates at relatively low bias (-1V to +1V) and the substrate leakage current dominates at higher bias (>1.5V). At low current region, the Shubunikov de Haas oscillation was successfully obtained at 4K. The carrier concentration at the inversion layer was estimated to be $6.9x10^{11}cm^{-2}$. The spin-orbit coupling constant(2) of α_{zero} = 27 ($x10^{-12}$eVm) or 12meV in spin split energy at Fermi level. The estimation decreases if we replace the effective mass of the bulk InAs value with higher value taking into account of the non-parabolicity of the energy band. However, the separate direct measurement of the spin split of the same sample exhibit band split energy of 14meV which is not so far from the estimation by Rashba oscillation. The present spin-orbit result is comparable to the number obtained in the strain relaxed $In_{0.75}Ga_{0.25}As/In_{0.75}Al_{0.25}As$ heterostructure(3). [1]D.C. Tsui, Phys. Rev. B 4, 4438 (1971) [2]Th. Schaepers et al, J. Appl. Phys. 83, 4324 (1998) [3]S. Yamada et al, 4th International Workshop on Quantum Functional Devices (Kanazawa, 2000).

10:20 AM (Student)

B2, Thermal Conductivity in Semiconductor Thin Films and Nanowires: *Jie Zou*[1]; Alexander A. Balandin[1]; [1]University of California at Riverside, Dept. of Electl. Eng., Riverside, CA 92521 USA

As the device feature dimensions continue to shrink toward nanometer scale, thermal properties of semiconductor low-dimensional structures are beginning to attract significant attention[1]. Downscaling trend in electronic and optoelectronic devices leads to an increase in power dissipation (per unit area) despite the reduction of the power supply voltage[2]. A variety of size effects that manifest themselves at nanoscale may adversely affect the removal of excessive heat. At the same time, these effects are very interesting from the fundamental-science point of view[3]. In this talk we present a self-consistent model for calculating the lattice thermal conductivity in semiconductor thin films and nanowires. The model is based on the solution of phonon Boltzmann equation. It rigorously takes into account modification of the acoustic phonon dispersion in low-dimensional structures with the lateral feature size of 10 nm-30 nm, and change in the non-equilibrium phonon distribution due to partially diffuse scattering from rough boundaries and interfaces. It will be shown that the presence of distinctive boundaries in such structures leads to a transformation of the acoustic branches of phonon dispersion to quasi-optical branches characterized by a low group velocity and different cut-off frequencies. This transformation affects both in-plane and cross-plane thermal conduction in low-dimensional structures. In this talk we also analyze three-phonon Umklapp scattering processes in thin films and nanowires and compare them with those in bulk semiconductors. The predictions of the thermal conductivity values based on our model are in good agreement with available experimental data for silicon thin films and nanowires. The described changes in phonon transport in semiconductor thin films and nanowires bear important consequences for nanostructure and device simulation since neither Fourier heat theory nor Debye approximation are accurate at nanometer length scale. The observed modification of the thermal resistance of the low-dimensional structures has to be taken into account in simulation of thermal transport in deep-submicron devices since it strongly affects the electrostatic discharge voltage (EDS) and other reliability characteristics. The change in the acoustic phonon dispersion and group velocity may be partially responsible for the experimentally observed drop of EDS in devices based on thin-film silicon-on-insulator (SOI) wafers. [1]G. Chen, Int. J. Therm. Sci. 39, 471 (2000); [2]International Technology Roadmap for Semiconductor Industry, 1999; [3]J. Zou and A. Balandin, Phonon heat conduction in a semiconductor nanowire, to appear in J. Appl. Phys., 2001.

10:40 AM (Student)

B3, Quantum Mechanical Calculation of QCA Molecule Properties: *Christopher J. Russo*[1]; *Craig S. Lent*[1]; [1]University of Notre Dame, Electl. Eng., 275 Fitzpatrick, Notre Dame, IN 46556 USA

Current computer architecture based on integrated silicon CMOS technology is rapidly approaching fundamental limits of scalability, primarily as a result of energy dissipation considerations. In the search for a new paradigm to achieve speeds and densities well beyond the foreseen limits of CMOS, a new model of device design using charge state and Coulomb interaction for information storage and propagation has been proposed. This paradigm of computation, based on Quantum Cellular Automata (QCA), provides a natural approach to the design of molecules that can encode and propagate binary information in their charge configurations. We investigate the properties of potential QCA molecules, using quantum mechanical calculations in the local density approximation. Specifically, the switching of a two-state cell with an appropriate driver charge is shown. Calculations of experimentally accessible molecular properties are investigated, and further details of molecular cell bistability are explored.

11:00 AM

B4, Nano-Transistor Modeling: Two Dimensional Green's Function Method: *A. Svizhenko*[1]; M. P. Anantram[1]; T. R. Govindan[1]; B. Biegel[1]; [1]NASA, Ames Rsrch. Ctr., MS T27A-1, Moffett Field, CA 94035-1000 USA

Two quantum mechanical effects that impact the operation of nanoscale transistors are inversion layer energy quantization and ballistic transport. While the qualitative effects of these features are reasonably understood, a comprehensive study of device physics in two dimensions is lacking (SIA Roadmap). Our work addresses this shortcoming and provides: (a) a framework to quantitatively explore device physics issues

such as the source-drain and gate leakage currents, DIBL, and threshold voltage shift due to quantization, and (b) a means of benchmarking quantum corrections to semiclassical models (such as density-gradient and quantum-corrected MEDICI). We have developed physical approximations and computer code capable of realistically simulating 2-D nanoscale transistors, using the non-equilibrium Green's function (NEGF) method. This is the most accurate full quantum model yet applied to 2-D device simulation. Open boundary conditions and oxide tunneling are treated on an equal footing. Acoustic phonon scattering is included, causing transport to deviate from ballistic in a realistic manner. Electrons in the ellipsoids of the conduction band are treated within the anisotropic effective mass approximation. Self-consistent solution of Poisson-NEGF equations is numerically intensive because of the number of spatial and energy coordinates involved. This makes the use of parallel/distributed computing imperative. For the self-consistent calculations presented here parallelization is performed by distributing the solution of NEGF equations to various processors, energy wise. The calculations were performed on a SGI Origin 2000 at the NAS computing facility located at the NASA Ames Research Center. We present simulation results for the "benchmark" MIT 25nm and 90nm MOSFETs[1]. We compare our results (labeled "quantum") to those from the PROPHET (classical) drift-diffusion simulator (labeled "DD") and the quantum-corrected MEDICI results (labeled "Medici") available in[1]. In the 25nm MOSFET, the channel length is less than ten times the electron wavelength, and the electron scattering time is comparable to its transit time. Our main results are: (i) Simulated subthreshold and drain current characteristics are shown in Fig. 1 (a,b) where the potential profiles are calculated self-consistently by the corresponding simulation methods. The current predicted by our quantum simulation has smaller subthreshold slope of the Vg dependence which results in higher threshold voltage. (ii) Quantum mechanically calculated electron density is much smaller than the background doping density in the poly silicon gate region near oxide interface. This creates and additional effective gate voltage (Fig. 2). Different ways to include this effect approximately will be discussed. (iii) We have developed a method to calculate the gate-oxide leakage current (tunnel current) within the context of the NEGF method. Fig. 3 compares the drain and gate-oxide leakage current for the MIT 25nm MOSFET, and for the same device with a 25nm gate length, for gate-oxide thickness of 1.5nm. There is an important difference in that the shorter gate length device has twenty times smaller current at zero gate bias than the longer gate length device, while the on-current at large gate voltages are comparable. This trend is true for a wide range of oxide thicknesses (Fig. 3b) and should be a device consideration. [1]The well tempered MOSFET information is at www-mtl.mit.edu:80/Well

11:20 AM

B5, A Coupled Shrödinger/Monte Carlo Technique for Quantum-Corrected Device Simulation: *Brian Winstead*[1]; Umberto Ravaioli[1]; [1]University of Illinois at Urbana–Champaign, Beckman Inst., Urbana, IL 61801 USA

As silicon MOSFETs are scaled below 100nm, quantum effects become a critical consideration. The development of accurate and practical full quantum transport models for these devices is a daunting task. Fortunately, quantum coherence along the transport path is not expected to become significant for room temperature operation until extremely scaled lengths in the sub-10nm regime. Thus for practical device simulation, a natural prescription is to try to retain the very mature semi-classical techniques as much as possible. To do this, the essential quantum effects such as tunneling and quantization can be captured as corrections to the semi-classical model. Physically based models such as full-band Monte Carlo are a useful starting point to add quantum corrections because they adequately describe the non-equilibrium and hot carrier phenomena which dominate today's devices, and can be used to calibrate lower levels of the simulation hierarchy such as drift-diffusion. Quantum extensions to semi-classical simulation comprise an active area of research and recent Monte Carlo models have been developed based on approximations to the Wigner transport equation[1] and on the Feynman effective potential[2]. In addition, quantum corrections based on approximate or exact 1-D Schrödinger solutions have been developed for drift-diffusion by several authors[3,4]. Here we present a new model for quantum-corrected full-band Monte Carlo device simulation which accounts for quantum repulsion at the silicon/gate-insulator interface through a self-consistent coupling with the Schrödinger equation. In a coupled Monte Carlo-Schrödinger simulation, the Schrödinger equation is periodically solved along 1-D slices of a 2-D domain. The quantum concentration slices are regarded as envelope functions for the Monte Carlo solution, and the Monte Carlo potential is corrected to reflect their shape. The correction is formulated in such a way that it is not a function of the particular magnitude of the quantum concentration, and thus there is no problem posed by the absence of the fermi level concept in a Monte Carlo model. In this work, the Monte Carlo-Schrödinger method is applied to a MOS capacitor for a wide range of biases, and is compared to self-consistent Schrödinger-Poisson calculations for validation. Preliminary results for a 2-D MOSFET simulation are also presented.

11:40 AM

B6, Quantitative Prediction of Threshold Voltage Fluctuations in Sub-100 nm MOSFETs by a New Dopant Model: *Hiroyuki Yamamoto*[1]; Yoshimitsu Okada[1]; Nobuyuki Sano[1]; [1]University of Tsukuba, Inst. of Appl. Phys., 1-1-1 Tennoudai, Tsukuba, Ibaraki, 305-8573 Japan

Threshold voltage (V_{th}) fluctuation associated with the discreteness of random dopants in the substrate is becoming a real and serious problem for future large-scale integrations of ultra-small MOSFETs. This problem has been theoretically investigated by the conventional 3-D and/or 2-D Drift-Diffusion (DD) simulations [1-3]. However, it has been pointed out that a naive application of the conventional dopant model to the extreme 'atomistic' situations, which is the case for most studies carried out so far, is physically incorrect and that the separation of the long-range and short-range parts of the Coulomb potential of the dopant is crucial in modeling the random discrete dopants [4]. Therefore, quantitative investigations of V_{th} variations with a reliable dopant model are of great importance. In the present paper, V_{th} fluctuations in sub-100 nm MOSFETs are studied in a predictable manner by employing a new dopant model that explicitly splits the long-range and short-range potentials of dopants.

Session C: Contact to Wide Bandgap Semiconductors – I

Wednesday AM Room: 141
June 27, 2001 Location: University of Notre Dame

Session Chairs: Lisa Porter, Carnegie Mellon, Dept. of Matls. Sci. & Eng., Pittsburgh, PA 15213-3890 USA; Karl-Mikael Zetterling, RTH Royal Institute of Technology, Kista S-16440 Sweden

10:00 AM (Student)

C1, Impact of Material Defects on SiC Schottky Barrier Diodes: Dallas T. Morisette[1]; James A. Cooper[1]; [1]Purdue University, Sch. of Electl. & Comp. Eng., 1285 Electrical Engineering Bldg., West Lafayette, IN 47907-1285 USA

This paper describes a study on the effect of material defects on SiC Schottky barrier diodes. Similar experiments on SiC PN diodes have been reported recently[1,2]. In this study we construct a detailed map of defects on a test wafer using synchrotron white beam x-ray topography (SWBXT) and electron beam induced current (EBIC), observe the electrical behavior of small diodes that are either defect free or contain a known defect, and determine the correlation between the observed electrical behavior and the presence of defects within the device. The study is conducted on a 50 mm diameter n-type 4H-SiC substrate with a 10 µm n-type epilayer doped 1e16 cm-3 with nitrogen. Individual die 2 mm square are defined by RIE. The wafer is then mapped using SWBXT and EBIC, and Schottky diodes ranging in diameter from 30-200 µm are fabricated within each die. Edge termination is formed by implanting 1e15 boron atoms per square cm at 30 keV in 30 µm rings surrounding each diode. The implants are activated at 1050°C to remove lattice damage without activating the dopants[3]. Nickel Schottky contacts are deposited by E-beam evaporation and patterned by liftoff. I-V measurements indicate a barrier height of 1.4 eV, an ideality factor of 1.1, and a breakdown voltage of 1400 V.

Leakage measurements on 200 devices reveal 158 diodes with nearly identical leakage characteristics, similar to those previously reported[4]. The other 42 diodes exhibit excessive reverse bias leakage. The average screw dislocation (SD) density on this wafer, as revealed by SWBXT, is 4,096 per square cm, and the density of EBIC defects is 29,400 per square cm. Of 200 diodes, 59% contain SD's and 98% contain EBIC defects. Diodes are classified as 1) defect free, 2) SD in diode area, 3) SD in edge termination ring, 4) EBIC defect in diode area, and 5) EBIC defect in termination ring. Surprisingly, to within statistical error, the probability of finding a good device is the same for each category, indicating there is no correlation between SD's or EBIC defects and excessive leakage current. In fact, 58% of the 158 well-behaved diodes contain SD's and 97% contain EBIC defects, while 40% of the diodes with excessive leakage current are completely free of SD's. This unexpected result suggests that, unlike SiC PN diodes[1,2], the reverse leakage current in SiC Schottky diodes is not dominated by either SD's or EBIC defects. While these defects may impact device performance in other ways, they do not appear to prevent the manufacture of high-voltage low-leakage SiC Schottky barrier diodes. A more detailed discussion of these results will be presented at the conference. Acknowledgements: We thank P. G. Neudeck and S. G. Bailey, NASA Glenn Research Center, for assistance with processing, EBIC imaging, and for helpful conversations, and M. Dudley of SUNY Stony Brook for SWBXT imaging. This work is supported by ONR/MURI grant No. N00014-95-1-1302. [1]R. Raghunathan, B. J. Baliga, Applied Physics Letters, 72, 3196 (1998); [2]P. G. Neudeck et al., IEEE Trans. Electron Devices, 46, 478 (1999); [3]A. Itoh, et al., Proc. 6th Int'l Conf. on Silicon Carbide and Related Materials, 685 (1996); [4]K. Schoen et al., IEEE Trans. Electron Devices, 45, 1595 (1998).

10:20 AM (Student)

C2, Chemically-Dependent Traps and Polytypes at Pt/Ti Contacts to 4H and 6H-SiC: *Sergey P. Tumakha*[1]; Leonard J. Brillson[2]; Gregg H. Jessen[2]; Robert S. Okojie[3]; D. Lukco[3]; [1]Ohio State University, Dept. of Phys., 174 W. 18th Ave., Columbus, OH 43210 USA; [2]Ohio State University, Electl. Eng., 205 Dreese Lab., Columbus, OH 43210 USA; [3]NASA Glenn Research Center, 21000 Brookpark Rd., MS 77-1, Cleveland, OH 44135 USA

We have used low energy electron-excited nanoluminescence (LEEN) spectroscopy combined with X-ray photoemission spectroscopy (XPS) to probe deep level defect states at interfaces of 4H and 6H-SiC with Pt/Ti. SiC represents an excellent candidate for high temperature electronic device applications because of its high thermal and chemical stability under harsh chemical conditions. We studied the process conditions under which thermally-stable Ohmic and Schottky contacts can be prepared on SiC while minimizing the formation of deep level electronic states. LEEN measurements taken over a range of incident electron beam energies EB from 0.5 to 4 keV provide a means to identify the presence of localized states and their spatial distribution on a nanometer scale. With increasing EB, the electron cascade and resultant generation of free electron-hole pairs peak at increasing depth, ranging from 5 nm at 1 keV to 60 nm at 4 keV for the Pt/Ti/SiC systems. Thus it is possible to excite luminescence selectively either at the intimate metal-SiC interface, the near-interface region extending tens of nanometers into the SiC, or the bulk SiC up to 0.2 microns into the solid. These electronic state measurements can then be correlated with chemical bonding and composition as measured via XPS. For the 6H-SiC specimens, we observed optical emission that varies with depth from the intimate interface and with SiC chemical preparation. The depth-dependent spectra exhibit 2.9 eV near band edge (NBE) features of 6H-SiC for bulk excitation, while they show a disordered and/or defected region within a few nanometers of the metal contact. Spectra from the near interface region indicate the existence of a SiC polytype with a higher band gap of ~ 3.4 eV- resembling 4H-SiC. Excitation of the intimate metal-SiC interface reveals the presence of a discrete state deep within the SiC band gap, i.e., emission energy = 1.9 eV, at a particular stage of the surface preparation. Significantly, XPS C 1s spectra of the SiC surface prior to meta llization reveal a striking change in C bonding for this same chemical treatment with a chemical component bonded almost 2 eV more strongly than C in SiC after multiple etching cycles. Analogous chemical treatments of 4H-SiC produce not only the 1.9 eV trap level but also a lower band gap SiC polytype with ~ 2.6 eV energy extending tens of nanometers beyond the interface. XPS measurements reveal significant differences in C 1s chemical bonding changes with process steps between the 4H and 6H-SiC surfaces. This work is the first to show the effect of metal-semiconductor interactions on not only localized states but also the lattice structure of the semiconductor near the interface. This work was supported in part by NASA, AFOSR, NSF, DOE, and Glennan Microsystems Initiative (GMI).

10:40 AM

C3, Influence of Semiconductor Surface Properties on the Ohmic Contact Characteristics for p-Type Silicon Carbide: *T. Worren*[1]; T. Jang[1]; D. J. Ewing[1]; L. M. Porter[1]; [1]Carnegie Mellon University, Dept. of Matls. Sci. & Eng., Pittsburgh, PA 15213 USA

In this study we have investigated important effects of the condition of the p-type 6H-SiC surface on the properties of ohmic contacts. The fabrication of reproducible ohmic contacts with low specific contact resistivities (SCR's) to p-type SiC is a critical problem for many SiC-based devices. The traditional approach consists of annealing an Al-based contact (e.g., TiAl) on highly doped SiC at temperatures between 900 and 1150°C. Another approach employs one or more Si layers along with a transition metal, such as Pt, to react with the Si and C in the substrate in equal ratios. We have investigated both of these contact systems in relationship to the nature of the SiC surface and its effect on the ohmic contact properties. In this study the SiC surfaces were etched for 0, 1 or 5 min. in SF_6 + Ar (1:1) prior to the deposition of the contact layers. The etch rate for these conditions is estimated to be approximately 10 nm/min. We have found a consistent decrease in the SCR values of numerous different samples as a function of surface etching time. A decrease of ~2 orders was observed for samples deposited under certain conditions. For example, samples with 1000 Å Pt/100 Å Si:B/SiC ($7.0x10^{18}$ cm^{-3} doping concentration) and annealed at 1100°C showed a decrease in SCR from $2x10^{-3}$ to $3x10^{-5}$ W cm^2 after etching. Both AFM and SEM analyses revealed that the etching process resulted in smoother SiC surfaces. AFM images of unetched substrates show that the surface consists of parallel grooves, the height of which were reduced when the substrates were etched for one or five minutes. The RMS roughness of the surfaces was found to be 1.3, 0.9 and 0.3 nm for the unetched, 1-min. and 5-min. etched substrates, respectively. These results show that the quality of the surface has a substantial effect on the ohmic contact characteristics even for contacts annealed at high temperatures and which have reacted with the semiconductor. Reactions between the contact layers and the SiC were revealed in TEM images of several samples. These results along with the surface chemistry as characterized with Auger electron spectroscopy will be presented.

11:00 AM (Student)

C4, Ohmic Contact Formation on Inductively Coupled Plasma (ICP) Etched 4H-Silicon Carbide Using Sputtered Titanium Tungsten: *Sang-Kwon Lee*[1]; Sang-Mo Koo[1]; Carl-Mikael Zetterling[1]; Mikael Ostling[1]; [1]KTH, Royal Institute of Technology, Dept. of Microelect. & Info. Tech., Electrum 229, Kista, Stockholm 16440 Sweden

Dry etching for pattern transfer is preferred as the key technique in silicon carbide device processing, since wet etching is difficult even in KOH at high temperature. Previous studies have shown that the electrical properties of SiC were changed during etching using ICP even at lower energies. In the present work, we investigated Ohmic contact formation on Inductively Coupled Plasma (ICP) etched and un-etched surfaces. Low resistivity sputtered titanium tungsten (30% Ti 70% W) was used as Ohmic contacts to highly doped n-type ($\approx 1.1x10^{19}$ cm^{-3}) 4H-SiC. After annealing at 950°C, the sputtered TiW contacts showed a good Ohmic behavior with uniform distribution of the contact resistance. We obtained a lowest specific contact resistivity (ρ_c) and sheet resistance (R_s)for un-etched TiW Ohmic contacts of $3x10^{-5}$ Ωcm^2 and 75 Ω/sq., respectively obtained from linear TLM measurements. We will discuss the Ohmic contact forma tion on ICP etched surface (600W RF Coil power, 30W and 60W platen power) with sacrificial oxidation (S/O) to remove the damage on surface and make a smooth surface. The RMS surface roughness of silicon carbide was 0.3nm, 1nm, and 0.3nm for 30W (without S/O), 60W (without S/O), 60W (with S/O) etched surface, respectively using AFM. It was found that a sacrificial oxidation prior to the metal deposition recovered the surface damages and made the surface smoother according to our AFM roughness measurement. We will also present microscopic contact resistance mapping and long-term reliability data with top-cap layers for these TiW contacts.

11:20 AM

C5, Reliability of Ti/$TaSi_2$/Pt Ohmic Contacts on 4H- and 6H-SiC After 1000 Hours in Air at 600°C: *Robert S. Okojie*[1]; Dorothy Lukco[2]; David J. Spry[3]; [1]NASA Glenn Research Center, Instrumentation & Controls/Sensors & Elect., 21000 Brookpark Rd., MS 77-1, Cleveland, OH 44135 USA; [2]AYT Research Corporation, 20001 Aerospace Parkway, OH 44142 USA; [3]Akima Corporation, Fairview Park, OH 44126 USA

Preliminary reliability of the Ti/$TaSi_2$/Pt n-type ohmic contact on 6H- and 4H-SiC is studied as a function of varying the metal thickness. In previous work[1], Auger Electron Spectroscopy (AES) and Scanning Electron Microscopy (SEM) performed on Ti(100nm)/$TaSi_2$(200nm)/Pt(300nm) that was treated in air at 600°C for 200 hours revealed potential reliability concerns that could adversely affect long-term device operation. Two failure mechanisms identified were two-dimensional contact oxidation and the diffusion of platinum into the SiC. These observations, along with a reaction kinetics model from previous work[1], and existing data[2], were utilized as a guide to improve the metallization by controlling the activity of platinum. By changing the layer structure to Ti(100nm)/$TaSi_2$(400nm)/Pt(200nm), we were able to demonstrate a stable ohmic contact after treatment in air at 600°C for 1000 hours. The measured specific contact resistivity of the contact structure to both n-type 6H-SiC (net doping level $7x10_{18}cm_{-3}$) and 4H-SiC (net doping $2x10_{19}cm_{-3}$), remained within a band of $1\text{-}5x10_{-5}$ Ωcm_2 after fifty hours of burn-in time. From the I-V characteristics, ohmic contact figure of merit (OCFM) values of $2.46x10_{-6}$ $VK_{-1}hr_{-1}$ and $2x10_{-6}VK_{-1}hr_{-1}$ for the 6H- and 4H-SiC at a current density of 1.18x103Acm_{-2} were calculated, respectively. The OCFM is a reliability figure defined as the maximum deviation of forward voltage from the minimum reference value, for a fixed maximum current density, operating temperature and duration at that temperature. In this work, relationships between platinum and tantalum disilicide thickness were observed such that reaction between them had either a positive or negative effect on the entire scheme. Excess platinum from platinum silicide formation due to the decomposition of tantalum disil icide would diffuse toward the SiC interface and disrupt the stability of the contact both electrically and mechanically. On the other hand, platinum as a limiting reactant forms a silicon-rich platinum silicide in the decomposition of tantalum disilicide, thereby preventing further platinum migration toward the SiC interface. This model was validated using four test samples having different Pt/$TaSi_2$ thickness ratios. The samples were simultaneously thermally treated at 600°C in air for several hundred hours. The surface morphology of the platinum-rich sample exhibited a non-uniform oxide growth network, and the corresponding AES depth profile after 200 hours at 600°C revealed the disruptive presence of platinum at the SiC interface. In contrast, the surface of the silicon-rich (i.e. less platinum) sample showed a smoother morphology while the AES profile clearly showed no platinum at the SiC interface even after 250 hours at 600°C in air. As a result of the optimization of th e metallization scheme, the I-V characteristics and the specific contact resistance remained practically stable after heat treatment at 600°C in air for 1000 hours. This talk will discuss prevalent reliability issues and associated failure mechanisms that appear to be unique to high temperature contact metallizations. Increased understanding of these issues should open new opportunities toward the development of more robust high temperature contacts. References: [1]Robert S. Okojie et al "Reaction Kinetics of Thermally Stable Contact Metallization on 6H-SiC," presented at the MRS Fall 2000 Meeting, Boston, MA, Nov. 27-Dec. 1, 2000; [2]ASM Handbook of Alloy Phase Diagrams, Vol. 3, p. 2(347), (1992).

11:40 AM (Student)

C6, The Role of Titanium in Ti/Al Contacts to p-Type 4H-SiC: *Brian J. Johnson*[1]; Michael A. Capano[1]; [1]Purdue University, Sch. of Electl. & Comp. Eng., 1285 Electrical Engineering Bldg., West Lafayette, IN 47907-1285 USA

In numerous SiC electronic devices, fabrication of stable, low-resistance ohmic contacts to p-type silicon carbide is a requirement if properly functioning devices are to be manufactured. Aluminum metal is the standard contact to p-type SiC, but Ti-Al alloys in recent years have seen increased application. This increased interest in Ti-Al alloys is stimulated by claims of lower specific contact resistance and improved stability of the Ti-Al contact metallization compared to Al metal. Nevertheless, no clear explanation in the literature exists regarding the role Ti plays in improving contacts to p-type SiC. Encouraging contact resistances have been reported using Ti-Al contacts formed by e-beam evaporation of a Ti-Al alloys. However, the vapor pressures for pure and Al and pure Ti are dramatically different, and there is no evidence that the as-deposited alloy composition resembles the composition of the Ti-Al source material. In this presentation, a systematic investigation of Al and Ti-Al contacts to p- type 4H-SiC is reported which exploits the interdiffusion of metals at high annealing temperatures. Experiments are designed to allow conclusions to be made about the phase equilibria and resulting contact resistivity following metal deposition and thermal processing. The p-type epilayer doping for all samples considered is 6x1018 cm-3. As a benchmark for comparison, pure Al contacts are deposited and patterned into transmission line method (TLM) structures using standard lithographic techniques. Aluminum contact samples are annealed at 700°C, 850°C, or 1000°C for 2 min in vacuum. Current-voltage (I-V) characteristics for the sample annealed at 1000°C are ohmic, and a specific contact resistance of 1.41±0.11x10-3 Ωcm2 is measured from this sample. Resistances for the samples annealed at 850°C and 700°C are approximately a factor of ten greater than for the 1000°C annealed sample. To ensure a known quantity of Ti at the SiC/metal interface, a first set of samples are prepared with Ti layers of 6 Å, 36 Å or 326 Å deposited onto SiC, followed by approximately 1600 Å of Al metal. All samples in this set are annealed at 1000°C for 2 min in vacuum. Auger depth profiles show conclusively that Ti and Al thoroughly intermix at temperatures as low as 700°C. Therefore, the layer thickness combinations above correspond to alloys of 0.2, 2, and 20 atomic percent titanium. Specific contact resistance is seen to decrease slightly with increasing Ti content. For alloy compositions of 0.2, 2, and 20 atomic percent titanium, the specific contact resistances are 1.99±0.23x10-3 Ωcm2, 1.48±0.05x10-3 Ωcm2, and 1.12±0.09x10-3 Ωcm2, respectively. Ti-Al contacts are all ohmic. A second set of samples are prepared with the same atomic concentrations of Ti (i.e. the Ti layer thicknesses are the same as in set 1), but the Ti layers lie between 800 Å thick layers of Al. The presentation relates contact resistance to fundamental thermodynamic principles and to solid-state phase transformations observed using diffraction and imaging techniques. Contact resistances of pure Al metal and Ti-Al alloys are also compared.

Session D: Materials Integration: Mismatched Epitaxy

Wednesday AM Room: 101
June 27, 2001 Location: University of Notre Dame

Session Chairs: Steven A. Ringel, Ohio State University, Dept. of Electl. Eng., Columbus, OH 43210 USA; Jerry Woodall, Yale University, Dept. of Electl. Eng., New Haven, CT 06520 USA

10:00 AM (Student)

D1, Development of Cross-Hatch Morphology in Lattice Mismatched Layers: *Aaron Maxwell Andrews*[1]; James S. Speck[1]; Alexei E. Romanov[2]; Manfred Bobeth[3]; Wolfgang Pompe[3]; [1]University of California–Santa Barbara, UCSB Matls. Dept., Santa Barbara, CA 93106-5050 USA; [2]Ioffe Institute, St. Petersburg, Russia; [3]Technical University of Dresden, Dresden, Germany

Cross-hatch morphology is a commonly observed morphological feature observed after strain relaxation for systems growing in a 2D mode. Here we demonstrate that four conditions are necessary for cross-hatch patterns to develop: (i) 2D growth; (ii) inclined slip systems to the free surface, (iii) strain relaxation; and (iv) subsequent elimination of surface steps, via lateral mass transport, produced during the strain relaxation. For films growing in a 2D mode, strain relaxation from threading dislocation motion creates surface steps and subsurface misfit dislocations. The specific cross-hatch pattern depends on the specific crystallography of the strain relaxing system. The most important example is the (001) oriented face-centered cubic (FCC) semiconductors. The {111} inclined slip planes intersect the free surface in the orthogonal <110> directions.

In the III-V semiconductors the initial relaxation is on the (111) and (-1-11) planes. Threading dislocation motion, along these slip planes, create u p-steps and down-steps on the surface. Strain relaxation alone creates a locally rough surface from the steps, but a mesoscopically smooth surface. Here, we show that the large surface undulations ('cross-hatch') are a result of lateral mass transport to eliminate the surface steps that were produced during strain relaxation. The current study focuses on modeling the cross-hatch morphology. Fully analytical solutions for stress, strain, and surface displacement for subsurface misfit dislocations were employed in this work. A Monte Carlo algorithm was used to generate the misfit dislocations and surface steps. For total surface displacement we used a linear superposition of surface displacement from misfit dislocations and the surface steps. Without lateral mass transport, the surface results in a locally rough film. Elimination of the surface steps results in locally smooth, long wavelength, large amplitude height undulations. This is the cross-hatch observed in microscopy. For experimental comparison to the model, an $In_{0.25}Ga_{0.75}As$ film was grown by molecular beam epitaxy (MBE) on a GaAs substrate to 20 times the equilibrium critical thickness (h_c). As grown, the film is 70% relaxed. The initial stress was calculated for a fully strained film with the same 1.9% mismatch and thickness. The model film was then relaxed to 70% and the final stress and surface profiles were compared. The qualitative agreement is good with respect to the amplitude of the observed undulations. However, there were quantitative discrepancies that lead to the conclusions that there is incomplete elimination of steps in the experiments and that the steps result from non-random dislocation sources. The long-term goal of this model is to use cross-hatch to learn about relaxation pathways, particularly sources of dislocations, blocking, and multiplication. This knowledge can lead to possible routes to more efficient relaxation.

10:20 AM

D2, Lattice-Mismatched Heteroepitaxy of GaInAs on InP: *S. P. Ahrenkiel*[1]; J. J. Carapella[1]; M. W. Wanlass[1]; L. M. Gedvilas[1]; R. K. Ahrenkiel[1]; [1]National Renewable Energy Laboratory, Nat'l. Ctr. for Photovoltaics, 1617 Cole Blvd., Golden, CO 80033 USA

Lattice-mismatched heteroepitaxy greatly expands the range of semiconductor material properties available for device applications. However, epitaxial layers that exceed the critical thickness for misfit dislocation formation on a given substrate often suffer from poor carrier transport, limiting device performance. Several groups have devised buffer schemes to grow thick, mismatched films with reduced dislocation densities. Compositionally step-graded alloy buffers are a prominent example, which use abrupt interfaces to inhibit dislocation propagation. We have used $InAs_yP_{1-y}$ (InAsP) step grades to grow thick (*2 µm) $Ga_xIn_{1-x}As$ ($x<0.47$) layers on InP substrates with lattice mismatch (LMM) up to 1.8%. The grades were grown using 0.3-µm-thick steps with LMM increases of 0.1% and 0.2% per step, followed by a one-µm-thick InAsP buffer. Strain relief occurs primarily by misfit dislocation arrays at the GaInAs/InAsP-buffer heterointerface, and threading dislocation densities (as determined from plan-view and cross-sectional TEM images) are typically $<10^6/cm^2$ in the GaInAs layers. Residual strain produces an increasingly three-dimensional growth front as LMM and thickness are increased, resulting in a <110> cross-hatched surface topography. Heterostructures with nominally identical GaInAs layers (LMM=1.6%) and InAsP buffers with various end-point compositions were grown to influence the dislocation density and distribution. The choice of buffer composition strongly influenced the GaInAs/InAsP-buffer heterointerface coherence and the minority-carrier lifetime in the GaInAs. We discuss high-resolution transmission-electron-diffraction investigations of these heterostructures.

10:40 AM

D3, Island and Pit Nucleation in InGaAs/GaAs Films: Nehal Chokshi[1]; Mathieu Bouville[1]; *Joanna Mirecki Millunchick*[1]; [1]University of Michigan, Dept. of Matls. Sci. & Eng., 2300 Hayward St., H. H. Dow Bldg., Rm. 2030, Ann Arbor, MI 48109 USA

3D roughening will occur in lattice mismatched films above some critical thickness. 3D islands and surface ripples have been shown to relieve strain to some degree. Theory shows that pits are even slightly more efficient at relieving strain than islands, but experimental evidence of pit nucleation has only appeared recently. This work presents a detailed study of the morphological evolution of $In_{0.25}Ga_{0.75}As$ alloy layers on (001) GaAs substrates (lattice mismatch ≅1.8%) as a function of thickness and growth conditions and shows that pit nucleation is an additional mechanism for ripple formation. A series of $In_{0.25}Ga_{0.75}As$/GaAs(001) films were grown using Molecular Beam Epitaxy to varying thicknesses and under various growth conditions in order to investigate the morphological evolution of these intermediately strained (lattice mismatch f=1.8%) layers. The intensity of the specular spot in the Reflection High Energy Electron Diffraction pattern shows that there are several regimes of growth: layer-by-layer growth, roughening, and 3D growth. The surface morphology in the layer by layer regime, as characterized by Atomic Force Microscopy, consists of flat topped mesas. Within the roughening regime, widely separated quantum dots nucleate first at the mesa edges, followed by the cooperative nucleation of both islands and pits at the beginning of the roughening regime. Pit nucleation and growth is an additional mechanism for strain relaxation by facilitating mass transfer of adatoms to growing islands. The islands and pits eventually coalesce into ripple arrays that are primarily aligned along the direction, with a secondary alignment along the <130>. This alignment, along with RHEED data, implies that the 3D features are bound by {136} facets. Computer rendering of these facets imply that they are unreconstructed, thus insensitive to growth conditions. As the films thickness increases, there is a shape transition from {136} faceted features to dome-like features. We will discuss the relative energies of the faceted surface versus the planar one in context of the critical thickness for 3D roughening.

11:00 AM (Student)

D4, Engineered SiGe/Si Substrates for Coplanar Integration of III-V Semiconductors and Strained Si Electronics with Silicon: *Arthur J. Pitera*[1]; Eugene A. Fitzgerald[1]; [1]Massachusetts Institute of Technology, Dept. of Matls. Sci. & Eng., 77 Massachusetts Ave., Rm. 13-4154, Cambridge, MA 02139 USA

Monolithic integration of III-V semiconductors and strained Si electronics with traditional Si CMOS can be achieved with SiGe compositionally graded buffers. However interconnection between device layers is hindered by thick buffer layers which can be graded across 15µm to pure Ge for integration of GaAs/Si. One solution to this limitation is to grow the SiGe films in trenches etched into Si wafers, thereby incorporating the graded buffer below the surface of the bulk substrate. In this study, the quality of relaxed SiGe graded buffers grown in trenches is investigated. The effect of the reduced lateral dimension of the trench on the threading dislocation density (TDD) relative to large area growth is also presented. In order to determine if dislocation nucleation and/or filtering at the sidewalls are important variables, two kinds of substrates were fabricated. In the first set of experiments, Si substrates were patterned with 50-200µm trenches with oxidized field and sidewalls. Etch pit density measurements of UHVCVD-grown SiGe buffers graded to $Si_{0.75}Ge_{0.25}$ at 900°C actually revealed an increase in TDD to $2.3x10^6cm^{-2}$ in 200µm features and $4.8x10^6cm^{-2}$ in 50µm features compared to $\sim5x10^5cm^{-2}$ when grown on unpatterned substrates. This result indicates active dislocation nucleation sources at the trench edges, thereby raising the total number of threading dislocations. A similar growth at 750°C partially suppressed sidewall nucleation at the expense of reduced glide kinetics, increasing the overall TDD in both blank and patterned substrates. These results are rather unsettling since such high dislocation densities cannot be tolerated for high-performance device applications. Therefore, in the second set of experiments an attempt to remove the dislocation nucleation sources was made by preparing patterned substrates without oxidation of the field or sidewalls. Growth of SiGe buffers to $Si_{0.75}Ge_{0.25}$ at 900°C resulted in a constant TDD of $\sim5x10^5cm^{-2}$, independent of feature dimensions demonstrating complete removal of dislocation nucleation sources at the sidewalls. A cursory glance of this growth also indicates a possible reduction in dislocation pile-ups. The effect of limited area graded buffer growth on pile-up formation is therefore investigated. Growth in reduced-area trenches lowers the number of intrinsic imperfections on the substrate surface that may initiate the formation of a dislocation pile-up. TEM data is presented demonstrating the dislocation structure in SiGe graded buffers grown in trenches and at trench sidewalls. AFM data is presented to compare the surface morphology of graded buffers grown in trenches compared to those grown on unpatterned wafers. A complete process for composite substrate fabrication is presented in which a final CMP planarization step is used to create areas of Si_xGe_{1-x} ($0\le x<1$) that are coplanar with the bulk Si substrate.

11:20 AM (Student)

D5, Visible LED Materials Based on Relaxed, Graded InGaP: Engineering High Performance in the Presence of Defects: *Lisa M. McGill*[1]; Eugene A. Fitzgerald[1]; Andrew Kim[2]; James Huang[2]; Sung Soo Yi[2]; Pat Grillot[2]; Steve Stockman[2]; [1]Massachusetts Institute of Technology, DMSE, 77 Massachusetts Ave., Rm. 13-5142, Cambridge, MA 02139 USA; [2]LumiLeds Lighting, San Jose, CA, USA

LED design in lattice-mismatched III-V materials systems demands the ability to produce efficient devices in the presence of defects. The InGaP/GaP system provides a unique opportunity to examine, in a systematic manner, the interaction of threading dislocation density, morphology and indium distribution within the active layer. Using atmospheric pressure OMVPE, we are able to modulate each of these factors in order to explore their individual effects and their interrelationships. We will present data on a series of quantum well structures, grown with increasing compressive mismatch on $In_{.20}Ga_{.80}P$ graded buffers of varying dislocation density. Through control of buffer grading rate, annealing, and active-layer growth temperature, we explore the effect on luminescence intensity of indium compositional fluctuation as it couples to threading dislocation density. These results may also be pertinent to the InGaN/GaN system. Blue lasers and blue and green LEDs are produced with these materials, despite high threading dislocation densities present in the device region. The cause of this insensitivity to dislocations is not well known, but it is believed that indium–and hence bandgap–fluctuations in the active layer act to trap carriers at photon-emitting recombination sites. Pursuant to the development of high-quality, graded-buffer transparent substrates for InGaP LEDs, we have also continued to probe the behavior of the "branch defect" recently identified by this group. This defect has been shown to degrade LED performance, but its origins are not well understood. We report evidence of branch defect formation in InGaP graded buffers grown by LumiLeds Lighting, using a commercially available OMVPE reactor. These samples display augmented branch defect development with increasing indium content and decreasing growth temperature. In commercial samples grown on GaP wafers that are offcut by 10° to an orthogonal {100}, branch defect strength and density trends are generally consistent with previous findings. However, in the LumiLeds samples, RMS roughness and branch defect density are decreased by 40% and threading density is decreased by at least an order of magnitude, relative to previous findings. Graded InGaP buffers were also grown in the same OMVPE run on GaP offcut 2° to (110); this leads to branch defects with a more complex internal structure than is seen in 10° offcut samples grown under similar conditions. Several possible explanations for branch defect formation have been put forward, including surface step coalescence, strain undulation and phase separation. To probe these theories, we have introduced controlled annealing steps into a series of graded InGaP buffers. Preliminary results indicate that high-temperature annealing at high final indium content promotes branch defect formation, which would support a surface-driven, kinetically limited model.

11:40 AM

D6, Lattice-Mismatched GaInP/GaInAs Devices on Ge Substrates: Bulk Lifetime, Interface Recombination, Sublattice Disorder, and Photovoltaic Efficiency: *Richard R. King*[1]; Hojun Yoon[1]; Kenneth M. Edmondson[1]; Takahiro Isshiki[1]; Moran Haddad[1]; Peter C. Colter[1]; David E. Joslin[1]; James H. Ermer[1]; Brian Keyes[2]; N. H. Karam[1]; [1]Spectrolab, Inc., 12500 Gladstone Ave., Sylmar, CA 91342 USA; [2]National Renewable Energy Laboratory, 1617 Cole Blvd., Golden, CO 80401 USA

This paper investigates minority-carrier lifetime in metamorphic GaInAs and GaInP grown lattice-mismatched to Ge substrates, and how it is influenced by dislocations, sublattice disorder, and other growth conditions. Recombination mechanisms in these materials are crucial for minority-carrier devices such as lattice-mismatched GaInP/GaInAs/Ge 3-junction solar cells, and metamorphic heterojunction bipolar transistors (HBTs). Recent improvements in lattice-matched 3-junction solar cells have resulted in record conversion efficiencies of 29.3% for space (AM0 spectrum, 0.1353 W/cm^2), and 32.4% for terrestrial concentrator cells (AM1.5D, 37.2 W/cm^2). Still higher efficiencies are predicted for metamorphic GaInP/GaInAs/Ge 3-junction cells, as a result of lowering the bandgaps of the top two subcells by the addition of In, to achieve better tuning to the solar spectrum. Double heterostructures (DHs) that reproduce the growth conditions in lattice-mismatched GaInP and GaInAs devices were grown by OMVPE, to directly measure bulk lifetimes and interface recombination velocities by time-resolved photoluminescence (TRPL). The AlGaInP/GaInP/AlGaInP and GaInP/GaInAs/GaInP DHs were imbedded in a metamorphic 3-junction solar cell structure, so that the DHs are affected by defect propagation from the composition-graded buffer in a way similar to the actual GaInP and GaInAs subcells. Bulk lifetimes of >4 ns were measured by TRPL in $Ga_{0.43}In_{0.57}P$ with 0.5% lattice-mismatch to the Ge substrate, at similar p-type doping levels as in the subcell base, and >9 ns for the $Ga_{0.92}In_{0.08}As$ base, corresponding to minority-carrier diffusion lengths L_n of >3 μm and >10 μm for the GaInP top and GaInAs middle subcells, respectively. These values are several times typical base thicknesses in 3-junction solar cells. However, the effect of dislocations on recombination is evident from the far longer lifetimes observed for lattice-matched companion samples, over 15 ns (L_n > 5 μm) for the top cell and >430 ns (L_n > 70 μm) for the middle subcell bases. The impact of bulk and interface recombination in these lattice-mismatched materials on multijunction cell efficiency and metamorphic HBT performance will be discussed in the paper. In addition, the saturation of recombination centers at the high current densities encountered in HBTs, concentrator solar cells, and DHs under high laser power excitation, will be explored. Group-III sublattice ordering can change the bandgap of GaInP by >100 meV at constant composition, and is essential to control for solar cells and HBTs. Recombination lifetimes will be presented for lattice-mismatched GaInP DHs with varying degrees of Ga and In ordering on the group-III sublattice, as directly determined by high-resolution x-ray diffraction (HRXRD) measurement of the ½{115} reflection. The highest AM0 efficiency achieved to date for 3-junction cells grown in the lattice-mismatched GaInP/GaInAs/Ge system is 27.3% using a 1.3-eV $Ga_{0.92}In_{0.08}As$ middle subcell and a 1.75-eV $Ga_{0.43}In_{0.57}P$ top cell, both grown with ~0.50% lattice mismatch to the Ge substrate. The latest metamorphic 3-junction cell efficiencies will be reported at the conference. *This work was funded in part by the Air Force Research Laboratory, Space Vehicles Directorate (AFRL/VS), and by Spectrolab, Inc.

Session E: Nanoscale Characterization

Wednesday AM Room: 155
June 27, 2001 Location: University of Notre Dame

Session Chairs: Ed Yu, University of California–San Diego, Dept. of Electl. & Comp. Eng., La Jolla, CA 92093-0407 USA; Julia Hsu, Lucent Technologies, Bell Labs., Murray Hill, NJ 07974 USA

10:00 AM (Student)

E1, Cross-Sectional Scanning Tunneling Microscopy Studies of Phase Separation in InAlAs Alloys: *B. Shin*[1]; A. Lin[1]; R. S. Goldman[1]; M. C. Hanna[2]; S. Francoeur[2]; A. G. Norman[2]; A. Mascarenhas[2]; [1]University of Michigan, Matls. Sci. & Eng., 2300 Hayward St., Ann Arbor, MI 48109-2136 USA; [2]National Renewable Energy Laboratory, 1617 Cole Blvd., Golden, CO 80401-3393 USA

In recent years, compound semiconductor alloys have been incorporated into a range of electronic and optoelectronic devices. In most of these systems, growth conditions have been reported for which phase separation occurs. Yet, the thermodynamic versus kinetic origin of phase separation, as well as the experimental conditions for determining the presence of phase separation has been the subject of debate for nearly twenty years[1,2]. In thin films of compound semiconductor alloys, both the difference in binary bond lengths and the film/substrate misfit are expected to play a significant role in the initiation of alloy phase separation. In this work, we have examined phase separation in the misfit-free InAlAs/InP system, using ultra-high vacuum cross-sectional scanning tunneling microscopy (XSTM). The structures were synthesized using metallorganic chemical vapor deposition. For p-doped InAlAs layers grown at 620°C, XSTM images show the presence of non-uniformities in the InAlAs. These non-uniformities are essentially isotropic, consisting of clusters with typical diameters of ~ 2nm and separations ranging from

5 to 10nm. For unintentionally doped InAlAs layers grown at 500°C, longer wavelength quasi-periodic modulations perpendicular to the growth direction are apparent. These lateral modulations are apparent in both topographic and conductance XSTM images, suggesting that they are due to a combination of compositional and strain variations. Interestingly, the average modulation wavelength increases from 10 to 20nm, as the film thickness is increased from 5 to 25nm. For thicknesses beyond 25nm, the average modulation wavelength does not increase further, suggesting that a saturation value has been attained. These modulation wavelengths are notably lower than those reported for similar films grown at higher temperatures[3]. Together, these results suggest that phase separation in the misfit-free InAlAs/InP system is a thermally activated kinetic process which may be significantly affected by the presence of impurities such as dopants. [1]G. B. Stringfellow, J. Cryst. Growth 65, 454 (1983); [2]A. Zunger and S. Mahajan, in Handbook on Semiconductors (North-Holland, Amsterdam, 1994), Vol. 3, p.1399; [3]H. K. Cho, J. Y. Lee, M. S. Kwon, B. Lee, J.-H. Baek, and W. S. Han, Mat. Sci. Eng. B 64, 174 (1999).

10:20 AM (Student)

E2, Atomic Force Microscope I-V Measurements of Polycarbonate Membrane Template-Synthesized Nanowires: *Lili Jia*[1]; Jonathan A. Nichols[1]; Jeremiah K. N. Mbindyo[2]; Thomas E. Mallouk[2]; Thomas N. Jackson[1]; [1]Pennsylvania State University, Electl. Eng., 121 Electrical Engineering E., University Park, PA 16802 USA; [2]Pennsylvania State University, Chem., 152 Davey Lab., University Park, PA 16802 USA

Metallic nanowires, with or without embedded molecular or semiconductor regions, are of interested as building blocks for self-assembled electronic systems[1]. Such systems may ultimately use colloidal crystallization other large-scale self-assembly, however, testing of individual device elements is also important. We have demonstrated that electric-field assisted fluidic assembly can be used to separate and position single nanowires[2]. but a more rapid characterization approach is also useful. Since our metallic nanowires are often fabricated by template-synthesis in track-etched polycarbonate membranes, testing nanowires and nanowire devices before release from the membrane is convenient. To allow individual nanowires to be tested we use an atomic force microscope (AFM) based approach. Nanowire filled membranes are mounted to a convenient substrate that also provides one connection to the nanowires. The membrane is then etched in an oxygen plasma until the tips of the nanowires are exposed. The AFM is then used to image the membrane with exposed nanowire tips. Our nanowires are typically 10-100 nm in diameter so at the smaller dimensions the AFM provides little information about the nanowire detail topography. However, the nanowire position is easily found and by using a conductive-tip AFM cantilever it is then possible to contact individual nanowires for testing. We will describe measurements made using this technique on 70 nm diameter nanowires with and without embedded molecular layers. [1]B. R. Martin, D. J. Dermody, B. D. Reiss, M. Fang, L. A. Lyon, M. J. Natan, and T. E. Mallouk, "Orthogonal Self-Assembly on Colloidal Cold-Platinum Nanorods", Adv. Mater., 11, pp. 1021-1025 (1999); [2]P. A. Smith, C. D. Nordquist, T. N. Jackson, T. S. Mayer, B. R. Martin, J. Mbindyo, and T. E. Mallouk, "Electric-Field Assisted Assembly and Alignment of Metallic Nanowires", Appl. Phys. Lett., 77, pp. 1399-1401 (2000).

10:40 AM (Student)

E3, Potential Imaging of Pentacene Organic Thin Film Transistors: *Jonathan A. Nichols*[1]; David G. Gundlach[1]; Thomas N. Jackson[1]; [1]Pennsylvania State University, Dept. of Electl. Eng., 121 Electrical Engineering E., University Park, PA 16802 USA

Electrostatic force microscopy (EFM) has been used to simultaneously obtain high resolution topographical and potential images of pentacene organic thin film transistors (OTFTs) during device operation. Pentacene has been used to fabricate thin film transistors with performance comparable to devices using hydrogenated amorphous silicon; such devices are of interest for use in displays and other broad area electronic applications. For this work, bottom contact OTFTs were fabricated by depositing 50 nm of pentacene onto heavily-doped, thermally oxidized, single-crystal silicon substrates (T_{sub}=60°C) with pre-patterned metal source and drain contacts. Topographical and potential images were obtained using non-contact mode atomic force microscopy. During imaging, drain-to-source and gate-to-source potentials for useful device operation were applied (typically volts to tens of volts). The relatively large bias potentials, macroscopically inhomogeneous device structure, and the long-range nature of electrostatic forces make EFM imaging of biased devices difficult. In particular, with typical device structures the large contribution to the electrostatic force from the cantilever (due to potential differences between the cantilever and device contact pads, for example) makes it difficult to make quantitative measurements and reduces resolution during surface potential imaging. To allow useful EFM imaging on these devices a special device layout with surrounding field plate biased at the cantilever potential was used; this allows much of the force contribution from the cantilever to be eliminated. EFM images of OTFTs obtained with this technique show potential drops at source and drain contacts with magnitude dependent on contact metallurgy and/or treatment and relatively small potential drops at grain boundaries in polycrystalline pentacene films.

11:00 AM (Student)

E4, Effect of Cantilever on Electrostatic Potentials Measured by Scanning Kelvin Probe Microscopy: *Hemant R. Bhangale*[1]; Goutam Koley[2]; Michael G. Spencer[2]; [1]Cornell University, Appl. & Eng. Phys., Ithaca, NY 14853 USA; [2]Cornell University, Electl. & Comp. Eng., Ithaca, NY 14853 USA

Scanning Kelvin probe microscope (SKPM) has become exceedingly important method to measure surface electrostatic potential because of its high resolution potential mapping capabilities which are especially useful in study of working nano-scale integrated circuit devices and other applications. Good qualitative images can be obtained using SKPM. However, it is difficult to measure exact quantitative value of potential due to various factors. SKPM probe tip is typically attached to a relatively large conducting cantilever and it is observed that electrostatic force on the cantilever can significantly affect measured electrostatic potential. The effect of cantilever on the measurement of electrostatic potentials by SKPM operated in feedback mode is modeled. The electrostatic force between a vibrating tip and surface with electric potential is proportional to the capacitance gradient associated with sample and probe tip. The accuracy of measurement of electrostatic potentials on closely spaced and differently biased regions is reduced due to the large capacitance gradient associated with the cantilever. The tip is modeled as a truncated conical structure with hemispherical end. The cantilever-sample capacitor is modeled as inclined plates capacitor since the cantilever holding the tip is slanted at an angle $\phi = 15°$ with respect to the sample surface. The sample consists of interlaced fingers alternately coming out from the same metal pad. The width of the fingers as well as the spacing between them is 1.7 μm. The metal pads were biased to 0 and 5 V so that alternate fingers have same biases. It is assumed that the electrostatic potential measured by tip is equal to the electrostatic potential of the finger directly below it while the cantilever is assumed to measure averaged potential of 2.5V since its area covers large number of fingers with alternating 0 V and 5V bias. It is observed that the accuracy of measurements increase with decrease in tip-sample distance as the capacitance gradient of the tip dominates that of the cantilever. It is further observed that longer tips and tips with smaller area of cantilevers electrostatic potentials more accurately as the capacitance gradient of the cantilever is reduced. For a typical operating distance of about 10-100nm, however, tip and cantilever have comparable contributions to the observed electrostatic potential. Hence, it is essential to separate the two components by using appropriate model to get accurate electrostatic potential mapping of sample surface. It can be seen that the model presented shows a good match between calculated and observed data. However, it should be noted that this simple model neglects interaction between tip and neighboring fingers, fine geometric factor such as non-spherical end of tip and deviation of cone angle along height of the tip. The authors would like to acknowledge Dr. Oliver Ambacher for providing us with the test structure. This work is supported by the Office of Naval Research MURI on Polarization Electronics contract no. N00014-96-1-1179, under the direction of Dr. Colin E. C. Wood.

11:20 AM (Student)

E5, Experimental and Modeling Studies of Schottky Contacts to Low-Temperature-Grown GaAs in Ex-Situ Structures: *Saurabh Lodha*[1]; David B. Janes[1]; Steve Howell[2]; Marcus V. Batistuta[1]; E. H. Chen[3]; R. Reifenberger[2]; [1]Purdue University, Elect. & Comp. Eng., West Lafayette, IN 47907 USA; [2]Purdue University, Dept. of Phys., West Lafayette, IN 47907 USA; [3]Yale University, Dept. of Electl. Eng., USA

Stoichiometric n-GaAs oxidizes rapidly when exposed to ambient conditions. Control of the surface Fermi level is essential for realization of

nanoscale devices and associated contact structures. Low temperature grown GaAs (LTG:GaAs) oxidizes more slowly, over a time constant of hours[1]. Ex-situ nonalloyed contacts using LTG:GaAs surface layers have been realized at micron[2] and nanometer[3] scales, with specific contact resistances close to 1e-7 Ohm-cm^2. In contrast to samples that were subjected to prolonged air exposure thereby indicating midgap Fermi level pinning[4], samples considered in studies 1-3 were exposed for relatively brief times (20-60 minutes) following either removal from the growth chamber or an oxide strip preceding metallization. Modeling of the contact performance[5] indicates a low barrier height due to an unpinned surface Fermi level following brief air exposure. To verify this behavior, it is important to look at Schottky barrier heights considering the electrical behavior of the LTG:GaAs layer and for different metal work-functions. The present study addresses these issues and provides direct evidence that the surface Fermi level is unpinned. We have experimentally studied the surface electrical behavior of LTG:GaAs surfaces using: i) the measured Schottky barrier height of metal-semiconductor diodes analyzed using device simulations and a physically-based model, ii) the measured barrier height as a function of metal work-function for two different metal systems. The samples consisted of 3.5 nm thick undoped and Be-doped LTG:GaAs on n:GaAs layers, both grown by MBE on GaAs(100) substrates. Metal contacts were fabricated using conventional photolithography and high vacuum e-beam evaporation. High frequency capacitance-voltage measurements for Au/Ti and Au/Ti/Ni contacts indicate that the barrier height for Ni contacts is higher than for Ti contacts by 0.3 eV for undoped layer and 0.4 eV for Be-doped layer indicating that the surface Fermi level is not strongly pinned. An effective depletion capacitance, computed by including the charge due to midgap states in the LTG layer produces an excellent fit with measured data for the Au/Ti and Au/Ti/Ni-undoped LTG:GaAs contacts indicating barrier heights of 0.41 eV and 0.60 eV respectively instead of the conventional extrapolated barrier heights of 0.63 eV and 0.88 eV respectively. As air exposure preceding metallization is increased from 10 minutes to 24 hours, the barrier height for both layers increases by just 0.07 V indicating a slow oxidation rate. Low values of barrier heights, which can be controlled by changing the metal work-function, indicate that the surface Fermi level for LTG:GaAs layers is unpinned. [1]T.B. Ng, et al. Appl. Phys. Lett. 69, 3551 (1996); [2]M.P. Patkar, et al. Appl. Phys. Lett. 66, 1412 (1995); [3]T.Lee, et al. Appl. Phys. Lett. 76, 212 (2000); [4]Holden, et al. Phys. Rev. B, 7795 (1998); [5]N.P. Chen, et al. J. Appl. Phys. 88, 309 (2000).

11:40 AM (Student)

E6, Properties of Surface States on Clean and Si-Deposited GaAs(001)-c(4x4) Surfaces Studied by Scanning Tunneling Microscopy and Spectroscopy: *Noboru Negoro*[1]; Hideki Hasegawa[1]; [1]Hokkaido University, Rsrch. Ctr. for Interface Quantum Elect. & Grad. Sch. of Elect. & Inform. Eng., N13, W8, Sapporo 060-8628 Japan

The origin and properties of the surface states as well as the microscopic mechanism of Fermi level pinning are not well understood even on the most studied and technologically most important GaAs (001) clean surface. Following our recent STM/STS study on the GaAs (001)-(2x4) surface[1], the present paper investigates microscopic topological and spectroscopic properties of the MBE-grown clean GaAs (001)-c(4x4) surface by using the UHV STM/STS technique. The effects of depositing a mono-layer level Si on this surface were also studied. All the experiments were carried out in a UHV-based multi-chamber system containing an MBE chamber, UHV STM/STS chamber (JEOL JSTM-4600) and an XPS chamber. Si-doped GaAs was grown by MBE. c(4x4) reconstructed surfaces were obtained by controlling As pressure and substrate temperature. Deposition of Si was done by MBE at 300°C on the c(4x4) surface. After surface preparation, the sample was transferred into STM chamber, and the STM/STS measurements were performed. The filled state STM image taken on the clean c(4x4) surface resolved each of unit cells clearly with nearly the same image intensity. Contrary to this, dark and light cells occurred randomly on the empty state image. As the positive sample bias was gradually decreased, the area of the dark region consisting of dark cells gradually increased, unit cell by unit cell. STS measurements on the dark region have revealed that the STS spectrum of the dark cell gives a conductance gap larger than the band gap energy of GaAs. The darker the cell, the larger the conductance gap. Thus, spots with normal and anomalously large STS conductance gaps coexisted on the same sample surface in contrast to the (2x4) surface where all most all the spots showed anomalously large conductance gaps. In accordance with the previous work on (2x4) surface[2], the observed conductance anomaly was explained by local charging of surface pinning states by single or a few electrons supplied to or from the STM tip. This led to a construction a map of surface states both in energy and space. It showed clearly that the surface states are not point defects, but they are continuously distributed in energy and space. Dramatic reduction of dark spots with anomalous conductance took place by deposition of one mono-layer Si. The observed conductance gap was that of GaAs, and not that of the strained Si, as expected. The result is consistent with our previous macroscopic PL, XPS and C-V study that the Si-interlayer-based surface passivation is much more effective on the c(4x4) surface than on (2x4) surface[2]. [1]H. Hasegawa et al: J. Vac. Sci. Technol. B18 (2000) 2100; [2]M. Mutoh et al: Jpn. J. Appl. Phys. 38 (1999) 2538.

Session F: Advanced Gate Dielectrics – I

Wednesday AM Room: 138
June 27, 2001 Location: University of Notre Dame

Session Chairs: Laura Mirkarimi, Agilent Laboratories, Palo Alto, CA 94304 USA; Bruce Wessels, Northwestern University, Dept. of Matls. Sci. & Eng., Evanston, IL 60208 USA

10:00 AM Invited

F1, Functionality of Epitaxial Ferroelectric Heterostructures and Possibilities for Integration with Silicon: *Charles Ahn*[1]; [1]Yale University, Dept. of Appl. Phys., Becton Ctr., 15 Prospect St., PO Box 208284, New Haven, CT 06520-8284 USA

Complex oxides exhibit a tremendous diversity of behavior, including magnetism, superconductivity, ferroelectricity, and piezoelectricity. The ability to integrate this functionality with mainstream Si technology opens broad possibilities for science and technology. In this talk, we consider some of the unique opportunities offered by epitaxial complex oxides and discuss possibilities for their integration with silicon. We will consider the methodology of crystalline oxides on silicon (COS) and discuss the results of the growth of epitaxial ferroelectrics and piezoelectrics on SrTi03-terminated Si. Evaluation of the piezoelectric properties of these films for microelectromechanical (MEMS) applications will be discussed.

10:40 AM (Student)

F2, In-Plane Anisotropic Dielectric Properties of Epitaxial Barium Titanate Thin Films: *Brent H. Hoerman*[1]; *David J. Towner*[1]; Bruce W. Wessels[1]; [1]Northwestern University, Dept. of Matls. Sci., 2225 N. Campus Dr., Evanston, IL 60208 USA

Epitaxial BaTiO3 thin films are of interest for integrated silicon devices because of their high dielectric constants. The dielectric properties of the thin films depend strongly on the orientation as well as the ferroelectric domain structure. In this study the in-plane dielectric properties including the dielectric constant, loss and tunability of epitaxial BaTiO3 thin films are shown to be highly anisotropic. For dielectric property measurements a-axis oriented BaTiO3 films were used. Films, 10-50nm thick, were deposited on (001) MgO substrates using low-pressure metal-organic chemical vapor deposition. Dielectric constants and loss tangents were calculated from the measured impedance of coplanar surface electrodes. The dependence of the dielectric constant on electric field direction was studied. A monotonic increase in the dielectric constant was observed as the electric field was rotated from the <100> direction towards the <110> direction. The dielectric constant along the <100> was 610 while that along the <110> was 1500. Furthermore, increases in the loss tangent (0.022 to 0.066), bias field tunability (22% to 37%), and the dependence of the dielectric constant on the applied AC driving signal level (Rayleigh constant) were also observed as the applied electric field rotated from the <100> towards the <110> direction. The observed in-plane anisotropy has been attributed to the presence of a multivariant

domain structure of the BaTiO3 films, in particular to the presence of an easy in-plane poling direction. Potential mechanisms responsible for the easy poling axis will be discussed.

11:00 AM (Student)

F3, Studies of Liquid Source Misted Chemical Deposited Strontium Tantalate ($SrTa_2O_6$) as MOS Gate Oxide: *Dong-Oh Lee*[1]; Paul Roman[1]; Chun-Tai Wu[1]; Bill Mahoney[2]; Mark Horn[2]; Paul Mumbauer[3]; Matthew Brubaker[3]; Robert Grant[3]; Jerzy Ruzyllo[1]; [1]The Pennsylvania State University, Electl. Eng., 121 Electrical Engineering E., University Park, PA 16802 USA; [2]The Pennsylvania State University, Nanofabrication Lab., University Park, PA 16802 USA; [3]Primaxx, Inc., 7377 William Ave., Allentown, PA 18106 USA

Extensive research of high-k materials to ensure continuous scaling of gate dielectrics below 20Å for advanced CMOS technologies is currently underway. The material of choice should have a dielectric constant higher than 15 with low leakage currents in the range of film thickness of interest, should be thermodynamically stable with Si and should maintain its structural integrity during post-deposition annealing cycles. Considerable attention has been paid to hafnium and zirconium oxides (HfO_2 and ZrO_2) and their silicates ($HfSi_xO_y$ and $ZrSi_xO_y$) and ultra high-k materials ($SrTiO_3$, $SrTa_2O_6$). In this report we study electrical and material characteristics of $SrTa_2O_6$ deposited on Si using the Liquid Source Misted Chemical Deposition (LSMCD) method. The LSMCD technique employs liquid metal-organic precursors as a source and deposits a controlled amount of liquid metal oxides in the form of sub-micron mist droplets onto the wafer surface at room temperature and atmospheric pressure. The process is carried out in nitrogen, and a high-voltage electrostatic field is used to control the deposition rate. In this investigation, the deposition runs were carried out in a commercial cluster consisting of a gas-phase surface conditioning module (including anhydrous HF:methanol, UV Cl_2, UV O_2 and UV NO nitridation capabilities), a LSMCD module, and a Rapid Thermal Processing (RTP) module in which wafers are annealed after deposition at temperatures not exceeding 700°C. P-type, (100) Si wafers 150 mm and 200 mm in diameter with varied resistivity were used as substrates. MOS capacitors with Pt/Ti electrodes were fabricated for electrical characterization. Prior to deposition Si surfaces were either HF-treated ex situ, or subjected to gas-phase surface conditioning in the cluster. The promising results, EOT (Equivalent Oxide Thickness) <1.4 nm, and Jg in the mA/cm^2 range were obtained with $SrTa_2O_6$ thinner than 10nm. AFM characterization revealed smooth surfaces of the $SrTa_2O_6$ films in the 0.3nm RMS range of surface roughness. To investigate the structural integrity of the $SrTa_2O_6$ films during post deposition annealing, 10nm thick $SrTa_2O_6$ films were subjected to a 1000°C rapid thermal anneal for 1 min. The C-V and J-V characteristics showed only a minor departure from the characteristics of the as-deposited films. This material deposited in the form of an ultra-thin amorphous film is expected to have a k value in the range of 15-20 and possibly much higher depending on the optimization of the film composition. It has also the potential for displaying sufficient thermodynamical stability with Si. In the full account of this work other aspects of misted deposition of $SrTa_2O_6$ for MOS gates, including depth profiles, and the effects of post metallization annealing and Si surface conditioning prior to high-k dielectric deposition are discussed.

11:20 AM (Student)

F4, Platinum and Iridium High Temperature Etching Characteristics: *Stefan Schneider*[1]; H. Kohlstedt[1]; R. Waser[1]; [1]Forschungszentrum Juelich, IFF, EKM, Juelich 52425 Germany

A reactive etch process to pattern noble metal electrodes like Platinum or Iridium are necessary for high density ferroelectric non-volatile memory devices. Conventional, sputter driven etch processes either yield in redeposition problems (fences) or in a severe sloping (CD loss) and are not acceptable for high density integration architectures. To systematically investigate possible reactive etch process regions, characterized by volatile etch products, we used a reactive ion beam etching (RIBE) tool with a filament free ICP source, that gives us exact control over the beam energy and the current density, and allows to use reactive gases. An energy dispersive quadrupole mass spectrometer is fitted to the chamber for in situ process monitoring. The wafer temperature can be controlled from ambient temperature up to 300°C. We study the influence of the ion energy and the ion current impinging on the wafer surface as well as it's angular dependence. Chlorinated as well as fluorinated process chemistries together with several additives are investigated and characterized in terms of their role to increase the etch rate, to maintain a vertical profile, or to enhance the process selectivity. Although the main focus of the study is on platinum, we also compare it's etch characteristics with those of Iridium. Blanket films were used to understand the etch behavior of the material by measuring the etch rates and by analyzing the surface (e.g. with XPS). Hardmask patterned wafers were used to study the influence of the process on the sidewall angle and the selectivity. Low temperature process results are compared with the more efficient high temperature process regimes.

11:40 AM (Student)

F5, The Thickness Dependent Gate Oxide Integrity Degradation by Cu Contamination: *Yih Hsia Lin*[1]; Y. C. Chen[2]; *F. M. Pan*[3]; *I. J. Hsieh*[2]; *Albert Chin*[1]; [1]National Chiao Tung University, Dept. of Electl. Eng., Mailbox 7, Hsinchu, Taiwan 300 China; [2]Chung Hua University, Dept. of Electl. Eng., Hsinchu, Taiwan 300 China; [3]National Nano-Device Laboratory, Hsinchu, Taiwan 300 China

It is reported recently that gate oxide integrity degradation by Cu contamination can only be found at very high Cu concentrations[1] and Cu contamination effect may be over-emphasized in VLSI. In this work, we have studied the oxide thickness dependent Cu contamination effect. Cu was introduced after front-end MOS device fabrication and annealed at 400°C for 1hr that is similar to VLSI back-end process. We also did not observe any Cu contamination related degradation on F-N tunneling current, oxide charge density, or breakdown electric field for 5nm thermal oxide contaminated by 10 ppm Cu. Instead, only weak effects of higher pre-F-N tunneling current and increased interface trap density are found. Near one order of magnitude higher pre-F-N tunneling current is found only at high 10ppm Cu contamination and increased interface trap density from non-contaminated 3E10 eV-1/cm2 to a saturated 2E11 eV-1/cm2 as Cu contamination level above 10 ppb. The additional leakage current suggests Cu behave like neutral traps inside oxide that is similar to stress-induced leakage current generated defects within oxide. In sharp contrast, strong degraded oxide integrity is found in 3nm oxide currently used for 0.18µm technology node, even at low Cu contamination level of 10ppb. More than an order of magnitude higher direct tunneling current, 2MV/cm lower breakdown electric field, poorer charge-to-breakdown and wide distribution, and worse stress-induced leakage current are found simultaneously. From theoretical J-V analysis, the strong oxide integrity degradation of ultra-thin 3nm oxide can be explained by the near 1 eV tunneling barrier lowering from interface assisted tunneling. This is further evidenced from the SIMS profile where Cu is accumulated at both poly-Si-oxide and oxide-Si interfaces. The large difference between Cu contaminated 5nm and 3nm oxides is due to stronger Cu penetration throughout oxide and accumulating at Si-oxide interface at thinner 3nm oxide. In contrast to previous reports of weak Cu contamination effect in relative thick oxide, the severe oxide integrity degradation in thinner oxide should be attracted much more attention for continuously scaling down VLSI technology below 0.18µm generation. [1]M. Inohara, H. Sakurai, T. Yamaguchi, H. Tomita, T. Iijima, H. Oyamatsu, T. Nakayama, H. Yoshimura, and Y. Toyoshima, Symp. On VLSI Tech., p. 26, (2000).

Session G: IR Quantum Devices and Materials

Wednesday PM Room: 129
June 27, 2001 Location: University of Notre Dame

Session Chairs: Andrew Johnson, DERA, Great Malvern WR14 3PS UK; Robert M. Biefeld, Sandia National Laboratories, Albuquerque, NM 87185-0601 USA

1:20 PM

G1, Long Wavelength Infrared Negative Luminescence from MCT Diodes: *Tim Ashley*[1]; Neil T. Gordon[1]; Chris L. Jones[2]; Chris D. Maxey[2]; Geoff R. Nash[1]; [1]DERA, St. Andrews Rd., Malvern, Worcestershire WR14 3PS UK; [2]BAE Systems Infrared, Ltd., Southampton SO15 0EG UK

The phenomenon of negative luminescence is attracting an increasing

amount of interest for a variety of applications, including as a 'source' of IR radiation for gas sensing; radiation shielding for and nonuniformity correction of high sensitivity staring infrared detectors; and dynamic infrared scene projection. Negative luminescence in the mid-waveband has recently been demonstrated convincingly by several groups, using both III-V and II-VI materials, however comparable long wavelength infrared components have not been available. In this paper we present data on mercury cadmium telluride (MCT) devices operating to 10 microns wavelength. The devices are grown by metal organic vapour phase epitaxy (MOVPE) onto GaAs substrates. They are fully doped, multilayer heterostructure diodes, employing separate control of doping and composition profiles to minimise the thermally generated leakage current. Initial devices have been grown on semi-insulating GaAs and comprise groups of individual diodes which are addressed in small units to form an overall device 1mm in diameter. Excellent agreement between theoretical and experimental spectral characteristics have been achieved, and quantitative measurements of the negative luminescent power indicate a very high quantum efficiency (proportion of the background radiation absorbed), limited principally by the absence of an anti-reflection coating. An increase in the electrical efficiency (modulated photons per Amp) of more than a factor of 100 has been observed under the reverse biased, negative luminescent mode compared with conventional, forward biased positive luminescence owing to suppression of the competing non-radiative Auger mechanisms following extraction of the majority of the electrons and holes from the active region of the diode. This makes a cheap and relatively efficient source of long wavelength IR radiation available for the first time. The prospects for improved efficiency through the use of integrated optical concentrators to couple a larger proportion of the internal radiation to the surroundings, as has been demonstrated for mid-IR InSb based devices, will be examined. This technique offers the potential for an order of magnitude increase in efficiency. The optical concentrators extend through the epitaxially grown material into the substrate, so these devices are grown on n-type conducting GaAs, in order that the substrate may be utilised to carry the current. The issues associated with achieving high quality growth of MCT onto such substrates, whilst maintaining a low resistance at the interface, necessary for efficient operation, will be discussed. Large area, long wavelength components thus look feasible, but do present challenges in their electrical operation owing to the large negative resistance as a consequence of Auger suppression. Techniques to accommodate this artefact will be discussed.

1:40 PM (Student)

G2, GaInSb Quantum Well Lasers Grown on AlInSb Metamorphic Buffer Layers: *Edwin Pease*[1]; L. Ralph Dawson[1]; Leslie G. Vaughn[1]; Luke F. Lester[1]; [1]University of New Mexico, Ctr. for High Tech. Matls., 1313 Goddard S.E., Albuquerque, NM 87106 USA

There is a growing need for antimonide-based, room temperature, mid-IR semiconductor lasers for atmospheric transmission with applications in chemical sensing, heat sensing, communications, and radar. High power, low threshold lasers using InGaAsSb quantum wells with emission wavelength of 2 µm have been demonstrated. However, to extend the wavelength beyond 2 µm increased As content has been needed to simultaneously alter the bandgap and maintain a lattice match to the GaSb substrate. However, increased As results in decreased valence band offset between quantum wells and barriers, and a corresponding decrease in performance. In this work the need for lattice match between the active region and the GaSb substrate is avoided by the use of intervening AlInSb digital alloy (DA) buffer layers, which provide a low defect density substrate hiving a lattice constant of the required value for the structure of interest and eliminating the absolute need for As in the structure. Using such buffer layers, we report optically pumped $Ga_{1-x}In_xSb$ quantum well lasers with x as large as 0.5, and emission wavelength as large as 2.7 µm at room temperature. The DA buffer structure is grown by solid source MBE and consists of alternating layers of $Al_{1-y}In_ySb$ and $Al_{1-z}In_zSb$, whose y, z, and thickness ratio are chosen to provide the desired average In content. After the growth of a suitable number of periods of such material, usually corresponding to a total thickness of 500 nm, the thickness ratio is changed to increase the average In content, usually in steps of 9%. The resulting buffer structure consists of a series of regions with In content of 0, .09, .18., .27, .36, each of which consists of thin layers of two different compositions of AlInSb. Advantages of this technique include not only the convenience of controlling the In content by adjusting shuttering times but providing strain concentration at the many interfaces within the structure. The latter feature is instrumental in filtering threading dislocations to provide material whose dislocation density is essentially zero as measured by cross sectional TEM. We report one laser structure with a DA buffer terminating with Al.731n.27Sb, using AlGaInSb barriers and Ga.61n.4Sb quantum wells, which gives both photoluminescence and intense laser emission (under optical pumping) at 2.5 µm at room temperature. A second laser structure with a DA buffer terminating with $Al_{.64}1n_{.36}Sb$, with AIGaInSb barriers and $Ga_{.5}1n_{.5}Sb$ quantum wells, gives both PL and intense laser emission at 2.7 µm at room temperature. In both cases the buffer layer served as the lower cladding layer and a lattice matched AlInSb layer was grown as the top cladding layer. Work is in progress to extend the In content in the buffer layers and the quantum wells to provide emission at wavelengths beyond 3 µm.

2:00 PM

G3, Linewidth of Terahertz Intersubband Plasmons in Quantum Wells: *Carsten A. Ullrich*[1]; Giovanni Vignale[2]; Michael E. Flatte[3]; [1]iQUEST, University of California, Santa Barbara, CA 93106 USA; [2]University of Missouri, Dept. of Phys., Columbia, MO 65211 USA; [3]University of Iowa, Dept. of Phys., Iowa City, IA 52242 USA

In semiconductor quantum wells, the conduction band splits up into several subbands, and electrons (supplied e.g. by remote doping) can perform collective transitions between them. These so-called intersubband plasmons are of great experimental and theoretical interest, being the basis of new devices operating at terahertz frequencies. To achieve better frequency resolution and larger peak absorption in detectors, and higher gain in lasers, it is desirable that the plasmons have a narrow linewidth. In the absence of electron-phonon scattering (for wide quantum wells at low temperature), the linewidth is caused by a complicated interplay of a variety of different damping mechanisms: intrinsic (electron-electron scattering) as well as extrinsic ones (impurity, alloy-disorder and interface roughness scattering). We present a quantitatively accurate theory [C.A. Ullrich and G. Vignale, submitted to Phys. Rev. Lett.] that treats both damping mechanisms from first principles and on equal footing. Intersubband plasmons are described using self-consistent linear response theory within a one-band effective-mass approximation. All damping effects are contained in the response function $\chi(r,r',\omega)$, which is obtained combining time-dependent density-functional theory [C.A. Ullrich and G. Vignale, Phys. Rev. B 58, 15756 (1998)] (which includes purely electronic damping but neglects impurities and disorder) with the memory function formalism [A. Gold and W. Gotze, Phys. Rev. B 33, 2496 (1988)] (which describes impurity and disorder scattering, but ignores electronic damping). Our theory explains recent experiment data [J.B. Williams, M.S. Sherwin, K.D. Maranowski, A.C. Gossard, submitted to Phys. Rev. Lett.] on the linewidth of intersubband plasmons in an n-type modulation doped 40-nm GaAs/AlGaAs quantum well. Two experimental parameters were independently controlled: the electronic sheet density (0.05-1.3*10^{11} cm^{-2}) and a DC field across the sample. The latter tends to push the electrons against one of the edges of the well, which provides an ideal tool to distinguish interface roughness from other damping effects. Our calculations show that at low temperatures and below the LO phonon energy, interface roughness is the dominating damping mechanism for intersubband plasmons, especially for applied DC fields, as compared to impurities (which, on the other hand, dominate the mobility). However, damping due to electron-electron scattering makes a significant contribution and provides an intrinsic lower limit of up to 0.1-0.2 meV for the linewidth. We will also briefly comment on extensions of the theory to include effects of non-parabolicity of the subbands. This work was supported by NSF grants DMR9706788, DMR0074959 and ECS0000556.

2:20 PM (Student)

G4, InAs Quantum Dot Lasers Grown on AlGaAsSb Metamorphic Buffers on GaAs Substrate: *Y.-C. Xin*[1]; L. G. Vaughn[1]; L. R. Dawson[1]; A. Stintz[1]; Y. Lin[1]; L. F. Lester[1]; [1]University of New Mexico, Ctr. for High Tech. Matls., 1313 Goddard S.E., Albuquerque, NM 87106 USA

Quantum dots (QDs) lasers have recently attracted considerable attention due to their superior lasing characteristics compared to conventional quantum well (QW) lasers, including low-threshold current density and a small linewidth enhancement factor[1, 2]. QD lasers grown on a GaAs substrate are currently a subject of strong interest with 1.3-µm emission from $In_xGa_{1-x}As$ QDs having been reported by various groups[3-5]. However, lasing beyond 1.3 µm in InAs QDs on GaAs has been very difficult to

realize. To extend the emission wavelength of InAs QDs on GaAs, we have fabricated the first 1.27-1.34 μm InAs QD lasers (emitting in the excited state) grown on AlGaAsSb metamorphic buffer layers by MBE. A threshold current density as low as 258 A/cM^2 under pulsed conditions has been achieved. Ground state emission occurs at 1.44 μm as determined by electroluminescence. Since the lattice mismatch is the driving force for the formation of compressively strained InAs QDs, reducing the mismatch leads to a greater thickness of the initial 2D layer that grows before strain energy accumulates to the critical level and dots form. As the QDs continue to enlarge, part or all of the initial planar layer is consumed, leading to larger dots. In addition, the strain within the dots is lower due to the decreased mismatch. Both of these effects will lead to longer emission wavelength. To reduce the lattice mismatch between the InAs dots and their surrounding material, we provided a growth platform with lattice constant significantly greater than that of GaAs by using an AlGaAsSb metamorphic buffer on a GaAs substrate. The buffer design for the laser diode consists of 8 layers of $Al_{0.5}Ga_{0.5}As_xSb_{1-x}$, whose Sb composition is graded from 0 to 24%. The final I -μm thick buffer layer of n-$Al_{0.5}Ga_{0.5}As_{0.76}Sb_{0.24}$ is almost totally relaxed as determined from x-ray diffraction data and serves as the lower cladding layer of the laser. InAs QDs are inserted into an $In_{0.4}Ga_{0.6}As$ QW, which is grown by the digital alloy technique and formed above and below the dots. The temperature is maintained at 490°C during the growth of the QD and QW active region. The upper p-type cladding layer is lattice-matched $Al_{0.74}In_{0.26}As$. Work is in progress to increase the Sb composition of the metamorphic buffer to extend the wavelength to 1.55 μm. [1]G.T. Liu, A. Stintz, H. Li, K.J. Malloy, L.F. Lester, Electron. Lett., 35,1163 (1999); [2]T. C. Newell, D. J. Bossert, A. Stintz, B. Fuchs, K. J. Malloy, L. F. Lester, IEEE Photon. Technol. Lett. 11, 1527-1529 (1999); [3]A. Stintz, G.T. Liu, H. Li, L.F. Lester, and K.J. Malloy, to be published in IEEE Photon. Technol. Lett., July 2000; [4]V.M. Ustinov, N.A. Maleev, A.E. Zhukov, et. al., Appl. Phys. Lett. 74, 19 (1999); [5]D.L. Huffaker, G. Park, Z. Zou, O.B. Shchekin, and D.G. Deppe, Appl. Phys. Lett., 73, 18 (1998).

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G5, Normal Incidence InAs/InAlGaAs Quantum Dot Infrared Photodetectors with Undoped Active Region: *Zhonghui Chen*[1]; E. T. Kim[1]; I. Mukhametzhanov[1]; J. Tie[1]; A. Madhukar[1]; Z. Ye[2]; J. C. Campbell[2]; [1]University of Southern California, Depts. of Matls. Sci. & Phys., 3651 Watt Way, Los Angeles, CA 90089-0241 USA; [2]The University of Texas at Austin, Microelect. Rsrch. Ctr., Dept. of Electl. Eng., Austin, TX 78712 USA

Epitaxical self-assembled semiconductor quantum dots are attractive candidates for mid and long wavelength (3-14μm) photodetectors. We report on n-type quantum dot infrared photodetectors (QDIPs) with undoped active region (n-i-n configuration) comprising InAs/InAlGaAs QDs. The QDIP samples were grown on GaAs(001)±0.1° substrates via molecular beam epitaxy. We have systematically studied InAs/GaAs as well as InAs/GaAs/AlGaAs/GaAs QDIPs consisting of a unique class of QDs grown via the punctuated island growth (PIG) approach. Photoluminescence (PL) spectra on the QDIP samples show full-width at half-maximum (FWHM) of about 25meV, indicating the high quality and uniformity of these QDs. The InAs QD size, density, as well as the structure and defect density of QDIPs were characterized using AFM and X-TEM. The interband transitions of the PIG InAs QDs embedded in n-i-n QDIP structures have been comprehensively characterized with PL, PL excitation and inter-band photocurrent spectroscopy. Our FTIR based intra- and inter-band photocurrent results show that appropriately designed InAs/AlGaAs QDIPs can serve as a sensor simultaneously for near IR (~1μm) and middle IR radiation. AlGaAs layers inserted in the active region of QDIPs can serve as confining layers as well as blocking layers. The intraband photoresponse peaks at 10.8μm (115meV) and 7.2μm (175meV) correspond to bound-to-bound transitions. A line width of the QDIP intraband photoresponse as narrow as 0.5μm (16meV) has been achieved. In addition, detailed FTIR intraband photovoltage and photocurrent spectroscopy studies offer evidence for dipole between different electron states. Measurements on these QDIPs show, at 77K, an intraband peak photoresponsivity of ~0.4A/W and peak detectivity between 5-10x10^{8}cmHz$^{1/2}$/W. In addition, we studied electronic structures of InAs/InGaAs QDs by using PL, PL excitation and interband photocurrent spectroscopy. The device characteristics (such as dark current and mid infrared photocurrent) of QDIPs based on the InAs/InGaAs and InAs/AlGaAs QDs will be discussed. (Work supported by AFOSR under MURI-98 program on Nanoscience).

3:00 PM Break

3:20 PM (Student)

G6, Tuning InAs/InAlGaAs Quantum Dot Structures for Infrared Photodetectors: *Eui-Tae Kim*[1]; Zonghui Chen[1]; Anupam Madhukar[1]; [1]University of Southern California, Dept. of Matls. Sci., 3651 Watt Way, VHE 514, Los Angeles, CA 90089-0241 USA

Manipulation of and control on the electronic structure of strain-driven coherent island based quantum dots (QDs) is central to exploiting this class of QDs for applications in electronics and optoelectronics. We have focused attention on the classes of QDs that can be formed within the In, Ga, Al and As combinations, and their characteristics. In this paper we will present some findings for the InAs (island)/InAlGaAs (barriers) combination QD structures with the particular objective of their potential for simultaneous near and mid infrared (IR) normal incidence photodetectors. We will present a systematic study of molecular beam epitaxically grown InAs QDs with InAlGaAs cap/bottom layers characterized using photoluminescence (PL), PL excitation (PLE), atomic force microscopy and transmission electron microscopy. Very uniform InAs QDs are formed with 2.5ML InAs delivery at the slow growth rate of 0.054ML/sec at 500°C. The QDs capped by 170 ML GaAs show PL peak position at 1.183μm with 23meV FWHM at 77K. With increasing In composition in a 30ML thick $In_xGa_{1-x}As$ layer replacing the first 30MLs of GaAs in an otherwise 170ML thick GaAs cap layer the PL peaks are red-shifted, reaching 1.246μm (1.335μm) at 79K (296K) with 19meV (20meV) of FWHM for x = 0.20. This is due to the attendant shallower confinement potential and larger strain relaxation in such QDs. PLE spectra show that the energy difference between the excited transitions and ground state transition decreases slightly with increasing In composition in the 30ML $In_xGa_{1-x}As$ layer. For example the structure (InAs QDs/30ML $In_{0.2}Ga_{0.8}As$/140ML GaAs) shows strong peaks at 76meV and 153meV and weak peaks at 54meV and 120meV above the ground state transition while the structure (InAs QDs/170ML GaAs) shows strong peaks at 83meV and 166meV and weak peaks at 60meV and 134meV. Such partially strain relieved QDs have been grown in n-i(QD)-n quantum dot infrared photodetector (QDIP) structures comprising a stack of 5 InAs QD layers with 150ML spacers and Si-doped top and bottom contact layers. In order to check the detection bands of such QDIPs, interband (for near IR) and intra-band (for mid IR) photocurrent spectroscopy has been performed utilizing a Fourier transform infrared spectrometer. All photocurrent (PC) data were acquired in the normal incident configuration. The QDIP samples with InAs QDs/150 ML GaAs show very strong and narrow (32meV) PC peak at 7.2μm at 77K. Change in PC spectra with various top and/or bottom layer of InAs QDs will be discussed. The complementary information obtained from PLE and PC spectroscopies provide a more comprehensive view of the electronic structure of such QDs. Work supported by AFOSR under the MURI 98 program on nanoscience.

3:40 PM

G7, Near 1.5 μm Infrared Detectors Based on Ge Quantum Dots on Si Substrate: *Song Tong*[1]; Jianlin Liu[1]; Vincent Pouyet[1]; Rahim Faez[1]; *Kang L. Wang*[1]; *Jun Wan*[1]; [1]University of California at Los Angeles, Electl. Eng. Dept., Device Rsrch. Lab., Los Angeles, CA 90095-1594 USA

The advantage of their compatibility with the state-of-the-art VLSI technology makes Si-based infrared photodetectors a very interesting subject of investigation for optical fiber communications in recent years. Ge quantum dots grown on Si are a competitive material in this field due to the low defects density and the possibility of tuning the energy to 1.5 μm comparing to its Si1-xGex counterpart. In this presentation, we report the results of photoresponse of p-i-n detectors with Ge quantum dots incorporated into the intrinsic layer. A strong resonant peak from 1.3 to 1.5 μm of Ge dots was observed at room temperature. Using a 1.55 μm laser, strong avalanche enhance of the photoresponse was observed at around 4.5 V reverse bias. The peak response wavelength was found to be dependent on Ge dot size. The quantum efficiencies of the detector were estimated.

4:00 PM (Student)

G8, Stable Growth of AlInAsSb Quaternaries Using a Digital Alloy Technique: *Leslie G. Vaughn*[1]; L. Ralph Dawson[1]; A. L. Gray[1];

Edwin Pease[1]; Luke F. Lester[1]; [1]University of New Mexico, Ctr. for High Tech. Matls., 1313 Goddard S.E., Albuquerque, NM 87106 USA

Alloys of the Al(x)In(1-x)As(y)Sb(1-y) quaternary are very useful in mid-IR laser structures such as barrier materials for InAs or InAsSb quantum wells on GaSb substrates. The region of stable growth of these alloys on GaSb is limited to $x < 0.06$[1]. The trend in reported results indicates that increasing the aluminum content may improve the efficiency and T° of laser structures by improving the hole confinement in the quantum well. Unfortunately, for larger aluminum mole fractions a miscibility gap is predicted, and very rough surfaces and multiple XRD peaks are observed for bulk-grown samples. Stable growth of these alloys at higher aluminum concentrations will open up a new material system for mid-IR applications. Using a digital alloy technique, smooth, bulk-like 1 micron-thick films of Al(x)In(1-x)As(y)Sb(1-y) quaternary alloys have been grown lattice-matched to GaSb with aluminum concentrations well into the predicted miscibility gap. Films with an overall x of 0.20 to 0.40 were grown incor porating very thin layers of AlSb, InAs and InSb binaries, with each binary period on the order of a few monolayers and a total digital alloy period of 20-25 angstroms. These binaries allowed for independent adjustment of the Al to In ratio and the As to Sb ratio without the nuances of ternaries and competing Group V species. For each composition, the Al to In ratio was fixed and the As to Sb ratio was varied to achieve lattice-match to GaSb. Optical inspection of these 1 micron-thick samples using Nomarski shows very smooth film surfaces with no crosshatching or microcracks, which occur due to dislocations. Preliminary x-ray diffraction data also show that the average composition of the digital alloy is lattice matched to within 50-200 arcseconds of the GaSb substrate for each of these films, and that the films are of high single-crystal quality. Additionally, photoluminescence measurements taken at 90-100K indicate a peak for the film with an overall x=0.2 at around 2.15 microns. The PL peak confirms that the material has a direct bandgap, as expected for bulk material of this composition and that the film is of optical device quality. These results are very promising for the use of Al(x)In(1-x)As(y)Sb(1-y) to increase performance in mid-IR laser structures. [1]H. K. Choi, G. W. Turner, M. J. Manfra, and M. K. Connors, Applied Physics Letters 68, 21 (1996).

4:20 PM

G9, Thermal and Optical Characteristics of MBE Grown InAs/AlSb Superlattices: *Dapeng Xu*[1]; Hong Wen Ren[1]; Anwen Liu[1]; Chih-Hsiang Lin[1]; Shin-Shem Steven Pei[1]; Theodorian Borca-Tasciuc[2]; D. Achimov[2]; W. L. Liu[2]; Gang Chen[2]; [1]University of Houston, Dept. of Electl. & Comp. Eng. & Space Vac. Epitaxy Ctr., Houston, TX 77204-5507 USA; [2]University of California at Los Angeles, Mechl. & Aeros. Eng. Dept., Los Angeles, CA 90095-1597 USA

There has been significant progress in the development of mid-infrared lasers, very long wavelength infrared photodetectors, resonant tunneling diodes, and field effect transistors based on InAs/GaSb/AlSb heterostructures. Many studies have been carried out in the growth, interface properties, and electrical and optical characteristics of the InAs/AlSb structures. The thermal conductivity of InAs/AlSb superlattices is also of considerable interests for the thermal management of mid-IR lasers, which are severely limited by the temperature rise in the active region. In addition, strong interests exist to understand heat conduction mechanisms in superlattices for optoelectronic, thermoelectric, and thermionic applications. Experimental results on the thermal conductivity of superlattices have been reported in recent years for several materials systems, including GaAs/AlAs, GaAs/AlGaAs, Si/SiGe, Si/Ge, and BiTe/SbTe. These studies demonstrate that the thermal conductivity of a superlattice could be orders of magnitude lower than the bulk values of its constituent materials or the equivalent composition alloys. In this work, we present experimental studies on the cross-plane thermal conductivity of InAs/AlSb superlattices. The thermal conductivity of MBE grown InAs/AlSb superlattices are characterized using the 3ω method from 80-300K. Significant reductions in thermal conductivity are observed in these superlattices comparing to the predictions of the Fourier heat conduction theory based on the bulk material properties. The influence of the growth temperature and post annealing is also investigated. It was demonstrated previously that annealing at higher than the growth temperature improves material quality by reordering as-grown lattices and reducing structural defects. Our study of mid-IR photodetectors based on InAs/GaInSb type-II SLs has unambiguously demonstrated the effect of thermal annealing. The photo-response from the samples annealed at ~ 510°C for 10 minutes after growth, was increased by nearly an order of magnitude over as-grown ones (without annealing). This remarkable improvement on photo-response was believed to be due to the improved material quality with longer carrier lifetime. However, for these annealed samples, further reduction in thermal conductivity was observed. The broadening of photoluminescence spectrum of these annealed samples suggested rougher interfaces due to additional interdiffusion caused by the post growth annealing. In summary, both the thermal and optical characteristics of InAs/AlSb superlattices depend strongly on the thickness, interface quality and, therefore, the growth and annealing temperatures of the superlattice. The correlation between the thermal and optical characteristics will also be presented.

4:40 PM, G10, Late News

Session H: Special Topical Session on Bioelectronic Materials and Biological/Electronic Interfaces

Wednesday PM Room: 101
June 27, 2001 Location: University of Notre Dame

Session Chairs: Carol Ashby, Sandia National Laboratories, Albuquerque, NM 87185-1425 USA; David Janes, Purdue University, Dept. of Electl. Eng., West Lafayette, IN 47907-1285 USA; George Maracas

1:20 PM Invited

H1, Nanoscale Optoelectronic Photosynthetic Devices: *Elias Greenbaum*[1]; Ida Lee[2]; Michael Guillorn[3]; James W. Lee[1]; Michael L. Simpson[3]; [1]Oak Ridge National Laboratory, Chem. Tech. Div., PO Box 2008, Oak Ridge, TN 37831-6194 USA; [2]The University of Tennessee, Dept. of Electl. Eng., Knoxville, TN 37996 USA; [3]Oak Ridge National Laboratory, Instrumentation & Controls Div., PO Box 2008, Oak Ridge, TN 37831 USA

This presentation provides an overview and recent progress in the Oak Ridge National Laboratory research program in molecular electronics and green plant photosynthesis. The photosynthetic reaction center is a nanoscale molecular diode and photovoltaic device. The key thrust of our research program is the construction of molecular electronic devices from these nanoscale structures. Progress in this multidisciplinary research program has been demonstrated by direct electrical contact of emergent electrons with the Photosystem I (PS I) reaction center by nanoparticle precipitation. Demonstration of stable diode properties of isolated reaction centers combined with the ability to orient PS I by self-assembly on a planar surface, makes this structure a good building block for 2-D and potentially 3-D devices. Metallization of isolated PS I does not alter their fundamental photophysical properties and they can be bonded to metal surfaces. We report here the first measurement of photovoltage from single PS I reaction centers. Working at the Cornell University National Nanofabrication Facility, we have constructed sets of dissimilar metal electrodes separated by distances as small as 6 nm. We plan to use these structures to make electrical contact to both ends of oriented PS I reaction centers and thereby realize biomolecular logic circuits. Potential applications of PS I reaction centers for optoelectronic applications as well as molecular logic device construction will be discussed.

2:00 PM Invited

H2, Protein-Based 3D Memories and Associative Processors: *J. A. Stuart*[1]; R. R. Birge[2]; [1]Syracuse University, W. M. Keck Ctr. for Molecular Elect., Syracuse, NY 13244 USA; [2]University of Connecticut, Dept. of Chem. & Molecular & Cell Bio., Storrs, CT 06269 USA

Molecular electronics offers a powerful and cost-effective path towards computer miniaturization and the generation of neural and three-dimensional architectures. Bioelectronics explores the use of native and

genetically modified biomolecules and offers advantages because nature has generated unique materials with optimized properties through evolution and natural selection. This presentation will explore the use of the protein, bacteriorhodopsin, in optical three-dimensional memories and parallel associative processors. Three-dimensional memories store information in a memory volume element, and provide as much as a thousand-fold improvement in memory storage capacity over current technology. The comparative advantages and disadvantages of holographic, two-photon and sequential one-photon volumetric architectures will be discussed. The associative memory operates in a fashion somewhat analogous to the human brain and responds to input data by finding (in a few nanoseconds) the closest match within the data base and feeding this information, and any associated information, to the output. Such a memory is critical to the development of artificial intelligence. The use of site directed mutagenesis to improve the properties of the protein for specific applications will also be discussed. Although a number of working prototypes have been developed, a number of cost/performance and architectural issues must be resolved prior to commercialization.

2:40 PM

H3, Enzyme Electrode Based on Nano-Patterned Alumina: *Juan Jiang*[1]; Pavlo Takhistov[1]; Albert E. Miller[1]; [1]University of Notre Dame, Cheml. Eng., 182 Fitzpatrick Hall, Notre Dame, IN 46556 USA

For the first time nano-porous (30-80 nm) anodic aluminum oxide (AAO) layer has been investigated for the purpose of application as a substrate material for enzymatic biosensor operating in aqueous solutions. Biocompability of nano-size porous alumina as an immobilization matrix for bio-colloidal systems have stimulated our interest to development of active biosensitive materials which are compatible with integrated silicon technology. Nano-scale porous AAO has been formed by electrical anodization in acid solution. By changing the anodization conditions, such as electrolyte concentration, temperature, and anodization time, the well-ordered hexagonal porous structure can be obtained; the pore size and depth can be well controlled. Nano-porous alumina was used as substrate to adsorb enzymes. The AAO has been used as a pH sensor and enzyme electrode. The pH change is driven by the enzymatic reactions, such as penicillin G is hydrolyzed to penicilloic acid in the presence of penicillinase. Penicillinase, a model enzyme in this work, was bound to the porous structure by physical adsorption. The advantage of adsorption is that usually no reagents are required and only a minimum of "activation" or clean-up steps. Adsorption tends to be less disruptive to enzyme proteins than chemical methods of attachment. Binding forces are due to hydrogen bonds, multiple salt linkages and Van der Waals forces. Due to the enlargement of the active sensor area, the immobilization of the enzyme has been enhanced, which in turn increased the sensitivity of the sensor. To characterize the interactions of enzyme with nano-porous alumina oxide, Electrical Impedance Spectroscopy (EIS), Cyclic Voltammetry, and Open Circuit Potential measurements have been performed. The measured signals has two components: a non-Faradaic component resulting from redistribution of charged and polar species at the electrode surface and a Faradic component resulting from electron exchange between enzyme electrode and solution (i.e. electrochemical reaction). Stability of enzyme/substrate complex as a function of pH and temperature has been determined by the analysis of the changes of cyclic voltammograms. In addition, the information about electrochemically coupled enzymatic reaction and substrate electrochemical response upon which the biosensor is based, is provided. A microchannel with the AAO biosensor incorporated as a portion of the channel's wall has been used for flow injection analysis (FIA). This pH-sensitive nanoporous electrode substrate can also be applied as sensors to urea and glucose using enzymes, which induce a pH change.

3:20 PM Break

3:40 PM Invited

H4, Semiconductor Nanocrystal Quantum Dots: From Scaling Laws to Biological Applications: *A. Paul Alivisatos*[1]; [1]University of California–Berkeley, Dept. of Chem., B62 Hildebrand Hall, Berkeley, CA 94720-1460 USA

Inorganic nanocrystals strongly exhibit size and shape dependent optical, electrical, and magnetic characteristics. Further, high quality and monodisperse nanocrystals of many inorganic solids can be prepared in colloidal form, in shapes ranging from spheres to rods, to teardrops, arrows, and even "tetrapods". This talk will describe work aimed at using semiconductor nanocrystals as luminescent labeling reagents for biological imaging experiments. Many different sizes of quantum dot (and hence colors) may be excited with a single excitation laser. In addition, the dots are fairly robust probes, and lend themselves to time-gated detection for autofluorescence background suppression. Recent experiments directed at using DNA to spatially organize nanocrystals into linear sequences, and work on controlling nanocrystal shapes will also be described.

4:20 PM Invited

H5, Constructed Networks of Dissociated Rat Hippocampal Neurons Cultured on Microelectrode Arrays: *Conrad D. James*[1]; Andrew J. H. Spence[1]; Harold G. Craighead[1]; Michael S. Isaacson[1]; Natalie Dowell[2]; William Shain[2]; James Turner[2]; [1]Cornell University, Appl. & Eng. Phys., 212 Clark Hall, Ithaca, NY 14853 USA; [2]Wadsworth Center, Dept. of Health, ESP P1 S. Dock J3, Albany, NY 12237 USA

The construction of cell networks from dissociated primary neurons has been investigated for an assortment of practical applications such as cell-based biosensors, tissue engineering, and prosthetic devices. These types of cultures have also proved useful for basic research into biologically-relevant phenomena such as synaptogenesis, protein and vesicle trafficking, and synaptic plasticity studies. Several polypeptides and proteins, such as poly-L-lysine and laminin, initiate and facilitate cell attachment and neurite outgrowth in vitro, and some of these molecules have been patterned onto surfaces to assemble artificial neuronal cell networks. In order to take full advantage of chemotropic methods of cell network formation, we present techniques for combining chemical patterning and microfabricated electrode arrays to study spontaneous and elicited action potentials and field excitatory post-synaptic potentials (fEPSPs) of hippocampal pyramidal cell networks. In addition to providing a method for conduc ting long-term, non-invasive electrophysiological investigations, microelectrode arrays permit multi-unit and multi-site-on-single-unit recording and stimulation. This technology has been used to explore the initiation and propagation of action potentials in neuronal cells and to document the nascent characteristics and development of rhythmic bursting activity in cell networks. The purposeful placement and positioning of cell bodies, dendritic processes, and axons on surfaces with embedded microelectrodes will allow the examination of the influence of cytoarchitecture and network architecture on electrical activity during maturation. In addition, we present a theoretical model of the correlation between intracellular and extracellular recordings to evaluate the performance of the electrode array transducer and to guide our interpretations of cell activity by measuring relevant electrophysiological parameters such as conduction velocity and action potential time-course.

5:00 PM Invited

H6, Chemical Sensors Based on Modulation of Work Function: *J. Janata*[1]; [1]Georgia Institute of Technology, Sch. of Chem. & Biochem., Atlanta, GA 30332 USA

Interaction of gas molecules with semiconductors can be regarded as a form of doping. When it takes place the internal energy of the semiconductor changes which is reflected in the change of the work function of the polymer. When only a fraction of the charge density is involved the guest molecule and the host matrix form a charge-transfer complex. The slope of the work function/concentration dependence has a fractional value of the typical Nernst slope reflecting the partial charge transfer due to the formation of the charge transfer complex. The modulation of work function as a transduction principle is important for an entire class of potentiometric solid state chemical sensors for gases. The ability to tune the affinity of the organic semiconductor for electrons (electron donacity) was demonstrated for several combinations of gases and organic vapors. A general sensing platform consisting of eight modules has been designed and fabricated in silicon. The operating function of this platform has been divided between a chemical sensing chip (CSC) and an electronic service chip (ESC). The CSC and ESC chips are connected by flip-chip bonding which greatly simplifies the packaging. The operation of the combined impedance and work function sensing has been verified by exposure to various gases.

Session I: Growth and Properties of Quantum Wires

Wednesday PM Room: 102
June 27, 2001 Location: University of Notre Dame

Session Chairs: James L. Merz, University of Notre Dame, Dept. of EE, Notre Dame, IN 46556-5602 USA; Hiroyuki Sakari, IIS, Minato-Ku, Tokyo 106-8558 Japan

1:20 PM Invited

I1, Epitaxial Growth and Transport Properties of Step Quantum Wires and Planar Superlattice Structures: *H. Sakaki*[1]; T. Noda[1]; Y. Nakamura[1]; T. Kawazu[1]; Y. Nagamune[1]; M. Lachab[1]; [1]University of Tokyo (IIS), 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505 Japan

In recent years, a variety of epitaxial methods have been explored to fabricate 10nm-scale quantum wire (QWR) and quantum dot (QD) structures, as they are attractive for fundamental physics studies and electronic and photonic applications. For example, the selective growth on patterned substrates has yielded sharp facet structures, with which QWRs and QDs are formed along facet ridges (R) and grooves (G) and at facet corners (C). The overgrowth onto the exposed edge of quantum wells (QWs) has been also used to form both T-shaped edge (E) QWRs and modulation doped E-QWRs. These two approaches offer relatively good shape controllability but suffer from the process complications caused by the non-planar aspects of resultant structures. As complementary and quasi-planar approaches, the self-organized (S-K) growth of QDs on lattice mismatched substrates and the spontaneous formation of QWRs along single or bunched atomic steps (S) on vicinal planes of miscut substrates have been widely investigated. In this talk, we first review both advantages and weakness of these representative methods. We then describe in detail the current state of art for the epitaxial growth of QWRs along the bunched steps with special emphasis on our recent effort to form such step QWRs on vicinal (111) B planes of GaAs. In particular, we report on our studies to clarify and to control electon transport phenomena along such quasi periodically modulated hetero interfaces. Device prospects of such step wire structures will be also discussed.

2:00 PM

I2, Ultrahigh Quality AlGaAs/GaAs Quantum Wires Grown by Flow Rate Modulation Epitaxy Using Tertiarybutylarsine: *Xue-Lun Wang*[1]; Xingquan Liu[1]; Mutsuo Ogura[1]; [1]Japan Science and Technology Corporation, Electron Dev. Div., Electrotechl. Lab., & CREST, 1-1-4 Umezono, Tsukuba 305-8568 Japan

Flow rate modulation epitaxy (FME) on patterned substrates has been proven to be a very powerful technique for the fabrication of high-quality semiconductor quantum wires (QWRs). Using AlGaAs/GaAs QWRs grown by this technique on V-grooved substrates, we have succeeded in the investigation of many intrinsic quantum effects of QWR structures and also in the first demonstration of QWR lasers emitting from ground state at room temperature. However, highly toxic AsH_3 gas has been exclusively used as the arsenic source material in the selective growth of GaAs until now. In this paper, we report the FME growth of V-shaped AlGaAs/GaAs QWRs using tertiarybutylarsine (TBAs), a less-toxic liquid material, as the arsenic source. We show that TBAs is an excellent replacement gas for AsH_3 for selective growth of QWRs, not only from the viewpoint of safety but also from the greatly improved QWR quality. Epitaxial growth was carried out in a low-pressure MOVPE reactor at 630°C on [01-1] oriented 4 μm pitch V-grooved GaAs substrates. The structural properties of the grown QWRs were characterized by TEM and AFM. From cross-sectional TEM observation, the growth selectivity of TBAs (ratio of growth rate at V-groove center to that at (111)A side wall) was found to be as high as that of growth using AsH_3. Further, the V-groove with an intersecting angle of about 78° at the QWR position is shaper than that of growth using AsH_3 (intersecting angle = 82°). Another important feature of growth using TBAs is that the step-bunching induced step arrays on the (311)A QWR facets were greatly suppressed compared with the growth using AsH_3 from AFM observation of thick QWR surface. The ultrahigh optical qualities of the grown QWRs were revealed by optical characterization using PL, PLE, and time-resolved PL. A 4.5 nm thick QWR grown using TBAs showed an energy separation between the ground and the first excited QWR states as large as 58 meV and a ground state Stokes shift as small as 3.9 meV at 5K. These values are 12 meV larger and 2.3 meV smaller than those of QWRs grown using AsH_3, indicating that TBAs can produce QWRs with stronger lateral quantum confinement and smoother heterointerfaces than AsH_3. From time-resolved PL measurements, the radiative-recombination dominated luminescence for a 5 nm QWR lasted to a temperature as high as 240K which is about 90K higher than that of a QWR grown using AsH_3, suggesting an extremely low concentration of nonradiative recombination centers in QWRs grown using TBAs. It is especially noteworthy to point out that this temperature is also about 90K higher than that of a quantum well (QWL) grown under similar conditions. This result clearly demonstrated the high predominance of QWRs over QWLs as the materials for high-efficiency optical devices.

2:20 PM

I3, Exciton Scattering by Auger Processes in a Single Quantum Wire: Valia Voliotis[1]; Roger Grousson[1]; Joel Bellessa[1]; Thierry Guillet[1]; Xue Lun Wang[2]; Mutsuo Ogura[2]; [1]University Paris VI and Paris VII, Groupe de Physique des Solides, 2 place Jussieu, Paris 75005 France; [2]Electrotechnical Laboratory, 1-1-4 Umezono, Tsukuba 305 Japan

Carrier relaxation and carrier capture in zero-dimensional (0D) quantum structures is a remaining question. For quantum boxes (QB), one would expect that at low excitation intensities emission from excited states should be observed due to the discrete spectrum of energy levels and the restricted inter-level relaxation. We recently observed a dependance of relaxation times via LA-phonons with the inter-level spacing [1]. Indeed a slowing down of the relaxation has been evidenced for small QBs. Nevertheless the relaxation times remain very fast (<100 ps). It implies that other mechanisms similar to Auger scattering are very efficient and lead to rapid thermalization of carriers and emission from the lowest lying level. We study a single V-shaped GaAs/GaAlAs quantum wire (QWR) by resonant time-resolved micro-photoluminescence (m-PL) under high excitation intensities. We have shown previously by m-PL experiments that strong localization occurs due to the thickness fluctuations along the axis of the wire[2]. Therefore exciton dynamics are governed by the properties of a QB system[1]. Here we show that state filling effects appear in the lowest lying levels when this collection of QBs is excited at high excitation intensity. However transfer of carriers from one QB to another adjacent one has been observed instead of emission from excited state transitions. This transfer is attributed to an Auger-like scattering process. We show that this mechanism is very efficient and occurs as soon as two electron-hole pairs are initially created in an excited state of a dot. One of them relaxes to the ground state while the other is ejected to a continuum wire state. The total energy of the system is conserved during this process. References: [1]J. Bellessa, V. Voliotis, R. Grousson, X. L. Wang, M. Ogura and M. Matsuhata, Phys. Rev. B 58, 9933 (1998); [2]J. Bellessa, V. Voliotis, R. Grousson, X. L. Wang, M. Ogura and M. Matsuhata, Appl. Phys. Lett. 71, 2481 (1997).

2:40 PM

I4, Magnetic and Structural Properties of Electrochemically Self-Assembled Fe/Co Quantum Wires: *Latika Menon*[1]; Hao Zeng[2]; David Sellmyer[2]; Supriyo Bandyopadhyay[1]; [1]University of Nebraska, Dept. of Electl. Eng., Lincoln, NE 68588-0511 USA; [2]University of Nebraska, Dept. of Phys., Ctr. for Matls. Rsrch. & Analy., Lincoln, NE 68588-0111 USA

An ordered array of Fe/Co nanowires (with density approaching 1E12 wires/cmE2) were self assembled by electrodeposition in alumite templates. The crystal structure of the wires was found to be bcc at the Fe end and remained so until about 67% at addition of Co. At the Co end, the structure was a mixture of bcc and hcp. Magnetic measurements have shown unprecedented high coercivities for the nanowires approaching 3000 Oe at room temperature for 8 nm diameter wires. While Fe nanowires show a non-monotonic dependence of coercivity on wire diameter, the Fe/Co alloy wires show a monotonically decreasing coercivity with increase in wire diameter. Temperature and size dependence of magnetic properties show no signs of superparamagnetic effects in the alloy wires

down to a diameter of 8 nm. These wires are extremely promising candidates for high density magnetic recording.

3:00 PM Break

Session J: Self-Assembled Nanostructures

Wednesday PM Room: 102
June 27, 2001 Location: University of Notre Dame

Session Chairs: Supriyo Bandyopadhyay, University of Nebraska, Dept. of Elect. Engr., Lincoln, NE 68588-0511 USA; Ray Tsui, Motorola Laboratories, Tempe, AZ 85284 USA

3:20 PM (Student)
J1, Structural Investigation of Wurtzite GaN Nanowires Fabricated Via Direct Reaction of Ga and Ammonia: *Randolph N. Jacobs*[1]; Lourdes Salamanca-Riba[1]; Maoqi He[2]; Gary L. Harris[2]; Piezhen Zhou[2]; S. Noor Mohammed[2]; Joshua B. Halpern[2]; [1]University of Maryland, Matls. & Nuclear Eng., Bldg. 090, College Park, MD 20742 USA; [2]Howard University, Matls. Sci. Rsrch. Ctr. of Excellence, 500 College Ave., Washington, DC 20059 USA

A structural investigation of large-scale GaN nanowires is carried out, with an emphasis in understanding the general growth mechanism. The one-dimensional structures reported here are grown through a novel method based on the reaction of Ga vapor with ammonia (NH_3) in a tube furnace at elevated temperatures. This new technique[1] is rather simple in that catalysts or templates such as carbon nanotubes (reported elsewhere) are not required. We have shown that these nanowires are wurtzite in structure, and generally range from approximately 25 to over 100 nm in diameter and greater than 500 µm in length. However, the fundamental growth mechanism involved in this new technique is not yet understood. In this study we use transmission electron microscopy (TEM) to carry out a detailed structural investigation and use x-ray diffraction (XRD) and energy dispersive x-ray spectroscopy (EDS) data for supporting analysis. In general, TEM images reveal three different GaN structures including thin hexa gonal platelets, faceted large diameter one-dimensional structures, and small diameter (<50 nm) nanowires. Our findings indicate that the nanowires nucleate and grow from the thin platelet structures. While several questions still remain, evidence obtained in this study suggests the exact orientation and structural features of the wires depend on specific growth conditions such as temperature and ammonia flow rate.
[1]M. He, I. Minus, P. Zhou, S.N. Mohammed, J.B. Halpern, R.N. Jacobs, W.L. Sarney, L. Salamanca-Riba, R.D. Vispute., Appl. Phys. Lett. 77, 3731 (2000).

3:40 PM (Student)
J2, Template Directed Vapor-Liquid-Solid Growth of Silicon Nanowires: *Kok-Keong Lew*[1]; Cordula Reuther[1]; Joan M. Redwing[1]; [1]Pennsylvania State University, Dept. of Matls. Sci. & Eng., 4 Steidle Bldg., University Park, PA 16802 USA

There is currently intense interest in one-dimensional nanostructures, such as nanotubes and nanowires, due to their potential to test fundamental concepts of dimensionality and to serve as building blocks for nanoscale devices. Carbon nanotubes have been the focus of much of this work, however, it has proven difficult to control conductivity in these structures which restricts their application. As a result, there is increasing interest in the development of novel methods for semiconductor nanostructure fabrication. Vapor-liquid-solid (VLS) growth is a promising technique for the synthesis of semiconductor nanowires. In this method, a metal catalyst is used to form a liquid alloy drop, which nucleates the growth of a single crystal semiconductor whisker from a vapor phase. The fabrication of nanometer-size wires can be achieved through careful control of the catalyst particle diameter and the VLS growth conditions. Prior studies have demonstrated the fabrication of Si, Ge, GaAs and InP nanowires using techniques such as lithography or laser ablation to define the initial size of the metal catalyst. In this study, we have investigated the use of nanoporous membranes as templates for vapor-liquid-solid growth of silicon nanowires. The use of nanopores for growth and assembly provides control over nanowire diameter (~10 nm to 200 nm) as well as growth direction. Furthermore, template directed synthesis offers the ability to combine metal electrodeposition with VLS growth for the fabrication of multi-layered metal-semiconductor-metal nanowires. In this study, gold was electrodeposited as a catalyst agent into commercially available anodic alumina membranes (200 nm nominal pore diameter) prior to VLS growth. The gold catalyst was positioned approximately 10 mm from the top surface of the pore. Vapor-liquid-solid growth was then carried out in a low pressure CVD reactor using a mixture of 5% SiH_4 in a H_2 carrier gas at 500°C and a total pressure of 10 Torr. The low temperature and pressure were required to achieve SiH_4 diffusion into the pores without reaction on the pore walls. The gold catalyst nucleated growth of silicon nanowires within the pores and nanowires were observed to emerge from the top of the pores and populate the surface after a growth time of 30 minutes. The presence of gold at the tips of the nanowires provided evidence of a vapor-liquid-solid growth mechanism. The majority of the nanowires had diameters in the range of 250-290 nm, which is close to the nominal pore size of the alumina membranes. Wet etching was used to release the nanowires from the alumina membrane. Initial TEM results indicate that the nanowires consist of single crystal silicon cores with a thin (~2 nm) oxide coating. The potential for using template directed VLS growth for the fabrication of more complex multi-layered nanowires will be discussed.

4:00 PM
J3, Nucleation and Heteroepitaxy Processes in Self-Assembly of Si Nanostructures: *Elena A. Guliants*[1]; Chunhai Ji[2]; Wayne A. Anderson[2]; [1]Taitech, Inc., AMC PO Box 33630, Wright-Patterson AFB, OH 45433-0630 USA; [2]State University of New York at Buffalo, Dept. of Elect. Eng., 217C Bonner Hall, Buffalo, NY 14260 USA

Self-assembly represents a big prospective class of fabrication techniques on the nanometer-length scale. The self-assembly methods rely on spontaneous structural changes that occur in bulk or thin-film materials due to the spatial fluctuations of their chemical or physical properties. To date, a vast majority of two-dimensional arrays of nanostructures are prepared using lithographic structure definition techniques such as optical, ion- and electron-beam lithography, and local anodic oxidation by atomic force or scanning tunneling microscopy. These techniques provide highly uniform arrays of nanostructures as compared to self-assembly methods, in which control over the nanostructure dimensions and array uniformity poses significant challenges. On the other hand, self-assembled systems have a potential advantage in ease of fabrication by avoiding additional processing steps such as patterning and etching. Besides, an instability issue is less pronounced in self-organized nanostructures since they initially assemble as energetically favored sites. Therefore, understanding the physical mechanisms underlying the processes of nanostructure formation is crucial for establishing the control over their dimensions and spatial distribution. In this work, self-assembly of Si nanostructures was studied by silicon deposition on a thin metallic prelayer. Spatially separated Si nanowires were obtained by magnetron sputtering of Si on a 25nm thick Ni prelayer at ~500-600°C. The formation of the NiSi2 compound at the Ni-Si interface followed by Si heteroepitaxy on the lattice-matched NiSi2 is shown to be the driving force for the wire formation. We have repeatedly demonstrated the formation of 2500nm length nanowires having a diameter of 500-800nm. The Si film formation follows the Stranski-Krastanow growth mode which was previously adopted for the lattice-matched systems. The grains comprising the Si epilayer have a cubic lattice with a lattice constant equal to that of NiSi2, and the Si film grows mechanically strained. The strain energy increases linearly with the Si film thickness until the latter reaches some critical value, when the relaxation process takes place via introduction of misfit dislocations. We will discuss how these dislocations affect the structure of the growing film and lead to the formation of individual Si whiskers. Moreover, it was previously established that the thickness of a Ni prelayer significantly altered the structure of the silicon film during metal-induced Si growth on a Ni prelayer. The phenomenon was attributed to the Ni silicide nucleation processes at the Ni-Si interface. Therefore, the Ni silicide nucleation mechanism is suggested to be one of the main factors that control the Si nanowire cross-section diameter. A discussion will be offered on how the Si nucleation behavior and Si deposi-

tion conditions contribute to the whisker assembly process. We will also discuss control of whisker crystal orientation and impurity content.

4:20 PM

J4, Synchronized Pinning Due to Commensurability Between the Vortex Lattice in a Niobium Film and an Underlying Self Assembled Periodic Magnetic Quantum Dot Array: *Latika Menon*[1]; Hou Zeng[2]; Supriyo Bandyopadhyay[1]; [1]University of Nebraska, Dept. of Electl. Eng., Lincoln, NE 68588-0511 USA; [2]University of Nebraska, Dept. of Phys., Ctr. for Matls. Rsch. & Analysis, Lincoln, NE 68588-0111 USA

The interaction between the Abrikosov vortex lattice in a superconducting thin film and an underlying ordered array of quantum dots (that act as localized pinning sites) can lead to novel pinning effects. The vortex lattice is a hexagonal close packed lattice and we have self assembled a hexagonal close packed array of magnetic quantum dots by electrodepositing nickel into a porous alumite film produced by anodization of aluminum. A 100 nm thin film of niobium was then sputtered on top. The anodization conditions were chosen to create Ni quantum dots of either 50 nm diameter or 200 nm diameter (with less than 1% size dispersion). The interdot separation was also either 100 nm or 200 nm, which are comparable to the coherence length of Nb just under the transition temperature. The magnetization of the superconducting film was measured in a SQUID as a function of an external magnetic field and showed a series of periodically spaced peaks corresponding to the critical fields at which the vortex lattice becomes commensurate with the quantum dot lattice (i.e. an integer number of vortices fit within a period of the quantum dot lattice). At these fields, the magnetization reaches a maximum because of a synchronized flux pinning effect in the superconductor caused by the Ni dots.

4:40 PM

J5, Cl2/Ar/H2-Inductively-Coupled-Plasma-Reactive Ion Etching of InP/InGaAsP Nanostructures: *Sean L. Rommel*[1]; Wu Lu[1]; Gabriel Cueva[1]; Ling Zhou[1]; Gary Pajer[2]; Joseph H. Abeles[2]; Ilesanmi Adesida[1]; [1]University of Illinois at Urbana-Champaign, Dept. of Electl. & Comp. Eng., 208 N. Wright St., 303 Microelect. Lab., Urbana, IL 61801 USA; [2]Sarnoff Corporation, 201 Washington Rd., Princeton, NJ 08543-5300 USA

Optoelectronic devices require etching processes which result in low damage, anisotropic etch profiles. For nanoscale devices, such as ring resonators, the fabrication requirements are quite stringent. These structures consist of a sub-micron waveguide coupled via a narrow air gap (often between 0.2 and 0.25 µm) to a resonating ring. Few groups have investigated these structures in InP-based systems largely because of difficulty achieving these profiles. Due to their high plasma densities, inductively-coupled-plasma reactive ion etching (ICP-RIE) plasmas result in high ion flux with low energies, minimizing etch damage while maintaining high etch rates. Therefore, they are ideal candidates for optoelectronic device processing. In this study, a Cl_2Ar/H2 ICP-RIE chemistry was used to etch InP-based waveguide structures. A 330 nm thick Si3N4 layer served as the etch mask. Sub-micron lines of varying widths patterned by electron beam lithography were transferred to the underlying Si3N4 mask via an SF6 plasma. The samples were etched in a PlasmaTherm SLR 770 ICP-RIE system. First, a study was performed to optimize the Cl2/Ar plasma conditions. These conditions, which were fixed to study the influence of H2, were found to occur with an RF power of 110 W, an inductive coil power of 900 W, a D.C. induced bias of 215 V, 1.5 mT, a Cl2/Ar ratio of 2/3 and 225°C substrate temperature. The details of this process optimization will be published elsewhere. The resulting etch profile exhibited a 0.25 µ/m undercut. Adding H2 to the etch was found to minimize this undercut. It is believed that the H2 reacts with the Cl2 thereby reducing the total number of chemically active Cl2 species. As H2 is added to the chemistry, the etch rate drastically decreases with concentration from 1.8 to 0.5 µ/m/min for Cl2/Ar/H2 ratios between 2/3/0 and 2/3/1.5. Optimal etching conditions appear to occur near the minimum etch rate. The most anisotropic profile occurs for a Cl2/Ar/H2 ratio of 2/3/2. Beyond this point, the supply of H2 begins to exceed the Cl_2 flow. The etch rate, therefore, begins to increase as the available H_2 increases, dominating the etch. Interestingly, the addition of H_2 causes InP and InGaAsP/InGaAs epitaxial layers to etch at different rates. For example, in layers etched with a $Cl_2/Ar/H_2$ ratio of 2/3/3, the InP layers exhibit large undercuts, whereas the InGaAsP/InGaAs layers show little lateral etching. As the H_2 concentration is increased, this difference becomes more apparent. InP layers are almost completely eroded due to lateral etching, whereas the InGaAsP layers act as a shadow mask to the underlying InP layers. This new etch process enables the fabrication of several previously unrealizable InP-based devices.

Session K: Contact to Wide Bandgap Semiconductors – II

Wednesday PM Room: 141
June 27, 2001 Location: University of Notre Dame

Session Chairs: Suzanne Mohney, Pennsylvania State University, University Park, PA 16802 USA; Tae-Yeon Seong, Kwangju Institute of Science & Technology, Semicond. Thin Film Lab., Puk-gu, Kwangju 500-712 Korea

1:20 PM

K1, Correlation Between I-V Characteristics and Dislocations for Au/Ni/n-GaN Schottky Contacts: *Kenji Shiojima*[1]; Tetsuya Suemitsu[1]; Mitsumasa Ogura[2]; [1]NTT, Photonics Labs., 3-1 Morinosato Wakamiya, Atsugi, Kanagawa 243-0198 Japan; [2]Kyoto University, Dept. of Matl. Sci. & Eng., Yoshidahon-machi, Sakyou-ku, Kyoto 606-8501 Japan

We have directly evaluated the effect of dislocations on the current-voltage (I-V) characteristics of n-GaN Schottky contacts. The key feature of our measurements is the combination of sub-micrometer contact formation by electron beam (EB) lithography and precise I-V measurements by atomic force microscopy (AFM) with a conductive probe. The Si-doped n-type GaN film was grown on an (0001) sapphire substrate in an MOCVD reactor. The electron concentration was $3x10^{17}$ cm^{-3}, and the mixed dislocation density was about $3x10^{8}$ cm^{-2}. Planar-type Schottky contacts were formed by the lift-off process. First, a Ti/Al ohmic contact with a large area was deposited, and then the sample was subjected to rapid thermal annealing at 800°C for 30 s. An array of Ni/Au circular Schottky contacts 0.5 µm in diameter with a period of 10 µm was formed on n-GaN by using EB lithography. A conductive AFM probe was put on each contact and I-V measurements were conducted for 18 c ontacts adjacent to one another. All showed good linearity in forward I-V, and the Schottky barrier height (SBH) and n-value were 0.823~0.843 eV and 1.15~1.20, respectively. The reverse current at -10 V was as low as 0.5~5 pA. The diode-to-diode variation of the current level was less than one order of magnitude. After the I-V measurements, the samples were soaked in acid solution to remove all metal contacts, and then AFM images of the GaN surface where the Ni/Au Schottky contacts used to be were taken. The marks of the array can be seen, but the height is only ~0.3 nm, and the surface morphology of steps and dark spots, which indicate mixed dislocations, is preserved. These marks can tell us where the diode contains mixed dislocations as well as the shape of the steps crossing the diode. Actually, most of the diodes contain one dislocation or none at all. From the obtained correlation between I-V characteristics and the number of mixed dislocations and total length of the steps in each dot, we found that neither dislocations nor steps affect the I-V. This suggested that a mixed dislocation would not act as a pico-ampere-order leakage path. It is likely that the depleted areas along mixed dislocations do not contribute to current conduction for Schottky contacts, i.e., the actual area at the metal/semiconductor interface could be reduced. In our experimental condition, the diameter of the depleted area, which is determined by both the electron concentration in GaN and the energy position of the mixed dislocations at the interface, might be negligibly small. These results indicate that, in fabricating short-gate FETs, gate Schottky contacts containing dislocations should not be considered a problem with respect to uniformity and reproducibility.

1:40 PM

K2, Characterization of Metal/p-GaN Schottky Interfaces by I-V-T Measurements: *Takayuki Sawada*[1]; Kazuaki Imai[1]; Kazuhiko Suzuki[1];

Naohito Kimura[1]; Yuji Ito[1]; Yusuke Izumi[1]; [1]Hokkaido Institute of Technology, Dept. of Appl. Elect., 7-15 Maeda, Teine-ku, Sapporo 006-8585 Japan

GaN-based compounds are attractive for applications in high-temperature/high-power electronic devices as well as in short-wavelength optoelectronic devices. For advancement of the devices, better understanding of metal/GaN Schottky interfaces is required. Especially, little has been reported on electrical properties at metal/p-GaN Schottky interfaces. In this paper, electrical properties at metal/p-GaN interfaces are investigated by I-V-T and C-V measurements of the Schottky diodes, and are compared with those of metal/n-GaN interfaces. Mg-doped p-GaN (Mg=5.0×1018cm-3) and undoped n-GaN (ND =1.8×1017cm-3) wafers grown by MOCVD were used. After surface treatment using 1HCl:2H2O solution, Ni,Au,Ag were deposited by thermal evaporation to form metal/GaN Schottky structures. I-V-T and C-V measurements were performed in the wide temperature range of 150-600K. Previously, we have shown that peculiar I-V characteristics observed in n-GaN Schottky diodes, such as large discrepancies in the Schottky barrier height (SBH) between I-V and C-V measurements, scattered SBHs and Richardson constants, and inflected I-V curves, are well explained by a leakage current arising from 'surface patches' with low SBHs. Richardson plots together with temperature dependence of the effective SBHs and ideality factors can be well reproduced using the model. The fraction of the total patchy area of 10-5 effectively reduce the SBH at RT, while it does not affect the flat-band SBH deduced from C-V curves. Surface defects with different chemical compositions are likely the origin of the patches. I-V-T characteristics of Au,Ni,Al/p-GaN Schottky diodes were measured for the first time. Relatively large ideality factors, being typically 1.6-2.5 at RT, for p-GaN samples seem again due to leakage current arising from 'surface patches'. Tunneling current may be also concerned because of a high Mg-doped wafer. It is found that the linearity of I-V curve improves with increasing the temperature and the effective SBH considerably increases: e.g. from 0.97 eV at RT to 1.72 eV at 600K for Au/p-GaN sample. Moreover, the effective SBH measured at 600 K becomes close to the SBH deduced from the Richardson plot, indicating the true SBH can be obtained at high-temperatures. These observations can be explained by shrunken influence of the leakage current at high-temperatures. A relatively large variation of the effective SBH with temperature seems to indicate the inhomogeneity of the M/S interface is worse for p-GaN samples. The sum of the effective SBHs for n- and p-GaN samples with a same contact metal is close to the GaN band gap at high-temperatures, while the sum is considerably smaller than the band gap at RT. Furthermore, it is found that the true SBH is weakly dependent on the metal work function with small S-value of about 0.2, and the interface Fermi level tends to be pinned at a characteristic energy level, being about two-third of the band gap.

2:00 PM (Student)

K3, Thermal and Environmental Aging of the Au/Ni/p-GaN Ohmic Contact Annealed in Air: *Sammy H. Wang*[1]; Suzanne E. Mohney[1]; [1]Pennsylvania State University, Dept. of Matls. Sci. & Eng., 218 Steidle Bldg., University Park, PA 16802 USA

In recent years, significant advances have been made in achieving low resistance ohmic contacts to p-GaN. We have compared 17 different contact metallizations, some reported in the literature and some developed in our own laboratory. Among the contacts we tested, we found that Au/Ni/p-GaN contacts annealed in air consistently provided the lowest specific contact resistance, but only when layer thicknesses of 10 nm were used for both metal layers. The specific contact resistance was as low as $4x10^{-4}$ ohm-cm^2, depending on the source of p-GaN we used. We will briefly review these results, but then we will focus on the environmental and thermal degradation that we observed in the Au/Ni/p-GaN contacts. When the contacts were not protected from the environment, degradation of the contacts always occurred over a period of days, and after 30 days in the laboratory at room temperature, the I-V curves of the originally ohmic contacts became non-linear, and the resistance due to the contacts ma rkedly increased. In order to pinpoint the degradation mechanism, we stored samples in ultra high pure (UHP) nitrogen, UHP oxygen, nitrogen gas saturated with water vapor, and vacuum at both room temperature for 1 day. We also stored samples for 15 days at room temperature suspended above water in a sealed container as well as in a sealed container containing the sample supported above a desiccant. The experiments conducted at room temperature revealed that water vapor was clearly the cause of the room temperature degradation, and the contacts must be passivated from the environment with a barrier to water vapor to protect them from this effect. Additional experiments are underway to determine if repassivation of the p-GaN occurs, or if there is a detrimental interaction between water vapor and the NiO present in the contacts after they are annealed in air. The aging studies at 200°C further revealed poor thermal stability of the contacts not only in water vapor but also in nitrogen gas and vacuum. Howe ver, the electrical characteristics of the contacts that degraded in vacuum could be recovered if the contacts were annealed again in air at 550°C for 10 minutes (the original annealing condition used for fabricating the ohmic contacts). We are currently performing materials characterization to understand what occurs in the contacts when annealed at 200°C and believe that changes in the p-type semiconductor NiO present in the annealed contact metallization are likely involved.

2:20 PM (Student)

K4, Low Resistance Pd/Ru Ohmic Contacts to p-GaN: *Ja-Soon Jang*[1]; Chang-Won Lee[1]; Seong-Ju Park[1]; Tae-Yeon Seong[1]; [1]Kwangju Institute of Science and Technology, Dept. of Matl. Sci. & Eng., 1 Oryong-dong, Puk-ku, Kwangju 500-712 Korea

Due to the successful development of GaN based devices, such as blue LEDs and LDs, the fabrication of high quality ohmic contacts with low resistance and thermal stability is of great technological importance. For ohmic contacts to p-GaN, however, there are two main obstacles, namely, i) a difficulty in growing p-GaN with a carrier concentration in excess of 10^{18} cm^{-3}; ii) the absence of appropriate metals having work function larger than that of p-GaN (6.5 eV). In our previous work, two-step surface treatment was introduced to overcome these problems (and hence, to improve the electrical properties of p-ohmic contacts). Until now, most of metallization schemes for p-GaN have been reported to Au-based schemes such as Ni/Au, Pd/Au, Ni/Pt/Au, and Pt/Ni/Au. However, Au-based contacts generally have poor thermal stability, leading to poor device reliability. In this work, we investigate Pd/Ru schemes for the formation of low resistance and thermally stable ohmic contacts to p-GaN:Mg (Na = ~$3x10^{17}$ cm^{-3}), which was two-step surface-treated using buffered oxide etch (BOE) solution. The I-V measurements show that annealing at 500°C for 2 min in a N_2 ambient improves the I-V characteristics of the Pd/Ru contacts. For example, specific contact resistance (which was measured using the TLM method) is $9.2x10^{-4}$ and $3.1x10^{-5}$ Ωcm^2 for the as-deposited and annealed contact, respectively. It is also shown that annealing results in a reduction (by ~70 meV) in the Schottky barrier heights of the Pd/Ru contacts, compared to the as-deposited ones. The C-V measurements show that the energy band bending behavior of the contacts is dependent on annealing treatment. Post-deposition annealing treatment is performed to investigate the thermal stability of the surface-treated contacts. To understand ohmic mechanisms, electronic transport mechanisms and interfacial reactions are investigated using current-voltage-temperature (I-V-T) measurements, Auger electron spectroscopy and glancing X-ray diffraction.

2:40 PM (Student)

K5, $TiAl_3$-Based Contacts to n-GaN: *Christopher M. Pelto*[1]; Y. A. Chang[1]; Yong Chen[2]; R. Stanley Williams[2]; [1]University of Wisconsin–Madison, Matls. Sci. Prog., 1509 University Ave., Madison, WI 53716 USA; [2]Hewlett-Packard Laboratories, 3500 Deer Creek Rd., 26U, Palo Alto, CA 94304 USA

We have measured the electrical properties of the standard bilayer Ti/Al contact to n-GaN and related them to some more novel contact systems involving $TiAl_3$. Researchers have found that the most common Ti/Al multilayer structure, with a Ti:Al ratio of approximately 1:3, often consists almost entirely of the single phase $TiAl_3$ following thermal treatment. It is not known why exactly Ti and Al are particularly good at forming an ohmic contact to n-GaN, because the kinetics of the reactions occurring in the Ti/Al/GaN structure are very complex and rather poorly understood at present. We employ the $TiAl_3$-based metallization schemes to help determine the specific role that the Ti and Al layers play in the operative ohmic contact mechanism of the multilayer Ti/Al-based contacts. I-V curves and specific contact resistances (ρ_c) were obtained for $TiAl_3$, $Ti/TiAl_3$, and $TiAl_3/Al/TiAl_3$ contacts and then compared to a Ti/Al contact processed on the same substrate. None of these $TiAl_3$ contacts perform as well as the Ti/Al standard. The best ρ_c value obtained for the $TiAl_3$ contact was 1.3E-4 Ω cm^2, compared to 3.8E-5 Ω cm^2 for the Ti/Al (25 nm/85 nm). Also interesting is the trend of the ρ_c values as

the annealing temperature is increased, since the $TiAl_3$ contact did not achieve this best ρ_c until a temperature of 1000°C, while the Ti/Al contact achieved a lowest ρ_c value at a more reasonable 700°C. Auger depth profiling was used as an initial means of characterizing the structure of the various contacts. The results of this study indicate that the reaction between the Ti and Al layers plays a very important role in the resultant success of the ohmic contact. The poor performance of the $Ti/TiAl_3$ contact, in particular, suggests that the role of the Ti is possibly more complex than once believed, since it seems to do more than simply penetrate the surface of the semiconductor.

3:00 PM Break

3:20 PM (Student)

K6, Characterization of Schottky Contacts on n-Type AlxGa1-xN: *L. Zhou*[1]; N. G. Kim[1]; F. A. Khan[1]; E. Piner[2]; I. Adesida[1]; [1]University of Illinois, Microelect. Lab., 128 N. Wright St., Urbana, IL 61801 USA; [2]ATMI/Epitronics, Phoenix, AZ 85027 USA

The study of Schottky contacts on AlxGa1-xN is of great importance for high power and high temperature heterostructure field effect transistors (HFETs) and photodetectors operating in the ultra-violet (UV) spectrum. For these devices, metals are needed which form high barrier heights and are stable at elevated temperatures. Schottky barrier heights of a variety of metals (i.e. Ni, Au) to n-type GaN have been studied extensively by many authors. However, there have been only a few papers published on Schottky contacts on different compositions of n-type AlGaN. In this paper, we report on a systematic study of contacts formed by eight metals (Au, Co, Cu, Ni, Pd, Pt, Re and Ta) deposited on n-AlxGa1-xN (x=0, 0.1, 0.15 and 0.2). Three measurement techniques: current-voltage, capacitance-voltage and modified Norde plot (current-voltage-temperature technique) were used to characterize the effective barrier heights formed by these contacts. We found that the abnormally low values of Richardson's constant sometim es reported in the literature were partly due to high series resistances being ignored in the calculation. The series resistance in our work generally increased with increasing Al fraction, from about 50 Ω to an average of about 1500 Ω for Al0.2Ga0.8N. High series resistances skewed the barrier heights measured using the capacitance-voltage (C-V) technique toward higher values when the measurement frequency was kept at 1 Mhz for all AlxGa1-xN compositions. Therefore, multi-frequency C-V measurements were performed and the values at 40 kHz were used for barrier height calculation. Furthermore, our results failed to show a linear correlation between the metal work function and the effective barrier height on AlxGa1-xN, with Au exhibiting the highest barrier height on Al0.2Ga0.8N rather than Pt, which has a higher work function. X-ray photoelectron spectroscopy (XPS) is used to study the impact of surface preparation on AlxGa1-xN surface band bending and the contact potentials.

3:40 PM

K7, Ohmic Contacts to AlGaN with High Al Content: *Suzanne E. Mohney*[1]; Kasper O. Schweitz[1]; Brett A. Hull[1]; Eric D. Readinger[1]; [1]Pennsylvania State University, Dept. of Matls. Sci. & Eng., 109 Steidle Bldg., University Park, PA 16827 USA

As the group III nitride semiconductor technology matures, an increasing number of devices are being fabricated from AlGaN with a high fraction of Al. In this presentation, we describe our work on ohmic contacts to both n-type and p-type $Al_xGa_{1-x}N$ with x greater than or equal to 0.4. For n-type AlGaN, we find increasingly higher specific contact resistances with increasing Al fraction. For Ti/Al/Pt/Au contacts, for example, we measure a minimum specific contact resistance of 7×10^{-6} ohm-cm^2 when x = 0.4, and if we adjust the layer thicknesses to achieve a contact with improved edge definition, we obtain a somewhat higher specific contact resistance of 2×10^{-4} ohm-cm^2. On the other hand, if we use these adjusted layer thicknesses on AlGaN with x = 0.6, we obtain a specific contact resistance of 1×10^{-2} ohm-cm^2, nearly two orders of magnitude higher, even though the carrier concentrations are near 10^{18} cm^{-3} in both AlGaN epilayers. A comparison is also made between this contact and other contacts that have been developed in our laboratory or reported in the literature, and the role of Au in the ohmic contact formation is highlighted. Somewhat to our surprise, ohmic contacts to p-$Al_{0.4}Ga_{0.6}N$ with linear I-V curves have been readily achieved using both Ni/Pt and Ni/Au contacts. Higher annealing temperatures than are typically used for ohmic contacts to p-GaN are required, with both contacts exhibiting linear I-V curves after they are annealed at 700°C or higher. Unfortunately, an extreme environmental sensitivity is observed, with degradation occurring at room temperature just minutes after the contacts are annealed. This sensitivity is similar to our previous findings on the reverse leakage currents of Schottky contacts to n-$Al_{0.17}Ga_{0.83}N$, in which reverse currents dropped by orders of magnitude with storage in air over a period of hours or d ays. In the case of the Schottky contacts to n-AlGaN, the change was clearly correlated with the storage environment and was not linked to illumination or prior electrical characterization history. The high reverse leakage currents before aging scaled with the area of the contacts, and the time dependence of the reverse leakage current was correlated with the thickness of the metal contact layers. We will determine if this same dependence exists for the degradation of the ohmic contacts to p-AlGaN, which would suggest that permeation of gases through the contact metal to the metal/semiconductor interface plays an important role in the changing electrical characteristics of the contacts.

4:00 PM (Student)

K8, Microstructural Analysis of Ti/Al/Ti/Au Ohmic Contacts to n-AlGaN/GaN: *Jiang Chen*[1]; Douglas G. Ivey[1]; Jennifer Bardwell[2]; H. Tang[2]; J. B. Webb[2]; Y. Liu[2]; [1]University of Alberta, Dept. of Chem. & Matls. Eng., 536 Chemical & Materials Engineering Bldg., Edmonton, Alberta T6G 2G6 Canada; [2]National Research Council of Canada (NRC), Inst. for Microstruct. Sci., Ottawa, Ontario K1A 0R6 Canada

Wide band gap GaN-based semiconductors are attracting increasing interest from both materials and electrical engineers/scientists because of their potential for use in blue and UV wavelength optical devices and high power, high temperature and high frequency electronic devices. To develop such devices, thermally stable, low resistance ohmic contacts with good surface morphologies are essential. Ti/Al-based metallizations have become the ohmic contact of choice for n-type materials. A low resistance variation to this contact, i.e., Ti/Al/Ti/Au, was recently reported for high speed, high power AlGaN/GaN heterojunction field effect transistors (HFET)[1]; however, no microstructural analysis has been done as yet. In this paper, high quality ohmic contacts with specific contact resistances as low as 6.33×10^{-6} ohm cm^2 are reported, using a Ti (30 nm)/Al (80 nm)/Ti (120 nm)/Au (55 nm) metallization scheme. The low resistance is achieved by rapid thermal annealing (RTA) after deposition at 700°C for 30s. All samples were examined using transmission electron microscopy (TEM); electron diffraction and energy dispersive x-ray (EDX) spectroscopy were employed to identify phases that had formed during annealing. Both cross section and plan view specimens were prepared for microstructural analysis. Cross section specimens were prepared either by wedge polishing followed by ion milling or focused ion beam (FIB) techniques. The individual metallization layers remained distinct until about 400°C, after which significant interdiffusion between layers occurred resulting in phase changes. These reactions will be reported and correlated to changes in electrical properties. [1]K. K. Chu, M. J. Murphy, J. Burm, W. J. Schaff, and L. F. Eastman, IEEE Proceedings, IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, 1997, pp 399-406.

4:20 PM, K9, Late News

4:40 PM, K10, Late News

Session L: III-N Growth

Wednesday PM Room: 155
June 27, 2001 Location: University of Notre Dame

Session Chairs: Russell D. Dupuis, University of Texas, Austin, TX 78712-1100 USA; Joan Redwing, Pennsylvania State University, University Park, PA 16802-5006 USA

1:20 PM (Student)

L1, Growth of InN by Molecular Beam Epitaxy: *Hai Lu*[1]; William J. Schaff[1]; Lester F. Eastman[1]; [1]Cornell University, Electl. & Comp. Eng., 429 Phillips Hall, Ithaca, NY 14853 USA

Indium nitride is expected to be used for fabrication of high-performance high electron mobility transistor (HEMT), since it will have higher peak-drift velocity and higher peak overshoot velocity than GaN, larger breakdown electric field and wider band gap than GaAs. In addition to spontaneous polarization, the significant lattice mismatch between InN and GaN or AlN can result in a large piezo-electric charge, for undoped HEMT applications. In this work, we prepared epitaxial InN on (0001) sapphire with an AlN buffer layer by molecular beam epitaxy (MBE) with the migration enhanced epitaxy (MEE) technique, which is composed of an alternative supply of pure In atoms and nitrogen plasma. A series of samples were grown with different substrate temperatures ranging from 360°C to 590°C. As grown films were characterized by x-ray diffraction, reflective high-energy electron diffraction, atomic-force microscopy and Hall measurements. The optimum growth temperature for InN was found to be between 450°C and 500°C. The effect of InN thickness on Hall mobility was investigated and comparison with published results obtained by metalorgainic chemical vapor deposition is made. It is revealed that InN with higher Hall mobility can be obtained by increasing the epilayer thickness, which is explained by the reduced defect densities away from the lattice mismatched substrate. We also found that using AlN buffer layer can significantly improve the structural and electrical properties of the following InN epilayer. With increasing the thickness of AlN buffer layer, the electron Hall mobility of according InN nearly continuously increases while the carrier concentration decreases. The surface morphology is also improved this way. Hall mobility more than 900 cm2/Vs with carrier concentration ~2e18 cm-3 at room temperature was achieved in this study. More importantly, it is found that under optimum growth condition, InN films grown on AlN buffer by conventional MBE technique can show comparable electrical properties as those films prepared by migration enhanced epitaxy. This fact makes it possible to grow high quality InN epilayer with much higher growth rate. Various InN-based heterostructures with AlInN or AlN barrier were fabricated. X-ray diffraction study clearly shows the formation of heterojunctions. Two-dimensional electron gas resulted from piezo-electric effect was observed in CV measurements for the first time. Some results on Mg doping of InN and growth of AlInN will be discussed as well.

1:40 PM (Student)

L2, Properties of High-Quality AlGaN/GaN Superlattices Grown by Metalorganic Chemical Vapor Deposition: *Uttiya Chowdhury*[1]; Michael M. Wong[1]; Ki Soo Kim[1]; Jonathan C. Denyszyn[1]; Tinggang Zhu[1]; Russell D. Dupuis[1]; [1]The University of Texas at Austin, Microelect. Rsrch. Ctr., 10100 Burnet Rd., Bldg. 160, Austin, TX 78758 USA

Many important system applications require high-efficiency compact short-wavelength UV light sources in the 280-350nm-wavelength regime. For example, compact spectrometers coupled with UV light sources can be used to detect various biological chemicals using laser-induced fluorescence. Also, high-efficiency UV light sources could be used in combination with various phosphors for lighting applications. For UV-emitting lasers and light-emitting diodes, AlGaN/GaN quantum-well and superlattice active regions are expected to provide the necessary performance. We report growth of high-quality AlGaN/GaN superlattices (SLs) by low-pressure metalorganic chemical vapor deposition (MOCVD). The SLs were grown heteroepitaxially on (0001) sapphire and 6H-SiC substrates in an EMCORE D125 UTM rotating disk reactor. The precursors used are adduct-purified trimethylgallium (TMGa), trimethylaluminum (TMAl), silane (SiH_4) and ammonia (NH_3). The epitaxial layers were grown in a H_2 ambient at 50-200 Torr. A two-step growth process beginning with GaN low-temperature buffer layer was used and the high temperature GaN and AlGaN layers were grown at ~1030C. The superlattice heterostructures (SLHs) consisted of ~0.5µm $Al_xGa_{1-x}N$ cladding regions and $Al_yGa_{1-y}N$/GaN SLs. The superlattice layer thicknesses were varied from GaN(2nm)/AlGaN(2nm) to GaN(5nm)/AlGaN(5nm) and number of periods was varied from 2 to 40. Comparison with conventional AlGaN/GaN two and three-quantum-well samples was also made. The cracking commonly observed for thick AlGaN layers grown on GaN complicates the growth of SLH active regions. We have solved this problem through the use of various buffer layer structures that permit us to optimize the SL growth on sapphire and SiC substrates. The structural properties of the SLHs were studied using triple-axis X-ray diffraction and reciprocal space mapping (RSM) combined with dynamical diffraction simulations. The intensity and full-width at half maximum (FWHM) of these SL X-ray peaks are dependent upon the growth conditions. Symmetric (004) and (002) X-ray diffraction data show superlattice-related peaks for all the samples that agree closely with the expected superlattice period. RSM shows that the AlGaN films and SLs are "coherent" and unrelaxed. The luminescence properties of the samples were studied at 300K and 4K. The 4K photoluminescence (PL) and cathodoluminescence (CL) data show bright peaks with narrow FWHMs (~6nm) at wavelengths as short as 321nm related to the bound state in the SL. The wavelengths of the primary SL peaks obtained from 300K and 4K PL and CL data correspond well with expected emission energies. The 4K time-resolved PL data show very long carrier lifetimes ~720ps in these SLH samples. The effect of growth pressure, growth interruption time at interfaces, and Si dopant concentration on material quality was compared using data from X-ray diffraction, surface roughness measurement by atomic force microscopy (AFM), secondary ion mass spectroscopy (SIMS), PL, and CL measurements. Further, interface abruptness and dislocation density was investigated using transmission electron microscopy. The results of these studies will be reported.

2:00 PM (Student)

L3, Growth and Characterization of AlN/GaN Heterostructures Using Low-Pressure Organometallic Vapor Phase Epitaxy: *Seth Martin Hubbard*[1]; Dimitris Pavlidis[1]; Viktor Valiaev[1]; Andreas Eisenbach[1]; [1]University of Michigan, Solid State Elect. Lab., 2312 EECS Bldg., 1301 Beal Ave., Ann Arbor, MI 48109 USA

Recently, III-Nitride based MODFET devices have shown great promise for high-frequency/high-power applications. For the most part, these devices are based on AlGaN/GaN type heterostructures. However, because AlN is expected to be a good insulating material with high dielectric constant, there exists the possibility of using an AlN/GaN system to create metal-insulator-semiconductor field effect transistors (MISFETs). Unfortunately, there is a large lattice mismatch between AlN and GaN. From the growth standpoint, we are challenged to grow both high quality AlN and GaN epilayers, which also exhibit good electronic properties. Low-pressure Organometallic Vapor Phase Epitaxity (OMVPE) is used to grow AlN/GaN MIS-type heterostructures. Grazing Incidence X-Ray Reflectivity (GIXRR) was used to calibrate the AlN growth rate as a function of reactor pressure. In addition, X-Ray Diffraction and Atomic Force Microscopy were used to verify GaN and AlN material quality and surface morphology. Structures were grown with AlN thickness between 30 Å and 350 Å. AFM scans show the AlN is growing in a 3-D island growth mode often seen for III-nitride materials with high Al composition. Surfaces of these samples exhibit defects 100-200 nm in size propagating out from dislocations in the underlying GaN channel layer. However, these defects are seen to decrease in size and density for very thin AlN layers, indicating the presence of an initial AlN wetting layer before the formation of defects. Van der Pauw Hall-effect measurements were performed on our samples at temperatures ranging from 20K to 300K. As the AlN thickness was increased, the 2DEG sheet carrier concentration increased and Hall mobility decreased. The decrease in electron mobility with increasing AlN thickness is related to strain relaxation at the interface and increased interface scattering. The optimal AlN thickness was found to be approximately 50 Å. The measured room temperature and 20K mobilities for this sample were 980 cm^2/Vs (n_s=8.14x10^{12} cm^{-2}) and 3230 cm^2/Vs (n_s=7.76x10^{12} cm^{-2}), respectively. To our knowl-

edge, this is the best reported mobility for OMVPE grown AlN/GaN MIS structures. Work supported by ONR (contract no. N00014-92-J-1552 and N00014-00-1-0879).

2:20 PM

L4, Growth and Characterization of Epitaxial AlGaN/GaN on Single-Crystal Aluminum Nitride Substrates: *Leo J. Schowalter*[1]; J. Carlos Rojo[1]; Remis Gaska[2]; Michael Shur[2]; J. Yang[3]; Asif Khan[3]; [1]Crystal IS, 25 Cord Dr., Latham, NY 12110 USA; [2]Sensor Electronic Technology, Latham, NY 12110 USA; [3]University of South Carolina, Electl. Eng. Dept., Columbia, SC 29208 USA

Aluminum nitride (AlN) has received attention as a candidate for III-nitride epitaxy applications due to its close lattice match, minimal differential thermal expansion compared to GaN, and high thermal conductivity. There is interest in AlN substrates as a competitive substrate for heteroepitaxial growth of GaN until commercial bulk GaN substrates become available. In addition, AlN is a more desirable substrate than GaN for device structures that require Al-rich nitride epitaxial layers such as solar-blind uv detectors and high power microwave devices. Since AlN is a very good electrical insulator, while having a higher thermal conductivity (>3 W/K-cm at room temperature), it is also very desirable for high power rf applications. Large (15mm diameter) AlN boules have been prepared using sublimation-recondensation growth. We have demonstrated the possibility of preparing substrates, cut from these boules, for epitaxial growth using chemical-mechanical polishing (CMP) techniques, although significant differences between the different crystallographic orientations have been observed. High quality epitaxial growth of III-nitrides has been demonstrated on "a-face" substrates and on the nitrogen (more reactive) face of "c-face" substrates for nearly on-axis substrates. When the nitrogen face of "off-axis" (more than 10°) c-face substrates were used, a rough surface morphology resulted even for AlN homoepitaxy. A two-dimensional-electron-gas (2º) structure was formed by growing a 30nm thick layer of $Al_{0.2}Ga_{0.8}N$ on top of a 0.5 µm thick intrinsic GaN layer on the AlN substrate by OMVPE. For the on-axis c-face, a sheet density of $8.5x10^{12}$ cm^{-2} and a mobility of 1000 cm^2/V-s has been measured at room temperature. The mobility increased to 2,200 at liquid nitrogen temperature while the sheet concentration remained constant. This is a very good indication of a true 2D electron gas and is the first such result reported for nitride growth on an AlN substrate.

2:40 PM

L5, Enhanced Ultraviolet Light Emission From Quaternary AlInGaN Grown by Atomic Layer Epitaxy: *Jianping Zhang*[1]; Edmundas Kuokstis[1]; Jinwei Yang[1]; Qhalid Fareed[1]; Grigory Simin[1]; Asif Khan[1]; Michael Shur[2]; Remis Gaska[2]; [1]University of South Carolina, Dept. of Electl. Eng., Columbia, SC 29208 USA; [2]SET, Inc., 21 Cavalier Way, Latham, NY 12110 USA

We report on Atomic Layer Epitaxy (ALE) of high quality quaternary AlInGaN materials for the development of high-efficiency ultraviolet light emitters. Our ALE technique is a modified MOCVD growth based on a modulation (pulse) flow of TMA, NH_3, TMIn, NH_3, TEG, and NH_3. A key advantage of this new technique is a significant reduction of the growth temperature for deposition of high aluminum content and high indium content AlInGaN materials and quantum well structures. ALE also allows for extremely efficient control of the growth rate, layer thickness and composition, which is crucial for the deposition of high quality multiple quantum well structures with abrupt heterointerfaces. Ultraviolet light emitters (λ < 300 nm) require materials with the band gap of 4 eV and higher, which correspond to a high Al content AlGaN alloys. Due to lattice mismatch with GaN and poor quality of such ternary compounds, the intensity of photo- and electro- luminescence is known to decrease rapidly with increase of Al fraction. Recently we proposed a new approach to the problem based on the use quaternary AlInGaN materials. This approach proved to decrease the lattice mismatch with GaN and improve significantly both the surface morphology of the epilayers and the luminescence intensity. The limitations on using quaternary materials for UV light emitters come from the difficulties of incorporating both high fractions of Al and In during regular MOCVD growth. Our new approach to low temperature ALE grown quaternary materials overcomes this problem. AlInGaN epitaxial layers were deposited on sapphire substrates at 740°C by repeating the hundreds of elementary growth steps, the sources (TMA, NH_3, TMIn, NH_3, TEG, NH_3) being alternatively turned on and off. We are able to obtain high quality, smooth surface and crack-free materials with aluminum and indium molar fractions up to 50% and 10%, respectively, Composition, structural quality, lattice constant and surface morphology of the samples were studied using Rutherford Backscattering Spectrometry (RBS), X-ray diffraction (XRD), and Atomic Force Microscopy (AFM). Room temperature photoluminescence of the samples was measured using pulsed nitrogen (337 nm) and excimer (193 nm) laser excitation. Our results show that ALE growth method has a great potential for the realization of deep UV light emitting devices. PL measurements demonstrate that our quaternary materials exhibit strong PL emission spanning from 270nm to 350 nm. The PL intensity does not decrease when the Al fraction increases in the quaternary material, in contrast to the conventional MOCVD-grown AlGaN. This implies our ALE-grown AlInGaN is more suitable for efficient UV to deep UV lighting sources.

3:00 PM Break

3:20 PM

L6, Cantilever Epitaxy and its Potential for GaN Substrates with Whole-Wafer Dislocation Densities Below 10^7/cm^2: *Carol I. H. Ashby*[1]; David M. Follstaedt[1]; Paula P. Provencio[1]; Nancy A. Missert[1]; Gregory M. Peake[1]; Leonardo Griego[1]; Christine C. Mitchell[1]; Jung Han[2]; Andrew A. Allerman[1]; [1]Sandia National Laboratories, MS 1425, PO Box 5800, Albuquerque, NM 87185-1425 USA; [2]Yale University, Electl. Eng., PO Box 208284, New Haven, CT 06520-8284 USA

The lack of an inexpensive whole-wafer substrate with low dislocation densities remains a serious impediment to the realization of high-performance microelectronic and optoelectronic devices in III-N materials systems. Cantilever epitaxy CE) is a single-growth alternative to conventional regrowth techniques, such as epitaxial lateral overgrowth (ELO) and pendeoepitaxy (PE), that can produce vertical threading dislocation (VTD) densities below 10^7/cm^2. The CE process consists of patterning a suitable substrate, such as sapphire, SiC, or Si, to provide a series of support posts. A coalesced film of III-N is then grown on the patterned substrate by varying growth conditions, such as temperature, during a single growth step to produce first predominately vertical growth and then more rapid lateral growth to form cantilever spans between the substrate support posts. The free-standing cantilevers are virtually free of VTDs (<10^6/cm^2) and the coalescence front between adjacent cantilevers displays few if any vertical dislocations when the initial predominantly vertical growth is performed to minimize VTD densities over the support regions. This can be achieved by selecting the proper ratio of support width to vertical growth thickness before initiating rapid lateral cantilever growth. These dimensions are selected to capitalize on the redirection of screw-component VTDs into horizontal threading dislocations (HTDs) that can occur at angled growth facets, such as the {1(1bar)01} and {11(2bar)2} family of planes. A screw-component VTD density of 2x10^6/cm^2 has been demonstrated using atomic force microscopy (AFM) over a 100-micrometer^2 area with a 1:4 support:cantilever areal ratio. A discussion of the types of substrate patterns and the growth conditions that lead to very low dislocation densities over the support posts will be presented. Characterization of the structural, optical, and electronic properties of low-dislocation-density CE wafers using AFM, transmission electron microscopy, cathodoluminescence, and Hall measurements will be presented. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under Contract DE-AC04-94AL85000.

3:40 PM

L7, Crystallographic Tilting in Pulsed Metalorganic Chemical Vapor Deposited GaN: *Qhalid Fareed*[1]; Jinwei Yang[1]; Jianping Zhang[1]; Durga Basak[1]; Asif Khan[1]; [1]University of South Carolina, Dept. of Electl. Eng., Columbia, SC 29208 USA

Progress in GaN-related wide band gap semiconductors has led to the successful production of blue/green light emitting diodes and ultra-violet laser diodes. Epitaxial lateral overgrowth (ELOG) of GaN used to reduce threading dislocation density in the epitaxy, has improved the performance and lifetime of these opto-electronic devices. In this growth method, dislocation density is reduced by 3 orders. Although, ELOG method serves to reduce TD density, an array of pure-edge dislocation appears at the coalescence sites and the mask edges. This is attributed to the crystallographic tilt in the wing region of the ELO GaN layer. This defects at the coalescence sites evidently create new dislocations are detrimental to the optical devices. In past we have reported on the pulsed ELOG procedure. This pulsed epitaxy approach allows ELOG at signifi-

cantly lower temperature. It also can be used to tailor the growth profile. This helps in controlling outdiffusion of impurities from mask material thereby improving electrical characteristics of the films. In this paper, we now report on the wing tilt in pulsed lateral overgrown GaN layers (PLOG) along different crystallographic axes. The measurements have been carried out using x-ray diffraction (XRD), atomic force microscopy (AFM) and electron back-scattered diffraction (EBSD). Using x-ray rocking measurement along (0002) diffraction peak with line source, tilt angle was determined for different angle of incidence "w". It is observed that the degree of crystallographic tilt in the wing regions of lateral overgrown GaN increases with increase in azimuth angle "f" (rotation along surface normal). At f=90°, a single peak with the highest intensity is observed and it starts splitting to three peaks as azimuth angle is changed. Maximum splitting was observed at f=0 and f = 180° proving the maximum tilting in the sample. Full width half maximum (FWHM) of diffraction (0002) peak for different azimuth angle was also measured. The FWHM is minimum (0.07 degree) at the highest intensity peak i.e. at f = 90° and raises to a maxima (0.14 degree) at f = 0 and f = 180°. Crystallographic tilting measurement on coalesced and non-coalesced samples has also been carried out. It is found that the tilting decreases in the thick coalesced samples compared to thin non-coalesced lateral overgrown GaN. It confirms that the wing tilt may completely diminish or vanishes with increasing in film thickness. A comparative data on wing tilt measurement from X-ray diffraction with atomic force microscopy and electron-backscattered diffraction mapping will also be presented.

4:00 PM (Student)

L8, Epitaxial Lateral Overgrowth of GaN Layer on Si(111) Substrate: *Jeong Wook Lee*[1]; Sung Hoon Jung[1]; Sang Hak Lee[1]; Ji-Beom Yoo[1]; In Whan Lee[2]; Ok Hyun Nam[2]; [1]Sungkyunkwan University, Matls. Eng., 300 Chunchun-dong, Jangan-gu, Suwon, Kyunggi-do 440-746 Korea; [2]Samsung Advanced Institute of Technology, Photonics Lab., PO Box 111, Suwon, Kyunggi-do, Korea

Silicon substrates are of great interest as low-cost, large-area substrates for the growth of III-V nitride layers. But, it is very difficult to grow GaN film on Si substrate. Because of their large lattice mismatch between GaN and Si, the use of an intermediate layer or buffer layer is essential. Epitaxial lateral overgrowth is a promising method to achieve low defect GaN. Epitaxial lateral overgrowth (ELOG) is one of the promising methods for the high quality GaN as a fabrication of optical and electronic devices. In this study, we investigate the lateral overgrowth of GaN on Si(111) substrate by metalorganic chemical vapor phase deposition (MOCVD). The lateral overgrowth on Si(111) was carried after achieving high quality GaN template layer on Si(111). To obtain high quality GaN template layer the high-temperature AlN buffer layers were deposited on Si substrate by MOCVD. The TMAl, TMGa and ammonia were used as source gases, respectively. The growth temperature of AlN buffer layer and GaN template layer were changed range in 1020°C to 1100°C. ELOG GaN was grown at the temperature range in 800°C to 1100°C. The crystal orientation AlN buffer layer was very critical for the planar growth of GaN on Si substrate. In-plane and out-of-plane misorientations of AlN buffer layer were analyzed by transmission electron microscopy. The 2000Å thick SiO_2 film was deposited by PECVD for the use of ELOG mask. The stripe patterns were developed along <11-20 > and <1-100 > crystal axis of GaN. The various stripe windows with a different spacing between stripes were developed on the SiO_2 mask by conventional photolithography and wet chemical etching. The effect of growth parameters such as AlN buffer layer, GaN template layer, crystal orientation relationship between AlN and GaN, growth temperature, and stripe-patterned direction on lateral overgrowth of GaN were investigated. Surface roughness and morphologies of AlN buffer layer, GaN template layer and ELOG GaN film were analyzed by atomic force microscopy (AFM) and scanning electron microscope (SEM). The effect of intermediate layers on ELOG GaN was characterized by double crystal x-ray diffractometer (DCXRD), low temperature photo-luminescence (PL) and transmission electron microscope (TEM).

4:20 PM

L9, Al1-xSixN Ternary Alloy Epitaxial Growth and its Spontaneous Ridge Formation: *Makoto Kasu*[1]; Naoki Kobayashi[1]; [1]NTT Basic Research Laboratories, Phys. Sci. Lab., 3-1 Morinosato-Wakamiya, Atsugi, Kanagawa 243-0198 Japan

Interest in heavily Si-doped AlN is increasing, because the electron field emission from heavily Si-doped AlN increases drastically, as the Si density (N_{Si}) is increased. We have clearly observed that the lattice constants of the heavily Si-doped AlN epitaxial layers change with the N_{Si}. Further we have found spontaneous formation of ridge structures whose top widths were 3 nm. Heavily Si-doped AlN epitaxial layers were grown on on-axis 6H-SiC (0001) substrates by low-pressure (300 Torr) metalorganic vapor phase epitaxy. The sources were trimethylaluminum, SiH_4, and NH_3. The Al, Si, and N densities were measured by Auger electron spectroscopy (AES) and secondary ion mass spectrography. The full width at half maximum of the (0002) reflection peak of the X-ray rocking curves of heavily Si-doped and undoped 200 nm-thick AlN epitaxial layers ranged from 50 to 150 arcsec. These values are smaller than those previously reported for AlN growth. From AES, the Al density in the Si-doped AlN was found to be lower than that in the undoped AlN. The difference between the Al densities is equal to the N_{Si} in the Si-doped AlN. However, the N densities of Si-doped and undoped AlN were the same. This suggests that in Si-doped AlN the Si atoms exist at Al substitutional sites. Therefore, the heavily Si-doped AlN can be regarded as $Al_{1-x}Si_xN$ ternary alloy. The (0002) and (11-24) X-ray reflection angles shifted to higher angles as the N_{Si} increased. Thus, the lattice constants along the c and a axes of the heavily Si-doped AlN were smaller than those of the undoped AlN. This agrees with the fact that Si-N bond length is shorter than the Al-N bond length. From atomic force microscopy (AFM) observations, the undoped AlN surface was found to consist of monolayer steps and terraces. Some terrace widths exceeded 100 nm. This suggests that undoped AlN growth proceeds in the step-flow mode. In contrast, on the heavily Si-doped AlN surface, sharp ridge structures were observed. The ridge shape became obvious as the N_{Si} increased. On the heavily Si-doped AlN (N_{Si}: $1x10^{21}$ cm^{-3}) surface, the angle between the sidewalls and the (0001) face was about 61 degrees, and we determined that the sidewalls were {1-101} facets. From cross-sectional AFM images, the top widths were as low as 3 nm, whereas the base widths were about 100 nm. Thus the top of the ridges was sharp in a nanometer scale. From our calculations, the ridge formation decreases the energy barrier necessary for the field emission by about 2.4 eV compared with that for a planar surface. This is one of the reasons for the large field emission.

4:40 PM

L10, Growth and Characterization of InGaN/GaN Multi-Quantum Wells Selectively Grown on Hexagonal GaN Microstructures: *Chang-Hee Hong*[1]; Chi Sun Kim[1]; Young Kue Hong[1]; Min Hong Kim[2]; Hyung Jae Lee[1]; [1]Chonbuk National University, Semicond. Phys. Rsrch. Ctr., 664-14 Dukjin-Dong Dukjin-Gu, Chonju 561-756 Korea; [2]LG Electronics Institute of Technology, OE Team, Dev. & Matls. Lab., 16 Woomyeon-Dong Seocho-Gu, Seoul 137-140 Korea

Nanostructures of GaN-based materials such as quantum wells, wires and dots can be used to the realization of a novel optoelectronic device. Recently, InGaN quantum wires and dots grown on three-dimensional microstructures have been achieved using selective metalorganic chemical vapor deposition. It was found that changing the geometry of the mask and the GaN template films could control the growth behavior of nanostructures. Also, the spatial control of In incorporation in InGaN quantum structures have been reported. However, in order to achieve much higher performance optical devices and new functional devices with selectively grown nanostructures, understanding the growth mechanism and the characteristics of the grown layers will be one of the most important issues. In this work, blue InGaN/GaN multi-quantum wells (MQWs) were selectively grown on hexagonal GaN microstructures and characterized by photoluminescence(PL) and cathodoluminescence(CL) and transmission electron microscopy(TEM) measurements. At first, the growth of hexagonal GaN microstructures has been systematically investigated depending on the growth pressure, growth temperature and fill factor grown on 6 mm-size dot-patterned GaN(0001)/sapphire with 100nm-thick-SiO2 films. The results indicate that the shape of these microstructures is strongly related to the formation of the flat (0001) facet. Under relatively lower growth pressure and higher growth temperature, the growth behavior of (0001) surface is two-dimensionally changed and the self-limited (0001) facet is easily formed. After the first growth, blue InGaN/GaN MQWs were grown on those microstructures. CL and PL measurements were used to observe emission properties from (0001) and (1-101) facets. The results show that blue emission is obtained from both the flat (0001) facet and the six (1-101) facets whereas yellow luminescence is strongly observed from lateral overgrown regions through the six (1-101) side walls. This might be attributed to extended

crystal defects or the complex of Ga-vacancy with adventitious impurities from the mask. From an analysis of TEM images, gettering many defects such as threading dislocations in reverse pyramidal pits were found.

Session M: Advanced Gate Dielectrics – II

Wednesday PM Room: 138
June 27, 2001 Location: University of Notre Dame

Session Chairs: Pat Lenahan, Pennsylvania State University, University Park, PA 16802 USA; Laura Mirkarimi, Agilent Laboratories, Palo Alto, CA 94304 USA

1:20 PM Invited

M1, Si-Compatible Gate Dielectrics with High K, High Optical Bandgap, and Their Epitaxy on Silicon: *Darrell G. Schlom*[1]; [1]Pennsylvania State University, Matls. Sci. & Eng., 108 MRI Bldg., Research Park, University Park, PA 16803-6602 USA

The need for an alternative higher-K gate oxide for silicon MOSFETs has led us to compile a comprehensive list of multicomponent oxides that are likely to be thermodynamically stable in contact with silicon. Unfortunately, limited experimental data for the dielectric constant (K) and optical bandgap of many of these compounds exist, complicating the selection of the most suitable candidate for thin film growth. Using the floating zone and Czochralski crystal growth methods we have grown single crystals of many of these compounds and measured their dielectric constants and optical bandgaps. The result is 14 Si-compatible gate oxide materials with K > 20, of which at least 6 have an optical bandgap > 5 eV. Based on these experimental results, and other considerations such as lattice match with silicon, we have selected LaAlO3 as the most promising candidate for an alternative gate dielectric for silicon MOSFETs. Using an oxide molecular beam epitaxy (MBE) system, we have grown epitaxial thin films of LaAlO3 on (100) Si and Sr2TiO4 on (100) Si using ORNL's crystalline oxide on semiconductor (COS) process. Structural and electrical characterization of these films will be presented.

2:00 PM (Student)

M2, Measurement of the Optical Bandgap of High K Candidate Materials for MOSFETs by Far UV Ellipsometry: *Seung-Gu Lim*[1]; Thomas N. Jackson[1]; J. H. Haeni[2]; D. G. Schlom[2]; A. M. Balbashov[3]; R. Uecker[4]; J. L. Freeouf[5]; [1]The Pennsylvania State University, Ctr. for Thin Film Dev., 121 Electrical Engineering E., University Park, PA 16802 USA; [2]The Pennsylvania State University, Dept. of Matls. Sci. & Eng. USA; [3]Moscow Power Engineering Institute, Krasnokazarmennaya 14, Moscow 111250 Russia; [4]Institute of Crystal Growth, Rudower Chaussee 6, Berlin D-12489 Germany; [5]Interface Studies, Inc., 672 N.W. Autumn Creek Way # M202, Beaverton, OR 97006 USA

We have developed a far UV spectroscopic ellipsometer system working up to 9 eV and used it to characterize high-K dielectric materials. The basic setup of our far UV spectroscopic ellipsometer is that of a fixed polarizer and a rotating analyzer, as is typical for conventional ellipsometers. In order to avoid UV absorption by oxygen and its radicals below 190 nm, the main system was placed inside a glove box purged by nitrogen gas, and optical components were specially selected for UV use. We have applied this system to characterize high-K dielectric materials. Recently, high-K dielectrics have been gaining greater attention as a possible substitute for SiO2 for a gate dielectric material. Although SiO2 has been known as the best gate dielectric material on silicon (or anything else!), its low dielectric constant (K = 3.9) limits its use in transistors as gate lengths continue to shrink. Studies show that the device performance is basically limited by the tunneling-derived leakage current through the ultra thin gate oxide required for gate lengths below around 50 nm. Devices with high-K gate dielectrics can provide comparable device performance with a much thicker dielectric layer, thereby avoiding the tunneling-induced leakage current. In this study, we have investigated the optical properties of four prospective high-K dielectrics, HfO2, LaAlO3, GdScO3, and SmScO3 with far UV spectroscopic ellipsometry measurements and transmission measurements. Optical dielectric functions and optical band gaps of these materials are presented. Such information is needed both to select candidates with adequate band gaps for this application and to permit optical metrology of gate dielectric films on silicon. This work was supported by NSF SBIR grant.

2:20 PM

M3, Atomic Scale Chemistry and Structure of Alternative Gate Oxides: *Susanne Stemmer*[1]; Jon-Paul Maria[2]; Angus I. Kingon[1]; [1]Rice University, Mechl. Eng. & Matls. Sci., MS-321, 6100 Main St., Houston, TX 77005-1892 USA; [2]North Carolina State University, Matls. Sci. & Eng., 1010 Main Campus Dr., Raleigh, NC 27695-7919 USA

Two very important issues in replacing SiO2 by alternative gate oxides are the thermal stability of the alternative gate dielectric and the electrical quality of the interface. Metal oxides potentially thermally stable in contact with silicon include Al2O3, La2O3, and HfO2. However, the excellent electrical properties of the Si/SiO2 interface may not be achieved for the Si/high-k heterostructures. Using alloys (silicates) could potentially alleviate some of these problems. A possible approach of preserving the quality of the interface is to replace the direct deposition of alloys by a step-process consisting of oxidizing silicon, followed by deposition of a metal oxide and subsequent reaction to a silicate. Here, we investigate 2.5 nm thick La2O3 films reactively evaporated on oxidized silicon. MOS structures for electrical measurements were formed by evaporating Pt electrodes. The gate dielectric stacks were then subjected to post-deposition rapid thermal annealing treatments. We employ electron-energy loss spectroscopy (EELS) and high-resolution transmission electron microscopy (TEM) to investigate the chemistry and structure of alternative oxides. We use probe sizes sufficient for sub-0.2 nm spatial resolution in EELS, while simultaneously recording chemically sensitive atomic-resolution Z-contrast images that also serve to accurately position the probe for EELS. Using these techniques we analyze chemical reactions between SiO2 and La2O3, the crystallization behavior and the thermal stability of the stack as a function of annealing temperature on the atomic scale. At annealing temperatures of 600°C we find no interdiffusion between the layers and no evidence of crystallization. At higher temperatures we observe some rearrangement of atoms as exhibited by crystallization, changes in the near-edge fine structure of oxygen K-edges and stoichiometry changes, although no complete reaction to a silicate is observed even at the highest annealing temperatures (1000°C). We compare the chemistry of the gate dielectric stacks with their electrical properties and present a reaction model for the observed behavior.

2:40 PM (Student)

M4, Electrical and Structural Characteristics of Zirconium Oxynitride Prepared by Nitridation of Zirconium Oxide: *Sanghun Jeon*[1]; Hyunsang Hwang[1]; [1]Kwangju Institute of Science and Technology, Semicond. Integrated Dev. & Proc. Lab., Dept. of Matls. Sci. & Eng., Oryongdong 1, Puk-gu, Kwangju 500-712 Korea

We investigated thermally stable ZrO_xN_y with ~3-5 at.% nitrogen prepared by NH_3 annealing of ZrO_2. Ultra-thin zirconium oxide was deposited by radio frequency magnetron sputtering. Rapid thermal nitridation was performed in an atmosphere of NH_3 at 700°C. An additional wet oxidation was performed at various temperatures. Compared with sputtered ZrO_2, an abrupt increase of equivalent oxide thickness of nitrided ZrO_2 was retarded with annealing temperature(>700°C). High resolution transmission electron microscopy of ZrO_2 after 800°C anneal for 5 min. shows relatively thick thickness, and a polycrystalline phase, while that of nitrided ZrO_2 shows thin thickness, and amorphous phase. In addition, based on AFM analysis, the surface roughness of nitrided ZrO_2, and ZrO_2, was 2.3angstrom, and 5.3angstrom, respectively, which was attributed to the difference of phase such as atomically flat amorphous phase, and high curvature polycrystalline phase. As summarized, nitrogen in ZrO_2 prevents the crystallization, and the increase of physical thickness and surface roughness.

3:00 PM Break

3:20 PM Invited

M5, Materials Research for Alternate Gate Dielectrics: Challenges and Achievements: *J. Raynien Kwo*[1]; [1]Agere Systems, Rm. 1D232, 600 Mountain Ave., Murray Hill, NJ 07974 USA

Nanoscale device technology is stimulating intense study of very thin dielectric layers on semiconductors. The aggressive scaling of CMOS technology calls for identifying high ε dielectrics to replace SiO_2 gate oxides with a thickness approaching the quantum tunneling regime. This is not a sharp physical limit, but rather the point beyond which the leakage current due to tunneling (about 1-10 A/cm²) becomes the dominant leakage mechanism in current device designs. There is also a hard physical limit below which SiO_2 will no longer maintain its bulk electronic structure, and this appears to be about 7 Å. Replacing SiO_2 is a challenging task because the alternate gate dielectric must provide many properties that are, at a minimum, comparable to those of SiO_2 yet with a much higher permittivity. In the past three years a number of amorphous metal oxides and silicates have emerged and showed promising results. Advances in oxide epitaxy in a few laboratories have led to single crystal oxides grown on Si surfaces showing an abrupt interface. This talk will review the performance requirements for materials associated with CMOS scaling, the challenges associated with these requirements, and the state-of-the-art in current research for alternate gate dielectrics. In particular, we present the growth and properties of Gd_2O_3 (ε=14) and Y_2O_3 (//025 = 18) dielectric films by an approach of ultrahigh vacuum vapor deposition from an oxide source. The results of epitaxial crystalline and amorphous gate oxides are compared. Our investigations have demonstrated many attractive features satisfying the requirements for gate dielectric applications. For example, we show the absence of SiO_2 at the dielectric/Si interface that leads to a significant thickness saving for the overall dielectric layer. The amorphous Y_2O_3 films show six orders of magnitude lower leakage than SiO_2 with an equivalent oxide thickness of 10Å. The thermal stability against high temperature anneals offered competitive advantages over SiO_2 and other high ε dielectric candidates. Key issues of reliability, gate electrode, and process compatibility will also be addressed. Better understanding of the leakage mechanism and finer control of the interfaces are needed before full integration of these new materials into CMOS processing. Work done in collaboration with M. Hong, A. R. Kortan, K. L. Queeney, Y. J. Chabal, R. L. Opila, Jr., D. A. Muller, S. N. G. Chu, B. J. Sapjeta, T. S. Lay, J. P. Mannaerts, T. Boone, H. W. Krautter, J. J. Krajewski, A. M. Sergent, and J. M. Rosamilia.

4:00 PM

M6, Dependence of Thermal Stability of $ZrO_2/SiO_2/Si$ Layered Structure on Ambient Oxygen: *Heiji Watanabe*[1]; [1]NEC Corporation, Sys. Dev. & Fundmtl. Rsrch., 34 Miyukigaoka, Tsukuba, Ibaraki 305-8501 Japan

As the gate oxide thickness of metal-oxide-semiconductor (MOS) devices is scaled down to below 15A, tunneling current through gate dielectric and gate reliability become serious problems. High-k materials, such as ZrO_2 and Zr silicate ($ZrSi_xO_y$), have received considerable attention as alternative gate dielectrics in recent years. Since gate dielectrics must withstand high-temperature annealing to activate dopants, high-k materials on Si (or SiO_2) must have sufficient thermal stability for MOS integration. Although the phase diagram of the ternary Zr-Si-O system indicates that ZrO_2 is thermodynamically stable in contact with Si, previous studies have reported interfacial reactions, such as growth of the interfacial oxide (or silicate), and silicide formation caused by thermal decomposition of high-k materials at high temperature. Recently, effects of residual oxygen on these interfacial reactions have been pointed out, but detailed studies have not been performed. In the current work, in-situ fabrication of ZrO_2 /SiO_2/Si layered structure was demonstrated, and thermal stability of the ZrO_2/SiO_2 /Si interfaces was systematically investigated on-line by x-ray photoelectron spectroscopy (XPS) and off-line by transmission electron microscopy (TEM). The ZrO_2/SiO_2/Si samples were fabricated by in-situ re-oxidation of a thin Zr layer (about 2 nm) deposited on a 0.6-nm-thick chemical oxide in an ultrahigh-vacuum (UHV) chamber. Since re-oxidation was carried out under low oxygen pressure ($1x10^{-4}$ Torr), the Zr layer was preferentially oxidized without any change in the interfacial oxide thickness. The XPS analysis revealed that the ZrO_2/SiO_2/Si interfaces are atomically abrupt and that the fabrication method has an advantage over ex-situ methods. Thermal stability of the ZrO_2/SiO_2/Si layered structure was examined as a function of annealing temperature and ambient oxygen pressure. When the samples were annealed in controlled oxygen ambient at $1x10^{-4}$ Torr (600-800 degrees for 10 minutes), the interfacial oxide layer gradually grew with increasing annealing temperature. Changes in Si2p and Zr3d spectra revealed that, while Si-O bond formation is the dominant reaction during high-temperature annealing, the interfacial oxide consists of a small number of Zr atoms (Zr silicate). This result means that both the interfacial oxide (silicate) and ZrO_2 overlayer are not thermally stable in oxygen ambient. Contrary, under UHV conditions of less than $2x10^{-8}$ Torr, there was no change in photoelectron spectra up to 800 degrees. These stable spectra indicate the intrinsic thermodynamic stability of the ZrO_2 /SiO_2 /Si layered structure and also indicate that the interfacial reactions crucially depend on ambient oxygen pressure. Moreover, it was found that the ZrO_2 overlayer drastically accelerates the interfacial oxidation reaction (Zr silicate formation) in oxygen ambient. All the above-mentioned results thus suggest that careful control and reduction of residual oxygen pressure are required in fabrication of sub-10A gate dielectric.

4:20 PM (Student)

M7, Electrical Properties of HfO2 Gate Dielectric on SiGe: *Tat Ngai*[1]; Katsunori Onishi[1]; Rino Choi[1]; Chang Seok Kang[1]; John Fretwell[1]; Xiao Chen[1]; James Chen[1]; Jack C. Lee[1]; Sanjay Banerjee[1]; [1]University of Texas at Austin, Microelect. Rsrch. Ctr., 10100 Burnet Rd., Austin, TX 78758 USA

SiGe has attracted a lot of attention in recent years as a possible solution to an inherent limitation in conventional CMOS technology– the factor of two difference between the hole and electron mobilities in Si. One of the obstacles to the realization of PMOS speed advantage in SiGe layers is poor gate oxide problems. Although high qualify SiO2 had been reported to grow on relaxed SiGe layers, high leakage currents due to direct tunneling in thin oxide films are still difficult to be overcome. These limitations have led to a search for new materials deposited with low temperatures as a gate dielectric for SiGe applications. In this paper, we examine electrical properties of HfO2 gate dielectric on compressively-strained and relaxed SiGe layers, and we also investigate the effect of Ge content in SiGe layers on the properties of the HfO2/SiGe interface. HfO2 is one of few high-k materials that is predicted to be thermally stable on Si based on a thermodynamic study. It has a high dielectric constant (~25) an d a large bandgap (5-6.8 eV). Coupled with the compatibility with poly-Si process, HfO2 has been seen as the possible replacement for conventional SiO2. In this studies, HfO2 was deposited directly on SiGe using reactive sputtering at room temperature, followed by a 5 min. anneal at 500°C in a nitrogen ambient. The compressively-strained SiGe layers were deposited on Si substrates using ultra-high vacuum chemical vapor deposition (UHVCVD) and the relaxed SiGe layers were deposited using rapid thermal chemical vapor deposition (RTCVD). The Ge content in the strained SiGe layers was 10%, 20%, and 30%, respectively; and 70% Ge content was used in the relaxed SiGe layers. The smoothness of HfO2/SiGe interface was observed by cross-sectional TEM. The electrical results of HfO2 capacitors with metal gates and poly-Si gates, such as leakage current, stress-induced leakage current, interface-trap density, breakdown field, etc., will be presented. The electrical characteristics of the resulting PMOSFETs, such as subthreshold and output characteristics, will also be presented.

4:40 PM (Student)

M8, Investigation of Aluminum Oxynitride as Replacement Dielectric for SiC Devices: *William Leroy Rose*[1]; Gary Harris[1]; Michael Spencer[1]; [1]Howard University, MSRCE/Electl. Eng., 2300 6th St., LKD Bldg., Washington, DC 20059 USA

SiC is a semiconductor material with tremendous possibility in the semiconductor industry. This potential is due to the physical and chemical properties of SiC that would allow it to be used in areas where the more prominent semiconductor materials such as Si are approaching and in some cases reached there operational limits. Among these properties of SiC are its wide band gap, high drift velocity, thermal conductivity, and critical breakdown field. SiC is also a physically hard material is thermally stable at temperatures above 400ºC, and is chemically inert to virtually all known solvents. These qualities of SiC make it an ideal candidate for high power, high speed, high temperature and hostile environment applications. Not withstanding the vast potential for SiC there are still a number of challenges yet to be overcome before this material can fully realize its potential and become commercially viable. Among these challenges is the need to develop an insulator that is reliable under the possible extreme operating conditions of these projected SiC devices. AlN deposited by metal-organic chemical vapor deposition (mocvd) and pulse laser deposition (PLD) on 6H n-type epitaxial SiC grown on 6H SiC substrates, These layers were oxidized in a quartz furnace at 1100ºC, at atmospheric pressure to form aluminum oxynitride (AlO:N). Shottky

contacts were made to the AlO:N surface and full metalization of the substrate back side for ohmic contact was done by e-beam evaporation thus creating MOS capacitors. CV and IV analysis of several devices were carried out using HP 4192A impedance analyzer and Hp 4140B pA meter/DC Voltage supply, respectively. The data revealed an eE product greater than 30 MV/cm without reaching breakdown. These MOS structures revealed no significant leakage (leakage current in the 10-9 range) even at applied fields greater that the breakdown field of pure SiC. Both depletion and accumulation mode were obtained and were controllable. This System is being used to fabricate SiC/AlN/AlO:N MOS transistors.

Session N: Mixed III-V-N and Novel IR Materials

Thursday AM Room: 129
June 28, 2001 Location: University of Notre Dame

Session Chairs: Charles Tu, University of California–San Diego, Dept. of Electl. & Comp. Eng., La Jolla, CA 92093-0407 USA; Andrew Allerman, Sandia National Laboratories, Albuquerque, NM 87185 USA

THURSDAY AM

8:20 AM (Student)
N1, Nitrogen Incorporation in GaInNAs for Long Wavelength Opto-Electronic Devices: *Vincent Gambin*[1]; Wonill Ha[1]; Sylvia Spruytte[1]; James S. Harris[1]; [1]Stanford University, Electl. Eng., EE/SSL, CIS-X, B113-4, Via Ortega, Stanford, CA 94305 USA

GaInNAs grown on GaAs substrates has recently been found to optically emit at wavelengths longer than previously possible for material epitaxially grown on GaAs substrates. This material system is promising as an active region for use in 1.3 and 1.55 µm optoelectronic devices. Adding small amounts of nitrogen to GaAs alloys preserves direct gap properties and can decrease the bandgap while shrinking the lattice constant. Adding nitrogen to InGaAs pushes emission to longer wavelengths and offsets the In lattice mismatch making higher In concentrations possible. Casual observation contradicts this finding considering the equilibrium nitrogen solubility in GaAs is extremely small and the GaN bandgap is larger, not smaller, than GaAs. The large electronegativity of nitrogen and the mixing of cubic GaAs and hexagonal GaN crystal systems create significant band bending and low solid solubility between the two systems. Many material growth challenges exist due to these divergent properties of GaAs and GaN. Ni tride-arsenide alloys were grown by elemental source MBE using a nitrogen r.f. plasma cell. Substrate growth temperatures were kept low, kinetically limiting phase segregation, thereby incorporating much more nitrogen than is thermodymically stable. In contrast to the AsP systems used in 1.55 µm InP based materials, the N growth rate is inversely proportional to the group III growth rate. This is characteristic of unity sticking coefficient; under these growth conditions all supplied reactive nitrogen is incorporated in the lattice. This greatly eases compositional control for mixed group V alloys. High nitrogen content materials grown at low temperatures do not initially exhibit strong optical emission. The defects generated during the low temperature growth are a source for non-radiative recombination and diminish photoluminescence. By rapid thermal annealing the material after growth, defects are removed from the active region and the crystal quality of the GaInNAs films significantly improves. How ever, nitrogen out-diffuses from the quantum well and blue-shifts optical emission when annealing GaInNAs. A new active region structure has been developed with the goal of decreasing nitrogen out-diffusion while still improving crystal quality. In this new structure GaNAs barriers are grown around GaInNAs quantum wells with nitrogen content greater in the barrier than in the wells. By using GaNAs barriers between the GaInNAs quantum wells, we have sharply reduced the luminescence blue-shift while still improving crystal quality and radiative emission. Nitride barriers also compensates the compressive strain in high In content GaInNAs. By adjusting plasma conditions, optimizing annealing, and controlling indium, nitrogen and nitrogen barrier concentrations, we have observed high intensity photoluminescence at and beyond 1.3 µms. Application of these new structures to QW lasers and modulators will also be described.

8:40 AM (Student)
N2, Local Ordering in Vibrational Spectra of InGaAsN Alloys: *Alexander M. Mintairov*[1]; *Pavel A. Blagnov*[2]; Thomas H. Kosel[1]; James L. Merz[1]; Victor M. Ustinov[2]; Alexei S. Vlasov[2]; Roseann Csencsits[3]; [1]Notre Dame University, Electl. Eng., South Bend, IN 46556 USA; [2]Ioffe Physical-Technical Institute, St. Petersburg, Russia; [3]Argonne National Laboratory

The InGaAsN alloys have recently attracted considerable attention as promising materials for laser diodes in the 1.3-1.5 mm range as well as more efficient solar cells. These applications exploit the unusual electronic property–a "giant bowing''–which arises from the large electronegativity and very small ion radii of the nitrogen[1,2], together with the possibility of perfect lattice matching to GaAs substrates. Up to now little is known about the micro/nanostructure, i.e. possible atomic ordering and phase separation, of these alloys, which can dramatically alter their electronic and transport properties important for device applications. In the present paper using Raman and IR vibrational spectroscopy we observed effects indicating a local ordering of nitrogen atoms in InxGa1-xAs1-yNy (x=0 and ~0.08, y~0.02) alloys grown by molecular beam epitaxy. We observed strong zinc blende forbidden Raman components of GaAs-type phonons, indicating a local trigonal distortion of the alloy lattice induced by nitrogen ordering and indium induced splitting of the Ga-N type vibration, indicating formation of different local nitrogen atomic arrangements. Transmission electron microscopy measurements failed to reveal evidence of N ordering or clustering in either diffraction or high-resolution (HREM) images. However, the low N content would only be expected to create very weak image contrast or diffraction effects even if long-range ordering of the N were present. The appearance of strong zinc blende forbidden Raman components indicates the ordering of the GaN3As microclusters in InGaAsN alloys as has been observed in GaAsN[3]. Such a property has not been observed in conventional III-V alloys. The results presented show that it does not depend on the macroscopic strain due to lattice mismatch between epi layer and substrate. The driving force for the ordering can be strong local strains (bond relaxation) caused by the small nitrogen radii. The authors wish to acknowledge the NATO Science for Piece Program (grant SFP-972484) References: [1]S. Sakai, Y. Ueta and Y. Terauchi, Jpn. J. Appl. Phys. 32, p. 4413 (1993); [2]S.-H. Wei and A. Zunger, Phys. Rev. Lett. 76, 664 (1996); [3]A. M. Mintairov, P. A. Blagnov, V. G. Melehin, N. N. Faleev, J. L. Merz, Y. Qiu, S. A. Nikishin, H. Temkin, Phys. Rev. B 56, 15836 (1997).

9:00 AM (Student)
N3, Deep Levels and Their Impact on Current Generation in MOCVD-Grown GaAs/InGaAsN Heterostructure Devices: *Robert J. Kaplar*[1]; Aaron R. Arehart[1]; Steven A. Ringel[1]; Andrew A. Allerman[2]; Robert M. Sieg[2]; Steven R. Kurtz[2]; [1]Ohio State University, Dept. of Electl. Eng., 205 Dreese Lab., 2015 Neil Ave., Columbus, OH 43210 USA; [2]Sandia National Laboratories, Albuquerque, NM 87185 USA

Recently, the quaternary semiconductor InGaAsN has attracted considerable interest. The InGaAsN alloy may be grown lattice-matched to GaAs such that its bandgap corresponds to emission at 1.30 and 1.55µm, making it an attractive candidate for use in infrared laser diode applications. Further, the efficiency of $In_{0.5}Ga_{0.5}P$/GaAs/Ge solar cells could potentially be improved by the insertion of a lattice-matched, ~1.0eV InGaAsN junction between the GaAs and Ge junctions. Unfortunately, to date InGaAsN has exhibited low minority-carrier diffusion lengths, which may be due in part to deep level defects. In this study, deep levels in MOCVD-grown InGaAsN have been characterized using deep level transient spectroscopy (DLTS), and further, current-voltage-temperature (IVT) measurements have been undertaken to investigate the impact of deep levels on device performance. DLTS was utilized first to examine deep levels in an n-$In_{0.07}Ga_{0.93}As_{0.98}N_{0.02}$ (1.05 eV, Sn-doped) on p^+-GaAs heterojunction solar cell. Three electron traps, E1, E3, and E4, were found in as-grown InGaAsN. It was determined that E1 is a distribution of defect states starting at the conduction-band edge and terminating at approximately E_C-0.2eV, and traps E3 and E4 were found to be located at E_C-0.34eV and E_C-0.82eV, respectively. Two additional traps were found in annealed material: an electron trap, E2, at E_C-0.36eV, and a hole trap, H1, at E_V+0.71eV. The activation energies of traps E2 and H1 thus add to 1.07eV, which is close to the 1.05eV bandgap of the InGaAsN. This suggests that E2 and H1 are the same trap observed under conditions of

electron and hole emission, respectively. It is therefore likely that E2/H1 is an efficient recombination-generation center, and to test this assertion, an IVT measurement was performed at a fixed reverse-bias. This resulted in an activation energy of 0.36eV, which is close to the 0.35eV activation energy of E2 obtained from DLTS, suggesting that E2/H1 dominates the reverse-bias generation current in the sample. To our knowledge, this is the first time that a deep level has been shown to impact the performance of an InGaAsN-based device. DLTS measurements were also performed on a second annealed sample of identical structure to the first. The gas-flow transition from the GaAs base to the InGaAsN emitter was different for the two samples, however. Peaks E2 and H1 were absent in the spectrum of the second sample, suggesting that E2/H1 is related to the InGaAsN/GaAs heterointerface and that the concentration of this defect may be minimized through the use of appropriate growth conditions. Finally, DLTS depth-profiling is currently being performed on peak E2 in order to investigate the possibility of further correlation between the concentration of E2/H1 and growth conditions.

9:20 AM (Student)

N4, Distribution of Nitrogen Atoms in GaAsN and InGaAsN Alloys Determined by Scanning Tunneling Microscopy: *H. A. McKay*[1]; R. M. Feenstra[1]; T. Schmidtling[2]; U. W. Pohl[2]; J. F. Geisz[3]; [1]Carnegie Mellon University, Phys. Dept., 5000 Forbes Ave., Pittsburgh, PA 15213 USA; [2]Technishe Universitat Berlin, Hardenbergstr. 36, Berlin D-10623 Germany; [3]National Renewable Energy Laboratory, Golden, CO 80401 USA

Considerable interest has developed in recent years concerning GaAsN and InGaAsN alloys with low N content, typically a few %. The large predicted band gap bowing in this system of highly mismatched anions leads to the possibility of considerable band gap reduction with modest N content[1,2]. GaAsN and InGaAsN alloys have displayed broad photoluminescence (PL) line widths, variable PL decay times, and short minority carrier diffusion lengths[3,4], and such observations have been taken as evidence of compositional fluctuations in the materials. In this work we use cross-sectional scanning tunneling microscopy (STM) to directly probe the arrangement of N atoms in $GaAs_{0.083}N_{0.017}$ and $In_{0.04}Ga_{0.96}As_{0.99}N_{0.01}$ alloys. Nitrogen atoms in the first and third surface planes relative to the (110) cleavage surface are observed in filled state images. Voltage dependent imaging is used to identify second plane N atoms. From an accurate determination of the position of about 1000 N atoms in a continuous strip of alloy material, we compute the distribution function of pair separations. The arrangement of N atoms is found to be quite consistent with that expected from random occupation, with the exception that an enhanced occurrence of [001]-oriented nearest-neighbor N pairs is found. In addition to structural determination, STM has been used probe the spectroscopic properties of the substitutional N atoms in as-grown and annealed $In_{0.04}Ga_{0.96}As_{0.99}N_{0.01}$ alloys. An electronic state located about 1 eV above the conduction band edge has been observed near the N atoms. Shifts in the position and amplitude of this state are seen, and are tentatively associated with the varying location of the N atoms relative to the surface. Little difference in spectroscopy is seen between as-grown and annealed InGaAsN samples. Work supported by the National Science Foundation. [1]M. Weyers, M. Sato, and H. Ando, Jpn. J. Appl. Phys., Part 2, 31, L853 (1992). [2]S.-H. Wei and A. Zunger, Phys. Rev. Lett. 76, 664 (1996). [3]Y. Qiu et al. Appl. Phys. Lett. 70, 3242 (1997). [4]S. R. Kurtz et al., Appl. Phys. Lett. 77, 400 (2000).

9:40 AM (Student)

N5, Novel Interface Properties of Metastable (GaIn)(NAs)/(GaAs)-Heterostructures: *Siegfried Nau*[1]; Torsten Torunski[1]; Georg Bernatz[1]; Jörg Koch[1]; Falko Höhnsdorf[1]; Kerstin Volz[1]; Wolfgang Stolz[1]; [1]Philipps University, Matls. Sci. Ctr. & Dept. of Phys., Hans-Meerwein-Str., Marburg D-35032 Germany

The novel metastable material system (GaIn)(NAs) is interesting both from an application as well as from a fundamental point of view. It allows for long wavelength emission at 1.3µm or even 1.55µm based on GaAs substrate. It is possible to deposit high quality (GaIn)(NAs)/GaAs-quantum well heterostructures (QWH) under extreme non-equilibrium growth conditions using MBE or MOVPE. The structure of heterointerfaces is of key importance for the optical and transport properties and, thus, for device performance. In the present study we have developed a novel investigation technique which allows for the quantitative evaluation of real interior interface structures. This technique has been demonstrated for the material systems GaAs, (GaIn)As, (GaIn)P and now could be extended to the (GaIn)(NAs)-system. It combines specific highly selective quasi-digital etching techniques to uncover the interior interface of the epitaxial QWH with subsequent atomic force microscopy (AFM) investigations. Using this novel technique the structure of interior interfaces can be determined with atomic resolution in growth direction and with a lateral resolution of 10 to 15 nm over large sample areas. The sample structures have been deposited by using low temperature MOVPE applying the efficiently decomposing precursors triethylgallium (TEGa), trimethylindium (TMIn), tertiarybutylarsine (TBAs), and 1,1-Dimethylhydrazine (UDMHy). In the present study we show the formation of interior (GaIn)(NAs) interfaces depending on the growth interruption time under As- as well as under As- and N-stabilization leading to different interface structures. The (GaIn)(NAs)-system shows a behavior for interface formation and changes of interface structure during growth interruptions that is different from the conventional III/V-materials. During growth interruptions one does not observe formation of large area monolayer terraces, well known from (Ga(In))As, but two dimensional small sized islands. Exceeding a certain critical interruption time a complete restructuring of the interface and the total (GaIn)(NAs)-layer is observed. Moreover, the correlation of structural properties investigated by means of AFM on interior interfaces, high resolution X-ray diffraction and TEM and the electronic properties determined by standard photoluminescence will be presented and discussed. The detection of the novel structural development of (GaIn)(NAs)/GaAs-heterostructures and its correlation to the electronic properties shows the importance of the presented novel interior interface investigation technique for a better understanding of growth processes and for achieving high quality heterostructures and devices in the (GaIn)(NAs)-material system.

10:00 AM Break

10:20 AM

N6, Infrared Absorption of Thermally Annealed GaInNAs: *Takeshi Kitatani*[1]; Masahiko Kondow[1]; Makoto Kudo[2]; [1]RWCP Optical Interconnection Hitachi Laboratory, 1-280 Higashi-koigakubo, Kokubunji-shi, Tokyo 185-8601 Japan; [2]Hitachi, Ltd., Central Rsrch. Lab., 1-280 Higashi-koigakubo, Kokubunji-shi, Tokyo 185-8601 Japan

The use of GaInNAs is expected to improve the performance of long-wavelength lasers, since this material could enable ideal electron confinement in the active region of lasers[1]. However, it is difficult to obtain good crystallinity, so the photoluminescence (PL) intensity of as-grown GaInNAs is lower than that of GaInAs. Thermal annealing is one method for enhancing the PL intensity of GaInNAs. However, after annealing, the peak wavelength is blue-shifted, and the shift is much larger than that for GaInAs. We previously reported that this blue-shift is based on a bandgap change in GaInNAs[2]. In our current research, to clarify the origin of this bandgap shift, we used infrared (IR) absorption measurements to investigate changes in the atomic structure of GaInNAs during thermal annealing. The observed variation in the absorption peak suggests that the blue-shift in the bandgap of thermally annealed GaInNAs is caused by a change in the bonding of GaInNAs. We grew a 1-µm-thick Ga0.95In0.05N0.02As0.98 bulk layer lattice matched to GaAs, by gas-source molecular beam epitaxy with RF radicals. The growth temperature was 460ºC, and the growth rate was 1.0 µm/hr. After crystal growth, the samples were thermally annealed in the MBE chamber for 1 hour at temperatures of 550, 600, or 650ºC under an AsH3 flow rate of 5 sccm. IR absorption of sample was measured at room temperature. In the as-grown samples, an absorption peak observed at 469 cm-1 was due to the TO mode of the Ga-N bonds[3]. At higher annealing temperatures, its peak intensity decreased, while a new peak appeared at 489 cm-1 with an increased intensity. Since the total absorbance of both peaks after annealing was almost the same as that before annealing, the transition from 469 cm-1 to 489 cm-1 is probably due to alternation of the bonding state of Ga-N. Furthermore, the transition to the higher wavenumber side is qualitatively consistent with the blue-shift in the bandgap, since the absorption peaks of larger bandgap semiconductors are generally observed in the higher wavenumber region. Therefore, the results suggest that the blue-shift in the bandgap of thermally annealed GaInNAs is probably based on the change in bonding. In summary, we measured the IR absorption of thermally annealed Ga0.95In0.05N0.02As0.98 bulk layers. From a transition in the absorption peaks, we confirmed that variation in bonding should cause the change in the bandgap of GaInNAs during thermal annealing. [1]M. Kondow, et al., Jpn. J. of Appl. Phys. 33

(1996) 1273. [2]T. Kitatani, et al., J. of Cryst. Growth 209 (2000) 345. [3]M. Kondow, et al., private communication.

10:40 AM

N7, GaInTlAs Layers Grown on InP by Low Temperature Molecular Beam Epitaxy: Structural and Optical Properties: Francisco Sanchez-Almazan[1]; Michel Gendry[1]; Philippe Regreny[1]; Marie-Paule Besland[1]; Geneviève Grenet[1]; Jose Olivares[2]; A. Sibai[2]; Georges Bremond[2]; Olivier Marty[3]; Michel Pitaval[3]; *Guy R. Hollinger*[1]; [1]Ecole Centrale de Lyon, LEOM-UMR CNRS 5512, Ecully, Cedex 69131 France; [2]INSA de Lyon, LPM-UMR CNRS 5511, Villeurbanne, Cedex 69621 France; [3]Université Lyon, 1 Lenac, Villeurbanne, Cedex 69621 France

GaInTlP and GaInTlAs quaternary thallium alloys have been proposed as new infrared materials for long wavelength operation. They can theoretically be prepared lattice matched to InP or GaAs. This encouraged growth studies either at high temperatures (400-450°C) or at low temperatures (<250°C). For growths performed at high temperatures, contradictory conclusions have been reached and the situation is presently rather confusing. Only Asahi et al[1] claimed successful growth of GaInTlP and GaInTlAs alloys in the growth temperature range of 400-450°C. In contrast, most other authors who measured Tl concentrations using analytical techniques, did not succeed in incorporating Tl into InP, GaInAs and InAs matrices using gas source molecular beam epitaxy (GSMBE) or solid source molecular beam epitaxy (SSMBE). Results for growth performed at low temperature are less contradictory and a few authors achieved the incorporation of a few % of Tl but the layers were not single crystalline. In this work, growth of GaInTlAs alloys on InP(001) has been attempted by SSMBE. Thallium incorporation into Ga1-xInxAs matrices was studied as a function of substrate temperature, arsenic overpressure, matrix composition and growth rate. Various qualitative and quantitative analytical methods have been used to actually evaluate the Tl concentration. At high temperatures (>350°C) thallium evaporates whereas at intermediary temperatures (270°C-350°C) thallium segregates into droplets on the surface. Only in the low temperature range (180°C-270°C) can thallium be incorporated in some conditions, leading to mirror like surfaces. Up to 18% Tl content was incorporated into a Ga0.70In0.30As matrix. For these high Tl concentrations, Tl droplets are avoided and Tl incorporation is achieved only when using high arsenic pressures. However, this limits surface adatom diffusion and leads to amorphous or polycristalline materials. Finally, a narrow window for single-crystal growth has been found for low Tl contents (4%) using optimized growth conditions with high growth rates and sufficiently low V/III pressure ratios[2]. For Tl concentration from 4 to 12%, no single crystalline growth conditions has been found and twinning occurred. The structural and optical properties of GaInTlAs single crystalline layers were studied using X-ray diffraction, transmission electron microscopy, atomic force microscopy, photoluminescence and optical absorption and were compared to those of reference Tl-free samples. It was shown that Tl incorporation in a GaInAs matrix leads to an increase of the lattice parameter and to a decrease of the band gap, in agreement with theoretical predictions. [1]H. Asahi, H. Koh, K. Takenaka, K. Asami, K. Oe, and S. Gonda. J. Crystal Growth 201/202, 1069 (1999). [2]F. Sanchez-Almazan, M. Gendry, P. Regreny, E. Bergignat, G. Grenet, G. Hollinger, J. Olivares, G. Bremond, O. Marty, M. Pitaval, J. Vac. Sci. Technol. A. May/June 2001.

11:00 AM

N8, Theoretical Study of the Effects of Isovalent Co-Alloying of Bi and N in GaAs: *Su-Huai Wei*[1]; A. Janotti[1]; S. B. Zhang[1]; [1]National Renewable Energy Laboratory, Basic Sci. Ctr., 1617 Cole Blvd., Golden, CO 80401 USA

Band structure and total energy calculations are performed to study GaAs 1-x-yNxBiy alloys as a novel 1-eV band-gap material lattice-matched to GaAs for infrared laser and solar cell applications. The structural and electronic properties of the alloy-stabilized zinc-blende GaBi and InBi are predicted. We find that with the appropriate ratio between the concentration of Bi and N (y=1.7x), this alloy is lattice-matched to GaAs. We show that co-alloying of Bi and N in GaAs lowers the alloy formation energy and drastically reduces the amount of N needed to reach the 1-eV band gap. Therefore, the GaAs 1-x-yNxBiy alloy is predicted to be a strong candidate for the 1-eV band-gap material.

11:20 AM (Student)

N9, A Dislocation-Free and Lattice-Matched Si/$GaP_{0.971}N_{0.029}$/Si Structure: *Kenji Momose*[1]; Hiroo Yonezu[1]; Yasuhiro Fujimoto[1]; Yoshifumi Motomura[1]; Yuzo Furukawa[1]; [1]Toyohashi University of Technology, Dept. of Electl. & Elect. Eng., 1-1 Hibarigaoka, Tempaku-cho, Toyohashi, Aichi 441-8580 Japan

The monolithic integration of Si and III-V compound semiconductor is a key technology to realize novel optoelectronic integrated circuits (OEICs). One of major problems to form of OEICs is the lattice-mismatch between Si and III-V compound semiconductors. III-V-N alloy semiconductors such as $GaP_{1-x}N_x$ and $GaAs_{1-x}N_x$, in which the lattice constants are decreased with increasing a nitrogen composition x, have attracted much attention for new materials lattice-matched to Si. We have already reported that a dislocation-free $GaP_{0.987}N_{0.013}$ alloy layer can be grown on Si with a thin GaP buffer layer, for the first time. In this work, we proposed a novel structure of Si/III-V compound semiconductor/Si substrate. A built-in III-V compound semiconductor layer can be used for optoelectronic devices such as laser diodes (LDs) and photodetectors. Furthermore, Si layer at the topmost surface will make it possible to fabricate Si-LSI in conventional process. We succeeded in the growth of a dislocation-free and lattice-matched Si/$GaP_{1-x}N_x$/Si structure. Epitaxial growth has been carried out using a solid-source molecular beam epitaxy apparatus. Si (100) wafers misoriented by 4° toward [011] were used as substrates. After the thermal treatment, a 20 nm thick GaP buffer layer was grown by migration enhanced epitaxy (MEE) at 450°C in order to prevent the 3D growth and the generation of anti-phase domain. A 400 nm thick $GaP_{0.971}N_{0.029}$ alloy layer was grown at 590°C. Then, a substrate temperature was decreased to 450°C and the P_2 flux was shut off. Subsequently, a 100 nm thick Si layer was grown at 590°C using an electron-beam evaporator. This growth procedure was found to be effective in suppressing the generation of threading dislocations as well as stacking faults in the initial growth stage of Si. RHEED patterns during the growth of all layers were kept streaky without apparent change to spot patterns. These results indicate that the epitaxial layers were grown two-dimensionally. A cross-sectional transmission electron microscopy image revealed that there were no threading dislocations and misfit dislocations in the epitaxial layer. A lattice mismatch at room temperature between Si and $GaP_{0.971}N_{0.029}$ was 0.13%, which is the same as that of AlAs/GaAs heterostructure. Moreover, the full-widths at half maximum (FWHM) of (400) X-ray rocking curves of the Si and $GaP_{0.971}N_{0.029}$ layer were 16 arcsec and 19 arcsec, respectively. It was clarified that the Si and $GaP_{0.971}N_{0.029}$ layers had no dislocations and high crystal quality. Future goals for this work are integration of QW structures, planar lightwave circuits, micro-optoelectronic devices and LSI in one chip based on the Si/$GaP_{1-x}N_x$/Si structure. Additionally, in the case of the semi-insulating $GaP_{1-x}N_x$ layer, this structure would be applicable to a silicon-on-insulator (SOI) structure with a high quality Si layer by epitaxial process.

11:40 AM (Student)

N10, A Dislocation-Free $GaAs_yP_{1-x-y}N_x/GaP_{0.98}N_{0.02}$ Quantum Well Structure Lattice-Matched to Si Substrate: *Yasuhiro Fujimoto*[1]; Hiroo Yonezu[1]; Atsushi Utsumi[1]; Kenji Momose[1]; Yuzo Furukawa[1]; [1]Toyohashi University of Technology, Dept. of Electl. & Elect. Eng., 1-1 Hibarigaoka, Tempaku-cho, Toyohashi, Aichi 441-8580 Japan

The growth of high-quality III-V compound semiconductors on Si substrates is a key technology for the realization of optoelectronic integrated circuits (OEICs). However, a large number of threading dislocations are generated in grown layers on Si substrates. It is mainly attributed to a large lattice mismatch between the grown layer and Si. Therefore, we first attempted to grow a $GaAs_yP_{1-x-y}N_x$ /$GaP_{0.98}N_{0.02}$ quantum well (QW) structure lattice-matched to Si using III-V-N alloys with N composition below 3%, in order to realize a dislocation-free QW structure on Si. As a result, it was found that the generation of misfit dislocations as well as threading dislocations was suppressed at the QW structure and the dislocation-free QW structure was successfully realized on Si. The epitaxial growth was carried out using a solid-source molecular beam epitaxy apparatus. Firstly, a 20 nm thick GaP layer was grown on Si (100) substrate misoriented by 4° toward the [011] direction to form a GaP/Si structure. The thickness of the GaP layer was chosen to be less than a critical thickness to prevent the generation of misfit dislocations. Then, $GaAs_{0.66}P_{0.31}N_{0.03}$ /$GaAs_{0.05}P_{0.92}N_{0.03}$ /$GaP_{0.98}N_{0.02}$ QW structure was grown on the GaP/Si structure. In this QW structure, the $GaP_{0.98}N_{0.02}$ cladding layer and the $GaAs_{0.05}P_{0.92}N_{0.03}$ guiding layer are lattice-matched to Si. The

$GaAs_{0.66}P_{0.31}N_{0.03}$ well layer forms a strained QW with a compressive strain of 2.3%. Streaky patterns were maintained without apparent transition to spot patterns during the growth of all layers. This means that each layer was grown two-dimensionally. It was confirmed that the $GaAs_yP_{1-x-y}N_x/GaP_{0.98}N_{0.02}$ QW structure was lattice-matched to the Si substrate from lattice constant measured by X-ray diffraction. In addition, the full-width at half maximum (FWHM) of a (400) X-ray rocking curve of the QW structure was 21 arcsec, evidence for the good crystallinity. A cross-sectional image taken by transmission electron microscopy revealed that no threading dislocations and misfit dislocations were observed at the QW structure. In the growth of III-V compound semiconductors on Si substrates, these results demonstrated that the dislocation-free $GaAs_yP_{1-x-y}N_x/GaP_{0.98}N_{0.02}$ QW structure was realized on Si for the first time. These results indicate that a highly reliable and performed $GaAs_yP_{1-x-y}N_x/GaP_{0.98}N_{0.02}$ laser diode could be realized on Si substrate in the near future.

Session O: Molecular and Organic Electronics

Thursday AM Room: 141
June 28, 2001 Location: University of Notre Dame

Session Chairs: George Malliaras, Cornell University, Matl. Sci. & Eng., Ithaca, NY 14853 USA; Marya Lieberman, University of Notre Dame, Chem. & Biochem., Notre Dame, IN 46556 USA; David Janes, Purdue University, Dept. of Electl. Eng., West Lafayette, IN 47907-1285 USA

8:20 AM (Student)
O1, Electrostatic Surface Potential of Conjugated Molecules on Au(111) Using Electrostatic Force Microscopy: *Stephen W. Howell*[1]; D. Kuila[2]; A. W. Ghosh[2]; T. Rakshit[2]; H. McNally[2]; B. Kasibhatla[3]; D. B. Janes[2]; S. Datta[2]; C. Kubiak[3]; R. Reifenberger[1]; [1]Purdue University, Dept. of Phys., West Lafayette, IN 47907 USA; [2]Purdue University, Sch. of Electl. & Comp. Eng., West Lafayette, IN 47907 USA; [3]University of California–San Diego, Dept. of Chem. & Biochem., La Jolla, CA 92093-0358 USA

In the field of molecular electronics, a common configuration for conduction/device experiments involves interfacing a monolayer of organic molecules on a flat metal surface, often in the form of a self-assembled monolayer (SAM). One of the fundamental issues involved in understanding and modeling the conduction properties of these systems is the relative position of the molecular states with respect to the Fermi level. This band alignment, along with the broadening of molecular states associated with bonding to the metal, determines the low-field conductivity as well as the turn-on voltage of metal/molecule/metal systems[1]. Knowledge of these quantities allows the prediction of band line-ups in much the same way as in semiconductor heterostructures or metal-semiconductor (Schottky) junctions. The electrostatic surface potential of the molecular layer with respect to that of the metal substrate is a key parameter in determining the nature of the molecule/metal junction, since it provides information abou t the charge transfer between the molecule and metal. In order to obtain experimental information on these important questions, an experimental study was conducted to determine the electrostatic potential of a variety of SAMs using an electrostatic force microscope[2]. A heavily doped silicon tip was used to measure the electrostatic surface potential that develops when a SAM is deposited on Au(111). Molecular SAMs studied so far include monolayers of alkanethiol molecules, which are relatively insulating, as well as molecules of more direct interest for molecular electronics, including conducting dithiol molecules such as xyxyl dithiol and molecules in which the conductivity can be modulated by "doping" via the formation of a charge-transfer complex. By referencing all measured potentials to that of bare Au, we have been able to establish the amount of charge transfer between the net dipole layer associated with each SAM, and to analyze the relative contributions arising from intrinsic dipoles in the mo lecule and those arising from the bonding to the surface. Measurements on several aromatic thiols, designed with symmetric and non-symmetric molecular end-groups, indicate that non-symmetric molecules have significantly higher surface potential than symmetric ones. In the case of doped molecules, the measured surface potential reflects the dipole layer associated with the charge transfer complex involving a donor molecule and an acceptor molecule. Initial modeling of the surface potential is based on a theory involving Hartree-Fock evaluation of the molecule's Mulliken charge distribution. The predicted values of surface potentials for dodecanethiol and octadecylthiol are consistent with the potentials measured for these molecules in the current study. The changes in electrostatic potential with chain length for the alkanethiols in our measurements and modeling are consistent with published reports[3,4], which considered variations with chain length but did not consider the reference potential of the ba re Au. The utility of these measurements is the correlation they provide with observed current-voltage behavior of SAMs, providing further confidence in the parameters used in ab initio calculations of the current-voltage characteristics of metal/molecule/metal systems.[1] [1]W. Tian, S. Datta, S. Hong, R. Reifenberger, J. I. Henderson and C. P. Kubiak, J. Chem. Phys. 109, 2874 (1998); [2]M. Nonnenmacher, et al. Appl. Phys. Lett. 58, 2921 (1991); [3]S. D. Evans and A. Ulman, Chem. Phys. Lett. 170, 462 (1990). [4] J. Lu, et al., Langmuir 15, 8184 (1999).

8:40 AM
O2, Progress Towards Molecular Quantum-Dot Cellular Automata: *Marya Lieberman*[1]; Thomas P. Fehlner[1]; [1]University of Notre Dame, Dept. of Chem. & Biochem., 251 NSH, Notre Dame, IN 46556 USA

The quantum-dot cellular automata (QCA) paradigm for computing describes how information can be transmitted and processed by Coulomb interactions between structures that contain electrical charge. QCA wires, logic gates, memories, etc. have been demonstrated at the micrometer scale in a prototype system based on lithographically fabricated metal dots. A large research effort is underway at Notre Dame to translate this paradigm to the smallest possible size scale, that of individual molecules. This talk will introduce design criteria for molecular QCA cells and describe a series of binuclear and tetranuclear mixed-valence compounds that meet these criteria. Recent results on the electrochemical, optical, and selective surface attachment properties of these molecular QCA cells will be presented.

9:00 AM (Student)
O3, Can Organic Molecules Be Ohmic? Modifying Conductance of Molecular Nanostructures By Doping: *Andre P. Labonte*[1]; Bala T. Kasibhatla[2]; Clifford P. Kubiak[2]; Ronald G. Reifenberger[1]; Supriyo Datta[3]; [1]Purdue University, Dept. of Phys., 1396 Physics Bldg., West Lafayette, IN 47907-1396 USA; [2]University of California-San Diego, Dept. of Chem. & Biochem., La Jolla, CA 92093-0358 USA; [3]Purdue University, Sch. of Electl. Eng., West Lafayette, IN 47907 USA

In the developing field of molecular electronics, molecular systems typically have relatively poor low-field conductivity, due to the properties of the metal-molecule systems studied to date. Scanning tunneling spectroscopy (STS) of organic "molecular wires" on Au(111) have shown electrical conductance depends on (i) electronic structure of the molecule, (ii) length of the molecule, and (iii) nature of the end-groups that attach the molecule to gold. These studies show that the conductance of organic molecules is strongly dependent on the properties of the molecule, and that the Fermi energy of gold lies within the HOMO/LUMO gap of most simple organic molecules. In order to realize a set of components for molecular electronics, it is necessary to develop good single-molecule conductors. Additionally, molecular systems in which the conductivity can be modified by a procedure comparable to doping of semiconductors would enable a new class of materials and devices. In the current study, we have demonstrated that organic molecules can be doped via the formation of a charge transfer complex. Scanning tunneling spectroscopy (STS) on self-assembled monolayers (SAMs) of organic molecules and their charge transfer complexes has verified that the doping results in a significant change in molecular conductivity. The result of this 1:1 molecular doping is a change in the conductance of the molecule from an electrical insulator to an electrical conductor (Ohmic for small voltages). The preparation and electrical properties of pentamethyl benzylthiol (PMBT) and tetramethyl xylyldithiol (TMXYL) SAMs and their 1:1 charge-transfer complexes with the electron acceptor, tetracyanoethylene (TCNE) will be described. We will show that "doping" the thiol

monolayers with TCNE triggers (i) a change in the structure of the monolayer and (ii) a change in electrical behavior insulating to conducting. Removal of the TCNE "dopant" with a stronger electron donor (TTF) affords monolayers of TMX YL that remain in the flattened orientation, with phenyl rings parallel to the Au(111) surface. STM studies show that the flat TMXYL monolayers are highly resistive. Together, these studies indicate that the higher conductance of the "doped" TMXYL monolayers relative to the "undoped" PMBT and TMXYL monolayers in either their vertical or horizontal orientation arises from the electronic structure of the surface confined charge transfer complexes.

9:20 AM (Student)

O4, Growth Characteristics of Carbon Nanotubes Grown Using Carbon Monoxide by Plasma Enhanced Chemical Vapor Deposition: *Jae-hee Han*[1]; Sun Hong Choi[1]; Tae Young Lee[1]; Ji-Hoon Yang[2]; Ji-Beom Yoo[1]; Chong-Yun Park[2]; [1]Sungkyunkwan University, Matls. Eng., 300 Chunchun-Dong, Jangan-Gu, Suwon, Kyunki-Do 440-746 Korea; [2]Sungkyunkwan University, Phys., 300 Chunchun-Dong, Jangan-Gu, Suwon, Kyounki-Do 440-746 Korea

In recent years, there have been intensive studies concerning the preparation, calculation, characterization and application of carbon nanotubes worldwide. It has been suggested that, due to its unique properties, this fascinating material is about to trigger a revolution in nano-devicing, optical computing, carbon chemistry and new functional structural materials. We have been already grown vertically aligned carbon nanotubes on catalyst metal (such as Ni, Ni-Fe)-coated glass and silicon (100) with and without buffer layer (such as Cr, SiN_x) at temperature below 600°C by plasma enhanced hot filament chemical vapor deposition (PECVD). Acetylene (C_2H_2) gas was used as the carbon source and ammonia (NH_3) gas was used as a catalyst and dilution gas. In this case, however, the growth of carbon nanotubes may occur not only from C atoms and aggregates but also from hydrocarbon radicals like CH_3¡¤ or C_2H¡¤ with subsequent dehydrogenation, similar to chemical vapor deposition of diamond. These radicals may have an effect on the properties of carbon nanotubes during the growth process. Therefore, in order to exclude these by-products, we used carbon monoxide (CO) as the source gas. Carbon nanotubes were grown as a result of the chemical reaction 2CO -> C + CO_2, which do not yield the radical but stabilized gas of CO_2. In this study, we investigated the effects of growth parameters such as pretreatment, temperature, bias voltage, plasma intensity, pressure, flow rate, composition of input gas on the properties of carbon nanotubes using CO gas, compared to the growth characteristics using C_2H_2. For the examination of morphology of carbon nanotubes, field emission scanning electron microscopy (FESEM) was used. To study the microstructure of carbon nanotubes, transmission electron microscopy (TEM) was employed.

9:40 AM

O5, Study on Emission Property of Field Emission Display with the Density of Carbon Nanotube: *Ha Jin Kim*[1]; In Taek Han[1]; Yong Wan Jin[1]; Jae Eun Jung[1]; Young Jun Park[1]; Nae-Sung Lee[1]; Jong Min Kim[1]; Jae-hee Han[2]; Won-Seok Yang[2]; Ji-Beom Yoo[2]; [1]Samsung Advanced Institute of Technology, Display Lab., PO Box 111, Suwon, Korea; [2]Sungkyunkwan University, Dept. of Matls. Eng., 300 Chunchun-dong, Jangan-gu, Suwon, Korea

Field Emission Display (FED) is an potential candidate for flat panel display due to its typical characteristics such as thin and light, non irradiation, full color and gray scale, high brightness, fast video rate, wide view angle, wide operating temperature and moisture limits. Mo or Si is conventionally used as the emitter material of FED, but it requires high voltage for electron emission because of high electron affinity. And it is known that they have many problems in stability and reliability. Carbon nanotubes have been suggested as an alternative material to solve these problems in fabrication FED with low operating voltage. Carbon nanotubes are also potential candidates for cold cathode field emitter because of high aspect ratio and small radii of curvature at their tips with high chemical stability, thermal conductivity, and high mechanical strength. We investigate vertically aligned carbon nanotube on glass substrate at low temperature using CVD (Chemical Vapor Deposition) for Field Emission Display. Carbon nanotubes were directly grown on substrate using selective area growth technique after gate opening and insulator etching using conventional lithography process. The carbon nanotubes were about 40nm in diameter and 1μ-m in length. Fabricated carbon nanotube FED shows turn on field of 7V/ μm in diode mode, and the emission current was modulated with gate voltage in triode mode. The emission current density can be optimized by tuning the density of carbon nanotubes. Density of carbon nanotube was controlled by treatment of catalytic metal layer and we achieved improved emission characteristics.

10:00 AM Break

10:20 AM (Student)

O6, Napthacene Organic Thin Film Transistors: *David J. Gundlach*[1]; Jon A. Nichols[1]; Thomas N. Jackson[1]; [1]Pennsylvania State University, Ctr. for Thin Film Dev., Dept. of Electl. Eng., 121 Electrical Engineering E., University Park, PA 16802 USA

Using thermally evaporated films of napthacene as the active layer material we have fabricated organic thin film transistors (OTFTs) with device performance acceptable for several large-area and low-cost electronic applications. Our napthacene OTFTs were fabricated on heavily-doped, thermally oxidized single-crystal silicon substrates with photolithographically defined pre-patterned palladium or gold source and drain contact metal. Prior to active layer deposition, we treated the silicon dioxide gate dielectric of half of the substrates with the silane coupling agent octadecyltrichlorosilane (OTS) using a vacuum vapor prime technique. In work with similar organic semiconductor materials we have found the use of silane couplings agents useful for improving device performance, most notably field-effect mobility. The remaining substrates were processed in parallel but left untreated. Napthacene was deposited by thermal evaporation onto treated and untreated substrates held at 60, 45, 25, and 15°C. TFTs fabricated on untreated substrates held at 15°C had field-effect mobility near 0.03 cm^2/V-s, on/off current ratio as large as 10^6, threshold voltage of -16 V, and subthreshold slope less than 1.5 V/decade. TFTs fabricated on OTS treated substrates held at 15°C had improved performance with field-effect mobility larger than 0.1 cm^2/V-s, on/off current ratio greater than 10^6, threshold voltage of -16 V, and subthreshold slope less than 2 V/decade. We find device performance degrades as substrate temperature is increased. For substrates held at 45 and 60°C the sticking coefficient is sufficiently low that nearly all of the deposited napthacene is re-evaporated from the substrate surface. In addition to fabricating and characterizing OTFTs we used atomic force microscopy and x-ray diffraction to investigate the film morphology and molecular ordering of the thermally evaporated napthacene active layers. We find napthacene films deposited onto substrates held at low temperature consist of a high density of submicron sized grains with a surprisingly high degree of molecular order. AFM scans of films deposited on substrates held at 25°C show poor film connectivity. Grain size and density is similar to films deposited at 15°C but the grains appear to coalesce to form isolated micron-sized dendritic clusters with regions of exposed substrate between clusters. The low mobility results for devices fabricated using well ordered films deposited at 25°C are consistent with the AFM topology scans showing poor film connectivity. Previous reports of napthacene TFTs list no observed field-effect[1]. This observation is consistent with our observation of poor film connectivity for films deposited onto modestly heated substrates, which may prevent carrier transport through the film. [1]G. Horowitz, X-Z. Peng, D. Fichou, and F. Garnier, Synth. Met., 51, 419 (1992).

10:40 AM

O7, Orientation of Pentacene Films Using Surface Alignment Layers and its Influence on Thin Film Transistor Characteristics: *Michele Swiggers*[1]; *George Malliaras*[1]; Randall Headrick[2]; Charles Dulcey[3]; R. Shashidhar[3]; [1]Cornell University, Matls. Sci. & Eng., Bard Hall, Ithaca, NY 14853-1501 USA; [2]Cornell University, Cornell High Energy Synchrotron Source, Ithaca, NY 14853 USA; [3]Naval Research Laboratory, Ctr. for Bio/Molecular Sci. & Eng., 4555 Overlook Ave. S.W., Washington, DC 20375 USA

We investigate the ability of alignment layers to produce order in thin pentacene films. Both rubbed and photoirradiated layers of polymers and self-assembled monolayers were investigated. Rubbed polyvinylalcohol layers were found to align approximately 27% of the pentacene grains within a 30° range. When introduced in a thin film transistor, they were found to enhance the saturation current by a factor of 2.5. A mechanism for this enhancement is proposed.

11:00 AM

O8, Polymer Encapsulation of Screen Printed Organic Thin Film Transistors: *Jianna Wang*[1]; Caprice Gray[1]; Gregg Duthaler[1]; Andrew

Ritenour[1]; Paul Drzaic[1]; [1]E Ink Corporation, 733 Concord Ave., Cambridge, MA 02138 USA

Organic thin film transistors (OTFTs) have drawn great attention for the fabrication of low cost, flexible displays and other large area electronic uses. One of the major barriers for OTFTs commercialization is device stability. Moisture, oxygen, organic solvents and other chemicals can easily degrade OTFTs. This suggests that OTFTs must be encapsulated before integration into any display circuitry. PECVD silicon nitride or silicon oxide films are compatible with OTFTs and have excellent barrier properties against moisture and oxygen. However, the high deposition and patterning costs are not desirable. Furthermore, unlike flexible polymer coatings, these traditional passivation films are easily cracked; meaning they are not compatible with large area flexible display applications. In our approach, low cost, easy to process polymer coatings have been selected as the encapsulants. OTFTs based on various organic semiconductors (OSCs) have been encapsulated. These OSCs include pentacene, copper phthalocyanine, alfa-sexithiophene, and poly(3-hexyl thiophene). For the material compatibility study between the selected encapsulants and OSCs, devices have been fabricated on a silicon wafer. A doped silicon wafer was the gate electrode; thermally grown silicon dioxide was the gate dielectric; thermally evaporated gold was the drain-source electrode that was patterned by traditional photolithography method. After the deposition of active semiconductor layer over the drain-source electrodes, OTFTs were encapsulated by applying a thick polymer coating (3-10 microns) in the channel areas. The selected encapsulants include screen printable polymer resins and room temperature vapor deposited parylene films. We have found several polymer coatings that are compatible with all the OSCs that have been studied. Preliminary results showed that although the polymer-encapsulated TFTs have lower on-current than the controlled devices, they have a much higher on/off ratio due to a much lower off-current. Lifetime studies showed that device degradation of the polymer-encapsulated TFTs are slower over time compared to the non-encapsulated devices. A screen printable polymeric resin has been successfully used to encapsulate OTFTs fabricated on glass substrates, where 80 nm chrome was the gate electrode, 1 micron parylene was the gate dielectric, 50 nm pentacene was the active layer, and 6-9 micron screen-printed silver ink was the drain-source electrodes. Good TFT performance has been achieved on the polymer encapsulated device with on/off ratio of 105 and field effect carrier mobility of 0.012 cm2/V.s.

11:20 AM (Student)

O9, Organic Thin Film Transistors with Improved Linear Region Performance Using Chemically-Modified Source and Drain Contacts: *David J. Gundlach*[1]; LiLi Jia[1]; Thomas N. Jackson[1]; [1]Pennsylvania State University, Ctr. for Thin Film Dev., Dept. of Electl. Eng., 121 Electrical Engineering E., University Park, PA 16802 USA

We report on the use of chemically modified source and drain contacts to fabricate pentacene OTFTs with improved linear region characteristics and suitable for high information content flat panel displays. To date, most reports of high performance OTFTs and single-crystal organic field-effect transistors have been for devices operating in saturation. For applications such as flat panel displays, pixel TFTs are operated exclusively or nearly exclusively in the linear region of device operation. Our OTFTs with improved linear region performance were fabricated on heavily-doped, thermally oxidized single-crystal silicon substrates with photolithographically defined pre-patterned palladium source and drain contact metal chemically modified with a self-assembling molecule with electron withdrawing properties. The pentacene OTFTs fabricated as described above with chemically-modified source and drain contacts have linear field-effect mobility greater than 0.5 cm^2/V-s at a drain-source voltage of -0.1 V, current on/off ratio greater than 10^7, and subthreshold slope less than 0.7 V/decade. Devices fabricated simultaneously but with untreated contacts have linear mobility less that 0.2 cm^2/V-s, typical for bottom contact OTFTs. To our best knowledge the treated contact devices have the highest linear region mobility reported for an organic thin film transistor. The process we have described for improving the linear region performance of pentacene TFTs can easily be extended to low cost glass or flexible plastic substrates[1] and may also prove useful for improving charge injection in organic electroluminescent devices. [1]C. D. Sheraw, J. A. Nichols, D. J. Gundlach, J. R. Huang, C. C. Kuo, H. Klauk, T. N. Jackson, M. G. Kane, J. Campi, F. P. Cuomo, and B. K. Greening, "Fast Organic Circuits on Flexible Polymeric Substrates," 2000 International Electron Devices Meeting Technical Digest, pp. 619-622, December 2000.

11:40 AM, O10, Late News

Session P: Quantum Dot Device Structures

Thursday AM Room: 102
June 28, 2001 Location: University of Notre Dame

Session Chairs: Ben Shanabrook, Naval Research Laboratories, Nanostruct. Sec., Washington, DC 20375-5000 USA; Supriyo Bandyopadhyay, University of Nebraska–Lincoln, Dept. of Electl. Eng., Lincoln, NE 68588-0511 USA

8:20 AM (Student)

P1, Electric Field Dependent Spectroscopy of Quantum Dot Molecules: *B. D. Gerardot*[1]; I. Shtrichman[1]; C. Metzner[1]; W. V. Schoenfeld[1]; P. M. Petroff[1]; [1]University of California, Matls. Dept., Santa Barbara, CA 93117 USA

Electronically coupled quantum dot pairs (QD molecules) have been proposed to operate as quantum gates, the basic building blocks for quantum computation schemes [1]. Coupling between two QDs is highly sensitive to the relative state energies of the dots. These energies are fixed for each QD by its dimensions and material composition. By varying an electric field between the two QDs, one can bring the electronic states of the dots into and out of resonance. In this work we study the coupling between adjacent quantum dots by measuring the photoluminescence (PL) spectra under applied external electric field. The MBE grown samples contain an intrinsic layer embedded between two n-doped GaAs layers which serve as the front and back electrodes of the device (n-i-n structure). The intrinsic GaAs layer contains vertically stacked InAs QD layers with different separation distances (45 or 150Å). Two GaAs/AlAs superlattice barriers surround the GaAs layer to reduce current flow through the device. Using a micro-PL setup with spatial resolution of 1 μm and low QD density samples (~10^7 cm-2), we are able to optically isolate and study a single QD pair. We compare the spectra of a single QD, a single QD molecule, and a single electronically uncoupled QD pair. We use a continues wave Ti:Sapphire laser, operating at an energy below the GaAs barrier, to excite the samples through their front semi-transparent metal gate. In the single QD sample we observe, as the excitation intensity is raised, a number of sharp peaks in the micro-PL spectra in agreement with previous works [2, 3]. When varying the electric field at constant excitation intensity, we find the peaks in the spectra change their relative intensity, due to an effective change in the density of carriers in the QD. No shift in the positions of the peaks is observed with the applied field. The spectra of the sample with 150Å separated QDs strongly resemble the single QD sample results. Due to the difference in their size and composition, we observe PL peaks originating from the two uncoupled QDs. This behavior is in contrast with the results from the 45Å separated QDs. New peaks appear and disappear around the ground state while varying the electric field, together with a gradual shift of few meV. We suggest that this phenomenon is due to the coupling between the higher energy states of the larger QD and the lower energy states of the smaller QD. We will compare the results with a theoretical model which accounts for the important many-body effects. [1] A. Berenco et. al., PRL 74, 4083 (1995) [2] E. Dekel et. al., PRL 80, 4991 (1998) [3] F. Findeis, et. al., Physica E 7, 354 (2000).

8:40 AM (Student)

P2, Resonant Tunneling with High Peak-to-Valley Ratios Observed in InAs/InP Quantum Dot Stacks: *Magnus Lars Borgstrom*[1]; Tomas Bryllert[1]; Torsten Sass[1]; Boel Gustafson[1]; Lars-Erik Wernersson[1]; Werner Seifert[1]; Lars Samuelson[1]; [1]Lund University, Fasta tillståndets fysik, Box 118, Lund S-22100 Sweden

The continuous demand for smaller components requires that new approaches to device fabrication be found. Resonant tunneling diodes have been recognized as excellent candidates for digital circuit applications because of their high switching speed, low power consumption and reduced complexity in implementing a given function. Resonant tunneling through coupled, quasi zero-dimensional double dots in semiconductor nanostructures was first demonstrated by Reed et al.[1] who studied resonant tunneling in GaAs-based triple barrier diodes, 100 nm in diameter, produced by lithography and etching. Our approach uses the more elegant way of fabricating semiconductor quantum dots (QDs) by spontaneous three-dimensional islanding in lattice-mismatched material systems (self-assembling QDs) using low-pressure metal organic vapour phase epitaxy. Recently, resonant tunneling through self-assembled InAs QDs embedded in AlAs barriers on GaAs has been reported[2]. Due to the generally high dot density as a result of self-assembling, such tunneling devices usually contain millions of dots in the area that is probed, even if there are some indications that only a few of them are active in the tunneling process. We have been able to fabricate low-density samples of self-assembled InAs QDs on InP (001) with a mean InAs island density as low as 4x10E6 cm-2. This results in only about 150 dots below a macroscopic contact. Such low densities were obtained by deposition of 0.3 monolayer InAs. Additional InAs produced by the chemical reactions at the InP surface with arsine contributes to dot formation. We reported earlier on resonant tunneling through self assembled InAs QDs in a InP (substrate)/ GaInAs/InP/InAs (dots)/InP/GaInAs double-barrier structure, using such a low density sample. The peak-to-valley ratio was about[3]. In the present study we report on resonant tunneling through an improved sample with two InAs QD layers stacked in an InP triple-barrier structure. A much higher peak-to-valley ratio of 85 was observed at 7K. Negative differential resistance in the I-V characteristics was obtained up to a point above the temperature of liquid nitrogen. Due to the design of the structure, the upper (slightly larger) QD in the stack has the function of a 0-dimensional emitter. Electrons easily fill the upper dot, whereas tunneling through the entire structure is only allowed when two states in the dots align energetically, resulting in sharp resonant tunneling peaks with high peak-to-valley ratios in one of the bias directions. In addition to I-V measurements, the samples were characterized using transmission electron microscopy and atomic force microscopy. [1]M. A. Reed, J. N. Randall, J. H. Luscombe, W. R. Frensley, R. J. Aggarwal, R. J. Matyi, T. M. Moore, and A. E. Wetsel, Adv. Solid State Phys. 29, 267 (1989); [2]I. E. Itskevich, T. Ihn, A. Thornton, M. Henini, T. J. Foster, P. Moriarty, A. Nogaret, P. H. Beton, L. Eaves, and P. C. Main, Phys. Rev. B 54, 16401 (1996).

9:00 AM

P3, Enhanced Intraband Stark Effects in Stacked InAs/GaAs Self-Assembled: *Weidong Sheng*[1]; Jean-Pierre Leburton[1]; [1]University of Illinois at Urbana–Champaign, Beckman Inst. for Adv. Sci. & Tech., 405 N. Mathews Ave., Urbana, IL 61801 USA

We present a theoretical study of the electronic properties and intraband optical transitions in vertically aligned double InAs/GaAs self-assembled quantum dots (SADs) that are subject to an electric field along their growth axis. The electron properties are calculated as a function of the applied electric field by using an eight-band k.p Hamiltonian. The strain-dependent Hamiltonian is discretized on a three-dimensional grid as a large sparse matrix with tens of million non-zero elements, which is solved by Lanczos algorithm. Intraband transitions between ground s-like states and excited p-like states in the conduction band are almost three times stronger than in single SAD's as a results of the strain field generated by the two SAD's. Indeed, the oscillator strengths for these transitions are mostly determined by the central cell contribution to the wave function in the momentum matrix elements. The latter is consistently one order of magnitude larger than the contribution of the envelope functions, as a result of the strong mixing between conduction and valence band states. Hence, the strain field which extends into the barrier region between the stacked double SADs, significantly influences the hole states, which, via conduction-valence states mixing, also modifies the conduction band states, differently for single and double SADs, and produces the enhanced transition strength. The same effect involving the sensitivity of the conduction-valence mixing to external perturbation, is also responsible for a strong anisotropy of the intraband transitions resulting from the electric field orientation in stacked double SAD's compared to single SAD's. Stacked double SAD's also exhibit field tunable transitions between the bonding and antibonding s-like states resulting from the quantum mechanical coupling between the dots, with polarization along the growth axis. For a system consisting of two vertically aligned SADs that are truncated pyramids separated by three monolayers of GaAs, with the same base 17.4 nm and individual height 3.6 nm, the energy of this transition is tunable by bias voltage, and could cover a window of 11-24 μm. Therefore, mid-infrared photodetectors consisting of vertically-coupled double-quantum-dot layers are expected to exhibit enhanced sensibility and voltage tunability, compared to devices using single-quantum-dot layer.

9:20 AM (Student)

P4, Charging Kinetics and Charging Saturation Mechanisms of 2D Array Si Nanocrystals Embedded in a MOS Structure: *Christophe Busseret*[1]; Abdelkader Souifi[1]; Thierry Baron[1]; Gerard Guillot[1]; François Martin[2]; Marie Noël Semeria[2]; [1]INSA, LPM, Bat 502, 20 ave. A. Einstein, Villeurbanne 69621 France; [2]CEA Leti, 17 ave. des Martyrs, Grenoble 38054 France

After the first proposal of a memory transistor using silicon nanocrystals (nc-Si) as floating gates, the idea have done great progress. Actually, memories with nc-Si are seen as good candidate to fill the gap between SDRAMs and EEPROMs. In this study, we describe and explain the electric charge saturation in nc-Si. Si quantum dots with average diameters around 5 nm are deposited by Low Pressure Chemical Vapor Deposition on a tunnel oxide thermally grown on a P-type Si substrate. A 8-nm-thick control oxide is then deposited with a High Temperature Oxide process, and finally N+ polysilicon gates have been elaborated. We present a detailed investigation of electron or hole injection in the nc-Si. A positive gate biasing gives rise to electron tunneling from the inversion layer in the substrate towards the dots. The C-V curves are then positively shifted as compared with a reference sample without nc-Si. On the opposite, a negative bias leads to hole injection from the substrate accumulation layer towards the nc-Si. The dots charging kinetics shows a logarithmic shape that involves a variation of the tunneling transparency of the oxide with time. Indeed, the charge tunneling towards the dots modifies the electric field in the oxide and then, the following carriers that could migrate from the substrate do not "see" the same oxide transparency. The kinetics is then readily simulated as soon as the electric field in oxide is estimated. We have developed a method to express the electric field around the dots and then simulate the charging curves. The number of individual charges that can be stored by each dot is important (around five carriers). At low gate biases, the full charge is obtained after a few hundred seconds for the 2 nm tunnel oxide whereas it does not occur before 105 s for 3 nm. The charge saturation is shown to increase with the gate bias. We can model the charge saturation for the different tunnel oxide thickness. At low gate biases, the saturation appears as soon as the electric field due to the dots charge compensates the external applied electric field. The results show that our model fits very well with the technological parameters. At large gate bias, the saturation charge decreases with increasing the electric field. This behavior indicates a modification of the saturation mechanism. It is shown that at high gate voltages the charge mechanism can be modeled by taking into account the Fowler-Nordheim tunneling. The choice of the charging conditions is therefore a compromise between the charging velocities and the maximum charge that could be stored. The charging velocity increases with the bias but the strongest voltages do not involve the maximum charge at saturation.

9:40 AM

P5, Red Light Emitting InP/GaInP Quantum Dot Lasers: How the Mechanism of Operation Influences Their Performance: *Thomas Riedl*[1]; Jörg Porsche[2]; Ferdinand Scholz[2]; Andreas Hangleiter[1]; [1]Technical University of Braunschweig, Inst. of Techl. Phys., Mendelssohnstr. 2, Braunschweig D-38106 Germany; [2]University of Stuttgart, 4th Phys. Inst., Pfaffenwaldring 57, Stuttgart D-70550 Germany

Self-assembly of quantum dots (QDs) in the Stranski-Krastanow growth mode yields optical quality unsurpassed by any other fabrication technique. Especially in the material system InGaAs/GaAs there have been strong efforts by various groups to realize QD laser devices meeting the theoretical predictions. For longer cavities some of these lasers show threshold current densities lower than that of quantum well (QW) lasers. In the material system InP/GaInP, however, which offers the possibility to realize QD lasers emitting in the visible part of the spectrum, only quite recently the first single layer lasers operating at room temperature (RT) have been fabricated and will be presented here. The samples were

grown by low pressure metalorganic vapour-phase epitaxy (MOVPE) on (100) GaAs substrate tilted towards the (111)B plane by 15º. Power-dependent photoluminescence (PL), and optical gain measurements have been carried out and the consequences of our findings are directly compared to the emission characteristics of our InP/GaInP QD injection lasers. At low excitation densities we observe strong PL due to the QD ground state at 1.69-1.71 eV (90K) with a FWHM of 30 meV due to nonuniformities in size and shape. At higher excitation densities up to 4 QD-related PL transitions appear. They are almost equally spaced with an energetical distance of approximately 45 meV. At 90 K our lasers with a cavity length of 1.5 mm emit at 1.75 eV which is identified as lasing due to the first excited state of the QDs. Well above threshold multimode lasing is found and explained in terms of spectral hole burning due to a narrow homogeneous linewidth and the absence of coupling between different dots. Towards higher temperatures the emission blueshifts by about 20 meV to the next higher excited state of the QDs. Optical gain measurements clarify this behaviour. In contrast lasers with a 3 fold stack of QDs and a comparable cavity length show ground state emission up to room temperature due to a larger filling factor and thus reduced gain saturation. The temperature dependence of the threshold current density is analyzed in detail. At low temperatures an almost constant threshold (approx. 250 A/cm^2) validates the expected behaviour for QD lasers. Towards 300K a thermally activated increase is found and a T0 of 40K to 60 K at RT is determined. The rise in threshold current density is accompanied by a dramatic decrease of the quantum efficiency. Our observations will be described in terms of carrier leakage and nonradiative recombination. Finally the performance of the QD lasers is compared to QW lasers emitting at similar wavelengths and concepts for further improvement are discussed.

Session Q: Materials Integration: Wafer Bonding and Alternate Substrates

Thursday AM Room: 136
June 28, 2001 Location: University of Notre Dame

Session Chairs: Pete Moran, University of Wisconsin, Chem. Eng. Dept., Madison, WI 53706 USA; Karl Hobart, Naval Research Laboratory, Washington, DC 20375 USA

8:20 AM (Student)
Q1, Dislocation Dynamics of SiGe Film Relaxation on Silicon on Insulator Substrates: *Eric M. Rehder*[1]; T. S. Kuan[2]; T. F. Kuech[1]; [1]University of Wisconsin, Matls. Sci. Prog., 1415 Engineering Dr., Madison, WI 53706 USA; [2]University at Albany, State University of New York, Albany, NY 12222 USA

The incorporation of relaxed SiGe films with Si substrates allows new opportunities and applications within the range of Si electronics. Relaxed Ge is closely lattice matched to GaAs. Also, Si layers deposited on relaxed SiGe films are under a tensile strain, which results in a conduction band offset. This brings devices based on electron confinement and tunneling to Si substrates. Relaxed SiGe requires strain-relieving dislocations, which are accompanied by threading dislocations terminating at the surface of the film. The threading dislocations degrade electronic and optical device operation. Silicon on insulator(SOI) substrates have been found to be effective in reducing the threading dislocation density (TDD) in SiGe films. The SOI top Si layer thickness is expected to play a significant role in the dislocation dynamics during film relaxation, which is the focus of our present study. Samples have been grown with a 1µm $Si_{0.82}Ge_{0.18}$ film on a SOI substrate where the SOI top Si layer has a thickness ranging from 50nm to 10µm. For comparison, a reference film was deposited on a bulk Si substrate. All the films develop similar crosshatch. X-ray reciprocal space maps of the film and substrate (004) peaks determine the films on the two substrates to have comparable mosaic spread and strain. The crosshatch and X-ray data indicates that the relaxed films have a similar density of interfacial misfit dislocations. Also observed on the thinnest SOI substrates, the SOI top Si layer is under a tensile strain with a peak shift of 155 arc seconds. TEM analysis observed a low film TDD on the thin SOI substrates, which increases with Si layer thickness approaching bulk Si behavior for the thickest SOI substrates. Threading dislocations are also observed terminating at the buried oxide. On bulk Si, as a gliding dislocation approaches a misfit dislocation, the misfit dislocation is pushed into the substrate in order to allow the approaching dislocation to pass. These loops in the substrate lead to dislocation repulsion and form pile-ups. We present a modification of this mechanism accounting for the affect of the SOI buried oxide. The buried oxide provides an image force assisting the intersection by pulling dislocations into the substrate toward the softer oxide material. Upon entering the relaxed Si of the substrate these dislocation loops strain the Si due to constraint from the oxide and base wafer. Upon reaching the oxide interface the dislocation loops annihilate at the amorphous oxide leaving the observed buried threading segments. The annihilation and reduction in pile-ups on the SOI substrate allows relaxation to occur with fewer pinned dislocations and a lower film TDD.

8:40 AM (Student)
Q2, Modeling of In-Plane Expansion and Buckling of SiGe Islands on BPSG: *Haizhou Yin*[1]; James C. Sturm[1]; Zhigang Suo[1]; Rui Huang[1]; Karl D. Hobart[2]; [1]Princeton University, Ctr. for Photonics & Optoelect., POEM, J301, Princeton, NJ 08544 USA; [2]Naval Research Lab, Washington, DC 20357 USA

There has been increasing interest in compliant substrates for integration of heterogeneous epitaxial materials. In this talk, borophosphorosilicate glass (BPSG) on silicon is used as a compliant substrate to allow the relaxation of strained SiGe layers[1]. The talk will focus on the relaxation process and its modeling. For the first time, we show quantitative 2-D modeling of the relaxation process and of the buckling process, along with good correlation with experiments. The SiGe layers are first grown in a strained state on a (100) silicon wafer by CVD, and then bonded to the BPSG wafer. After the silicon substrate under the SiGe is removed by hydrogen implantation and cleavage, the SiGe is patterned into islands. The samples are then annealed at 800°C to allow the SiGe to relax. The relaxation takes place by two competing mechanisms: a desired in-plane expansion and an undesired out-of-plane bending (namely, buckling). The in-plane expansion of the SiGe islands is observed by X-ray diffraction from their (400) peak, while the buckling is measured by AFM. The characteristic time of in-plane expansion is linearly proportional to the island area. And the buckling rate is independent of the island size. Islands will buckle if the in-plane expansion alone is not fast enough to relax the strain. We study the buckling dependence of the island size and it clearly shows islands smaller than 40µm have negligible buckling. An analytical 2-D model for the in-plane expansion of the islands has been developed. It is in good agreement with our experimental data of small islands, but it underestimates the relaxation rate for larger islands. The underestimation stems from the fact that the analytical 2-D model for in-plane expansion ignores the relaxation contribution of the buckling. Surface roughness of the center of the 200µm SiGe islands is measured as a function of anneal time at 800°C to study the buckling rate. In-plane expansion in this case can be neglected because the center of large islands relaxes solely by buckling. A theory for buckling of thin film islands on viscous compliant substrate has recently been developed[2]. It is shown that the buckling amplitude grows exponentially over time. Our data agrees well with such predictions. The BPSG viscosity at 800°C can be independently extracted both from in-plane expansion and buckling modeling and the viscosities extracted are in close agreement. This is sound evidence that the models for 2-D in-plane expansion and buckling are valid in our case. This work is supported by DARPA(N66001-00-1-8957) and ARO (DAA655-98-1-0270). Reference: [1]K. Hobart, et. al. Journal of Electronic Materials, 29, 897 (2000); [2]N. Sridhar, D. J. Srolovitz and Z. Suo, to be published.

9:00 AM (Student)
Q3, High Quality Heteroepitaxial InGaAs Layers Grown on Strain Relaxed Seed Membranes Using the 'Paramorphic' Approach: *Mouloud Boudaa*[1]; Jean-Louis Leclercq[1]; Marie-Paule Besland[1]; Philippe Regreny[1]; Olivier Marty[2]; Guy R. Hollinger[1]; [1]Ecole Centrale de Lyon, LEOM, Ecully, Cedex 69621 France; [2]Université Lyon, 1 Lenac, Villeurbanne, Cedex 69621 France

The most common method for preparing relaxed mismatched layers is metamorphic heteroepitaxial growth, where strain is plastically and par-

tially relaxed in a graded buffer layer. However, threading dislocations are not completely eliminated which limits the electrical and optical properties of the epitaxial layers. To overcome these problems and as an alternative to compliant substrates, we have developed a new concept, the paramorphic approach that allows preparing ideally relaxed materials on seed membranes.[1] First, a thin strained seed layer is epitaxially grown on top of a sacrificial layer lattice-matched to the substrate. Then, the sacrificial layer is removed by selective chemical etching and subsequently, the seed layer separated from its original substrate is elastically relaxed and deposited on the substrate. Consequently, thick layers, lattice matched to the cubic strain relaxed seed membrane, are expected to be grown epitaxially without any structural defect. In practice, we use a microtechnology approach to prepare trampoline shape seed platforms, lattice mismatched to the substrate. Previously, we have demonstrated the validity of the paramorphic approach by growing (using molecular beam epitaxy-MBE) thick In0.65Ga0.35As layers on totally relaxed 50x50 µm2 In0.65Ga0.35As and InAs0.25P0.75 seed platforms 0.81% mismatched to InP[1]. Recently, we have focused on the preparation of larger platforms, compatible with the fabrication of optoelectronic devices. The limitation of the size of the platform is due to the non infinite etching selectivity between the seed layer and the sacrificial layer. As MBE regrowth is difficult on In0.65Ga0.35As, InAs0.25P0.75 seed layers are preferred. Using a bilayer made of InAsP and InGaAs for the seed strain relaxed layer, we succeeded to fabricate 300x300 µm2 platforms on InP. Moiré-fringes observed in plan-view TEM images of the platform/substrate interface proved the full and homogeneous elastic relaxation of the seed membranes. Up to 2µm In0.65Ga0.35As thick layers were grown without any structural defect as demonstrated by Nomarski microscopy, AFM imagery and cross-section TEM. 300K and 77K photoluminescence measurements show that the band gap energies found for layers of different thickness grown on the platforms are constant and equal to the expected values for relaxed materials (l~2µm at 300K). The superior quality of the material grown on the relaxed platform is demonstrated by a photoluminescence intensity 10 times higher at room temperature than on an unprocessed area. A PIN photodiode technology on 300x300 µm2 InAs0.25P0.75 seed membranes is in progress as well as work to reach operation wavelengths higher than 2µm using seed platforms with higher misfits. Results corresponding to thick InxGa1-xAs layers and InAs/ InAsxP1-x quantum well heterostructures grown on relaxed membranes will be presented. [1]J. F. Damlencourt, J. L. Leclercq, M. Gendry, P. Regreny and G. Hollinger, App. Phys. Lett. 75, 3638 (1999).

9:20 AM

Q4, Silicon on Sapphire Substrates Formed by Wafer Bonding: *P. D. Moran*[1]; T. F. Kuech[1]; [1]University of Wisconsin, Chem. Eng., 1415 Engineering Dr., Madison, WI 53706 USA

This work examines the feasibility of employing wafer bonding to make thin silicon on sapphire (SOS) structures that would serve as a better platform than heteroepitaxially grown SOS structures for the fabrication of high-speed, low-power electronics. Due to the difference in lattice constant and thermal expansion coefficients (TEC) between the Si and sapphire, a large number of extended defects are always present in the Si layers heteroepitaxially on sapphire forming conventional SOS structures. The wafer-bonding approach clearly eliminates defects due to the lattice mismatch in heteroepitaxial SOS structures. However, exposure of the bonded SOS structure to sufficiently high temperatures during subsequent device processing will result in TEC-induced defects in the silicon layer. Knowledge of the temperature at which a large number of TEC defects emerge in SOS structures is important for defining the thermal budget of subsequent device processing. The emergence of these defects can be detected by examining high-resolution x-ray diffraction (HRXD) rocking curves from a bonded SOS structure after exposure to increasingly higher temperature anneals. Four-inch diameter SOS heterostructures were formed by bonding a silicon-on-insulator (SOI) wafer to a sapphire substrate at room temperature and selectively removing the bulk of the native SOI wafer. The resulting structure consists of a ~200nm Si layer on a sapphire substrate with a 300nm thermal silicon dioxide layer between the silicon and sapphire wafer. HRXD rocking curve measurements from the structure after room temperature bonding and thinning are observed to have a FWHM = 90", in good agreement with theoretical simulation of that which would result from a defect-free Si layer. TEC-related defects detectable by an increase in diffuse scattering emerge upon cycling the bonded SOS structure to temperatures as low as 650°C, but not at 550°C. Upon exposure of the structure to 850°C, TEC induced defects result in a HRXD rocking curve FWHM of 400". Though significantly broader than the FWHM from a defect-free silicon layer (90"), the rocking curve is significantly narrower than the 900" FWHM from heteroepitaxially grown SOS. These results demonstrate that wafer bonding is a viable method for forming SOS structures with less structural defects than heteroepitaxially grown SOS material. The temperature range in which no defects were detected by HRXD from the bonded SOS is compatible with some SiGe epitaxial growth techniques.

9:40 AM (Student)

Q5, GaAs/GaN Diodes Wafer-Fused at 500°C: *Sarah Marie E. Monteith*[1]; Jacek Jasinski[3]; Andrew Huntington[2]; Andreas Stonas[2]; Larry Coldren[2]; Steven DenBaars[2]; Zuzanna Liliental-Weber[3]; Umesh Mishra[2]; Evelyn Hu[2]; [1]University of California, iQUEST Bldg. 981, Santa Barbara, CA 93106-9560 USA; [2]University of California, Matls. & Electl. & Comp. Eng. Depts., Santa Barbara, CA 93106-9560 USA; [3]Lawrence Berkeley National Laboratory, MSD 62-203, 1 Cyclotron Rd, Berkeley, CA 94720 USA

High-speed high-power devices could benefit dramatically from a heterostructure combining the high mobility of GaAs with the high breakdown fields achievable in GaN. The large lattice mismatch between these two materials precludes the growth of high quality heterostructures by conventional epitaxial methods. Wafer fusion, a technique which bonds two materials in intimate contact under elevated temperature and pressure, has been shown effective in forming heterostructure devices from lattice-mismatched materials (e.g. InP-GaAs, InGaAs-Si). From initial studies of the wafer-fused GaAs/GaN diode,*it seemed that thermally stable, high-melting point GaN would require a temperature of 750°C to undergo bond rearrangement and stable mechanical fusion to GaAs. However, our current work demonstrates that a mechanically stable and electrically active junction can be fused at 500°C. To our knowledge, this is the lowest process temperature reported for a GaAs/GaN fused interface. Such an improvement is vital to the development of a wafer-fused high-speed high-power electronic device; secondary ion mass spectrometry (SIMS) measurements verify that minimization of the process temperature and time is critical in preventing dopant diffusion and compensation across the fused junction. The starting materials for the fusion process are Si-doped n-GaN, grown by metal-organic chemical vapor deposition (MOCVD), and C-doped p-GaAs, grown by molecular beam epitaxy (MBE). The GaAs structure includes a buried sacrificial AlAs layer (0.3µm) to aid in the removal of the GaAs substrate after the fusion step. GaN is fused to GaAs under an applied pressure of 2MPa in a nitrogen ambient. Fusion conditions are varied over a range of temperatures (500-750°C) and times (0.25-1hour). The GaAs substrate and the buried AlAs layer are selectively removed in two consecutive wet chemical etch steps; this reveals 1µm of p-GaAs fused to n-GaN on sapphire. Diode structures are fabricated, contacted, and probed. Current-Voltage (I-V) measurements indicate leaky reverse-biased behavior. SIMS data reveal substantial diffusion of dopants and impurities, a situation which is alleviated, but not completely eliminated, by decreased process temperatures and times. These measurements will be presented, along with corresponding cross-sectional transmission electron microscopy (TEM) images. Together, this information describes the relationship between controllable fusion parameters and the resulting chemical and electrical quality of the GaAs/GaN fused junction. *L.S. McCarthy, J.G. Champlain, P. Kozodoy, G. Parish, R.K. Sink, and U.K. Mishra, "First Demonstration of a GaAs/GaN Fused p-n Heterojunction," presented at the TMS Electronic Materials Conference, 1998.

10:00 AM Break

10:20 AM (Student)

Q6, GaN MSM Photodetectors on Lithium Gallate: Demonstration of Performance and Integration Onto Si: *Sa Huang*[1]; Sangbeom Kang[1]; William A. Doolittle[1]; Sang-Woo Seo[1]; Kyeong Lee[1]; Nan M. Jokerst[1]; April S. Brown[1]; [1]Georgia Institute of Technology, Microelect. Rsrch. Ctr., 791 Atlantic Dr., Atlanta, GA 30332-0250 USA

The development of nitride-based optoelectronics and electronic devices on sapphire and SiC substrates has attracted considerable research activities. Lithium gallate (LiGaO2) is promising substrate material due to its relatively small lattice mismatch to GaN of only 0.9%, and its promise as an easily removable growth platform to enable heterogeneous

materials integration. In this abstract, we report the first performance of a GaN device (MSM photodetector) grown on LiGaO2, and our success in the integration of the device with Si substrates. The GaN device structures were grown by rf-plasma enhanced molecular beam epitaxy (MBE). The films were characterized with x-ray diffraction, Hall measurements, AFM and photoluminescence. Platinum and gold Schottky contacts were used for the device fabrication. The substrate was removed via an epitaxial lift-off process using an HF (mixed with water 1:10) etch. The device was then bonded onto bare Si and metal-coated Si wafers. We have found that the surface morphology of the substrate and the film significantly affect the performance of the device. We have developed a CMP process for the LGO to realize device quality material. The rms roughness of the substrate is reduced to 0.1nm after polishing. The LGO substrate removal rate is approximately 4.5 mm/minute. The substrate is easily removed without damaging the film. Device sizes are in the range of 50mm-150mm. We are exploring the relationships between device/film size and ease of integration. Films and devices exhibit curling and breakage for larger sizes due to defects and strain in the film. After bonding, the dark current and responsivity are unchanged from that achieved before integration. Our GaN/ LiGaO2 material exhibits dislocation densities of approximately 10^7-10^8 cm^{-2} and x-ray diffraction full widths at half maximum (FWHM) of 75 arcsec. The devices exhibit a high responsivity of 0.105 A/W at a reverse bias voltage of 20 V at 308 nm, and low dark currents of 7.88 pA at a 60V and 0.1 pA at 2V reverse bias.

10:40 AM

Q7, The Integration of Continuous-Wave InGaN Multiple-Quantum-Well Laser Diodes with Copper and Diamond Substrates by Laser Lift-Off: *William S. Wong*[1]; Michael Kneissl[1]; David W. Treat[1]; Mark Teepe[1]; Naoko Miyashita[1]; Noble M. Johnson[1]; [1]Xerox Corporation, Palo Alto Rsrch. Ctr., Elect. Matls. Lab., 3333 Coyote Hill Rd., Palo Alto, CA 94304 USA

An effective means for improving blue-laser performance can be achieved by thin-film lift-off and transfer of prefabricated, fully functional devices from sapphire onto another host substrate. Although high-performance continuous-wave (In,Ga,Al)N laser diodes (LDs) possessing lifetimes greater than 10000 hours have been realized on sapphire substrates,[1] a major impediment to the development of III-nitride LDs still remains the efficient dissipation of heat generated from the active area of the device. The high thermal resistance of the sapphire substrate and the relatively high current densities combine to degrade the device performance and lifetimes due in part to excessive heating during operation. Substrates such as copper or diamond would be more ideal in terms of thermal conductivity although direct deposition and fabrication of III-nitride-based laser devices on these materials are either unfeasible or result in poor-quality thin films. Thin-film laser lift-off (LLO) techniques have recently been established as an effective tool for combining GaN thin films with a variety of dissimilar substrates.[2] As further illustration of this integration methodology, we describe and demonstrate the transfer of prefabricated continuous-wave InGaN multiple-quantum-well (MQW) ridge-waveguide LD from sapphire onto Cu and diamond substrates. Reduced threshold currents and increased differential quantum efficiencies were measured for LDs on Cu due to a 50% reduction of the thermal impedance. Light output for LDs on Cu was three times greater than comparable LDs on sapphire with a maximum output of 100 mW. CW operation was possible up to heatsink temperatures of 90°C for LDs on Cu and diamond. In addition to improved device performance, the removal of the sapphire growth substrate constraint allows for easily cleaved mirror facets and fabrication of LD structures with a backside n-contact through the conductive Cu substrate. Cross-sectional scanning electron microscopy and atomic force microscopy showed improved surface roughness (< 0.5 nm rms) for the cleaved mirrors over conventional etched mirrors. The combined enhanced device performance and ability to form cleaved mirror facets further establishes the use of LLO as a viable tool for materials integration. [1]S. Nakamura, M. Senoh, S. Nagahama, N. Iwasa, T. Yamada, T. Matushita, Y. Sugimoto, T. Kozaki, H. Umemoto, M. Sano, and K. Chocho, Jpn. J. Appl. Phys., Part 2 v. 37, L627 (1998). [2]W.S. Wong, A.B. Wengrow, Y. Cho, A. Salleo, N.J. Quitoriano, N.W. Cheung, and T. Sands, J. Electron. Mater. v. 28,1409 (1999).

11:00 AM

Q8, Formation of Hybrid SiC/Si and SiC/SiO2/Si Wafers by Oxygen Implantation, Wafer Bonding and Etching: *J. T. Torvik*[1]; R. Krutsinger[1]; B. Van Zeghbroeck[2]; T. A. Winningham[3]; K. Douglas[3]; W. Wesch[4]; [1]Astralux, Inc., 2500 Central Ave., Boulder, CO 80301 USA; [2]University of Colorado at Boulder, Dept. of ECE, Boulder, CO 80309 USA; [3]University of Colorado at Boulder, Dept. of Phys., Boulder, CO 80309 USA; [4]Friedrich-Schiller-Universitaet Jena, Institut fuer Festkoerperphysik, Max-Wien-Platz 1 Jena, Jena D-07743 Germany

We demonstrate the use of oxygen implantation, wafer-bonding, and chemical etching to transfer thin SiC membranes onto a substrate of choice such as Si and SiO2. The ultimate goal is to make large-area single-crystal hybrid SiC wafers on substrates optimized for electrical, thermal or insulating properties. The main application for this technology is insulating substrates for RF applications, but also include conducting substrates for near-dc power and optoelectronic devices and possibly even seeds for large-diameter boule growth. The wide bandgap semiconductors SiC and III-nitrides are excellent candidates for compact, high power, high-temperature, and high-speed devices due to these material's extraordinary high thermal conductivities, high breakdown fields, and high saturated electron velocities. Wide-bandgap transistors such as SiC-MESFETs and AlGaN-HEMTs have just recently surpassed the theoretical limits of their Si and III-V arsenide counterparts in terms of high-temperature operation and RF-power performance. Despite this achievement, these devices often exhibit trapping related problems such as backgating and gain compression. Thus, the availability of semi-insulating SiC substrates with a low defect density is crucial for developing wide bandgap microwave power devices. Unfortunately, bulk semi-insulating SiC wafers are expensive and only commercially available up to 2-inches in diameter. The Smart Cut process[1] has been explored as an alternative method of fabricating SiC wafers. The Smart Cut process uses hydrogen implantation and a high temperature treatment to "slice" off a thin SiC membrane from a bulk SiC wafer. This membrane can subsequently be bonded to another substrate. In this work, we discuss using oxygen implantation and chemical etching to make hybrid SiC wafers. Our three-step process consists of: 1) forming a buried oxide layer in a SiC wafer by oxygen implantation, 2) wafer-bonding of the SiC wafer to SiO2/Si and Si wafers, and 3) lifting-off (or delaminating) the thin SiC membrane by chemical etching. First, 4H-SiC was ion-implanted with 1e18 O+/cm2 at 700ºC, forming a buried SiOx layer roughly 1µm below the SiC surface. Second, we developed a highly reproducible process for direct wafer bonding of SiC to either conducting (Si) or insulating substrates (SiO2) under uniaxial pressure at temperatures up to 1000ºC. Third, an efficient lift-off process by etching in diluted hydrofluoric acid was developed leaving a thin SiC membrane on the Si and SiO2 substrates. We demonstrate a high-quality structural and electrical interface, good reproducibility and high yield. Data on scaling this process to large diameters will be discussed. The effect of using wafers cut on and off-axis and Si- and C-faces will also be discussed. [1]L. Di Cioccio et al. "SiC on insulator formation using the Smart Cut process", El. Lett. 32, 1144, (1996).

11:20 AM

Q9, Wafer Bonding Fabrication of High Voltage Power Electronic Devices: *K. D. Hobart*[1]; F. J. Kub[1]; [1]Naval Research Laboratory, Code 6813, 4555 Overlook Ave. S.W., Washington, DC 20375 USA

Direct wafer bonding has been successfully applied to the fabrication of high voltage, high power switching devices. Two device concepts have been demonstrated with the direct wafer bonding technique: (1) a fast-turn-off insulating gate bipolar transistor (IGBT) and (2) a very high voltage thyristor. The motivation behind this work is to exploit the direct wafer bonding process to produce switching transistors that extend the functionality and performance of Si power devices. Power devices, especially high voltage devices, are particularly attractive to wafer bonding processes because the devices are quite thick in order to stand off the required voltage. In this work we demonstrate that direct wafer bonding can be used to join two fully functional IGBTs into a single double-side, double-gate IGBT or D-IGBT that has improved performance. Additionally, we show that very thick, large area thyristors can be fabricated by joining two halves of the transistor to produce a device that is capable of standing off over 7kV and passing 3kA. The bonding process also allows for vertical engineering, for example, for lifetime reduction in the central region of the device where charge control is most important. The bonding process relies on hydrogen termination of the bonding surfaces

using an HF-last process to achieve an electrically transparent bond interface. The bonding processes described here are performed in atmosphere. Previous work has shown that this interface is of high electrical quality if the temperature range between 700 and 900°C is avoided. For the bonding of fully functional IGBT wafers, the bonding temperature is limited to 400°C because of the Al metalization. To achieve sufficient bond strength for dicing and packaging of the devices, a long furnace exposure is required (~5 hours) but is not detrimental to device performance. Fabrication of the thyristors is not limited to low temperatures and a high temperature bond anneal (>1000°C) is performed followed by back end fabrication (gate definition, metalization, passivation and packaging). The performance of the two device types where characterized with both static and dynamic methods. Compared to the control IGBT, the D-IGBTs showed much lower (40%) forward drop, $V_{CE(Sat)}$, due to the presence of the p^+ base of the bottom transistor (now collector) which provided enhanced hole injection. By turning the bottom transistor "on" prior to turning the top transistor "off", hole injection was extinguished prior to the switching event resulting in a reduction of the turn-off time and switching loss. The bonded thyristors showed similar forward drop to control devices (<5V at 2.8kA) but the bonded devices showed improved switching behavior due to lifetime killing in the center region of the device. Summarizing, wafer bonding has successfully been applied to the fabrication of high performance high power switching transistors.

11:40 AM

Q10, Electrical and Optical Characterization of Wafer-Bonded 4H/6H-SiC and SiC/Si N-p Heterojunction Diodes: *John T. Torvik*[1]; Ross Krutsinger[1]; Bart Van Zeghbroeck[2]; [1]Astralux, Inc., 2500 Central Ave., Boulder, CO 80301 USA; [2]University of Colorado at Boulder, Dept. of Electl. & Comp. Eng., Boulder, CO 80309 USA

In this work, we demonstrate discrete SiC bandgap engineering by direct wafer bonding of 4H-SiC to 6H-SiC and Si for bipolar device applications. SiC is an extraordinary semiconductor with high thermal conductivity, high breakdown field, high saturated electron velocity, radiation hardness, and chemical inertness. Hence, SiC lends itself to a variety of commercial power devices applications, which is a field currently dominated by traditional Si and III-V devices. Nevertheless, the potential of SiC devices in the power device area is evident by the reports of Bipolar Junctions Transistors, Metal Oxide Semiconductor Field Effect Transistors and Metal-Semiconductor Field Effect Transistors exceeding the theoretical performance limits of its Si and GaAs counterparts. Unfortunately, more sophisticated SiC-based microwave devices, such as heterojunction bipolar transistors, are not yet practical due to the absence of SiC bandgap engineering. SiC bandgap engineering has proven elusive due to the difficulty of polytype control (4H, 6H, 3C etc.) during growth and the binary nature of SiC. 4H-SiC (0001) was bonded to 6H-SiC (0001) and bulk Si (100) wafers under uniaxial pressure at temperatures up to 1000ºC. The process resulted in a strong bond free of large defects such as voids and cracks. Large-area 3x3 mm2 SiC/Si n-p heterojunction diodes were fabricated and the current-voltage (I-V) traces exhibit rectifying diode characteristics. Specifically, the I-V characteristics exhibit a reverse leakage current density of 0.9 mA/cm2 at -20 V, and an on-state forward current density of 0.26A/cm2 at 3V. A built-in potential of 1.2 eV was extracted from capacitance-voltage measurements indicating that SiC/Si forms a Type I heterojunction with conduction and valence band offsets of 0.6eV and 1.5 eV, respectively. Similarly, large-area 3x3 mm2 wafer bonded 4H-SiC/6H-SiC n-p heterojunction diodes were fabricated and characterized using electrical and optical techniques. The current-voltage characteristics exhibit a reverse leakage current density of 0.8 mA/cm2 at -30V and an on-state forward current density of 0.5 A/cm2 at 5V. Minority carrier injection across the bonded n-p interface was confirmed by electroluminescence spectroscopy.

Session R: Doping and Defects in Group III – Nitrides and ZnO

Thursday AM Room: 155
June 28, 2001 Location: University of Notre Dame

Session Chairs: Christian Wetzel, Uniroyal Optoelectronics, Tampa, FL 33619 USA; James Speck, University of California–Santa Barbara, Dept. of Matls., Santa Barbara, CA 93106 USA

8:20 AM

R1, Sub-Micron Scale Photoluminescence Images of Epitaxially Laterally Overgrown GaN at a Low Temperature: *Masahiro Yoshimoto*[1]; Junji Saraie[1]; Shuji Nakamura[2]; [1]Kyoto Institute of Technology, Dept. Elect. & Info. Sci., Matsugasaki, Sakyo, Kyoto 606-8585 Japan; [2]University of California–Santa Barbara, Matls. Dept., Santa Barbara, CA 93106 USA

Epitaxially lateral overgrowth (ELO) has been extensively studied for reduction of the dislocation density of GaN. In this work, microscopic photoluminescence (μ-PL) images of ELO GaN with a spatial resolution of 0.3 μm were obtained at 15K with a newly developed PL microscope. Although the spatial resolution could not be reduced beyond the diffraction limit in the PL microscope using a conventional objective, its high optical throughput resulted in a high signal/noise ratio. Monochromated μ-PL images for the emission ascribed to excitons bound to donors (D^0X) visualized an inhomogeneous incorporation of donors in ELO GaN. An improvement of the crystallinity characterized based on the intensity of free-exciton emission (E_{XA}) was also described. GaN was grown by a two-flow metalorganic chemical vapor deposition (MOCVD). In ELO GaN growth, a striped mask consisting of SiO_2 was deposited on a GaN layer grown on a sapphire (0001)-oriented substrate. The striped mask was formed along GaN <1-100> direction with a width of 16 μm and a separation of 9 μm. The ELO GaN with a thickness of 15 μm was grown on the GaN with the striped mask. The selectively grown GaN fully coalesced on the SiO_2 mask. The areas of GaN grown on the opening and the stripe are called as a window region and a wing region, respectively, in this abstract. The PL spectra in both the plan-view and cross-sectional alignments were dominated by the E_{XA} peak at 3.494 eV and the D^0X peak at 3.487 eV. Cross-sectional PL images were obtained for a sample cleaved perpendicular to the direction of the SiO_2 mask. The E_{XA} emission in the wing region became around twice as intense as in the window region, showing an improvement of the crystallinity in the wing region. The E_{XA} intensity increased along the growing direction. In the cross-sectional images for D^0X, a bright emission was observed in an area of the wing region within a distance of around 8 μm from the mask. In plan-view observation, the D^0X emission was suppressed at the center of the wing region. Taking account that the value of 8 μm is half width of the SiO_2 mask (16 μm), the incorporation of donors such as Si atoms is enhanced during the lateral growth. The peripheral area of the wing region was adhered to the SiO_2 mask for a longer time than the central area of the wing region during ELO growth. This probably causes the enhancement of the donor incorporation in the peripheral area. Once GaN coalesces on the SiO_2 mask, the incorporation of donors is suppressed.

8:40 AM

R2, Dislocation Electrical Activity in GaN Films Grown By Molecular Beam Epitaxy: *Julia W. P. Hsu*[1]; Michael J. Manfra[1]; David V. Lang[1]; S. N. G. Chu[1]; C. H. Chen[1]; Loren N. Pfeiffer[1]; A. M. Sergent[1]; [1]Lucent Technologies, Bell Labs., 600 Mountain Ave., Murray Hill, NJ 07974 USA

Gate leakage in MBE GaN films grown on HVPE templates was investigated using macroscopic Schottky diode measurements and scanning current-voltage microscopy (SIVM). These results were correlated with structural and chemical information obtained by TEM. We will present results on how dislocation electrical activity depends on the type of

dislocation and growth stoichiometry. The reverse bias leakage current in macroscopic GaN Schottky diodes is found to be insensitive to barrier height. Using a scanning current-voltage microscope, we show that the reverse bias current occurs at small isolated regions, while most of the sample is insulating. By comparing the current maps to topographic images and transmission electron microscopy results, we conclude that reverse bias leakage occurs primarily at dislocations with a screw component. Edge dislocations apparently do not contribute significantly to excess reverse bias leakage in GaN. Furthermore, both SIVM and macroscopic Schottky diode results show that MBE films grown under Ga-rich conditions have orders of magnitude higher reverse bias leakage than films grown under Ga-lean conditions. Cross sectional TEM images of Ga-rich films show ≤ 100 nm size bumps exclusively at the surface terminations of screw dislocations. Energy dispersive X-ray spectroscopy taken with a 15 nm size beam on the cross sectional TEM samples reveals that Ga and O are the two dominant elements in these bumps, indicating that they are oxidized Ga particles and not GaN. TEM images taken under kinematic conditions show a much stronger contrast for dislocations with a screw component in the Ga-rich sample than those in the Ga-lean sample. This is consistent with excess Ga in the vicinity of dislocations with a screw component when grown under Ga-rich conditions. Hence, we conclude that excess Ga associated with dislocations with a screw component, rather than intrinsic dislocation gap states, is responsible for excess reverse bias leakage in MBE GaN.

9:00 AM

R3, Phosphoric Acid Decoration Etch of Defects in HVPE and MOVPE GaN: *X. Xu*[1]; R. P. Vaudo[1]; J. S. Testa[1]; J. A. Malcarne[1]; J. S. Flynn[1]; G. R. Brandes[1]; [1]ATMI, Inc., 7 Commerce Dr., Danbury, CT 06810 USA

The type and density of defects in GaN epitaxial layers strongly impact the performance of GaN-based devices. The defect density is large in device epilayers grown by metal-organic vapor phase epitaxy (MOVPE) on foreign growth templates because of the large lattice mismatch and the close proximity of the device epilayers to the growth interface. GaN substrates grown using the hydride vapor phase epitaxy (HVPE) technique are lattice matched, but defects present in the substrate will propagate to the epilayer. Transmission electron microscopy is a tested technique for examining defects in nitride materials, but the process is too laborious and expensive to be used for routine feedback. Wet etching is attractive because it is simple to implement, inexpensive and fast. However, the effectiveness of wet etching of GaN to reveal defect density is still not well established and has not been applied in the same study to materials produced by different growth techniques and with different defect densities. We report the results of a systematic investigation of hot phosphoric acid etching of GaN grown using HVPE and MOVPE techniques. Specifically, we etched, counted and characterized defects in thin (2-3 m) GaN films grown on sapphire and silicon carbide by MOVPE, thick (>200 m) GaN films grown on sapphire by HVPE, and polished free-standing GaN substrates produced by HVPE. The GaN materials were etched in concentrated (85%) phosphoric acid at temperatures of 160-200°C for a time period of 5-20 minutes. Atomic force microscopy (AFM) was used to examine the surfaces after etching. Hot phosphoric acid was found to be very effective in revealing defects on the GaN surface, but samples prepared by the different techniques required different etch conditions in order to best reveal the defects. MOVPE GaN films grown on SiC required longer etch times at higher temperature compared with films grown on sapphire. The trend corresponds, but may not be fully explained, by the higher dislocation density of material grown on sapphire (~1x109 cm-2 on SiC, ~5x109 cm-2 on sapphire). As etch time is increased, additional defects become apparent. For the case of GaN on SiC, etch pits are visible at step terminations and are mixed-type or pure-screw dislocations. Etching for 20 min at 180ºC revealed additional smaller pits not located at step terminations; we hypothesize these are pure-edge dislocations. The rougher surface morphology of as-grown HVPE films made it difficult to accurately determine defect density. However, once polished, 5 minutes of etching at 180ºC was sufficient to clearly decorate defects. The observed defect density of 2x107 cm-2 was comparable to TEM-measured values. A detailed comparison and discussion of the wet etching and TEM identification of defects in HVPE and MOVPE GaN materials will be presented.

9:20 AM

R4, Deep Centers With Anomalous Capture Behavior in Free-Standing GaN: *Zhaoqiang Fang*[1]; David C. Look[1]; P. Visconti[2]; C.-Z. Lu[2]; D.-F. Wang[2]; Hadis Morkoc[2]; S. S. Park[3]; K. Y. Lee[3]; [1]Wright State University, Semicond. Rsrch. Ctr., 3640 Colonel Glenn Hwy., Dayton, OH 45435 USA; [2]Virginia Commonwealth University, Electl. Eng. & Phys. Dept., PO Box 843072, Richmond, VA 23284 USA; [3]Samsung Advanced Institute of Technology, PO Box 111, Suwon 440-600 Korea

Hydride vapor phase epitaxy (HVPE) is a promising technique for growing thick GaN layers, which can be used as substrates after removal from the sapphire (the separated thick layer is called “free-standing” GaN). The GaN layer used in this study was grown to a thickness of about 300 microns, and then separated by a laser decomposition process. The top (Ga) surface was mechanically polished followed by reactive ion etching and wet-chemical etching. Schottky barrier diodes (SBDs) were then fabricated by depositing Ni/Au Schottky contacts on the top surface (Ga-face) and a large Ti/Al/Ti/Au ohmic contact on the opposite surface. The SBDs showed very good 300-K I-V characteristics, with leakage currents as low as 10^{-7} A/cm^2 at a reverse bias (V_b) of -10 V. Deep level transient spectroscopy (DLTS) measurements made on several SBDs, using different filling pulse heights (V_f), revealed the presence of five electron traps, i.e. A_1 (with an activation energy E_T=1.0 eV), A (E_T=0.66eV), B (E_T=0.59 eV), C (E_T=0.34 eV), and D (E_T=0.25 eV). The same traps are often found in epi-GaN grown by other techniques. However, the prominence of trap C found in the free-standing GaN might be related to the surface damage, since the trap C can be detected only near the top surface region (~3000 Å). In addition to these traps, two new traps A’ (with E_T=0.77 eV) and B’ (with E_T=0.46 eV) were observed. Unlike the case for trap C, the traps A’ and B’ have been confirmed to be bulk traps and are influenced by the high electric field in the depletion region. Also in contrast to the other traps, traps A’ and B’ were found to be strongly dependent on the filling pulse width (W_f) used in the DLTS measurements, and in fact become dominant traps as W_f increased. Good fits of DLTS peak height versus W_f for both traps can be obtained if we assume that they are due to “line- defects”. As studied by Wosinski for dislocation-related electron traps in plastically deformed n-GaAs [J. Appl. Phys. 65, 1566 (1989)], the electron capture rate is limited by a time-dependent Coulomb barrier, with the barrier height proportional to the number of electrons already trapped, resulting in an almost linear dependence of the DLTS peak height on logarithmic W_f. Some evidence, obtained from repeated DLTS measurements over a period of several weeks on SBDs made on a similar GaN layer, indicates that traps A’ and B’ grow in intensity, evidently due to localized material changes.

9:40 AM

R5, Polarity Dependence of Nitrogen-Doping into ZnO Layers Grown on GaN Templates by Plasma-Assisted Molecular Beam Epitaxy: *Hang-Ju Ko*[1]; Yefen Chen[1]; Soon-Ku Hong[1]; Takafumi Yao[1]; [1]Tohoku University, Yao Lab., Inst. for Matls. Rsrch., Katahira 2-1-1, Aoba-ku, Sendai 980-8577 Japan

This paper reports the different incorporation behaviors of nitrogen acceptors into ZnO layers with different polarities grown on GaN templates by plasama-assisted molecular beam epitaxy (P-MBE). The structural and optical properties also show clear difference for N-doped ZnO layers with different polarities. ZnO has attracted great attention for the application to excitonic optical devices due to extremely large excitonic binding energy of 60 meV[1]. P-MBE growth of high-quality undoped ZnO layers[2] and highly-doped n-type ZnO layers[3] have been already reported. Hence the growth of high-quality p-type ZnO is crucial to the fabrication of light-emitting devices. However, p-type doping technique has not been established yet, in spite of several reports on p-ZnO using either As doping[4] or codoping of Ga and N[5]. It is obvious that we need more ZnO has the wurtzite structure: the (0001)ZnO plane of is terminated by Zinc (Zn-polar), while (000-1)ZnO is terminated by oxygen (O-polar). Since nitrogen has stronger bond strength with Zn than with oxygen, different indorporation of nitrogen can be expected. The polarity of ZnO layers grown on GaN templates by P-MBE can be controlled by engineering the interface structure [6]. This paper reports nitrogen doping into ZnO layers with different polarities. N-doping into ZnO films was performed at 500°C using (N2 + O2) rf-plasma. The flow-rate ratio of nitrogen to oxygen gas was fixed to 0.1. The Zn to O beam pressure ratio is kept to maintain oxygen rich growth conditions. RHEED showed a spotty pattern during growth for both polarities. The (0002) omega-rocking curve

of x-ray diffraction of N-doped ZnO films show a well-defined Gaussian shape. The typical linewidth of the diffraction curve for of N-doped ZnO with Zn-polarity is 7 arcmin, which is narrower than that of N-doped ZnO with O-polarity (13 arcmin). Most interestingly, the lattice parameter along c axis of ZnO:N with Zn-polarity, which is measured by high resolution XRD of (006)ZnO, is by 0.004 nm larger than that of ZnO:N with O-polarity which is located at almost the same angle as that of undoped ZnO. Low temperature photoluminescence (PL) studies also show clear difference for both types of N-doped ZnO layers. The typical PL spectrum of N-doped ZnO films with O-polarity shows only week excitonic emission, while the PL of N-doped ZnO films with Zn-polarity shows very strong exciton emission and deep level emission. The excitonic emission lines are located at 3.357 eV and 3.360 eV. The intensity ratio of excitonic emission lines of N-doped ZnO samples with Zn- to O-polarity is 4. The observed PL spectra and XRD suggest that N-incorporation is enhanced during doping into Zn-polar ZnO. Preliminary electrical measurements show the growth of high-resistive ZnO layers as compared with the typical carrier concentration of 1017cm-3 for undoped ZnO layers. In conclusion, we have observed different incorporation of nitrogen acceptors into ZnO layers with different polarities with more efficient nitrogen doping into Zn-polar ZnO layers than O-polar ZnO.
References: [1]D. M. Bagnall, Y. F. Chen, Z. Zhu, T. Yao, S. Koyama, M. Y. Shen, T. Goto, Appl. Phys. Lett., 70, 2230(1997); [2]H. J. Ko, Y. F. Chen, T. Yao, K. Miyajima, A. Yamamoto, T. Goto, Appl. Phys. Lett., 77, 537(2000); [3]H. J. Ko, Y. F. Chen, S. K. Hong, H. Wenisch, T. Yao, D. C. Look, Appl. Phys. Lett., 77, 3761(2000); [4]Y. R. Ryu, S. Zhu, D. C. Look, J. M. Wrobel, H. M. Jeong, H. W.Whit, J. Cryst. Growth, 216, 330(2000); [5]M. Joseph, H. Tabata, T. Kawai, Jpn. J. Appl. Phys., 38, L1205(1999) [6]S. K. Hong, T. Hanada, H. J. Ko, Y. Chen, T. Yao, D. Imai, K. Araki, M. Shinohara, Appl. Phys. Lett. 77, 3571(2000).

10:00 AM Break

10:20 AM

R6, Controlled n-Type Doping Using Oxygen in GaN Grown by rf Plasma Molecular Beam Epitaxy: A. J. Ptak[1]; L. J. Holbert[1]; C. H. Swartz[1]; Lijun Wang[1]; N. C. Giles[1]; *T. H. Myers*[1]; G. C. B. Braga[2]; J. A. Freitas[3]; D. D. Koleske[3]; R. L. Henry[3]; A. E. Wickenden[3]; C. Tian[4]; A. Hockett[4]; S. Mithra[4]; P. Van Lierde[4]; [1]West Virginia University, Dept. of Phys., PO Box 6315, Morgantown, WV 26506 USA; [2]Universidade de Brasilia, Inst. of Phys., Brazil; [3]Naval Research Laboratory, Elect. Sci. & Tech. Div., Washington, DC 20375 USA; [4]Evans Analytical Group, Charles Evans & Assoc., Redwood, CA 94086 USA

Oxygen is a well-recognized n-type impurity in GaN and is possibly the origin of the large n-type background in GaN grown by many techniques in many systems. Molecular beam epitaxy (MBE) growth of GaN at West Virginia University has resulted in layers with low residual n-type backgrounds (< 5x1015 cm-3) due to both controlled growth species and an extremely clean growth environment. This has allowed a systematic study of oxygen incorporation kinetics and the resultant electrical and structural properties of oxygen-doped GaN to be studied. The O-doped GaN layers were grown by rf plasma-assisted MBE using an EPI Unibulb nitrogen plasma source. A conventional effusion cell was used for Ga. N-polarity GaN was obtained by nucleating GaN buffer layers directly on sapphire under heavily Ga-rich conditions. Incorporation in Ga-polarity GaN was studied by growth on (0001)-oriented MOCVD GaN templates grown on a-plane sapphire substrates supplied by NRL. Oxygen step-doped structures were produced by sequentially opening and closing a precision leak valve. O partial pressures were continuously monitored with a mass spectrometer. In-situ growth rates were monitored using laser interferometry. Secondary ion mass spectrometry (SIMS) determination of O concentrations was performed at Charles Evans and Associates (Redwood, Ca). Doping profiles obtained this way were quite sharp, with O levels almost immediately dropping to the initial background levels. O incorporation was found to be linear with system O partial pressure. Oxygen incorporation was found to be a factor of 10 larger on N-polarity samples. O incorporation rates were fairly constant for Ga-rich growth, but were found to increase by over a factor of 100 in going from Ga-rich to N-rich growth. O was incorporated at levels between < 1016 to 1 x1020 cm-3. A series of uniformly O-doped layers were also grown and characterized by Hall effect, photoluminescence, Raman and FTIR measurements. N-type carrier concentrations were found to track well with O incorporation, indicating little, if any, compensation. Electrical activation energies are consistent with a ~35 meV donor energy level for O in GaN. N-type carrier concentrations up to 5 x1019 cm-3 have been obtained. Raman studies indicate that O-doping may induce less strain than Si in GaN. These and other characterizations will be discussed during this talk. This work was supported at WVU by ONR Grant N00014-96-1-1008 monitored by Colin E. C. Wood.

10:40 AM (Student)

R7, Optical Memory Effects and Yellow Luminescence in GaN: *Y. C. Chang*[1]; A. E. Oberhofer[1]; J. F. Muth[1]; R. M. Kolbas[1]; R. F. Davis[2]; [1]North Carolina State University, Electl. & Comp. Eng., 232 Daniels Hall, Raleigh, NC 27695-7911 USA; [2]North Carolina State University, Matls. Sci. & Eng., Raleigh, NC 27695-7907 USA

Several groups have reported the metastable nature of defect-related levels in III-V nitrides including optical metastability in bulk GaN single crystals, reconfigurable optical properties in InGaN/GaN heterostructures and InGaN/GaN quantum wells, and electrical metastability in the form of persistent photoconductivity. Here we report on optical metastability and its relation to the so-called sub-bandgap yellow luminescence in GaN samples grown on SiC and sapphire substrates. Brief exposures to a high intensity ultraviolet light (20 µm spot; 30 kW/cm2; 250 fs; 280 nm) resulted in temporary changes in the optical properties of the GaN layer. The photo-induced changes created high contrast patterns on samples (77K<T<400K) that could be observed with low intensity ultraviolet excitation (0.4 W/cm2) under an optical microscope. No pattern was observed under room lighting or under a high power optical microscope using visible-light illumination. The sub-bandgap yellow photoluminescence peak at 2.2 eV (widely observed in many GaN samples) increased significantly after the patterns were created. The yellow emission slowly returned (2 hours) to its initial value at room temperature. After the pattern faded the writing/reading process could be repeated on the same location on the samples. The retention time of the image and the return to the baseline yellow emission decreased to a few seconds at temperatures above 100°C. A 1.34 eV thermal activation energy was calculated from the data using a stretched exponential. The difference between the bandgap of the GaN and the fitted 1.34 eV thermal activation is about 2.06 eV, which is in the range for the so-called yellow luminescence. We suggest that the effect of intense laser illumination is to influence the number of, or the charge state, of one or more deep levels at approximately 1.2 eV. This results in the increased intensity of the yellow luminescence and the yellow memory effect pattern. Relaxation of these states to their original configuration restores the original optical properties which makes it possible to write, store and read information with ultra-violet light on GaN.

11:00 AM (Student)

R8, Point Defect Distributions and Interdiffusion at AlGaN/GaN HEMT Structures: *Shawn T. Bradley*[1]; Leonard J. Brillson[1]; Gregg H. Jessen[1]; William J. Schaff[2]; N. Ikeo[3]; Y. Sakai[3]; [1]The Ohio State University, Electl. Eng., 205 Dreese Lab., 2015 Neil Ave., Columbus, OH 43210 USA; [2]Cornell University, Electl. Eng., Ithaca, NY 14853 USA; [3]JEOL, Ltd., R&D, Tokyo 196-8558 Japan

Low energy electron-excited nanoluminescence (LEEN) spectroscopy reveals spatially localized point defects that strongly affect two dimensional electron gas (2°) densities and mobilities at AlGaN/GaN high electron mobility transistor structures. Auger electron spectroscopy (AES) shows that stoichiometry varies radially across the growth wafer both at the near-surface GaN/AlGaN interface, at the 2° AlGaN/GaN junction, and even at the GaN buffer/sapphire interface. The AlGaN band gap and defects measured by LEEN spectroscopy vary across the wafer and correlate with AlGaN/GaN interdiffusion measured by high resolution AES depth profiling. The spatial variations of interface diffusion and stoichiometry indicate optimal radii for high 2° densities and mobilities. AlGaN/GaN HEMT structure grown by plasma-induced MBE consisted of a 7 nm AlN buffer layer deposited on Al_2O_3 at 800C and a 25 nm $Al_xGa_{1-x}N$ barrier layer grown at 850C with nominal x = 0.30 on a GaN buffer layer 1µm thick at 800C. A GaN film 2 nm thick capped the $Al_xGa_{1-x}N$ epilayer. Despite nearly identical growth conditions, different wafers and even regions within wafers exhibited 2° densities ranging from 1.3 x 10^{13} e/cm^2 to zero and mobilities ranging from 1478 to 570 cm^2/V-s. Previously, we showed that the presence of deep levels located ~2.34 eV below the conduction band are responsible for low or absent 2° carrier confinement.[1] LEEN depth profiles show that this defect resides exclusively in the AlGaN. Both the AlGaN-related 2.34 eV and GaN-related 2.18 eV ("yellow") defect emissions decrease with increasing radius R. A surface-

related 1.6 eV feature associated with the outer GaN cap layer increases with increasing Ga concentration. The density of 2.34 eV AlGaN deep levels increases as interdiffusion increases at the interior AlGaN/GaN interface with decreasing R (e.g., < 5 nm to >13 nm) as measured by 500 eV Ar+ AES depth profiling. Ga and O interdiffusion (~100 nm) at the GaN/Al_2O_3 junction also varies with R. We believe these radial variations to be due to increasing temperature with decreasing R. The spatial distributions of defects suggest that: (a) the 2.34 and 2.18 eV defects are related to Ga vacancies[2,3] or their complexes, (b) that the <1.6 eV defect at the GaN surface is related to Ga interstitials[4] or their complexes. In principle, these correlations can identify and further minimize defect formation in device fabrication of nanoscale nitride thin film structures. [1]S. T. Bradley, G. H. Jessen, L. J. Brillson, M. J. Murphy, and W. J. Schaff, J. Electron. Mater., in press; [2]J. Neugebauer and C. G. Van de Walle, Appl. Phys. Lett. 69, 503 (1997); [3]E. J. Tarsa, B. Heying, X. Hwu, P. Fini, S. P. DenBaars, and J. S. Speck, J. Appl. Phys. 82, 5472 (1997); [4]P. Boguslawski, E. L. Briggs, and J. Bernholc, Phys. Rev. B51, 17255 (1995).

11:20 AM, R9, Late News

Session S: Si-Based Heterojunction Growth and Characterization

Thursday AM Room: 138
June 28, 2001 Location: University of Notre Dame

Session Chair: Eugene Fitzgerald, Massachusetts Institute of Technology, Dept. of Matl. Sci. & Eng., Cambridge, MA 02139 USA

8:20 AM (Student)

S1, Investigating Hole Mobility Enhancements in Surface Strained Si/SiGe Heterostructures: *Christopher W. Leitz*[1]; Matthew T. Currie[1]; Eugene A. Fitzgerald[2]; Dimitri A. Antoniadis[3]; [1]Massachusetts Institute of Technology, Dept. of Matls. Sci. & Eng., 77 Massachusetts Ave., Rm. 13-4150, Cambridge, MA 02139 USA; [2]Massachusetts Institute of Technology, Dept. of Matls. Sci. & Eng., 77 Massachusetts Ave., Rm. 13-5153, Cambridge, MA 02139 USA; [3]Massachusetts Institute of Technology, Dept. of Electl. Eng. & Comp. Sci., 77 Massachusetts Ave., Rm. 39-415B, Cambridge, MA 02139 USA

Surface channel strained Si devices fabricated on relaxed SiGe virtual substrates exhibit enhanced electron and hole mobilities, making them attractive candidates for SiGe-based CMOS applications. While electron mobility enhancements in surface strained Si/SiGe have been well-documented, hole mobility in these heterostructures has not been thoroughly explored. In this study, we investigate the dependence of hole mobility in strained Si/SiGe MOSFETs on substrate Ge content and strained layer thickness. We also explore methods of increasing hole mobility beyond that of strained Si while retaining the high quality Si/SiO_2 interface. In these experiments, MOSFETs are fabricated by a novel short flow process utilizing a deposited gate dielectric and only one lithography step. This type of device allows us to measure effective mobility at vertical fields approaching 1 MV/cm, thereby enabling us to quickly explore the impact of materials parameters on channel mobility at fields approaching those of state-of-the-art MOSFETs. We show for the first time that hole mobility enhancements saturate at virtual substrate compositions of 40% Ge and above, with mobility enhancements over twice that of co-processed bulk Si devices at vertical fields up to 7 x 10^5 V/cm. Peak mobility enhancements are demonstrated on devices fabricated on 40% Ge virtual substrates while mobility enhancements drop slightly at higher virtual substrate Ge contents, indicating that misfit dislocations degrade hole mobility at these mismatch levels. Furthermore, we demonstrate that hole mobility in strained $Si/Si_{0.7}Ge_{0.3}$ heterostructures displays no strong dependence on strained layer thickness, and preliminary measurements indicate that alloy scattering in surface channel MOSFETs does not greatly degrade hole mobility. Based on these results, we have explored alternative heterostructures aimed at attaining maximum electron and hole mobility enhancements while maintaining thermodynamically stable channel thicknesses and the high quality Si/SiO_2 interface. These devices offer the promise of symmetric electron and hole mobilities, which would enable greater flexibility in circuit design. We show that such heterostructures have peak effective hole mobilities of over 300 cm^2/V-s, and hole mobility enhancements of 2.2 are maintained at fields up to 8 x 10^5 V/cm. These results show promise for realizing optimized heterostructures for SiGe-based CMOS applications.

8:40 AM

S2, Growth and Stabilization of Sub 100-nm Vertical n-Channel MOSFET's: *John Edward Gray*[1]; M. Yang[2]; H. Yin[1]; J. C. Sturm[1]; [1]Princeton University, Electl. Eng., J-423, Equad, Olden St., Princeton, NJ 08544 USA; [2]IBM Microelectronics, Hopewell Junction, NY, USA

Vertical MOSFETs (VFETs) are a promising alternative to their conventional surface-channel counterparts, because of their potential ability to scale to short channel lengths and potential high packing densities. One approach towards constructing such devices involves defining the doping profiles and channel lengths by epitaxial growth. With low temperature CVD or MBE, very sharp profiles can be realized. The critical issue of this method is that because of oxidation-enhanced-diffusion or transient enhanced diffusion during subsequent processing (e.g. the gate oxidation on a pillar sidewall), excessive dopant diffusion can prevent successful device fabrication below channel lengths of 100 nm. In this paper, we report (i.) the growth of record ultra-sharp n-channel VFET structures by low temperature RTCVD, (ii.) the stabilization of such structures against phosphorus diffusion from the source-drains by the use of SiGeC for the first time, and (iii.) the first ~50 nm device results. The first topic addressed is the growth of ultra-sharp n-type doping profiles, which is a classical issues with both CVD and MBE because of surface segregation effects of P and As. By employing a surface cleaning technique when making the transition from high (~1020 cm-3) to low P doping[1,2] and a high pressure growth method to increase the P incorporation, a record transition slope on falling P profiles as sharp as ~3 nm/decade can be achieved, vs. < 100nm/decade with conventional approaches. On the rising edge, the P slope was improved from ~20 nm/decade to an ultrasharp transition of ~5 nm/decade (limited by SIMS resolution) by pre-dosing the interface with phosphorus during a growth interrupt. Without such methods, rising slopes of ~20 nm/decade are commonly observed. The VFET process employs a wet oxidation step at 750°C to grow gate oxide on the pillar sidewalls. It is well known that the interstitial silicon atoms injected by oxidation can increase diffusion P and B diffusion coefficients by ~30X at this temperature. As previously reported for p-channel devices[3, 4], incorporating SiGeC regions in the source/drains to getter the interstitial silicon atoms can greatly reduce this undesired effect so that short channel structures can be realized. Here we report the results of this method applied to n-channel structures for various S/D doping levels, and the subsequent device results. For the first time we have successfully realized vertical n-channel FET's with channel lengths under 50 nm using CVD epitaxial growth. This work was supported by DARPA (N660001-97-1-8904) and ARO (DAA655-98-1-1270). [1]J. O. Chu, K. Ismail, and S. Koester, Abs. 40th Elec. Mat. Conf., Charlottesville, VA (1998); [2]M. Yang, M. Carroll, J. C. Sturm, and T. Buyuklimanli, J. Electrochem. Soc. 147, 3541-3545 (2000); [3]M. Yang, C-L. Chang, M. Carroll, and J. C. Sturm, IEEE Elec. Dev. Lett. 20, pp. 301-303 (1999); [4]M. Yang, and J. C. Sturm, Thin Solid Films 369, pp. 366-370 (2000).

9:00 AM (Student)

S3, Improvement of SiO2/SiGe Interface of SiGe pMOSFETs Using Water Vapor Annealing: *Tat Ngai*[1]; John Fretwell[1]; Xiao Chen[1]; James Chen[1]; Sanjay Banerjee[1]; [1]University of Texas at Austin, Microelect. Rsrch. Ctr., 10100 Burnet Rd., Austin, TX 78758 USA

The enhancement of hole mobilities in compressively-strained SiGe layers deposited on Si is well known. However, the realization of surface-channel SiGe PMOSFETs has been hindered by poor gate oxide quality. Although buried-channel SiGe PMOSFETs using thin Si cap layers can alleviate these problems, the reduction of effective gate capacitance is a drawback. A gate oxide deposition process using remote plasma chemical vapor deposition (RPCVD) has been developed to deposit ultra-thin gate oxides (down to 20 Å). These RPCVD oxides can be deposited directly on SiGe without a Si capping layer. Typical interfacial state density (Dit) values are 1 × 1010 cm2eV-1 and 3 × 1011 cm2eV-1 for Si and SiGe,

respectively, and the breakdown field strength (Ebd) values are in excess of 10 MV/cm in both cases. However, the SiO2/SiGe interface with these high quality RPCVD gate oxides is still unsatisfactory for the fabrication of surface-channel SiGe pMOSFETs even after conventional forming gas annealing. In this study, SiGe pMOSFETs were annealed in a wet atmosphere at 300°C for 3 hours. The SiGe pMOSFETs under-perform the control Si devices without H2O vapor annealing. The deviation from stoichiometry at the oxide/SiGe interface overshadows the hole mobility enhancement of the strained SiGe layer. After the water vapor annealing for three hours, more than 20% drive current enhancement is observed in the SiGe devices compared to the Si devices. The typical threshold voltage of the SiGe pMOSFET is -0.39 V and reduced to -0.20 V, and the subthreshold slope of SiGe devices decreases from 117 mV/dec to 87 mV/dec after the annealing. There are two possible explanations of the contribution of the water vapor annealing to the improvement of SiGe pMOSFETs. It has been reported that strained Si-O bonds can react with H2O and form silanol (Si-OH), and during annealing, the silanol releases water molecules and reconstructs Si-O bonds. Therefore, through the absorption and desorption of water molecules, the Si-O bond strain may be reduced. The other explanation is the creation of atomic hydrogen by a reaction with the Al metallization such as 2Al + 3H2O => 6H + Al2O3. Dangling Si and Ge bonds at the interface may be passivated by the atomic hydrogen formed at 300°C. To confirm the effect of the forming gas annealing on SiGe devices, the SiGe pMOSFETs after the wet annealing were further subjected to a half hour, 450°C forming gas annealing in a dry ambient. The electrical characteristics of these devices were degraded and were almost identical to those of the SiGe devices without the water vapor annealing. The degradation of the device performance indicates that the forming gas annealing breaks the Si-H bonds formed during the water vapor annealing.

9:20 AM (Student)

S4, Monte Carlo Modeling of Ion Implantation into SiGe: *Gaurav Shrivastav*[1]; Geng Wang[1]; Yang Chen[1]; Di Li[1]; Stimit Oak[1]; Sanjay Banerjee[1]; Lee Lin[1]; Al Tasch[1]; [1]University of Texas at Austin, Microelect. Rsrch. Ctr., MC R9950, 10100 Burnet Rd., Bldg. 160, Austin, TX 78758 USA

Si/SiGe based devices are becoming increasingly important since they offer significant performance enhancements associated with bandgap engineering and strain engineering, while working within mainstream Si technology. Also, SiGe HBTs can operate in the high frequency domain with performance that could earlier be realized using compound semiconductors only. With an increase in the usage of SiGe based devices, it becomes imperative to develop models that could accurately predict the implanted impurity profiles in this material. In this paper we present a Monte Carlo model for predicting the as-implanted impurity profiles for B, P and As into and through a SiGe layer. The model can predict the implanted profile for varying Ge mole fractions and for different locations and thicknesses of the SiGe layer. It takes into account the stress induced in the SiGe layer due to a mismatch in lattice constants between Si and Ge and the resulting tetragonal lattice structure. It also considers whether the SiGe layer is strained or relaxed and whether it has a constant Ge mole fraction or is linearly graded. The model is sufficiently general and can be extended easily to include other heterostructure materials like GaAs. The model is based on UT-MARLOWE, an existing implant simulator which simulates implants into Si and SiO2, using the Binary Collision Approximation (BCA). The collisions of the ion with the target atoms i.e. Si and Ge are rigorously calculated using the BCA, while the motion between collisions is modeled with the dielectric induced electronic stopping. In order to verify the model, B, P and As have been implanted into SiGe layers with Ge mole fractions ranging from 0.18 to 0.4. The implant parameters cover a fairly wide range with the implant energies ranging from 5keV to 50keV and the doses varying from 1e13cm-2 to 1e15cm-2. The tilt/rotation angles used are 0/0 and 7/30 degrees. SIMS measurements were carried out for the as implanted profiles and the results are in good agreement with the model.

9:40 AM

S5, Growth of $Ca_xCd_{1-x}F_2$ Alloy on Si Substrates Using Very Thin CaF_2 Buffer Layer: *Kazuo Tsutsui*[1]; Hiroshi Kambayashi[1]; Hiroshi Maeda[1]; [1]Tokyo Institute of Technology, Dept. of Adv. Appl. Elect., 4259 Nagatsuta, Midoriku, Yokohama, Kanagawa 226-8502 Japan

Heteroepitaxy of CaF_2 and CdF_2 on Si(111) substrates by molecular beam epitaxy (MBE) is interesting from the viewpoint of Si-based quantum devices applications. The CaF_2 /CdF_2 /CaF_2 structure which can be grown directly on Si surface provides deep quantum well (2.9eV) for electrons in conduction band. Resonant tunneling diodes (RTD) composed of this heterostructures have been reported thus far. However, considering vertical tunneling devices such as the RTDs, too high energy barrier and large effective mass of electrons in the fluoride heterostructure is rather disadvantage since such properties require ultra thin barrier layers in order to obtain enough current density. Epitaxial growth of alloy of these fluorides, $Ca_xCd_{1-x}F_2$, provides possibility of band engineering on the fluoride heterostrucutre and Si system, and solutions of the above problem. Recently, we demonstrated growth of $Ca_xCd_{1-x}F_2$ on Si substrates using CaF_2 buffer layer. The CaF_2 buffer is important to control the active reactivity of CdF_2 with Si. In this work, we investigated growth characteristics of $Ca_xCd_{1-x}F_2$ focused on growth temperature, composition (x) and thickness of the CaF_2 buffer layer. The $Ca_xCd_{1-x}F_2$/CaF_2/Si(111) structures were grown by MBE varying the layer thickness and growth temperature, and were characterized by X-ray diffraction, Rutherford backscattering spectroscopy and AFM. It was found that $Ca_xCd_{1-x}F_2$ layers with composition of whole range were epitaxially grown on the CaF_2 buffer layer and that optimum growth temperature was varied depending on the composition; lower temperature for small x, while, higher temperature for large x were desirable. The temperature and composition dependencies can be understood from the differences in migration characteristics between CaF_2 and CdF_2 and the chemical reactivity of CdF_2 with Si. In addition, thickness of the CaF_2 buffer layer was reduced to 0.6nm (2ML) keeping crystallinity and surface morphology of the $Ca_xCd_{1-x}F_2$ as good as those grown on thicker buffer layers. The capability of the thin buffer layer is promising because electrons can tunnel through the CaF_2 buffer layer. Electrical characteristics of the $Ca_xCd_{1-x}F_2$ layers is now under investigation.

10:00 AM Break

10:20 AM (Student)

S6, Annealing Effect on Properties of $Si_{0.2}Ge_{0.8}$/$Si_{0.7}Ge_{0.3}$/Si(001) p-Type Modulation Doped Heterostructures Studied by Magnetotransport Measurements and Raman Spectroscopy: *Maksym Myronov*[1]; S. G. Lyapin[2]; P. J. Phillips[1]; O. A. Mironov[1]; P. C. Klipstein[2]; E. H. C. Parker[1]; T. E. Whall[1]; [1]University of Warwick, Dept. of Phys., Gibbet Hill Rd., Coventry CV4 7AL UK; [2]University of Oxford, Clarendon Lab., Dept. of Phys., Parks Rd., Oxford OX1 3PU UK

We report the results of post-growth furnace thermal annealing effect on properties of $Si_{0.2}Ge_{0.8}$/$Si_{0.7}Ge_{0.3}$/Si(001) p-type modulation doped (MOD) heterostructures with 10nm and 14nm $Si_{0.2}Ge_{0.8}$ channel thicknesses studied by magnetotransport measurements and Raman spectroscopy. The heterostructures were grown on Si(001) substrates by SS-MBE. The $Si_{0.2}Ge_{0.8}$ channel was grown on a relatively thin 850nm $Si_{0.7}Ge_{0.3}$ virtual substrate involving a low-temperature Si buffer. The active layers of MOD heterostructures consist of $Si_{0.2}Ge_{0.8}$ undoped channel layer for mobile carriers (in this case holes), 7nm $Si_{0.7}Ge_{0.3}$ undoped spacer layer that separates the ionized dopants from the channel and 10nm B doped ($2x10^{18}cm^{-3}$) $Si_{0.7}Ge_{0.3}$ doped layer. The growth was performed at relatively low temperature (300ºC) to avoid strain induced roughening of the $Si_{0.2}Ge_{0.8}$ channel. To improve the magnetotransport characteristics of grown structures annealing treatments were performed following growth in nitrogen atmosphere in the temperature range of 600-900ºC for 30min. The Hall mobility and sheet carrier density of as-grown and annealed samples were obtained by a combination of resistivity and Hall effect measurements in the temperature range of 9-300K. Annealing at 600ºC is seen to have a negligible effect on the Hall mobility. Increasing the annealing temperature results in pronounced successive increases of Hall mobility. For both heterostructures the highest Hall mobilities at 9K and at 300K were observed after annealing at 750ºC. Further increasing of annealing temperature up to 900ºC results in decreasing of Hall mobility. For sheet carrier density was observed opposite behaviour with increasing annealing temperature. The best Hall mobility was obtained in the sample with 10nm $Si_{0.2}Ge_{0.8}$ channel. At 9K we observed an increase of mobility (at sheet carrier density) from $624cm^2V^{-1}s^{-1}$ ($1.37x10^{12}cm^{-2}$) in the as-grown sample up to $1680^2V^{-1}s^{-1}$($1.27x10^{12}cm^{-2}$) in the annealed one, and at 300K from $170^2V^{-1}s^{-1}$($2.6x10^{12}cm^{-2}$) up to $512^2V^{-1}s^{-1}$ ($2.11x10^{12}cm^{-2}$). The very same as-grown and annealed samples studied by magnetotransport were characterized by Raman spectroscopy at 293K. In the optical phonon range of Raman spectra of as-grown samples in addition to Ge-Ge(~290cm^{-1}), Si-Ge(~410cm^{-1}) and Si-Si(~500cm^{-1}) phonon modes originated from $Si_{0.7}Ge_{0.3}$ epilayers, we clearly observed the Ge-Ge(~306cm^{-1})

mode from $Si_{0.2}Ge_{0.8}$ channel layer. The analysis of Raman spectra of as-grown samples showed that 10nm $Si_{0.2}Ge_{0.8}$ channel is fully strained but 14nm $Si_{0.2}Ge_{0.8}$ channel is partially relaxed due to downward shift of Ge-Ge mode originated from latter one. With increasing of annealing temperature the downward shift of Ge-Ge mode originated from $Si_{0.2}Ge_{0.8}$ channel layer was observed for both samples, due to Ge diffusion in the buffer\channel\spacer region, which resulted in decreasing of Ge content in $Si_{0.2}Ge_{0.8}$ channel and its broadening.

10:40 AM

S7, Diffusion of Ion Implanted n-Type Dopants in Silicon Germanium Alloys: *Satoshi Eguchi*[1]; Hasan Nayfeh[1]; Christopher W. Leitz[2]; Eugene A. Fitzgerald[2]; Judy L. Hoyt[1]; [1]Massachusetts Institute of Technology, Microsys. Tech. Labs., Dept. of EECS, 60 Vassar St., Cambridge, MA 02139 USA; [2]Massachusetts Institute of Technology, Dept. of Matl. Sci. & Eng., 77 Massachusetts Ave., Cambridge, MA 02139 USA

MOSFETs fabricated using a strained Si channel on a relaxed SiGe layer exhibit enhanced mobility and current drive. An understanding of n-type dopant diffusion in SiGe, specifically the formation of the source/drain regions in the NMOS and the n-body region in the PMOS, is essential for the development of strained Si CMOS. In addition, n-type SiGe fabrication technology is expected to be important for the fabrication of other devices such as thermoelectric generators and the pnp HBT. We present here a study of n-type dopant diffusion in relaxed SiGe. We compare the diffusivities of ion implanted arsenic (As) and phosphorus (P) in SiGe and Si. The SiGe samples have a 2 micron-thick graded-SiGe layer, and a $Si_{0.8}Ge_{0.2}$, 2 micron-thick top layer, grown on <100> Czochralzki silicon. The SiGe layers were in-situ doped with boron (B) to 10^{17} cm^{-3}. The phosphorus-doped Si and SiGe samples were implanted at 30 KeV, 8 x 10^{14} cm^{-2}, and the arsenic implants were 30 KeV, 4 x 10^{14} cm^{-2}. Both ion implants were performed at a 7° tilt and 22° rotation to minimize channeling. After implantation, a 50 nm-thick low temperature oxide cap layer was deposited on the wafers. The samples were then furnace annealed at 1000°C for 30 minutes in an Ar ambient. The oxide layers were stripped and samples were analyzed by secondary ion mass spectrometry (SIMS) at Charles Evans and Associates. The diffusivity of n-type dopants is observed to be enhanced in SiGe compared to Si, in contrast to the diffusion of B, which is known to be retarded in SiGe relative to B diffusion in Si. The SIMS data was compared with TSUPREM-4 simulations. The expression for the concentration-dependent diffusivity of P in Si must be multiplied by a factor of roughly two, in order to match the P in SiGe profile. The junction depth in the SiGe sample is about 0.7 micron. Under similar diffusion conditions, the arsenic effective diffusivity enhancement factor is roughly 7 for diffusion in SiGe compared to diffusion in Si. The junction depth is roughly 0.35 microns for the As-doped sample. As diffusion in SiGe is enhanced significantly more than P diffusion in SiGe. However, the diffusivity of P in Si is roughly 9 times larger than that of As in Si. This implies that the ratio of the effective diffusivity of P to As in SiGe is 18:7 (~2.5) at an average doping of 10^{20} cm^{-3}. These results indicate that the diffusion of ion implanted As is much easier to control than that of P in SiGe.

Session T: Spin-Dependent (or Spintronic) Electronic Materials

Thursday PM Room: 129
June 28, 2001 Location: University of Notre Dame

Session Chairs: Jack Furdyna, University of Notre Dame, Dept. of Phys., Notre Dame, IN 46556 USA; Robert Shull, NIST, Gaithersburg, MD 20899-8552 USA; Chris Palmstrom, University of Minnesota, Dept. of Cheml. Eng. & Matls. Sci., Minneapolis, MN 55455 USA

1:20 PM (Student)

T1, Characterization and Spin Transport Across the Fe_xCo_{1-x}/GaAs(100) Interface: *Brian D. Schultz*[1]; L. C. Chen[1]; A. Isakovic[2]; J. Berezovsky[2]; P. A. Crowell[2]; M. M. R. Evans[3]; C. J. Palmstrøm[1]; [1]University of Minnesota, Dept. of Chem. Eng. & Matls. Sci., 421 Washington Ave. S.E., Minneapolis, MN 55455 USA; [2]University of Minnesota, Sch. of Phys. & Astron., 116 Church St. S.E., Minneapolis, MN 55455 USA; [3]University of Wisconsin–Eau Claire, Dept. of Phys. & Astron., Eau Claire, WI 54702 USA

Two distinct surface contributions to the magnetic anisotropy can be used to control the magnetic properties of thin films of bcc Fe_xCo_{1-x} grown on GaAs (100). On bare GaAs (100), the sp^3 bonding in the zincblende structure results in a two-fold surface symmetry of the gallium and arsenic bonding and a (2x4)/c(2x8) surface reconstruction for an arsenic surface coverage ~0.75 monolayers. This two-fold surface symmetry reduces the expected cubic four-fold magnetic anisotropy for Fe_xCo_{1-x} films to a strong uniaxial magnetic anisotropy. However, four-fold symmetry is restored in films grown with an interlayer of $Sc_yEr_{1-y}As$ (100), in which the rock-salt structure provides an unreconstructed surface. Initial STM images of 0.10 monolayer deposited Fe_xCo_{1-x} on GaAs(100) (2x4)/c(2x8) surface grown by MBE at 95°C indicate isolated clusters of atomic dimensions with preferential attachment along the arsenic dimer rows. The images also indicate that the (2x4)/c(2x8) reconstruction remains relatively undisturbed by the initial nucleation and growth at this coverage. STM images of Fe_xCo_{1-x} grown on viscinal GaAs(100) surfaces at 95°C suggest that the step edges provide no additional preferential growth sites for substrates miscut towards either the (111)A or (111)B planes. Furthermore, the deposition of bcc Fe_xCo_{1-x} on Sc_yEr_{1-y}(100) indicate there is no preferred nucleation site for the Fe_xCo_{1-x} atoms on the unreconstructed surface. Control of the interfacial properties of ferromagnetic metals and semiconductors is important for optimizing spin dependent transport across these interfaces. Spin dependent ejection of photo generated carriers from GaAs(100) into Fe_xCo_{1-x} ferromagnetic metal contacts has recently been measured. Spin polarization signals as high as 17% have been observed for electrons generated in a GaInAs quantum well 2000Å beneath the $Fe_{0.5}Co_{0.5}$ contact in an Fe_xCo_{1-x}/GaAs/$Ga_yIn_{1-y}As$/GaAs MBE grown heterostructure. This paper will emphasize the correlation between the structure and chemistry of the Fe_xCo_{1-x}/GaAs and Fe_xCo_{1-x}/$Sc_yEr_{1-y}As$/GaAs interfaces, determined by STM, RHEED, LEED, XPS, RBS, XRD and TEM, and the magnetic and transport properties. Supported by: ONR-N/N00014-1-0233, DARPA N/N00014-99-1-1005, and NSF-MRSEC NSF/DMK-9809364.

1:40 PM

T2, Spin-Polarized Transport in Mn-Containing Dilute Magnetic III-V Semiconductors: *Leeor Kronik*[1]; Manish Jain[1]; James R. Chelikowsky[1]; Vitaliy V. Godlevsky[2]; [1]University of Minnesota, Dept. of Cheml. Eng. & Matls. Sci., & MN Supercompg. Inst., MN 55455 USA; [2]Rutgers University, Dept. of Phys. & Astron., Piscataway, NJ 08854 USA

Mn-based dilute magnetic III-V semiconductors have attracted a lot of recent attention, due to significant advances in their fabrication[1] and to the recent demonstration of spin-polarized hole injection from these materials[2]. A detailed understanding of the electronic structure is required

for further design of an optimized spin-injector based on these materials. In this talk, we present ab initio density functional calculations for the dilute magnetic semiconductors Mn_{x}Ga_{1-x}As and Mn_{x}In_{1-x}As, with a realistic x=0.063. We find that the introduction of Mn perturbs the position of the nearest As atoms (pushing it outwards for MnGaAs, inwards for MnInAs), in agreement with EXAFS measurements[3], but does not break the tetrahedral symmetry. We find that neither material is half-metallic in the strict sense, namely, both the majority and minority spin densities of state possess a bandgap. However, both materials feature an impurity band of majority spin just above the valence band edge. Holes in this band have well-defined spin and effective masses comparable to those found in GaAs and InAs. Therefore, the theoretical band-structure limit of spin-injection from these materials is 100%, but attaining this limit requires careful "engineering" of the Fermi level position, especially at the injecting interface. [1]H. Ohno, Science, 281, 951 (1998), and references therein; [2]B. Beschoten et al., Phys. Rev. Lett. 83, 3073 (1999); Y. Ohno et al., Nature, 402, 790 (1999); [3]R. Shioda et al., Phys. Rev. B 58, 1100 (1998).

2:00 PM (Student)

T3, Growth of the Dilute Magnetic Semiconductor (Ga,Mn)P by Gas Source MBE: *M. E. Overberg*[1]; C. R. Abernathy[1]; S. J. Pearton[1]; F. Sharifi[2]; A. Hebard[2]; N. Theodoropoulou[2]; S. von Molnar[3]; M. Anane[3]; P. Xiong[3]; [1]University of Florida, Dept. of Matls. Sci. & Eng., Rhines Hall, PO Box 116400, Gainesville, FL 32611 USA; [2]University of Florida, Dept. of Phys., Gainesville, FL, USA; [3]Florida State University, Dept. Phys. & MARTECH, Tallahassee, FL USA

Dilute magnetic semiconductors (DMS) offer the use of the spin degree of freedom of the electron in addition to its charge in device applications. Controlling the phase of the spin wavefunction within these devices would potentially enable the development of high speed logic and memory, quantum-based communication, and electro-optic switches and modulators. To date, current work in this "spintronics" area has focused upon (Ga,Mn)As, (In,Mn)As, and (Ga,Mn)Sb. Recent theoretical calculations have predicted a Curie temperature for (Ga,Mn)P of roughly 100 K(1). While having a slightly lower predicted Curie temperature compared to (Ga,Mn)As, the close lattice matching of (Ga,Mn)P to Si offers the possibility of uniting spin-exploiting devices with current electronic device technology. In this paper, we will report on the growth of (Ga,Mn)P:C thin films by gas source molecular beam epitaxy (GSMBE) utilizing phosphine as the group V source. The (Ga,Mn)P material was co-doped with C via a CBr_4 source for enhanced p-type doping. The carrier concentration of similarly grown p-GaP:C was found to be 2.6E+20/cm^3, corresponding to a film resistivity of 3.4E-3 Ω-cm. Upon addition of the Mn, the film resistivity was found to increase by a factor of 30, indicating that Mn may serve as a deep level in GaP. X-ray diffraction (XRD) of the grown films indicates a second MnP phase in layers grown at a temperature of 600°C. Analysis of this material by SQUID magnetometry suggests the presence of a ferromagnetic phase with a Tc above 250K. This behavior is most likely due to the presence of MnP that has been reported to have a Tc of 291K. Although the formation of the MnP phase can be reduced by lowering the growth temperature to 400°C, a separate $Mn_{5.64}P_3$ phase appears. It was found that the formation of this phase could be reduced by lowering the Mn flux from 675°C to 650°C, which corresponds to a reduction in the Mn source vapor pressure from 1E-5 to 5E-6 torr. This decrease also resulted in a change in the RHEED pattern suggesting a change in morphology from polycrystalline to single crystal. Measurement of the magnetic properties of this single crystal material via SQUID magnetometry will also be presented. [1]T. Dietl, H. Ohno, F. Matsukura, J. Cibert, and D. Ferrand, Science, 287, p. 1019 (2000).

2:20 PM

T4, Spontaneous Anisotropic Magnetoresistance in GaMnAs: *David V. Baxter*[1]; D. Ruzmetov[1]; J. Scherschligt[1]; J. Furdyna[2]; Y. Sasaki[2]; X. Liu[2]; [1]Indiana University, Dept. of Phys., Swain Hall W., Rm. 117, 701 E. Third St., Bloomington, IN 47405 USA; [2]University of Notre Dame, Dept. of Phys., 225 Nieuwland Science Hall 309, Notre Dame, IN 46556-5670 USA

The recent discovery of ferromagnetism in III-V semiconductors containing Mn (e.g., Ga1-xMnxAs) presents exciting opportunities for creating novel magnetoelectronic devices. This also represents a new class of magnetic materials, one in which ferromagnetic exchange is mediated by free carriers but with the density of such carriers substantially lower that the density of magnetic moments. As the potential for device applications of these materials is explored, it is important to investigate their basic transport properties in order to test our understanding of their behavior. We report on the temperature and magnetic field dependence of the resistivity and Hall effect for a series of Ga1-xMnxAs samples for x ranging from 0.033 to 0.053. The spontaneous anisotropic magnetoresistance (AMR), i.e., the dependence of the sample resistivity on the relative orientation of the magnetization and current density, is on the order of -5% at 4.2K in these materials. In conventional ferromagnetic metals, this AMR is described in terms of two parallel conduction channels (one spin-up and one spin-down), with the spin-orbit perturbation providing the necessary anisotropy. In such materials the effect is usually positive (larger resistance for current parallel to the magnetization). In GaMnAs, the effect is of the opposite sign, and the spin-orbit coupling is so strong that models involving independent spin-up and spin-down current channels are no longer a viable starting point. This points to the need for new microscopic theories of transport in these unconventional magneto-electronic materials. It is interesting, furthermore, that in some samples we see unusual behavior in the perpendicular magnetoresistance for small fields. This may indicate that these measurements can be used to detect inhomogeneity in the distribution of Mn. *Supported by DARPA and by the 21st Century Fund of Indiana.

2:40 PM

T5, Molecular Beam Epitaxy Growth of Heusler Alloy Ni_2MnGe Thin Films on GaAs(001): *J. Lu*[1]; J. W. Dong[1]; J. Q. Xie[1]; V. V. Godlevsky[2]; K. M. Rabe[2]; Y. Xin[3]; C. J. Palmstrøm[1]; [1]University of Minnesota, Dept. of Chem. Eng. & Matl. Sci., 421 Washington Ave. S.E., Box 192, Minneapolis, MN 55455 USA; [2]Rutgers University, Dept. of Phys., Piscataway, NJ, USA; [3]Florida State University, Nat'l High Magnetic Field Lab., Tallahassee, FL, USA

Ferromagnetic Heusler alloys, such as Ni_2MnX (X = Ga, In, Ge), thin films grown on semiconductors have drawn attention due to their ferromagnetic properties and close lattice match to III-V semiconductors resulting in promising potential application in electron spin transport devices. A number of the Heusler alloys have been predicted to be half-metals. In this work, the Heusler alloys Ni2MnGe single crystal films have been grown on GaAs(001) successfully by molecular beam epitaxy (MBE). Reflection high-energy electron diffraction (RHEED), X-ray diffraction (XRD) and cross-sectional transmission electron microscopy (TEM) are used to characterize the structure of Ni_2MnGe films. During the growth of Ni_2MnGe, RHEED pattern was streaky (2x2) indicative of high structural quality. X-ray diffraction data revealed that the Ni_2MnGe film has tetragonal structure with a = 5.65 Å, b = 5.90 Å, and has an epitaxial relationship $Ni_2MnGe(001)||GaAs(001)$, $Ni_2MnGe(110)||GaAs(110)$. TEM shows ordering of Ni_2MnGe with double periodicity which might be induced by surface reconstruction. First principle calculations are used to explain the formation of tetragonal structure of Ni_2MnGe and to predict the electronic structure. This study also reveals that film structural ordering changes dramatically with growth temperature. High temperature growth (300°C) results in interfacial reaction, and low temperature (80°C) growth leads to disordered structure. The optimum growth temperature is determined to be 160°C. The magnetic properties of Ni2MnGe films were measured by vibrating sample and superconducting quantum interference device magnetometers. Curie temperatures of Ni_2MnGe is determined to be ~320K, and saturation magnetization ~400 emu/cm3 at 50K. No strong in-plane magnetization anisotropy was observed. In this talk we will discuss the structural and electrical properties of Ni_2MnGe film. This project is supported by Air Force Office of Science Research Contract No. F49620-98-1-0433, Office of Navel Research Contract No. N/N00014-99-1-0233 and MRSEC Program of the National Science Foundation under Award No. DMR-9809364.

3:00 PM Break

3:20 PM (Student)

T6, MBE Growth of Ferromagnetic Ni_2MnIn Thin Films on InAs (001): *J. Q. Xie*[1]; J. W. Dong[1]; J. Lu[1]; C. J. Palmstrøm[1]; [1]University of Minnesota, Dept. of Cheml. Eng. & Matls. Sci., 421 Washington Ave. S.E., Minneapolis, MN 55455 USA

There has been a growing interest in ferromagnetic/semiconductor hererostructures for the development of spintronic devices which utilize the carrier spin as well as its charge.[1,2] Several groups reported successful electrical spin injection into semiconductors using diluted magnetic semi-

conductors (DMS) as spin contacts at low temperatures (< 52 K) and sometimes with high magnetic field (several Tesla).[3-5] However, until now, spin injection effects on the order of 1% or less were observed using ferromagnetic metals as spin contacts.[6,7] A recent theoretical study suggested that atomically ordered and suitably oriented interfaces between some ferromagnetic metals and some semiconductors should be almost perfect spin filters.[8] This study indicates the importance of investigating ferromagnetic/semiconductor hererostructures with suitable band structure alignment. InAs is the semiconductor of interest due to its high electron mobility and the ease to form an ohmic contact to it. Although no elemental ferromagnet is lattice matched to InAs, the lattice mismatch between Ni_2MnIn and InAs is only 0.2%. In the bulk, Ni_2MnIn is reported to have a cubic ($L2_1$) crystal structure with a lattice constant a_0 = 6.069 Å and a Curie temperature ~314 K.[9] The band structure calculations by Kilian and Victora[10] show that the minority spins are situated at the Γ point in Ni_2MnIn and the majority spins far away from the Γ point. Therefore, the band structure alignment between Ni_2MnIn and InAs would enhance the injection of the minority spins, suggesting that Ni_2MnIn may be a good choice as a ferromagnetic contact for spin injection. In this talk, we report on the epitaxial growth of Ni_2MnIn thin films on InAs (001) by the molecular beam epitaxy (MBE) technique. Both in situ reflection high energy electron diffraction and ex situ x-ray diffraction and Rutherford backscattering spectrometer measurements indicate that Ni_2MnIn films grow epitaxially on MBE-grown (001) InAs substrates. Superconducting quantum interference device magnetometer measurements show that the deposited films are ferromagnetic with the highest Curie temperature ~290K. Our results also indicate that magnetic properties of the films are very sensitive to their composition. In this talk, the effects of interfacial layers and growth temperature on the structural and magnetic properties of Ni_2MnIn thin films will be discussed. References: [1]G. A. Prinz, Science 282, 160 (1998); [2]S. Datta and B. Das, Appl. Phys. Lett. 56, 665 (1990); [3]R. Fiederling et al., Nature 402, 787 (1999); [4]Y. Ohno et al., Nature 402, 790 (1999); [5]B. T. Jonker et al., Phys. Rev. B 62, 8180 (2000); [6]P. Hammer et al., Phys. Rev. Lett. 83, 203 (1999); [7]S. Gardelis et al., Phys. Rev. B 60, 7764 (1999); [8]G. Kirczenow, cond-mat/0010153; [9]P. J. Webster et al., Philos. Mag. 49, 295 (1984); [10]K. A. Kilian and R. H. Victora, J. Appl. Phys. 87, 7064 (2000).

3:40 PM

T7, Influence of Material and Device Parameters on Spin Effects in Quantum Dots: *Philippe Matagne*[1]; Jean-Pierre Leburton[1]; [1]University of Illinois, CEG, Beckman Institute, 405 N. Mathews, Urbana, IL 61801 USA

We present a detailed analysis of single electron charging effects in cylindrical vertical quantum dots (CVQD). Emphasis is placed on three-dimensional (3D) device effects introduced by the device configuration that includes i) the influence of the doping in the lead reservoirs, ii) the effect of depletion in the vertical direction with applied bias and iii) the effect of gate length on the confining potential in the quantum well. We perform a full 3D self-consistent quantum simulation of single-electron charging in quantized CQVDs by using the density functional theory, and find significant discrepancies with the popular 2D harmonic oscillator model. In particular, we show that the spin sequences realized in filling electronic shells are a sensitive function of the potential non-parabolicity arising from the 3D CQVD geometry and varying with applied gate bias. We also show that the profile of the addition energy spectrum is not necessarily a signature of a particular spin filling sequence.

4:00 PM (Student)

T8, The Effect of Mn Ions on the Formation of CdSe Self-Assembled Quantum Dots: *Luba Titova*[1]; Mijin Kim[1]; Sanghoon Lee[2]; Jacek K. Furdyna[1]; Malgorzata Dobrowolska[1]; [1]University of Notre Dame, Phys. Dept., Nieuwland Science Hall 225, Notre Dame, IN 46556 USA; [2]Kwangwoon University, Dept. of Elect. Matls. Eng., Seoul 136-701 Korea

It has been shown earlier[1] that a substantial red shift and a decrease of the PL linewidth emitted by CdSe quantum dots (QDs) occurs when the dots are grown on ZnMnSe rather than ZnSe. These results suggest that Mn ions play an important role in the self-assembly process. In order to further investigate the role which Mn plays in the QD formation, we have fabricated a series of CdSe self-assembled QDs on Mn-passivated ZnSe buffers. The amount of Mn delivered to the ZnSe surface was controlled by both Mn flux and by deposition time. The samples were studied by means of photoluminescence (PL) and magneto-PL. The characteristics of the PL line (such as its linewidth and energy position) show a strong dependence on the growth conditions under which Mn was deposited on the surface. While all the samples show significant red shifts of the PL line, the narrowing of the PL line was the most pronounced for those samples where the Mn was delivered under higher flux for a short time. The magneto-PL shows significant Zeeman shifts, indicating the presence of Mn ions within the dots. The observed Zeeman shift as a function of magnetic field shows two different types of behaviors (linear and Brillouin-type) depending on the condition of Mn deposition. In this paper we discuss the implications of this observation. Finally, we also discuss magnetic polaron effects which are observed in these magnetic QD systems. [1]C. S. Kim, M. Kim, S. Lee, J. Kossut, J. K. Furdyna, and M. Dobrowolska, J. Cryst. Growth. 214/215, 395 (2000).

4:20 PM

T9, Electron Spin Dynamics in III-V Quantum Wells: *Wayne H. Lau*[1]; Michael E. Flatté[1]; [1]University of Iowa, Optl. Sci. & Tech. Ctr., Dept. of Phys. & Astron., Iowa City, IA 52242 USA

In recent years there has been considerable interest in exploiting not only charge but also spin in solid-state electronics, which has led to new ultrafast optical studies of electron spin dynamics in bulk and quantum well semiconductors[1-3] and their possible application to ultrafast spin-dependent switching of electronic devices. One of the important factors in utilizing coherent spin dynamics in electronic devices is that the spin coherence time must be sufficiently long so that information stored in the spin polarized ensembles will not be lost during processing. Accurate quantitative calculations of spin lifetimes are thus essential to optimizing spin coherence in quantum wells. Electron spin coherence times in zincblende type semiconductors near room temperature are dominated by the precessional D'yakonov-Perel' (DP) mechanism[4], which is a direct result of the spin splitting of the conduction band that occurs at zero magnetic field at finite crystal momentum in inversion asymmetric crystals. In quantum wells, this inversion asymmetry can arise not only from bulk inversion asymmetry (BIA) of the constituent semiconductors, but also from structure inversion asymmetry (SIA) of an asymmetric potential. The effect of BIA is dominant in structural symmetric quantum wells. On the other hand, in asymmetric quantum wells (e.g., in the presence of external electric field along the growth direction), the contribution to electron spin decoherence due to SIA may become important. Hence the application of applied electric field can be used as a convenient way to manipulate spin coherence in quantum wells. We have previously calculated the electron spin coherence times (T1) in (100)-oriented zincblende semiconductor quantum wells within a nonperturbative fourteen-bulk-band nanostructure model. Quantitative agreement between calculated spin lifetimes and measurements is found for GaAs/AlGaAs and GaSb/AlSb quantum wells[2,5]. We have now calculated T1 for (110)-oriented systems, motivated by recent experimental investigations of the electron spin lifetimes in 75ÅGaAs/100ÅAl0.4Ga0.6As quantum wells near room temperature[3]. In these quantum wells the measured spin lifetimes (T1) increase tenfold compared to those of their (100)-oriented counterparts and exceed one nanosecond at room temperature. Our predicted spin lifetimes for these systems are in good agreement with the measured spin lifetimes. We also report the dependence of electron spin coherence times on applied electric field in (110)-oriented GaAs/AlGaAs quantum wells near room temperature. These results may be used to optimize devices for the manipulation of spin coherence. We would like to acknowledge NSF Grant No. ECS-0000556. [1]J. M. Kikkawa and D. D. Awschalom, Phys. Rev. Lett. 80, 4313 (1998); [2]Ryota Terauchi, et al., Jpn. J. Appl. Phys. 38, 2549 (1999); [3]Y. Ohno, et al., Phys. Rev. Lett. 82, 4196 (1999); [4]M. I. D'yakonov and V. I. Perel', Sov. Phys. Solid State, 13, 3023 (1972); [5]W. H. Lau, J. T. Olesberg, and M. E. Flatté, e-Print arXiv: cond-mat/0004461 (2000).

4:40 PM, T10, Late News

Session U: Growth and Properties of Quantum Dot Structures

Thursday PM Room: 102
June 28, 2001 Location: University of Notre Dame

Session Chairs: Mark Miller, University of Utah, Salt Lake City, UT 84112-0560 USA; Arthur Gossard, University of California–Santa Barbara, Dept. of Electl. & Comp. Eng., Santa Barbara, CA 93106 USA

1:20 PM

U1, Growth of InAs and InAsSb Quantum Dots by Metal-Organic Chemical Vapor Deposition: *J. G. Cederberg*[1]; R. M. Biefeld[1]; A. A. Allerman[1]; E. D. Jones[1]; S. R. Kurtz[1]; [1]Sandia National Laboratories, PO Box 5800, Albuquerque, NM 87185 USA

Quantum dots (QD) represent an area of intense research interest for light emitters and novel electronic devices. Our laboratory is investigating InAsSb QD grown on GaAs as a model system. The addition of Sb to InAs should shift the QD emission to longer wavelengths, approaching the technologically interesting 1.55 µm region. A type II offset may exist between GaAs and InAsSb. The type of offset in this system will be investigated. Also, the effect Sb has on InAs QD growth has not been investigated, and may provide insight into semiconductor nanostructure formation. We have established conditions for InAs QD on GaAs growth in our MOCVD system. Optimum conditions for QD growth were determined from AFM measurements and PL measurements performed at 4 and 77K. AFM images show that the formation of QD is very dramatic, occurring at slightly greater than 2 ML of InAs. The QD formed are dense (1 x 10^{10} cm^{-2}) and small (2-3 nm in height, 10 nm at the base). Decreasing the amount of deposit by 1 Å results in formation of a 2D step bunched surface. Increasing the amount of InAs above 2.2 ML causes the island to coalesce, forming larger islands, that are less dense. PL spectra at 77K from QD structures buried by 30 nm of GaAs show emission related to QD formation. When the InAs deposit is less than 2.2 ML thick no QD-related PL is observed, only emission from an In(Ga)As QW. Increasing the InAs deposit to 2.2 ML produces a feature at 1.17 eV related to the formation of quantum confined structures. Increasing the thickness of InAs deposited to 2.9 ML causes a shift in the emission to 0.98 eV. The low intensity from the sample with 2.2 ML of InAs compared to the sample with 2.9 ML suggests that the small, regular islands formed may not be optically active or the large islands observed in the 2.9 ML sample are a result of surface migration during sample cooling. This effect will be discussed further in the presentation. In addition to our results on the growth and characterization of InAs/GaAs QD, results from our efforts to form InAsSb QD on GaAs will be discussed. Our laboratory has extensive experience in the growth of ternary and quaternary Sb alloys and their heterostructures by MOCVD, which has been extended to the growth of Sb-containing QD structures. Sandia National Laboratories is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under contract DE-AC04-94AL85000.

1:40 PM (Student)

U2, InP Self-Assembled Quantum Dots Embedded in In0.49(Alx Ga1-x)0.51P Grown by Metalorganic Chemical Vapor Deposition: *Jae-Hyun Ryou*[1]; Russell D. Dupuis[1]; C. V. Reddy[2]; Venkatesh Narayanamurti[2]; David T. Mathes[3]; Robert Hull[3]; David A. Kellogg[4]; Gabriel Walter[4]; Nick Holonyak[4]; [1]The University of Texas at Austin, Microelect. Rsrch. Ctr., PRC/MER 1.608 R9900, Austin, TX 78712-1100 USA; [2]Harvard University, Gordon McKay Lab. of Appl. Sci., 9 Oxford St., Cambridge, MA 02138 USA; [3]The University of Virginia, Dept. of Matls. Sci. & Eng., 116 Engineer's Way, Charlottesville, VA 22904-4745 USA; [4]The University of Illinois at Urbana–Champaign, Ctr. for Compd. Semicond. Microelect., 208 N. Wright St., Urbana, IL 61801 USA

III-Phosphide self-assembled quantum dot (SAQD or simply QD) structures offer a potential to realize injection lasers operating in the visible spectral region with improved performance characteristics such as low threshold current densities, high characteristic temperature, and high differential gain. Also, SAQD growth can overcome the limitation of lattice matching between the substrate and the epitaxial active region due to the intrinsic nature of growth mode (i.e., strain-induced S-K growth). InP quantum dots have been grown and characterized on direct-bandgap $In_{0.49}Ga_{0.51}P$ matrices by several research groups and on indirect-bandgap $In_{0.49}Al_{0.51}P$ matrices by these authors. As expected, growth characteristics and optical properties are different in these cases. In this study, we report the characteristics of InP SAQDs embedded in $In_{0.49}(Al_xGa_{1-x})_{0.51}P$ grown by low-pressure metalorganic chemical vapor deposition (LP-MOCVD) to make a complete bridge between two material systems. The InP QD growth studies are done at a temperature of ~650°C by altering growth times using various $In_{0.49}(Al_xGa_{1-x})_{0.51}P$ matrices (x=0.0, 0.3, 0.6, and 1.0). The morphology change (average sizes and densities) of the exposed SAQDs (grown without the upper cladding layer), depending on growth time and matrix material system, is characterized by atomic force microscopy (AFM). As growth time increases from the "planar-layer-growth equivalent" of 7.5MLs to 15MLs for InP/$In_{0.49}(Al_{0.6}Ga_{0.4})_{0.51}P$ quantum dot structures, the dominant QD size increases, while the densities remain almost the same (1~2x10^8dots/mm^{-2}) and the dominant heights are 10~25nm, depending on growth time. Photoluminescence (PL) spectra are taken at 4K and 300K to determine the light-emitting characteristics of the $In_{0.49}(Al_xGa_{1-x})_{0.51}P$ quantum dot heterostructures (QDH). 4K PL spectra from the InP SAQDs embedded in $In_{0.49}(Al_xGa_{1-x})_{0.51}P$ cladding layers exhibit PL emission in the visible orange and red spectral regions. Emission peaks appear at higher energy for shorter growth times and higher bandgap matrices-2.10, 1.90, and 1.82eV peak energy for 3.75, 7.5, and 15ML InP/$In_{0.49}(Al_{0.6}Ga_{0.4})_{0.51}P$ QDH, while 2.06, 1.92, and 1.87eV for 7.5, 11.25, and 15ML InP/$In_{0.49}Al_{0.51}P$ QDH, respectively. Since the bandgap of the "active" InP SAQDs is modified by multi-dimensional quantum confinement, bulk material properties like the band offset do not apply in this case. We further study the InP/$In_{0.49}(Al_xGa_{1-x})_{0.51}P$ (x=0.6) SAQDs using ballistic electron emission microscopy (BEEM) techniques to determine the band structure of the dots. Also, transmission electron microscopy (TEM) is used to characterize the microscopic material quality and morphology of the individual QD and the interfaces between SAQD and cladding layers. Defect-free self-assembled quantum dots are observed for the height of less than ~30nm. In summary, we will report on the optical, structural, and electronic properties of InP SAQDs embedded in $In_{0.49}(Al_xGa_{1-x})_{0.51}P$ layers grown on GaAs substrate by MOCVD.

2:00 PM

U3, Matrix Effect on the Stacking Behavior of InAs Nanostructures Grown on InP (001) Substrates: *Hanxuan Li*[1]; Theda Daniels-Race[1]; Mohamed-Ali Hasan[2]; [1]Duke University, Dept. of Electl. & Comp. Eng., Durham, NC 27708-0291 USA; [2]The University of North Carolina at Charlotte, Dept. of Electl. & Comp. Eng., Charlotte, NC 28223 USA

Self-organization of Stranski-Krastonow islands in lattice-mismatched heteroepitaxy has evolved as a novel method for fabrication of semiconductor nanostructures. The ordering stacking behavior of self-organized nanostructure superlattices is promising to improve the size uniformity of nanostructures. For different material systems, various stacking sequences have been observed, ranging from vertical correlation for InAs/GaAs and GeSi/Si, vertical anticorrelation in II-VI submonolayer dot superlattices, to face-center-cubic (fcc) stacking for IV-VI system. These different stacking behaviors have been explained theoretically by taking into account the elastic anisotropy of matrix materials. For InAs/AlInAs superlattices grown on InP (001) substrates, our previous work revealed the lateral ordering effect (H. Li et al., Appl. Phys. Lett. 75, 1173 (1999)). In this work, we have investigated the matrix effects on the stacking behaviors of InAs nanostructures grown on InP substrates. Specifically, we prepared InAs nanostructures with InAlAs, InGaAs, and AlInGaAs spacer layers. The samples were grown by a Riber solid-source molecular beam epitaxy (MBE) system on InP (001) substrates. All superlattice samples consisted of several monolayers (MLs) of InAs alternating with spacer layers of thickness ranging from 2.5 to 30 nm. The structural properties and surface morphology of the samples were investigated by reflection high-energy electron diffraction (RHEED), atomic force microcopy (AFM), and transmission electron microscopy (TEM) measurements. For InAs/AlInAs superlattices, lateral correlation phe-

nomena can be observed in all the samples with different InAlAs spacer thickness and InAs coverage. No evidence of vertical correlation is found. For samples with InGaAs and InAlGaAs spacer layers, however, vertical correlation is observed. The different stacking behaviors are explained qualitatively by taking into account the surface morphologies of the buffer layer, shapes of the nanostructures, and anisotropy of strain relaxation. This work is partially supported by NSF grant #NSF-ECS-96-33780 and the Department of Energy grant # DE-FG02-97ER45648.

2:20 PM (Student)

U4, Fermi-Level Effect on the Interdiffusion of InAs and InGaAs Quantum Dots: *Oleg B. Shchekin*[1]; Dennis G. Deppe[1]; Dingyan Lu[1]; [1]The University of Texas at Austin, Microelect. Rsrch. Ctr., 10100 Burnet Rd., MER 1.606 R9950, Austin, TX 78758 USA

InAs and InGaAs quantum dots are important for the development of GaAs-based lasers operating at extended wavelengths, and their critical features can be altered by diffusion and segregation of the column III constituents during crystal growth. Although a few studies have now looked at interdiffusion of the QDs during and after crystal growth, none to our knowledge have been able to define the specific point defects responsible. In our study we show that interdiffusion in self-organized InAs and InGaAs quantum dots (QDs) undergoes mostly through interstitial defects. The interdiffusion of QD materials is analyzed by performing a number of growths under identical conditions except for modulation doped regions grown after the QDs. Photoluminescence is used to analyze spectral shifts that result from interdiffusion of the QDs grown with different types of modulation doping. Numerous growths have been performed and duplicated to verify the repeatability of the experimental results. For some of the samples, InAs QDs are formed by depositing 2.7 monolayers of InAs on GaAs, while for other samples InGaAs QDs are grown by using paused submonolayer deposition of a total of 10 monolayers of 50%InGaAs. Furthermore, in some of the InAs QD samples 2 monolayers of AlAs are also deposited on top of the dots to inhibit indium segregation. The modulation doping is performed using ~30 angstrom thick Be or Si doped layers placed 100 angstroms after the dot layers. In all samples a consistent and significant trend is that interdiffusion increases from the Si doped samples, to the undoped samples, and is greatest for the p-type modulation doped samples. For example, for the InAs QD samples with 2 MLs of AlAs the ground state transition wavelengths are 1.236 μm from the n-doping, 1.213 μm for no doping, and 1.175 μm for p-doping. The ground state and first excited state transition energy differences were 80meV, 98meV and 65meV for undoped, n-doped and p-doped samples, respectively, consistent with greater interdiffusion as the hole concentration in the QDs is increased. Similar dependence on doping was observed in other InAs and InGaAs QD samples. These experimental results indicate that donor type defects are responsible for the QD interdiffusion, the most likely of which are column III interstitials consistent with past experiments on interdiffusion in III-V heterostructures.

2:40 PM

U5, Self-Ordered Structures and Compositional Modulations on the Atomic Scale in (Cd,Zn,Mn)Se and In(Sb,As) Quantum Dot Structures: *Peter Moeck*[1]; Teya Topuria[1]; Nigel D. Browning[1]; Malgorzata Dobrowolska[2]; Shahoon Lee[2]; Jacek K. Furdyna[2]; Graham R. Booker[3]; Nigel J. Mason[4]; Robin J. Nicholas[4]; [1]University of Illinois at Chicago, Dept. of Phys., MC 273, 845 W. Taylor St., Chicago, IL 60607-7059 USA; [2]University of Notre Dame, Dept. of Phys., Notre Dame, IN 46556 USA; [3]University of Oxford, Dept. of Matls., Parks Rd., Oxford, England OX1 3PH UK; [4]University of Oxford, Dept. of Phys., Clarendon Lab., Parks Rd., Oxford, England OX1 3PU UK

Semiconductor Quantum dots (QDs) are thought to be achievable by means of self-ordering processes during heteroepitaxial growth in the Stranski-Krastanow mode(or its variants in cases of multi-sheet arrangements of embedded fractional monolayers below their actual critical thickness)[1]. Related to intra-dot ordering of QDs on a tens of nm scale during Stranski-Krastanow growth seems to be self-ordering on an atomic scale that leads to agglomerates in the size range of a few nm to a few hundred nm with internal compositional modulations[2-5]. We will show that some of such CdSe and InSb rich agglomerates fulfill all of the criteria that have to be met for a structure to be considered as constituting a novel type of QD. We will briefly discuss possible causes for atomic self-ordering in the structures we investigated and mention some implications of their possible existence in other QDs structures that were grown in the Stranski-Ktastanow mode (or its variants, mentioned above). As research into self-assembled QDs progresses, it is becoming common consensus that the classical Stranski-Krastanow model has to be modified considerably in order to account for the richness of the observed effects. We will propose a tentative reformulation of the Stranski-Krastanow model along the lines of dissipative self-ordering and provide experimental support from STEM and TEM observations[2-5] of self-ordered structures and compositional modulations on the atomic scale in (Cd,Zn,Mn)Se and In(Sb,As) structures that were grown with the intention of producing QDs. [1]V.A. Shchukin and D. Bimberg, Rev. Mod. Phys. 71, 1125 (1999) and refs. therein; [2]P. Moeck et al. Proc. 2000 U.S. Workshop on the Physics and Chemistry of II-VI Materials, 30th October-1st November, 2000, Albuquerque, New Mexico, to be published in J. Electron. Mater.; [3]P. Moeck et al. Proc. Mater. Res. Soc. Symp. Vol. 642, P6.3.1, accessible at www.mrs.org/publications/epubs/proceedings/fall2000/; [4]T. Topuria et al. Proc. Mater. Res. Soc. Symp. Vol. 642, P8.3.1, accessible at www.mrs.org/publications/epubs/proceedings/fall2000/; [5]P. Moeck et al., submitted to Appl. Phys. Lett.

3:00 PM Break

3:20 PM

U6, Spontaneous Emission Modification in Single InAs Quantum Dots Using a Three-Dimensional Cavity: *G. S. Solomon*[1]; M. Pelton[2]; Y. Yamamoto[2]; [1]Stanford University, Solid State Photonics Lab. & Edward L. Ginzton Lab., Stanford, CA 94305-4085 USA; [2]Stanford University, Edward L. Ginzton Lab., Stanford, CA, USA

The modification of spontaneous emission from individual, strain-induced InAs quantum dots (QDs) is demonstrated using a three-dimensional (3D) microcavity. The microcavity is initially a planar, semiconductor cavity formed from two epitaxial GaAs and AlAs distributed-Bragg reflector (DBR) layers, which is processed into a micropost cavity using e-beam lithorgraphy and dry etching. The emission properties of isolated QDs are measured first without a cavity, where the emission is nearly isotropic within the host GaAs. The spontaneous emission lifetime is measured to be 1.3 ns. The properties of the vacuum field are modified using principles of cavity quantum electrodynamics (cavity QED). This is initially observed using a planar microcavity, where a continuous distribution of modes is present from the cutoff wavelength to the stopband edge. In the micropost cavity, the continuous mode distribution becomes discrete. Inhibited and enhanced spontaneous emission of individual QDs is now observed within the discrete electromagnetic cavity mode. The spontaneous emission rate is reduced to 280 ps and the single-mode, polarization-degenerate coupling efficiency is increased to nearly 80%. Thus, these sources are promising candidates for single photon-light sources.

3:40 PM

U7, Pyramidal Three-Dimensional Optical Microcavities with High Resonance Q Values in Short-Wavelength Region: Akio Ueta[1]; Hidekazu Kumano[1]; Togo Shimozawa[1]; *Ikuo Suemune*[1]; [1]Hokkaido University, Rsrch. Inst. for Elect. Sci., Kita-12, Nishi-6, Sapporo 060-0812 Japan

Control of spontaneous emission processes by the modification of the photonic fields is attracting much attention from the viewpoints of basic physics and applications to high-speed light emitters and quantum computing. Semiconductor microcavities based on distributed Bragg reflectors have been intensively studied, but the enhancement of the spontaneous emission rate in this kind of 1-dimensional cavities are limited to below ~3. Various kinds of three-dimensional microcavities have been studied to overcome this problem, such as micro-spheres, microdiscs, and pillar structures. However micro-spheres and microdiscs have the problem of how to take out the light output possibly normal to the surface and the pillar structures have the one of the mechanical stabilities. We have demonstrated that pyramidal structures can function as 3-dimensional microcavities where discrete photonic modes exist with the respective 3-dimensional resonances[1]. These pyramidal structures are called as “photonic dots” from such functions as the 3-dimensional resonances in the discrete photonic modes. In this paper, observation of photonic resonance modes with the Q value as large as ~5000 is demonstrated in ZnS pyramidal structures directly grown on GaAs. The main factors contributing to this high Q value will be discussed. The ZnS pyramidal structures were grown selectively with metalorganic molecular-beam epitaxy at the substrate temperature of 350°C. (001) GaAs surfaces were covered with

carbonaceous masks deposited with scanning electron-beam irradiation, where square mask openings with the size of 0.5~1.5 mm aligned along [100] directions were formed. ZnS is selectively grown in the square opening area, and pyramidal structures of which side facets were completed with the (034) crystal plane in a self-organized manner were fabricated. The size of the pyramidal structures are almost uniquely determined by the size of the mask openings. The optical resonances were observed in the wavelength range of 390 nm ~430nm. In spite of the simple pyramidal structure in the present 3-D. microcavity, the resonance Q value as large as ~5000 was observed with reflection spectrum measurements. The successful observation of the optical resonance in the short wavelength region is attributed to the large refractive indices of the GaAs substrates due to the E1 and E2 peaks in the above wavelength range. Reference [1]I. Suemune et al, APL, 74 (1999) 1963.

4:00 PM (Student)

U8, Lateral Conductivity and Large Negative Magnetoresistance in Self-Organized Quantum Dots: *Boaz Kochman*[1]; Siddhartha Ghosh[1]; Jasprit Singh[1]; Pallab K. Bhattacharya[1]; [1]University of Michigan, Dept. of Electl. Eng. & Comp. Sci., Solid State Elect. Lab., 1301 Beal Ave., Ann Arbor, MI 48103 USA

Epitaxially grown and strained self-organized quantum dots have generated a great deal of interest for some time both from a physics and device-application point of view. While there have been a number of optical and electronic studies reported on self-organized dots, there is little understanding of lateral transport. The self-organized dot system is highly suitable for studying conduction mechanisms in localized states in a quasi-zero-dimensional space. In this work, we measure lateral conductance in self-organized InAs dot layers using a gated device, which allows us to vary electron density in the dot region and individually study several regimes of transport. At low temperature and very low electron densities, only the ground state of the dots is occupied. Since the electrons are highly localized in the ground state we find negligible conductivity. At moderate electron densities, the excited state is occupied but the extended states are not. In this case, we find that above 100K electrons are thermally excited into the extended states, and transport occurs primarily through the extended states. Below 100K thermal energy is too low for significant electron activation into the extended states, but the electron wavefunction in the excited state is sufficiently spread to allow significant coupling. As in amorphous materials, we expect variable range hopping which is mediated by phonons. We extend Mott's variable range hopping model used to describe conduction in amorphous materials[1] to our case of self-organized quantum dots. Our model predicts that the in-plane conductance varies as $G=G_0\exp[-(T_0/T)^{1/3}]$, which matches experimental results well. The temperature T_0 is related to the inter-dot size fluctuations arising from the self-organization process and is found to be 7100K. At low temperatures we have also observed a large negative magnetoresistance as is often found in amorphous semiconductors[2], which further reinforces the hypothesis that hopping conduction is prevalent in this temperature regime. At high electron densities, the extended states are occupied, so transport is essentially similar to transport in degenerate semiconductors. We also measure electron velocity in self-organized quantum dot layers as a function of electric field at room temperature. We find that electron mobility decreases with increasing electric field in the range measured (up to 10 kV/cm). We develop a Monte Carlo model to understand the origin of this effect. In the thermally activated conduction regime, the dots can be viewed as traps for electrons drifting in the extended states. At a higher field, the average electron energy is higher and because these hot electrons are less likely to be trapped by the dots, we observe a higher mobility. Velocity-field measurements at low temperatures are currently underway and will be also be presented. This work supported by the National Science Foundation and the Army Research Office (MURI program). [1]N.F. Mott, Philos. Mag. 19, 835(1969); [2]B. Movaghar and L. Schweitzer, J. Phys. C 11, 125(1978).

4:20 PM

U9, Phonon Emission by Individual InAs/GaAs Quantum Dots: *Andrei Yu Silov*[1]; Arthur W. E. Minnaert[1]; Joachim H. Wolter[1]; [1]COBRA Research Institute, Eindhoven Univ. of Tech., Bldg. NL A2.10, PO Box 513, Eindhoven 5600MB The Netherlands

We show that the micro-photoluminescence (PL) of the self-assembled InAs/GaAs quantum dots displays efficient phonon emission from the individual dots. The correlation analysis allowed us to determine experimentally the involved phonon energies and the average number of phonons emitted per photon. The quantum dots were grown by Molecular Beam Epitaxy on exactly oriented [001] GaAs substrates. The dots are from 7 to 12 nm at the base with a height ranging from 2.5 to 4 nm. The low-temperature PL is at its maximum at 1.313 eV under non-resonant excitation. To isolate a countable amount of the quantum dots, mesas with sub-micron dimensions were developed using wet chemical under etching. The micro-PL autocorrelation as a function of the emitted photon energy always shows a strong peak centered at the GaAs-like LO-phonon energy. These are the same phonons as observed in our resonant macro-PL experiments. The correlation function of the micro-PL was defined in such a way that its peak value gives the Huang-Rhys parameter averaged over the size-distribution of the self-assembled quantum dots. We found that the FWHM of the autocorrelation peak amounts to 1.5 meV. This clearly demonstrates a spread in the phonon energies due to the (non-uniform) strain field. On account of the spread in phonon energy it is impossible to measure the Huang-Rhys parameter for the individual dots from the low temperature micro-PL data alone. We used the size-dependent carrier escape to demonstrate that the light emission by a single dot is indeed accompanied by the phonon emission. Since a principle line and the phonon-assisted line represent the same initial state, they both are quenched at the identical rate as the temperature increases. This enables to pinpoint unambiguously a correlated pair of the micro-PL lines. We found the Huang-Rhys parameter for the individual dots as large as 0.6.

4:40 PM (Student)

U10, Temperature Dependence of Carrier Relaxation and Dynamics in InAs and InGaAs QDs: Experiment and Model: *Chuanshun Cao*[1]; Dennis D. Deppe[1]; Thomas F. Boggess[2]; Lin Zhang[2]; [1]The University of Texas at Austin, Dept. of Electl. & Comp. Eng., Microelect. Rsrch. Ctr., 10100 Burnet Rd., Bldg. 160, Austin, TX 78758 USA; [2]The University of Iowa, Dept. of Phys. & Astron., Optical Sci. & Tech. Ctr., Iowa City, IA 52242 USA

Carrier relaxation in self-organized InAs and InGaAs quantum dots (QD) has now been a focus of may experimental studies. However, few have dealt with the temperature dependence of the carrier relaxation, or provided models that are capable of predicting and explaining this temperature dependence. Here we present a rate equation model based on coupling of the self-organized QD zero-dimensional levels, and its wetting layer, to a thermal phonon reservoir, and compare the model to experimental data on self-organized InGaAs and InAs QDs of different sizes. Both the experimental data and the rate equation model show that the carrier relaxation can have widely varying values depending on the electronic structure, and either increase or decrease with increasing temperature. Our experimental results show evidence of a weak phonon bottleneck for small InAs QDs that have widely separated energy levels. The experiment data shows that the temperature dependencies of the carrier relaxation times are quite different between two different QD samples. For rather large InGaAs QDs (350Å in diameter and 110Å in height after covering), the electron-hole pairs excited to the wetting layer relax to the QD ground state in times as short as ~1 psec for 11K, while this relaxation time increase to ~2.3 psec for 200K. But for the InAs QDs (250Å in diameter and 30Å in height after covering), the carrier relaxation time for 11K and 200K are 6 psec and 5.2 psec, respectively, shows a decrease with increasing the temperature.In our modeling, the differences between the two QDs samples are the degeneracy of wetting layer energy states which couple to the QD upper energy levels and the energy separations between the ground and higher excitations. For InGaAs QDs we find the energy separations between multiple discrete radiative transitions to be 65, 51, 51,46 meV, and for InAs QDs we find 93, 82, 60 meV. The different energy separations between radiative transitions reflect the different energy separations between the discrete electron and hole energies. By considering a narrow spectrum phonon reservoir (due to optical phonons) and the large density of levels due to the QD wetting layer we are able to model both the change in the relaxation times between the two different samples and the two different temperature dependencies of the relaxation times. Both the experimental data and the mechanisms leading to the different dynamic behavior will be discussed extensively in the talk.

Session V:
SiC Growth and Characterization

Thursday PM Room: 141
June 28, 2001 Location: University of Notre Dame

Session Chairs: Michael Spencer, Cornell University, Electl. Eng. Dept., Ithaca, NY 14853 USA; Robert S. Okojie, NASA Glenn Research Center, Cleveland, OH 44135 USA

1:20 PM

V1, High Quality Step-Flow Growth of Homoepitaxial 6H-SiC: *William V. Lampert*[1]; Christopher J. Eiting[1]; Scott A. Smith[1]; Krishnamurthy Mahalingam[1]; T. W. Haas[1]; Larry Grazulis[2]; James S. Solomon[2]; [1]Air Force Research Laboratory, Matls. & Mfg. Direct., AFRL/MLPS, Wright-Patterson AFB, OH 45433-7707 USA; [2]University of Dayton, Univ. of Dayton Rsrch. Inst., 300 College Park, Dayton, OH 45469 USA

The physical and electronic properties of SiC make it a candidate semiconductor material for many applications of interest to the Air Force, including high temperature detectors and transistors, high power switches and rectifiers, and high frequency transistors. Novel SiC devices utilizing nearly lattice-matched polytype heterostructures can be envisioned as well. Of all the epitaxial growth techniques, molecular beam epitaxy (MBE) is probably the most likely candidate for growing such structures because of its monolayer control capability and its compatibility with in-situ surface characterization. In this presentation, we will report on the step-flow growth of homoepitaxial 6H-SiC by solid-source MBE using C_{60} and Si effusion cells. Specifically, we will discuss the effect of growth conditions such as surface reconstruction, source flux, and substrate temperature on the growth mode of these epitaxial layers. We will also talk about the influence of such ex-situ substrate preparation steps as chemical-mechanical polishing (CMP) and wet etching on the quality of the films. Atomic force microscopy (AFM) images will be presented that show terraced surfaces and surface roughnesses of less than 1.0 nm rms. These images also show evidence of step-bunching and faceting. Scanning electron micrographs (SEM) and cross-sectional transmission electron microscopy (TEM) results will be displayed to demonstrate the high quality of the interface and the 6H-SiC epitaxial layers.

1:40 PM

V2, Lateral Growth of Thin Cantilevers from Atomically Flat 4H- and 6H-SiC Mesa Surfaces: *Philip G. Neudeck*[1]; J. Anthony Powell[1]; Andrew J. Trunek[2]; Glenn M. Beheim[1]; David J. Spry[2]; [1]NASA Glenn Research Center, 21000 Brookpark Rd., MS 77-1, Cleveland, OH 44135-3191 USA; [2]Akima Corporation, NASA Glenn Rsrch. Ctr., 21000 Brookpark Rd., MS 77-3, Cleveland, OH 44135-3191 USA

We report on the formation of thin, lateral single-crystal SiC cantilevers that are observed to emanate from atomically flat (i.e., completely step free) 4H- and 6H-SiC mesas produced by CVD homoepitaxy on pre-growth patterned on-axis commercial substrates. These cantilevers, which are on the order of a micrometer in thickness, form in epitaxial growth conditions where the two-dimensional (2D) nucleation rate is close enough to zero that device-size mesas (as large as 0.4 x 0.4 mm observed to date) become step free as previously described[1, 2]. Based on preliminary observations, we propose the following mechanism for the observed cantilever formation. In the absence of steps and 2D nucleation on the top of a large step-free surface, vertical epilayer growth in the c-axis direction ceases as previously reported[1, 2]. Nevertheless, growth reactants in the CVD system impinge on the atomically flat surface areas and become mobile surface adatoms that diffuse around the step-free surface. These mobile adatoms eventually diffuse to the edge and flow off the top surface onto the mesa sidewall. The favorable bonding (i.e., high step density) of the mesa sidewall promotes rapid incorporation of adatoms into the crystal before they diffuse more than a few micrometers below the top edge of the mesa sidewall. Cantilevers are not observed on mesas that contain screw dislocations prior to epitaxial growth, as the screw dislocations readily provide steps for incorporating top surface adatoms into the crystal resulting in vertical growth of the mesa top surface and preventing realization of a step-free top surface[2]. Cantilevers extending on the order of ten micrometers from the edge of the mesa have been observed. The cantilevers exhibit well-known {1100} hexagonal crystal growth facets. Because the crystal structure of the cantilevers is established laterally from the mesa sidewall, these cantilevers may prove useful in terminating the vertical propagation of some screw dislocations that reside outside the pre-growth mesa. The thin cantilevers also offer a new method for realizing single-crystal SiC-based three-dimensional structures for MEMS applications. [1]J. A. Powell, et. al., EMC Late News Paper, (2000); [2]J. A. Powell, et. al., Appl. Phys. Lett., 77(10), p. 1449 (2000).

2:00 PM (Student)

V3, In-Situ Etching of SiC Prior to Epitaxial Growth Using H2/O2 Gas Mixtures: *Ishwara Bhat*[1]; *Rongjun Wang*[1]; [1]Rensselaer Polytechnic Institute, ECSE Dept., JEC 6032, 110 8th St., Troy, NY 12180 USA

Quality of a SiC epitaxial layer depends to a great extent on the quality of substrate surface. Hydrogen etching at the growth temperature is the conventional method used for removing scratches on the commercially available substrates. However, Si droplets usually form on the surface. Formation of droplets can be inhibited by adding a small amount of C3H8 in the H2 flow. However, addition of C3H8 reduces the etching rate considerably. We have investigated a new method to etch SiC by adding a small amount of oxygen in the hydrogen flow to overcome the above problem. Etching experiments under various temperatures and oxygen flow rates are performed. The etched surfaces are examined by optical microscope, AFM and XPS. Etching was performed in a horizontal water-cooled cold-wall CVD reactor. High purity oxygen diluted in Argon was used as the source, in addition to hydrogen as the bulk of carrier flow. The substrates used were (0001) Si-face, 3.5°-off 6H-SiC from Cree Research, Inc. Etching was carried out for 30 minutes at 100torr and at a temperature in the range from 1500 to 1600°C with different flow rates of oxygen. First, etch rate was measured at different temperatures and oxygen flow rates. The result shows that at a certain temperature, etch rate first increases rapidly (liner region) and then saturates with the increase of oxygen flow. When observed under the optical microscope, samples etched using a low oxygen flow (linear region) show a smooth and featureless surface, and samples etched under the saturation region show very poor morphology. The oxygen flow and the etch rate required for getting the rough surface increases with the etching temperature. Etch rate as high as 8•m/hr was obtained. High-resolution XPS spectra from Si2p for etched samples were obtained. They can be fitted with four Gaussian peaks which are assigned to Si (99.2eV), SiC (100.4eV), SiOx (x<2) (101.7), and SiO2 (103eV). The fraction of each compound was calculated by determining the ratio of peak area. The result shows that SiO2 on the surface increases while Si decreases with the increase of oxygen level in the system during etching. We believe that the saturation of etching rate and the rough surface obtained at higher oxygen concentration are the direct result of the formation of SiO2 on the surface. AFM on sample etched with pure hydrogen shows lots of sub-micron size white dots probably caused by Si droplets. They can be removed by dipping the sample into hot HF/HNO3 solution for a few minutes. No white-dots can be seen on all H2/O2 etched samples. AFM also reveals the appearance of micro step bunching. The width and height of step increase with the increase of oxygen used during the etching. Excellent surface was obtained when epitaxial growth was carried out on this oxygen-etched surface.

2:20 PM

V4, Al Doping (>1e20 cm-3) of SiC by Liquid Phase Epitaxy and Resulted Ohmic Contacts: *Alexander L. Syrkin*[1]; Vladimir A. Dmitriev[1]; Alexey Morozov[1]; Oleg Kovalenkov[1]; Dmitriy Bauman[2]; John Crofton[3]; [1]Technologies and Devices International, Inc., 8660 Dakota Dr., Gaithersburg, MD 20877 USA; [2]Crystal Growth Research Center, St. Petersburg 194021 Russia; [3]Murray State University, Dept. of Phys. & Eng., Murray, KY 42071 USA

Highly doped p^+-SiC layers are required for most of bipolar devices based on this material. High doping level is needed particularly for the fabrication of low resistivity Ohmic contacts. Contact resistivity is currently one of the limiting factors for several types of SiC-based power and microwave power devices (e.g. IMPATT diodes, microwave limiters etc.). Commonly used epitaxial techniques such as chemical vapor depo-

sition and sublimation epitaxy cannot provide Al atomic concentration sufficiently high for reproducible Ohmic contacts with specific contact resistance lower then 10^{-4} Ω cm^2. Much higher concentration of Al can be obtained only by ion implantation, but in contrast to epitaxial methods, ion implantation introduces a lot of structural defects and requires post-implantation high temperature annealing. We report on results of intentional doping in 6H- and 4H-SiC with Al during epitaxial growth from liquid phase. Liquid phase epitaxy (LPE) does not introduce damage in grown SiC and does not require post-growth anneal to activate impurities. 4H-and 6H-SiC layers doped with Al were grown on both (0001) off-axis commercial SiC wafers and p-n epitaxial structures. Surface morphology and crystal structure of grown layers were investigated by scanning electron microscopy, optical microscopy and x-ray diffraction. Al atomic concentration in grown materials measured by SIMS ranged from 5×10^{19} to 7×10^{20} cm^{-3} for different samples. SiC epitaxial samples grown by LPE technique have been used for Ohmic contact fabrication. An Al-Ti alloy was used to form the ohmic contacts. For comparison, Ohmic contacts were also formed on commercially available p-SiC epitaxial layers. Contact resistance was measured by the linear TLM method. Semiconductor sheet resistances were determined using four point probe measurements in addition to the measurements obtained from the TLM contact resistance patterns. Contacts with record-low resistivity were obtained for p-6H-SiC and p-4H-SiC layers grown by LPE. Results of material and contact investigation will be presented. This work is supported by ONR (contract monitor John Zolper).

2:40 PM (Student)

V5, Growth and Doping of SiC Thin Films on Low-Stress, Amorphous Si_3N_4/Si Substrate for Robust MEMS Applications: *Lin Cheng*[1]; Ming Pan[1]; James Scofield[2]; Andrew J. Steckl[1]; [1]University of Cincinnati, Nanoelect. Lab., Cincinnati, OH 45221-0030 USA; [2]Wright-Patterson Air Force Base, Air Force Rsrch. Lab., OH 45433 USA

We have investigated in-situ N_2-doped 3C-SiC thin films grown by low pressure chemical vapor deposition (LPCVD) at relatively low temperatures on low-stress amorphous Si_3N_4/p-Si (111) substrate using single organosilane precursor [trimethylsilane $SiH(CH_3)_3$]. The effects of N_2 flow rate and growth temperatures on the electrical properties of SiC films were investigated by Hall effect measurement over a range of temperatures. The electron carrier concentration is between 10^{17}~10^{18}/cm^3. The lowest resistivities at 400K and 300K are $8.11x10^{-2}$ and $2.02x10^{-1}$ Ω-cm, respectively. The corresponding sheet resistances are 811 and 2024 Ω/square. The resistivity and sheet resistance can be readily controlled by the flow rate of N_2 and growth temperature. The structure of the SiC films was studied by X-ray diffraction (XRD) spectra and reflection-mode Fourier transform infrared (FTIR) spectra. The crystalline 3C-SiC films oriented in the <111> direction with a 2θ peak at 35.5° and line widths between 0.20°~0.25° were obtained on all growth runs. The Si-C bond vibration peak frequency around 780 cm^{-1} was also shown on all samples. The surface and interface of the grown films were examined by scanning electronic microscope (SEM). The SiC-Si_3N_4 interface is very smooth and free of voids. Initial fabrication of MEMS structures by inductively coupled plasma (ICP) dry etching has shown that LPCVD conformal growth of SiC on low-stress amorphous Si_3N_4 layer is successful. During the ICP etching processes, NF_3/Ar, Cl_2/Ar and NF_3/Cl_2/Ar gases systems were utilized to produce smooth surfaces that are free of hydrogen passivation effects. Surface roughness and morphology were examined by atomic force microscope (AFM). Several different materials (photoresists, ITO, Al) were evaluated as possible masks for high selectivity. Vertical side walls indicating high anisotropy NF_3/Ar etching has been obtained under certain conditions. A detailed discussion of etching rate dependence on etching conditions (such as gas flow rate, gases ratio, ICP power, RF chuck power, DC bias and chamber pressure) will be presented. Simple MEMS structures such as cantilevers, lateral resonators and resonating membranes has been fabricated. The film stress was measured by using bent-beam strain gauges. The deflecting angle of our bent-beam is 6°. The residual stress generated by a bimorph involving a SiC thin film has been estimated ~188 MPa. Lateral deflection of the supporting beam vernier structures correlates directly to the stress in the deposited film. A value of Young's Modulus E = 426 GPa was used for stress calculations and was obtained from MEMS resonance measurements for SiC films.

3:00 PM Break

3:20 PM (Student)

V6, Nucleation of Threading Dislocations in Sublimation Grown SiC: E. K. Sanchez[1]; J. Q. Liu[1]; W. M. Vetter[2]; M. Dudley[2]; *M. Skowronski*[1]; [1]Carnegie Mellon University, Matls. Sci. & Eng., 5000 Forbes Ave., Pittsburgh, PA 15213 USA; [2]State University of New York, Matls. Sci. & Eng., Stony Brook, NY 11794 USA

Commercially available SiC wafers have 1c [0001] screw dislocation densities in the 10^3-10^4 cm^-2 range and threading edge dislocations densities between 10^4 and 10^5 cm^-2[1,2]. Both types have been shown to be detrimental to devices parameters such as the breakdown voltage and carrier lifetimes. Their formation mechanism is still unknown. This report describes the initial stages of PVT growth focusing on nucleation of 2D islands and the formation of threading dislocations. The sublimation growth of silicon carbide on 6H Lely platelets used as seed crystals, with no surface damage and no threading dislocations, was investigated. Since careful seed preparation removed all step sources on basal plane seeds, the SiC growth was initiated by nucleation of 2D islands. Cross sectional transmission electron microscopy images revealed a layer of stacking faults at the seed/crystal interface with width between 1 and 10 microns. The number of stacking faults ranged from 5 to 100 with both Frank and Shockley st acking faults present. The width of the stacking fault band correlated well with the threading dislocation density and the growth rate. A growth rate of 1.5 mm/hr resulted in a screw dislocation density of 4x10^3 cm^-2 while the 0.020 mm/hr rate produced a crystal with a threading screw dislocation density of only 20 cm^-2. This is the lowest screw dislocation density reported in seeded sublimation growth of SiC. The change in dislocation density was interpreted as due to lower super-saturation during growth and lower 2D island density. Growth on off-axis seeds have screw dislocation densities about 2 orders of magnitude lower than the growth on basal plane seeds which is consistent with proposed interpretation. Off-axis surfaces have many steps and hence have no need to nucleate 2D islands. [1]M. Dudley, X. Huang, Mater. Sci. Forum 338-342, 431 (2000); [2]J. Takahashi, N. Ohtani, M. Kanaya, J. Cryst. Growth 167, 596 (1996).

3:40 PM (Student)

V7, Evidence of Basal Plane Slip During Sublimation Growth of Silicon Carbide: *Seoyong Ha*[1]; William M. Vetter[2]; Michael Dudley[2]; Marek Skowronski[1]; [1]Carnegie Mellon University, Matls. Sci. & Eng., 5000 Forbes Ave., Pittsburgh, PA 15213 USA; [2]State University of New York at Stony Brook, Matls. Sci. & Eng., Stony Brook, NY 11794 USA

High resolution X-ray diffraction (HRXRD), synchrotron white beam X-ray topography (SWBXT) and optical microscopy of KOH etched SiC wafers were used to study the morphology of the basal plane dislocations in the physical vapor transport (PVT) grown silicon carbide crystals. Basal plane slip system has been known as the primary deformation mechanism of hexagonal silicon carbide polytypes. High temperature deformation studies of single crystals and modeling of stress distribution in growing crystals indicated the likelihood of plastic deformation due to thermoelastic stresses during growth. In this study, we report the morphology of basal plane dislocation distribution observed in several hexagonal silicon carbide wafers grown by the PVT method. Arrays of etch pits were observed on silicon faces of KOH etched off-cut wafers. They were aligned parallel to each other and perpendicular to the off-cut direction. Each array was a single line or a band with a width between 30~200 ìm. The etch pits had the oval-shaped morphology characteristic of basal plane dislocations. SWBXT showed one to one correlation of these etch pit arrays and highly concentrated contrasts due to basal plane dislocations. The dislocation lines were approximately parallel to each other and the Burgers vectors were identical in an array. Based on these characteristics, the arrays of etch pits were interpreted as the slip traces of high temperature deformation during growth. The arrays could be found both in the middle and in the edge area of the off-cut wafers. They were up to 10 mm long in a 50 mm diameter wafer, which indicates that they are formed due to a long range stress such as the thermoelastic stress from non-uniform temperature field in the growing crystals. Similar arrays of the basal plane dislocations were found around threading dislocation arrays described before by Takahashi et al. Their morphology was consistent with a train of basal plane dislocations gliding in one plane piling up against a threading dislocation fence. HRXRD and SWBXT were used to study the misorientation related to such structure. The basal dislocation

pile-ups were interpreted as a plausible origin of tilt domains in SiC crystals.

4:00 PM

V8, EPR Study of the Interaction Between Intrinsic Defects and N/B Impurities in Semi-Insulating SiC: *Valery V. Konovalov*[1]; Mary Ellen Zvanut[1]; [1]University of Alabama at Birmingham, Dept. of Phys., CH310, University Blvd. 1300, Birmingham, AL 35294-1170 USA

Electron paramagnetic resonance (EPR) is employed to examine the thermo- and photo-activated interactions between as-grown defects and nitrogen/boron impurities in high quality electronic-grade SiC. The studies reveal an intrinsic defect (ID) which photoexchanges charge with B and has an energy level within 1.3 eV of the conduction band edge (Ec). 4H SiC substrates with different densities of N and B impurities were studied between 4.2 and 300K by 9.5 GHz EPR. Spectra obtained in the dark reveal: 1) in the most lightly doped samples, an anisotropic line and four satellite lines which are thought to be due to an intrinsic defect; 2) in the p-type samples, the shallow B acceptor which is stable between 4.2 and 80K; 3) in the n-type samples, the N donor which is observed only above 50K. Illumination with sub-band gap light (460 nm) at 4.2K and subsequent annealing without light between 15-300K produced different EPR responses. For the lightest doped samples, illumination quenched the ID signal and produced an approximately equal amount of paramagnetic shallow B acceptors. The B signal was stable without light at 4.2K, but, at T > 80K, began to diminish as the ID center increased, and was completely replaced by the initial ID signal after heating to 200K. In contrast, for n-type samples illumination increased the intensity of the N signal and produced the ID signal. After blocking the light, the spectrum returned to the initial state observed in the dark. The observed phenomena can be described by a model involving photo-induced charge transfer between ID and boron. The most probable channel includes photoexcitation of an electron from the valence band to ID, making it non-paramagnetic. The B acceptor captures a valence band hole and becomes paramagnetic. The electron and hole, localized on ID and B, are separated by an energy barrier and do not recombine until T > 80K. The B signal was much weaker after illumination at 633 nm compared to 460 nm, suggesting that the defect level is less than 1.3 eV below Ec. In n-type samples, ID should lie below the Fermi level and only reveal an EPR signal when illuminated. The thermal excitation of the N donor observed in the dark may be attributed to ID, or it may require a second shallow donor defect. The EPR data suggest that B, and perhaps N, exchange charge with ID. Comparing the estimated energy depth to deep levels identified by other techniques indicates that ID may be the 1.1 eV level which is thought to pin the Fermi level. Future photo-induced EPR measurements will focus on the relationship between ID, the impurities, and the 1.1 eV level.

4:20 PM (Student)

V9, Observations of Deep Levels in 4H-SiC Using Optoelectronic Modulation Spectroscopy: *Chi-Hsin Chiu*[1]; Philippa J. M. Parmiter[2]; Keith Hilton[2]; Michael J. Uren[2]; Garth Swanson[1]; [1]King's College London, Dept. of Electl. Eng., Strand, London WC2R 2LS UK; [2]DERA Malvern, St Andrews Rd., Malvern, Worcestershire WR14 3PS UK

OEMS senses the effect of light of definite photon energy on an electrical parameter associated with a semiconductor device structure. In this modulation spectroscopy the photon energy is periodically modulated and it is the modulation of the electrical parameter that is measured. The magnitude is then displayed as a spectrum as the mean photon energy is scanned. If the response is not in phase with the variation of photon energy the phase as well as magnitude can be plotted to form a pair of related spectra. The method has been previously used in various modes to explore the optical responses of FET's, pn and Schottky diodes as well as simple resistors. In this study, OEMS is applied to 4H-SiC MESFET's in which channel conduction is determined by the thickness of the gate and backplane depletion regions, and by the carrier concentration and their average carrier mobility. If any of these parameters were affected by the incident light a change in channel current would be seen. Sub band-gap photons were used to permit penetration into the semiconductor in order to excite charges in deep defect states. Pairs of magnitude and phase spectra have been used to infer whether the responses were from electron or hole traps. Eleven discrete trap responses have been observed, eight were assigned as electron traps and three as hole traps. Five of these had been observed previously using optical admittance spectroscopy. An electron trap at 1.20eV gave the most prominent response with a distinctive signature indicating that these traps were spatially delocalised with an extent of ~17nm, possibly associated with an extended defect structure. An unresolved continuum of hole traps was seen between 2.3eV and 2.9eV. A response at 0.72eV appeared to be the superimposed response of an electron and hole trap at closely similar energies. Previous DLOS observations are consistent with some of the states observed here.

4:40 PM, V10, Late News

Session W: Non-Destructive Testing and In-Situ Monitoring and Control

Thursday PM, June 28, 2001
Room: 136
Location: University of Notre Dame

Session Chairs: Kurt Eyink, Wright-Patterson AFB, OH 45433 USA; Mark Goorsky, University of California–Los Angeles, Dept. of Matl. Sci. & Eng., Los Angeles, CA 90095-1595 USA

1:20 PM (Student)

W1, Emissivity and Sample Temperature Variations During Growth on Silicon on Insulator Substrates: *Eric M. Rehder*[1]; T. F. Kuech[1]; [1]University of Wisconsin–Madison, Matls. Sci. Prog., 1415 Engineering Dr., Madison, WI 53706 USA

Pyrometry temperature measurements are routinely used in semiconductor processing. Pyrometry has many well-known limitations, which require careful calibrations of the sample emissivity for reproducible results and moderate accuracy. During the deposition or etching of heterogeneous films, optical interference between the air-film and film-substrate interfaces produces oscillations in the emissivity and the apparent temperature. The reflectivity at the film-substrate interface is usually rather low allowing this complicating effect to be ignored. For example during $Si_{0.82}Ge_{0.18}$ deposition on a Si wafer, the emissivity oscillations are 3% about the value of 0.68, leading to apparent temperature variations of 5°C at 550°C. Silicon on insulator (SOI) substrates have a highly reflective buried Si/SiO_2 interface that leads to much stronger emissivity oscillations. During $Si_{0.82}Ge_{0.18}$ deposition on an SOI substrate the emissivity values will oscillate between 0.35 and 0.95. We have implemented a reflectivity-corrected pyrometry system to a Si chemical vapor deposition system to correct for these variations. The black body and reflectivity measurements are performed at 940nm, where the Si is opaque. Therefore the emissivity (ε) is derived from the relationship ε = 1-R. With the real-time sample emissivity, such oscillations and sample variations can be taken into account and corrected in the process of inverting the black body intensity to obtain the true temperature. An uncorrected pyrometer operating at 1μm wavelength would measure a temperature change of 50°C, while a two-color pyrometer operating at wavelengths of 2.1 and 2.4μm would yield a temperature change of over 1000°C. The emissivity oscillation, when integrated over all wavelengths and emission angles, becomes a variation in the radiative emission of the sample. When heating at a constant input power, we observe sample temperature changes by 35°C as the top silicon layer is grown to 300nm on a SOI substrate with a 200nm SiO_2 layer. In order to achieve constant temperature film growth on SOI substrates, the true sample temperature needs to be determined and fed back to the sample heater. Standard pyrometry and adjacent thermocouple monitors will not be able to accurately correct for this variation. The description of the present emissivity-corrected technique and its application will be presented.

1:40 PM (Student)

W2, Monitoring of Ultra-Thin Oxide Processing Using Non-Contact Surface Photovoltage Method: *J. Wang*[1]; D. Lee[1]; C.-T. Wu[1]; W. Dimachkie[1]; E. Kamieniecki[2]; P. Roman[1]; J. Ruzyllo[1]; [1]Pennsylvania State University, Dept. of Electl. Eng., University Park, PA 16802 USA; [2]QC Solutions, Inc., Billerica, MA 01862 USA

Measurements of electronic properties of the silicon surface and near-surface region are necessary to monitor and develop processing methods in advanced MOS manufacturing. Non-contact surface photovoltage (SPV) measurements may provide a quick and easy method of evaluating surface electrical properties and mapping these properties over an entire wafer. The purpose of this work is to investigate the use of the SPV-based Surface Charge Profiler (SCP) method in monitoring of gate dielectric formation processes. First, this method is used to study changes taking place during the growth of ultra-thin oxides. Then, the parameters measured with SCP are compared with those from C-V measurements made on thicker oxides. Finally, high-resolution maps of surface parameters obtained with SCP are used to characterize gate dielectric formation processes and equipment. In this method, an alternating current SPV signal is obtained by illuminating the wafer with a beam of chopped low-intensity, short-wavelength light with shallow penetration depth (450 nm). The real and imaginary parts of the signal are analyzed to determine the surface depletion width (W_d) and the surface minority carrier lifetime (τ). Under depletion conditions W_d can be used along with the known wafer doping to determine the total surface charge density (Q_s), and when the surface is inverted, doping concentration (N_{sc}) can be deduced. Measurements were made using a commercial SCP tool. P-type, (100) wafers with various resistivities were used. In our experiments, wafers were first treated with a 1 minute dHF(dilute hydrofluoric acid) step and 2 minutes DI water rinsing before oxides were grown. Oxides were grown at 750°C in 3% O_2 in 1slm N_2. The growth time was varied from 0 to 45 minutes. to facilitate the study of surface parameters in different stages of oxidation. Thicker oxides (50 nm) were grown at 1000°C and nitrided with subsequent N_2O annealing. Thin films of alternate high-k dielectrics were also deposited by the LSMCD (Liquid Source Misted Chemical Deposition) method. As an example of the results obtained we first investigate changes of surface electrical parameters during an oxidation process via the SCP technique. Surface charge Q_s and lifetime τ data as a function of various oxide thickness are obtained. Minimum values in Q_s and τ are observed when the oxide grows to the thickness of about 1.2 nm. And also Q_s tends to be constant after the oxide thickness grows beyond 3 nm which indicates the development of the interface. Complete discussion of these results is presented in the full account of this work.

2:00 PM

W3, Angle Dependent Surface Photovoltage Spectroscopy Study of GaAs/GaAlAs Vertical Cavity Surface Emitting Laser Structures: J. S. Liang[1]; *Y. S. Huang*[1]; C. W. Tien[2]; Y. M. Chang[2]; C. W. Chen[2]; N. Y. Li[2]; P. W. Li[3]; Fred. H. Pollak[4]; [1]National Taiwan University of Science and Technology, Electl. Eng., 43 Sec., 4 Keelung Rd., Taipei 106, Taiwan, China; [2]Kingmax Optoelectronics, Inc., Hu Ko, Hsin Chu 303 Taiwan; [3]National Central University, Electl. Eng., Chung Li, Taoyuan 320 Taiwan; [4]Brooklyn College of CUNY, Phys., Brooklyn, NY 11210 USA

Vertical cavity surface emitting lasers (VCSELs) only laser effectively when the emission wavelength of the quantum well (QW) coincides with the Fabry-Perot resonance of the inner cavity and with the maximum reflectivity wavelength of the distributed Bragg reflectors (DBRs). In order to characterize epitaxial structures before laser processing, methods for the rapid determination of the excitonic transition of QW, cavity mode, and thickness of quarter wavelength layers in the DBRs are demanded. An angle dependent surface photovoltage spectroscopy (SPS) study has been performed at room temperature on several GaAs/GaAlAs-based VCSELs structures (emitting at wavelength near 850 nm). For comparison purposes, we have also (a) measured angle dependent photoreflectance (PR) and reflectance (R); and (b) calculated the number of photo-excited carriers (PEC), which is related to the SPS signal. The SPS spectra exhibit both the fundamental conduction to heavy-hole (1C-1H) excitonic transition and cavity mode plus additi onal interference features related to the properties of the mirror stack.* The PR data show both the 1C-1H excitonic transition and cavity mode as well, whereas in the R spectra only the cavity mode is clearly visible. The energy position of the excitonic feature is not dependent on the angle of incidence, in contrast to that of the cavity mode, whose angular dependence can be fitted with a simple model. The amplitude of the excitonic feature is about one order of magnitude smaller than that of cavity mode. In addition, the interference pattern from DBRs is in good agreement with the PEC calculation. This study demonstrates the considerable potential of SPS for the characterization of VCSEL structures. *Y. S. Huang, L. Malikova, Fred H. Pollak, H. Shen, J. Pamulapati and P. Newman, Appl. Phys. Lett. 77, 37 (2000).

2:20 PM

W4, Characterization of Subsurface Damage in Nano-Patterned GaAs Using Micro-Raman: *Kurt G. Eyink*[1]; Larry Grazulis[1]; John D. Busbee[1]; [1]Air Force Research Laboratory, Matls. & Mfg. Direct., AFRL/MLPS, 3005 P St., Ste. 6, Wright-Patterson AFB, OH 45433 USA

A single point diamond machine has been used to fabricated patterns consisting of a series of equi-spaced lines in an area of nominally 10µx10µ. On a single GaAs wafer patterns with line spacing of 200nm, 100nm, 66nm and 50nm were machined using loads of 5mg, 7mg, 9mg and 12mg. AFM was used to characterize the surface morphology and depth of cut of these patterns as a function of load. It was found that the depth of cut increased in a monotonic manner to a depth of approximately 10nm. The technique of µ-Raman was used to characterize the subsurface damage in these layers by comparing the LO and TO phonon spectra. At high loads the patterned area exhibited a strong TO phonon, nearly half the intensity of the LO phonon, along with an increase in the background in the phonon spectra. The increased TO phonon presence indicates residual stress in the patterned regions. The patterned areas were annealed at ~600°C under an As flux for 1 hour and recharacterized using AFM and µ-Raman. AFM results indicated essentially no change in the surface morphology. Raman spectra showed that the TO phonon decreased to nearly the same intensity as in the unpatterned area and the background returned to the level found on the unpatterned unannealed areas. Results will be shown and discussed for all the different depths of cut and line spacings.

2:40 PM (Student)

W5, Contactless Characterization of Multi-Epitaxial Wafer by Depth-Resolved Cathodeluminescence: *Fumitaro Ishikawa*[1]; Hideki Hasegawa[1]; [1]Hokkaido University, Rsrch. Ctr. for Interface Quantum Elect. & Grad. Sch. of Inform. & Elect. Eng., Kita-13, Nishi-8, Sapporo, Hokkaido 060-8628 Japan

For growth optimization and screening of epitaxial multi-layer structure wafers for production of advanced heterostructure devices, a non-destructive, highly sensitive and non time-consuming characterization method of buried hetero-interfaces is strongly desired. In this paper, a cathodoluminescence interface spectroscopy (CLIS) technique is proposed as such a method. CL was used previously for characterization of carrier profiles and surface and bulk deep states under a name of LEEN[1]. However, no systematic use for interface characterization has been made. For the principle of the CLIS technique, consider a simple heterostructure consisting of two materials A and B which gives, under an electron acceleration voltage V_{acc}, two near-bandgap CL peaks at energies, E_A and E_B with peak intensities $I_A(V_{acc})$ and $I_B(V_{acc})$, respectively. Since the penetration depth of electrons is strongly dependent on V_{acc}, I_A and I_B depend also strongly on V_{acc}. Plots of $I_A(V_{acc})$ and $I_B(V_{acc})$ vs. V_{acc} can be defined as CLIS spectra. If CLIS spectra for the ideal defect-free case are known by theory, or by experiments on near-ideal reference samples, then any deviations in measured spectra from ideal spectra such as change in spectra shapes and intensities, and/or appearance of unexpected CL peaks, indicate that some anomalies are present in the heterostructure. Then, by a subsequent computer analysis, it should be possible to identify the causes of the anomalies. For theoretical analysis of CLIS spectra, our one-dimensional Scharfetter-Gummel vector-matrix type semiconductor program for PL analysis[2] was modified to analyze CL. Excitation by incident electrons can be obtained by calculating the Everhart-Hoff electron energy loss curve[3]. Experimentally, CLIS spectra were taken first on a well characterized commercial high quality InGaP/GaAs wafer grown by MOVPE. Two peaks coming from InGaP and GaAs were seen, and the CLIS spectra were found to agree with the theoretical analysis. Then, the technique was applied to various InGaP/GaAs heterostructures grown on GaAs by GSMBE using TBP as the P source. A simple InGaP/GaAs heterostructure showed presence of an additional CL peak. From the theoretical analysis of its CLIS spectra, this peak was concluded to come from the interface. The CLIS spectra of an InGaP/GaAs/InGaP quantum well sample were more complicated. By analysis, a quantum well peak and interface peaks were identified with possible ordering in the bottom InGaP layer. The interface peaks were due to P-vacancy related interface defects. By proper group V switching, they could be removed. Detailed analysis of MOVPE grown HBT wafers is being performed, and the result will be also reported. [1]T. M. Levin et al, J. Vac. Sci. Technol. B 17,

2545(1999); [2]B. Adamowicz and H. Hasegawa, Thin Solid Films 367, 180 (2000); [3]T. E. Everhart and P. H. Hoff, J. Appl. Phys. 42, 5837 (1971).

3:00 PM Break

3:20 PM

W6, Chemical Imaging of an InGaN Multi-Quantum Well Structure on Fully Coalesced Lateral Epitaxial Overgrown GaN: *Thomas H. Myers*[1]; Aaron J. Ptak[1]; Patrick J. Treado[2]; Matthew P. Nelson[2]; Ryan D. Smith[2]; Monica C. Hansen[3]; James S. Speck[3]; Steven P. DenBaars[3]; [1]West Virginia University, Phys. Dept., 224 Hodges Hall, PO Box 6315, Morgantown, WV 26501 USA; [2]ChemIcon, Inc., Pittsburgh, PA 15208 USA; [3]University of California, Dept. of Electl. Eng., Santa Barbara, CA 93106 USA

GaN and its alloys lag far behind other semiconductor systems in crystal quality, purity and alloy composition uniformity. The need exists for non-destructive techniques which allow rapid, high throughput screening of material both in the research laboratory and in production environments for the determination of crystal quality, doping levels and uniformity, strain, alloy composition and defect content. Chemical imaging combines high definition digital imaging with various optical spectroscopies (e.g., infrared, Raman and photoluminescence) techniques for the chemical analysis of a wide range of materials. In this technique, a complete spectral measurement is obtained for each pixel in a digital image. Chemical imaging has been shown to be effective in the non-contact, non-invasive characterization of defects in semiconductors, including CdZnTe, ZnSe, Si, SiGe, SiC, GaN and related materials. A feasibility study was performed to assess the combination of Raman Chemical Imaging Spectroscopy (RCIS) and Photoluminescence Chemical Imaging Spectroscopy (PCIS) into a single instrument to provide high throughput screening of chemical composition, structural quality, doping levels and uniformity, strain and structural quality of GaN and related semiconductor materials by extending existing chemical imaging technology currently optimized for visible wavelength operation into the UV. This was accomplished by demonstrating the high speed materials screening capability of RCIS and PCIS independently, performing an engineering study to establish design specifications for a UV PCIS instrument and prototyping a UV chemical imaging system based on the outcome of the engineering study. The results obtained from an InGaN multi-quantum well stack on a fully coalesced lateral epitaxial overgrowth structure grown by MOCVD at UCSB will be reported. RCIS was used to measure disorder, strain and carrier concentration variation simultaneously. PCIS was demonstrated to directly image dislocations in direct bandgap semiconductors in a nondestructive fashion, allowing automated maps to be generated. PCIS was also used to map variations in both composition and point defect content simultaneously. PCIS provided the capability of mapping stoichiometric variations in a layer buried inside this complex structure. The combination of these two techniques into a single imaging instrument will provide unsurpassed semiconductor characterization and screening with analysis times of seconds to minutes. The information obtained from chemical imaging techniques will be compared to that obtained by cathodoluminescence. The work performed at ChemIcon, Inc. and at West Virginia University was supported by the Navy Small Business Innovations Research Contract N00014-00-M-0125 monitored by Colin E. C. Wood.

3:40 PM (Student)

W7, Optical Characterization of InGaN/GaN Multiple Quantum Wells with Si-Doped Barriers: *Mee-Yi Ryu*[1]; Phil W. Yu[1]; Eunsoon Oh[2]; Ok Hyun Nam[3]; Chul Soo Sone[3]; Yong Jo Park[3]; [1]Kwangju Institute of Science and Technology, Infor. & Comm., 1 Oryong-dong Puk-gu, Kwangju 500-712 South Korea; [2]Seoul National University, BK21 Phys. Rsrch. Div., San 56-1, Shilim-dong, Kwanak-gu, Seoul 151-742 South Korea; [3]Samsung Advanced Institute of Technology, Compd. Semicond. Lab., PO Box 111, Suwon 440-600 South Korea

The effects of Si doping in the barriers on the optical properties and recombination dynamics of InGaN/GaN multiple quantum wells (MQWs) has been investigated by means of photoluminescence (PL) and time-resolved PL (TRPL) measurements. The MQW structures were grown on undoped 1.2-μm-thick GaN layers, and capped with undoped 0.1-μm-thick GaN layers. The MQW regions were made up of 5 quantum wells consisting of 2-nm-thick $In_{0.1}Ga_{0.9}N$ wells and 8-nm-thick GaN barriers. Samples labeled N2, N3, and N4 (N1) consisted of Si-doped (undoped) barriers and nominally undoped wells. Si doping concentrations [Si] for samples N2, N3, and N4 were estimated to be about ~ 1×10^{18}, 3×10^{18}, and 1×10^{19} cm^{-3}, respectively. The peak energies and the full width at half maximum (FWHM) values of both the stimulated emission (SE) and spontaneous emission (SPE) increase with increasing Si doping concentration. The blueshift of the PL emission peak with increasing [Si] has been attributed to the decrease of potential fluctuation and/or the screening of piezoelectric field. The increase of the FWHM with increasing [Si] is due to the band filling of localized states at potential fluctuations by carriers originated from Si-doped barriers. The temperature-dependent PL peak energies of undoped (N1) and highly doped (N4) samples continuously redshift with increasing temperature, whereas the PL peak energies of N2 and N3 exhibits S-shaped (redshift-blueshift-redshift) behavior with increasing temperature. The influence of Si doping on the recombination dynamics of the MQWs was investigated using TRPL measurements. As the emission photon energy decreases, the PL decay becomes slower, and hence, the peak energy of the emission shifts to the low energy side as time proceeds. The PL decay profiles of N3 (N1) are well described by a three (two)-exponential function. The PL spectrum consisting of three (or two) Gaussian peaks was interpreted by the results of the PL decay profiles. These PL emission peaks have three (or two) different origins (i.e., different recombination times) of the first (τ_1), the second (τ_2), and the third (τ_3) PL emission. The shapes of the time-delayed PL spectra for N1 and N2 are unchanged during the delay time of 40 ns, whereas the shapes for N3 and N4 are largely changed during the delay time of 60 ns. The redshift with delay time was clearly observed for all samples. The redshift of the emission peak with delay time, and the increase of the emission peak energies and the FWHMs with increasing [Si] are attributed to the band filling of localized states.

4:00 PM

W8, Precise AlGaN Layer Thickness Determination of GaN/AlGaN HEMT Structures by X-ray Diffraction: *Abbas Torabi*[1]; W. E. Hoke[1]; [1]Raytheon RFC, 358 Lowell St., Andover, MA 01810 USA

The promise of high power RF devices in nitride based semiconductors has created enormous interest in these materials in recent years. An impediment to advancement of these devices has been development of an effective epitaxy technique for the nitrides. The lack of high quality epi, smooth interfaces, low defect density, etc, challenges the characterization of the material as well. In this paper we report on the characterization and evaluation of the epitaxial structures grown by MOCVD for RF device applications. Though, x-ray diffraction has successfully been used to evaluate layer thickness and chemical composition in arsenide and phosphide based PHEMT structures, its application to nitride based GaN/AlGaN structures has proved less successful. This is mainly due to rough surfaces and interfaces of the nitride-based structure and presence of high mosacity and high defect density in the epi. In a series of GaN/AlGaN samples grown by MOCVD, we have shown that as the quality of the nitrides epitaxy improves and the surfaces become smoother, Pendellösung oscillations appear in x-ray diffraction profiles and intensity fringes are observed in Grazing Incidence x-ray reflectivity (GIXA) profiles. These intensity oscillations lead to precise layer thickness determination for the critical AlGaN layer in the structure. The results from the x-ray diffraction and GIXA measurements are in very close agreement, indicating the quality of the results. Additionally, we have evaluated the surfaces of these samples by AFM for surface roughness (Ra) determination and presence of step flow condition. A correlation between the AFM roughness value and x-ray data shows that the smoother surfaces are indication of smoother GaN/AlGaN interfaces and hence presence of intensity oscillations in x-ray data. The threshold of surface roughness for observation of intensity oscillation in x-ray diffraction profiles is evaluated to be 5Å as measured by AFM in a 25 mm2 area. The surfaces with higher Ra value do not produce significant fringes in x-ray profile to allow a quantitative thickness evaluation, while the lower Ra value is indicative of smoother interfaces at the GaN/AlGaN channel and hence higher quality epi. In undoped AlGaN/GaN HEMTs the 2-DEG density of the channel depends on the strain in the ternary layer, which is in turn a function of Al mole fraction (the lattice mismatch), and the layer thickness. Thus Al mole fraction and layer thickness determination is of critical importance for these HEMT structures. A GIXA and x-ray diffraction evaluation on relatively smooth interfaces can provide this information. We will discuss our results and show how we have applied this method for uniformity evaluation of layer thickness and composition variation across 2 inch wafers.

4:20 PM, W9, Late News

4:40 PM, W10, Late News

Session X: III-V Nitride Processing and Devices

Thursday PM Room: 155
June 28, 2001 Location: University of Notre Dame

Session Chairs: Charles Eddy, Boston University, ECE Dept., Boston, MA 02215 USA; Steve Stockman, LumiLeds Lighting, Optoelectr. Div., San Jose, CA 95131 USA

1:20 PM (Student)

X1, A Comparison of Sidewall Recombination in Photoelectrochemical and Dry Etched InGaN/GaN Quantum Well Probes: *E. D. Haberer*[1]; A. Stonas[2]; S. DenBaars[1]; E. L. Hu[2]; [1]University of California–Santa Barbara, Matls. Dept., Santa Barbara, CA 93106 USA; [2]University of California–Santa Barbara, Dept. of Electl. & Comp. Eng., Santa Barbara, CA 93106 USA

As GaN material and device technology matures, there is increasing interest in scaling devices to smaller dimensions. In doing so, it is important to consider the effects of air/semiconductor interfaces on device performance. Depending on the nature of the surface states and bond reconstruction, the air/semiconductor interface can be a source of nonradiative recombination. As the surface area to volume ratio increases, as in smaller optical devices, nonradiative sidewall recombination can become an increasingly dominant mechanism of recombination. Furthermore, the etching technique used to form device sidewalls can also impact sidewall recombination. Dry etching processes, commonly used in GaN device fabrication, use low energy ion bombardment to attain the anisotropic etch profiles critical to high resolution device formation. The physical nature of ion bombardment can cause damage to the lattice, increasing sidewall recombination and degradation of device performance. Alternatively, photoelectrochemical (PEC) etching can be used to generate anisotropic profiles in GaN. Because PEC is a photoinduced, electrochemical etching technique, it may be a low damage option for anisotropic etch profiles. We have previously studied the size dependent effects of dry etching on the photoluminescence of the InGaN/GaN system. This study extends the earlier study by exploring smaller feature sizes (< 1 micron) and by comparing the effects of PEC etching to dry etching. In these studies, we used an InGaN/GaN quantum well (QW) probe to evaluate the nonradiative sidewall recombination associated with both PEC etching and dry etching. The structure used in these studies was a graded composition InGaN QW capped with 500 angstroms of GaN grown by MOCVD. Ridges about 1500 angstroms deep, with widths ranging from 0.1-8 microns were etched into the QW structure using both PEC and dry etching. Using the two etching methods, the etching conditions were varied from almost completely chemical (PEC etching) to part physical, part chemical (Ar ion bombardment plus Cl_2 flow) to purely physical (Ar ion bombardment only). In this manner the effects of each component on sidewall recombination could be evaluated and compared. The etched valleys were filled with 2000 angstroms of electron beam deposited Au. Sidewall recombination was quantified by taking room temperature photoluminescence (PL) measurements. A He-Cd laser with a 230 micron spot size was used as an excitation source. The amount of damage was determined by comparing the maximum normalized intensity of the QW peak before and after bombardment and dividing by the fill factor (mesa width divided by pitch). Our studies showed (1) decreased PL intensity remaining with decreasing ridge width and (2) the remaining PL intensity was slightly larger in etches with a chemical component than for etches with only a physical component. We also found that, regardless of the etching technique, the minimum optically active etched feature size or the width at which the PL began to decrease rapidly was much smaller in GaN than observed in other III-V materials.

1:40 PM

X2, Plasma Damage in GaN Schottky Structures-Effect of PA-RIE: *Zoulikha Mouffak*[1]; Nasr-Eddine Medelci-Djezzar[1]; Chris Boney[1]; Abdelhak Bensaoula[1]; Leonard Trombetta[2]; [1]University of Houston–SVEC, Nitride Matls. & Dev. Lab., 4800 Calhoun, Bldg. SR1, Rm. 724, Houston, TX 77204-5507 USA; [2]University of Houston, Electl. Eng., 4800 Calhoun, Houston, TX 77004 USA

Plasma etching using $BCl_3/Cl_2/N_2$ was shown to provide the best results on GaN, yielding highly anisotropic etch profiles and smooth sidewalls. Unfortunately all plasma processes induce surface damage. Studies using inductively coupled plasmas (ICP) showed high damage levels that could be removed by wet etching[1]. While this approach might be adequate for thick devices (i.e. LEDs and some lasers), it is not acceptable in others where removal of a relatively thick layer after plasma etching may not be possible. This issue will become more acute as device geometries shrink and sophisticated heterostructures are employed (i.e. HEMT). Furthermore, wet etching is always a potential source of additional surface contamination. Development of an all-dry etching technique that would induce less damage would be highly desirable. We have previously shown that photo-assisted reactive ion etching (PA-RIE) resulted in improved etch rates and surface composition in comparison with conventional reactive ion etching (RIE)[2]. In this paper, we present the first study of RIE induced damage in GaN using simple Schottky structures and a $BCl_3/Cl_2/N_2$ gas mixture. We also perform a comparative investigation between RIE and PA-RIE. In the case of RIE of p and n-type GaN structures, I-V characteristics at different RF powers and exposure times show significant changes caused by damage. This damage results in a reduction of the barrier height for n-type GaN (and so a reduction in the reverse breakdown voltage V_B) and an enhancement of the barrier height for p type GaN (and so, an increase in V_B). This damage effect saturates at higher RF powers. By contrast, our preliminary data on the PA-RIE process points to much reduced damage levels. This work was supported by funds from NASA cooperative agreement No. NCC8-127 to SVEC, Texas Advanced Technology Program Contract No. 003652-0228-1999, Texas Space Grant Consortium (TSGC), and The Institute for Space Systems Operations (ISSO). [1]X. A. Cao, S. J. Pearton, G. T. Dang, A. P. Zhang, F. Ren, and J. M. Van Hove, IEEE Transactions on Electronic Devices 47(7), 1320 (2000); [2]A. Tempez, N. Medelci, N. Badi, D. Starikov, and A. Bensaoula, J. Vac. Sci. Technol. A 17(4), 2209 (1999).

2:00 PM

X3, Surface Passivation of GaN/AlGaN Heterostructure Using ECR-CVD SiNx Film and Ultrathin Al_2O_3 Layer: *Tamotsu Hashizume*[1]; Shinya Ootomo[1]; Susumu Oyama[1]; [1]Hokkaido University, Rsrch. Ctr. for Interface Quantum Elect., N-13, W-8, Sapporo, Hokkaido 060-8628 Japan

GaN and related heterostructures are now well established as materials for the production of high-power/high-frequency devices such as high-electron mobility transistors (HEMTs). However, several key problems related to surfaces and interfaces impede the realization of reliable device performance, namely a significant frequency-dependent collapse or the so-called "DC-to-RF dispersion" in drain current and poor Schottky gate properties, especially large leakage current for GaN/AlGaN HEMT devices. Thus, understanding and controlling surface properties of GaN-based heterostructures are of utmost importance for the reliable device performance. In this paper, we demonstrate successful surface passivation and interface control processes for GaN/AlGaN heterostructure on the basis of a systematic investigation on chemical and electrical properties of surfaces and interfaces. Si-doped n-GaN layers and GaN/$Al_{0.25}Ga_{0.75}N$ heterostructures grown on sapphire substrates by MOVPE were used. In order to control the surface, a combination of wet and ECR plasma treatments was applied to the surfaces. Final surface passivation was performed by the deposition of thick SiNx film on the sample surface at 280°C by ECR-CVD. In order to improve Schottky gate properties on the GaN/AlGaN HEMT structure, in addition, a novel interface control approach was attempted. The basic idea is to insert an ultrathin Al_2O_3 layer between the AlGaN surface and Schottky metals. The process started from the formation of ultrathin (1 nm) Al layer on the NH_4OH-treated GaN/AlGaN surface at RT using a K-cell in the MBE chamber. Then the sample was annealed at 700°C for 10 min in an UHV environment (base pressure: $2x\ 10^{-10}$ Torr). During the annealing, the surface natural oxide of AlGaN can be converted to the Al oxide (Al_2O_3) through the reduction process by highly reactive metallic Al driven by the large heat of forma-

tion of Al_2O_3. Surface properties were investigated at each processing step by XPS, Raman, AFM, I-V and C-V methods. Detailed XPS and AES analyses revealed the formation of near oxide-free and stoichiometric GaN and AlGaN surfaces after the treatments in the NH_4OH solution and in the ECR N_2 plasma. This resulted in the reduction of Fermi level pinning. The ECR-CVD SiNx/n-GaN passivation structure prepared after these surface treatments showed good C-V characteristics. A minimum Dit value of 1x 10^{11} $cm^{-2}eV^{-1}$ or less was realized. This SiNx-based passivation process was found to enhance the drain current and to suppress the drift of drain current in the GaN/AlGaN HEMT. In situ XPS analysis confirmed that the formation of the novel AlGaN/ultrathin Al_2O_3/Au Schottky gate structure, resulting in more than two orders reduction of gate leakage current for the GaN/AlGaN HEMT device.

2:20 PM

X4, Effects of High Density Plasma Etching on Contacts to GaN and $Al_xGa_{1-x}N$: *Rajwinder Singh*[1]; Adrian W. Williams[1]; Charles R. Eddy[1]; Theodore D. Moustakas[1]; Hock M. Ng[2]; [1]Boston University, Electl. & Comp. Eng., 8 St. Mary's St., Boston, MA 02215 USA; [2]Lucent Technologies, Bell Labs., Murray Hill, NJ, USA

High density plasma etching is a leading candidate for creating device structures in III-Nitride semiconductors. Film and contact quality degradation due to plasma damage during etch processing are important concerns in the quest for practical devices. Examples of devices where plasma damage concerns are paramount include vertical conduction GaN devices and GaN/AlGaN HFETs with recessed drain and source contact structures. In this paper, the results of studies on electrical quality of Ti/Al/Au contacts to n-GaN, n-$Al_{0.1}Ga_{0.9}N$ and $Al_{0.2}Ga_{0.8}N$ are reported. The plasma damage is carried out over a range of rf bias energies in a chlorine chemistry. The as-deposited films are found to have poor ohmicity and contact resistivity for all material compositions studied. Rapid thermal annealing at 700°C significantly improves the resistivity as well as the ohmicity of the contacts. In all GaN and AlGaN films studied in our investigations, contact resistivity shows a rapid improvement in the first 30 seconds. Subsequent annealing for longer intervals results in negligible further improvement in contacts to GaN films and a steady reduction in contact resistivity in the case of AlGaN films. Results of efforts to improve contact quality using in-situ and ex-situ treatments are reported.

2:40 PM (Student)

X5, Effect of a MBE Grown AlN Surface Layer on the DC and RF: *Jeonghyun Hwang*[1]; William J. Schaff[1]; Bruce Green[1]; [1]Cornell University, Electl. & Comp. Eng., 429 Phillips Hall, Ithaca, NY 14853 USA

Heterojunction Field Effect Transistors (HFET)s made from GaN are useful for application to high power microwave amplifiers. While large channel currents and high breakdown voltages are seen for 2 dimensional electron gas (2DEG) HFETs, these large DC channel currents are often not obtained as peak channel currents under RF modulation. It has been shown previously that application of surface layers of Si3N4 permit higher peak channel currents at microwave frequencies. As an alternative to Si3N4, AlN as a surface layer for GaN heterojunction field effect transistors (HFET)s is studied. MBE has been used to grow AlN over a wide temperature range, and is applied at 150°C in this study. The deposition follows all other transistor processing steps. This deposition uses alternating beams of Al and remote plasma RF nitrogen to produce a 500Å thick AlN layer. This technique is an approximation of migration enhanced epitaxy (MEE), although the substrate temperature here is presumed to be too low for growing single crystal AlN. MEE was chosen as an alternative to MBE, since MEE can be used to grow high quality materials, such as GaAs, at lower substrate temperatures than MBE. The low temperature requirement of the existing device structures makes MEE possibly more attractive. MEE also might give better sidewall coverage, especially along the side of the gate. GaN HFET with 0.3x100µm T-shaped gates is fabricated using devices from one an MBE grown epitaxial layer. This wafer has a 300K Hall mobility of 1450 cm2/Vsec and electron sheet density of 1.1x1013 cm-2. Comparisons between transistors before and after AlN deposition are made. Addition of AlN surface layer produces almost 3dB increase in the 8 GHz output power of HFETs. RF output current increases from 400mA/mm to 800mA/mm. The AlN layer changes properties of the surface which would otherwise limit high frequency channel current. These results are similar to those obtained for Si3N4 surface layers reported elsewhere. Comparison of device properties such as ft, breakdown voltages, and gate leakage current before and after AlN deposition will also be given.

3:00 PM Break

3:20 PM

X6, Fabrication and DC Characteristics of Various Al-Content MOCVD Grown AlGaN/GaN HEMTs on Sapphire Substrate: *S. Arulkumaran*[1]; T. Egawa[1]; G. Zhao[1]; H. Ishikawa[1]; M. Umeno[1]; [1]Nagoya Institute of Technology, Rsrch. Ctr. for Micro-Struct. Dev., Gokiso-cho, Showa-ku, Nagoya, Aichi 466-8555 Japan

Heterostructures of AlxGa1-xN/GaN were grown on sapphire substrate by MOCVD with a good uniformity and a product of sheet carrier density and mobility of 9.81x1015/Vs, 1.17x1016/Vs and 1.32x1016/Vs for the Al composition 19%, 26% and 33%, respectively. Various gate length high electron mobility transistors (HEMTs) with 15 and 200 micron wide gate have been fabricated and characterised. The increase of extrinsic transconductance of the fabricated HEMTs has been observed with the increase of heterostructure Al-content. The AlxGa1-xN/GaN layers were grown by atmospheric pressure MOCVD on (0001)-oriented sapphire substrates using the following growth conditions. The device structure consists of 3 nm un-doped AlGaN barrier layer, 15 nm silicon doped AlGaN supply layer, 7 nm un-doped AlGaN spacer layer, 3000 nm insulating GaN (i-GaN) layer and a 30 nm i-GaN buffer on top of the sapphire substrate. The device isolation was accomplished by mesa dry etching down to the i-GaN by BCl3 plasma reactive ion etching. The ohmic contact was performed by the deposition of a Ti/Al/Ti/Au (25/100/45/55 nm), which was subsequently alloyed at 760°C for 60 sec in N2 atmosphere. The gate metals Pd/Ti/Au (40/40/80 nm) were performed using optical lithography through conventional lift-off method. Before loading the sample for evaporation of gate and ohmic metals, the samples were etched in conc. HCl solution for 60 sec to remove the native oxide on the surface of the sample. The DC characteristics were measured in dark using HP4145B semiconductor analyser. To measure the 2° channel depth, C-V measurements were carried out using HP4845A LCR Bridge. Good I-V characteristics of 1.8 micron gate length and 15 micron gate width HEMTs, yielding a maximum transconductance of 159, 166 and 204 mS/mm with maximum drain current density of 536, 429 and 687 mA/mm for 19%, 26% and 33% of Al-content AlGaN/GaN structures, respectively. The measured contact resistance from transmission line structure are 1.48, 2.06 and 2.0 Ohm-mm for 19%, 26% and 33% of Al-content heterostructures, respectively. The high value of contact resistance leads to the low drain current density for 26% AlGaN/GaN structures compared with the 19% AlGaN/GaN structures. The source resistance has also been measured for these HEMTs structures. Source resistance values are high for less gate width devices. The dependence of transconductance with gate length and also with gate offset from source will be discussed in detail. In summary, we have demonstrated the different Al-content AlxGa1-xN/GaN based various gate length HEMTs with good I-V characteristics grown on sapphire substrates. The increase of transconductance was observed with the increase of Al-content of AlGaN/GaN heterostructures. From this we realise that, high Al-content AlGaN/GaN heterostructures are suitable for high power and high frequency device applications.

3:40 PM (Student)

X7, GaN and AlGaN High-Voltage Rectifiers Grown by Metalorganic Chemical Vapor Deposition: *Ting Gang Zhu*[1]; Uttiya Chowdhury[1]; Michael M. Wong[1]; Ki Soo Kim[1]; Jonathan C. Denyszyn[1]; Russell D. Dupuis[1]; [1]The University of Texas at Austin, Microelect. Rsrch. Ctr., 10100 Burnet Rd., Bldg. 160, Austin, TX 78758 USA

The unique material properties of III-N based semiconductors make them potentially important for high-power and high-temperature electronic devices. Schottky barrier diodes and p-i-n rectifiers are the primary devices for demonstrating the high-power handling capability of semiconductor materials. Additionally, the p-i-n diode constitutes the basic building block of the base-collector-subcollector junctions of the HBT structure; thus a study of these devices will potentially help to understand more complex devices, e.g., HBTs, in other high-power applications. We report the study of the electrical characteristics of AlGaN and GaN vertical p-i-n junctions and Schottky rectifiers grown by metalorganic chemical vapor deposition (MOCVD). The device structures are grown in an EMCORE D125 UTM MOCVD system at pressures of ~100 Torr and temperatures in the range 1030°C < T_g < 1100°C. Hydrogen is main process gas and the carrier gas for the metal alkyl sources. Ammonia is used as the N source and adduct-purified

trimethylgallium (TMGa) and trimethylaluminium (TMAl) are used as Column III precursors, with a V/III ratio of ~2,500-5,000. GaN p-i-n rectifier devices are often grown on insulating sapphire substrates, so the device contacts are made from the top of the wafer; thus etching of the device structure is indispensable. We have employed reactive-ion etching (RIE), inductively coupled plasma etching (ICP), chemically-assisted ion-beam etching (CAIBE), and photoelectrochemical etching (PEC) for etching the mesa structure. Comparison of different processing techniques and their effect on device performance will be discussed. We have also grown such rectifier devices on 6H-SiC substrates and the performance is somewhat improved. We have studied the forward on-resistance, reverse leakage currents, and breakdown voltages in different rectifier structures. For example, a p-GaN/i-$Al_{0.20}Ga_{0.80}N$/n-$Al_{0.20}Ga_{0.80}N$ diode with a thin "i" region of ~1.5µm exhibits a blocking voltage in excess of ~350V at a reverse leakage current density below 1A/cm^2. The forward voltage drop is ~10V at a current density of 100A/cm^2. The corresponding breakdown electric field strength of ~4.6 MV/cm is the highest reported to date for an AlGaN p-i-n mesa device. We have also studied the effect of varying the Al alloy composition on the AlGaN rectifier characteristics by fabricating $Al_xGa_{1-x}N$ p-i-ns with $0<x<0.45$. GaN p-i-n rectifiers with a relatively thin "i" region of 2µm exhibits a breakdown voltage over 400V and forward voltage as low as 6V at 100A/cm^2 for a 60µm-dia. vertical-geometry device. This breakdown is presently limited by the failure of the contact at the mesa edges. These results indicate the great potential for GaN-based devices in high-voltage applications. Additionally, we describe our studies of the use of Mg ion implantation for p-guard rings as planar edge terminations in mesa-geometry GaN Schottky rectifiers to improve the reverse-bias device performance. We will also compare the performance of devices grown on sapphire and SiC substrates.

4:00 PM

X8, Responsivity Spectra of GaN Based Schottky Barrier UV Detectors Using Synchrotron Radiation: *Atsushi Motogaito*[1]; Motoo Yamaguchi[1]; Keiichi Ohta[1]; Kazumasa Hiramatsu[1]; Youichiro Ohuchi[2]; Kazuyuki Tadatomo[2]; Yutaka Hamamura[3]; Kazutoshi Fukui[4]; [1]Mie University, Dept. of Electl. & Elect. Eng., 1515 Kamihama, Tsu, Mie 514-8507 Japan; [2]Mitsubishi Cable Industries, Ltd., Photonics Rsrch. Lab., 4-3 Ikejiri, Itami, Hyogo 664-0027 Japan; [3]Nikon Corporation, Precision Equip. Co., 1-10-1 Asamizodai, Sagamihara, Kanagawa 228-0828 Japan; [4]Institute for Molecular Science, Dept. of Vac. UV Photosci., Myodaiji, Okazaki, Aichi 444-8585 Japan

Ultraviolet (UV) detectors are one of the most attractive devices in the group III-nitride semiconductors. Recently, Si-based photodetectors are mainly used for the measurement of UV light. However, light sensitivity often deteriorates due to radiation damage in the vacuum ultraviolet (VUV) region (6-30 eV). Several groups have reported on GaN or AlGaN based UV detectors. They have responsivity from 250 to 360 nm (3.4-5.0 eV) and clear cut-off characteristics at a cut-off wavelength (360 nm), however there are no reports of responsivity spectra in the VUV region. Synchrotron radiation (SR) is a powerful light source of X-ray region and is also the useful light source of VUV-infrared region because of its wide wavelength continuity. It gives us the chances not only to investigate the electronic and optical structures but also to characterize the responsivity spectra of UV detectors in wide wavelength region. In this paper, we describe the responsivity spectra of Schottky type UV detectors between VUV and visible light region (41-563 nm, 2-30 eV) using SR at UVSOR BL7B in Institute of Molecular Science, Japan. The UV detectors used in this study adopt the Schottky contacts with a comb-shaped electrode. The advantages of this structure are (1) the absorption depth of UV light is so shallow that the light is absorbed near the surface of i-GaN and (2) the damage of the interface between Schottky metal and i-GaN is suppressed because the UV light is absorbed only at the surface of the window region. They consist of a 3.0 µm thick n-GaN layer and a 2.5 µm thick i-GaN layer which are grown on a (0001) sapphire substrate by MOVPE. The Au/Ni Schottky contact was fabricated on i-GaN with a comb-shaped electrode composed of 2-µm-electrodes and 2-µm-windows. The diameter of the detector was 6.5 mm. The responsivity spectra of the detectors were obtained in the wide range between 2 eV (563 nm) and 30 eV (41 nm). It was also found that the photoemission from the surface of Au and GaN occurs at higher than 8.0 and 9.5 eV (≤155 and ≤130 nm), respectively. We were able to cancel the photoemission current from Au by improving the measuring circuit, and thus we succeeded in operating the detectors without any photoemission current from Au less than 9.5 eV (≥130 nm). However, the photoemission current from the GaN surface was included in the diode current more than 9.5eV. These results show that these Schottky type detectors with the comb-shaped electrode are effective to detect VUV-UV light (130-360 nm, 3.4-9.5 eV).

4:20 PM

X9, Device Characteristics of a Pt-Ga2O3(Gd2O3)-GaN Capacitor: *T. S. Lay*[1]; W. D. Liu[1]; M. Hong[2]; J. Kwo[2]; J. P. Mannaerts[2]; W. H. Hung[3]; D. J. Huang[3]; [1]National Sun Yat-Sen University, Inst. of Electro-Optl. Eng., Kaohsiung 804 Taiwan; [2]Lucent Technologies, Bell Labs., Murray Hill, NJ 07974 USA; [3]Synchrotron Radiation Research Center, Hsinchu, Taiwan

We have investigated the device parameters of a Pt-Ga2O3(Gd2O3)-GaN capacitor by using high-frequency C-V measurement and soft x-ray photoelectron spectroscopy (XPS). The 18 nm-thick Ga2O3(Gd2O3) film was deposited on a n-type GaN wafer by e-beam evaporation in an UHV chamber. The C-V and G-V curves of the capacitor were measured at modulation frequencies of 1MHz, 100KHz, and 10KHz. The actual C-V characteristics have been corrected from the measured C-V and G-V data at different high frequencies by considering the leakage current through the oxide film. From the corrected C-V data, we obtain the Ga2O3(Gd2O3) dielectric constant ~ 14, and the interface density of states (Dit) ~4x10^11 cm^-2eV^-1 near midgap. The energy band discontinuities at the Ga2O3(Gd2O3)-GaN interface were determined by XPS of photon energy = 175 eV. We have measured the energy levels of the Fermi edge and the Ga2O3(Gd2O3) valence band edge. From the data, the conduction-band offset ~ 0.9 eV and the valence-band offset ~1.1 eV were deduced for the Ga2O3(Gd2O3)-GaN interface.

4:40 PM, X10, Late News

Session Y: Heteroepitaxy on Si

Friday AM, June 29, 2001 — Room: 129, Location: University of Notre Dame

Session Chairs: Robert Sacks, Picometrix, Ann Arbor, MI 48105 USA; Ralph Dawson, The University of New Mexico, Ctr. for High Tech. Matls., Albuquerque, NM 87106 USA

8:20 AM

Y1, Growth of InP and InP-Based InGaAsP Heterostructures on Silicon Substrates by Solid-Source Molecular Beam Epitaxy: *Clifton G. Fonstad*[1]; K. Henry Choy[1]; P. Aitor Postigo[2]; [1]Massachusetts Institute of Technology, Dept. of Electl. Eng. & Comp. Sci., 77 Massachusetts Ave., Rm. 13-3050, Cambridge, MA 02319 USA; [2]Centro Nacional de Microelectronica, Inst. de Microelect. de Madrid, Isaac Newton 8, Parque Technologigo de Madrid, Tres Cantos, Madrid 28760 Spain

We report the first growth of InP and InP-based heterostructures on Si by conventional molecular beam epitaxy. Prior reports employed MOCVD, and found the best results using substrates misoriented from the (100) direction by 2 or 3 degrees, and using a thin intermediate layer of GaAs. In the present work it has been found that layers with characteristics comparable to, or better than, those reported for MOCVD layers can be obtained with MBE using direct growth on (100)-oriented Si. The present work represents the initial stages of a program to grow InP-based heterostructures on silicon membranes to address thermal expansion coefficient differences that have stymied epitaxy of III-V heterostructures on Si. We know using etch-release layers between GaAs structures and Si yields strain-free AlGaAs devices on Si. This technique, and the new silicon membrane approach (using recent advances in SOI and MEMS technology) are being pursued for InP. Our initial observations there will also be presented. A conventional solid-source MBE system with a GaP sublimation source was used. Surface oxide was removed prior to growth

by atomic hydrogen with the substrate at 630°C, yielding a strong 2x2 RHEED reconstruction. Obtaining a good growth, and shiny, featureless surface, requires growing the first 100 nm at a slow rate (0.2 μm/hr) with the following conditions: 1) High V-to III-flux ratio: When initiating growth on Si, the phosphorous flux is 4 times higher than that used to grow InP on InP. This contrasts with the growth of GaAs on Si and InAs on GaAs by MBE, but it correlates well with observations on the MOCVD growth of InP on Si. Significantly, unlike the situation with MOCVD, a high P2 flux at a reasonable growth rate can be readily achieved using a GaP sublimation cell. 2) Substrate temperature 100 to 150 degrees lower than used when growing on InP: This result also correlates well with earlier findings with MOCVD. 3) Atomic hydrogen flux: A similar benefit has been reported for growths assisted by atomic hydrogen in other heteroepitaxial systems. After this initial period, growth can proceed using parameters identical to those used when growing on InP substrates. The FWHM of X-ray peaks measured on the InP-on-Si epilayers was 300 arc second. The photoluminescence spectrum measured on a series of InGaAs/InP quantum wells grown on silicon, showed line widths similar those of InP grown on InP, but the intensity was a factor of 30 lower. These results are comparable to the best results for MOCVD growths on Si, but the film thicknesses in the present work are much smaller those in the MOCVD work; significantly better results can be anticipated from thicker films and with the application the above-mentioned etch-release and Si membrane techniques.

8:40 AM

Y2, Molecular Beam Epitaxy of CaF_2 on Si(111): Cunrang Wang[1]; Bernhard H. Müller[1]; *Karl R. Hofmann*[1]; [1]University of Hannover, Inst. of Semicond. Dev. & Elect. Matls., Appelstr. 11A, Hannover 30167 Germany

Epitaxialy grown CaF_2 insulators are highly attractive for Si-based quantum devices. But these applications require flat defect-free ultra-thin films, preferably grown at low temperature for the compatibility with other processes. The lattice mismatch between Si and CaF_2 is only 0.6% at room temperature and the crystal structures are compatible. Furthermore the surface free energy of CaF_2(111) is much smaller than that Si(111), so wetting of CaF_2 on Si(111) can be expected allowing the growth of flat, high-quality films. However, the existence of a chemically reacted interface layer makes the growth mechanism complicated. The common opinion is that flat films can only be grown at temperatures around 700°C. In this work the MBE growth of epitaxial CaF_2 layers with a film thickness from 3 to 5nm on Si(111) substrates has been studied in the temperature range between 370°C and 690°C, with growth rates of about 0.1nm/min. The surface morphology was determined by ex-situ atomic force microscopy (AFM) in addition to reflection high-energy electron diffraction (RHEED) measurements during growth. A strong temperature dependence of the CaF_2 surface morphology with four different growth regimes was found. At temperatures below 420°C, the most striking feature is the formation of large CaF_2 clusters. Between them triangular shaped islands with two distinct orientations are visible, revealing their cystallographic orientations (A- and B- stacking). In the temperature region between 430°C and 470°C, the CaF_2 epilayers surface is very smooth, exhibiting a nearly perfect layer-by-layer growth mode. RHEED measurements showed that at this temperature the first two monolayers of CaF_2 grow as one double layer, giving insight into the growth mechanism at the Si-CaF_2 interface. The transition to the low temperature region is very narrow, about 30°C. Again the islands are anisotropic and reveal a B-stacking of the complete film. Surprisingly, above 520°C, the surface is becoming rough again. The average island size is reduced and more condensation on islands and at or near the substrate steps occurs. In the same time the islands change to a more round, isotropic shape. Obviously the probability of the CaF_2 admolecules to jump down from the islands decreases. The authors attribute this effect to a higher average Schwoebel barrier for round islands as compared to the triangular islands in the low temperature region. RHEED observations at 650°C demonstrate that in this region the initial growth mode is different compared to the 450°C case. The first layer of CaF is completed before the second starts to grow. Further increase of the temperature to 690°C again leads to larger isotropic islands and smoother surfaces. In conclusion, a growth temperature between 430°C and 470°C seems to be best to obtain atomically flat, pinhole free thin CaF_2 films on Si(111).

9:00 AM (Student)

Y3, Epitaxial Growth of BeZnSe on CaF_2/Si(111) Substrate: *Takeo Maruyama*[1]; Naoto Nakamura[1]; Masahiro Watanabe[1]; [1]Tokyo Institute of Technology, Rsrch. Ctr. for Quantum Effect Elect., 2-12-1 O-okayama, Meguro-ku, Tokyo 152-8552 Japan

Be-chalcogenides II-VI semiconductors is good candidate for the materials of long life-time II-VI lasers because of the strong covalent bonding of Be. Moreover, BeMgZnSe quaternary compound semiconductor can be lattice matched to silicon (Si) and its energy band gap covers ultraviolet (UV) region (290-345nm). From this point, we have proposed UV lasers on Si substrate using BeZnSe/BeMgZnSe/BeMgSe quantum-well. This material system has potential of heterostructure for band engineering on silicon substrate. In the growth of BeMgZnSe on Si substrate, it is problematic that amorphous $SiSe_x$ layer is formed at interface[1] because of intermixing between Se and Si, which prevent the growth of high quality epitaxial BeMgZnSe layers. In order to avoid reaction between Si and Se, we introduce CaF_2 interlayer epitaxially grown on Si substrate. In this paper, we report epitaxial growth of BeZnSe on Si(111) substrate using CaF_2(111) epitaxial interlayer. CaF_2 has fluorite lattice structure and mismatch with Si is +0.6% at room temperature. It is known that atomically flat CaF_2 layer can be grown epitaxially on Si(111) using molecular beam epitaxy (MBE) based technique. Si(111) substrate was chemically cleaned and protective oxide layer was grown. After loaded into ultra-high vacuum chamber, protective oxide was removed at 700°C with Si flux, which leads atomically clean 7x7 surface. CaF_2 interlayer was grown on Si using partially ionized beam epitaxy (PIBE) method[2] at temperature of 600°C and thickness of 10nm, which leads atomically flat CaF_2 layer because ionization of CaF_2 enhance formation of Si-Ca bonding at heterointerface. After the growth of CaF_2, $Be_xZn_{1-x}Se$ (x=0.2-1.0) was grown by MBE at growth temperature of 300°C, thickness of 200 nm and growth rate of 2 nm/min. In-situ reflection high energy electron diffraction (RHEED) pattern indicated that epitaxial BeZnSe layer was obtained on the CaF_2 interlayer. Lattice constant of the obtained layer was evaluated by X-ray diffraction (XRD). (111) peaks of XRD results confirmed that the BeZnSe is lattice matched to Si when x=0.45, which is consistent with Vegard's law. Surface morphology was studied using atomic force microscope. [1]J. P. Faurie, V. Bousquet, P. Brunet and E. Tournie: J. Cryst. Growth, vol. 184/185, pp. 11-15, 1998; [2]M. Watanabe, Y. Iketani, M. Asada: Jpn. J. Appl. Phys., vol. 39, pp. L964-L967, 2000.

9:20 AM

Y4, Selective Growth of CdF2/CaF2 Resonant Tunneling Diode Nanostructure on Si: *Masahiro Watanabe*[1]; Naoto Sakamaki[1]; Tatsuya Ishikawa[1]; Daisuke Okamoto[1]; [1]Tokyo Institute of Technology, Rsrch. Ctr. for Quantum Effect Elect., 2-12-1 O-okayama, Meguro-ku, Tokyo 152-8552 Japan

CdF_2/CaF_2 heterostructure is an attractive candidate for quantum devices on Si substrate such as resonant tunneling diodes and quantum intersubband transition devices because of its large conduction band discontinuity (ΔE_C=2.9eV) at the heterointerface. Due to the large ΔE_C and wide band gap energy of CdF_2 (E_g=8eV) and CaF_2 (E_g=12eV), resonant tunneling diodes (RTD) using CdF_2/CaF_2 heterostructures are expected to show negative differential resistance (NDR) characteristics with extremely large peak to valley ratio (PVR) because of the small valley current even at room temperature. CdF_2 and CaF_2 have fluorite lattice structure and well lattice matched to Si with mismatches of -0.8%, +0.6% at room temperature, respectively. Recently, we have reported high peak-to-valley current ratio of double barrier CdF_2/CaF_2 RTD grown on Si(111) substrate [1] using molecular beam epitaxy (MBE) and partially ionized beam epitaxy (PIBE). In this paper, we propose novel fabrication technique of CdF_2/CaF_2 RTD using selective growth in sub-micrometer size patterned area formed by electron beam lithography, which dramatically enhances uniformity and stability of the device performance. N-type Si(111) substrate with 0.1° miscutt was chemically cleaned and 15 nm-thick SiO_2 layer was formed by dry oxidation. Subsequently, SiO_2 holes of 100-400 nm-diameter with 500 nm intervals were formed by electron beam lithography and wet chemical etching. Silicon surface at the bottom of the holes were wet oxidized again for protection. After loaded into the ultra-high vacuum chamber, the protective oxide layer was removed by thermal heating with Si flux. Firstly, 1nm-thick CaF_2 was grown at 750°C, with ionization by electron bombardment without acceleration. Using the selective growth technique, pinhole or defect density in CaF_2 island can be suppressed when the size of selective area is smaller

than critical diameter of CaF_2 island. On the first CaF_2 barrier layer, 6.5 nm-thick CdF_2 quantum well layer was grown at 50°C. After the growth, the top 1 nm-thick CaF_2 barrier layer was grown at 50°C with ionization and acceleration. Au/Al electrode of 100 µm-square was evaporated on the array of selectively grown double barrier RTDs. In the measurement of current-voltage characteristics, clear room temperature NDR was observed. Moreover, stability, uniformity of I-V characteristics were significantly improved for the sample with selective area smaller than 200 micro meters diameter. Selective area size dependence and growth temperature dependence of NDR characteristics will be also discussed. [1]M. Watanabe, T. Funayama, T. Teraji, N. Sakamaki, Jpn. J. Appl. Phys., 39 [7B] (2000) L716.

9:40 AM, Y5, Late News

Session Z: Erbium Doping and Ordering

Friday AM Room: Room 129
June 29, 2001 Location: University of Notre Dame

Session Chairs: Robert Sacks, Picometrix, Ann Arbor, MI 48105 USA; Ralph Dawson, University of New Mexico, Ctr. for High Tech. Matls., Albuquerque, NM 87106 USA

10:20 AM

Z1, Erbium Doping in GaP and GaNP Grown by MOMBE: *Ikuo Suemune*[1]; Hidekazu Kumano[1]; Togo Shimozawa[1]; Ktsuhiro Uesugi[1]; [1]Hokkaido University, Rsrch. Inst. for Elect. Sci., Kita-12, Nishi-6, Sapporo 060-0812 Japan

With the development of the wavelength division multiplexing (WDM) in optical-fiber communication systems, demand for the temperature-stabilized semiconductor laser sources is being expanded. Erbium (Er)-doped semiconductors are known to emit ~1.54mm luminescence originated from the Er3+ 4f-4f transitions and are well matched to Er-doped fiber amplifiers. Although Er-doped GaAs and InP have been extensively studied, they showed limited luminescence efficiency[1,2]. On the other hand, high luminescence efficiency has been reported with Er-doped GaP light emitting diodes (LED) at room temperature[3]. This suggests that wide bandgap semiconductors are preferable to prevent Auger recombinations[4]. Codoping with oxygen or nitrogen (N) has been also studied in Si-based semiconductors and is reported to improve the luminescence efficiency[5]. Concerning the N doping in compound semiconductors, the improvement of the luminescence efficiency with the increase of the N composition was reported in polycrystalline GaNAs films doped with Er[6]. In this paper, Er doping is studied in a wide bandgap GaP and GaNP and the codoping effect of Er and N in GaP was studied. Nitrogen composition up to 2% was observed in GaNP grown by metalorganic molecular-beam epitaxy (MOMBE). Observation of bright but broad Infra-red (IR) luminescence will be reported with Er doping in GaNP. The sharp luminescence specific to the 4f-4f transitions was only observed with Er doping in GaP. The GaNP films were grown on S-doped (001) GaP substrates with MOMBE at 570°C. The precursors used are triethylgallium (TEGa), trisdimethylamino-phosphorous (TDMAP), and monomethylhydrazine (MMHy) and are supplied on the growth surface without thermal cracking. Solid Er was evaporated using a Kneudsen cell. The N composition was evaluated with symmetric and asymmetric X-ray diffraction (XRD) measurements[7]. The maximum Er concentration in this work is estimated to be ~0.5% with the highest Er-cell temperature of 1020°C. The visible luminescence near the absorption edge was not much influenced by the Er doping except for the slight red shift or splitting of the LO phonon replica. IR luminescence was observed both from the Er-doped and undoped GaNP films. The IR spectra were broad ranging from 1.2~1.5 mm, and usually observed sharp peaks at ~1.54mm due to the Er3+ 4f-4f transition was observed from Er doping in GaP. The details of the codoping effect of Er and N will be discussed during the conference. References: [1]H. Ennen et al, Appl. Phys. Lett., 43, 10 (1983) 943; [2]K. Uwai et al, Appl. Phys. Lett. 51, 13 (1987) 1010; [3]G. M. Ford et al, Appl. Phys. Lett., 68,8 (1996) 1126; [4]Jung H. Shin et al, Appl. Phys. Lett. 76, 24 (2000) 3567; [5]A. Taguchi et al, J. Appl. Phys. 83 (1998) 2800; [6]A. R. Zanatta, Appl. Phys. Lett. 75, 21 (1999) 3279; [7]K. Uesugi et al, Appl. Phys. Lett. 74, 9 (1999) 1254.

10:40 AM (Student)

Z2, Optimum Er Concentration for In-Situ Doped GaN Visible and IR Luminescence: *Dong-Seon Lee*[1]; J. Heikenfeld[1]; M. Garter[1]; A. J. Steckl[1]; U. Hommerich[2]; J. T. Seo[2]; A. Braud[2]; J. Zavada[3]; [1]University of Cincinnati, Nanoelect. Lab., Cincinnati, OH 45221-0030 USA; [2]Hampton University, Dept. of Phys., Rsrch. Ctr. for Optl. Phys., Hampton, VA 23668 USA; [3]US Army European Research Office, London, UK

We have previously reported the first visible green emission[1] from Er-doped GaN thin films using molecular beam epitaxy (MBE). We have observed, as expected, that the visible emission, both from photoluminescence (PL) and from electroluminescence (EL) is a strong function of Er concentration. In this paper, we report on the effect of Er concentration on PL and EL intensity and on the determination of an optimum Er doping level. Er was in-situ doped into GaN over a wide range of concentration, 0.01-10 atomic %. GaN:Er films were grown at 700°C on p-type (111) Si substrate by MBE with a Ga elemental source and a nitrogen plasma source. Er was introduced in-situ during growth from a solid source. Er concentration was adjusted by control of Er cell temperature from 740°C to 980°C. Both secondary ion mass spectroscopy (SIMS) and Rutherford back scattering (RBS) measurements showed that Er concentration in GaN increased exponentially with Er cell temperature. No saturation phenomenon in concentration was observed up to 10 at.% of Er. Photoluminescence (PL) intensity of green emission at 537nm, which is a characteristic visible emission line due to Er 4f-4f inner shell transition, was highly dependent upon Er concentration. PL increased with Er concentration, exhibited a maximum at ~1 at.% of Er, then decreased with additional Er incorporation. The same optimum Er concentration was observed in EL intensity measurements. PL lifetime measurements at 537 nm showed that samples with conce ntration < 1 at.% had a lifetime of ~5 µs. For Er concentration > 1 at.%, the lifetime decreased rapidly to values below 1 µs. This clearly indicates that concentration quenching effect starts at ~ 1 at.% of Er in GaN. PL intensity of 1.54 µm emission, another characteristic emission from Er, showed the same behavior as that of green emission. Decrease of PL and EL intensity at higher Er concentration is believed to be initially due to Er cross-relaxation process, eventually followed by segregation or precipitation. A similar indication was provided by X-ray diffraction (XRD) measurements. XRD results showed that Er incorporation above 1 at.% rapidly reduced the crystalline quality of GaN host in terms of intensity of the (0002) peak and its full width half maximum (FWHM). In summary, we have determined that the optimum Er doping concentration into GaN is ~1 at.%. [1]A. J. Steckl and R. Birkhahn, Appl. Phys. Lett. 73 (12), 1700 (1998).

11:00 AM (Student)

Z3, Flat Panel Display Material Issues and Options for Rare Earth-Doped GaN Electroluminescent Phosphors: *Jason C. Heikenfeld*[1]; Andrew J. Steckl[1]; [1]University of Cincinnati, Nanoelect. Lab., Cincinnati, OH 45221-0030 USA

Rare earth (RE)-doped GaN phosphors[1] have several qualities which are ideal for alternating current electroluminescent display devices (AC-ELDs). Preliminary GaN:RE AC-ELDs have exhibited brightness values of ~40 cd/m^2, full-color capability, and operation lifetimes of >1000 hrs. Many structural, optical, and electrical materials issues for GaN-based AC-ELDs differ from commercial ZnS- and oxide-based AC-ELDs. We will present the flat panel display material issues and options for GaN:RE electroluminescent phosphors. A conventional AC-ELD device generally uses a structure consisting of the following layers metal/dielectric/phosphor/dielectric/indium-tin oxide/glass substrate. One of the most attractive qualities of GaN-based phosphors for AC-ELDs is chemical and thermal stability. GaN-based phosphors, which have a low reactivity and diffusivity, are less susceptible to moisture and other environmental degradation factors that cause rapid aging in commercial ZnS-based phosphors. The GaN:RE phosphor exhibits an optical turn-on voltage (<100 V) which is significantly less than that of other chemically stable phosphors (>200V) based on oxide materials. Due to the thermal and chemical stability of GaN:RE and indium-tin-oxide films, higher temperature (and/or reactive by-products) are allowed during formation of dielectric films. When deposited on an amorphous dielectric layer, GaN:RE is generally c-axis oriented with a (0002) linewidth of 0.174° and exhibits the

same emission witnessed in GaN:RE grown on single-crystal lattice-matched substrates. GaN:RE phosphors can be deposited at ~600°C which allows compatibility with standard FPD glass substrates. In place of indium-tin-oxide electrodes, a ZnO:Al electrode and AlN dielectric layer may be utilized to promote GaN:RE grain growth. Utilizing a promising AC-ELD structure[2] which is being pioneered for use in flat TVs, GaN:RE phosphors are allowed deposition temperatures in the range of 600-900°C. This high-yield and high-performance device structure uses simple screen-printing and sintering of a thick-film dielectric layer. Such thick-film dielectrics can be based on barium titanate along with glass or fluxing agents that facilitate low temperature (<900°C) sintering of a high permittivity (ε ~6000) dielectric layer. Using the GaN:RE phosphor removes the need for a ceramic substrate and a thin-film planarization layers required by ZnS-based phosphors. The chemical and thermal stability of GaN:RE has allowed us to develop a novel AC-ELD fabrication technique drawing on several advantages of the aforementioned structures on glass and ceramic substrates. We will present the latest material issues and options for GaN:RE electroluminescent phosphors. Improved viability of GaN:RE for flat panel displays has been achieved by significantly improving device yield and performance while utilizing simple and low-cost fabrication methods. [1]A. J. Steckl, J. Heikenfeld, M. Garter, R. Birkhahn, and D. S. Lee, Compound Semiconductor 6 (1), 48 (2000). [2]S. Grossman, Electronic Design, p. 25, May 1 (2000).

11:20 AM (Student)
Z4, Sinusoidally-Modulated III-V Semiconductor Superlattices by Molecular Beam Epitaxy: *Xinyu Liu*[1]; Yuji Sasaki[1]; Paul M. Reimer[2]; Sanghoon Lee[3]; Jacek K. Furdyna[1]; [1]University of Notre Dame, Phys. Dept., 225 Nieuwland Science Hall, Notre Dame, IN 46556 USA; [2]Goshen College, Turner Precision X-ray Lab., Goshen, IN 46526 USA; [3]Kwangwoon University, Dept. of Elect. Mats. Eng., Seoul 139-701 Korea

III-V semiconductor "sinusoidal superlattices", i.e., periodic structures in which the chemical composition of an alloy varies sinusoidally along the growth direction, were fabricated by a novel MBE growth method. This was accomplished by substrate rotation in the presence of an inhomogeneous distribution of elemental fluxes over the substrate area instead of shutter openings and closings. We first focus on sinusoidal $GaAs_{1-x}Sb_x$ superlattices, i.e., on a system comprised of one cation and two anions, to demonstrate that the period of the superlattice is determined by the rate of rotation when the flux intensities are fixed; and that the amplitude of compositional modulation can be controlled by the position of the growth relative to the axis of rotation. The compositional profile is concluded to be very nearly sinusoidal on the basis of θ-2θ X-ray spectra, from the fact that only a single pair of satellite peaks occurs around each "alloy" Bragg reflection. The quality of the superlattices is very high, as inferred from the fact that the satellite peaks are as narrow as the "parent" Bragg reflections. The modulation amplitude of the chemical composition x was determined by fitting X-ray scans around the Bragg reflections for Ga $As_{1-x}Sb_x$ sinusoidal superlattices to a simple scattering theory. We will also discuss sinusoidal superlattice formation in two-cation systems, such as GaInAs and GaAlAs; and we will compare these superlattices with their II-VI-based counterparts, e.g., $ZnSe_{1-x}Te_x$. Finally, we discuss the special advantages of such a shutter-less method of superlattice fabrication, and the capability of generating various potential profiles using this new technique. Supported by U.S. Department of Energy Grant No. 97ER45644.

11:40 AM
Z5, Anomalous Properties of Triple-Period-A (TP-A) Type Ordering in GaInP with Sb Added During Growth: *Tohru Suzuki*[1]; Toshinari Ichihashi[1]; Chung-Chi Hsu[2]; [1]NEC Corporation, Sys. Dev. & Fund. Rsch., 34 Miyukigaoka, Tsukuba, Ibaraki 305 Japan; [2]The Chinese University of Hong Kong, Dept. of Elect. Eng., Shatin, N.T., Hong Kong China

Since the discovery of the A-type ordering of TP-A type in MBE-grown AlInAs alloys and of CuPt-A type in MBE-grown AlInP alloys, A-type ordering, in which ordering directions are [111]A or [-1-11]A, has been observed in several other alloys grown by MBE and MOVPE. In the past year TP-A ordering that had never been observed in MOVPE-grown GaInP, in which only CuPt-B had been reported, was found in MOVPE-grown GaInP when very small amount (0.1~1%) of Sb is added during growth under conventional growth conditions in which CuPt-B is formed unless Sb is added. This phenomenon has been interpreted as the Sb's low volatility having enabled the MOVPE growth surface to form double layers of group-V atoms with x3 periodicity arising from the top-most dimer arrays. The TP-A ordering observed in this GaInP has shown very special properties; we have reported that the streak orientation in the dark field pattern is opposite to that which has been reported for any other alloy systems grown by any growth methods and for other types of ordering. The streak orientation has been related to a new orientation relation between the variant-domain-orientation of the TP-A-ordering and the ordering direction. Recently, in MOVPE-grown Sb-added GaInP alloys, we discovered a violation of a variant selection rule that has not, thus far, been observed in any types of ordering examined in any alloy systems grown by any growth methods and conditions. The conventional 'rule' is that between the two allowed ordering directions among the 4 equivalent directions, ordering tends to occur in the direction in which a vicinal substrate surface has a misorientation. This rule thus far ubiquitously observed, however, has been violated in the present TP-A ordering in Sb-added GaInP; that is, the ordering direction is opposite to that in which the substrate surface is misoriented. In this paper we describe the details of this new anomaly and the domain orientation anomaly observed earlier. Both anomalies should be closely related to each other. We will also discuss the implications of these conspicuous phenomena
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Session AA: Nanoscale Fabrication and Self-Assembled Systems

Friday AM Room: 102
June 29, 2001 Location: University of Notre Dame

Session Chairs: E. L. Hu, iQUEST/UCSB, Santa Barbara, CA 93106 USA; David Janes, Purdue University, Dept. of Electl. Eng., West Lafayette, IN 47907-1285 USA

8:20 AM
AA1, Room Temperature Infra-Red Absorption in Electrochemically Self-Assembled 3.5 nm CdS Quantum Dots: *Supriyo Bandyopadhyay*[1]; Nikolai Kouklin[1]; Alexander Balandin[2]; [1]University of Nebraska, Electl. Eng., Lincoln, NE 68588-0511 USA; [2]University of California, Electl. Eng., Riverside, CA 92521 USA

We have observed infrared absorption in electrochemically self assembled well-ordered CdS quantum dot arrays. The absorption is peaked at 3.3 microns wavelength and corresponds to transitions between the lowest two quantized subband states in the conduction band. The effective diameter of the dots estimated from this measurement is 3.6 nm which is in excellent agreement with the 3.5 nm diameter estimated from the blueshift in the band edges measured by band-to-band absorption. We have measured the infra-red absorption by two different techniques: polarized Raman spectroscopy and Fourier Transform Infrared Spectroscopy (FTIR). Both techniques show an absorption peak at 3.3 microns. We have measured the absorption at both 77K and room temperature. The linewidth is temperature insensitive showing that the major contribution is from inhomogeneous broadening. This observation holds out the promise for room temperature infrared photodetectors at 3.3 micron wavelength. The corresponding spectral region is suitable for remote sensing applications, targeting and ranging. In the past, Stranski-Krastanow grown dots have shown infra-red photoresponse at around 17 microns wavelength under cooling. In contrast, our system absorbs at 3.3 microns at room temperature. Additionally, the potential barriers surrounding our dots are much more opaque; hence, we expect significantly reduced dark current.

8:40 AM
AA2, Electrochemical Self-Organization of Nanopores on Anodized Aluminum Oxide: *Sunil K. Thamida*[1]; Pavlo Takhistov[1]; Hsueh-Chia Chang[1]; [1]University of Notre Dame, Chem. Eng., 182 Fitzpatrick Hall, Notre Dame, IN 46556 USA

Nanoporous Aluminum oxide forms when Aluminum is anodized in an acidic electrolyte of pH<6. The electrochemical reactions involved in Aluminum anodization and its oxide formation have been widely studied. The pore size was found to vary linearly with the applied voltage. Also the pores were found to be arranged in a hexagonally packed colonies. It has drawn attention of exparimentalists to achieve a hexagonally packed array of nanopores which open windows to novel applications of nanoporous materials such as selective substrates, optic filters, quantum dot arrays, bio-sensors, etc. In spite of the surfeit of experimental data, pore formation still lacks a model that completely describes the observed phenomenon. A more satisfactory description of steady state pore selection based on electric field dependent oxide formation and dissolution is postulated recently based on the assumption that pore bases are spherical. We approach this problem from the point of view of interfacial pattern formation. At the beginning of anodization, the oxide layer remains flat and soon attains a constant thickness. At metal-oxide(m-o) interface, metal dissolves while at oxide-electrolyte(o-e) interface, oxide forms and dissolves simultaneously. The dissolution of oxide is due to the hydrogen ion concentration of the acidic electrolyte. By neglecting the space charge in the oxide, the potential field inside the oxide layer is governed by a Laplace equation. We perform a linear stability analysis and find that pores would evolve whose wavelength is proportional to the applied voltage which is consistent with experimental data in the range of 0<pH<1. Once the pores are initiated, they propagate to a few micrometers deep depending on the time of anodization. The steady state shape of the pore base was obtained by the method of hodograph transform for a wide range of pH values. The numerical simulation provided a useful information on shape of the pore base whether it is flat or spherical or like a long nose. We could predict why we observe a (decrease-reach base state-increase-reach maximum and level off or steady state) behavior of current density Vs time in potentiostatic anodization. But linear stability analysis would not specify the pore topography(circular or elliptic or stripes). Depending on the relative magnitudes of the wave number in each directions, there could be a multitude of topographies possible. In order to predict the topography of pores and their ordering, one needs to perform a non-linear analysis of the interfacial growth equations. A similar approach has given fruitful result in the case of electropolishing patterns on Aluminum. Our goal is to engineer a regular array of nanopores on thin film Aluminum by anodization.

9:00 AM

AA3, Template Based Electrochemical Fabrication of Nanostructured Materials and Their Applications: Albert E. Miller[2]; Charles Arvin[2]; Pavlo Takhistov[2]; Juan Jiang[2]; *Michael Crouse*[2]; Stephen P. McGinnis[1]; Paul Sines[1]; Daniel Gray[1]; Biswait Das[1]; [1]West Virginia University, CSEE Dept., PO Box 6109, Morgantown, WV 26505 USA; [2]University of Notre Dame, Dept. of Chem. Eng., Notre Dame, IN 46556 USA

West Virginia University and the University of Notre Dame have developed a thin film template based nanostructure synthesis technique that has the potential to provide economical fabrication of low dimensional photonic devices. This technique is based on the electrochemical synthesis of semiconductor nanostructures in a porous template formed by the anodization of aluminum deposited on a silicon substrate. The nanostructure diameter is determined by the pore size in the alumina template, and can be varied between 10-100 nm. The electrochemical deposition of various II-VI compounds is carried out in non-aqueous systems with the alumina template left in place. This non-aqueous in-situ deposition has several significant advantages including: no destructive chemical interactions with the alumina template, improved nanowire microstructure, and no tedious alumina template manipulations are required. The control and flexibility of nanostructure size using this method provides the ability to continuously vary the individual structures from zero dimensional confinement (quantum dots) to three dimensional bulk solids. We are currently using this technique to develop large area photovoltaic cells, narrow-band optical detectors, and electro-optic modulators based on the quantum confined Stark effect. In addition, we are exploring how this technique can be used to fabricate biosensitive active materials. The biocompatibility of nano-size colloidal gold and magnetite as an immobilization matrix for biomolecules has stimulated development of active biosensitive materials which are compatible with integrated silicon technology. We have electrophoretically deposited two types of colloidal gold particles and nanoscale megnetite colloids into nanoporous silicon formed using the alumina template. The nanoscale irregularity of the silicon/electrolyte interface and the difference in conductivity of the Si and electrolyte causes a significant gradient in the electrical potential in the pores. This “electrofocusing” effect allows the direct deposition of the gold nano-colloids into the silicon pores. The deposited colloids are mechanically and chemically stable and can be released from the substrate by either manipulation of the pH of the surrounding electrolyte or by reversing the applied electrical field. We will present methods for the synthesis of the thin film anodized aluminum template and the electrochemical deposition of various compound semiconductors and colloids. The factors controlling the regularity of the hexagonal matrix; particularly, how the thin film aluminum precursor microstructure affects the resulting pore structure will be discussed. In addition, we will present the results of optical (PL, absorption, photocurrent spectroscopy), electronic (transport, capacitance spectroscopy), and structural (AFM, FESEM, TEM) characterization of the nanostructure arrays. Finally, we will discuss the use of this fabrication technique to construct several types of photonic devices and active biosensor materials. This will include an analysis of the performance of these devices and the potential for their integration with current silicon CMOS technology.

9:20 AM (Student)

AA4, Gas-Phase Generated Nanocrystals with Self-Adjusted Sub-µm Film Feature Size: Frank Otten[1]; Uwe Auer[2]; F. Einar Kruis[3]; Werner Prost[2]; Franz Josef Tegude[2]; Heinz Fissan[3]; [1]Gerhard-Mercator-University Duisburg, Proc. & Aerosol Tech. Dept. & Solid State Elect. Dept., Bismarckstr. 81, Duisburg 47057 Germany; [2]Gerhard-Mercator-University Duisburg, Solid State Elect. Dept., Lotharstr. 55, Duisburg 47048 Germany; [3]Gerhard-Mercator-University Duisburg, Proc. & Aerosol Tech. Dept., Bismarckstr. 81, Duisburg 47057 Germany

The exploitation of semiconductor quantum effects is inhibited due to the extremely sophisticated and expensive technology necessary for a full 3-dimensional definition of nanostructures below the quantum limit. A different route is the direct generation of 3-D nanocrystals through the liquid phase[1] or through the gas phase[2,3]. These generation processes have the potential for low-cost and parallel production of films consisting of quantum dots[4,5]. Gas-phase generation processing is advantageous because ligands and liquid solvents are absent in comparison to the liquid-phase nanocrystal generation process[2]. Is was shown that gas-phase generated nanocrystals have the potential for future nanoelectronic devices[4,5] and for sensors[7]. Especially lead sulfide (PbS) is advantageous because quantum effects occur already at nanocrystal sizes below 20 nm. The band gap of single nanocrystals can be tuned from 0.41 eV up to several eV by decreasing the size[1]. A limitation for the exploitation of gas phase generated nanocrystal films is the lack of suitable lithographic tools. In this contribution a process is developed to overcome this disadvantage. Single-sized PbS nanocrystals are selectively deposited from the gas-phase onto photoresist-patterned substrates at atmospheric pressure, forming patterned nanocrystal thin films. Selective deposition is obtained by means of electrostatic control of the charged nanocrystals in the gas phase. This process is characterized by low cost and high parallelism. During the deposition of nanocrystals from the gas phase a preferred deposition into the resist openings, i.e. onto the unmasked substrate surface is observed. An electrostatic model is developed to explain this focusing effect. It explains the observed minimum film feature sizes smaller than the employed optical lithographic resolution for the patterned photoresist. The model is supported by REM pictures of samples with nanocrystal coverage ranging from zero to one µm thick nanocrystal film. This work is partly supported by Deutsche Forschungs-gemeinschaft TE 179/8-1. [1]Y. Wang and N. Herron: J. Phys. Chem., 1991, 95, 525; [2]F.E. Kruis, K. Nielsch, H. Fissan, B. Rellinghaus and E.F. Wassermann: Appl. Phys. Lett., 1998, 74, 547; [3]K. Deppert, J.-O. Bovin, J.-O. Malm and L. Samuelson: J. Crystal Growth, 1996, 169, 13; [4]W. Prost, F.E. Kruis, F. Otten, K. Nielsch, B. Rellinghaus, U. Auer, A. Peled, E.F. Wassermann, H. Fissan and F.J. Tegude: Microelectron. Eng., 1998, 41/42, 535; [5]K.K. Nanda, F.E. Kruis, H. Fissan and M. Acet: annual scientific meeting ‘ESF-NANO 1999’, (ed. Fissan et al.), 20; 1999, Duisburg, Germany; [6]L. Montelius, T. Junno, S-B. Carlsson, M.H. Magnusson, K. Deppert, H. Xu and L. Samuelson: Microelectron. Reliab., 1998, 38, (6-8), 943; [7]F.E. Kruis, H. Fissan and A. Peled: J. Aerosol Sci., 1998, 29, (5/6), 511.

9:40 AM

AA5, Self-Assembled ZnO Nanostructures Within a Diblock Copolymer Matrix on Si and SiO2 Surfaces: *Agis A. Iliadis*[1]; Hasina Afroz Ali[1]; Robert F. Mulligan[2]; Unchul Lee[3]; Peter Kofinas[2]; [1]University of Maryland, Electl. & Comp. Eng. Dept., College Park, MD 20742 USA; [2]University of Maryland, Matls. & Nuclear Eng. Dept., College Park, MD 20742 USA; [3]Army Research Laboratory, 2800 Powder Mill Rd., Adelphi, MD 20783 USA

The development of self-assembled ZnO nanoparticles within a diblock copolymer matrix on the surfaces of p-type Si and SiO2/Si wafers, is reported. Diblock copolymers consisting of poly (norbornene) and poly (norbornene-dicarboxcylic acid) (NOR/NORCOOH), were synthesized using the opening metathesis polymerization (ROMP) method. The self-assembled microphase separated morphology of the block copolymer is used as a templating medium within which metal oxide nanoclusters can be grown in a controlled manner through a nanoreaction scheme. The self-assembly of the metal-oxide within the matrix of the diblock copolymer is achieved at room temperature by introducing ZnCl2 precursor into the second (minority) polymer (NORCOOH) block, and processing the copolymer by wet chemical methods to substitute the chlorine atoms with oxygen. The doped polymer in solution was spin-cast on Si and SiO2 surfaces, processed to substitute the Cl atoms with oxygen and allowed to dry. A photolithographic approach using spin-on photoresists was developed in order to pattern the copolymer on the wafer surface and deposit metallizations. The properties of the films were evaluated using x-ray photoemission spectroscopy (XPS), infrared spectroscopy, and electrical and optical measurements. Infrared spectroscopy confirmed that the ZnCl2 was associated with the second block of the copolymer providing the self-assembly capability, and XPS verified the conversion of ZnCl2 to ZnO, by monitoring the disappearance of the Cl 1s peak, and the change in the binding energy of the Zn 2p3 peak in high resolution spectra. The substitution of Cl by O was found to be a highly preferential process, whereby only one approach using a weak base (NH4OH) succeeded in effectively replacing Cl with O to result in ZnO self-assembled nanoclusters. The novel properties of such ZnO-copolymer nanocomposites, and the development of the photolithographic processing steps, will be discussed. This work provides a promising approach for nanoscale fabrication and delivery of such nanoclusters into device technologies.

10:00 AM Break

10:20 AM

AA6, Room Temperature Coulomb Diamond Characteristic of Single Electron Transistor: *Y. Gotoh*[1]; K. Matsumoto[1]; T. Maeda[1]; [1]Electotechnical Laboratory, 1-1-4 Umezono, Tsukuba, Ibaraki 305-8568 Japan

It was so far difficult to observe the Coulomb diamond characteristics at room temperature. We have succeeded in fabricating the single electron transistor (SET), which shows the room temperature Coulomb diamond characteristics using the atomic force microscopy (AFM) nano-oxidation process. In the process, the Ti metal on the atomically flat Al2O3 substrate was selectively oxidized by the applied bias between the AFM cantilever and the thin Ti film to form the oxidized Ti line (TiOx), which worked as the energy barrier for the electron. The SET structure had one island between two tunnel junctions made by the TiOx barrier, and the gate electrode was formed on the backside of the Al2O3 substrate. In order to fabricate the smaller island and the narrower tunnel junctions, the single wall carbon nanotube (SWNT) AFM cantilever was adopted in the process. The SWNT was grown onto the top of the conventional Si AFM cantilever by the chemical vapor deposition (CVD). The diameter of the SWNT was 2nm, which was ten times smaller than the conventional Si cantilever. The size of the fabricated SET was that the tunnel junction width of 16nm, and the island length and width of 25nm and 5nm, respectively. After the AFM nano-oxidation process, the SET was annealed from 120 to 170 degrees Centigrade in air for the further reduction of the island size. This annealing process could uniformly oxidize Ti film from the surface close to the air. The Coulomb diamond characteristics of the SET were measured at room temperature. The gate bias was applied from -6V to 6V with 50mV step and the drain bias was changed from -1V to 1V with 20mV step. The clear six Coulomb diamonds were observed between VG=-6V to +6V, and the Coulomb oscillation characteristic showed 2V periods. From the slope of the Coulomb diamond characteristics at room temperature, the tunnel junction capacitances were calculated to be C1=0.03aF and C2=0.09aF. Because of fluctuation of the size of AFM nano-oxidation process, two-tunnel junctions had the slightly difference capacitance values. The calculated Coulomb energy, e2/2 C $B-t (B where C $B-t (B= C1+ C2+Cg, was as high as 400meV which was 15 times higher than the room temperature thermal energy of 26meV. This high value of the Coulomb energy attributed the observation of the clear Coulomb diamond characteristics even at room temperature in our SET. We have first succeed in observing the stable Coulomb diamond characteristics even at room temperature in the SET which was fabricated by the SWNT cantilever AFM nano-oxidation process and the thermal squeezing process.

10:40 AM (Student)

AA7, Single Crystalline Si Formed on Amorphous Substrate at Low Temperature by NanoPatterning and Nickel Induced Lateral Crystallization: *Jian Gu*[1]; Stephen Y. Chou[1]; Henny Zandbergen[2]; [1]Princeton University, Dept. of Elect. Eng., Princeton, NJ 08544 USA; [2]Princeton University, Princeton Matls. Inst., Princeton, NJ 08544 USA

Forming single crystalline silicon on amorphous substrate at low temperature is highly desired for fabrication of high performance thin-film-transistors (TFTs) for many important applications, including active matrix liquid-crystal display (AMLCD) and future 3-dimensional (3-D) integrated circuits[1-2]. However, it is difficult to achieve because single crystalline silicon cannot grow epitaxially on an amorphous substrate. Excimer laser annealing has been a candidate to obtain this goal[1]. Here, we will report a new approach that can also achieve single crystalline silicon on amorphous substrate at low temperature. It is accomplished by NanoPatterning of amorphous silicon (a-Si) film followed by nickel induced Lateral Crystallization (NanoPLC). Traditionally, Nickel Induced Lateral Crystallization (NILC) creates polycrystalline silicon film because multiple NiSi2 precipitates serve as seeds for the crystal growth[3]. With nanopatterning, we can limit one seed at the starting location of lateral crystallization for each pattern, leading to the single crystalline silicon formation. In our fabrication process, 45 nm a-Si film on thermally oxidized Si wafer was patterned into nanoscale lines by nanoimprint lithogrpahy (NIL), then crystallized at 500°C by NILC. The line width ranged from 20 nm to 450 nm. The single crystalline properties of crystallized a-Si lines were verified by comparing the convergent beam diffraction pattern along the line using transmission electron microscope (TEM). More than 80 lines were examined. TEM study shows that single crystalline silicon has been formed inside the line. What more intriguing is that this was achieved in all the crystallized lines with line width of 40 nm to 200 nm (totally 46 lines). This result implies not only a superior device performance to the conventional TFTs; but also a better device-to-device uniformity, which is a key for most TFT applications. TEM study also shows that the line width affects the silicon grain formation significantly. For lines with a width above 250 nm, single crystalline silicon can still form. However, Competitive Grain Growth (CGG) could happen at the beginning of lateral crystallization. While narrower line width, i.e. 30 nm or less, resulted in amorphous film with little lateral crystallization. By combining nanopatterning and NILC, single crystalline silicon has been formed on amorphous substrate at low temperature. Line width affects the grain formation significantly. The results should potentially impact the fabrication of high performance TFTs, AMLCD and 3-D integrated circuits. [1]James S. Im, Robert S. Sposili, and M. A. Crowder, Appl. Phys. Lett. 70, 3434 (1997); [2]Vivek Subramanian and Krishna. C. Saraswat, IEEE Trans. Electron Devices, vol. 45, No. 9, 1934 (1998); [3]G. A. Bhat, Z. Jin, H. S. Kwok, and M. Wong, IEEE Electron Device Lett. 20, 97 (1999).

11:00 AM

AA8, Temperature-Dependent Ordering Process of Self-Assembled Ge Islands in the Multi-Layer Structures: Makoto Miura[1]; Jean-Michel Hartmann[2]; Jing Zhang[2]; Bruce Joyce[2]; *Yasuhiro Shiraki*[1]; [1]The University of Tokyo, Rsrch. Ctr. for Adv. Sci. & Tech. (RCAST), 4-6-1 Komaba, Meguro-ku, Tokyo 153-8904 Japan; [2]Imperial College of Science and Technology and Medicine, The Blackett Lab., Ctr. for Elect. Matls. & Dev., Prince Consort Rd., London SW7 2BZ UK

The ordering effect of the self-assembled Ge islands in the multiple layers was found to strongly depend on the growth temperature as well as the Si spacer layer thickness, which reflects the correlation between atom migration and strain fields induced by the buried islands. The structures used in this study were 10 repeated Ge island layers with Si spacer layers grown on Si (001) substrates by using gas source molecular beam

epitaxy. The Ge coverage was set to 5.8 ML and 7.2 ML at the growth temperature of 600°C and 525°C, respectively, where the number of the islands became the largest at each temperature. At 600°C, the size- and the positional-ordering of the islands was found to appear only in a certain range of the Si spacer layer thickness. When the Si spacer layer thickness was 39 nm, the excellent ordering of the islands was observed, i.e., the initially distributed islands changed their morphology to the well-ordered islands whose size and inter distance were almost equalized. During ordering, the island size was found to increase along with the decrease in the density. Further decrease of the Si spacer layer thickness resulted in larger distribution. The ordering effect was also observed but in different ways when the growth temperature was 525°C. The elongated hut-cluster-shaped islands changed their shape to the well-ordered pyramid-shaped islands when the Si spacer layer thickness was decreased from 88 nm to 22 nm. During this shape change, the largely distributed length of the hut-clusters decreased and was equalized to their width whose distribution was very small. At the same time, the density was found to increase with ordering in contrast to the case of 600°C. We attributed these characteristic features of the ordering to the correlation between the migration of Ge adatoms on Si surfaces and the surface potentials induced by the buried Ge islands. When the growth temperature is high (~600°C), Ge adatoms freely migrate into the potential minima provided by the strain field from buried islands. When the Si spacer layer thickness becomes thinner, however, the potential barriers next to the potential minima become too high for Ge adatoms to freely migrate to the potential minima, which results in the breakdown of the ordering. In the case of 525°C, small Ge migration at this temperature and characteristic shapes of the buried hut-clusters induce the ordering of the islands only in the direction of the length of the hut-clusters. Thus, the well-ordered smaller islands are realized when the Si spacer layer thickness becomes small.

11:20 AM (Student)

AA9, Fabrication of Germanium Dots on Different Dielectric Substrates: *Dong-Won Kim*[1]; Young-Hee Kim[1]; Freek E. Prins[1]; Dim-Lee Kwong[1]; Sanjay Banerjee[1]; [1]The University of Texas at Austin, Microelect. Rsrch. Ctr., 2.604H, MC R9950, Austin, TX 78758 USA

Silicon or silicon-germanium dots embedded in an insulator have potential application for room temperature operation of single-electron transistor memories and nonvolatile memory devices. In contrast to Si dots, Ge dots have only been realized by CVD on crystalline Si substrates so far. On insulators the fabrication of Ge dots is much more difficult because of the low evaporation temperature of Ge and the higher surface energies of the insulators as compared to Si. In this study, we have achieved direct growth of Ge dots on insulators such as nitrided oxides, which are suitable for tunneling oxides (3nm) in memory devices. This was accomplished using ultrahigh vacuum chemical vapor deposition (UHVCVD) of GeH_4 at low temperature. Germanium dots were grown at different temperatures on various dielectric substrates, Si_3N_4, SiO_2, oxynitride, NH_3-annealed oxynitride, NH_3-annealed nitride, and N_2O-annealed nitrided oxide. These samples were studied using atomic force microscopy (AFM), angle resolved X-ray Photoelectron Spectroscopy (ARXPS), Auger electron spectroscopy (AES) in order to characterize the Ge dots and the chemical composition of those substrate surfaces. The final surface morphologies of the various dielectric substrates after the growth of Ge dots at 550°C for 2 minutes and in situ annealed for 5 minutes under high vacuum were studied using AFM. Only for the N_2O-annealed nitride oxide substrate well-defined dots, approximately 3nm in height were observed. In order to investigate the influence of the atomic nitrogen concentration in the dielectric substrates, AES studies were performed, before growth of the Ge dots. From the AES data, we conclude that there is no direct correlation between the nitrogen concentration in the dielectric substrates and Ge dot formation. From the surface analysis of the dielectric substrates using ARXPS, we found that the surface of the Si_3N_4 consists of SiN_x, whereas the surfaces of oxynitride (SiO_xN_y) and NH_3-annealed oxynitride consist of SiO_x. In contrast, the surface of the N_2O-annealed nitride oxide substrate exhibits both Si-N and Si-O bonds. We therefore conclude, that during the N_2O anneal, the top surface of N_2O-annealed nitrided oxide is oxidized and changed from pure Si_3N_4 to SiO_xN_y. The top surfaces of NH_3-annealed oxynitride and oxynitride (SiO_xN_y) are passivated by the oxide which is stochiometric SiO_2. These observations indicate that the surface N atoms which are bonded to the Si, are dissociated and partially substituted by oxygen during N_2O treatment. This partial substitution by oxygen atoms may generate large numbers of surface dangling bonds. As dangling bonds on the surface act as Ge nucleation sites, this will result in a large number of dielectric surface defect sites available for Ge nucleation. This is further confirmed by studying the growth kinetics and the influence of in-situ annealing of the samples.

11:40 AM (Student)

AA10, The Influence of a Buried Misfit Dislocation Network on the Pyramid-to-Dome Transition Size in Ge Self-Assembled Quantum Dots on Si(001): *Hyung-Jun Kim*[1]; Joon-Yeon Chang[1]; Ya-Hong Xie[1]; [1]University of California–Los Angeles, Dept. of Matls. Sci. & Eng., Box 951595, Los Angeles, CA 90095 USA

We report experimental observation of a marked difference in the critical size of pyramid-to-dome transition in SiGe self-assembled quantum dots (SAQDs) grown on Si(001) from those grown on a relaxed SiGe buffer layer. This change in critical dot size is related to the total free energy of pyramids and domes, as discussed in the literature[1]. Our results point to the fact that the relative free energy of pyramids and domes are influenced by the misfit strain within the dots, with pyramids being stable up to large dot size when the misfit strain is low. All the samples used in this study are grown by molecular beam epitaxy (MBE). Two types of substrates are used for the SAQDs growths: bulk Si (001) and approximately 10% relaxed Si0.75Ge0.25 buffer layers (600Å thick) with a thin Si cap layer (100Å). Typical sample structure includes a pure Ge wetting layer (4.5Å) grown at 280C, followed by 2.5Å thick of SixGe1-x SAQDs grown at 650C. The Si concentration is varying between 0 to 0.5. The purpose of the low-temperature wetting layer is to minimize alloying between the substrate and the wetting layer, thereby giving us a more precise control of the SAQDs composition. The resulting size and shape of SAQDs are characterized using a Park Scientific atomic force microscope (AFM) in contact mode. We also carry out plan-view transmission electron microscopy (TEM) study to correlate individual dots with the underlying misfit dislocation network in the relaxed buffer layers. We have observed that the for the same SAQDs composition, the critical dot size for the pyramid-to-dome transition for samples grown on the relaxed buffer layer is significantly larger than those grown on bulk Si (001). For Si0.5Ge0.5 dots, this difference is 1050Å to 780Å. Corresponding TEM study using Burger's vector analysis indicates that dislocation pile up resulting in larger relaxation of the in-plane lattice constant at the surface of the relaxed buffer layer, resulting in smaller misfit strain within the SAQD grown directly on top of these dislocation pile ups. As a result, the critical dot size is increased. Our results illustrate the importance of SAQD misfit strain in influencing their size distribution. Such misfit strain needs to be controlled in order to achieve uniform size and shape distribution. [1]R.S. Williams, G. Medeiros-Ribeiro, T.I. Kamins, and D.A.A. Ohlberg, J. Phys. Chem. B. 102, 9605 (1998).

Session BB: SiC Processing and Characterization

Friday AM — Room: 141
June 29, 2001 — Location: University of Notre Dame

Session Chair: Michael Capano, Purdue University, Sch. of ECE, West Lafayette, IN 47907-1285 USA

8:20 AM (Student)

BB1, Comparative Hall Measurements on "Wet and Dry" Oxidized 4H-SiC MOSFETs: *Kiran Chatty*[1]; Jeffery Paul Langer[1]; T. Paul Chow[1]; Ronald J. Gutmann[1]; Emil Arnold[2]; Dev Alok[2]; [1]Rensselaer Polytechnic Institute, Ctr. for Integrated Elect., CII-6015, 110 8th St., Troy, NY 12180 USA; [2]Philips Research, 345 Scarborough Rd., Briarcliff Manor, NY 10510 USA

In this work we report on using Hall effect measurements to compare the properties of 4H-SiC inversion-mode MOSFETs with "wet" and "dry" gate oxides. Wet oxidized MOSFETs were found to have a higher interface state density compared to the dry oxidized MOSFETs resulting in a

higher trapped charge density with wet oxidation. MOS-gated Hall bar structures were fabricated on a p/p+ epilayer with a nominal epilayer thickness and doping of 10µm and $7x10^{15}cm^{-3}$ respectively. The gate oxide was deposited at 400°C followed by oxidation and anneals. In the dry oxide sample, oxidation was carried out at 1100°C for 3 hours in dry oxygen, followed by 1 hour argon anneal at 1100°C resulting in ~200nm thick oxide. The oxidation scheme in the wet oxide sample was similar, except that oxidation was carried out in pyrogenic steam and the argon anneal at 1100°C was followed by a re-oxidation anneal at 950°C for 3 hours in pyrogenic steam, resulting in an oxide thickness of ~250nm. Hall mobility (μ_{Hall}) and carrier concentration (N) were extracted from Hall measurements on MOS-gated Hall bar structures. The maximum μ_{Hall} was ~80 $cm^2/V-s$ in the wet oxide sample and ~70 $cm^2/V-s$ in the dry oxide sample. In contrast, the field-effect mobility (μ_{FE}), extracted from the transconductance (g_m), was much lower (~5 $cm^2/V-s$ in dry oxide sample at V_G=80V compared to ~2 $cm^2/V-s$ in the wet oxide sample at V_G=100V). The g_m in the dry oxide sample increases more sharply with V_G and reaches a peak while in the wet oxide sample g_m increases monotonically. g_m and μ_{FE} are limited by trapping of carriers in the interface states. The N in both the wet (~$6.3x10^{10}$ cm^{-2} at V_G=100V) and dry oxide samples (~$7.0x10^{11}$ cm^{-2} at V_G=100V) are more than an order of magnitude less than predicted by the chargesheet model (N_{ideal} ~$1x10^{13}$ cm^{-2} at V_G=100V). The trapped charge density (Q_t) is ~2.5 times larger in wet oxide sample (~$8.6x10^{12}$ cm^{-2}) compared to the dry oxide sample (~$3.4x10^{12}$ cm^{-2}) at E_C-E=0.1eV (calculated as $Q_t=q(N_{ideal}-N)$). The interface state density ($D_{it}=dQ_t/d\Psi_s$), extracted using Hall measurements, was higher in wet oxide sample (D_{it}~$8x10^{13}$ cm^{-2} eV^{-1} at E_C-E=0.1eV) compared to dry oxide sample (D_{it}~$5x10^{13}$ cm^{-2} eV^{-1} at E_C-E=0.1eV). The dry oxidized 4H-SiC MOSFETs had a better transconductance, lower threshold voltage, improved subthreshold slope and a higher inversion carrier concentration compared to the wet oxidized 4H-SiC MOSFETs, due to a lower interface state density near the conduction band edge. Acknowledgements: The authors from RPI acknowledge the support of this work by Philips Research, MURI Contract #N00014-95-1-1302, DARPA under Contract #MDA972-98 C-0001 and NSF Center for Power Electronics Systems under contract #EEC-9731677.

8:40 AM (Student)

BB2, Low Damage Etching of Silicon Carbide Using Cl2 Based Plasmas: *Farid Ahmed Khan*[1]; Ling Zhou[1]; Vipan Kumar[1]; I. Adesida[1]; [1]University of Illinois, Dept. of Electl. Eng. & Microelect. Lab., 208 N. Wright St., Urbana, IL 61801 USA

Silicon Carbide (SiC) is a wide bandgap semiconductor with potential applications for radiation resistant, high power, high frequency, and high temperature devices in the automotive, aerospace, power-generation and petroleum industries. Static induction transistors, metal-semiconductor-field effect transistors (MESFETs), and metal-oxide-semiconductor field effect transistors (MOSFETs) are examples of devices that have been realized in this material. Etching of SiC is non-trivial with wet etching and it is only possible using electrochemical techniques. High density plasma techniques such as inductively-coupled plasma reactive ion etching (ICP-RIE) are versatile for achieving high etch rates with minimal damage to etched surfaces. Fluorine-based plasmas have been investigated for etching SiC in ICP-RIE systems for device fabrication and via-hole formation[1]. The prime advantage of fluorine-based plasmas for etching SiC is that they yield very high etch rates. Etch rates in excess of 1 µm/min have been reported using fluorine-based ICP-RIE plasmas[1]. However, while such high etch rates are very suitable for via-hole formation into SiC, lower etch rates are desirable for SiC device fabrication. Moreover, etch damage induced by fluorine-based plasmas on SiC surface has been reported to be highly stable which could not be completely annealed even at temperatures exceeding 1000°C [2, 3]. Recently, it was found that etch damage induced by chlorine-based plasmas could be fully annealed out at 800°C[1]. This has provided the impetus to further investigate chlorine-based ICP-RIE plasmas for SiC device fabrication. In this study, we will report on the etching of SiC using ICP-RIE in various Cl2-based mixtures, including Cl2/Ar, HCl/Ar, Cl2/SF6 and HCl/SF6. Etch rates have been investigated as functions of gas flow rate, bias voltage, pressure, and ICP power. Smooth surfaces and low damage are important for device fabrication; we will present AFM studies of etched surfaces and Schottky diode measurements on etched SiC epi-layers. A detailed study of surface damage and its annealing will be presented. Results of auger electron spectroscopy and x-ray photoelectron spectroscopy on these surfaces will also be presented. [1]F.A. Khan, et al., J. Electro. Mat. 30, 212 (2001); [2]H. Cho, et al., Appl. Phys. Lett. 76, 739 (2000); [3]J. Pearton, et al., Appl. Phys. Lett. 68, 2987 (1996).

9:00 AM (Student)

BB3, Mesa Isolation with Good Edge Acuity by Electron Cyclotron Resonance Plasma Etching of SiC Using Cl_2, CH_4, Ar_2, and a Resist Mask: *C. I. Thomas*[1]; H. Y. Cha[1]; D. W. Woodard[1]; V. Tilak[2]; K. Chu[1]; L. F. Eastman[1]; M. G. Spencer[1]; [1]Cornell University, Sch. of Electl. & Comp. Eng., 401 Phillips Hall, Ithaca, NY 14853 USA; [2]Cornell University, Sch. of Appl. & Eng. Phys., Ithaca, NY 14853 USA

SiC is well suited to high power and high frequency applications due to its high breakdown field and its high saturated electron velocity. In addition, its wide bandgap allows devices fabricated from SiC to withstand high temperatures of operation. In processing microwave MESFET devices on semi-insulating substrates, it is important to etch mesas for device isolation. To facilitate the connection of the gate contacts and the drain and source ohmic contacts, it is required that the mesa edges have a gentle slope. The easiest way to achieve this slope is to use a resist mask for the etch. Most of the dry etches used for etching SiC, while they have very high etch rates, cannot be easily used with resist masks. These etches either quickly polymerize the resist or develop pinholes in it, limiting the use of resist masks to only small etch depths. A $Cl_2/CH_4/Ar_2$ gas mixture was developed for use in the Electron Cyclotron Resonance (ECR) plasma etching of SiC for device fabrication. The maximum etch depth done with this gas system and a photoresist mask was 4 microns. Etch rates were studied as a function of the system stage temperature, chamber pressure, microwave power, and sample bias. The $Cl_2/CH_4/Ar_2$ mixture allows the use of both photoresist and e-beam resist as masks. This quality of the etch made it possible to achieve mesas with good slope acuity and also made it possible to use a composite lithography fabrication process. Photolithography was used within its comfortable range of accuracy and e-beam lithography was used for the submicron work. Etch rates as high as 1000A/min were achieved with smooth etched surfaces free from micromasking. The etch rate of the resist to that of SiC was 2:1 for photoresist and 1:1 for e-beam resist. For optimized conditions, the resist mask was removed after the etch by soaking in acetone for photoresist masks and in methylene chloride for e-beam resist masks. This work was made possible by the support of Advanced Engineering and Sciences ITT Incorporated. Program manager Steven Grice.

9:20 AM (Student)

BB4, Optimization of Carbon-Face SiC Metal Oxide Semiconductor Structures Using Low Temperature Oxidation and Post Oxidation Annealing: Chun Wang[1]; Mary Ellen Zvanut[1]; [1]University of Alabama at Birmingham, Phys. Dept., CH310, 1300 University Blvd., Birmingham, AL 35294-1170 USA

Most attempts at fabricating functional metal oxide semiconductor (MOS) structures using SiC involve oxidation of the Si-face between 1050 and 1200°C. Despite innovations such as low-temperature reoxidation, post oxidation NO annealing, and the use of non-polar faces, the oxides have not achieved device quality. The carbon-face has been explored only briefly because preliminary studies produced low quality structures. Assuming that the results originate from the instability of the C-face at typical Si-face oxidation temperatures, we have examined low temperature oxidation of C-face SiC substrates, and we have investigated the effects of several post oxidation conditions. The results confirm that the quality of the oxide grown on the carbon terminated surface can be improved by reducing the oxidation temperature below that typically used for the Si-face. Metal oxide semiconductor capacitors were fabricated on Si-face and C-face substrates with 1016 cm-2 N-doped epitaxial layers. The general oxidation procedure consisted of a steam oxidation at either 1150°C, 1050°C, or 950°C, followed in the last two cases by a dry oxidation at the same temperature. Oxidation time was adjusted to obtain a film thickness of approximately 50 nm. Al was evaporated to form 0.004 cm2 contacts. Room temperature high-low frequency capacitance-voltage (CV) data were used to obtain Vfb, and dark current-voltage (IV) data provided Vo. The latter was used instead of the typical breakdown voltage to avoid complete destruction of the sample. Vo was measured at a current density of 0.3 mA/cm2 (~1 uA) in accumulation. Whenever possible, 300°C high-low CV measurements were made. Reported results for each type of sample are averages from approximately nine capacitors. As expected, 57 nm oxides grown on the Si face in steam at 1150°C show consistent Vo (35 V) and Vfb (8 V);

however, the C-face structures exhibit erratic current-voltage curves with Vo as low as 10V. Although lowering the oxidation temperature to 1050°C improves C-face device characteristics slightly, oxidation at 950°C increases Vo to 30V and reduces Vfb to 6.5V. Encouragingly, Vo measured for these oxides coincides with the field expected for the onset of Fowler-Nordheim tunneling. Unlike oxides grown on the Si-face, C-face oxides grown at 950°C deteriorated after post oxidation Ar annealing. Preliminary results of NO annealing, a treatment known to dramatically reduce interface states in Si-face structures, showed a 20% reduction in Vfb without deteriorating the IV response. In summary, our data suggest that using oxidation temperatures below those used for the Si-face improves the electrical characteristics of an oxide grown the carbon-face of SiC. In addition to this result, we will discuss the effects of oxidation temperatures as low as 700°C and NO anneals at different temperatures.

9:40 AM

BB5, Defect Density at the SiC/SiO2 Interface During High Temperature Gas Exposure: *Peter Tobias*[1]; Brage Golding[1]; Ruby N. Ghosh[1]; [1]Michigan State University, Ctr. for Sensor Matls., 303 Physics & Astronomy Bldg., East Lansing, MI 48824 USA

A low density of states at interfaces between semiconductors and insulators allows for a stronger effect of electrical fields on the semiconductor, because the field is less shielded. Exposure to gases can change the density of states; e.g. annealing in hydrogen reduces this density at the Si/SiO2 interface. There have been attempts to use this method also for the SiC/SiO2 interface but results are not yet conclusive. We have fabricated MOS capacitors on thermal oxidized SiC by sputtering or e-beam depositing metal gates of platinum. The density of states in the accessible regions of the band gap were obtained from quasi-static and high-frequency capacitance-voltage (CV) curves of the devices. Additional CV characterization was performed in a furnace from 300 to 900K, which allows us to monitor interface state density (Dit) in-situ, i.e. during the gas exposures. This is in contrast to the traditional technique of measuring Dit after a time-temperature anneal. The positive effect of hydrogen annealing appears to be reversed following prolonged operation at high temperature in an atmosphere devoid of hydrogen. This is important for both SiC sensors and electronic circuits operating at high temperatures, because the device characteristics would change with time. We have also studied the properties of the insulator silicon dioxide at high temperature like the leakage current that could lead to wear-out. Thermal SiO2 on SiC is a poor insulator compared with thermal SiO2 on Si, making quasi-static characterization of devices often impossible, especially at higher temperatures. There are indications that reducing gases like hydrogen that improve the interface lead to higher leakage currents and that oxidizing gases like oxygen have the opposite effect. If both a good interface and a good insulator are desired, there would be a trade-off in fabricating silicon carbide MOS devices for higher temperature applications.

10:00 AM Break

10:20 AM (Student)

BB6, Characterization and Modeling of Low-Voltage 4H-SiC Schottky and PN Diodes: *Malay Trivedi*[1]; Krishna Shenai[1]; Philip G. Neudeck[2]; [1]University of Illinois at Chicago, EECS Dept., 851 S. Morgan St., 1120 SEO, Chicago, IL 60607 USA; [2]NASA Glenn Research Center, 21000 Brookpark Rd., Cleveland, OH 44135 USA

This paper reports the characterization and modeling of the influence of structural crystal defects on the static and transient performance of low-voltage (<200 V) 4H-SiC Schottky and PN junction diodes at temperatures up to 150°C. It is shown that the specific fabrication artifacts exercise a strong influence on forward and reverse conduction of the diodes. The observed anomalies include high reverse leakage current and significant deviation from ideal performance in the forward I-V characteristics of the diodes. The observed static characteristics were modeled by connecting a small diode in parallel with the main diode. The parameters of the small diode model the changes in material properties occurring at the localized defect sites. A good match is demonstrated between the measured and modeled results. No noticeable anomalies were observed in the reverse recovery performance of the diode. The reverse recovery current in the Schottky and PN diodes is shown to be because of displacement current through the junction capacitance, with negligible contribution form minority carriers. The forward and reverse conduction is shown to be more sensitive to specific fabrication artifacts than the C-V characteristics and transient performance. A significant deviation from ideal performance was observed in the forward I-V characteristics. In case of Schottky diodes, the deviation of the ideality factor of Schottky diodes from unity is modeled using the To anomaly to account for the presence of an interfacial layer and surface-state energy distribution. The barrier height extracted from C-V and I-V characteristics yield different values, but converge at higher temperatures, consistent with the To model. The Schottky diode current had a room-temperature ideality factor of 1.32. The 4H-SiC junction diode exhibited excess current levels at low values of forward bias (<2 V) with an ideality factor of 2. The enhanced current flow in the Schottky and PN diodes at low forward bias is attributed to altered material parameters at the defect locations. Modeling the diodes as a parallel combination of the main diode and a defect diode (with altered parameters) results in a good match of modeled performance with measured data. The defects do not seem to alter the reverse recovery performance of the diode. The reverse recovery performance of the Schottky diodes was independent of temperature. A current tail was observed in the reverse recovery characteristics of the Schottky and PN diodes. This is explained in terms of displacement current through the junction capacitance under the influence of changing diode reverse voltage.

10:40 AM

BB7, Spectroscopy of Light Emission Due to Electron-Hole Recombination in 4H and 6H SiC MOSFETs: *P. J. Macfarlane*[1]; R. E. Stahlbush[1]; [1]Naval Research Laboratory, Code 6816, 4555 Overlook Ave., Washington, DC 20375 USA

SiC, with its wide bandgap, high breakdown field and large thermal conductivity, is an attractive alternative for Si in high power, high temperature microelectronic devices. Because SiC can be thermally oxidized similarly to Si, SiC has been proposed as a replacement for Si in power MOS-gated devices. However, the channel mobility of SiC-based MOS devices continues to be significantly less than half of the bulk mobility. The reduced mobility is thought to be related to the high concentration of interface traps in these devices. Recently, we demonstrated that we could image light emission due to interface trap and bulk electron-hole recombination in 4H and 6H SiC MOSFETs. The light emission is generated by alternately driving the channel region between accumulation and inversion using what is essentially a charge pumping set-up. Here, we present results of spectral analyses conducted on the light emitted due to interface trap recombination. Spectral studies of the emission from 4H and 6H devices indicate the presence a broad emission band extending from approximately 500 to 800 nm. We suggest is that this band is due to the emptying and filling of interface traps driven by the transitions between accumulation and inversion. By gating the photodetector, light emission from interface traps in the top half of the bandgap can be separated from the emission from interface traps in the bottom half of the bandgap. While an exact correlation cannot be made between the intensity of the emission spectra and energy distribution of interface traps, comparisons of the 4H and 6H spectra suggest differences and similarities between the distribution of interfaces traps in the 4H and 6H bandgaps. More interface trap recombination is observed in the 4H devices corresponding to the larger Dit measured in the 4H. It is also seen that in both 4H and 6H MOSFETs more light is emitted from transitions that are related to interface traps with states in the upper half of the bandgap. This result is consistent with electrical measurements that show a higher interface trap density in the top half of the bandgap. Finally, comparisons of 4H and 6H polytypes devices indicate that the relative densities of interface traps in the two halves of the bandgap differ in the two polytypes. In the 4H devices, the relative concentration of states in the lower half of the bandgap is larger than that observed in the 6H. In addition to these results, we will discuss the time evolution of the emission spectrum. This work is supported by Office of Naval Research's program for Advanced Electronic Power Systems (AEPS).

11:00 AM

BB8, The Effects of Defects on SiC PIN Diode Operation Examined by Light Emission: *R. E. Stahlbush*[1]; P. J. Macfarlane[1]; A. K. Agarwal[2]; [1]Naval Research Laboratory, Code 6816, 4555 Overlook Ave. S.W., Washington, DC 20375 USA; [2]Cree, Inc., 4600 Silicon Dr., Durham, NC 27703 USA

SiC is an attractive material for fabricating high power devices. Compared to silicon, silicon carbide has a larger bandgap, a higher breakdown field and better thermal conductivity. However, there are obstacles to this new technology. The concentration defects in SiC wafers needs to be

reduced and effects of the defects on devices needs to be determined. In this presentation, the effects of defects on PIN diode operation will be studied by examining light emission. This emission reveals defects affecting both forward and reverse bias operation of the diode. We have examined diodes with an active area of 0.01 cm2 and reverse breakdown voltages in the 1.5 to 2 kV range. A series of guard rings surround the active area. Driving the diodes into reverse breakdown causes avalanching within the bulk. The position of the resulting emission locates the breakdown position. In these diodes, breakdown typically occurs between the edge of the active region and the first guard ring. This is a region at which the electric field peaks. Two different breakdown mechanisms have been observed. In some of the diodes, the breakdown location is fixed due to a defect that locally lowers the breakdown field. In other diodes, the breakdown the location dances from spot to spot. The time scale for the jumping of the breakdown spot ranges from fractions of a second to tens of seconds. In this case, charging and discharging of the overlying oxide layer alters the local electric field causing the breakdown position to jump around. Some diodes exhibit a combination of these mechanisms. Defects also affect the current flow in forward biased diodes. In the devices studied to date, the metal over the p+ anode restricts direct observation to the region outside of the metal contact. Light observed in a band around the contact is not uniform and varied from device to device. The emission pattern is sensitive to the magnitude of the forward current. At lower injection levels emission is less uniform and tends to exhibit local spikes. As the current drops, it appears that the influence of traps increases. This conclusion is supported by the spectrum of the emitted light. As the current increases, a larger fraction of the light is emitted near the SiC bandgap and less of the light is emitted at the lower energies associated with recombination at traps. We will present images of diodes in which there are windows in the contacts allowing light from the whole area under the diode to be imaged. This work is supported by the Office of Naval Research AEPS program.

11:20 AM

BB9, Bipolar Silicon Carbide Power Diodes Realized by Aluminum Implantations and High Temperature rf-Annealing: *M. Lazar*[1]; K. Isoird[1]; L. Ottaviani[1]; M. L. Locatelli[1]; C. Raynaud[1]; D. Planson[1]; J. P. Chante[1]; [1]Centre de Génie Electrique de Lyon (CEGELY), UMR No. 5005-Insa de Lyon, Léonard de Vinci, 20, av. A. Einstein, 69621 Villeurbanne, Cedex, France

Silicon carbide has received an important attention for high-power, high-temperature and high-speed electronic fields. Ion implantation, the only method to locally dope SiC, seems to be a delicate point especially to obtain p-type silicon carbide regions. High temperature post-implantation annealings in particular conditions (high heating ramp, silicon and carbide overpressure) are needed to achieve well activated layers in a well preserved crystalline state. In a first time an optimized post-annealing process was obtained. A SiC dedicated furnace was used to anneal room temperature (RT) and 300°C aluminum (Al) implanted 6H-SiC samples. Recrystallization and surface preserving were investigated by physico-chemical analyses like: Rutherford Backscattering Spectrometry (RBS), X-Ray Photoelectron Spectroscopy (XPS) and Atomic Force Microscopy (AFM). Systematic Secondary Ion Mass Spectroscopy (SIMS) analyses were carried out before and after annealing. Well recrystallized samples were found even if ion implantations (at room temperature) have lead to amorphous layers, in terms of RBS results, with an annealing at 1700°C during 30 min. A relatively important roughness (14.4 nm rms) was found by AFM analyses. SIMS investigations show that the doping profile is preserved and no Al diffusion occurs[1]. Four-point probe measurements prove a high electrical dopant activation, in terms of Al incorporation in SiC active lattice sites. 50% (respectively 100%) activation was found after an annealing at 1700°C during 30 min for RT (respectively 300°C) implanted samples. This process has been applied to fabricate 4H- and 6H-SiC bipolar power diodes, on n-type epitaxial layers purchased from Cree Research (40 µm, 1.1x1015cm-3 epitaxial doping for 4H-SiC wafers and 10 µm, 6x1015cm-3 epitaxial doping for 6H-SiC wafers). A Junction Termination Extension (JTE) structure was chosen after physical and electrical simulations using ISE TCAD and MEDICI program softwares. Several electrical test-structures were added to investigate dopant preservation and activation, the quality of the ohmic contact metallization and lithographic process. Hall effect in a Van der Pauw geometry and TLM (Transmission Line Model) measurements confirm the dopant activation and 5x10-4 cm2 contact resistance was found at 300K for an Al-Ti process metallization on p-type doped zones (4x10-19 cm-3 Al implanted box profile). Forward current density obtained by I-V measurements at 300K on JTE bipolar diodes is 50 A/cm2 at 5V drop voltage. In reverse bias these diodes have shown blocking voltage capabilities up to 1kV for 6H-SiC wafer and 2.3 kV for the 4H-SiC one. [1]M. Lazar, L. Ottaviani, M. L. Locatelli, D. Planson, B. Canut and J. P. Chante: Mater. Sci. Forum 338-342 (1999), 921.

11:40 AM

BB10, Low-Dose Boron and Aluminum P-Type Implants in 4H- and 6H-SiC: *Nelson Saks*[1]; Anant K. Agarwal[2]; Sei-Hyung Ryu[2]; John W. Palmour[2]; [1]Naval Research Laboratory, Code 6813, 4555 Overlook Ave., Washington, DC 20375 USA; [2]CREE, 4600 Silicon Dr., Durham, NC 27703 USA

Aluminum and boron implants for p-type layers in 4H- and 6H-SiC have been characterized with anneal temperatures from 1300 to 1600°C. Previous studies of p-type implantation in SiC have concentrated primarily on high dose (10^15 to 10^16 ions/cm2) implants for low-resistance contacts. Here we study lower dose implants (10^13 to 10^14 ions/cm2) intended for lightly doped layers such as the active regions of high-voltage power devices. SIMS and capacitance-voltage data are used to establish depth profiles for the as-implanted and electrically activated acceptors, respectively. Hall effect measurements are used to characterize free hole density and hole mobility as a function of temperature. Excellent activation of implanted aluminum is found for 1600°C anneals. Activation of boron implants is relatively poor and dose dependent even at 1600°C. The hole mobility is higher in the boron-implanted layers compared to aluminum, suggesting reduced residual implant damage for boron implants.

Session CC: Characterization of Wide Bandgap Semiconductors

Friday AM Room: 155
June 29, 2001 Location: University of Notre Dame

Session Chairs: Bob Vaudo, ATMI, Danbury, CT 06810 USA; Tom Myers, West Virginia University, Phys. Dept., Morgantown, WV 26501 USA

8:20 AM

CC1, UV Optical Gain in GaN Layers and GaN/InGaN Multiple Quantum Wells: *Edmundas Kuokstis*[1]; Jinwei Yang[1]; Jan-Pole Alexis[1]; Grigory Simin[1]; Asif Khan[1]; Michael Shur[2]; Remis Gaska[2]; [1]University of South Carolina, Dept. of Electl. Eng., Columbia, SC 29208 USA; [2]Sensor Electronic Technology, Inc., Latham, NY 12110 USA

We present photoluminescence (PL) and optical gain (OG) spectroscopy results for GaN epilayers and GaN/$In_xGa_{1-x}N$ multiple quantum wells (MQW) grown on sapphire substrates by low-pressure MOCVD. Optical emission from 1-1.5 µm thick GaN layers and GaN/InGaN MQW (4 MQW with the thickness of barriers and wells 4-6 nm) was studied at room temperature using CW (He-Cd, λ = 325 nm) and pulsed excitation (N_2 laser, 337 nm, power density up to 5 MW/cm^2, and ArF eximer laser, 193 nm, power density up to 1 MW/cm^2). Excitation beam was directed nearly perpendicular to the layer surface. PL and OG spectra were measured for two different geometries: (i) "reflection geometry", where optical signal was detected nearly perpendicular to the surface; (ii) "thin strip" technique, where emission was measured from the edge of the sample. In conventional "reflection geometry" and at low excitation levels, typical PL spectra consist of rather broad emission band. In case of GaN it is close to 360 nm, while in case of GaN/InGaN MQW it is located in a spectral region of 360-460 nm depending on the sample structure and x. However, intensity of luminescence for GaN/InGaN MQW was enhanced more than two orders in comparison with thick GaN layers. At higher excitation densities by N_2 laser, the second narrow peak emerged. In GaN it appeared on the long wave side of spontaneous luminescence

band, whereas in GaN/InGaN MQW it was observed on the short wave side. It is attributed to the stimulated emission of spontaneous luminescence. Detailed studies of the stimulated emission point to band-to-band recombination in dense electron-hole plasma as a dominant recombination channel. In order to measure OG coefficient in GaN layers and GaN/InGaN MQW we used "thin strip" technique. The excitation beam of N_2 laser was focused into a thin strip on the surface close to the edge of the samples. The length of the strip was controlled by a special diaphragm and varied from 5 µm to 1000 µm. This allowed us to measure UV light emission intensity as a function of the excited strip length (region with population inversion) and extract OG coefficient. The maximum value of OG for 375 nm wavelength was close to 400 cm^{-1} in GaN layers, and up to 300 cm^{-1} in GaN/InGaN MQW. Note that this value was obtained in GaN for strip length of approximately 200 µm and 500 µm in GaN/InGaN MQW. OG saturation mechanism, which includes non-uniform material composition and partial strain relaxation close to the sample edges will be discussed.

8:40 AM

CC2, Large Field Emission from Heavily Si-Doped AlN and AlxGa1-xN (0.4<x<1): *Makoto Kasu*[1]; Naoki Kobayashi[1]; [1]NTT Basic Research Laboratories, Phys. Sci. Lab., 3-1 Morinosato-Wakamiya, Atsugi, Kanagawa 243-0198 Japan

The negative electron affinity of AlN and $Al_xGa_{1-x}N$ (x>0.75) was reported by Benjamin et al.[1] However, this is still controversial. Further, the field-emission (FE) currents from undoped AlN and $Al_xGa_{1-x}N$ are still low. Although theoretically the Al content, x, dependence and donor-density dependence of FE characteristics in $Al_xGa_{1-x}N$ have been reported,[2] there have been few experimental studies. Recently, we found that for AlN as the Si dopant density (N_{Si}) increased, the threshold electric field for FE decreased and the FE current increased drastically, and observed light emission from phosphors excited by field-emitted electrons.[3] Here we have grown high-quality AlN and $Al_xGa_{1-x}N$, and have used a reliable method to measure FE characteristics. We have obtained FE I-V characteristics for different Al contents, N_{Si}, thicknesses of $Al_xGa_{1-x}N$. We have obtained a FE current density of 66 mA/cm^2 from heavily Si-doped AlN, which is twice that of diamond.[4]Heavily Si-doped AlN and $Al_xGa_{1-x}N$ epitaxial layers were grown on on-axis n-type 6H-SiC (0001) substrates by MOVPE. The sources were trimethylaluminum, trimethylgallium, NH_3, and SiH_4. The N_{Si} was measured by Auger electron spectroscopy and SIMS. FE I-V characteristics were measured using a modified scanning tunneling microscope. The electric field was obtained as a slope of a linear relation between the sample-anode distance for 1 nA and the applied bias. Using this method, we were able to separate the sample-anode bias from the voltage drops in the contact and sample, and, consequently, to obtain the net sample-anode electric field. We have found that as the Al content in $Al_xGa_{1-x}N$ (N_{Si}: $2x10^{20}$ cm^{-3}, thickness: 0.2 µm) increased from x=0.4 to 1, the electric field decreased from 515 to 110 V/µm. This reflects the smaller electron affinity for higher Al content. Next, we have found that as the N_{Si} in AlN (thickness: 0.2 µm) increased from $5x10^{18}$ to $1x10^{21}$ cm^{-3}, the electric field decreased from 240 to 87 V/µm. This dependence agrees with our previous reports.[3]Thirdly, we have found that as the Si-doped (N_{Si}: $1x10^{21}$ cm^{-3}) AlN thickness increased from 0.1 to 0.4 µm, the electric field decreased from 220 to 39.5 V/ µm. This reflects the sharpness of spontaneously-formed ridge structure for the thick Si-doped AlN, as we observed by atomic force microscopy. As a result, for 0.4-µm-thick Si-doped (N_{Si}: $1x10^{21}$ cm^{-3}) AlN, we have obtained a FE current density of 66 mA/cm^2, which is the twice that of diamond.[4] [1]M. C. Benjamin et al., Appl. Surf. Sci. 104/105 (1996) 455; [2]M. S. Chung et al., Appl. Surf. Sci. 146 (1999) 138, J. Vac. Sci. Technol. B18 (2000) 919; [3]M. Kasu et al., Appl. Phys. Lett. 76 (2000) 2910, J. Crystal Growth 221 (2000) 739. [4]W. Zhu et al., Science 282 (1998) 1471.

9:00 AM

CC3, Recombination Mechanisms in AlGaN and Their Effects on the Response of Ultraviolet Detectors: *Jean-Luc Reverchon*[1]; Jean-Yves Duboz[1]; Marie-Antoinette Poisson[1]; [1]Thales, Laboratoire Central de Recherche, Domaine de Corbeville, Orsay 91404 France

AlGaN is now widely studied and used in blue light emitting diodes, blue laser diodes, high power field effect transistors and UV detectors. In the case of UV photoconductors, deep levels in AlGaN lead to a non-ideal behavior, which includes sub-bandgap absorption, nonlinearity and persistent photoconductivity. We present here an experimental analysis of these effects in AlGaN. The AlGaN layer was first studied by photoluminescence (PL). In addition to the usual band edge and yellow band emission, we observed a broad blue band at 3.2eV. This feature is usually ascribed to donor-acceptor pair (DAP) recombinations. Transmission and photoconductivity measurements show a strong band edge absorption at 3.6eV. From 3.4 to 3.5eV, the transmission decreases by 50%, showing a strong residual absorption. This absorption above 3.4 eV could be due to GaN clusters arising from a non-uniform growth. Careful investigations by Xray diffraction, TEM and CL allow to rule out this possibility and to attribute the residual absorption to deep levels in AlGaN. In addition to a shallow donor responsible for the residual n doping, we thus have an acceptor band (A) and a deep donor band (D) at respectively 3.4eV and 0.2eV below the conduction band. The A and D band are full with electrons at thermodynamic equilibrium. However, holes can be created in both bands by photoexcitation, and recombination involving these bands become possible. In particular, electrons can be excited from the A band to the conduction band by photons with energy larger than 3.4 eV. Electrons in the conduction band can now relax towards the A band, and thus have a shorter lifetime, which in turn reduces the detector photoresponse (quenching). We experimentally verified this model. The AC (chopper frequency) response at energies larger than 3.6 eV was measured while a monochromatic DC illumination at lower energies was superimposed on the detector. The AC response drastically diminishes when the DC light energy increases above 3.4eV, as expected from our model. Other experimental observations were the following: The response time decreases with increasing flux; the photocurrent varies non linearly with the incident power P, as P0.4 for power densities in the W/m2 range; The response decay is not exponential, and is faster during light switch on than during light switch off. We performed a numerical simulation of the recombination including band to band transitions, absorption from and relaxation to the A band. All the experimentally observed phenomena could be explained and numerically reproduced by our model and material parameters are reduced.

9:20 AM (Student)

CC4, Characterization of Nitrides by Scanning Kelvin Probe Microscopy: *Goutam Koley*[1]; V. Tilak[2]; Bruce Green[1]; L. F. Eastman[1]; Michael G. Spencer[1]; [1]Cornell University, Sch. of Electl. & Comp. Eng., 401 Phillips Hall, Ithaca, NY 14853 USA; [2]Cornell University, Sch. of Appl. & Eng. Phys., Ithaca, NY 14853 USA

Scanning Kelvin probe microscopy (SKPM) has established itself as a useful tool for characterization of semiconductors. Characterization of p-n junctions, fixed charges on surface, as well as cross-sections of heterostructures have been reported using SKPM. Measurements performed on devices have also opened up new possibilities for characterization and trouble-shooting. SKPM works on the basis of electrostatic interaction between the tip and the sample. The SKPM is usually performed in conjunction with atomic force microscopy (AFM) operated in non-contact mode. The AFM helps in maintaining a constant distance between the tip and the sample. In SKPM operation an ac signal with frequency ω is applied to the tip and the ω-component of the force between the tip and the sample is measured. This force can arise due to the difference in Fermi level of the tip and the sample as well as due to any charge on the sample. An electrostatic potential applied externally to the sample can also be measured accurately by SKPM. III-nitride semiconductors have attracted a lot of interest recently due to opto-electronic and high power microwave applications. In this communication we will report on the characterization of III-nitrides using SKPM. The surface potential of nitride epilayers as well as dislocation induced surface potential variations have been studied. The bare surface barrier height (BSBH) measured on the unintentionally doped n-GaN was ~0.7 eV whereas on n^+ doped GaN was ~0.6 eV. The surface potential variation measured around dislocations was ~0.1-0.2 eV for $Al_{0.35}Ga_{0.65}N$ and ~0.3-0.5 eV for n-GaN. Additionally, measurements were performed on dc biased nitride heterostructure field effect transistor (HFET) devices. Through steady state measurements it was possible to measure the electrostatic potential across a dc biased device along with topography. Transient response of gate pulsed HFETs were also measured between the gate and the drain with an aim of understanding the problem of "current slump" which is quite common for nitride devices. It has been proposed that the charging of the surface states in the ungated and exposed parts of the device causes frequency dependent current slump by reducing the two dimensional electron gas (2º) density at the AlGaN/GaN interface. This is

supported by the experimental observation of improved device performance after surface passivation by silicon nitride. To explain the observed transients we propose that the surface states are charged by electrons tunneling from the gate when it is biased negative, while the discharging of the surface states occurs through thermionic emission when the gate is biased to ground potential. Both the charging and discharging of the surface states are observed by SKPM when the gate is pulsed. The time constant of the observed transients are of the order of ~100 ms. This work is supported by the Office of Naval Research MURI on Polarization Electronics contract no. N00014-96-1-1179, under the direction of Dr. Colin E. C. Wood.

9:40 AM, CC5, Late News

10:00 AM Break

10:20 AM

CC6, Valence-Band Discontinuities in p-InGaN/n-GaN Heterojunction Diodes: *Toshiki Makimoto*[1]; Kazuhide Kumakura[1]; Naoki Kobayashi[1]; Toshio Nishida[1]; [1]NTT, Basic Rsrch. Labs., 3-1 Morinosato, Wakamiya, Atsugi-shi, Kanagawa 243-0198 Japan

The valence-band discontinuity between p-InGaN and n-GaN is one of the important device parameters. For example, in heterojunction bipolar transistors (HBTs), holes should be confined within the base layer using this discontinuity. However, the reported values are rather scattered for nitride semiconductors.[1, 2] One possible reason for this is the influence of piezoelectric charges at hetero-interfaces in the previous reports. In this work, we have evaluated the valence-band discontinuity between p-InGaN and n-GaN using capacitance-voltage (C-V) characteristics of p-InGaN/n-GaN heterojunction diodes. In the previous reports, undoped structures were used to evaluate valence-band discontinuity. In this work, heavily doped p-InGaN layers were used, so piezoelectric charges at InGaN/GaN interfaces are considered to be less effective to the obtained values. Recently, we have reported that Mg-doped InGaN layers show high hole concentrations above $1x10^{18}$ cm^{-3} at room temperature and that In atoms in p-GaN reduce etching damage to form better p-type Ohmic contacts on the etched surface. Using these characteristics along with lower bandgap of InGaN, p-InGaN is considered to be a suitable base material in nitride HBTs. Therefore, we have applied this p-InGaN to a base layer of an InGaN/GaN HBT which showed a current gain of 1.2 at room temperature. To improve the characteristics further, structural parameters such as valence-band discontinuity between p-InGaN and n-GaN should be optimized. The p-InGaN/n-GaN heterojunction diodes were grown on SiC substrates using metalorganic vapor phase epitaxy. The In mole fraction (x) in p-InGaN was changed from 0 to 28%, while Mg and Si doping concentrations were fixed at $3x10^{19}$ cm^{-3} and $2x10^{17}$ cm^{-3} in p-InGaN and n-GaN, respectively. The rectified I-V characteristics showed that the ideality factors are around 2, indicating that tunneling current through the defects is quite low. The diffusion potential was obtained from the relationship between $1/C^2$ and V. Using this diffusion potential and fermi level positions in p-InGaN and n-GaN layers, the valence-band discontinuity was found to be expressed as a following equation. [Valence-band discontinuity] (meV) = 9 x [In mole fraction] (%) The valence-band discontinuity evaluated in this work is lower than that evaluated using photoluminescence characteristics. (13 for the coefficient of In mole fraction in the above equation[2]. References: [1]G. Martin, A. Botchkarev, A. Rockett, and H. Morkoc, Appl. Phys. Lett. 68, 2541 (1996). [2]Ch. Manz, M. Kunzer, H. Obloh, A. Ramakrishnan, and U. Kaufmann, Appl. Phys. Lett. 74, 3993 (1999).

10:40 AM

CC7, Measurement of Carrier Transport in GaN Using GaN Homojunction and AlGaN/GaN Heterojunction p-i-n Diodes: *M. Wraback*[1]; H. Shen[1]; J. C. Carrano[2]; C. J. Collins[3]; J. C. Campbell[3]; C. J. Eiting[3]; D. J. H. Lambert[3]; U. Chowdhury[3]; M. M. Wong[3]; R. D. Dupuis[3]; M. J. Schurman[4]; I. A. Ferguson[4]; [1]US Army Research Laboratory, Sensors & Electron Dev. Direct., AMSRL-SE-EM, 2800 Powder Mill Rd., Adelphi, MD 20783 USA; [2]US Military Academy, Photonics Rsrch. Ctr., West Point, NY 10996 USA; [3]Microelectronics Research Center, Dept. of Electl. & Comp. Eng., The University of Texas at Austin, Austin, TX 78712 USA; [4]Emcore Corporation, Somerset, NJ 08873 USA

We present an optically-detected time-of-flight technique with femtosecond resolution that monitors the change in the electroabsorption due to charge transport in a III-N p-i-n diode, and show how it may be used to determine the electron transit time, electron velocity overshoot, and electron and hole velocity-field characteristics in GaN at room temperature. The samples under study were grown by MOCVD. The experiments were performed using frequency-doubled ultrashort pulses derived from a 250 kHz regenerative amplifier-pumped optical parametric amplifier. For a GaN homojunction p-i-n diode, the experimentally obtained peak steady-state electron velocity of 1.9 X 10^7 cm/sec, corresponding to a transit time of ~2.5 ps across the 0.53 µm depletion region, occurs at 225 kV/cm. While the shape of the electron velocity-field characteristic is in qualitative agreement with theoretical predictions, the peak velocity is lower than expected. Moreover, no transient electron velocity overshoot was observed in this device, a phenomenon that may be attributed to the photo-excitation of the electron-hole pairs in the p-layer near the interface of the p- and i-layers, where they may be influenced by both the electric field nonuniformity associated with the "optical dead space" in the p-layer and the nonuniform field at the p-i junction on the short time scale during which velocity overshoot is expected to occur (< 0.5 ps). These issues have been addressed by performing measurements on an AlGaN/GaN heterojunction p-i-n diode. In this structure the p-layer is an $Al_{0.1}Ga_{0.9}N$ window that allows the electron-hole pairs to be excited directly in the i-region of the diode, where the electric field is expected to be more uniform. In this device, transient electron velocity overshoot is observed at fields exceeding the critical field for intervalley transfer. We have observed a peak electron velocity of ~7.25 X 10^7 cm/s at a field of ~330 kV/cm, limited by the temporal resolution of the experiment (~80 fs). The peak velocity is attained in less than 200 fs, and decays within 1 ps to a steady-state velocity of ~3.3 X 10^7 cm/s in this improved device. At fields greater than ~400 kV/cm the steady-state electron velocity begins to drop, signifying the onset of a negative differential resistance regime. It is important to note that the steady-state velocity in this heterojunction device is more than 1.5 times higher than that observed in the homojunction device at comparable fields in the high field regime. Although the material quality in the heterojunction diode is probably better than that of the previously fabricated homojunction diode, a more important factor in attaining the high steady-state velocity may be the improved lateral uniformity of the electric field in the i-region resulting from the use of a semitransparent p-contact metal covering the entire excitation area.

11:00 AM (Student)

CC8, Nonlinear Piezoelectricity in InGaN/GaN Quantum Wells with Si Doped Barriers: *G. O. Vaschenko*[1]; D. Patel[1]; C. S. Menoni[1]; S. Keller[2]; U. K. Mishra[2]; S. P. DenBaars[2]; C. N. Tome[3]; [1]Colorado State University, Eng. Rsrch. Ctr., Rm. B323, Fort Collins, CO 80523 USA; [2]University of California at Santa Barbara, USA; [3]Los Alamos National Laboratory

InGaN/GaN quantum wells show anomalously small shifts of the photoluminescence (PL) emission peak under applied hydrostatic pressure. In this work we show that this anomaly results from an increase in the piezoelectric field (F_{pz}) in the wells. Our hydrostatic pressure study was done on a set of multiple quantum well samples with 3 nm wells having approximately 13% In composition, and Si doping concentration in the GaN barriers ranging from 10^{17} to $3x10^{19}$ cm^{-2}. In each sample we observe a shift of the photoluminescence (PL) peak with applied pressure which is much smaller than that of the GaN barriers and of a thick InGaN epilayer also characterized in this experiment. The PL peak pressure coefficient of the epilayer is 37 meV/GPa, while that of the quantum wells ranges from 19 to 26 meV/GPa, depending on Si-doping in the barrier. The PL decay measurements show that the well lifetime increases dramatically (by a factor of 6 in the highly doped sample) with th e applied pressure, while it barely changes in the epilayer. The steady state and dynamic behavior of the well PL are indicative of a significant increase of F_{pz}. This increase leads to a continuous red shift of the PL peak emission, which manifests as a lower pressure coefficient. The increase in the lifetime results from the spatial separation of the carriers in the wells leading to a reduction of the electron-hole wavefunction overlap. The variation of the pressure coefficients with doping suggests that F_{pz} is smaller in the highest doped samples due to screening of the field by the free electrons available from the barrier dopant. To calculate the changes of F_{pz} with pressure we first determined the red shift $\Delta E(p)$ of the e1-hh1 QW transition with respect to that of the InGaN epilayer for which $F_{pz} = 0$. We then calculated the field that gives rise to such red shift using the approach described in[1]. Using the values of the $F_{pz}(p)$ determin ed from our experiment, we calculated the pressure dependence of the

lifetime and found that its dramatic increase observed in the experiments is well reproduced. [1]D.A.B. Miller et.al, PRB 32, 1043 (1985).

11:20 AM (Student)

CC9, Advancement in the Electrical Characteristics of AlGaN/GaN Heterostructures Grown by MBE on LiGaO2 Substrates: *Sangbeom Kang*[1]; W. Alan Doolittle[1]; Z. R. Dai[2]; Z. L. Wang[2]; Stuart R. Stock[2]; April S. Brown[1]; [1]Georgia Institute of Technology, Sch. of Electl. & Comp. Eng., MiRC, 791 Atlantic Dr., Atlanta, GA 30332-0269 USA; [2]Georgia Institute of Technology, Matls. Sci. & Eng., 771 Ferst Dr. N.W., Atlanta, GA 30332-0245 USA

$LiGaO_2$ (LGO) is an attractive alterative substrate for III-Nitride growth due to its' small lattice mismatch to GaN. In addition to this, LGO can be readily removed by wet etching, leading to the promise of advanced packaging and device integration via bonding to an appropriate platform. There has been rapid progress in the development of AlGaN/GaN heterostructure field effect transistors (HFETs) on several kinds of substrates, such as sapphire and SiC. Continued improvements in defect minimization, as well as the ability to improve heat removal, will yield higher performance and higher reliability devices. In this study, we present the electrical and structural characteristics of AlGaN/GaN heterostructures grown on LGO substrates. The films were produced by MBE with an rf-plasma nitrogen source. The growth rate was 0.9-1.0 µm/h. All the structures were entirely undoped. The thickness of the GaN layer was varied between 500-800nm, with AlGaN thicknesses of 55nm or 35 nm. The Al composition in th e $Al_xGa_{1-x}N$ cap-layer was varied from 14% to 27%, which was estimated by x-ray diffraction. Hall measurement results show that sheet electron concentrations increase as Al composition increases, as expected. However, the electron mobility did not show a clear dependence on the Al composition. The best electron mobility of this study was obtained with an $Al_{0.26}Ga_{0.74}N$ /GaN heterostructure with a GaN thickness of 770 nm and an AlGaN thickness of 35 nm. The 2° exhibited a 300K mobility of 1365 cm^2Vs (3730 cm^2/Vs at 77K). The sheet electron concentration was 7.7×10^{12} cm^{-2} at 300K and 8.51×10^{12} cm^{-2} at 77K. For the purpose of enhancing the 2° mobility in the AlGaN/GaN heterostructures on LGO, AlGaN/GaN superlattice (SL) nucleation layers were grown before the growth of active device layers. Previous results have indicated that Li impurities (deep acceptors) can diffuse from LGO [Appl. Ph ys. Lett. v74, p3380, 1999]. SIMS analysis indicates that AlGaN/GaN SL layer getters or reduces out-diffused Li impurities from LGO in comparison to structures grown without this blocking layer. Using such buffers, we can achieve good 2° mobilities (~1040 cm^2/Vs with 7.7×10^{12} cm^{-2}) at 300K for a AlGaN/GaN heterostructure with relatively thin a GaN layer of ~ 500nm. AFM was used on a GaN sample with a SL buffer to estimate the density of threading dislocations that intersect the surface. For a 10µm×10µm area, we observe a density of approximately 2-3×10^8 cm^{-2}. High resolution TEM was used to assess the structural characteristics of the films. TEM images show that flat surfaces and interfaces are obtained without the V-defects that were observed in previous samples. However, stacking faults are clearly evident. While Liliental-Weber [Phyica B, v273-274, p124, 1999] have suggested that such stacking faults may result from high concentrations of imp urities, most notably magnesium, the fact that the stacking faults exist in the AlGaN cap layer as well as the buffer layers indicates that the source of the stacking faults may be different in this case. One possible source is the asymmetric strain introduced by the orthorhombic substrate [Sold-State Electron. v44, p229, 2000], leading to rotational forces acting on the nitride film. These forces are likely relieved by the formation of the stacking faults. We also observe in one sample low contrast, threading boundaries, spaced with distances in accordance with ~1% strain. Their density is much higher than the commonly observed threading dislocations. These kinds of high-density boundaries possibly limit the 2° mobility significantly. The measured mobility on this particular sample was ~ 442 cm^2/Vs with sheet electron concentrations of ~ 4.0×10^{12} cm^{-2} at 300K.

11:40 AM

CC10, Transport and Low Frequency Noise Properties of Thin Highly Doped GaN Layers: *Remis Gaska*[1]; Michael S. Shur[2]; A. Dmitriev[3]; S. Rumyantsev[3]; M. E. Levinshtein[3]; J. W. Yang[4]; M. Asif Khan[4]; G. Simin[4]; [1]Sensor Electronic Technology, 21 Cavalier Way, Latham, NY 12110 USA; [2]Sensor Electronic Technology and Rensselaer Polytechnic Institute, CII 9017 CIEEM, Troy, NY 12180 USA; [3]Rensselaer Polytechnic Institute, ECSE & CIEEM, CII9015, Troy, NY, USA; [4]University of South Carolina, Dept. of Electl. Eng., Columbia, SC 29208 USA

We report on transport and low frequency noise properties of thin highly doped GaN layers at room temperature and at elevated temperatures. The experimental studies involved GaN films grown by low pressure MOCVD over sapphire and insulated 4H-SiC substrates using an AlGaN buffer followed by the deposition of approximately one micron thick i-GaN layer. The active GaN layers on top had thickness of 70 nm or less and doped from 5x1017 to 2x1018 cm-3. These layers allowed us to fabricate GaN Highly Doped MESFETs (HDMESFETs) with the maximum drain current over 300 mA/mm. The values of the electron Hall mobility achieved for the layers grown on SiC were approximately 200 cm2/V-s. The values of the electron Hall mobility achieved for the layers grown on sapphire varied from 80 to 100 cm2/V-s. These layers exhibited a record low level of the 1/f noise comparable to that of the best GaN-based HEMTs and more than an order of magnitude better that the results obtained for any other thin GaN films, even those with a considerably higher mobility. We also report on the theoretical calculations of the electron mobility and electron concentration in thin-doped GaN films and consider the effects of the reduced dimensionality on the electron mobility. Our calculations show that two effects are important for the transport properties in thin-doped layers: 1. Electron re-distribution because of the surface depletion and the n+-n junction and 2. Reduced dimensionality effects that, in principle, might start playing a role even when the mean free path for energy relaxation scattering events becomes comparable with the effective thickness of the doped channel. We also compare the temperature dependences of the electron mobility for these doped layers with those for the two-dimensional electrons and show that the mobility of the highly doped layer approaches that of the two-dimensional electron gas diminish at elevated temperatures (close to the device operating temperature). Our device simulations results based on these transpor t data and preliminary experimental results on RF power of GaN HDMESFETs show that HDMESFETs developed on this GaN material might compete with conventional GaN-based HEMTs, especially for short-channel devices and/or at elevated temperatures.

Session DD: Semiconductors: Processing and Oxidation

Friday AM Room: 138
June 29, 2001 Location: University of Notre Dame

Session Chairs: Carol Ashby, Sandia National Laboratories, Albuquerque, NM 87185-1425 USA; Lou Guido, Virginia Tech, Blacksburg, VA 24061 USA

8:20 AM (Student)

DD1, Lateral Oxidation of $AlAs_xSb_{1-x}$ Compounds: *Aaron Maxwell Andrews*[1]; Sheila K. Mathis[1]; Thomas E. Mates[1]; James S. Speck[1]; [1]University of California–Santa Barbara, Matls. Dept., Santa Barbara, CA 93106-5050 USA

Lateral oxidation of AlAs has been shown to enhance the relaxation of $In_{1-x}Ga_xAs$ compressively strained epilayers. The removal of blocking and trailing misfit dislocation cores at the oxidation front result in enhanced threading dislocation mobility and furthered relaxation. For films grown beyond the equilibrium critical thickness (h_c), we have previously demonstrated additional strain relief of ~0.5% after lateral oxidation. The goal in the current study is to produce epilayers with a 6.1 Å lattice parameter using common substrates. InP has the largest lattice parameter of readily available substrates. The AlAsSb alloy can be grown to the InP lattice parameter and beyond, but oxidation of AlAsSb results in a metallic Sb float layer and a nonplanar free surface. The original AlAsSb shrinks after oxidizing, AlO_x. The formation of the Sb float layer increases the total thickness. Recently, however, Salesse et al. (Appl. Surf. Sci. 161, 426 (2000)) reported that the addition of methanol during wet oxidation of n-type AlAsSb lattice matched to InP reduces the amount of

Sb and As in the oxide and possibly eliminates the Sb float layer. Before using InP substrates, the effect of methanol on the oxidation of unintentionally doped $AlAs_xSb_{1-x}$ compounds was investigated by strained growth on GaAs substrates. Using MBE growth, A 2000 Å oxidation layer was lattice matched, $AlAs_{0.804}Sb_{0.196}$, to the 3000 Å $In_{0.25}Ga_{0.75}As$ capping layer. This is approximately a 1.9% mismatch and at this thickness the films were ~85% relaxed. Both mesas and stripes were etched to expose the oxidation layer. The layers were oxidized in a furnace from 300 to 400°C with a water:methanol mixture of 1:0, 3:1, 1:1, 1:3, and 0:1 heated to 90°C. At 400°C the oxidation rate of AlAs, $AlAs_{0.8}Sb_{0.2}$, and $AlAs_{0.56}Sb_{0.44}$ in pure water was 1.1, 2.0, and 4.5 mm/min. The oxidation rate increases with increased Sb concentration. Introduction of methanol to the wet oxidation of these layers resulted in a 50% decrease in oxidation rate of for 3:1 methanol:water mixtures at 400°C and thus counterbalances the increasing oxidation rate with increasing Sb content in the Al-containing layers. The films did not oxidize in pure methanol. Most importantly for these studies, oxidation in the mixed water/methanol mixture resulted in a significant reduction in the surface rippling and delamination of the cap layer. Selective area Secondary Ion Mass Spectrometry (SIMS) with an oxygen beam showed that there was Sb segregation to the upper and lower oxide interfaces. There was residual Ga in the oxide and the As and Sb levels were below detection limits. We will present detailed studies of the effects of oxidation environment on strain relaxation of InGaAs layers grown AlAsSb oxidation layers.

8:40 AM (Student)

DD2, Protection of Compliant $In_{0.25}Ga_{0.75}As$/GaAs Structures During Lateral Oxidation Using an Amorphous InGaP Layer: *Gregory W. Pickrell*[1]; John H. Epple[1]; K. L. Chang[1]; K. Y. Cheng[1]; K. C. Hsieh[1]; [1]University of Illinois, Electl. & Comp. Eng., Microelect. Bldg., 208 N. Wright St., Urbana, IL 61801 USA

Interest in compliant epitaxy techniques has grown as the need for substrates with different lattice-constants has increased. Important optical and transport devices could be realized using materials with lattice-constants between those of GaAs and InP. One method of realizing these materials involves the growth of a strained InGaAs layer on an underlying AlGaAs layer followed by lateral oxidation to relax the top layer[1, 2]. While this technique has proven successful, it is limited by the damage caused to the top InGaAs layer during the oxidation process. Using very-low-temperature (VLT) molecular beam epitaxy (MBE) growth techniques, an amorphous InGaP layer was deposited to protect the surface during post-growth oxidation procedures. Amorphous InGaP was used because of the availability of a selective etch to remove the layer after processing. Also, the oxidation rate of InGaP is slow as compared to materials such as GaAs. In addition, this method has the benefit that the amorphous layer has no fixed lattice constant, which requires less compositional control, as opposed to techniques involving single-crystal protection layers. Finally, this technique has an added advantage over other amorphous protective layers, such as silicon dioxide, because of the reduced thermal stresses involved with the VLT process. The oxidized structures consisted of single crystal $In_{0.25}Ga_{0.75}As$ grown on an underlying AlGaAs layer, then capped with the thin amorphous InGaP layers of varying thicknesses. The $In_{0.25}Ga_{0.75}As$ grown in this study had low threading dislocation (TD) densities (~10^7 cm^{-2}) due to the choice of growth parameters[3]. In addition, there is a noticeable reduction in TD density due to the lateral oxidation process[1, 4]. The characteristics of the amorphous InGaP layers were investigated, including the effects of phosphorus overpressure during growth on the protective ability of the InGaP layer. Also examined was the oxidation rate of the amorphous InGaP layers as compared to single crystal InGaP and GaAs. In addition, the effects of the InGaP layer thickness on the threading dislocation density of the $In_{0.25}Ga_{0.75}As$ layers were explored. With improved material quality, subsequent regrowths should show improved characteristics, possibly allowing the fabrication of high-quality devices. Additionally, the amorphous protection layer is a versatile technique that can be used in multiple applications and other material systems. [1]K. L. Chang, J. H. Epple, G. W. Pickrell, H. C. Lin, K. Y. Cheng, and K. C. Hsieh, J. Appl. Phys., 88, 6922 (2000). [2]P. Chavarkar, L. Zhao, S. Keller, A. Fisher, C. Zheng, J. S. Speck and U. K. Mishra, Appl. Phys. Lett., 75, 2253 (1999). [3]G. W. Pickrell, K. L. Chang, J. H. Epple, K. Y. Cheng and K. C. Hsieh, J. Vac. Sci. Tech. B., 18, 2611 (2000). [4]S. K. Mathis, P. Chavarkar, A. M. Andrews, U. K. Mishra, J. S. Speck, J. Vac. Sci. Tech. B., 18, 2066 (2000).

9:00 AM (Student)

DD3, Structural Instability of Wet Oxidized GaP and $Al_{0.4}Ga_{0.6}P$: *Kuo-Lih Chang*[1]; John H. Epple[1]; Hung-Cheng Lin[1]; K. Y. Cheng[1]; K. C. Hsieh[1]; [1]University of Illinois, Electl. & Comp. Eng., 208 N. Wright St., Microelect. Lab., Urbana, IL 61821 USA

Since its discovery in 1990, the study of native oxide formed by wet vapor oxidation of crystalline Al-bearing compound semiconductors has been used in many applications ranging from electronic to optical devices. Most studies focused in As-based Al-bearing compounds. We have found that wet oxidation of single crystal GaP at 650°C for more than 6 hours leads to the formation of monoclinic polycrystalline $GaPO_4 \cdot 2H_2O$ with cracks. In contrast, wet oxidation of $Al_{0.4}Ga_{0.6}P$ epilayer at 650°C up to 24 hours gives rise to a smooth amorphous oxide without cracks. In this work, the microstructure stability of monoclinic polycrystalline $GaPO_4 \cdot 2H_2O$ and amorphous AlGaP oxides subject to ampoule-seal annealing and electron irradiation is investigated. Wet oxidation of GaP substrates and epitaxial AlGaP layers was performed in an open tube furnace, supplied with water vapor using nitrogen as a carrier gas at 85°C. Samples were oxidized for 24 hours at 650°C and further annealed at 650°C for 18 hours in a sealed ampoule. Cross-sectional transmission electron microscopy (XTEM) and energy dispersive x-ray spectroscopy (EDAX) are used to determine the microstructure and composition variation. The oxidized $Al_{0.4}Ga_{0.6}P$ film undergoes a structural change from amorphous to polycrystalline as verified by TEM during ampoule-seal annealing. The diffraction patterns suggest that polycrystalline oxide matches with hexagonal $GaPO_4$ or $AlPO_4$ (a=4.902 Å for $GaPO_4$ or 5.029 Å for $AlPO_4$, and c=11.05 Å). In this experiment, EDAX has been used to study the variation of oxygen and phosphorous near the oxidation front. A small amount of oxygen and phosphorous are found in the unoxidized region near the oxidation front of the AlGaP oxide. In comparison, when GaP is oxidized, there is no apparent phosphorous loss in the oxide and no phosphorous accumulation in the unoxidized region. Therefore, the extra phosphorous seen in the unoxidized AlGaP near the oxide front is attributed to phosphorous release from AlP during oxidation. Consequently, the chemical reaction of the wet oxidation of AlP is believed to be similar to that of AlAs, indicating that some phosphorous in AlP forms volatile P_2O_5 or elemental phosphorous either escaping from the sample or diffusing deeper into the substrate. During ampoule-seal annealing, the GaP wet oxide remains monoclinic $GaPO_4 \cdot 2H_2O$. The structural stability no longer prevailed when the sample was subjected to electron beam bombardment. The crystalline $GaPO_4 \cdot 2H_2O$ deteriorated to become amorphous as seen when the diffraction spots disappear with an increasing exposure of electron beam. In contrast, the hexagonal $AlGaPO_4$ oxide exhibits a stronger structural stability against radiation damage.

9:20 AM

DD4, Properties of InAlP Native Oxides Supporting MOS Inversion-Layer Behavior: *Pedro J. Barrios*[2]; Douglas C. Hall[1]; Uttiya Chowdhury[3]; Russell D. Dupuis[3]; Jacek B. Jasinski[4]; Zuzanna Liliental-Weber[4]; Thomas H. Kosel[1]; Gregory L. Snider[1]; [1]University of Notre Dame, Dept. of Electl. Eng., 260 Fitzpatrick Hall, Notre Dame, IN 46556-5637 USA; [2]National Research Council, Inst. for Microstruc. Scis., Ottawa, Ontario K1A 0R6 Canada; [3]The University of Texas at Austin, Microelect. Rsrch. Ctr., PRC/MER-R9900, Austin, TX 78712 USA; [4]Lawrence Berkeley National Laboratory, 1 Cyclotron Rd., Berkeley, CA 94720 USA

GaAs remains the most widely employed semiconductor for high-speed electronic applications due to its crystal growth and processing maturity, and wide array of compatible, high electron mobility alloys of varying bandgap that can be grown epitaxially on its surface. However, its incapacity to produce a native oxide of electrical characteristics similar to those of SiO_2 on Si, has hindered its development in low-power applications. Native oxides produced by the wet oxidation of epitaxial AlGaAs suffer from high leakage currents and As-related traps. However, wet thermal native oxides of As-free $In_{0.485}Al_{0.515}P$ (lattice matched to GaAs) have been found to have excellent insulating properties and may provide a viable oxide for III-V MOS applications.[1,2] Two ~63 nm thick InAlP films, both with and without a 10 nm InGaP oxidation barrier, are grown by MOCVD on GaAs and surface-oxidized in water vapor (500°C, 30-120 min). Fully oxidized (60 min), the films expand to 110 nm as revealed by transmission electron microscopy (TEM) and variable-angle spectroscopic ellipsometry (VASE) measurements. Upon etching one

oxide film back to 49 nm for more direct comparison to oxidized AlGaAs samples, the leakage increased only slightly (2-3X) to ~6e-10 A/cm^2 at 5V, still about 4 orders of magnitude less than our best leakage current in comparable thickness $Al_{0.98}Ga_{0.02}As$ native oxides. Breakdown fields for these thin InAlP native oxides are in the 5 MV/cm range, more than 1.5 times higher than our AlGaAs oxides and similar to those reported for deposited Ga2O3(Gd2O3).[3] However, leakage was found to increase significantly (to ~1.6e-2 A/cm^2) for an oxide film etched to ~25 nm, exposing a region which TEM imaging shows is filled with higher density precipitates. We have reported[2] that high-frequency (1 MHz) and quasi-static C-V measurements on illuminated InAlP oxide MOS capacitors show clear signs of an inversion layer, dependent on oxidation time (optimal at 60 min), suggesting a relatively clean interface and possibly unpinned Fermi level. TEM studies show the oxidation front stopping within the InAlP just above the underlying interface in samples with or without an InGaP barrier, providing a clean semiconductor heterointerface at which the inversion layer likely forms. While unprotected GaAs oxidizes relatively quickly at these temperatures, its oxidation appears to be prevented (or greatly retarded) by the InAlP oxide "cap". In contrast, the porous AlGaAs native oxides do not prevent GaAs oxidation. The InAlP oxide thus appears sufficiently dense (consistent with the observed diffusion-limited oxidation kinetics) to prevent the outdiffusion of Ga and As, as necessary for GaAs oxidation. Finally, TEM imaging shows that InAlP oxides on structures with the InGaP barrier layer have much smoother interfaces and greater thickness uniformity. This work was supported by AFOSR. [1]Adrian L. Holmes, Ph.D. Dissertation, The U. of Texas at Austin, December 1999; [2]P. J. Barrios, D. C. Hall, G. L. Snider, T. H. Kosel, U. Chowdhury and R. D. Dupuis, in State-of-the-Art Program on Compound Semiconductors (SOTAPOCS XXXIV), 199th Meeting of The Electrochemical Society (Washington, DC, March 25-30, 2001); [3]M. Hong, J. Kwo, A. R. Kortan, J. P. Mannaerts, and A. M. Sergent, Science 283, 1897 (1999).

9:40 AM

DD5, Deep Oxidation of AlGaAs Heterostructures for Strongly-Confined Optical Waveguides: Yong Luo[1]; *Douglas C. Hall*[1]; [1]University of Notre Dame, Dept. of Electl. Eng., 260 Fitzpatrick Hall, Notre Dame, IN 46556-5637 USA

Impurity-induced layer disordering (IILD), when used in conjunction with wet thermal oxidation to first intermix fast (high x) and slow (low x) oxidizing layers, has been shown to enable deep oxidation through a conventional $Al_xGa_{1-x}As$ quantum well heterostructure (QWH) for the fabrication of low-loss, high-index-contrast, tightly-curved buried channel waveguides (WGs).[1] Without the IILD step, higher x confinement layers typically oxidize laterally beneath the mask, pinching off the current path to the active stripe before oxidation can proceed downward through the lower x WG layers. Photon-enhanced anisotropic oxidation along p-n junctions has also been observed, presenting an additional obstacle to deep oxidation of non-disordered heterostructures.[2] We report here the achievement of deep-oxidation, avoiding these problems without use of the IILD process, by applying a process gas modification which substantially decreases the oxidation rate selectivity between high and low Al composition AlGaAs. Normally, ultra high purity (UHP) N_2 is used as the H_2O carrier gas during the wet thermal oxidation of AlGaAs. We have previously investigated in detail how oxidation rates, oxide refractive index and surface roughness depend upon added O_2 concentration (0-5% O_2 to N_2 ratio) during the wet oxidation of $Al_xGa_{1-x}As$ ($x \leq 0.8$).[3] Due to a proportionately greater rate enhancement for low x materials, the rate selectivity between high and low x AlGaAs is substantially reduced. For example, at 450°C the rate selectivity R(x=0.8)/R(x=0.3) decreases from (30.2 nm/min)/(1.77 nm/min)=17.1X in UHP N_2 to 43.2/17.9=2.4X with the addition of 7000 ppm O_2 to N_2. We present here the application of this rate selectivity modification to the fabrication of buried-channel index-guided WGs. We utilize a conventional separate-confinement QWH laser diode structure grown by MOCVD: a 10 nm GaAs QW sandwiched by two undoped 75 nm $Al_{0.2}Ga_{0.8}As$ waveguiding layers and p-type upper and n-type lower $Al_{0.8}Ga_{0.2}As$ current confinement layers of thickness around 1 μm, with a 50 nm p^+ cap layer. Wet oxidation of this heterostructure at 450°C is compared for different times with both ridge and planar geometries and with both UHP N_2 and 7000 PPM O_2+N_2. For planar structures, a 7-8 μm Si_3N_4 masking stripe is used to protect the GaAs cap layer. With UHP N_2, SEM micrographs reveal that in 90 min the oxidation front progresses laterally 2.1 μm under the mask, but barely penetrates into the upper x=0.2 WG layer. In contrast, in 50 min with added O_2 and lateral oxidation of 2.6 μm, the oxide penetrates through the WG to a depth of 1.3-1.5 μm, simply forming an index-guided WG with strong optical confinement. Penetration is deeper under the nitride mask edge, suggesting a stress or defect-related oxidation enhancement. For both planar and ridge geometries, with and without O_2 addition, we observe little to no anisotropic oxide "spike" formation as seen in Ref.[2], suggesting that effect may be growth dependent and not a fundamental limitation for formation of deep-oxide waveguides. The ability to oxidize through a complete AlGaAs heterostructure WG with a simple one step process enables new possibilities for III-V integrated optics and optoelectronics. This research was supported by NSF. [1]M. R. Krames, A. D. Minervini, and N. Holonyak, Jr., Appl. Phys. Lett. 67, 73 (1995); [2]S. A. Maranowski, N. Holonyak, Jr., T. A. Richard, and F. A. Kish, Appl. Phys. Lett. 62, 2087 (1993); [3]Y. Luo, D. C. Hall, B. Olga, and H. Hou, 42nd Electron. Mat. Conf. (Denver, CO, 2000), paper F2.

10:00 AM (Student)

DD6, Microwave Annealing for Ultra-Shallow p+-n Junctions: *Taras Kirichenko*[1]; Puneet Kohli[1]; Swaroop Ganguly[1]; Hong-Jyh Li[1]; Sanjay Banerjee[1]; Mihail Shevelev[2]; E. Graetz[3]; [1]University of Texas at Austin, Microelect. Rsrch. Ctr., 10100 Burnet Rd., Bldg. 160, Austin, TX 78712 USA; [2]Gyrotron Technologies, Inc., Bristol, PA 19007 USA; [3]International SEMATECH, Austin, TX 78741 USA

A novel semiconductor annealing technique, using a microwave gyrotron source is proposed. We investigated the formation of ultra-shallow junctions by microwave processing of ultra-low energy, high dose B and BF2 implanted source/drain junctions in Si. A high-frequency, high-power source a microwave electromagnetic radiation based on a cyclotron resonance maser, called a gyrotron, is used for the annealing. The two most important figures of merit to be considered when evaluating the efficacy of doping and annealing strategies for fabrication of source/drain extension regions are the sheet resistance and the junction depth. While there exists a trade-off between these two quantities, one must improve both simultaneously when scaling down device dimensions. For next-generation ultra-large scale integration (ULSI) devices, the International Technology Roadmap for Semiconductors (ITRS) roadmap demands ultra-shallow junctions, and, at the same time, low sheet resistances which may be obtained only by achieving active carrier concentrations above the B solid solubility limits for p+/n junctions. It is becoming increasingly clear that simply reducing the energy of conventional beam line implants, and the thermal budget of rapid thermal annealing (RTA) is not sufficient to achieve low resistance source/drain junctions. Transient enhanced diffusion (TED) of B, and to a lesser extent As, as well as B-enhanced diffusion, which occurs as the doping in the source/drain regions is increased to reach the low source/drain series resistance targets, are important. The critical importance of control of the annealing ambient is emphasized by the observation of oxidation-enhanced diffusion of B and As. The upper limit of active dopant concentration that can be achieved conventionally is limited by solid solubility. This is especially problematic for acceptors, where the highest solid solubility (active peak concentration for B ~ 1E20/cm3 at 950-1000ºC) is too low. Therefore it is important to examine doping and annealing techniques that could potentially exceed this thermodynamic equilibrium solid solubility limit. A study of B/BF2 implants at ultra-low energy (300eV and 500eV) and high doses (1E15/cm2 and 5E15/cm2) into Si was carried out. The samples were annealed by a gyrotron beam. There appears to be evidence for electromagnetic field-dependent activation of dopants. The activation levels achieved exceed the levels reported by thermal means at the corresponding temperatures. We conjecture that coupling between the electromagnetic radiation and the implanted silicon lattice might lead to a reduction in TED by inhibiting dopant-interstitial pairing, thus giving rise to an "athermal" annealing mechanism. Secondary ion mass spectrometry (SIMS) was used to examine the impurity profile after ion implantation and diffusion. Spreading resistance profiling (SRP) was used to examine the activated dopant profile. We observed the active B concentrations as high as 1E20/cm2 for the annealing temperatures not exceeding 800ºC. Plan-view transmission electron microscopy (TEM) was used to confirm very low defect densities in the substrate.

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