2003 Electronics Materials Conference Grid

	WEDNESDAY, JUNE 25TH		THURSDAY, JUNE 26TH		FRIDAY, JUNE 27TH	
	AM	PM	AM	PM	AM	PM
Ballroom Center	**EMC Plenary Lecture/Student Awards**	**REGISTRATION** 3:00PM–5:00PM, Tuesday, June 24, 2003, Olpin Union Building 7:30AM–5:00PM, Wednesday, June 25, 2003, Olpin Union Building 7:30AM–4:00PM, Thursday, June 26, 2003, Olpin Union Building 7:30AM–10:00AM, Friday, June 27, 2003, Olpin Union Building			**EXHIBITS** 9:15AM–4:00PM & 7:00PM–9:00PM, Wednesday, June 25, 2003 9:00AM–4:00PM, Thursday, June 26, 2003	
101	Session D. Spin Dependent (or Spintronic) Electronic Materials - I	Session K. Spin Dependent (or Spintronic) Electronic Materials - II Session L. Non-Destructive Testing and In-Situ Monitoring				
102	Session E. III-V Low Dimensional Structures	Session M. Metal Contacts to Semiconductors				
Auditorium	Session F. Materials Integration I: Wafer Bonding and Alternative Substrates	Session N. Materials Integration II: Wafer Bonding and Alternative Substrates	Session U. SiC: Growth and Characteriaztion	Session BB. SiC: Defects, Processing and Devices	Session HH. Narrow Bandgap Nitrides and Arsenides	
Ballroom Center	Session A. Nanoscale Characterization	Session G. Nitrides: Advanced Characterization	Session O. Nitrides: Defect Reduction and Epitaxy	Session V. UV and Visible Nitride Emitters	Session CC. Nitrides: Substrates and Properties	
Ballroom East	Session B. Semiconductors: Processing and Oxidation	Session H. Epitaxial Oxide and Oxidation	Session P. Epitaxy I: Growth and Characterization	Session W. Epitaxy II: Metamorphic Growth and Integration	Session DD. Epitaxy III: Devices	
Ballroom West	Session C. Si-Based Heterojunction Growth and Characterization	Session I. Low Dimensional Structures for Devices Session J. Low Dimensional Device Structures	Session Q. Materials Issues for Organic Optoelectronics and Transistors	Session X. Narrow Bandgap Antimonides and Arsenides		
Panorama East			Session T. Contacts to Group III Nitrides	Session AA. AlGaN/GaN HEMTs: Growth		
Saltair	Session VI: Jt. DRC/EMC Invited Session: Carbon-Based and Nanowire Devices	Session VII.A: Jt. DRC/EMC Session: Carbon-Based and Molecular Electronic Devices Session VIII: Jt. DRC/EMC Invited Session: Plastic Electronics	Session S. High K Dielectrics - I	Session Z. High K Dielectrics - II	Session GG. AlGaN/GaN HEMTs: RF Dispersion, Processing Effects, and Novel Gate Oxides	
Theatre			Session R. Nanoscale Fabrication and Self-Assembled Systems	Session Y. Molecular Electronics and Nanotubes	Session EE. Low Dimensional Structures: Quantum Dots and Wires Session FF. Si/Ge Low Dimensional Structures	

2003 EMC At-A-Glance

Wednesday Morning, June 25, 2003

8:20 AM EMC PLENARY LECTURE/STUDENT AWARDS

Room: Center Ballroom

Plenary Speaker: Stephen Forrest
Princeton University, Department of Electrical Engineering, EQUAD B301, Princeton, NJ 08544 USA

Topic: "Organic Electronics: Is it for Real or is it Just the Latest Fad?"

Break: 9:20 AM–10:00 AM

Joint DRC/EMC Invited Session VI: Carbon-Based and Nanowire Devices

10:00 AM **VI.-1 Invited, Functional Semiconductor Nanowires and Their Optical Properties**
..... P. Yang

10:40 AM **VI.-2 Invited, Pushing to the Performance Limit of Carbon Nanotube Electronics**
..... H. Dai

11:20 AM **VI.-3 Invited, Carbon Nanotube Field-Effect Transistors–An Example of an Ultra-Thin Body, Schottky Barrier Device**
..... J. Appenzeller

Session A: Nanoscale Characterization

10:00 AM **A1 (Student), Cross-Sectional Scanning Tunneling Microscopy and Spectroscopy of InGaP/GaAs Heterojunctions**
..... Yang Dong

10:20 AM **A2 (Student), Local Conductivity and Surface Potential Measurements of Mg-Doped p-GaN**
..... Blake S. Simpkins

10:40 AM **A3, Electrical Characterisation of Self-Assembled Nanoparticle Coated Crystals**
..... Werner Prost

11:00 AM **A4, Near-Field Magneto-Photoluminescence of Quantum-Dot-Like Composition Fluctuations in GaAsN and InGaAsN Alloys**
..... J. L. Merz

11:20 AM **A5, Structural/Compositional Characterization of ONO Stacks on Silicon**
..... Igor Levin

Session B: Semiconductors: Processing and Oxidation

10:00 AM **B1 (Student), High Resolution Secondary Ion Mass Spectrometry Analysis of Vertical Cavity Surface Emitting Lasers**
..... Yong K. Kim

10:20 AM **B2 (Student), Improving Oxidation Uniformity for Uniform Performance of Large VCSEL Arrays**
..... Zhi-Jian Wei

10:40 AM **B3, Strain and the Thermodynamics of Buried AlGaAs Layer Oxidation**
..... Alexana Roshko

11:00 AM **B4 (Student), Completely Pinning-Free Surface Passivation of GaAs (001) Surfaces by Forming Si and GaN Interface Control Layers on Ga-Rich (4x6) Surface**
..... Sanguan Anantathanasarn

11:20 AM **B5 (Student), Chemical and Electronic Studies of GaSb Surface Passivation Based on Non-Aqueous Sulfide Solutions**
..... Zhiyan Liu

11:40 AM **B6, Late News**

2003 EMC AT-A-GLANCE

Wednesday Morning, June 25, 2003

Session C: Si-Based Heterojunction Growth and Characterization

10:00 AM C1, Fermi Level Stabilization in Plastically Strained SiGe Alloys
..... P. N. Grillot

10:20 AM C2, Fabrication of Relaxed SiGe-On-Insulator Substrates by Oxygen Implantation into Pseudomorphic SiGe/Si Heterostructure
..... Zhenghua An

10:40 AM C3 (Student), Impact of Ion Implantation Damage and Thermal Budget on Mobility Enhancement in Strained Si n-MOSFETs
..... G. Xia

11:00 AM C4, Impact of Virtual Substrate Ge Composition on Strained Si MOSFET Performance
..... Sarah H. Olsen

11:20 AM C5 (Student), Very High Hole Mobility Strained Si/SiGe Layers for p-Type Heterostructure-Based PMOS Devices at Room and Low Temperatures
..... Corina Elena Tanasa

11:40 AM C6, Partially- and Fully-Depleted Strained Si/Si1-yGey MOSFETs Fabricated on Relaxed Si1-xGex-On-Insulator (SGOI)
..... Zhiyuan Cheng

Session D: Spin-Dependent (or Spintronic) Electronic Materials - I

10:00 AM D1, High Efficiency Spin Injection from a Ferromagnetic Metal into a Semiconductor Through Fe/InAs Junction
..... Kanji Yoh

10:20 AM D2 (Student), $Fe_{1-x}Co_x$/GaAs Spin Polarized Transport Devices: Growth, Characterization, and Transport Measurements
..... B. D. Schultz

10:40 AM D3, On Spin Loss During Optical Spin Injection in ZnMnSe/CdZnSe Quantum Structures
..... I. A. Buyanova

11:00 AM D4, Ultrafast Spin Dynamics Monitored by Pump-Probe Second Harmonic Generation
..... Norman H. Tolk

11:20 AM D5, Anisotropy of Spin Dephasing Rates in Quantum Wires
..... Supriyo Bandyopadhyay

11:40 AM D6 Cancelled, Comparison of Electron Spin Relaxation Times in GaAs and GaN
..... Srini Krishnamurthy

Session E: III-V Low Dimensional Structures

10:00 AM E1, Controlling the Electronic States of Self-Assembled InAs Quantum Dots by using InGaAs Layer
..... Jin Soo Kim

10:20 AM E2, Photoexcited Carrier Dynamics in Self-Assembled InAs/AlAs Quantum Dots
..... Z. Ma

10:40 AM E3 (Student), Growth of Uniform InAs Quantum Dots on Strain Modulated InGaAs Superlattice
..... Zhenhua Zhang

11:00 AM E4 (Student), Effect of InAlGaAs Lateral Potential Confinement Layer on InAs Quantum Dot Infrared Photodetectors
..... Eui-Tae Kim

11:20 AM E5, Determination of Subband Energy Levels of DQW AlGaAs Lasers by Photo-Reflectance and Self-Excited Electron Raman Scattering at 300K
..... Wataru Susaki

2003 EMC AT-A-GLANCE

Wednesday Afternoon, June 25, 2003

Session F: Materials Integration: Wafer Bonding and Alternative Substrates - I

Wednesday Morning cont...

10:00 AM **F1 (Student), Heterogeneous Integration of (In,Ga)N Light-Emitting Diodes, CdSxSe1-x Filters and Silicon Photodetectors for Fluorescence-Detecting Microanalytical Systems**
..... ZhongSheng Luo

10:20 AM **F2, Dielectrophoretic Manipulation of Analytes for Biological Assay Applications**
..... Conrad David James

10:40 AM **F3, Characteristics of Si Thin Films Transferred onto Glass by Ion-Cut Employing Pulsed and Direct-Current (DC) Plasma Immersion Ion Implantation**
..... F. Lu

11:00 AM **F4, Fabrication of Hybrid Distributed Bragg Reflectors using Metallic Wafer Bonding**
..... Hung-Cheng Lin

11:20 AM **F5, Late News**

Joint DRC/EMC Session VII.A: Carbon-Based and Molecular Electronic Devices

1:30 PM **VII.A-1, Selective Growth and Electrical Properties of Single-Walled Carbon Nanotubes**
..... R. Zhang

1:50 PM **VII.A-2, Negative Differential Resistance in a Bilayer Molecular Junction**
..... J. Le

2:10 PM **VII.A-3, Fabrication and I-V Characterization of Carbon Nanotube Single Electron Transistor Operated at Room Temperature**
..... T. Kamimura

2:30 PM **VII.A-4, Random Networks of Single-Wall Carbon Nanotubes: Electronic and Sensor Applications**
..... E. S. Snow

3:10 PM **Break**

Joint DRC/EMC Invited Session VIII: Plastic Electronics

3:30 PM **VIII.-1 Invited, Large Area Printing of Organic Transistors**
..... G. B. Blanchet

4:10 PM **VIII.-2 Invited, Stretchable and Deformable Macroelectronics**
..... S. Wagner

4:50 PM **VIII.-3 Invited, Nanoscale Transport in Organic Transistors and LEDs**
..... J. Zaumseil

Session G: Nitrides: Advanced Characterization

1:30 PM **G1, Dopant-Defect Interactions in GaN and Related Alloys**
..... P. N. Grillot

1:50 PM **G2 (Student), Investigation of Deep Level Luminescence at 2.45 eV in InGaN:Mg**
..... Bing Han

2:10 PM **G3, Microcatholuminescence Spectroscopy of Localized Electronic States at Photoelectrochemically-Etched GaN Whiskers**
..... Xiaoling Sun

2:30 PM **G4, Microstructural and Optical Properties of Heteroepitaxial GaN Grown on AlN Buffers on SiC**
..... B. J. Skromme

2:50 PM **G5 (Student), Atomic Ordering in InGaN Alloys**
..... Manu Rao

3:10 PM **Break**

3:30 PM **G6, Electroreflectance Studies of Stark-Shifts and Polarization-Induced Electric Fields in InGaN Quantum Wells**
..... Robert J. Kaplar

3:50 PM **G7, Spectral Ellipsometry Characterization of MBE Grown GaN on 4H SiC**
..... Todd M. Holden

4:10 PM **G8, Universal Theory for the Determination of Both Screw and Edge Dislocation Densities for GaN and Related Materials using High Resolution X-Ray Diffraction**
..... Simon Bates

4:30 PM **G9 (Student), Characterization of Multiple Carriers in GaN and InN Epilayers Using Variable Magnetic Field Hall Measurements**
..... Craig H Swartz

4:50 PM **G10 (Student), Characterization of Post-Epilayer Growth Anodized GaN/SiC Heterostructures**
..... Jie Bai

2003 EMC AT-A-GLANCE

Wednesday Afternoon, June 25, 2003

Session H: Epitaxial Oxides and Ferroelectrics

1:30 PM **H1 Invited, X-Ray Imaging of Thin Films and their Interface with Substrate with Sub-Angstrom Resolution**
..... Y. Yacoby

2:10 PM **H2, Lanthanum Aluminate on Silicon for Alternative Gate Dielectric Applications**
..... L. F. Edge

2:30 PM **H3 (Student), Epitaxial MgO with a SrO Buffer Layer on Si(001) by Molecular Beam Epitaxy**
..... Feng Niu

2:50 PM **H4 (Student), Integration of $BaTiO_3$ Ferroelectric Thin Films with GaAs Using MgO and Al_xO_y Buffer Layers**
..... Timothy Murphy

3:10 PM **Break**

3:30 PM **H5, Structural and Dielectric Characterization of Epitaxial Rare-Earth Scandate Thin Films**
..... J. Schubert

3:50 PM **H6, Thermodynamics of Cavity Nucleation in the Ion-Implanted Single Crystal BaTiO3 for Ferroelectric Thin Film Layer Transfer**
..... Young-Bae Park

4:10 PM **H7, Electric Field Cycling-Induced Oxygen Tracer Drift in PZT Thin Films for Ferroelectric Memories**
..... Lawrence F. Schloss

4:30 PM **H8 (Student), Ion Beam Etching of Lead Zirconate Titanate Films**
..... Steven J. Gross

Session I: Low Dimensional Structures for Devices

1:30 PM **I1 (Student), Characterization of MBE-Grown Silicon Germanium/Silicon Multiple Quantum Wells for Terahertz Detector Applications**
.....Pengcheng Lv

1:50 PM **I2, Mid-Infrared Ge Quantum Dot Photodetector**
.....Fei Liu

2:10 PM **I3, Phase Diagram of the Stranski-Krastanov Mode for the SiGe/Si Heterostructure System and Application for Solar Cells with Self-Assembled Ge Quantum Dots**
..... Kazuo Nakajima

2:30 PM **I4, Stark Shift in Multiple Quantum Well Structures Containing a Delta-Doping Superlattice for Amplitude Modulation**
..... Patricia Lustoza Souza

2:50 PM **I5 (Student), Fabrication and Speed-Power Characterization of Quantum Wire Switches with Nanometer-Scale Schottky Gate Control for GaAs Hexagonal BDD Quantum Circuits**
..... Miki Yumoto

3:10 PM **Break**

Session J: Low Dimensional Device Structures

3:30 PM **J1, Spatial Ordering of InAs Quantum Dots in a Microdisk Cavity to Achieve Large Spontaneous Emission Enhancement**
.....Zhigang Xie

3:50 PM **J2, Effect of Si-Delta-Doping on the Luminescence and Laser Properties of InP/InAlGaP Quantum Dots**
..... X. B. Zhang

4:10 PM **J3 (Student), InP Quantum Dot Coupled to InGaP Quantum Well Heterostructure for Room Temperature Continuous Wave Lasers Grown by Metalorganic Chemical Vapor Deposition**
..... Richard Dean Heller

4:30 PM **J4 (Student), Tunneling Between a Single Impurity and a Quantum Dot.**
.....Erik M. Lind

4:50 PM **J5, Dependence of InAs Quantum Dots Optical Properties on Capping Materials: GaNAs Strain Compensating Layers (SCL) and GaAs Layers**
..... X. Q. Zhang

Session K: Spin-Dependent (or Spintronic) Electronic Materials - II

1:30 PM **K1 (Student), Magnetic Properties of Mg and Mn Co-Doped GaN Films Grown by PEMBE**
..... Min-Chang Jeong

1:50 PM **K2 (Student), Electronic Properties of Epitaxial (In,Mn)As**
..... Steven J. May

2:10 PM **K3, Room Temperature Ferromagnetic Properties of Mn-Doped InxGa1-xN**
..... Meredith Lynn Reed

2:30 PM **K4, Ferromagnetic GaMnAs and GaMnP Formed by Mn Ion Implantation and Pulsed Laser Melting**
..... M. A. Scarpulla

2:50 PM **Late News**

Session L: Non-Destructive Testing and In-Situ Monitoring

3:30 PM **L1, SiC Epitaxial Film Characterization Using FTIR Spectroscopy and Improved Parameter Estimation**
..... Michael S. Mazzola

3:50 PM **L2, Spectroscopic Ellipsometric Monitoring of Planar InAs Growth on GaAs(001)**
..... Kurt G. Eyink

4:10 PM **L3 (Student), Impact of Low Frequency Magnetic Field on the Electrical Characteristics of Shallow P+N Junctions**
..... Moustapha Abdelaoui

4:30 PM **L4, Using High-Resolution X-Ray Diffraction and X-Ray Topography to Pinpoint Defects in GaAs Wafers**
..... Christine H. Russell

4:50 PM **L5, Late News**

2003 EMC AT-A-GLANCE

Wednesday Afternoon, June 25, 2003

Session M: Metal Contacts to Semiconductors

1:30 PM **M1, Thermodynamically Stable NiSi Ohmic Contacts to n-Type 6H-SiC**
..... Christpher Deeb

1:50 PM **M2 (Student), Comparison and Optimization of Ohmic Contacts on p-Type Silicon Carbide**
..... Feroz Abdul Mohammad

2:10 PM **M3, Catalytic Graphitization and Ohmic Contact Formation on 4H-SiC**
..... Weijie Lu

2:30 PM **M4 (Student), WSix Schottky Contacts to Both n-SiC and n-GaN**
..... Jihyun Kim

2:50 PM **M5 (Student), Low Resistance and Thermally Stable Re/Ti/Au Ohmic Contacts to n-ZnO**
..... Sang-Ho Kim

3:10 PM **Break**

3:30 PM **M6, Re-Examination of Barrier Heights between Metals and Se-Passivated n-Type Si(100)**
..... Shruddha Agarwal

3:50 PM **M7, Ohmic Contacts to n-GaSb and n-GaInAsSb**
..... Robin K. Huang

4:10 PM **M8 (Student), Interfacial Reactions of Mn Thin Films on GaAs (100)**
..... J. L. Hilton

4:30 PM **M9, II-VI Ultra-Violet Detectors: Issues of Schottky Metal Contacts**
..... Zhen Guo

4:50 PM **M10, Late News**

Session N: Materials Integration: Wafer Bonding and Alternative Substrates - II

1:30 PM **N1 (Student), Scanning Photocurrent Measurements for the Nondestructive Evaluation of Waferbonded Interfaces**
..... Phil Mages

1:50 PM **N2 (Student), Integration of Lattice-Mismatched Semiconductors with Si using SiO_2 CMP Layers and Wafer Bonding Ge/GeSi/Si Virtual Substrates**
..... Arthur J. Pitera

2:10 PM **N3 (Student), Stress Balance of Si/SiGe and SiO_2/SiGe on Compliant Substrates**
..... Haizhou Yin

2:30 PM **N4 (Student), Adhesive Wafer Bonding of GaAs on Si and its Effect of SeS2 Treatments on the Structural Modification Changes of n-GaAs(100) Substrate**
..... Premchander Perumal

2:50 PM **N5, Late News**

3:10 PM **Break**

3:30 PM **N6 (Student), Wafer-Fused nAlGaAs-pGaAs-nGaN Heterojunction Bipolar Transistors**
..... Sarah Marie Estrada

3:50 PM **N7, Wafer-Bonding and Epitaxial Transfer of GaInAsSb/GaSb to GaAs Substrates for Monolithic Series Interconnection of Thermophotovoltaic Cells**
..... Christine A. Wang

4:10 PM **N8 (Student), III-V on Insulator Composite Substrates**
..... Sumiko Lynn Hayashi

4:30 PM **N9 (Student), $IN_{0.4}GaAs/IN_{0.2}GaAs$ Multi-Quantum-Wells Grown on Twist Bonded GaAs Compliant Substrates**
..... Yuanming Deng

4:50 PM **N10, Fabrication of AIN-Silicon-on-Insulator Structure and Computer Simulation of Self-Heating Effect**
..... Ming Zhu

Session O: Nitrides: Defect Reduction and Epitaxy

Thursday Morning Begins

8:20 AM **O1 (Student), Nanometer Scale Lateral Epitaxy Overgrowth of GaN Employing Block Copolymer Lithography**
..... R. R. Li

8:40 AM **O2, Developing Cantilever Epitaxy of GaN for Advanced Devices**
..... David M. Follstaedt

9:00 AM **O3 (Student), Reduction of Dislocation Density in MOVPE GaN Films by ELOG Without Photolithography and Chemical Etching**
..... Xiaolong Fang

9:20 AM **O4, Multiple Quantum Well AlGaN Structure Grown on Patterned Sapphire Substrate**
..... Mikhail E. Gaevski

9:40 AM **O5 (Student), InGaN/GaN Buried Heterostructure Formed by MOCVD Growth on Nonplanar Substrates**
..... Dawei Ren

10:00 AM **Break**

10:20 AM **O6 (Student), Study on Sapphire Nitridation in Hydride Vapor Phase Epitaxy System: Nitridation Mechanism**
..... Fransiska Dwikusuma

10:40 AM **O7, Interface Interdiffusion and Chemical Reaction in GaN/Sapphire and AlGaN/Sapphire Heterojunctions**
..... Xiaoling Sun

11:00 AM **O8, The Chemistry and Kinetics of LiGaO2 Substrate Nitridation for the Optimization of GaN Epitaxial Growth**
..... Maria Losurdo

11:20 AM **O9, Identification of the Adducts Formed between Magnesocene ($MgCp_2$) and NH_3: Origin of the Memory Effect**
..... George T. Wang

2003 EMC AT-A-GLANCE

Thursday Morning, June 26, 2003

Session P: Epitaxy I: Growth and Characterization

8:20 AM **P1, A Chemical and Kinetic Study of P-for-As Anion Exchange Reactions in GaAs/GaAsP Superlattice Structures**
..... April Susan Brown

8:40 AM **P2, Growth and Polarization Anisotropy Characterization of Ordered InGaAsP for Optical Fiber Applications**
..... Stefan Neumann

9:00 AM **P3, Surface Structure and Stability of Pseudomorphic InGaAs Layers**
..... Joanna Mirecki Millunchick

9:20 AM **P4 (Student), Surfactant Modified Lateral Growth and Surface Morphology of GaAs (001)**
..... Ryan R. Wixom

9:40 AM **P5 (Student), Experimental Studies and Modeling of Selective Area Growth of InP-Related Alloys by MOCVD**
..... Sang-Jun Choi

10:00 AM **Break**

10:20 AM **P6, Faceting and Lateral Overgrowth on a SiO_2-Masked GaAs Substrate - Dependence on Nanoscale Dimensions**
..... S. C. Lee

10:40 AM **P7 (Student), The Effect of N on Ordering in GaInP**
..... David Cook Chapman

11:00 AM **P8 (Student), The Effect of Nitrogen on the Optical and Transport Properties of Ga0.48In0.52NyP1-y Grown on GaAs (001) Substrates**
..... Y. G. Hong

11:20 AM **P9, Heteroepitaxial and Homoepitaxial Growth of ZnO{0001} Thin Films via Metalorganic Vapor Phase Epitaxy and their Characterization**
..... Robert F. Davis

11:40 AM **P10, Late News**

Session Q: Materials Issues for Organic Optoelectronics and Transistors

8:20 AM **Q1, Organic Light Emitting Diodes with Laminated Electrodes**
..... Tae-Woo Lee

8:40 AM **Q2, Combinatorial Methods for Investigating the Effect of Layer Thickness and Doping on the Performance of Red Organic Light-Emitting Devices**
..... David J. Gundlach

9:00 AM **Q3, Efficient, Fast Response and Color-Tunable Polymer Light-Emitting Devices**
..... Cheng Huang

9:20 AM **Q4, Hall Effect Measurement of Low Mobility Organic Semiconductors**
..... Jeffery Robert Lindemuth

9:40 AM **Q5, Bias-Stress Effects in Polythiophene and Polyfluorene Thin-Film Transistors**
..... Alberto Salleo

10:00 AM **Break**

10:20 AM **Q6 Invited, Pentacene Thin Film Transistors: From Film Growth to Applications in Sensors**
..... George Malliaras

11:00 AM **Q7, Shadow Mask Patterned Pentacene Based Transponder Circuitry**
..... Paul F. Baude

11:20 AM **Q8 (Student), Stability of Pentacene Based Thin Film Transistors in an Acidic Ambient**
..... Karthik Shankar

Session R: Nanoscale Fabrication and Self Assembled Systems

8:20 AM **R1 (Student), The Growth of GaAsN Islands on InP**
..... Päivi Pohjola

8:40 AM **R2, Ultra-High Dense InGaAsN:Sb/GaAs Quantum Dot Arrays Fabricated Non-Lithographically for Long-Wavelength Optical Devices**
..... N. Kouklin

9:00 AM **R3, Well-Aligned Zinc Oxide Nanodots Array on Patterned Substrates**
..... Shizuo Fujita

9:20 AM **R4 (Student), Ordered Arrays of InGaAs Nanostructures by Selective Area Growth or Modulated Self-Assembly Using Block Copolymer Lithography**
..... R. R. Li

9:40 AM **R5 (Student), Biomolecular Nanomotor Motility in SU-8 Microchannels**
..... Lili Jia

10:00 AM **Break**

10:20 AM **R6 (Student), Lateral Nanogaps by Vertical Processing**
..... Karthik Shankar

10:40 AM **R7 (Student), 30-nm Period Gratings in Hydrogen Silsesquioxane Resist Fabricated by Electron-Beam Lithography**
..... Michael J. Word

11:00 AM **R8, Pulsed Laser Annealing of Self-Organized InAs/GaAs Quantum Dots**
..... Subhananda Chakrabarti

11:20 AM **R9 (Student), A Systematic Study of SiGe Quantum Fortresses and Possible Applications to Quantum Cellular Automata**
..... Thomas E. Vandervelde

11:40 AM **R10, Morphological Evolution of $Si_{1-x}Ge_x$ Films Grown on Intentionally Pitted Si(100) Surfaces Using Molecular Beam Epitaxy**
..... Qingfang Yao

2003 EMC AT-A-GLANCE

Thursday Morning, June 26, 2003

Session S: High-K Dielectrics - I

8:20 AM **S1, Atomic Layer Deposition of Metal Oxide High-k Gate Dielectrics for MOSFETs and Carbon Nanotube Transistors**
..... Paul C. McIntyre

9:00 AM **S2 (Student), Charge Trapping in Atomic Layer Deposited Hafnium Oxide on Silicon**
..... Andrew Y. Kang

9:20 AM **S3 (Student), Integration and Electrical Performance of Aluminum Oxide Thin Films Deposited by Low Temperature Metal Organic Chemical Vapor Deposition (MOCVD) for CMOS Gate Dielectric Applications**
..... Spyridon Skordas

9:40 AM **S4, Experimental and Theoretical Analysis of HfO_2 Thin Film Growth by MOCVD**
..... A. N. Vorob'ev

10:00 AM **Break**

10:20 AM **S5 (Student), UV-Ozone Oxidized High-k Dielectrics on Si and Ge Substrates**
..... David Chi

10:40 AM **S6, Modeling of the Accumulation Capacitance in the Case of High-K Gate Dielectrics**
..... Samares Kar

11:00 AM **S7 (Student), Development of Hybrid TiAlOx Layer as a Novel High-k Gate Oxide**
..... Wei Fan

11:20 AM **S8 (Student), Improved Electrical Properties of SONOS-Type Flash Memory Using High-k Dielectric as Charge Trapping Layer and Blocking Layer**
..... Sangmoo Choi

11:40 AM **S9, Aluminum Oxide Layers as Potential Components for Crested Tunnel Barriers**
..... Elena Cimpoiasu

Session T: Contacts to Group III Nitrides

8:20 AM **T1 (Student), Formation of Low Resistance and Transparent Ohmic Contacts to p-Type GaN using Transparent Conducting Oxides**
..... June O. Song

8:40 AM **T2, Effects of Oxidation of Ni/Pt and Ni/Pt/Au p-Contacts on Performance of InGaN/GaN Multiple-Quantum Well Light-Emitting Diodes**
..... Chul Huh

9:00 AM **T3 (Student), Surface Treatment of n-GaN for Ohmic Contact Formation**
..... Deepak Selvanathan

9:20 AM **T4 (Student), The Study of n-Ohmic Contact in III-Nitride Semiconductor for High Temperature Applications with the Use of W and WSi**
..... Ben Luo

9:40 AM **T5 (Student), Optimization of AlGaN/GaN HEMT Sunken Ohmic Contacts**
..... Haiting Wang

10:00 AM **Break**

10:20 AM **T6 (Student), Compositional Shift of III-Nitride Alloy Semiconductors Induced by Reaction with Metallic Thin Films**
..... Brett A. Hull

10:40 AM **T7, Improvement of Schottky Characteristics by Insertion of Refractory Metal into Ni/Au Electrodes on n-(Al)GaN with Thermal Annealing**
..... Naruhisa Miura

11:00 AM **T8 (Student), High Temperature GaN Based Schottky Diode Gas Sensors**
..... Jihyun Kim

11:20 AM **T9, Study of Schottky Contacts on Strained AlGaN/GaN Heterostructures**
..... Zhaojun Lin

11:40 AM **T10, Late News**

Session U: SiC: Growth and Characterization

8:20 AM **U1 (Student), Electro-Chemical-Mechanical Polishing of Silicon Carbide**
..... Canhua Li

8:40 AM **U2, Large Diameter High Purity Semi-Insulating 4H-SiC Substrates for Microwave Device Applications**
..... D. P. Malta

9:00 AM **U3, Electrical Characteristics of 4H-SiC Epitaxial Layers Grown by Chemical Vapor Deposition on Porous SiC Substrates**
..... Zhaoqiang Fang

9:20 AM **U4 (Student), Studies of Pore Morphology Modification in Porous SiC during High-Temperature Processing**
..... Jie Bai

9:40 AM **U5, Study of Bulk Wet Etching and Optical Properties of Porous 6H-SiC**
..... Tim K. Hossain

10:00 AM **Break**

10:20 AM **U6, Growth and Characterization of Intentionally Al Doped 3C-SiC on Step Free 4H-SiC and 6H-SiC Mesa Substrates**
..... Andrew J. Trunek

10:40 AM **U7, Surface Characterization of 3C-SiC Mesa Heterofilms: Evidence for Growth by Edge/Corner Nucleation Mechanism**
..... Philip G. Neudeck

11:00 AM **U8, Hot-Wall CVD Epi-Growth of 4H-SiC using PVT Buffer Layer**
..... Ying Gao

11:20 AM **U9 (Student), Experimental Investigation and Simulation of Si-Droplets Formation during SiC CVD Epitaxial Growth and Implant Annealing Processes**
..... Yingquan Song

11:40 AM **U10, Late News**

2003 EMC AT-A-GLANCE

Thursday Afternoon, June 26, 2003

Session V: UV and Visible Nitride Emitters

1:30 PM **V1 (Student), Ternary AlGaN-Based LEDs Emitting at 292 nm**
..... Ting Gang Zhu

1:50 PM **V2, Deep Ultra Violet Light Emitting Diodes Based on Short Period Superlattices of AlN/AlGaN**
..... Sergey A. Nikishin

2:10 PM **V3, OMVPE Growth and Characterization of AlGaN for Ultraviolet Optoelectronics**
..... Maria Gherasimova

2:30 PM **V4, Growth of High Quality AlGaN Layers on Single Crystal Bulk AlN Substrates**
..... Qhalid Fareed

2:50 PM **Break**

3:10 PM **V5, High Optical Quality InGaN/GaN Multiple Quantum Disks on GaN Nano-Columns Grown by rf-Plasma Assisted Molecular Beam Epitaxy**
..... Akihiko Kikuchi

3:30 PM **V6 (Student), Mg Fluctuation in p-GaN Layers and its Effects on InGaN/GaN Blue Light-Emitting Diodes Dependent on p-GaN Growth Temperature**
..... Chi Sun Kim

3:50 PM **V7, Mg Doping of AlGaN and GaN Epitaxial Layers Grown by MOVPE**
..... Chak-wah Tang

4:10 PM **V8 Cancelled, InGaN/GaN Blue LEDs Fabricated on <11-20> Patterned Sapphire Substrates**
..... Tzu-Chi Wen

4:30 PM **V9 Cancelled, Nitride-Based LEDs with Si-Doped In0.23Ga0.77N/GaN Short-Period Superlattice Tunneling Contact Layer**
..... Tzu-Chi Wen

Session W: Epitaxy II: Metamorphic Growth and Integration

1:30 PM **W1 (Student), Lower Surface Defect Densities and Improved Electrical Properties if InAs Epilayers Grown on GaP Substrates**
..... Aristo Yulius

1:50 PM **W2 (Student), Metamorphic InAs Bipolar Junction Transistors on GaAs and InP Grown by Molecular Beam Epitaxy**
..... Xiaohua Wu

2:10 PM **W3 (Student), 2 Micron Emission from InAs Quantum Dashes Grown on a GaAs Substrate Using AlGaAsSb Metamorphic Buffers**
..... Ganesh Balakrishnan

2:30 PM **W4 (Student), "Arsenic Free" Infrared Photovoltaic Detectors with Metamor phic InAlSb Digital Alloy Buffer Layers**
..... Elena A. Plis

2:50 PM **W5 (Student), Carrier Recombination in Metamorphic InAsP/InGaAs Double Heterostructure Grown on Off-Cut and On-Axis InP Substrates**
..... Yong Lin

3:10 PM **Break**

3:30 PM **W6 (Student), Segmented Growth Optimization and Chemical-Mechanical Polishing of InAlAs Graded Buffer Layers for InAs-Based Device Structures**
..... Atif M. Noori

3:50 PM **W7 (Student), Correlation of Minority Carrier Electron and Hole Lifetimes and the Reverse Saturation Current Density in GaAs Diodes Grown on Ge/SiGe/Si Substrates**
..... Carrie L. Andre

4:10 PM **W8 (Student), Low Temperature MBE-Grown GaAs on Silicon Substrates for Ultra-Fast Photoconductive Switches Application**
..... Kai Ma

4:30 PM **W9, Ge Overgrowth of Oxidized and Reduced Ge/Si Islands**
..... Vilma Zela

4:50 PM **W10, Quantification of Substitutional Carbon and Oxygen's Affect on the Electron Minority Carrier Lifetime in Pseudomorphically Strained SiGeC**
..... Malcolm S. Carroll

Session X: Narrow Bandgap Antimonides and Arsenides

1:30 PM **X1, Correlation of Growth Conditions with Photoluminescence and Lasing Properties of Mid-IR Antimonide Type-II "W" Structures**
..... Chadwick L. Canedy

1:50 PM **X2 (Student), Interrelationships in the Electronic and Structural Characteristics of AlGaAsSb-InAs HEMT Structures**
..... Gregory Edward Triplett

2:10 PM **X3 (Student), Interdiffusion Studies of Al and Ga in AlSb/GaSb Quantum Wells**
..... M. Gonzalez Debs

2:30 PM **X4, Control of As Cross-Contamination in InAs/GaSb Superlattice IR Detectors**
..... Eric M. Jackson

2:50 PM **X5 (Student), Microstructure of Lateral Epitaxially Overgrown InAs Thin Films**
..... G. Suryanarayanan

3:10 PM **Break**

3:30 PM **X6, Etch Characteristics of the Group-III Antimonides Using BCl3/Cl2 in Inductively Coupled Plasma (ICP) Dry Etching**
..... Carlos J. Monroy

3:50 PM **X7 (Student), Characterization of Contact Resistivity on InAs/GaSb Interface**
..... Yingda Dong

4:10 PM **X8, Non-Contact Determination of Free Carrier Concentration in n-GaSb and n-GaInAsSb**
..... J. E. Maslar

4:30 PM **X9 (Student), A Novel Approach to Enhancing the Polishing Process of InP or GaSb-Based Wafer Substrates for Large-Scale Manufacturing**
..... Frank F. Shi

2003 EMC AT-A-GLANCE

Thursday Afternoon, June 26, 2003

Session Y: Molecular Electronics and Nanotubes

1:30 PM **Y1, Realization of "Molecular Enamel Wire" Concept for Molecular Electronics**
.....Rodion Vladimirovich Belosludov

1:50 PM **Y2 (Student), Measuring Electronic Conduction in DNA Attached to Au-Electrodes**
..... Sugata Bhattacharya

2:10 PM **Y3, Nature of Electrical Contacts in Au-Octanedithiol-GaAs Diodes**
..... Julia W.P. Hsu

2:30 PM **Y4 (Student), Metal-Molecules-Metal Devices with Preformed Metal Contact Structures**
..... Jaewon Choi

2:50 PM **Y5, Clocked Molecular Quantum-Dot Cellular Automata**
..... Craig S. Lent

Session Z: High-K Dielectrics - II

1:30 PM **Z1 Invited, Spectroscopic Studies of the Electronic Structure of Transition Metal and Rare Earth High-K Gate Oxides**
..... G. Lucovsky

2:10 PM **Z2 Cancelled, Characterization of HfO2 Films for High-k Gate Application**
..... Joseph Kulik

2:30 PM **Z3 (Student), Transmission Electron Microscopy Investigations of the Structure and Stability of Gate Dielectrics**
..... Yan Yang

2:50 PM **Z4 (Student), Spin Dependent Recombination at Deep Level Centers at the 4H Silicon Carbide/Silicon Dioxide Interface**
..... Nathaniel A. Bohna

3:10 PM **Break**

3:30 PM **Z5 Cancelled, Effect of SiOx Content on Electrical and Morphological Properties of HfSiOx Thin Films**
..... Koray Karakaya

3:50 PM **Z6, Combinatorial Ternary Phase Diagramming for Discovery of New Gate Materials and their Characterizations**
..... T. Chikyow

Session AA: AlGaN/GaN HEMTs: Growth

1:30 PM **AA1 (Student), Correlation Between Dislocation Density and Mobility of GaN Based HEMTs**
..... Allen M. West

1:50 PM **AA2 (Student), Improved Performance of AlGaN/GaN HEMTs Grown by Metalorganic Chemical Vapor Deposition**
..... Michael M. Wong

2:10 PM **AA3 (Student), AlGaN/GaN HEMTs on Si Substrates: Influence of Layer Structure on Device Performance**
..... Peter Javorka

2:30 PM **AA4 (Student), The Influence of Layer Parameters on the 2DEG Density in AlGaN/GaN Heterostructures**
..... Stefan Karl Davidsson

2:50 PM **AA5, Bow Reduction of AlGaN/GaN HEMT Structures Using Interlayers by MOVPE**
..... Masahiro Sakai

2003 EMC AT-A-GLANCE

Friday Morning, June 27, 2003

Session BB: SiC: Defects, Processing and Devices

Thursday Afternoon, cont...

1:30 PM **BB1, Dependence of Stacking Fault Growth on Current Density and Stress in SiC PiN Diodes**
..... R. E. Stahlbush

1:50 PM **BB2, Partial Dislocations and Stacking Faults in 4H-SiC PiN Diodes**
..... Mark E. Twigg

2:10 PM **BB3, Study of Forward Voltage Drop Degradation in Diffused SiC PIN Diodes**
..... Stanislav Soloviev

2:30 PM **BB4, Vanadium, Carbon Vacancies, and Boron in Semi-Insulating SiC**
..... Mary Ellen Zvanut

2:50 PM **BB5 (Student), Traps in Double Implanted 4H-SiC Diodes**
..... Souvick Mitra

3:10 PM **Break**

3:30 PM **BB6 Cancelled, Silicon Carbide-Oxide Interfaces: The Role of Charged Defects on High Temperature Device Performance**
..... Ruby Nandini Ghosh

3:50 PM **BB7, Reduction of the Interface Trap Density of the 4H-SiC (11-20)/SiO2 Interface**
..... Sarit Dhar

4:10 PM **BB8 (Student), The Influence of Processing Steps on Reverse-Bias Characteristics of 4H-SiC Schottky Barrier Diodes**
..... Kelly A. Neely

4:30 PM **BB9, 16.8 $m\Omega cm^2$, 600 V, Normally-Off Planar Power ACCUFET in 4H-SiC**
..... Saichirou Kaneko

4:50 PM **BB10, Late News**

Session CC: Nitrides: Substrates and Properties

8:20 AM **CC1, HVPE-GaN Thick Films for Quasi-Substrate Applications: Strain Distribution and Wafer Bending**
..... T. Paskova

8:40 AM **CC2, Strain Reduction for Crack-Free Growth of AlGaN on Porous GaN**
..... Qhalid Fareed

9:00 AM **CC3 (Student), Asymmetric Strain in III-N Resulting from the Substrate with Direction-Dependent Thermal Expansion Coefficients**
..... Sa Huang

9:20 AM **CC4 (Student), III-Nitride Growth on Lithium Niobate: Polarity Control by Electrostatic Boundary Condition**
..... Gon Namkoong

9:40 AM **CC5, Homoepitaxy of Nitride Films on Bulk Nitride Substrates and Sapphire-Based Templates by MOCVD**
..... Dae-Woo Kim

10:00 AM **Break**

10:20 AM **CC6 (Student), Growth of High-Quality AlN Single Crystals by Sublimation**
..... Rafael Dalmau

10:40 AM **CC7, Near-Band-Edge Photoluminescence Dynamics in AlN Epilayers Grown on A-Plane Single Crystal Bulk AlN**
..... Edmundas Kuokstis

11:00 AM **CC8, Effect of Growth Condition on Structural Properties of AlN Epitaxial Layer**
..... David W. Weyburne

11:20 AM **CC9, Growth Mode Control of GaN by Si using Si-Irradiation Technique in rf-MBE**
..... Xu Qiang Shen

11:40 AM **CC10, Late News**

Session DD: Epitaxy III: Devices

8:20 AM **DD1 (Student), Monolithic Integration of AlGaInP Light Emitting Diodes on Si Substrates**
..... O. Kwon

8:40 AM **DD2 (Student), Planarized Regrowth Technology for Vertically Stacked Waveguides using Metalorganic Chemical Vapor Deposition**
..... Seung-June Choi

9:00 AM **DD3 (Student), Semiconductor Optical Amplifier and Electroabsorption Modulator Monolithically Integrated via Selective Area Growth**
..... Ryan A. Stevenson

9:20 AM **DD4 (Student), Long-Wavelength GaAsSb Quantum Well Heterostructures Laser Grown by Metalorganic Chemical Vapor Deposition**
..... Min-Soo Noh

9:40 AM **DD5 (Student), Effects of Silicon Complexes on Tunnel Junctions for Vertical Epitaxial Integration**
..... Jizhi Zhang

10:00 AM **Break**

10:20 AM **DD6 (Student), InAs/GaP/InGaP High-Temperature Power Schottky Rectifier**
..... An Chen

10:40 AM **DD7 (Student), Optimization of Metalorganic Chemical Vapor Deposition of AlGaN/GaN Heterostructures for High Electron Mobility Transistors**
..... Yugang Zhou

11:00 AM **DD8, Stability of AlGaN/GaN HEMT Epitaxial Wafers**
..... David William Gotthold

11:20 AM **DD9, Study of Collector-Up AlGaN/GaN HBTs Grown by Metalorganic Chemical Vapor Deposition**
..... Uttiya Chowdhury

11:40 AM **DD10, Late News**

2003 EMC AT-A-GLANCE

Friday Morning, June 27, 2003

Session EE: Low-Dimensional Structures: Quantum Dots and Wires

8:20 AM **EE1, The Growth Behaviours of Aligned ZnO Nanowires on Si, Sapphire, and GaN Substrates by Carbothermal Reduction and Thermal CVD Methods**
..... Hyun-Gi Hong

8:40 AM **EE2, Microcharacterization of Size-Selected, Colloidal InP Quantum Dots and Rods**
..... S. P. Ahrenkiel

9:00 AM **EE3, Observation of Multiple Negative Differential Resistances in Semiconductor Quantum Wires Self Assembled in Porous Alumina Templates**
..... Supriyo Bandyopadhyay

9:20 AM **EE4, One Unit Cell Width Ferroelectric Domains**
..... Shlomo Berger

9:40 AM **EE5, MBE-Grown Fe Ferromagnetic Quantum Dots**
..... Tak Ki So

10:00 AM **Break**

Session FF: Silicon/Germanium Low-Dimensional Structures

10:20 AM **FF1 (Student), Ordering of Self-Assembled Ge Islands on Photolithographically Patterned Structures on Si (001)**
..... Bin Yang

10:40 AM **FF2, Growth of Chemically Vapor Deposited Ge Nanowires on Si(001)**
..... Ted Kamins

11:00 AM **FF3, Silicon Nanowires Grown by Vapor Phase Epitaxy**
..... Sun-Gon Jun

11:20 AM **FF4, Strong Near-Infrared Photoluminescence and Absorption from Si/SiGe Type-II Multiple Quantum Wells on Bulk Crystal SiGe Substrates**
..... Shuran Sheng

Session GG: AlGaN/GaN HEMTs: RF Dispersion, Processing Effects and Novel Gate Oxides

8:20 AM **GG1, Influence of Dual Frequency PECVD Si3N4 Passivation on the Electrical Characteristics of AlGaN/GaN Heterostructure Field Effect Transistors**
..... Wei Sin Tan

8:40 AM **GG2, RF Dispersion in Unpassivated AlGaN/GaN HEMTs Grown by MBE**
..... Oleg Mitrofanov

9:00 AM **GG3, Reduction of Surface-Induced Current Collapse in AlGaN/GaN HFETs on Free-Standing GaN Substrates**
..... Yoshihiro Irokawa

9:20 AM **GG4 (Student), The Effect of Processing Induced Stress on AlGaN/GaN HFET Characteristics**
..... Adam M. Conway

9:40 AM **GG5, Characterization of Processing Effects on Defects in AlGaN/GaN HEMT's and Correlation with Device Performance**
..... Gregg H. Jessen

10:00 AM **Break**

10:20 AM **GG6 (Student), Trap States Induced Frequency Dispersion of AlGaN/GaN Heterostructure Field Effect Transistors**
..... R. M. Chu

10:40 AM **GG7 (Student), AlGaN/GaN Metal Oxide Semiconductor Field Effect Transistors using Titanium Dioxide**
..... Peter J. Hansen

11:00 AM **GG8 (Student), AlGaN/GaN MOSHEMT Using Sc_2O_3 as the Gate Oxide**
..... Rishabh Mehandru

11:20 AM **GG9 (Student), Highly Selective, Smooth PEC Undercut Etching of Heterostructures**
..... Yan Gao

Session HH: Narrow Bandgap Nitrides and Arsenides

8:20 AM **HH1, Identification of Defects in GaNP by Optically Detected Magnetic Resonance**
..... Weimin M. Chen

8:40 AM **HH2, Signature of the Defect Limiting the Minority-Carrier Lifetime in GaInNAs**
..... Aaron J. Ptak

9:00 AM **HH3, Trap-Dominated Minority-Carrier Recombination in GaInNAs pn Junctions**
..... Daniel J. Friedman

9:20 AM **HH4 (Student), Strong Photolumines cence Enhancement of 1.3 μm GaInNAs Active Layers by Introduction of Antimony**
..... Seth Robert Bank

9:40 AM **HH5, Effects of MOCVD Growth Conditions on Properties of GaInNAs/GaAs Quantum Wells**
..... Noppadon Nuntawong

10:00 AM **Break**

10:20 AM **HH6 (Student), An Investigation of GaNAs(Sb) for Strain Compensated Active Regions at 1.3 and 1.55 μm**
..... Homan Bernard Yuen

10:40 AM **HH7, Growth of Metastable GaAsBi Alloy by Molecular Beam Epitaxy**
..... Masahiro Yoshimoto

11:00 AM **HH8 (Student), Infra-Red Properties of Mn Doped InAs and (In,Mn)As Epitaxial Films**
..... Philip T. Chiu

Wednesday, June 25, 2003

EMC PLENARY LECTURE/STUDENT AWARDS

Ceremony: 8:20 AM

Room: Ballroom Center

Plenary Speaker: Stephen Forrest, Princeton University, Dept. of Electl. Engrg., EQUAD B301, Princeton, NJ 08544 USA

Topic: Organic Electronics: Is it for Real or is it Just the Latest Fad?

Break: 9:20 AM - 10:00 AM

Joint DRC/EMC Invited Session VI: Carbon-Based and Nanowire Devices

Wednesday AM Room: Saltair
June 25, 2003 Location: Olpin Union Building

Session Chair: Theresa Mayer, Pennsylvania State University, University Park, PA 16802-2705 USA

10:00 AM Invited

VI.-1, Functional Semiconductor Nanowires and Their Optical Properties: *P. Yang*[1]; [1]University of California, Dept. of Chmst., Berkeley, CA 94720 USA

Nanowires are of both fundamental and technological interest. They represent the critical components in the potential nanoscale electronic and photonic device applications. In this talk, I will introduce the vapor-liquid-solid crystal growth mechanism for the general synthesis o f nanowires of different compositions, sizes, orientation and doping profile. Particularly, synthesis and organization of different types of heterostructured nanowires will be discussed. Wide band gap semiconductor nanostructures with near-cylindrical geometry and large dielectric constants exhibit two-dimensional ultraviolet and visible photonic confinement (i.e. waveguiding). Combined with optical gain, the waveguiding behavior facilitates highly directional lasing at room temperature in controlled-growth nanowires with suitable resonant feedback. The nanowire optical emission has been studied in detail using high-resolution optical microscopy. The waveguiding behavior of individual zinc oxide (ZnO, GaN) nanowires depends on the wavelength of the emitted light and the directional coupling of the photoluminescence (PL) to the emission dipoles of the nanowire. Pumping at: high pulse intensity leads to the transition from spontaneous to stimulated emission, and analysis of the polarization, linewidth, and spacing of the spectral features facilitates identification of the transverse and longitudinal cavity modes and their gain properties. The observation of Iasing action in arrayed and isolated ZnO/GaN nanowires without requiring fabrication of mirrors suggests the single-crystalline, well-facetted nanowires can indeed function as effective resonance cavities. This concept of using well-cleaved nanowires as natural optical cavities may be extendable to many other different semiconductor systems. [1]Y. Wu, R Fan, P. Yang, Nanolett, 2, 83, 2002. [2]M. Huang, S. Mao, H. Feick, H. Yan, Y. Wu, H. Kind, E. Weber, R. Russo, P. Yang, Science, 292, 1897, 2001. [3]J. Johnson, H. J. Choi, K. P. Knutsen, R. D. Schaller, R. J. Saykally, P. Yang, Nature Materials, 1, 101, 2002. [4]J. Johnson, Hi, Yan, R. Schaller, L. Haber, R. Saykally, P. Yang, J. Phys Chem B, 105, 11387, 2001.

10:40 AM Invited

VI.-2, Pushing to the Performance Limit of Carbon Nanotube Electronics: *H. Dai*[1]; [1]Stanford University, Dept. of Chmst., Stanford, CA 94305 USA

This presentation will cover our latest results in the following areas and describe the potential of nanotubes in nanoelectronics applications. (I) Controlled synthesis of nanotube structures on surfaces; patterned growth of nanotubes. (2) Nanoelectronics based on nanotube transistor arrays derived by chemical synthetic routes. Arrays of nanotube transistors for logic and ring oscillators will be presented, (3) Integration of high k zirconia dielectrics into nanotube transistors affording high performance nanotube transistors. The latest results on optimizing the performance of nanotube transistors will be presented.

11:20 AM Invited

VI.-3, Carbon Nanotube Field-Effect Transistors-An Example of an Ultra-Thin Body, Schottky Barrier Device: *J. Appenzeller*[1]; J. Knoch[2]; Ph. Avouris[1]; [1]IBM T. J. Watson Rsch. Ctr., Yorktown Heights, NY 10598 USA; [2]Massachusetts Institute of Technology, Cambridge, MA 02139 USA

We present experimental and simulation results on carbon nanotube field-effect transistors (CNFETs) and discuss their performance in the context of Schottky barriers in a strongly confined geometry. We focus in particular on the impact of the body thickness - the tube diameter - and explain why conventional output characteristics can be obtained in case of CNFETs.

Session A: Nanoscale Characterization

Wednesday AM Room: Ballroom Center
June 25, 2003 Location: Olpin Union Building

Session Chairs: Julia Hsu, Lucent Technologies, Bell Labs., Murray Hill, NJ 07974 USA; Edward Yu, University of California, Dept. of Electl. & Compu. Engrg., La Jolla, CA 92093-0407 USA

10:00 AM Student

A1, Cross-Sectional Scanning Tunneling Microscopy and Spectroscopy of InGaP/GaAs Heterojunctions: *Yang Dong*[1]; R. M. Feenstra[1]; M. P. Semtsiv[2]; W. T. Masselink[2]; [1]Carnegie Mellon University, Dept. of Physics, 5000 Forbes Ave., Pittsburgh, PA 15213 USA; [2]Humboldt-Universität zu Berlin, Dept. of Physics, Berlin D-10115 Germany

Heterojunctions between InXGa1-XP and GaAs have attracted attention recently because of their applications for heterojunction bipolar transistors (the InXGa1-XP at x~0.5 is an alternate barrier material, with nearly all the band gap difference of 0.45 eV occurring in the valence band). In this work, we report cross-sectional scanning tunneling microscopy and spectroscopy (STM and STS) studies of compositionally abrupt InGaP/GaAs heterojunctions prepared by solid source molecular beam epitaxy. Cross-sectional STM is a powerful tool for studying atomic-scale structural and electronic properties of epitaxially grown material and device structures; it permits the study of spatial variations of the electronic band structure at nanometer scales. Although there is prior STM work on the surface structure of InGaP,[1,2] no cross-sectional work has previously been reported for InGaP/GaAs heterojunctions. In our study an atomically flat (1-10) surface was exposed by cleavage in the ultra-high-vacuum STM chamber. Images of the InXGa1-XP (x=0.485) layer show clear atomic resolution, revealing a random arrangement of In and Ga atom in the alloy. From the atomic resolution images of interfaces, 2-5 unit cells of transition region and the diffusion of atoms

across the interfaces is observed. It is found that GaAs-on-InGaP interface has a slight wider transition region and more interface atom diffusion than the InGaP-on-GaAs interface. Indium outdiffusion into GaAs layer is clearly seen. Tunneling spectroscopy measurements have been performed near the interface. A clear spectroscopic feature, located near the conduction band minimum, is found in the InGaP. This feature indicates the existence of point defect states in the InGaP, although the origin of the states is not known at present. Spatially resolved spectra with nanometer spacing across the interface were acquired, from which band offsets (revealing that nearly all of band offset occurs in the valence band) were determined. [1]P. Vogt, K. Lüdge, M. Zorn, M. Pristovsek, W. Braun, W. Richter and N. Esser, Phys. Rev. B 62, 12601 (2000). [2]J. J. O'Shea, C. M. Reaves, S. P. DenBaars, M. A. Chin and V. Narayanamurti, Appl. Phys. Lett. 69, 3022 (1996).

10:20 AM Student

A2, Local Conductivity and Surface Potential Measurements of Mg-Doped p-GaN: *Blake S. Simpkins*[1]; E. T. Yu[2]; U. Chowdhury[3]; M. M. Wong[3]; T. G. Zhu[3]; D. W. Yoo[3]; R. D. Dupuis[3]; [1]University of California at San Diego, Matls. Engrg., 9500 Gilman Dr., MC 0418, La Jolla, CA 92093-0418 USA; [2]University of California at San Diego, Electl. & Compu. Engrg., 9500 Gilman Dr., EBU1 Rm. 3809, MC 0407, La Jolla, CA 92093-0407 USA; [3]The University of Texas at Austin, Microelect. Rsch. Ctr., Austin, TX 78712 USA

Effective p-type doping of GaN-based materials is a necessity for the realization of efficient optical and electronic devices such as light emitting diodes and heterojunction bipolar transistors. However, magnesium, the most widely used acceptor dopant in GaN-based materials, suffers from a large activation energy,[1] acceptor passivation through hydrogen defect complexes,[2] and inversion domain formation accompanying high levels of Mg incorporation[3] - all of which have hampered attempts to achieve high p-type conductivity. In the current study, conductive atomic force (C-AFM) and scanning Kelvin probe (SKPM) microscopies are used to examine nanoscale conductivity and surface potential variations in GaN:Mg layers grown by metal-organic chemical vapor deposition. Forward and reverse bias C-AFM imaging reveals submicron-scale regions of decreased conductivity that exhibit clear six-fold symmetry, indicating a possible crystallographic origin to these conductivity variations. Surface potential measurements of these same areas reveal a decrease in surface potential directly correlated with regions of decreased conductivity. The effect of ultraviolet illumination on surface potential has also been studied, and the expected decrease in surface barrier upon illumination[4] is observed. In addition, regions of initially lower barrier height exhibit a greater barrier decrease upon illumination. The implications and possible origins of these behaviors, along with the correlation between conductivity and surface potential variations, are currently under investigation. Possible explanations include dopant segregation, inclusion formation, and surface state variations. Results of companion studies on n-type and undoped nitride epitaxial layers will also be presented. [1]W. Kim, A. Salvador, A. E. Botcharev, O. Atkas, S. N. Mohammad, and H. Morkoc, Appl. Phys. Lett. 69, 559 (1996). [2]W. Gotz, N. M. Johnson, J. Walker, D. P. Bour, H. Amano, and I. Akasaki, Appl. Phys. Lett. 67, 2666 (1995). [3]V. Ramachandran, R. M. Feenstra, W. L. Sarney, L. Salamanca-Riba, J. E. Northrup, L. T. Romano, and D. W. Greve, Appl. Phys. Lett. 75, 808 (1999). [4]L. Kronik and Y. Shapira, Surf. Sci. 37, 1 (1999).

10:40 AM

A3, Electrical Characterisation of Self-Assembled Nanoparticle Coated Crystals: Klaus Dieter Katzer[2]; Victor Khorenko[1]; Thai Quoc Do[1]; Wolfgang Mertin[2]; Franz Josef Tegude[1]; *Werner Prost*[1]; Douglas Cunningham[3]; Jose Luiz Martinez-Albertos[3]; Barry D. Moore[3]; [1]University Duisburg-Essen, Solid-State-Elect. Dept., Faculty of Engrg., Lotharstr. 55, Duisburg D-47048 Germany; [2]University Duisburg-Essen, Dept. Werkstoffe der Elektrotechnik, Faculty of Engrg., Bismarkstr. 81, Duisburg D-47048 Germany; [3]University of Strathclyde, Dept. of Pure & Applied Chmst., 295 Cathedral St., Glasgow, Scottland G1 1XL UK

The control of the conductivity of nanoscale elements is the subject of enormous research works in areas such as DNA and carbon nanotubes. A promising alternative is the fabrication of insulating nanoscale structures and subsequent definition of the conductivity by coverage with nanoparticles. Here we demonstrate production of organised arrays of nanoparticles on geometrically regular crystals with controllable dimensions in the size range 20 nm to 5000 nm.[1] The conductivity of these nanocrystals can be controlled by covering with different nanoparticles. These nanoparticle-coated crystals may become building blocks of future nanoelectronic devices and circuits. In this work the surface potential and the I-V characteristics of nanocrystals coated with gold nanoparticles are presented. Nanoparticle-coated crystals (NCCs) can be prepared in a single step self-assembly process by co-precipitating water soluble nanoparticles and a crystal forming inorganic salt from aqueous solution, using a water miscible solvent. This procedure, pioneered by Moore, is termed Crystal LAttice Mediated Self-assembly (CLAMS[1] and gives more than 1012 flat-faced, very regular and high reproducible NCCs in one experiment. For the work described we have used the insulating inorganic salts, potassium sulfate, K2SO4, or rubidium sulfate, Rb2SO4, as the core crystalline material and 2-5 nm tiopronin (N-(2-mercaptopropionyl)-glycine) protected gold nanoparticles for the coating. The NCCs were deposited onto conducting or insulating surfaces covered with Au-electrodes by a spin-on coating technique. The electrical characteristics of the NCC were investigated as followed; (i)Scanning Force Microscopy Kelvin Force surface potential measurements reveal a work function of the Au-covered NCC of 5.12 eV which is very close to the bulk gold value (5.26 eV[2]). (ii) Scanning Force Microscopy I-V measurements are done with a variable DC voltage applied between the diamond coated tip and the NCC. They show a diode-like I-V characteristic with a current of 5-10 µA at 1 V. (iii) I-V measurements of interdigital pattern with 2 µm wide fingers separated by 1 µm spacing. A s. i. GaAs wafer covered with 200 nm SiNx suppresses the leakage to the 10-13 A range. 3-5 NCC are deposited making shorts and resulting in a back-to-back diode like characteristic with a current of 3 nA at 1V. In summary, we have determined the I-V data of the Au covered NCC. The conductivity of the Au covered NCC is surprisingly high, giving currents in the 10 µA range through a single NCC. We observe a diode like behaviour both to the diamond tip of the SFM and to Au electrodes. These first results are very promising towards electronic devices at the nanoscale made of nanoparticle-covered crystals. [1]B.D. Moore, D.Cunningham, "Nanoparticle Structures" WO03002225 International Patent Application, Jan 2003. [2]Landolt-Börnstein; New Series III/24b, chapter 3.1.2.4.

11:00 AM

A4, Near-Field Magneto-Photoluminescence of Quantum-Dot-Like Composition Fluctuations in GaAsN and InGaAsN Alloys: A. M. Mintairov[1]; P. A. Blagnov[2]; *J. L. Merz*[1]; V. M. Ustinov[2]; A. S. Vlasov[2]; A. R. Kovsh[2]; J. S. Wang[3]; L. Wei[3]; J. Y. Chi[3]; [1]University of Notre Dame, Dept. of Electl. Engrg., Notre Dame, IN 46556 USA; [2]Ioffe Physico-Technical Institute, RAS, St. Petersburg 194021 Russia; [3]Industrial Technology Research Institute, Hsinchu Taiwan

InxGa1-xAs1-yNy (x~0-0.08, y~0-0.05) alloys have recently attracted considerable attention as promising materials for laser diodes and efficient solar cells at 1.3&1.5 ìm. In the present paper we use near-field magneto-photoluminescence measurements to study optical and structural properties of quantum-dot-like compositional fluctuations in these alloys with different N and In content.[1] Coherently strained GaAs1-yNy and lattice matched InxGa1-xAs1-yNy (x~0.03-0.08, y~0.01-0.03) layers with thickness 0.1-1 ìm were grown by solid source MBE on (001) semi-insulating GaAs substrates at temperatures of 450-520°C. Near-field photoluminescence (NPL) spectra with spatial and spectral resolution of 300 nm and 0.5 meV, respectively, were taken in collection-illumination mode. The spectra were excited by 20 mW of Ar ion laser excitation at 514.5 nm, measured in the temperature range 5-300 K and magnetic field strengths 0-10 T. Between 5K and 70K the spectra of all samples reveal structure, consisting of a series of mult iple narrow lines (halfwidth ã=0.05-2 meV) superimposed on a broad (ã=20-60 meV) band located at 1-1.2 mm. We attribute the narrow lines to emission of excitons localized on QD-like composition fluctuations (N-rich clusters). Using temperature dependent near-field spectroscopy we estimated the exciton localization energy in the cluster to be 10-60 meV for T=5K. We did not observe Zeeman splitting (i.e., zero exciton g-factor) of the narrow lines in GaAsN. However, in InGaAsN these lines have clear Zeeman splitting. The splitting energy increased with increasing In content and has values of 0.7 (g-factor ~1) and 1.7 (g-factor ~2) meV at 10 T for y=0.01 and 0.03, respectively. This strong dependence of the Zeeman splitting in InGaAsN on In content can be related to a large value of the electron g-factor of InAs (-15) compared with GaN (2) and GaAs (-.044). We found that the value of the diamagnetic coefficient (â)

increases with increasing N content but shows little dependence on the presence of In. â has values 0.3-3 ìeV/T2 for y=0.01 and 3-12 ìeV/T² for y=0.03. The cluster radius for different emission energies deduced from â was found to have average value 6 and 10 nm for y=0.01 and 0.03 respectively. From monochromatic intensity images produced by near-field scanning optical microscopy (NSOM), we found that the lateral distribution of clusters in the layer is strongly inhomogeneous on a length scale of 1 ìm. We estimate the density of the QD-like clusters in our samples to be 100-300 ìm-³, which is ten orders of magnitude higher than that predicted for a random alloy, and suggesting their spontaneous formation. [1]A.M. Mintairov, T.H. Kosel, J.L. Merz, P.A. Blagnov, A.S. Vlasov V.M. Ustinov, and R.E. Cook, Physical Review Letters 87, 277401 (31 December 2001).

11:20 AM
A5, Structural/Compositional Characterization of ONO Stacks on Silicon: *Igor Levin*[1]; [1]NIST, Ceram. Div., Stop 8520, 100 Bureau Dr., Gaithersburg, MD 20899 USA

Silicon oxide-nitride-oxide multilayers (ONO stacks) attract considerable interest for the charge-storage structures in non-volatile memory devices. The critical structural and compositional parameters that affect electrical performance of ONO-based devices include the physical density of the amorphous oxide/nitride layers, which are 5-10 nm thick, and depth distributions of both oxygen and nitrogen atoms. In this study we applied spatially-resolved electron-energy loss spectroscopy (EELS) in a transmission electron microscope (TEM) to analyze O and N elemental distributions in the differently processed ONO stacks, while physical densities of individual layers were measured using X-ray reflectometry (XRR). EELS measurements were made using (i) energy-filtered TEM and EELS spectrum-line acquisition in a fixed-beam high-resolution TEM equipped with a thermionic electron source, and a post-column energy filter, and (ii) EELS spectrum-imaging in a dedicated scanning transmission electron microscope (STEM) equipped with a cold field-emission source and an EELS spectrometer. The results revealed radiation-induced nitrogen segregation to both the Si/SiOx and SiOx/poly-Si interfaces; the extent of nitrogen segregation increased visibly with increasing the radiation dose. Under the high radiation doses, the nitride layer was transformed into an oxynitride layer, containing a substantial amount of oxygen. The EELS metrology was optimized to obtain artifact-free nitrogen profiles across the Si/SiOx interfaces. The results of structural/compositional analyses were correlated with electrical performance of ONO-based flash-memory devices.

Session B: Semiconductors: Processing and Oxidation

Wednesday AM Room: Ballroom East
June 25, 2003 Location: Olpin Union Building

Session Chairs: Douglas C. Hall, University of Notre Dame, Dept. of Electl. Engrg., Notre Dame, IN 46556-5637 USA; Maria Losurdo, Institute of Inorganic Methodologies and Plasmas, Bari 70126 Italy

10:00 AM Student
B1, High Resolution Secondary Ion Mass Spectrometry Analysis of Vertical Cavity Surface Emitting Lasers: *Yong K. Kim*[1]; Judith E. Baker[2]; Kent D. Choquette[3]; Andrew A. Allerman[4]; [1]University of Illinois at Urbana-Champaign, Matls. Sci. & Engrg., 208 N. Wright St., Urbana, IL 61801 USA; [2]University of Illinois at Urbana-Champaign, The Frederick Seitz Matls. Rsch. Lab., Urbana, IL 61801 USA; [3]University of Illinois at Urbana-Champaign, Electl. & Compu. Engrg., 208 N. Wright St., Urbana, IL 61801 USA; [4]Sandia National Laboratories, Albuquerque, NM 87185 USA

Vertical cavity surface emitting lasers (VCSELs) have emerged as an important optoelectronic source, principally for 850-nm high-speed local area networks such as 10-Gigabit Ethernet. The epitaxial structure of a VCSEL is quite complex, requiring as many as 100 distinct layers with stringent tolerances on thickness, composition, and doping concentration. Optical reflectance characterization can provide a wealth of information regarding the thickness and composition, but the sophisticated doping profiles required to enable low series resistance in VCSELs are difficult to determine. We show that depth profile analysis by high-resolution secondary ion mass spectrometry (SIMS) can be useful as a diagnostic method for VCSEL epiwafers, and that the doping of a few or even one layer can dramatically impact the laser performance. The basic device structure of 850-nm VCSELs consist of an active cavity containing GaAs multiple quantum wells, and p- and n-type doped distributed Bragg reflectors (DBR), all of which are grown by metalorganic vapor phase epitaxy (MOVPE). DBR mirrors are comprised of $Al_xGa_{1-x}As$/GaAs layers doped with C and Si for p- and n- type dopants, respectively. In order to achieve confinement of both the optical mode and current, high Al composition layers adjacent to the active region are incorporated which form buried oxide apertures produced by wet oxidation. Thus, material properties of the aperture layers can affect electrical and optical performance, especially since all the current is funneling through these layers into the active region. Chemical concentrations of p- and n- type dopants in VCSEL wafers were measured by high resolution SIMS. The SIMS analyses were performed by using a CAMECA IMS-5f with a 14.5 KeV Cs+ primary beam scanning over an area of 150x150 μm². In order to obtain precise depth resolution and avoid mass interferences among Si, Al-H, and C-O, high resolution mode measurements were carried out. The raw counts data from the measurement were quantified by using standard reference samples and relative sensitivity factors (RSF). The measurement results were compared with the electronic carrier concentrations measured by Hall measurements and Polaron C-V measurements. These SIMS depth profiles were correlated to device characteristics such as light output versus current and voltage. We have determined that self-pulsating VCSEL behavior[1] of the light output can result from unexpected doping profiles in the oxide aperture layers. For example, we have measured the Si concentration in the n-type oxide layer of a self-pulsating VCSEL to be approximately equal to the C concentration in that layer. The background carbon in the n-type layers is formed by the MOVPE gas source precursors. This implies the Si concentrations are insufficient to compensate for the background carbon. We also find that the Si chemical concentration in the n-type DBRs can be extremely high (~$1x10^{19}$). Such high doping concentrations can have reliability implications. Thus, we show that high resolution SIMS can accurately determine the doping profiles in VCSEL structures, which in turn can dramatically influence the resulting device performance. [1]K.D. Choquette, H.Q. Hou, K.L. Lear, H.C. Chui, K.M. Geib, A. Mar, and B.E. Hammons, Electron. Lett., 1996, 32, pp. 459-460.

10:20 AM Student
B2, Improving Oxidation Uniformity for Uniform Performance of Large VCSEL Arrays: *Zhi-Jian Wei*[1]; Yuanming Deng[1]; Ryan Stevenson[1]; P. Daniel Dapkus[1]; Hanzhuang Liang[2]; [1]University of Southern California, Ctr. for Photonic Tech., Dept. of Electl. Engrg., Vivian Hall of Engrg. 309, 3651 USC Watt Way, Los Angeles, CA 90089 USA; [2]University of Southern California, Dept. of Aeros. & Mech. Engrg., Olin Hall of Engrg., Los Angeles, CA 90089 USA

The oxide aperture Vertical Cavity Surface Emitting Laser (VCSEL) is an important laser source in many telecomm and interconnection applications. Large (>8x8) VCSEL arrays are envisioned as possible solutions for high band width interconnect systems. Controlling the performance uniformity of large VCSEL arrays requires the control of the oxide aperture size formed by wet oxidation. In our studies of the oxidation process, we have found that the oxidation uniformity is controlled by turbulence in the oxidant flow and by the sensitivity of the oxidation rate to the aluminum content of the aperture layer. Non-laminar flow creates spatial and temporal nonuniformities in the oxidant supply to the oxidation layer. The use of thin (20nm) high aluminum content oxidation layers makes the process sensitive to the environment surrounding the VCSEL mesa. For example, during sample loading, water condenses randomly on the cold sample surface, which causes nonuniform initiation of AlAs oxidation across the array. This abstract summarizes our studies of oxidation uniformity and presents an approach to achieve excellent performance uniformity for large VCSEL array. To create the laminar flow in our 6 inch oxidation tube, we borrowed an idea from wind tunnel design to modify the furnace design. The key is to insert a specially designed quartz flow straightener in the tube. This straightener

is constructed of about 1100 hexagonally packed 2mm diameter and 8cm long quartz tubes. Based on fluid flow modeling and our experiments laminar oxidant flow can be created and maintained over a large distance (~ 4 times that of the straightener length) along the flow direction. This range overlaps with the uniform temperature region in the furnace. To eliminate water condensation, we pre-bake the sample in a dry ultra-high purity N_2 environment at an elevated temperature and carefully control the sample introduction into the oxidation flow. If the oxidation layer is set at $Al_{0.98}Ga_{0.02}As$, the sensitivity of oxidation to the environment at the beginning of the oxidation is further reduced. By incorporating these changes to our oxidation process we were able to achieve the significant improvement in the performance uniformity of the VCSEL arrays. We have demonstrated large (20 x 20) VCSEL array with average threshold current of 448 microA and standard deviation of only 29 microA. The same array exhibited an average slope efficiency (at 1mW output power) of 55%W/A with the standard deviation of only 1.9% W/A. In summary, the improvement of oxidation process uniformity will impact the design of oxidation processes. We expect it to be used in future large VCSEL arrays for large-scale parallel optical signal transmission in the optical communication system.

10:40 AM

B3, Strain and the Thermodynamics of Buried AlGaAs Layer Oxidation: *Alexana Roshko*[1]; Roy H. Geiss[1]; Robert R. Keller[1]; Dennis W. Readey[2]; Ye Chen[1]; Kristine A. Bertness[1]; [1]NIST, 325 Broadway, Boulder, CO 80305 USA; [2]Colorado School of Mines, Golden, CO 80401 USA

AlGaAs native oxides, formed by wet-thermal oxidation, play an important role in optoelectronic devices such as VCSELs. Yet strain produced by contraction of the buried AlGaAs layers during oxidation continues to be a problem for these devices. We have used electron backscatter diffraction, EBSD, mapping to determine the distribution of strain in the GaAs matrix surrounding partially oxidized AlGaAs layers. We have also performed thermodynamic calculations and combined these with kinetic data to determine the phases present in oxidized layers. The distribution and density of these phases is expected to affect the strain distribution in specimens containing oxide layers. The EBSD measurements were performed on specimens grown by MBE with 80 nm thick AlAs layers buried in a GaAs matrix. The AlAs layers were partially oxidized, laterally to depths of 10 to 40 µm. From EBSD maps it appears that in most specimens the largest strain field exists behind the oxide - AlAs interface, that is, adjacent the oxidized layer. Although in some specimens the maps suggest a strain field may be in front of the interface, adjacent the unoxidized AlAs layer. In either case the strain is usually not symmetric about the oxidized layer, but appears instead to be concentrated on the side closest to the substrate. This is likely the result of the relatively thick substrate constraining the structure more than the comparatively thin structure above the oxide layer. From the thermodynamic and kinetic calculations it is shown that several different regions of differing densities could exist along the length of the oxide layers. Correlations between the strain field maps and the calculated distribution of phases will be discussed, as will measurements on specimens with a VCSEL structure containing an $Al_{0.98}Ga_{0.02}As$ aperture layer.

11:00 AM Student

B4, Completely Pinning-Free Surface Passivation of GaAs (001) Surfaces by Forming Si and GaN Interface Control Layers on Ga-Rich (4x6) Surface: *Sanguan Anantathanasarn*[1]; Noboru Negoro[1]; Hideki Hasegawa[1]; [1]Hokkaido University, Rsch. Ctr. for Integrated Quantum Elect. & Grad. Sch. of Elect. & Info. Engrg., North-13, West-8, Sapporo 060-8628 Japan

For GaAs-based advanced electronic and photonic devices utilizing nanostructures, the well-known unsolved issue of surface passivation becomes a more and more important technological issue. Our group has proposed to insert a suitable interface control layer (ICL) such as Si[1] and GaN[2] between III-V semiconductor and insulator. These ICL-based approaches gave impressive results on InP and InGaAs. However, satisfactory effects have not been obtained on GaAs, where Si ICLs and GaN ICLs were formed on the traditional As-rich (2x4)-(001) GaAs surfaces. In this paper, we demonstrate that completely pinning-free surface passivation of technologically important (001) GaAs surfaces can be realized by forming Si and GaN ICLs on the untraditional Ga-rich (4x6) surface, as confirmed by microscopic STS and macroscopic MIS C-V measurements. Samples were fabricated and characterized in-situ in a UHV-based multi-chamber system. For process optimization, various and microscopic characterization techniques were used, including UHV STM/STS, XPS, UHV PL, UHV contactless MIS C-V and conventional MIS C-V techniques. UHV contactless MIS C-V technique uses a narrow UHV gap, produced and maintained by a piezoelectric feedback mechanism, as the insulator. The initial (4x6) GaAs surface was prepared by careful annealing and cooling down of MBE-grown surface without As_4 flux, followed by a subsequent irradiation by a monolayer of Ga flux at 500°C. STM study indicated formation of (4x6) unit cells over the entire surface, whereas the surface had partly As-rich (2x6) phase before Ga-flux irradiation. Si ICL was grown by MBE using Si K-cell, followed by its partial nitridation using N-radicals to form a thin SiN_x layer. Cubic(c-) GaN ICL was formed by direct nitridation of GaAs surface using N-radicals, followed by deposition of a thin SiN_x film. Detailed XPS analysis showed that Si ICL thickness was 0.46 nm and c-GaN ICL thickness was 0.7 nm. As a main passivation dielectric, a thick SiO_2 dielectric film was deposited subsequently by rf-CVD. After forming Si ICL and c-GaN ICL on the (4x6) surface, in-situ UHV PL intensity for GaAs band-edge emission became 10 times larger than that of the As-rich (2x4) reference surface. UHV STS and UHV contactless MIS C-V measurements on these surfaces indicated complete unpinning of Fermi level over the entire energy gap of GaAs. MIS C-V measurements in air on MIS capacitors having $Al/SiO_2/SiN_x/Si$ ICL/(4x6) GaAs and $Al/SiO_2/SiN_x$/c-GaN ICL/(4x6) GaAs structures showed large capacitance variations with remarkably reduced frequency dispersion. Thus, excellent interface properties in UHV conditions could be successfully maintained to air-exposed practical MIS structures, giving minimum interface state density values of $1x10^{11}$ and $4x10^{10}$ $cm^{-2}eV^{-1}$ for c-GaN ICL and Si ICL structures, respectively. [1]H. Hasegawa et al, J. Vac. Sci. Technol. B7, 870 (1989); [2]S. Anantathanasarn and H. Hasegawa, J. Vac. Sci. Technol. B19, 1589 (2001).

11:20 AM Student

B5, Chemical and Electronic Studies of GaSb Surface Passivation Based on Non-Aqueous Sulfide Solutions: *Zhiyan Liu*[1]; Dovas A. Saulys[2]; Thomas F. Kuech[1]; [1]University of Wisconsin, Madison, Dept. of Chem. Engrg., 1415 Engrg. Dr., Madison, WI 53706 USA; [2]University of Wisconsin, Madison, Matls. Rsch. Sci. & Engrg. Ctr., 1415 Engrg. Dr., Madison, WI 53706 USA

GaSb is an important III-V compound semiconductor for high-speed and optoelectronic device applications, and the performance of GaSb devices are strongly dependent on the chemical and electronic properties of GaSb surfaces or interfaces. As for most III-V semiconductors, high densities of surface defects (e.g. native oxide) and surface states lead to high surface recombination velocities, limiting their applications. Thus, III-V semiconductor surfaces are typically passivated with aqueous sulfide or selenide-containing solutions. The reactions between the chalcogenide and semiconductor surface species change the electronic structures of semiconductor surfaces, therefore reduce the density of surface states and improve device characteristics. Unfortunately, due to the high chemical reactivity of GaSb surfaces, aqueous processing leads to the growth of surface oxides. Chemical passivation using sulfides in a non-aqueous solution, such as alcohol, can provide advantages in the GaSb applications. In the work reported here, GaSb surfaces were passivated with sulfide solutions of the organic alcohols methanol, 2-propanol, and 1-hexanol. The lower polarities of alcohols allow a stronger interaction, and more efficient bonding between sulfide and the semiconductor surface. The efficiency of the passivation was determined by the increase in photoluminescence (PL) intensities after the passivation. The chemical characterization of the passivated surfaces, which was determined by x-ray photoemission spectroscopy (XPS), indicated the reduced oxygen and increased sulfur concentration on the surface after the passivation using the sulfide-alcohol solutions. To compensate for the lower solubility of Na_2S in alcohols, stoichiometric amounts of a cation complexing agent, 15-crown-5, were added. The oxygen atoms within the crown ether form a 'cage-like' structure, which has been used to capture and solubilize cations of suitable sizes and therefore increase the solubility and activity of sulfur ions in the solution. The results indicated after introduction of the 15-crown-5, the solubility of Na_2S in long-chain alcohols is significantly increased by at least 3 orders. During the passivation reaction, the electrons are released from the semiconductor surface and flow into the solution. To study the effect of electron flow rate on the passivation reaction, small amounts of organic oxidizing agents, including naphthalene, benzophenone, and 1,4-benzoquinone with different reduction potentials, were added into an organic, aprotic passiva-

tion regime consisting of a 15-crown-5/Na_2S/benzene solution. The increases in PL intensity were found to correlate with the reduction potentials (relative ease of reduction) of the additives indicating improved passivation of the surface.

11:40 AM B6, Late News

Session C: Si-Based Heterojunction Growth and Characterization

Wednesday AM Room: Ballroom West
June 25, 2003 Location: Olpin Union Building

Session Chairs: Mike Tischler, Epitronics Corporation, Mesa, AZ 85210 USA; Tom Langdo, Amberwave Systems Corp, Salem, NH 03079 USA

10:00 AM

C1, Fermi Level Stabilization in Plastically Strained SiGe Alloys: *P. N. Grillot*[1]; S. A. Ringel[2]; [1]LumiLeds Lighting, US LLC, 370 W. Trimble Rd., San Jose, CA 95131 USA; [2]The Ohio State University, Dept. of Electl. Engrg., Columbus, OH 43210 USA

Strain-relaxed, lattice mismatched SiGe/Si heterostructures play an important role as a virtual substrate, or as active device layers in a variety of applications, including photodetectors, solar cells, SiGe CMOS, and III-V integration on Si. The use of strain-relaxed lattice mismatched layers necessitates the introduction of high dislocation densities in the graded regions of such structures, however, and the electronic properties of these defects may have important consequences on the operation of the device layers grown on top of these graded buffers. One property that we have previously identified in such graded layers is the ability of these defects to affect the conductivity type of strain-relaxed SiGe. More specifically, we have observed electrical conductivity type conversion in strain-relaxed SiGe, where samples that were intentionally doped with low concentrations of arsenic donor species were found to be background p-type, and not background n-type after growth. In this talk, we will discuss the causes and consequences of this electrical conductivity type conversion, and we will identify the specific defect states that cause electrical conductivity type conversion in strain relaxed SiGe alloys. A careful comparison of our results on strain relaxed SiGe to previous results in plastically deformed bulk Si and bulk Ge indicates that the same electronic defect states are present in each case. Moreover, the same specific electronic defect states, located at the same energy position, pin the Fermi energy below midgap in strain relaxed SiGe and in plastically deformed bulk Si and bulk Ge. Thus, in Si, Ge, or SiGe samples that are lightly doped n-type, the defect states generated by dislocation nucleation and motion are capable of converting the conductivity of these samples from background n-type to background p-type. These results will be discussed and interpreted in terms of the Fermi-level stabilization theory and the Fermi-level effect in semiconductor crystals. According to the Fermi-level stabilization theory, any physical process that substantially damages a semiconductor crystal will create deep donor-like or deep acceptor-like defect states that always act to compensate the majority carrier doping species, and tend to pin the Fermi level near midgap in high resistivity samples. The implications of these results on electronic and optoelectronic device design will also be discussed for various technologies, including SiGe based devices, and III-V devices.

10:20 AM

C2, Fabrication of Relaxed SiGe-On-Insulator Substrates by Oxygen Implantation into Pseudomorphic SiGe/Si Heterostructure: *Zhenghua An*[1]; Ricky K.Y. Fu[1]; Peng Chen[1]; Miao Zhang[2]; Paul K. Chu[1]; Chenglu Lin[2]; [1]City University of Hong Kong, Dept. of Physics & Matls. Sci., Tat Chee Ave., Kowloon Hong Kong; [2]Shanghai Institute of Microsystem and Information Technology, State Key Lab of Functional Matls. for Informatics, 865 Changning Rd., Shanghai China

Tensile-strained silicon has been shown to possess higher electron and hole mobilities than single crystal silicon thereby offering an additional means to further improve the performance of metal-oxide-semiconductor (MOS) devices. Relaxed SiGe-on-insulator (SGOI) substrate that is a potential candidate for realizing strained-Si structures retains the good compatibility with the silicon integrated circuit technology. Most of the previous studies focus on SiGe materials with a thick SiGe buffer layer as the SIMOX (separation by implantation of oxygen) substrate resulting in SiGe/SiO2/SiGe/Si structures. This thick buffer layer is believed to be useful for suppressing Ge loss during high temperature annealing. However, besides the high cost, the buffer layer gives rise to some deleterious effects. For instance, the implanted oxygen is located in the SiGe layer, and Ge is rejected from the oxygen-rich region during the formation of the SiO2 buried layer resulting in a Ge concentration ceiling of about 14% for SiGe SIMOX. Moreover, the thick buffer layer adversely restricts the annealing temperature range since the melting point of SiGe decreases with increasing Ge, but the formation of the buried silicon dioxide layer requires higher temperature because of the required Ge rejection process. In the work reported here, we started with pseudomorphical SiGe/Si without a thick SiGe buffer layer as the SIMOX substrate and employed a modified SIMOX process to fabricate the SGOI structure. A 115nm thick SiGe film with a uniform Ge concentration of 14% was pseudomorphically grown on Si (100). An additional 8nm Si cap layer was deposited to prevent the SiGe from sputtering loss before 3x1017cm-2 of O+ was implanted into the interface of the SiGe/Si substrate at 550°C. A two-step annealing process was adopted to suppress Ge loss. The first step conducted at a moderate temperature of 800°C was used to improve the ability of the buried layer against Ge diffusion and the second annealing step at 1350°C formed the buried silicon dioxide layer with high quality. HRTEM (high resolution transmission electron microscopy) images confirm the formation of the fine SGOI structure with abrupt interfaces and also show the excellent microstructure in the SGOI film. The top SiGe/SiO2 interface is found to be even sharper than the SiO2/substrate interface. The usefulness of the first-step annealing is corroborated by RBS (Rutherford backscattering spectroscopy) in which reduced Ge loss during high temperature annealing is observed. Rocking curve results indicate that the final SGOI film is fully relaxed and the relaxation mechanism of the SGOI substrate is ascribed to a large slip between the top SiGe layer and buried oxide at high temperature.

10:40 AM Student

C3, Impact of Ion Implantation Damage and Thermal Budget on Mobility Enhancement in Strained Si n-MOSFETs: *G. Xia*[1]; H. M. Nayfeh[1]; M. J. Lee[1]; E. A. Fitzgerald[1]; D. A. Antoniadis[1]; J. L. Hoyt[1]; J. Li[2]; D. H. Anjum[2]; R. Hull[2]; [1]Massachusetts Institute of Technology, Microsys. Tech. Lab., 60 Vassar St., MIT 39-427A, Cambridge, MA 02139 USA; [2]University of Virginia, Dept. of Matls. Sci., Charlottesville, VA 22904 USA

Enhanced mobility and current drive have been demonstrated in strained Si n-MOSFETs, down to the smallest channel lengths fabricated thus far (~45 nm). As device channel length is scaled, the channel ion implant dose must be increased. In addition, with scaling, the lateral damage associated with the source/drain extension regions comprises a larger portion of the channel. Both of these effects increase the possibility of loss of mobility enhancement in scaled strained Si CMOS. Ion implantation damage may supply point defects that assist Ge diffusion and the relaxation of strain. Thermal processing can cause strain relaxation by the formation of misfit dislocations and Ge out-diffusion. Residual ion implantation damage, remaining after annealing, may act as carrier scattering centers. To investigate the impact of these processing factors on strain and mobility enhancement, long-channel strained Si and bulk n-MOSFETs were subjected to Si and Ge implants of varying dose, and the mobility and strain characteristics were analyzed. The strained Si layer was epitaxially grown on relaxed $Si_{0.8}Ge_{0.2}$ virtual substrates by UHVCVD. The layers were in-situ doped with boron to a level of 10^{17} cm^{-3}. The thickness of the strained Si layer was 18 nm prior to processing, and ~ 10 nm after processing. In order to avoid Coulomb scattering effects associated with channel dopant ionized impurities, neutral Si and Ge were implanted into the channel at energies in the range of 35 KeV, at six different doses ranging from 4 x 10^{12} to 1 x 10^{15} atoms/cm^2. The ion implants were performed prior to gate oxidation. The gate oxide was grown to a thickness of 5 nm at 800C. Three rapid thermal annealing (RTA) splits, 1000C-1s, 1000C-10s, and 950C-10s, were used to anneal the implantation damage and activate the source/drains. After processing, effective electron mobility measurements were made using the split-CV method. For strained Si n-MOSFETs with implantation, the

strained Si mobility enhancement factor (compared with the universal electron mobility of bulk Si n-MOSFETs without implantation) is degraded depending upon the implant dose and RTA. For each RTA condition, there is a threshold implantation dose, above which the strained Si mobility starts to degrade significantly. The threshold dose is smaller for devices with higher thermal budget. For 1000C-1s RTA and Si implant doses up to 3 x 10^{13} cm^{-2} (damage similar to 10 KeV B, 5 x 10^{14} cm^{-2}) no impact on strained Si electron mobility is seen. For 1000C-10s RTA, the Si implant threshold dose is reduced to 3 x 10^{12} cm^{-2} (damage similar to 10 KeV B, 7 x 10^{13} cm^{-2}). At a vertical effective field of 0.75MV/cm, the mobility enhancement factor is degraded from 1.6X to 1X for Si implant dose of 5 x 10^{14} and 1000C-1s RTA. For bulk Si control devices with implantation, mobility is degraded by 15% at most. The results will be discussed in terms of strain relaxation and residual ion implant damage observed by cross section transmission electron microscopy.

11:00 AM

C4, Impact of Virtual Substrate Ge Composition on Strained Si MOSFET Performance: *Sarah H. Olsen*[1]; Anthony G. O'Neill[1]; Sanatan Chattopadhyay[1]; Kelvin S.K. Kwa[1]; Luke S. Driscoll[1]; Steve J. Bull[2]; Andrew M. Waite[3]; Yue T. Tang[3]; Alan G.R. Evans[3]; David J. Norris[4]; Anthony G. Cullis[4]; Jing Zhang[5]; [1]Newcastle University, Sch. of Electl., Elect. & Compu. Engrg., Merz Ct., Newcastle upon Tyne NE1 7RU UK; [2]Newcastle University, Dept. of Mechl., Matls. & Mfg. Engrg., Newcastle upon Tyne NE1 7RU UK; [3]Southampton University, Dept. of Elect. & Compu. Sci., Southampton SO17 1BJ UK; [4]Sheffield University, Dept. of Elect. & Electl. Engrg., Sheffield S1 3JD UK; [5]Imperial College, Ctr. for Elect. Matls. & Devices, Physics Dept., London SW7 2BW UK

We report a study of strained Si MOSFETs fabricated with a high thermal budget, having virtual substrate (VS) Ge compositions varying from 0 to 30%. 15 nm of strained Si was grown on a relaxed VS of SiGe. Increasing the Ge fraction in the SiGe VS increases the amount of tensile strain in the Si layer. This reduces the critical thickness of strained Si, above which it becomes metastable and subject to relaxation during high temperature device fabrication. Ge diffusion also occurs during processing, which reduces device performance if it resides at the Si/SiO2 interface. Strained Si/SiGe MODFETs fabricated at low temperatures on Si0.7Ge0.3 virtual substrates show electron mobility enhancements greater than 50%, while strained Si MOSFETs fabricated at high temperatures on Si0.85Ge0.15 show good performance enhancements, but lower mobility compared with MODFET devices. Increasing the Ge composition in the VS is shown to result in significant enhancements in MOSFET drain current and transconductance due to increased strain in the device channels. Performance gains exceeding 200% compared with conventional unstrained devices are demonstrated. Performance advantages were found to saturate for VS Ge compositions greater than Si0.75Ge0.25, in good agreement with theory. These results demonstrate that maximum enhancements in the on-state electrical performance of strained Si surface channel MOSFETs are obtainable from high Ge composition VS material without compromising processing thermal budget. However, increasing the Ge composition above 20% also has the effect of significantly increasing the off-state leakage in many devices in our sample. For a Ge composition of 30%, all devices have a leakage current 100x greater than in the control Si devices. The reduction in device yield with increasing Ge composition is related to strain relaxation. The strain state has been studied by Raman spectroscopy and TEM and the gate oxide quality was investigated by C-V measurements. It is found that additional features in the C-V profile appear in all samples containing Ge, but the oxide leakage current is minimal. Dit measurements show an increase of more than one order of magnitude between the samples where the Ge composition is 15% to those where the Ge composition is 30%. The electrical data indicate the presence of excessive Ge at the Si/SiO2 interface resulting from diffusion during high temperature processing, which is also confirmed by SIMS. The low gate leakage current suggests a lack of hopping conduction through the oxide, so traps are believed to reside at the interface. Our results identify the appropriate parameter window for virtual substrate Ge composition and strained Si layer thickness, if acceptable Ion and Ioff MOSFET performance are to be achieved using a high thermal budget process.

11:20 AM Student

C5, Very High Hole Mobility Strained Si/SiGe Layers for p-Type Heterostructure-Based PMOS Devices at Room and Low Temperatures: *Corina Elena Tanasa*[1]; Dimitri Antoniadis[2]; Christopher Leitz[3]; Larry Lee[4]; Gene Fitzgerald[5]; Judy Hoyt[2]; [1]Massachusetts Institute of Technology, Electl. Engrg., 26 Olmsted Rd., Apt. C, Stanford, CA 94305 USA; [2]Massachusetts Institute of Technology, Electl. Engrg., Bldg. 39, 4th Floor, 60 Vassar St., Cambridge, MA 02139 USA; [3]AmberWave Systems, 13 Garabedian Dr., Salem, NH 03079 USA; [4]Massachusetts Institute of Technology, Matls. Sci. & Engrg., 77 Mass. Ave., Bldg. 12-007, Cambridge, MA 02139-4307 USA; [5]Massachusetts Institute of Technology, Matls. Sci. & Engrg., 77 Mass. Ave., Bldg. 13-5153, Cambridge, MA 02139 USA

Heterostructure-based PMOS devices with the composition of strained Si on relaxed SiGe, and of strained Si on strained SiGe on relaxed SiGe, are studied, where the strained SiGe layers are Si(40%)Ge(60%) and Si(20%)Ge(80%), and the relaxed layer is Si(70%)Ge(30%). Previously measured mobilities for these devices at 300K, averaged over all the layers of the heterostructure, were of 350 to 550 cm2/Vs at 0.4MV/cm effective field.[1] The same mobilities are now measured at 150K and 200K and mobility values up to 1200 cm2/Vs are obtained. The slopes of the graphs of mobility vs. effective field are extracted and the mobility degrading mechanisms of phonon scattering and surface scattering are identified for each of the heterostructure layers, at room and low temperature. The exponential coefficients of mobility dependence on effective field for each mechanism are obtained, with values - 1.4 for phonon scattering at 300K, and - 2 for surface scattering at 150K, in the surface strained Si channel, and - 0.7 for phonon scattering at 300K, and about 0 for phonon scattering at 150K, in the buried strained SiGe channel. The CV curves of the PMOS devices are then modeled in MEDICI. Effective field and inversion charge population versus gate voltage are obtained for each of the strained Si/strained SiGe/relaxed SiGe inversion layers. From the experimental data and the modeling data a newly proposed algorithm is able to extract the mobilities in each of the individual inversion layers (not averaged over the layers). Values of 250 cm2/Vs at 0.35 MV/cm effective field in strained Si surface channel, and 360 cm2/Vs at 0.16 MV/cm in strained Si(40%)Ge(60%) buried channel, are obtained. The interplay between gate voltage, inversion carrier concentration, screening effect and thickness of the strained Si and SiGe layers is fully explained. [1]C.W.Leitz, M.T.Currie, M.L.Lee, Z.Y.Cheng, D.A.Antoniadis, E.A.Fitzgerald, 'Hole Mobility Enhancements in Strained Si/SiGe p-Type MOSFET Grown on Relaxed SiGe Virtual Substrates', Appl. Phys. Lett. 79, 4246 (2001).

11:40 AM

C6, Partially- and Fully-Depleted Strained Si/Si1-yGey MOSFETs Fabricated on Relaxed Si1-xGex-On-Insulator (SGOI): *Zhiyuan Cheng*[1]; Jongwan Jung[2]; Arthur J. Pitera[1]; Minjoo L. Lee[1]; Hasan Nayfeh[2]; Judy L. Hoyt[2]; Dimitri A. Antoniadis[2]; Eugene A. Fitzgerald[1]; [1]Massachusetts Institute of Technology, Dept. of Matls. Sci. & Engrg., 77 Massachusetts Ave., Cambridge, MA 02139 USA; [2]Massachusetts Institute of Technology, Dept. of Electl. Engrg. & Compu. Sci., 77 Massachusetts Ave., Cambridge, MA 02139 USA

Relaxed Si1-xGex-on-insulator (SGOI) is a promising technology that combines the benefits of an insulating substrate with the enhanced current drive and speed associated with channel materials such as strained Si and strained Si1-yGy. Key device issues for this technology include optimization of the heterostructure layer stack for enhancement of both n- and p-MOSFET performance, and potential influence of the SiGe/buried-oxide interface on performance of fully-depleted SGOI. From a materials growth point of view, optimization of epitaxial regrowth of strained Si on SGOI substrates must be addressed. To examine these issues, fully- and partially-depleted strained Si on SGOI n- and p-MOSFETs are fabricated and compared. The influence of the thickness of re-grown SiGe on the performance of strained Si/relaxed Si1-xGex SGOI n-MOSFETs is investigated. Finally, dual-channel (strained Si/strained Si1-yGy/relaxed Si1-xGx) MOSFETs are demonstrated on SGOI. In a surface channel SGOI CMOS structure, the strained-Si surface channel provides mobility enhancement for both electrons and holes. To further boost hole mobility, a dual-channel structure can be utilized, where a compressively strained Si1-yGey layer and then a tensile strained Si cap layer are grown on the relaxed Si1-xGex-on-insulator (SGOI) substrate (y>x). The strained Si layer is used as the electron channel layer for n-MOSFET's (surface channel) and the strained Si1-yGey is used as the hole channel for p-MOSFET's (buried channel). Both n- and p-MOSFET's SGOI structures were demonstrated in this work. The gate oxide thickness was 5 nm. Relaxed-SiGe-on-insulator substrates were fabricated using a wafer-bonding and etch-back approach where 20% SiGe was

used as an etch-stop. For the surface-channel devices, the SGOI substrate was then put back into the UHVCVD reactor to grow a thin relaxed-Si0.78Ge0.22 layer followed by a strained-Si channel layer. In order to study the impact of the regrown material quality, three different structures were grown with the thickness of the re-grown Si0.78Ge0.22 layer varying from 0, to 5, to 150nm. The structure with no Si0.78Ge0.22 regrown layer shows degraded mobility throughout the entire vertical effective field range. Regrowth of a very thin (i.e. 5 nm) Si0.78Ge0.22 layer before strained Si deposition results in the same mobility enhancement as regrowth of a thick (150 nm) Si0.78Ge0.22 layer. It is thus recommended that a thin layer of SiGe be grown prior to strained Si regrowth. Partially depleted surface strained Si n- and p-MOSFETs show well behaved characteristics, with mobilities comparable to those measured on bulk relaxed SiGe virtual substrates. However, the measured sub-threshold swing for fully-depleted devices is larger than that of partially-depleted SGOI MOSFETs. This effect may be related to traps at the interface between the relaxed Si0.78Ge0.22 and the buried oxide. Dual-channel structures consisting of strained-Si/strained-Si0.4Ge0.6/relaxed-Si0.7Ge0.3 on SGOI were also fabricated. Although the hole mobility was enhanced, the enhancement was dramatically reduced for devices that received an 850C-30 min source/drain annealing step, compared to those annealed at 600C.

Session D: Spin-Dependent (or Spintronic) Electronic Materials - I

Wednesday AM Room: 101
June 25, 2003 Location: Olpin Union Building

Session Chairs: Chris Palmstrøm, University of Minnesota, Dept. of Chem. Engrg. & Matls. Sci., Minneapolis, MN 55455 USA; Stefano Sanvito, Trinity College, Dept. of Physics, Dublin 2 Ireland

10:00 AM

D1, High Efficiency Spin Injection from a Ferromagnetic Metal into a Semiconductor Through Fe/InAs Junction: *Kanji Yoh*[1]; Hiroshi Ohno[2]; Kazuhisa Sueoka[2]; Koichi Mukasa[2]; Manfred E. Ramsteiner[3]; [1]Hokkaido University, RCIQE, N13,W8, Kita-ku, Sapporo, Hokkaido 060-8628 Japan; [2]Hokkaido University, Grad. Sch. of Engrg., N13, W8, Kita-ku, Sapporo, Hokkaido 060-8628 Japan; [3]Paul Drude Institute, Hausvogteiplatz 5-7, Berlin D-10117 Germany

Spin-injection from ferromagnetic metals into semiconductors is one of the key technologies to achieve spintronics[1] in the future. In spite of its potential importance, there have been keen discussions on whether or not an efficient spin injection into semiconductor is possible at all. Experimentally, spin injection from high Tc ferromagnetic metals into semiconductor has been reported by several groups[2] in Fe/GaAs system where electrons tunnel through a Schottky barrier which would limit the drain current drastically. Besides, those tunneling barriers, which might work as a spin filter, are believed to be the very reason which enables spin-injection through ferromagnet/semiconductor junction. There have been theoretical controversy[3,4] on the topic. We have been demonstrating the spin injection, where there is no Schottky barriers in Fe/InAs hybrid structure with the injection efficiency of ~12%.[5] The crystal quality bcc Fe thin film was grown on zinc-blend p-type InAs wafer in a ultra-high-vacuum. Fe film was patterned into line/space array (width: w = 2μm, pitch: p = 4μm,) so that it circularly polarized light could be observed at the top of the sample in parallel to the external magnetic field. In flat-band condition, ballistically injected electrons readily recombine with holes in the p-type InAs and emit photons. A clear electro-luminescence was detected from the top of the sample by the InSb photo-detector. The σ^+ and σ^- components of the luminescence were measured by switching the angle of the quarter-wave plate. The external magnetic field dependence of the polarization efficiency calculated by the measured results of the σ^+ and σ^- components intensity of the luminescence PL. Considering the opposite polarization behavior from the non-magnetic sample and photoluminescence results, which is due to the Zeeman effect, the net polarization in the Fe electrode is estimated to be much higher, approaching a theoretical limit of 20-25% with the current measurement method. Taking into account both spin polarization of 40% to 45% of the Fe spin injector[6], and optical selection rules for electrolumoinescence from both heavy and light hole contributions yielding maximum 50% spin polarization, one can roughly estimate high spin injection efficiency of 80-90% at the Fe/InAs junction. These results clearly indicate that the high efficiency spin injection in the FM/SC hybrid system is possible without a tunneling barrier. [1]S. Datta and B. Das; Appl.Phys.Lett. 56 (1990) 665. [2]H. J. Zhu et al, Appl.Phys.Lett. 80 (2001) 016601. [3]P. C. van Son et al, Phys.Rev.Lett. 58 (1987) 2271. [4]O. Wunnicke et al, Phys.Rev.B 65 (2002)24136(R). [5]H. Ohno et al, Jpn.J.Appl.Phys.Vol.42 (2993) pp.L1-L3 Part 2, No.2A, 1 February 2003. [6]R. J. Soulen et al, SCIENCE, 282, pp.85-88 (1998).

10:20 AM Student

D2, $Fe_{1-x}Co_x$/GaAs Spin Polarized Transport Devices: Growth, Characterization, and Transport Measurements: *B. D. Schultz*[1]; J. Strand[2]; A. F. Isakovic[2]; C. Adelmann[1]; P. A. Crowell[2]; C. J. Palmstrøm[1]; [1]University of Minnesota, Chem. Engrg. & Matls. Sci., Minneapolis, MN 55455 USA; [2]University of Minnesota, Sch. of Physics & Astron., Minneapolis, MN 55455 USA

The interfacial properties and reactions of epitaxial ferromagnetic metals and semiconductors are important for minimizing spin randomized scattering effects and for optimizing the spin injection efficiency across metal/semiconductor interfaces. In-situ AES and XPS of MBE grown Fe deposited on GaAs indicates significant reduction in the Fe-Ga-As reactions by lowering the growth temperature below 100°C. For Co deposition on GaAs, even lower growth temperatures are required to limit the Co-Ga-As reactions. $Sc_{1-y}Er_yAs$ interlayers have been used to further reduce these ferromagnet-Ga-As reactions. In-situ STM images show preferential attachment of the $Fe_{1-x}Co_x$ atoms on the GaAs while no preferential attachment occurs on the $Sc_{1-y}Er_yAs$ interlayers. Spin based LED devices consisting of $Al_{1-x}Ga_xAs$ quantum wells embedded within the depletion region of an n-p diode are used to measure the injection of spin polarized carriers across the $Fe_{1-x}Co_x$/semiconductor interface. Electrons are injected through a delta-doped Schottky tunnel barrier to circumvent the inherent problems associated with spin injection using diffusive transport contacts. Doping profiles are used to control both the width of the Schottky barrier and the carrier concentration in the drift region between the interface and the quantum well spin detector. Optimization of the semiconductor LED structure was undertaken in order to improve the efficiency of polarized light emission. The electroluminescence polarization as a function of wavelength, electrical bias, perpendicular magnetic field and temperature was measured and compared with the photoluminescence under identical conditions for both ferromagnetic Fe/$Al_{1-x}Ga_xAs$ and nonmagnetic Al/$Al_{1-x}Ga_xAs$ LED structures. Measurements of the bias dependence at 5.0 T and 10 K show a peak in the optical polarization signal at low bias voltages and a slow decrease in the signal at higher bias. Evidence of nuclear polarization by electrical spin injection in these $Fe_{1-x}Co_x$/GaAs heterostructures has also been observed using small (<500 Oe) in-plane magnetic fields and the electroluminescence polarization as a probe of carrier spin dynamics. The optical polarization signal tracks the in-plane Fe magnetization, and it also demonstrates hysteresis. A dynamical model has been used to fit the experimental data using parameters determined from optical Hanle effect measurements. The data and the model indicate the build-up of a large nuclear magnetic field in the semiconductor. This paper will emphasize the material design issues of the $Fe_{1-x}Co_x$/GaAs interface and LED structures as well as the measurements of spin polarized transport across the $Fe_{1-x}Co_x$/$Al_{1-x}Ga_xAs$ interface. This research was supported in part by the ONR N/N00014-1-0233, DARPA N/N00014-99-1-1005, DARPA N/N00014-01-1-0830, NSF/DMR-9819659, and NSF-MRSEC NSF/DMR-9809364.

10:40 AM

D3, On Spin Loss During Optical Spin Injection in ZnMnSe/CdZnSe Quantum Structures: *I. A. Buyanova*[1]; W. M. Chen[1]; K. Kayanuma[2]; Z. H. Chen[2]; A. Murayama[2]; Y. Oka[2]; A. A. Toropov[3]; Ya V. Terent'ev[3]; S. V. Sorokin[3]; A. V. Lebedev[3]; S. V. Ivanov[3]; P. S. Kop'ev[3]; [1]Linkoping University, Dept. of Physics & Measurement Tech., Linkoping 58183 Sweden; [2]Tohoku University, Inst. of Multidisciplinary Rsch. for Advd. Matls., Sendai 980-8577 Japan; [3]A.F. Ioffe Physico-Technical Institute, Russian Academy of Sciences, St. Petersburg 194021 Russia

Efficient spin injection across a semiconductor heterointerface is one of the key issues in determining the success of future spintronic devices, and has therefore received great research interest in recent years. Though the efficiency of electrical spin injection has been demonstrated to be higher, the efficiency of optical spin injection is still rather limited (i.e. typically less than 30%). The exact mechanism for the reduced optical spin injection efficiency is up to now unknown, as many physical processes are involved during the spin injection. The aim of this work is to carry out an in-depth investigation of physical processes causing spin loss during optical spin injection from the ZnMnSe-based diluted magnetic semiconductors (DMS) to an adjacent nonmagnetic ZnCdSe quantum well (QW) as a spin detector. Both cw- and time-resolved photoluminescence (PL) spectroscopies with tunable laser excitation were employed. By selective excitation of only the lowest lying spin state of the DMS exciton in an applied magnetic field, a complete spin polarization within the DMS can be ensured and its role in spin loss can therefore be excluded. The limited spin injection efficiency of about 30% observed in the cw PL studies is therefore caused by spin loss across the heterointerfaces and during the energy relaxation within the QW. From the time-resolved PL studies it is shown that the QW PL decays upon spin injection from the DMS in two characteristic times, about 100 ps and 600-700 ps, respectively. The fast component (representing the main portion of the QW PL) exhibits extremely fast spin depolarization (within tens of ps), providing explanation for the observed limited efficiency of optical spin injection. The fast spin depolarization is believed to be due to efficient spin relaxation accompanying energy relaxation of hot excitons and hot carriers within the QW subjected to the injection of the DMS exciton spins. This is consistent with the observation of decreasing spin polarization with increasing excitation photon e nergy, with respect to the bottom of the QW exciton, in optical orientation experiments. The spin polarization of the slow component of the QW PL decay, on the other hand, is shown to remain for a rather long time (> ns) and is a result of the spin injection from the DMS. The mechanism for this slow and spin polarized process is discussed in terms of a delayed spin injection arising from one of the particles of the DMS exciton or/and from trapped spins in the DMS. Financial support from the Swedish Research Council (VR) and the Swedish Foundation for International Cooperation in Research and Higher Education (STINT) is greatly appreciated.

11:00 AM

D4, Ultrafast Spin Dynamics Monitored by Pump-Probe Second Harmonic Generation: *Norman H. Tolk*[1]; Yuri D. Glinka[1]; T. V. Shahbazyan[1]; I. E. Perakis[1]; Jerome K. Miller[1]; Yingying Jiang[1]; Mikel E. Barry[1]; X. Liu[2]; Y. Sasaki[2]; J. K. Furdyna[2]; [1]Vanderbilt University, Physics & Astron., VU Sta. B 1807, Nashville, TN 37235 USA; [2]University of Notre Dame, Physics, Notre Dame, IN 46556 USA

Ultrafast spin-sensitive spectroscopy provides unique information about spin relaxation in semiconductor heterostructures as well as spin-polarized electron transport across interfaces. Knowledge of the processes governing spin dynamics is essential for designing novel multifunctional electronic and opto-electronic devices, including base components for quantum computing. Among the wide variety of multilayer semiconductor systems, GaSb/InAs heterostructures are especially promising. The excitation of an ensemble of spins by circularly polarized laser light at the photon energy just above the band gap gives rise to a net magnetization. The typical time resolved techniques, such as polarized photoluminescence spectroscopy, pump-probe transmission/reflection and Faraday or Kerr rotation, all rely on the linear response of the spin subsystem to the probing light, and are well suited for monitoring the spin dynamics in the bulk of semiconductor structures. On the other hand, the nonlinear optical effects, such as second harmonic generation (SHG), are known to be highly sensitive to local magnetic fields occurring at magnetized surfaces and at interfaces in magnetic-semiconductor-based multilayers. Therefore, the application of SHG in the pump-probe configuration has become a promising method for studying the spin dynamics at the interfaces of semiconductor structures. We report the first application of ultrafast pump-probe SHG measurements to characterize optically induced magnetization in non-magnetic GaAs/GaSb and GaAs/GaSb/InAs heterostructures. A normally incident circularly polarized pump beam of 150 fs pulse duration is used to create selectively an excess of spin-polarized electrons in the GaAs epilayer. A linearly polarized probe beam from the same source is used to measure the SHG signal in reflection geometry. The pump-induced SHG signal, which is monitored as a function of probe-to-pump delay times, is due to interfacial electric and magnetic fields created by the pump-excited carriers. Only the GaAs/GaSb/InAs samples show a significant induced magnetization, indicating a spin-polarized electron transport across the heterostructure. The temperature dependence of the induced SHG signals in the range 4.3-300 K reveals two distinct processes that affect the magnetization dynamics: the evolution of the local spin density at the interfaces and the spin relaxation.

11:20 AM

D5, Anisotropy of Spin Dephasing Rates in Quantum Wires: *Supriyo Bandyopadhyay*[1]; Sandipan Pramanik[1]; [1]Virginia Commonwealth University, Electl. Engrg., 601 W. Main St., Richmond, VA 23284 USA

We have studied spin dephasing in compound semiconductor quantum wires due to the D'yakonov-Perel' mechanism. Spin dephasing due to both bulk inversion asymmetry (Dresselhaus spin orbit interaction) and structural inversion asymmetry (Rashba spin orbit coupling) have been considered. The spin precession equation has been solved self-consistently with the Boltzman Transport Equation to evaluate the dynamical spin vector as a function of time. The Boltzmann equation yields the instantaneous value of the carrier wavevector which enters the spin precession equation. The Boltzman Equation has been solved using an ensemble Monte Carlo simulator where both carrier and phonon confinement effects are accounted for. We have considered carrier interaction with polar and non-polar acoustic phonons, polar and non-polar optical phonons, and surface phonons. We found that the spin dephasing rate is strongly sensitive to the electric field causing carrier transport. The rate goes up by three orders of magnitude if the field is increased from 200 V/cm to 2000 V/cm. There is also a significant anisotropy in the depahsing rate. If the initial injected spins are parallel to the axis of the quantum wire, the spin dephasing time in GaAs or InAs is several tens of nanoseconds at 77K, while if the spin is injected perpendicular to the wire axis, the dephasing time drops to tens of picoseconds. This has important consequences for the design of spintronic devices such as spin interferometers based on the Rashba effect. Additionally, we have found that the steady state spin "distribution function" (the distribution of the x-, y- and z-components of the spin vector) are very different depending on whether spin is injected parallel or perpendicular to the wire axis. For parallel injection, the distribution function is approximately Gaussian and peaked around zero, while for perpendicular injection, the distribution function is uniformly distributed between the extremal values of -1 and +1. This feature can be explained by invoking the relative importance of the Dresselhaus effect and the Rashba effect.

11:40 AM Cancelled

D6, Comparison of Electron Spin Relaxation Times in GaAs and GaN: *Srini Krishnamurthy*[1]; Mark van Schilfgaarde[2]; Nathan Newman[2]; [1]SRI International, Appl. Physl. Scis., 333 Ravenswood Ave., 306-21, Menlo Park, CA 94025 USA; [2]Arizona State University, Chem. & Matls. Engrg., PO Box 876006, Tempe, AZ 85287-6006 USA

Creation of realistic spin injection devices require injector material with coherent spin population at room temperature, efficient spin injection, spin relaxation and manipulation in the active device material, and spin detection. The conductivity match between the injector and active device material is expected to enhance spin-injection efficiency. While several material systems are being considered for spin injection and manipulation, we explore GaMnN/GaN combination for spin injection devices because of the higher curie temperature of 650 K expected in GaMnN alloy. In the GaN device region, it is essential to understand the limitations of various spin scattering mechanism on injected electrons' spin depolarization. With a combination of long range tight-binding and empirical pseudopotential band structures, we calculated the spin relaxation times in GaAs and GaN. Spin scattering due to Elliot-Yafet, D'yakonov-Perel (DP), and Bir-Aronov-Pikus mechanisms are considered within second-order perturbation theory. The calculated temperature-dependent spin lifetimes in GaAs agrees very well with recent measurements.[1] Similar calculations carried out in GaN indicate that the electron spin lifetimes are about three orders of magnitude larger than that in GaAs, in the temperature range of 5 K to 300 K. We further find that the spin relaxation time decreases sharply with injected electron energy. However, because of the dominant DP scattering mechanism, we find it advantageous to inject electrons at the state with threshold energy for the emission of a longitudinal optic phonon. We expect GaN to perform considerably better than GaAs in spin injection devices. The spin life-

times in GaAs and GaN, calculated as functions of temperature, injection energy, and impurity (both n and p) doping density will be presented. The comparison with GaAs experiments will be made. [1]J.M. Kikkawa and D.D. Awschalom, Phys. Rev. Lett., 80, 4313 (1998).

Session E: III-V Low-Dimensional Structures

Wednesday AM Room: 102
June 25, 2003 Location: Olpin Union Building

Session Chairs: Ben Shannabrook, Naval Research Laboratories, Nanostruct. Sect., Washington, DC 20375-5000 USA; Mark Miller, University of Utah, Salt Lake City, UT 84112-0506 USA

10:00 AM

E1, Controlling the Electronic States of Self-Assembled InAs Quantum Dots by using InGaAs Layer: *Jin Soo Kim*[1]; Jin Hong Lee[1]; Sung Ui Hong[1]; Won Seok Han[1]; Ho-Sang Kwack[1]; Dae Kon Oh[1]; [1]Electronics and Telecommunications Research Institute (ETRI), Basic Rsch. Lab., 161 Gajeong-dong, Yuseong-gu, Daejeon 305-350 Korea

Self-assembled InAs quantum dots (QDs) with different structure of InGaAs layer were grown and their structural and optical properties were investigated by transmission electron microscopy (TEM) and photoluminescence (PL) spectroscopy. By varying the thickness of InGaAs overgrowth layer on 3.2 monolayer InAs QDs, the shape, especially the height was systematically controlled resulting in the change of optical properties. The emission wavelength of InAs QDs covered by 8.5 nm InGaAs layer is 1.30 μm at room temperature with energy-level spacing of 80 meV between the ground state and the first excited state, which is about 1.5 times larger than that of InAs QDs embedded in GaAs matrix. The enlarging in energy-level spacing can be attributed to the fact that wave-function of QDs can be more confined in the QD with high aspect ratio (height/width), which was confirmed by TEM images, leading to the stronger quantum confinement effects. By inserting 1 nm thin InGaAs layer below the InAs QDs with 6 nm InGaAs overgrowth layer, the peak position was red-shifted with larger energy-level spacing compared to that of QDs with InGaAs overgrowth layer only. The PL peak position of InAs QDs covered by $In_xGa_{1-x}As$ layer with graded In composition was 1.33 μm at room temperature with energy-level spacing of 85 meV and narrower PL linewidth. From these results, device performances of QD laser diode such as thermal stability can be significantly improved by controlling the aspect ratio of QDs by using InGaAs layer.

10:20 AM

E2, Photoexcited Carrier Dynamics in Self-Assembled InAs/AlAs Quantum Dots: *Z. Ma*[1]; K. Pierz[1]; P. Dawson[1]; E. O. Göbel[1]; J. Hübner[2]; M. Oestreich[3]; W. W. Rühle[2]; Z.-X. Ma[4]; [1]Physikalisch-Technische Bundesanstalt, Lab. 2.41, Bundesallee 100, Braunschweig 38116 Germany; [2]Philipps-Universität Marburg, Fachbereich Physik, Renthof 5, Marburg 35032 Germany; [3]Universität Hannover, Institut für Festkörperphysik, Appelstr. 2, Hannover 30167 Germany; [4]Brooklyn College, Physics Dept. and NYSCAT, 2900 Bedford Ave., Brooklyn, NY 11210 USA

Photoexcited carrier dynamics in self-assembled InAs-based quantum dots have been intensively studied in recent years. Usually, a photo-created electron-hole pair in the barrier or wetting layer is captured in the same quantum dot on the time scale of 100 picoseconds and radiatively recombine in the quantum dot within a lifetime of order of nanoseconds. It has been demonstrated, however, that by either varying the relative diffusivity of electrons and holes or by reducing the ratio of electron/hole density to quantum dot density, it is possible to create a situation where the electron and the hole are captured by adjacent quantum dots. This situation is considerably enhanced by appearance of X-states in the barriers resulting in microsecond carrier recombination times. The self-assembled InAs quantum dots were grown by solid-source MBE at 510°C . The dot diameter and density of the dots are ~10 nm and ~10^{12} cm^{-2}, respectively. TEM images show that the large dots are spatially close while the small ones are more distant. Due to the existence of X-states in the AlAs barriers, the carrier dynamics are much different from other quantum dot systems. We report here on time-resolved photoluminescence spectra in the range up to 1.8 nanoseconds and on excitation power dependence of the photoluminescence of InAs/AlAs quantum dots, at a temperature of 6K. For the time-resolved spectra, the quantum dot ground state emission peaked at around 1.6 eV initially shifts to lower energies and then to higher energies at ~1 nanosecond, while it continuously shifts to lower energies as much as ~35 meV with increasing excitation power density from 0.008 to 1300 W/cm^2, accompanied by a shrinkage of linewidth. In our measurements, the electron/hole pairs were mainly excited in the wetting layer and across the type II energy gap formed by the AlAs X-states and the confined hole states in the quantum dots. The electrons can be scattered into adjacent dots via AlAs X-states, resulting in separation of electrons and holes. Since the overlap of wave function of electrons and holes strongly depends on the distance between dots, the life-time varies with emission energy. Recombination of electrons and holes in closer quantum dots, which occurs at low energies, is faster than recombination involving quantum dots with larger distance. This explains the blueshift in time-resolved spectra and the red shift of ground state emission as well as the dependence of the spectra on excitation power. The initial red shift in time-resolved spectra might be due to the carrier transfer into larger dots as observed in conventional InAs/GaAs quantum dots. If this is the case, carrier tunnelling between spatially close dots will lead to a fast decay in the time scale of nanoseconds.

10:40 AM Student

E3, Growth of Uniform InAs Quantum Dots on Strain Modulated InGaAs Superlattice: *Zhenhua Zhang*[1]; Kuang-Chien Hsieh[1]; Keh-Yung Cheng[1]; [1]University of Illinois at Urbana-Champaign, Dept. of Electl. & Compu. Engrg., 150 Micro & Nanotech. Lab., 208 N. Wright St., Urbana, IL 61801 USA

Recently, extensive research has been devoted to the quantum dot (QD) nanostructures for their attractive physical properties expected from the 3-D carrier confinement. In particular, InP based InAs QDs are attracting more attentions for their abilities to work as light emitters in the long wavelength (1.3-1.55 μm) region. When forming InAs nanostructures on different matrix layer materials, such as InGaAs, AlInAs, InAlGaAs, and InGaAsP, both QDs and quantum wires (QWRs) were observed under different growth conditions. However, the mechanism of morphology control on the QDs formation is not fully understood and requires further investigation. There are many parameters evolving in the formation of InAs nanostructures on InGaAs matrix layer. In order to achieve randomly distributed QDs, two important factors are considered, i.e., the strain field caused by phase separation in the matrix layer; and the anisotropic surface diffusion of the incoming In atoms. Both phenomena prefer the formation of QWRs along [1-10] direction. Our previous researches have shown that thick (9 ML) InAs layer and high growth temperature can be used to overcome the wire formation. However, large, non-uniform QDs with relatively low density achieved under these conditions are not suitable for laser device applications. In this study, instead of the thick InAs layer, 2-4 ML InAs was deposited on a strain modulated InGaAs superlattice layer to form InAs QD nanostructures on InP substrate using molecular beam epitaxy (MBE) technique. The strain modulated matrix layer was formed using a multi-period III-stabilized (20Å)/V-stabilized (20Å) InGaAs superlattice layer grown on the bulk InGaAs buffer layer. The III-stabilized InGaAs layer was grown under lower arsenic overpressure while other growth conditions were kept identical to the V-stabilized InGaAs layer. It has been shown experimentally that thick III-stabilized InGaAs layer leads to the wire formation along [110] direction on the growth front. Hence, by repeating these two structures periodically, the modulated InGaAs matrix layer can effectively modify the strain distribution in matrix layer and prevent the anisotropic surface diffusion during QDs growth. As a result, uniform QD nanostructures were observed. Compared with our previous results using thick InAs layer, the average diameter of QDs grown on strain modulated matrix layer was decreased from 50 nm to 40 nm and the standard deviation was decreased from 18.6 nm to 14.0 nm, which is a 25% improvement showing the better uniformity. Meanwhile, the density of QDs was increased from 1.8×10^{10} cm^{-2} to 5×10^{10} cm^{-2}. The data proves that the strain modulated InGaAs superlattice layer is an effective way to achieve good InAs QDs morphology on InGaAs/InP. With further optimization of the growth process, light-emitting QDs devices operating at a wavelength of 1.55 μm may be fabricated.

11:00 AM Student

E4, Effect of InAlGaAs Lateral Potential Confinement Layer on InAs Quantum Dot Infrared Photodetectors: *Eui-Tae Kim*[1]; Max Ho[1]; Zhonghui Chen[1]; Zhengmao Ye[2]; Joe C. Campbell[2]; Anupam Madhukar[1]; [1]University of Southern California, Nanostruc. Matls. & Devices Lab., 3651 Watt Way, VHE514, Los Angeles, CA 90089 USA; [2]University of Texas at Austin, Microelect. Rsch. Ctr., Bldg. 160, 10,100 Burnet Rd., Austin, TX 78712 USA

Intensive research is focused on the applications of strain-driven coherent island based InAs/GaAs quantum dots (QDs), such as lasers and infrared photodetectors. Understanding and manipulation of the electronic states of these QDs are central to exploiting their full potential. Tuning of the QD electronic structure can be achieved by varying QD size, QD capping layers, or thermal annealing. Most such approaches affect the QD electronic structure as a whole and do not allow tuning primarily subsets of QD states. Recently, we demonstrated the possibility to manipulate specific subsets of QD states using a lateral potential confinement layer (LPCL) positioned at different height of QDs.[1] Such a selective manipulation of QD states is very useful for tuning detection bands of quantum dot infrared photodetectors (QDIPs). In this presentation, we report an LPCL effect on QDIP performance and high excited states involved in intraband transitions in QDIPs. For this study, QD and QDIP samples were grown by molecular beam epitaxy on (001) undoped GaAs under As pressure of $7.0x10^{-6}$torr. InAs QDs were formed by 2.5ML InAs deposition at the rate of 0.054ML/sec at 500°C. The 2.5ML InAs QD layer shows very uniform QD size uniformity (a full width at half maximum of 23meV in photoluminescence (PL) peak at 78K) and thus is a good candidate for the study on QD electronic structure. The QDIPs (n-i(QD)-n) comprised a stack of 5 InAs QD layers with 200ML spacers and silicon-doped top and bottom contact layers. The InAs QDs capped by 30ML $In_{0.15}Ga_{0.85}As$ and GaAs layers were used as a reference. To investigate the change in the electronic states of such QDs/QDIPs by a LPCL positioned at the bottom, upper, and top region of the QDs, 10MLs of the 30ML $In_{0.15}Ga_{0.85}As$ were replaced by $In_{0.15}Al_{0.25}Ga_{0.60}As$. The PL and PLE studies show that the electron and hole ground states and the first subset of excited hole states are perturbed most effectively by the LPCL located in the bottom region of QDs, indicating that the charge center of gravity of these states resides near the QD bottom. However, in these studies, the LPCL effect on higher excited states than the second could not be seen. Thus, photocurrent (PC) spectroscopy utilizing a Fourier transform infrared spectrometer is used to investigate the LPCL effect on QD high excited states involved in intraband transitions in QDIPs. The complementary information obtained from PL, PLE and PC spectroscopies provide a more comprehensive view of the electronic structure of such QDs. In addition, the LPCL acts as a dark current blocking layer and provides a means of enhancing QDIP performance. Work supported by AFOSR under the MURI 98 program on nanoscience. [1]E.T.Kim, Z.H.Chen, and A.Madhukar, Appl. Phys. Lett 81, 3473 (2002).

11:20 AM

E5, Determination of Subband Energy Levels of DQW AlGaAs Lasers by Photo-Reflectance and Self-Excited Electron Raman Scattering at 300K: *Wataru Susaki*[1]; [1]Osaka Electro-Communication University, 18-8 Hatsu-Cho, Neyagawa 572-8530 Japan

It is a key issue to determine the subband energy levels of electrons and holes in quantum well (QW) lasers for design improvement of characteristics such as very low temperature sensitive threshold current by complete confinement of injected carriers in QWs. We have observed self-excited electronic Raman scattering (ERS) spectra at room temperature above threshold from InGaAs and InGaP QW lasers.[1, 2] In this paper, subband energy levels of AlGaAs double quantum well (DQW) layer structure with a separate confinement scheme are determined by photoreflectance at room temperature. Also subband energy levels are compared with those determined by the self-excited ERS of lasers fabricated from the wafer. Subband energy levels determined by both measurements are a good agreement. The layer is grown on a GaAs substrate by MOCVD.[3] Two 8nm-Al0.1Ga0.9As-QWs are formed in Al0.35Ga0.65As wavegide/barrier layers. These layers are not doped and surrounded by n- and p-Al0.48Ga0.52As cladding layers (>1mm). The thickness of Al0.35Ga0.65As waveguide adjacent to the n-Al0.48Ga0.52As cladding layer is 10nm and that adjacent to the p- Al0.48Ga0.52As cladding layer is 12nm. The barrier layer surrounded by QWs is 8nm thick. Photoreflectance of the layer is measured using a stabilized 532nm SHG YAG laser modulated at 720Hz by an optical chopper to modulate electric field by creating photo excited carriers in p-cladding layers. Carriers in the waveguides, the barrier, and QW layers are completely depleted and carriers adjacent to regions of n- and p-cladding layers are also depleted. It will be reasonable to assume that the electric field F in the non-doped layers (wavegude/QW/barrier/QW/waveguide) is constant. F is determined from Frantz-Keldish oscillation frequencies in the waveguide cladding layers. The determined F is 90kV/cm. The subband energy difference between the second electron subband level e2 and the first electron subband level e1 is 91meV. e2-e1 determined by the self-excited ERS from lasers is 105meV. The discrepancy of e2-e1 is due to F in the layers. F is negligibly small because of extremely high-injected carrier density (~5x10^18/cm3) at threshold in lasers. The subband levels and wave functions are calculated by a finite difference numerical method of the Schroedinger equation using the conduction band offset ratio to the bandgap energy difference 0.64 (determined from the ERS). e2-e1 decreases by the Stark shift from 105meV to 90meV, which shows a good agreement between both measurements. Details of the determination of subband levels of the DQW layer by photo-reflectance will be reported. References: [1]W. Susaki, et al., Proc. SPIE, 4287, 176(2001). [2]W. Susaki, et al., Proc. ISCS, 227(2001). [3]A. Shima, et al., Proc. SPIE, 4248, 48(2001).

Session F: Materials Integration: Wafer Bonding and Alternative Substrates - I

Wednesday AM Room: Auditorium
June 25, 2003 Location: Olpin Union Building

Session Chairs: Thomas Kuech, University of Wisconsin, Dept. of Chem. Engrg., Madison, WI 53706 USA; Peter Moran, Michigan Technological University, Dept. of Chem. Engrg., Houghton, MI 49931 USA

10:00 AM Student

F1, Heterogeneous Integration of (In,Ga)N Light-Emitting Diodes, CdSxSe1-x Filters and Silicon Photodetectors for Fluorescence-Detecting Microanalytical Systems: *ZhongSheng Luo*[1]; J. Alex Chediak[1]; Jeonggi Seo[2]; Nathan Cheung[3]; Luke Lee[4]; Timothy D. Sands[5]; [1]University of California, Berkeley, Matls. Sci. & Engrg., Cory 144MA, Berkeley, CA 94720 USA; [2]University of California, Berkeley, Applied Sci. & Tech. Grad. Grp., Berkeley, CA 94720 USA; [3]University of California, Berkeley, Dept. of Electl. Engrg., Berkeley, CA 94720 USA; [4]University of California, Berkeley, Dept. of Bioengrg., Berkeley, CA 94720 USA; [5]Purdue University, Sch. of Matls. Engrg., Sch. of Electl. & Compu. Engrg., & the Birck Nanotech. Ctr., W. Lafayette, IN 47906 USA

Fluorescence detection is widely used as an analytical technique due to its high sensitivity. This technique is usually implemented using laser-induced fluorescence (LIF), microfluidic chips and confocal microscopy. One drawback for this conventional scheme is that the size of the associated optics and detector is large relative to the size of the microfluidic chip. Therefore, the ability to integrate optical components, detector and microfluidic device into a microsystem is a major challenge in the development of microanalytical systems. To address above issue, a novel heterogeneous integration scheme is presented, where the photodetector, light sources, optical filters and microfluidic device are integrated into a single platform to perform the same function as a bench-top system. With this scheme, multicolor LEDs with matching thin-film filters can be integrated into the same chip, enabling excitation and detection of more than one type of dye from the same sample, which would be particularly important for applications in which real-time control is required. This integration scheme is enabled by a novel "pixel-to-point" transfer technique based on the double-transfer laser lift-off method in which the LED pixels are transferred from their sapphire growth substrates to specific points on the photodetector substrates. The pixel-to-point process involves three steps: (1) temporarily bonding the LED pixel to a specially designed pick-up rod, (2) removing the sapphire substrates using laser lift-off, and (3) registering and permanently bonding the LED pixel

to the designated area. A prototype system-on-a-chip with single wavelength capability has been demonstrated. The integrated microanlytical device replaces the conventional gas laser with a thin-film (In,Ga)N light-emitting diode (LED), and the grating, bulk glass and/or DBR filter with a CdS thin film deposited directly onto a photodetector by pulsed-laser deposition (PLD). The LED is transferred by laser lift-off to the silicon photodetector substrate, thereby combining all nondisposable components on a single substrate. The final integration step is achieved by temporarily positioning a disposable polydimethylsiloxane (PDMS) microfludic to the excitation/detection subsystem. Preliminary testing of this prototype was conducted using an (In,Ga)N LED with peak emission at 463 nm and FluoSpheres® carboxylate-modified fluorescent microspheres (40nm in diameter) with a fluorescence peak centered at 515nm. A detection sensitivity of 6 x 10-8 M (equivalent fluorescein concentration) was achieved on a 2mm wide and 100mm deep PDMS channel. Due to its bandgap tunability, CdSxSe1-x thin-film filters with different cut-off wavelengths can be achieved by adjusting the composition of the PLD target. These thin-film filters may be deposited onto photodetectors using a sequential masking and deposition process. Progress toward an integrated multiwavelength fluorescence detection system will be highlighted. Funding support from NSF (DMI-0088145) is acknowledged.

10:20 AM

F2, Dielectrophoretic Manipulation of Analytes for Biological Assay Applications: *Conrad David James*[1]; Dawn Jonita Bennett[1]; Murat Okandan[1]; Paul C. Galambos[1]; Seethambal S. Mani[1]; [1]Sandia National Laboratories, MEMS Device Tech., MS 1080, 1515 Eubank Blvd. SE, Albuquerque, NM 87123 USA

Dielectrophoresis (DEP) has been proposed as a mechanism to manipulate biological analytes such as cells and DNA in microanalytical systems.[1,2] The tunability of the DEP force as a function of the intrinsic properties (size, conductivity, dielectric properties) of the analyte is a quality that makes DEP an attractive method for sorting, collection, and filtration processes in microchip devices. However, in most DEP devices, anodic bonding and other post-processing steps are required to assemble multiple substrates into functional devices, reducing both device fabrication throughput and reproducibility. We have fabricated and tested monolithic microfluidic devices capable of dielectrophoretic manipulation of analytes. The Sandia-developed fabrication process SwIFT(Surface micromachining with Integrated Fluidics Technology) is capable of producing complex monolithic fluidic structures using multiple sacrificial and structural layers of both conductive and insulating materials. These fully encapsulated devices require no post-process wafer bonding and contain integrated microelectrodes for introducing electric fields to manipulate cells, viruses, and DNA. The objective of this work is to develop a fluidic microsystem for biological detection applications that can selectively collect cells, viruses, and biological molecules from a raw sample and then separate relevant components for further analysis and identification. The work presented here is one component of such a system that is aimed at developing multiplexing capabilities for detecting multiple biological analytes within a single reaction vessel. With our current devices, we have demonstrated selective trapping of DNA, yeast cells, and latex particles. By manipulating fluid conductivity and the frequency of the AC voltage applied to the microelectrodes, analytes were collected and concentrated within fluidic compartments. Spatial separation of different subpopulations of analytes within a mixture was also achieved. To improve device functionality, we have used computational modeling to predict device function and to optimize the trapping efficiency of the DEP force for a given electrode configuration. Current devices contain microelectrodes on the floor and ceiling of the fluidic channels to extend the DEP force throughout the vertical height of the channels, thus improving trapping efficiency. We foresee possibilities for using these devices in sample preparation applications for biological diagnostic testing. [1]Hughes, MP; "Strategies for dielectrophoretic separation in laboratory-on-a-chip systems," Electrophoresis 2002, Vol. 23, 2569-2582. [2]Chou et al.; "Electrodeless dielectrophoresis of single- and double-stranded DNA," Biophysical Journal 2002, Vol. 83, 2170-2179. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

10:40 AM

F3, Characteristics of Si Thin Films Transferred onto Glass by Ion-Cut Employing Pulsed and Direct-Current (DC) Plasma Immersion Ion Implantation: *F. Lu*[2]; D. Qiao[2]; M Cai[2]; P. K.L. Yu[2]; S. S. Lau[2]; R. K.Y. Fu[1]; C. P. Li[1]; L. S. Hung[1]; Paul K. Chu[1]; [1]City University of Hong Kong, Dept. of Physics & Matls. Sci., Tat Chee Ave., Kowloon Hong Kong; [2]University of California at San Diego, ECE Dept., La Jolla, CA 92093 USA

Ion-cutting using plasma immersion ion implantation, PIII, was investigated for the integration of single crystalline Si layers on glass. In PIII, the sample is immersed in a plasma consisting of the ions of interest. A DC (direct current) or AC (alternating current) voltage is applied to the sample to extract ions from the plasma and implant into the sample. PIII is inherently more efficient for high dose implantation as the implantation time is independent of the wafer size and the instrumental footprint is smaller than that of a conventional beam-line ion implanter. In the work reported here, it was found that p-Si wafers implanted nominally at room temperature with H doses on the order of a few times 1E16 cm-2 could be readily bonded to glass substrates with proper surface treatment similar to that used in conventional implantation for ion-cutting. The wafer surface of the as-implanted Si was converted from p-type to n-type. Upon bonding at room temperature, annealing (300°C), and exfoliation (450°C), the transferred Si layer on glass and the as-exfoliated surface of the implanted Si wafer remained n-type. Transmission electron microscopic examination showed a highly defective region near the top of the Si layer transferred onto glass due to H implantation. However, the crystalline quality was nearly defect-free in the deeper region of the layer, in spite of the incorporation of other impurities in the region. Annealing at sequentially higher temperatures led to the recovery of p-type conductivity at ~600-650°C. The thickness of the transferred layers suggested that the implanted species were mostly H3+ (trimer) ions from the PIII machine used in this study. Although secondary ion mass spectrometry (SIMS) results showed co-implanted atmospheric impurities such as oxygen, nitrogen and carbon that affected the electrical properties of the transferred Si layers, sufficient electrical activities were obtained in the Si layers integrated on glass. Our experimental results show that the direct current (DC) PIII mode appears to be more suitable for the ion-cutting process. This thin film transfer process was demonstrated on the fabrication of substrates for organic light emitting diodes (OLED). Our data indicate that the PIII method is a convenient and viable method for layer integration, and the results will improve if the background pressure in the chamber is improved.

11:00 AM

F4, Fabrication of Hybrid Distributed Bragg Reflectors using Metallic Wafer Bonding: *Hung-Cheng Lin*[1]; Zhenhua Zhang[1]; Chaofeng Xu[1]; Kuang-Chien Hsieh[1]; Keh-Yung Cheng[1]; [1]University of Illinois at Urbana-Champlaign, Dept. of Electl. & Compu. Engrg., 150 Micro & Nanotech. Lab., 208 N. Wright St., Urbana, IL 61801 USA

Hybrid distributed Bragg Reflectors (DBRs) consisted of a substrate-independent DBR stack and a Cr/Au/Ni/AuGe metal layer were fabricated and characterized for optoelectronic applications such as surface-emitting lasers and light-emitting diodes. The metal layer serves as a high-reflectance mirror as well as an adhesion material for wafer bonding. The compositional thickness of the Cr/Au/Ni/AuGe layer was varied for an optimum optical reflectance and bonding capability. Consequently, the hybrid DBR utilizing the reflective metal layer can achieve a reflectivity of higher than 99.5% in fewer periods than that required in a conventional DBR. In addition, it can be fused with various materials including semiconductors and dielectrics at a low bonding temperature of 320°C for heterogeneous integration. When bonded with n-GaAs and n-InP substrates, the metallic bonding interface becomes ohmic after the wafer bonding process. The substrate-independent DBR employed in this work is Si/Al-oxide deposited by e-beam evaporation with in-situ reflection monitoring. Other interesting material combinations such as the amorphous (Ga,As)/(Al,As) grown by very-low-temperature molecular beam epitaxy can also be used and is currently under investigation. Due to the amorphous nature of these materials, these DBRs can be fabricated on any substrates without the limitation of lattice-matching. To fabricate the hybrid DBR, we firstly deposited Si/Al-oxide stacks on a wafer. The reflectivity of the as-deposited DBRs were measured using a spectrophotometer. Then, the Cr/Au/Ni/AuGe metals were evaporated on the DBR surface and the metal/DBR structures were bonded with a new host substrate. Atomic force microscopy shows that the metallic bonding allows a

process latitude larger than 10 nm on the surface roughness. The original substrate was removed by selective etching, which stopped at the DBR. The reflectance of the exposed hybrid DBRs were measured and compared with the as-deposited results and the theoretical values. The theoretical values were calculated using the transfer matrix method with assumptions of ideal layer thickness and lossless materials. We found that the reflectivity of the hybrid DBRs exceed the as-deposited values toward the theoretical limits. The overall reflectivity of the DBR stop band as well as the side lobes was improved while the band position remained stable. Thus, the Cr/Au/Ni/AuGe metal layer can reduce the reflectivity loss due to process imperfections and therefore enhance the DBR performance. Furthermore, the hybrid DBR is thermally stable when annealed to 400°C in 2 min. Under a scanning electron microscope, the bonded DBR and the bonding interface demonstrate a robust and uniform integrity suitable for device fabrications. The hybrid DBR have been successfully applied to the fabrication of long-wavelength GaInAsP/InP VCSELs on Si substrates. It would also be useful to other optoelectronic device applications.

11:20 AM F5, Late News

Joint DRC/EMC Session VII.A: Carbon-Based and Molecular Electronic Devices

Wednesday PM Room: Saltair
June 25, 2003 Location: Olpin Union Building

Session Chair: Ray Tsui, Motorola Laboratories, Physl. Scis. Rsch. Labs., Tempe, AZ 85284 USA

1:30 PM

VII.A-1, Selective Growth and Electrical Properties of Single-Walled Carbon Nanotubes: *R. Zhang*[1]; I. Amlani[1]; R. Tsui[1]; J. Treske[1]; J. Baker[1]; [1]Motorola Laboratories, Physl. Scis. Rsch. Labs., 7700 S. River Pkwy., Tempe, AZ 85284 USA

We have studied selective area chemical vapor deposition (CVD) of single-walled carbon nanotubes (SWNTs) on substrates patterned with catalyst films consisting of an ultra-thin transition metal layer supported by a thin Al under-layer. Oxidized Si wafers were used as substrates. The transition metal layer consists of Ni, FeCo or NiFe. A hot-wall CVD reactor operating at sub-atmospheric pressures was used, and the growth conditions were optimized to achieve selective bridging of SWNTs across adjacent catalyst patterns. Two approaches were utilized to fabricate SWNT circuits: i) using SWNTs grown on substrates with catalyst layers patterned on top of pre-fabricated Ti/Au electrodes, ii) contacting the SWNTs with electrodes after CVD on substrates patterned only with catalyst layers. We have also characterized the electrical properties of the SWNT circuits made from both approaches. In the case of electrodes having catalyst patterns on top, the circuit resistance is typically very high, suggesting a large contact resistance at the SWNT/electrode interface. This is most likely caused by resistive catalyst material being present at the interfaces, due to the manner in which the bi-layer film works to catalyze the growth of SWNTs. Upon heating up during the CVD process, the Al layer melts and oxidizes to create Al2O3 clusters. Nanoparticles of the transition metal then form on the clusters to serve as active catalytic sites. These Al2O3 clusters are extremely resistive in nature and degrade the quality of the SWNT/electrode interface. This problem can be alleviated by moving the catalyst patterns away from the electrode edges, resulting in a direct contact between the as-grown SWNT and the Au surface of the electrodes. In the other approach where the electrodes are fabricated on top of the SWNTs after selective growth, the circuit resistance is usually low, in the range of a few hundred kW to a few MW, and can be further reduced by annealing. We have also studied the electronic transport properties of the SWNT bridges by applying a gate voltage to the Si substrate. The results indicate that as much as about 90% of the SWNTs show semiconducting behavior. These SWNT structures have allowed us to fabricate field-effect transistors with high gain and single-electron transistors showing Coulomb blockade at room temperature.

1:50 PM

VII.A-2, Negative Differential Resistance in a Bilayer Molecular Junction: *J. Le*[1]; Y. He[2]; C. Mead[1]; T. R. Hoye[2]; R. A. Kiehl[1]; [1]University of Minnesota, Dept. of Electl. Engrg., Minneapolis, MN 55455 USA; [2]University of Minnesota, Dept. of Chmst., Minneapolis, MN 55455 USA

We report, for the first time, negative differential resistance in a bilayer molecular junction. The molecular junctions were formed by contacting an amino nitro benzenethiol self-assembled monolayer (SAM) supported on a gold film with a second SAM comprised of alkanethiol molecules supported on the surface of a mercury drop. Current-voltage (I-V) characteristics of the Hg-alkanethiol-benzenethiol-Au molecular junctions show reproducible negative differential resistance (NDR) at room-temperature. The Au supported SAM was comprised of 4-[[2-amino-5-nitro-4(phenylethynyl)phenyl]ethynyl] benzenethiol molecules, which were synthesized by us according to procedures described elsewhere.[1] The Hg supported SAM was formed from $CH_3(CH_2)_9SH$ molecules. The gold substrates were prepared by thermal evaporation of 25 nm thick Au layer with 15 nm Cr adhesion layer (0.2 Å/s) onto 1 cm x 1cm single-crystal silicon pieces under a vacuum of ~10_{-6} Torr. The bilayer was formed by bringing into contact the SAM-coated drop of Hg with the surface of the SAM on Au in distilled isooctane by motorized micromanipulator using a technique described elsewhere.[2] The Au film and the Hg drop are used as electrodes and the current-voltage (I-V) characteristics were recorded using a HP4145B Semiconductor Parameter Analyzer. The amino nitro benzenethiol molecule used in the junction is one of a variety of related molecules that have been found to exhibit NDR has been reported for temperatures below about 150K.[3] The alkanethiol molecule used in this study is known for its ability to form a high quality SAM and has well established electrical characteristics. The I-V characteristic of a bilayer in which both SAM's are formed by an alkanethiol molecule represents a control structure for our experiments (no benzenethiol). The characteristic is linear and symmetric at relatively low bias voltage (<0.1 V) and increases exponentially at high bias voltage, which agrees with previous studies[2] and is consistent with tunneling across and insulating molecule.[2] Typical current-voltage characteristics for the Hg-alkanethiol-benzenethiol-Au bilayer junction shows NDR with a peak at ~0.7V and a peak to valley ratio of about 1.3 at room temperature. Sweeping from -1.5 to 1.5 V gives a highly asymmetric characteristic with no NDR in the negative bias regime. Repeated I-V sweeps were found to produce a reduction of the current density, which was partially recovered after a few seconds. Similar results were obtained for many different junctions formed on the same bilayer SAM. In conclusion, negative differential resistance is reported for the first time for a bilayer molecular junction, which was formed from molecules that separately exhibit NDR and electron tunneling characteristics. The results suggest that the NDR mechanism in the first molecule can be accessed by tunnel injection through the second molecule. These results and other experiment with such two-layer molecular systems will be useful for improving understanding and optimizing design of molecular electronic devices. [1]Allara, D.L.; Dunbar, T.D.; Weiss, P.S.; Bumm, L.A.; Cygan, M.T.; Tour, J.M.; Reinerth, W.A.; Yao, Y.; Kozaki, M.; Jones, L., II Ann. N.Y. Acad. Sci. 1998, 852, 349. [2]Holmlin, R.E.; Haag, R.; Chabinye, M.L.; Ismagilov, R.F.; Cohen, A.E.; Terfort, A.; Rampi, M.A.; Whitesides, G.M. J. Am. Chem. Soc. 2001, 281, 127. [3]Chen, J.; Reed, M.A. Chemical Physics 2002, 281, 127.

2:10 PM

VII.A-3, Fabrication and I-V Characterization of Carbon Nanotube Single Electron Transistor Operated at Room Temperature: *T. Kamimura*[1]; K. Sakamoto[2]; M. Maeda[2]; K. Kurachi[2]; K. Matsumoto[3]; [1]University of Tsukuba and CREST/JST Japan; [2]Meiji University Japan; [3]National Institute of Advanced Industrial Science and Technology, University of Tsukuba and CREST/JST, 1-1-1 Umezono, Tsukuba, Ibaraki 305-8568 Japan

Abstract not available.

2:30 PM

VII.A-4, Random Networks of Single-Wall Carbon Nanotubes: Electronic and Sensor Applications: *E. S. Snow*[1]; J. P. Novak[1]; P. Campbell[1]; D. Park[1]; [1]Naval Research Laboratory, Elect. Sci. & Tech. Div., Code 6876, Washington, DC 20375 USA

We describe a new electronic material that is composed of random networks of single-wall carbon nanotubes (SWCNTs). The electronic properties of the networks can vary from semiconducting to metallic depending on the network density, and the electron mobility of the

semiconducting networks is more than an order of magnitude larger than the mobility of materials used for commercial thin-film transistors. The networks are chemically robust and transparent. They can be deposited on arbitrary substrates and are easily patterned into devices. These properties make random networks of SWCNTs interesting candidates for a variety of applications including electronics on noncrystalline and compliant substrates and chemical and biological sensors. Because of their unique structural, mechanical and electrical properties, single-wall carbon nanotubes (SWCNTs) offer promise for electronic and sensor applications. However, the controlled assembly of SWCNT devices stands in the way of high-yield device fabrication that is a requirement for commercial applications. One problem is the lack of position and orientation control. The second problem is the lack of control of the precise atomic structure of SWCNTs that results in a wide variety of electronic properties ranging from semiconducting to metallic behavior. Researchers have made little progress in solving either of these two problems, and they remain the most prohibitive barriers for commercial electronic applications. We present an alternative approach to realizing SWCNT electronic applications that circumvents the two problems detailed above. Our solution is to use random networks of SWCNTs.[1] We show that random networks of SWCNTs form an electrically-conducting thin film. Such a network is electrically conducting because of the high quality electrical contact formed between intersecting nanotubes. Devices fabricated from such networks circumvent the requirement of position and structural control because the device properties are determined by the averaged properties of the individual SWCNTs. We find that high-density networks are metallic, whereas low-density networks near the percolation threshold for electrical conduction exhibit semiconducting behavior. It is this ability to form semiconducting networks of SWCNTs that holds potential for a wide range of electronic and sensor applications. [1]E.S. Snow, J.P. Novak, P.M. Campbell, and D. Park, Appl. Phys. Lett. (in press).

3:10 PM Break

Joint DRC/EMC Invited Session VIII: Plastic Electronics

Wednesday PM Room: Saltair
June 25, 2003 Location: Olpin Union Building

Session Chair: Lynn Loo, University of Texas at Austin, Austin, TX 78712 USA

3:30 PM Invited

VIII.-1, Large Area Printing of Organic Transistors: *G. B. Blanchet*[1]; [1]Dupont, Central Rsch., Experimental Sta. E356/284, Wilmington, DE 19880 USA

Organic electronic systems offer the advantage of lightweight, mechanical flexibility and large area coverage at potentially lower manufacturing cost. Although the production of functioning plastic transistors using approaches such as ink jet, screen printing and stamping, has been described in the literature, no one-transistor layer has yet been fabricated using a technique appropriate for their commercialization. Although solution processability of many organics may ultimately allow for the printing of electronic devices in a printing press, designing chemically compatible solutions to be printed sequentially represents a significant technical barrier. Thermal transfer, a non-lithographic technique enables printing multi-layer electronics devices via a dry (i.e. solvent-less) additive process. This high-speed method is capable of patterning a range of organic materials over large areas (~ 1 m^2 with micron dimensions and excellent electrical performance. The imaging process and film structure are illustrated in Figure 1. Thermal transfer involves the pixelized transfer of a thin solid layer, encompassing a digital image, from a donor film onto a flexible receiver. The sequential transfer of images from different solid layers builds multilayer devices. A 40 Walt 780 nm infrared diode laser, split into 250 2.7 µm x 5 µm individually addressable spots, is focused through the donor base at a light absorbing layer. The efficient conversion of light to heat at this interface decomposes surrounding organics into gaseous products. Their expansion thus propels the thin conducting layer on top onto the receiver film. The desired conducting pattern is printed by selectively transferring the individual 5-µm x 2.7-µm pixels comprising the image from the donor layer onto the receiver. The electrical properties d printed organic conductors, p and n-channel transistors and inverter circuits will be described. Pentacene and copper hexa-decafluoro-phthalocyanine serve as the p and n-type organic semiconductors while a doped polyaniline/single wall carbon nanotubes composite operates as a high-resolution printable conductor. The good electrical performance of these devices derives directly from the low resistance, ohmic contacts between the printed source/drain electrodes and the organic semiconductors. The behavior of these contacts is quantified and some morphological evidence for their low resistance presented. The excellent characteristics of the circuits and the operational flexibility of the printing technique is further illustrated by printing a 28" diagonal source/drain and gate layers of an electrophoretic display backplane onto a flexible substrate. This novel printing technology applied to the fabrication of large area integrated electronic devices may represent the means 20 build realistic flexible electronic devices providing a practical route to realizing the benefits of plastic materials for electronics.

4:10 PM Invited

VIII.-2, Stretchable and Deformable Macroelectronics: *S. Wagner*[1]; S. P. Lacour[1]; P.-H. I. Hsu[1]; J. C. Sturm[1]; Z. Suo[2]; [1]Princeton University, Dept. of Electl. Engrg., Princeton, NJ 08544 USA; [2]Princeton University, Depts. of Mechl. & Aeros. Engrg. & POEM, Princeton, NJ 08544 USA

Many concepts for service automation depend on stretchable and deformable electronics. Automated services require intelligent machines that must be cautious, and therefore need to sense over their entire surface. The machine might be a robot teaming with an astronaut, or a vacuum cleaner doing its job after the homeowners have left for work. A number of specialized products also will depend on stretchable and deformable electronics: sensor skin for prostheses, hemispherical photosensor arrays for collision avoidance cameras, or see-through displays for eyeglasses. Some applications, like the camera target, will be deformed to a 3-D shape only once, while others, like the sensor skin covering a robot's elbow, will be stretched and relaxed many times. Our tools for making integrated circuits are designed to fabricate, evaluate, and package planar geometries. Because we cannot afford to build a separate tool kit for making curved circuits we are lucky to have this planar technology base, but it forces us to observe certain fabrication sequences. Stretchable and deformable circuits will be made flat, and will be deformed at the last possible manufacturing step. Permanent and elastic deformation will enter this technology as back-end fabrication steps. The sensor glove illustrates an electronic skin [l] and its main components: the thin-film transistor backplane, the chemical sensor functional frontplane, and the computation and communication network, To date most work has gone into the backplane, some into exploring new Functions, and little into circuit and network architectures. Two architectural models exist for stretchable and deformable macroelectronic systems. One model is the AMLCD, in which a matrix of functional cells is switched locally and is driven by peripheral ICs. The other model is the PC, in which peripherals are driven by a central processor. Architecture and network design will be start out from the AMLCD model to accommodate low transistor counts and low bandwidth. Over time architecture and networks will become hybrids of the AMLCD and PC models, with first simple circuits and then computation progressively placed into cells, and into local networks of cells. Designs increasingly will take on their own distinct characteristics as transistor count and network bandwidth are raised, and as products become defined, Next to well-defined applications, what architecture and network design need most at present are reliable forecasts of the development of cell functionality, particularly the transistor count per cell. Materials, devices, on-cell circuits and cell functionality dominate present-day research on stretchable and deformable macroelectronics. Cell functions under consideration today include light filter, reflector, emitter and sensor (X-rays), touch sensor, actuator, temperature sensor and microheater. Making circuits flexible or bendable, w s relatively easy when simple geometric criteria are followed. Stretching and 3-D deformation pose qualitatively different design and fabrication challenges. In fabrication and in most prospective applications such circuits undergo tensile strain, i.e. the circuits are expanded. The thin film transistor structures of the backplane, and most of the functional frontplane materials, break at tensile strains of the order of one percent. However, many applications require one-time or reversible elongation

of up to ten percent. Our approach has been to subdivide the integrated circuit into mechanically separate islands, which are fabricated on a deformable substrate that takes up most of the total strain. [3] By experiment and modeling, these islands can be made sufficiently stiff to withstand the tensile stress transmitted from the substrate. In this way the burden of stretching and deformation is transferred to the substrate, which may undergo one-the plastic or repeated elastic deformation. The island geometry relies on interconnects designed to accommodate this deformation. For circuits shaped only once, plastic deformation of metal, or of sacrificial masks far metal patterning, may be used. [3] Research on elastic, reversibly stretchable, interconnect metallization for elastic circuits has only begun.[4] [1] V. Lumelsky, M.S. Shur and S.Wagner, eds., Sensitive Skin, Selected Topics in Electronics and Systems - VoI.18, World Scientific, New Jersey 2000, p.133. [2] Y. Chen, K. Denis, P. Kazlas, P. Drzaic, 2001 SID Digest of Technical Papers 32, 157-159 (2001). [3] P. I. Hsu, R. Bhattacharya, H, Gleskova, M. Huang, Z. Xi, Z. Suo, S. Wagner, and J.C. Sturm, Applied Physics Lett. 87, 1723-1725 (2002). [4] Stephanie Perichon Lacour, Sigurd Wagner, Zhenuy Huang, Z. Suo, Applied Physics Lett., 7 April 2003, in press.

4:50 PM Invited

VIII.-3, Nanoscale Transport in Organic Transistors and LEDs: *J. Zaumseil*[1]; T.-W. Lee[1]; J. W.P. Hsu[1]; Y.-L. Loo[2]; R. Cirelli[3]; J. A. Rogers[4]; [1]Bell Laboratories, 600 Mountain Ave., Murray Hill, NJ 07974 USA; [2]University of Texas at Austin, 1 University Sta., Austin, TX 78712 USA; [3]New Jersey Nanotechnology Center, 600 Mountain Ave., Murray Hill, NJ 07974 USA; [4]University of Illinois at Urbana-Champaign, 1304 W. Green St., Urbana, IL 61802 USA

Unconventional tools for nanofabncation provide new opportunities for building and studying the behavior of organic optoelectronic systems. This talk begins by describing two such methods - soft contact lamination (SCL) and nanotransfer printing (nTP) - and some of their unusual capabilities. It then focuses on their use for building organic test structures and devices to probe transport on three important length scales: those that are comparable to (i) the typical grain size (-300 nm) in thin film organic semiconductors, (ii) the thickness (-100 nm) of thin layers of electroluminescent (EL) polymers and (iii) the size (-1 nm) of the molecules themselves. In the first case, we study the behavior of transistors with printed channel lengths that range from several microns to -700 nm. In the second, we examine the current-voltage characteristics and quantum efficiencies of polymer light emitting diodes (PLEDs) that use laminated electrodes. For the third, we construct organic transistors whose laminated contacts are chemically modified with organic self-assembled monolayers of linear aliphatic molecules with lengths of 1-2 nm. In all cases, detailed knowledge concerning the contact resistance between the metal (Au) electrodes and t h ~ organic is paramount.[1] We describe systematic measurements of the resistance of contacts formed in various ways, and use the information to interpret the behavior of the systems described above. The results provide some guidelines for the design of organic transistors and PLP,Ds for applications in displays and other areas. [1]J. Zaumseii, R. Baldwin and S.A. Rogers, submitted to J. Awl. Phys.

Session G: Nitrides: Advanced Characterization

Wednesday PM Room: Ballroom Center
June 25, 2003 Location: Olpin Union Building

Session Chairs: Christian Wetzel, Uniroyal Optoelectronics, Tampa, FL 33619 USA; James Speck, University of California-Santa Barbara, Dept. of Matls., Santa Barbara, CA 93106 USA

1:30 PM

G1, Dopant-Defect Interactions in GaN and Related Alloys: *P. N. Grillot*[1]; L. W. Cook[1]; J. Yu[1]; A. Y. Kim[1]; W. Goetz[1]; R. D. Pai[1]; J. C. Caylor[1]; J. W. Huang[1]; S. A. Stockman[1]; [1]LumiLeds Lighting, US LLC, 370 W. Trimble Rd., San Jose, CA 95131 USA

The performance of GaN electronic and optoelectronic devices can be substantially affected by unintentional impurity incorporation through processes such as increased recombination-generation currents, parasitic radiative or non-radiative recombination, and ionized impurity scattering. Carbon and oxygen are two such impurities that are particularly troublesome to the performance of GaN based devices, partly due to the common presence of carbon and oxygen in the CVD growth environment through the use of organometallic sources, and partly through virtual or actual leaks in the reactor. In fact, both carbon and oxygen have been previously correlated to defect related blue luminescence in GaN, with carbon apparently giving rise to defect related blue luminescence near 415-420 nm (~2.95 eV), and oxygen apparently giving rise to defect related blue luminescence near 440 nm (~2.8 eV). In this talk, we will discuss interactions between the incorporation of these unintentional carbon and oxygen impurity species and intentional shallow donor and acceptor dopant species, such as Si and Mg, in the GaN material system. We will also discuss the effect of growth conditions, such as growth pressure, alloy composition, and majority carrier dopant concentration, on impurity incorporation in GaN and AlGaN. Examples of dopant-defect interactions that will be discussed in this talk include enhanced oxygen and carbon incorporation in GaN and AlGaN that are heavily doped with Mg, and the effect of Si doping vs. Mg doping on carbon incorporation and defect related luminescence in GaN. More specifically, it has recently been suggested that the presence of Si causes carbon to incorporate on the nitrogen site in GaN, and suppresses carbon-related defect luminescence, while the presence of Mg may cause carbon to incorporate on the gallium site in GaN, giving rise to carbon-related defect luminescence near 415-420 nm. These interactions will be discussed in terms of the Fermi-level effect, which describes the effect of the Fermi energy on the defect formation energy (and hence the defect concentration).

1:50 PM Student

G2, Investigation of Deep Level Luminescence at 2.45 eV in InGaN:Mg: *Bing Han*[1]; Melville P. Ulmer[2]; Bruce W. Wessels[1]; [1]Northwestern University, Dept. of Matls. Sci. & Engrg. & Matls. Rsch. Ctr., Evanston, IL 60208 USA; [2]Northwestern University, Dept. of Physics & Astron., Evanston, IL 60208 USA

P-type doping of InGaN has met with limited success, which has been attributed to a number of factors including strong self-compensation by deep native donor defects (V_N). In this study deep level defects formed upon doping InGaN epilayers with Mg acceptors have been investigated by photoluminescence (PL) spectroscopy. $In_{0.07}Ga_{0.93}N$ epilayers were prepared by metalorganic vapor phase epitaxy (MOVPE) at 780°C. Undoped films exhibited band-edge emission at 3.06 eV. Upon Mg doping the band-edge luminescence quenches; a 2.45 eV broad green luminescence band with the FWHM of 800 meV dominates the room temperature PL spectrum. This luminescence band has been previously observed but its origin is not understood. Preliminary evidence including excitation intensity dependence suggests that it may involve donor-acceptor pair (DAP) recombination. The green band exhibits an "S-shaped" emission energy shift, a decrease of the FWHM, and an enhancement of PL intensity with increasing measurement temperature. These complex temperature dependences are attributed to large compositional fluctuations in the compensated films, which were also observed in the optical absorption spectroscopy. InGaN:Mg epilayers with a GaN capping layer were subsequently annealed at 1030°C in a H_2 atmosphere. No phase separation was observed. Upon annealing the emission intensity increases suggesting the quenching of competitive non-radiative recombination process, also indicating that the defects responsible for the emission are thermally stable. The above complex temperature dependences were not observed in the annealed films, indicating a reduction of alloy compositional fluctuations. As a consequence of annealing a fine structure related to phonon replicas was observed for the 2.45 eV band, with an energy separation of 105 meV. By analysis of the band shape, the Huang-Rhys factor was determined to be six, indicating strong electron-phonon coupling responsible for the large width of the green band.

2:10 PM

G3, Microcatholuminescence Spectroscopy of Localized Electronic States at Photoelectrochemically-Etched GaN Whiskers: *Xiaoling Sun*[1]; Leonard J. Brillson[1]; Tim Hossian[2]; Ilesanmi Adesida[2]; [1]The Ohio State University, Electl. Engrg., 205 Dreese Lab., 2015 Neil Ave., Columbus,

OH 43210 USA; [2]University of Illinois, Dept. of Electl. & Compu. Engrg. & Microelect. Lab., Urbana, IL 61801 USA

Photoelectrochemical wet etching of hydride vapor phase epitaxy (HVPE)-grown GaN produces highly anisotropic GaN whiskers due to the high recombination of photogenerated free carriers near edge and mixed dislocations and the resultant selective etching.[1,2] The etched whiskers are typically 10-50 nm in diameter and up to 1 μm in height. We have used low temperature (10K) cathodoluminescence spectroscopy (CLS) in a UHV scanning electron microscope (SEM) to probe the electronic features of GaN whiskers by focusing on individual whiskers in plan view and comparing the spectra to those of the underlying GaN. We were able to maintain the electron beam on individual whiskers and obtain reproducible results on different whiskers. We also performed depth dependent CL vs. electron beam energies between 2 and 25 keV in a larger area with high whisker density. At 5 keV, the 30 nm spot spectra show large differences between the whiskers and the underlying subsurface regions. Similar differences are apparent for near-surface (3 keV) excitation of the GaN and whiskers versus the GaN bulk. CL spectra reveal several emissions that can be identified with: the donor bound exciton (D^0X) at 3.47 eV, excitons bound to stacking faults (SX) at 3.40 eV and 3.31 eV and donor acceptor pairs (DAP) at 3.27 eV along with its LO, 2LO phonon replicas. The D^0X linewidth (FWHM =19.9 meV) is considerably larger than that of the underlying GaN (FWHM =15.5 meV), indicating lower crystal quality of the whiskers, in principle due to the dislocations at the whisker cores. We observe a shoulder feature at 3.44 eV previously assigned to O donor levels.[3,4] This feature is better resolved in the whiskers, indicating a higher concentration of O than in the bulk GaN. Furthermore, the DAP is also stronger in whiskers, consistent with the presence of a higher donor concentration. Interestingly, the SX emissions within the whiskers are weaker than those of the underlying GaN, indicating either stronger nonradiative recombination via the dislocation and/or a selective etching effect, i.e., preferential etching of stacking faults versus dislocations. These results illustrate that photoelectrochemical etching alters the electronic states within GaN whiskers, in part due to the introduction of accumulation of additional O impurities. [1]C. Youtsey, L. T. Romano, and I. Adesida, Appl. Phys. Lett. 73, 797 (1998). [2]C. Youtsey, L. T. Romano, R. J. Molnar, I. Adesida, Appl. Phys. Lett. 74, 3537 (1999). [3]S.H. Goss, X.L. Sun, L. J. Brillson, D. C. Look, and R. J. Molnar, Appl. Phys. Lett. 78, 3630 (2001). [4]X. L. Sun, S. H. Goss, L. J. Brillson, D. C. Look, and R. J. Molnar, J. Appl. Phys, 91, 6729 (2002).

2:30 PM

G4, Microstructural and Optical Properties of Heteroepitaxial GaN Grown on AlN Buffers on SiC: *B. J. Skromme*[1]; H. X. Liu[1]; M. K. Mikhov[1]; G. N. Ali[1]; K. C. Palle[1]; D. J. Smith[2]; Z. J. Reitmeyer[3]; R. F. Davis[3]; [1]Arizona State University, Dept. of Electl. Engrg., Box 875706, Tempe, AZ 85287-5706 USA; [2]Arizona State University, Ctr. for Solid State Sci., Box 871704, Tempe, AZ 85287-1704 USA; [3]North Carolina State University, Dept. of Matls. Sci. & Engrg., Raleigh, NC 27695-7907 USA

Growth of GaN on SiC offers the advantages of reduced lattice mismatch, better substrate thermal conductivity, and electrical contact through the substrate in comparison with the more common growth on sapphire. Yet the microstructural properties of GaN/SiC have not been characterized as thoroughly. In this work, we describe characterization of GaN layers grown by low pressure (20 Torr) metalorganic chemical vapor deposition on high temperature AlN buffer layers on SiC substrates using secondary electron imaging (SEI), cathodoluminescence (CL), atomic force microscopy (AFM), transmission electron microscopy (TEM), room and low temperature photoluminescence (PL), and optical reflectance. In particular, we study the effects of high temperature (1600°C) H_2 etching of the SiC substrates prior to growth, the effects of Si doping of the GaN, and the behavior as a function of GaN layer thickness. The GaN layers were grown at a temperature of 1015°C and a N/Ga ratio of 1300, and the 0.1 μm thick AlN layers at 1115°C and a N/Al ratio of 24,000. In all GaN layers grown on as-polished commercial SiC wafers (no H_2 etching), we observe columnar subgrain boundaries by AFM, SEI, and optical microscopy, which appear nonradiative (dark) in panchromatic CL images. Mottled CL contrast is observed within individual grains, presumably due to threading dislocations. Average grain size increases from about 3 to 10 μm as the GaN layer thickness increases from 0.5 to 2.6 μm. Simultaneously, we observe gradual relaxation of the biaxial compressive lattice mismatch stress, which varies from -2.1×10^{-3} in the 0.5 μm thick layer to -5.7×10^{-4} in the 2.6 μm thick layer, based on low temperature PL and reflectance of the excitonic features. On a H_2-etched substrate, however, no subgrain structure could be detected in a 1 μm thick layer, and a uniform mottled contrast is observed in CL. This sample also exhibits greater strain relaxation, similar to that of the 2.6 μm thick layer grown on the unetched substrate. The difference is attributed to a more two-dimensional growth mode on the smoother etched substrate, which is less likely to produce strain fields that stimulate the formation of grain boundaries. Cross-sectional TEM imaging shows a higher density of dislocations and strain contrast near the buffer layer in the unetched case, and a considerable decrease in the density of threading dislocations in the etched case. Plan-view TEM measurements are in progress. Doping of the GaN with 3×10^{18} cm^{-3} Si eliminates the subgrain boundaries for growth on both H_2-etched or unetched substrates, and produces a uniform, mottled CL contrast. PL spectra and intensities will be discussed as a function of thickness and H_2 etching.

2:50 PM Student

G5, Atomic Ordering in InGaN Alloys: *Manu Rao*[1]; Yong-Qian Wang[1]; Subhash Mahajan[1]; [1]Arizona State University, Chem. & Matls. Engrg., Tempe, AZ 85287-6006 USA

Atomic ordering has been mainly observed in InGaN layers grown by MBE but has also been reported in layers grown by MOCVD. The mechanisms responsible for the evolution of the ordered structures are not well understood. A surface enrichment of In above a certain level may make it energetically feasible to incorporate an In-rich layer. This would cause In depletion at the surface and therefore growth of a Ga-rich layer. This process could continue repeatedly and therefore, vertical phase separation may be responsible for ordering. However, an alternative mechanism may operate. Theoretical studies have shown that during growth of InGaN on GaN, In has a strong preference to occupy sites of reduced N coordination compared with Ga. A {10-11} GaN facet has alternate stacking of sites with high and low N coordination. Consequently, InGaN growth on this surface should result in alternating In and Ga rich {0001} planes being formed by facet migration across the substrate surface. A similar local atomic structure can be found on bi-layer steps present on the growing surface during MOCVD growth and therefore this may be the ordering mechanism in operation. Using an MOCVD system, thin GaN nucleation layers were deposited on (0001) sapphire substrates at low temperature followed by high temperature annealing. The annealing results in a change in the microstructure to one of larger islands bounded by {10-11} facets with a corresponding increase in the overall surface roughness. InGaN was then deposited over a range of temperatures and thicknesses to evaluate the influence of these factors on ordering. XRD θ-2θ scans as well as TEM-SAD of [10-10] cross sections were performed to detect evidence of atomic ordering. Preliminary results show evidence for atomic ordering. The (0001) spot is a systematic extinction in the [10-10] ZADP. However, this spot was found to be present in some of the thicker samples. This spot corresponds to (1:1) ordering, which is the type expected from the structure of the {10-11} facets. The extra spot only exists in thicker samples, suggesting that strain due to mismatch initially inhibits ordering, but plays less of a role as the samples relax during growth. Further systematic experimentation will clarify whether the facets are indeed responsible for the ordering observed. The support of this work by NSF is gratefully acknowledged.

3:10 PM Break

3:30 PM

G6, Electroreflectance Studies of Stark-Shifts and Polarization-Induced Electric Fields in InGaN Quantum Wells: *Robert J. Kaplar*[1]; Steven R. Kurtz[1]; Daniel D. Koleske[1]; Arthur J. Fischer[1]; [1]Sandia National Laboratories, PO Box 5800, MS 0601, Albuquerque, NM 87185 USA

Electroreflectance of InGaN quantum well LEDs revealed several quantum well transitions. Studying those transitions as a function of applied voltage enabled us to observe Stark-shifts, make peak assignments, and compare our results with bandstructure models which included polarization-induced electric fields and carrier screening. Because electroreflectance is insensitive to defects and inhomogeneities, comparison of electroreflectance with photoluminescence and electroluminescence provided insight into the role of In-segregation or localization in quantum well emission. Samples studied were grown by MOCVD and consisted of nominally undoped $In_xGa_{1-x}N$ ($x \cong 0.05$) quantum wells sandwiched between Si-doped GaN barriers. P-n junctions were formed

by growing Mg-doped GaN p^+-layers on top of the n-type layers. C-V profiling of the diodes yielded a series of peaks in the doping versus depth plot, allowing us to observe depletion of each single quantum well. Small-signal electroreflectance measurements were made at several DC bias values chosen such that only the topmost quantum well ranged from fully populated to depleted. Electroreflectance spectra consisted of ≥3 peaks indicating several transitions associated with a single quantum well. Lineshape fits of the lower energy peaks showed a Stark-shift towards the blue with quantum well depletion, consistent with the polarization-induced field in compressively strained InGaN grown on Ga-face GaN. Using parameters obtained from the C-V measurements to determine the Fermi energy versus bias, we employed a Schroedinger-Poisson solver to construct a realistic model of the quantum-confined energy levels in the InGaN quantum wells, including screening and polarization-field-induced band-bending. Energies of the lowest electron to heavy-hole transitions were in reasonably good agreement with the values obtained from the model, and further, both the direction and the magnitude of the calculated Stark-shifts for these transitions were consistent with the experimental data. Comparison of the highest energy experimental peak with our calculations suggests that this peak may be due to a transition involving higher energy electron or continuum states. An intermediate energy peak is tentatively assigned to the crystal-field hole state. Finally, photoluminescence and electroluminesence energies coincide with the lowest energy electron to heavy hole transitions observed in electroreflectance, and at 300K there was no evidence for a Stokes shift between absorption and emission processes. However, defect-related features were observed in low temperature electroluminescence. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin company, for the US Department of Energy under contract DE-AC04-94AL85000.

3:50 PM

G7, Spectral Ellipsometry Characterization of MBE Grown GaN on 4H SiC: *Todd M. Holden*[1]; Fred H. Pollak[1]; Rajinder Sandhu[2]; Benjamin Heying[2]; Ioulia Smorchkova[2]; Mike Wojtowicz[2]; [1]Brooklyn College and New York State Center for Advanced Technology in Ultrafast Materials and Applications, Physics Dept., 3438N, 2900 Bedford Ave., Brooklyn, NY 11210 USA; [2]Northrop Grumman Space Technology, One Space Park, Redondo Beach, CA 90278 USA

Spectral ellipsometry is a powerful tool to characterize $Ga_xAl_{1-x}N$ based heterostructure properties, such as material quality, interface quality, surface roughness, layer thicknesses, and dielectric functions. The dielectric function and sample structure of several molecular beam epitaxy (MBE) grown GaN films on 4H SiC substrates (c-axis perpendicular to the surface) were studied using spectral ellipsometry for the energy range 0.8-5.3 eV. SiC is a desirable substrate for $Ga_xAl_{1-x}N$ based devices because of its relatively small lattice mismatch (1-4%) and high thermal conductivity. Three samples, consisting of the SiC substrate, a 20 nm AlN nucleation layer, and 500 nm GaN, were grown under identical conditions except for the temperature and conditions for the AlN nucleation layer. For energies below the fundamental bandgap of GaN, complicated interference patterns were observed due to the (birefringent) SiC and GaN layers. The data was analyzed using a uniaxial anisotropic model to allow for the birefringence of the SiC substrate. The extracted dielectric function of GaN was fit using a model taking into account both discrete and continuum excitonic effects. Two of the three samples exhibited sharp discrete and continuum excitonic features at the fundamental bandgap similar to the best literature values for GaN grown on sapphire. In the third sample the discrete exciton was not resolved, similar to most published GaN on Sapphire and bulk GaN data. From our model, we also determined that the two samples exhibiting a discrete exciton feature had a small surface roughness (≤2nm), while the third sample had a larger surface roughness (~ 5nm). The abruptness of the GaN/AlN and AlN/SiC interfaces were determined to be smaller than the AlN nucleation layer thickness (20nm) in all cases.

4:10 PM

G8, Universal Theory for the Determination of Both Screw and Edge Dislocation Densities for GaN and Related Materials using High Resolution X-Ray Diffraction: *Simon Bates*[1]; [1]Bede Scientific Incorporated, 14 Inverness Dr. E., Ste. H-100, Englewood, CO 80112 USA

High resolution x-ray diffraction is a powerful tool for the measurement of dislocation density within bulk substrates and epi-layer materials. The broadening of the x-ray diffraction peak along specific directions can be directly related to specific types of dislocations once the instrumental function has been removed. However, until now there has not been a single theoretical approach for modeling all accessible reflections. A self consistent "mosaic block" model of both screw and edge threading dislocations will be presented. The model predicts peak broadening along the omega axis for the symmetric as well as the in-plane asymmetric Bragg reflections driven by screw dislocations and finite correlation length effects. The change in the measured omega peak width as a function of the 2Theta and Omega offset angle allows the direct extraction of the screw dislocation density. Edge dislocations give broadening along the omega axis for out of plane asymmetric Bragg reflections only. By analyzing the change in the omega peak width as a function of the Chi offset allows the extraction of the edge dislocation density. The full model will be presented along with its application to a series of GaN samples with known electrical properties.

4:30 PM Student

G9, Characterization of Multiple Carriers in GaN and InN Epilayers Using Variable Magnetic Field Hall Measurements: *Craig H Swartz*[1]; Randy P. Tomkins[1]; Thomas Hubbard Myers[1]; Hai Lu[2]; William J. Schaff[2]; Lester F. Eastman[2]; [1]West Virginia University, Dept. of Physics, PO Box 6315, 224 Hodges Hall, Morgantown, WV 26506-6315 USA; [2]Cornell University, Dept. of Electl. & Compu. Engrg., Ithaca, NY 14853 USA

Electrical characterization using Hall measurements is one of the cornerstone techniques for characterizing semiconductors. Mixed conduction effects in multi-layer samples can complicate interpretation in the Group III-nitride system as conduction at the substrate-epilayer interface and (at least for InN) at the free surface can dominate the transport. Standard measurements at a single magnetic field are of limited use when applied to systems with prominent mixed-conduction since they provide only averaged results. Multiple-carrier or multiple-layer analysis of single field Hall measurements also requires a priori assumptions about the system. Variable magnetic field Hall measurements can be used to determine, in principle, the influence of the various carriers. A combination of quantitative mobility spectrum analysis (QMSA) and multiple-carrier fitting (MCF) is a robust approach for identifying the number and carrier type as well as quantifying mobilities and concentrations for multiple species.[1,2,3] Much development has centered around HgCdTe with carrier mobilities comparable to n-type conduction in the Group III-nitride system. Resistivity and Hall measurements were made at West Virginia University as a function of temperature and magnetic field up to 4.5 T on GaN layers grown by metal-organic chemical vapor deposition and hydride vapor epitaxy, and on InN samples grown by molecular beam epitaxy. QMSA and MCF analyses were performed using standard techniques.[1,2] This approach allowed direct determination of interfacial conduction between the GaN and the sapphire substrate while also allowing measurement of the bulk electrical properties. The results on InN were more interesting. Analysis always indicated three types of electrons, a low mobility electron (~200 cm2/Vs) tentatively assigned to buffer layer conduction, an electron with a temperature-independent mobility at a sheet density of about 2-3 x1013 cm-3 believed to be a surface electron and a third electron whose mobility and concentration varies as expected for "bulk" electrons. Finally, variable magnetic field analysis of a 7.5 μm thick InN sample continued to give strong evidence for a low mobility interfacial and surface electrons. There is then a continuous spread at higher mobility with increasing mobilities and decreasing associated sheet concentration, which is interpreted as material improving (and background doping decreasing) with increasing sample thickness resulting in a true continuum mobility spectrum. Indeed, the measurements suggest maximum mobilities greater than 4000 cm2/Vs in "bulk" InN. The temperature characteristics of the maximum mobility follow a classic trend, with a peak around 150-175 K and lower maximums at both lower and higher temperatures. [1]J.R. Meyer, et al., Semicond, Sci. Technol. 8, 805 (1993). [2]I. Vurgaftman,et al., J. Appl. Phys. 84, 4966 (1998). [3]Y. Gui, et al., J. Appl. Phys. 84, 4327 (1998).

4:50 PM Student

G10, Characterization of Post-Epilayer Growth Anodized GaN/SiC Heterostructures: *Jie Bai*[1]; Michael Dudley[1]; Pelagia-Irene Gouma[1]; Marina Mynbaeva[2]; [1]Stony Brook University, Matls. Sci. & Engrg., Stony Brook, NY 11794-2275 USA; [2]Ioffe Physico-Technical Institute, St. Petersburg 194021 Russia

GaN based heterostructures have attracted much attention due to their potential application in a variety of electronic and optoelectronic de-

vices. For the case of GaN/SiC, electrochemical anodization of the heterostructure is one strategy that has been adopted to partially relieve undesired stress arising from lattice mismatch and differences in thermal expansion. GaN/SiC heterostructures that were subjected to post growth anodization were found to have improved photoluminescence properties. The study presented here was designed to investigate the influence of such a post-epilayer growth anodization treatment on the structural properties of the heterostructure and its potential role in refining optical properties. Transmission Electron Microscopy (TEM), Synchrotron X-ray topography and High Resolution X-ray diffraction techniques were used to compare microstructures and strains in anodized and virgin structures. High Resolution X-ray Diffraction shows that the anodized epilayer peak is broader than the unanodized epilayer peak and the diffuse scattering intensity is higher for the anodized epilayer and overlaps with the substrate. TEM shows that the anodization produced a "dendritic-type" porous structure which shows a step-wise appearance in both the GaN epilayer and the SiC substrate. The density and the type of the dislocations in the anodized epilayer is mostly no different from those observed in the unanodized sample. Surface asperities were revealed in the TEM micrographs of the anodized GaN, which were associated with points of dislocation termination at the epilayer surface.

Session H: Epitaxial Oxides and Ferroelectrics

Wednesday PM Room: Ballroom East
June 25, 2003 Location: Olpin Union Building

Session Chairs: Darrell Schlom, Pennsylvania State University, University Park, PA 16803-6602 USA; Charles Ahn, Yale University, Dept. of Applied Physics, New Haven, CT 06520-8284 USA

1:30 PM Invited

H1, X-Ray Imaging of Thin Films and their Interface with Substrate with Sub-Angstrom Resolution: *Y. Yacoby*[1]; [1]Hebrew University, Racah Inst. of Physics, Jerusalem 91904 Isreal

We discuss a new x-ray method called Coherent Bragg Rod Analysis (COBRA) to image epitaxially grown thin films and their interface with the substrate crystal. The structure is determined by measuring the diffraction intensities along the substrate defined Bragg rods and then calculating the diffraction phases. In calculating the diffraction phases we make use of the fact that the complex scattering factors vary continuously along the Bragg rods. It turns out that this fact and the fact that we have some a-priori information about the system, for example the substrate structure, allows us to determine the complex scattering factors along the Bragg rods. The structure itself is obtained by Fourier transforming the complex scattering factors into real space. We have applied COBRA to investigate the structure of a number of different systems. We have studied the structure of Gd_2O_3, films grown on GaAs. Gd_2O_3 is an excellent passivation layer for GaAs and may be useful as a high k passivation layer for Si. The structure analysis shows that the Gd_2O_3, film adapts itself to the CaAs substrate in two ways. The Gd_2O_3, film abandons its bulk layer sequence in favor of the GaAs layer sequence and the Gd atoms very close to the interface are displaced so as to obtain the in-plane positions of the underlying Ga and As atoms in the substrate. This ability of Gd203 to adapt itself to the GaAs structure may be at the heart of its ability to passivate GaAs so effectively. We have also applied COBRA to investigate the structure ferroelectric thin films, in particular $PbTiO_3$ grown on $SrTiO_3$. At room temperature $PbTiO_3$ is ferroelectric and its 'a' axis is almost perfectly matched with the $SrTiO_3$ cubic unit cell. Yet the distortions observed in $PbTiO_3$ film are much larger that the distortions in the bulk crystal. We have observed this behavior in both 4 and 9 $PbTiO_3$ unit cell films.

2:10 PM

H2, Lanthanum Aluminate on Silicon for Alternative Gate Dielectric Applications: *L. F. Edge*[1]; V. Vaithyanathan[1]; J. Lettieri[1]; D. G. Schlom[1]; S. A. Chambers[2]; C. L. Hinkle[3]; G. Lucovsky[3]; Y. Yang[4]; S. Stemmer[4]; H. Li[5]; Y. Wei[5]; K. Eisenbeiser[5]; [1]Pennsylvania State University, Matls. Sci. & Engrg. Dept., Matls. Rsch. Inst., University Park, PA 16802 USA; [2]Pacific Northwest National Laboratory, Environml. Molecular Scis. Lab., Richland, WA 99352 USA; [3]North Carolina State University, Dept. of Physics, Raleigh, NC 27695 USA; [4]University of California at Santa Barbara, Matls. Dept., Santa Barbara, CA 93106 USA; [5]Motorola Labs, Physl. Sci. Rsch. Lab., Tempe, AZ 85284 USA

$LaAlO_3$ is one of the most promising alternative gate dielectrics for the replacement of SiO_2 in silicon MOSFETs. Single crystalline $LaAlO_3$ is known to have a dielectric constant of 24 and an optical bandgap of 5.6 eV. The band offsets between $LaAlO_3$ and Si have been predicted to be in the range 2.1 to 3.5 eV for electrons and 1.0 to 1.9 eV for holes.[1,2] It will be shown that $LaAlO_3$ is stable in contact with silicon under standard MOSFET processing conditions. Epitaxial Si has been grown by MBE on single crystals of $LaAlO_3$ and annealed at 1026°C, which is a standard implant activation anneal for MOSFETs, and the interface remained stable and free of SiO_2. A major challenge in the growth of alternative gate dielectrics on Si is the formation of unwanted SiO_2 at the interface. One technique to prevent the formation of SiO_2 is to grow in a low temperature / excess oxidant regime. We have investigated the oxidation kinetics of Al and La, both individually and together (codeposition), to determine the minimum oxygen partial pressure required to achieve fully oxidized $LaAlO_3$. A Sr deoxidation process was used to remove the native SiO_2 from the silicon wafer and ~0.5 ML of Sr was deposited on the wafer before the $LaAlO_3$ deposition. Using these optimized conditions, amorphous $LaAlO_3$ films as thin as 10 Å have been grown on silicon by MBE. AES and XPS analyses indicate that the films are fully oxidized and show no SiO_2. [1]J. Robertson, MRS Bull. 27(3) (2002) p. 220. [2]P. W. Peacook and J. Robertson, J. Appl. Phys. 92 (2002) p. 4713.

2:30 PM Student

H3, Epitaxial MgO with a SrO Buffer Layer on Si(001) by Molecular Beam Epitaxy: Feng Niu[1]; *Anthony L. Meier*[1]; Bruce W. Wessels[1]; [1]Northwestern University, Matls. Sci. & Engrg., 2220 Campus Dr., Evanston, IL 60208 USA

Epitaxial MgO on Si is being considered for integration of optoelectronic and electro-optic devices on Si. MgO is attractive because of its low dielectric constant and refractive index. The mismatch between MgO and Si, however, is large 22.5% so heteroepitaxy is difficult. In this study, high crystalline quality epitaxial MgO on Si(100) substrates were deposited at temperatures as low as 150°C by solid source molecular beam epitaxy and oxygen as the oxidant. In order to attain epitaxy a multilayer structure was developed. The structure consisted of interlayers of Sr silicide and epitaxial SrO. The SrO was introduced in order to reduce strain at the interface. Thin MgO layers grown at 150°C showed streaky reflection high-energy electron diffraction patterns. The MgO showed a cube on cube orientation with respect to Si. Epitaxial MgO layers as thick as 35 nm were deposited. The effects of oxygen partial pressure during MgO deposition (10-8 to 10-7Torr), and the substrate temperature (25°C to 600°C) were investigated. In order to obtain high quality MgO, SrO interlayers of 5nm or greater were required. Films were characterized by x-ray diffraction (XRD) and atomic force microscopy (AFM). The FWHM of the SrO(200) x-ray rocking curve was less than 0.05°. The FWHM of the MgO(200) rocking curve was 2.2°.

2:50 PM Student

H4, Integration of $BaTiO_3$ Ferroelectric Thin Films with GaAs Using MgO and Al_xO_y Buffer Layers: *Timothy Murphy*[1]; Ding-Yuan Chen[1]; Jamie D. Phillips[1]; [1]University of Michigan, Electl. Engrg. & Compu. Sci., Solid State Elect. Lab., 1301 Beal Ave., Ann Arbor, MI 48109-2122 USA

The integration of perovskite oxides with semiconductors is highly attractive due to the potential of providing functional properties including ferroelectric, piezoelectric, electro-optic, and superconducting properties with semiconductor electronics and optoelectronics. The integration of ferroelectric oxides with GaAs-based materials may have a large impact on applications including monolithic optoelectronic integrated circuits, advanced metal-oxide-semiconductor structures, and multi-functional optoelectronic devices. For these applications, single crystalline ferroelectric films are necessary and therefore, require epitaxial growth techniques. Unfortunately, the lattice constant of perovskite ferroelectric materials such as $BaTiO_3$ (c=4.03 Å) is significantly smaller than GaAs (a=5.65 Å), with a lattice mismatch of approximately 30%. Furthermore, the elevated growth temperatures typically required for the epitaxial growth of these oxides (>600°C) present problems with interdiffusion or

alloy formation at the ferroelectric/GaAs interface. The growth of MgO buffer layers provide an attractive alternative, where high quality cube-on-cube oriented (001) MgO films on (001) GaAs at low growth temperatures (~350°C) have been achieved.[1,2] Here we present recent work on the integration of $BaTiO_3$ thin films on GaAs that incorporates both traditional MgO buffers and the novel use of Al_xO_y buffers produced through wet-oxidation of AlGaAs. The use of wet-oxidized Al_xO_y buffers is attractive for integrating $BaTiO_3$ on GaAs due to the low index of refraction (n~1.6), ability to obtain thick layers with excellent flatness, and potential for strain relaxation and defect reduction.[3] These characteristics are highly desirable for photonics applications requiring waveguide structures and for electrical devices requiring selective isolation layers. In this work, results on $BaTiO_3$ thin films deposited by pulsed laser deposition (PLD) on GaAs (001) substrates using MgO buffers and MgO/GaAs/Al_xO_y buffers will be presented. MgO buffer layers were deposited using PLD with varying GaAs surface treatments. The Al_xO_y buffer layers were obtained through the selective wet-oxidation of AlGaAs/GaAs structures grown by molecular beam epitaxy. The GaAs/AlGaAs structure used a thin cap layer of GaAs to provide a crystalline template for the MgO and $BaTiO_3$ deposition. A thin MgO buffer layer is then deposited on the GaAs template followed by the $BaTiO_3$ ferroelectric film. Structural and electrical properties of these thin films structures will be presented. Surface morphology and crystalline orientation and quality for differing buffer layers and surface treatments will be compared using x-ray diffraction measurements and electron microscopy. Electrical and polarization characteristics of metal-ferroelectric-buffer-GaAs capacitors fabricated from these structures will be presented and compared. [1]K. Nashimoto, D. Fork, and T. Geballe, Appl. Phys. Lett. 60, 1199 (1992). [2]E. Tarsa, M. De Graef, D. Clarke, A. Gossard, and J. Speck, J. Appl. Phys. 73, 3276 (1993). [3]K. Chang, J. Epple, G. Pickrell, H. Lin, K. Cheng, and K. Hsieh, J. Appl. Phys. 88, 6922 (2000).

3:10 PM Break

3:30 PM

H5, Structural and Dielectric Characterization of Epitaxial Rare-Earth Scandate Thin Films: *J. Schubert*[1]; Y. Jia[2]; M. Biegalski[2]; O. Trithaveesak[1]; S. Trolier-McKinstry[2]; D. G. Schlom[2]; [1]Forschungszentrum Jülich GmbH, Inst. für Schichten & Grenzflächen (ISG 1-IT), Leo Brandt Str.13, 52425 Jülich Germany; [2]The Pennsylvania State University, Dept. of Matls. Sci. & Engrg., University Park, PA 16802 USA

The rare-earth scandates ($ReScO_3$, where Re is a rare earth element) were recently proposed as candidate materials for the replacement of SiO_2 in silicon MOSFETs in either amorphous or epitaxial form. That rare-earth scandates are promising for this application was based on measurements on single crystals of three different rare-earth scandates: $DyScO_3$, $GdScO_3$, and $SmScO_3$. All showed relatively high dielectric constants (K), high optical band gap energies, and stability in direct contact with silicon. In this work we investigate the dielectric properties and structural perfection of epitaxial $ReScO_3$ thin films, including compositions identical to those whose properties have been studied as single crystals (i.e., $DyScO_3$ and $GdScO_3$) as well as a new composition whose high melting temperature prevented it from being made and studied as a single crystal (i.e., $LaScO_3$ with T_m ~2290°C). The $ReScO_3$ have an orthorhombic crystal structure (space group Pbnm) with lattice parameters fitting nicely to the lattice parameter of Si(100). To verify that the dielectric properties of $ReScO_3$ single crystals apply to epitaxial $ReScO_3$ thin films and to investigate the properties of new rare-earth scandates, we have prepared $GdScO_3$, $DyScO_3$, and $LaScO_3$ epitaxial thin films using pulsed-laser deposition. The films were grown on $SrTiO_3$(100) and $SrTiO_3$(100) covered with an epitaxial $SrRuO_3$ layer (50-100 nm thick) grown ex situ by pulsed-laser deposition as well. The growth temperature ranged from 500°C to 1000°C. The thin film growth was performed at a pressure of $5x10^{-2}$ Torr using a mixture of O_2 and O_3. The typical film thickness was in the 300 nm range. We have characterized the crystal structure of the films using Rutherford Backscattering spectrometry/channelling and four-circle x-ray diffraction measurements. All of the materials showed epitaxial growth on $SrTiO_3$(100). Channelling minimum yield values (χ_{min}) as low as 3% and rocking curve widths as narrow as 0.06° indicate the good crystalline quality of these epitaxial layers. Electrical measurements were performed to determine the K-values of the different materials in thin film form.

3:50 PM

H6, Thermodynamics of Cavity Nucleation in the Ion-Implanted Single Crystal BaTiO3 for Ferroelectric Thin Film Layer Transfer: *Young-Bae Park*[1]; Harry Atwater[1]; Jennifer Ruglovsky[1]; [1]Harvard University, Appl. Physics Dept., McKay Gordon Lab., 9 Oxford St., Cambridge, Boston, MA 02138 USA

In recent decades, ferroelectric materials have been extensively studied for application in dynamic random access memories, non-volatile random access memories (NV-RAM), MEMS and electro-optic device. In most cases, ferroelectric thin films have polycrystalline microstructures which for ferroelectric device applications may affect charge retention, time-dependent fatigue, piezoelectric coefficients, etc. Although ferroelectric thin films offer several advantages over bulk materials, no thin film devices superior to bulk devices exist to date in spite of a number of different oxide film growth methods to obtain a high quality ferroelectric active layer formation. There is considerable interest in a recent layer transfer and wafer bonding process that produces "Smart-Cut" or "ion-sliced" single crystal thin film layers. Light elements such as hydrogen and helium are implanted into a wafer to a specified projected range and a film of equivalent thickness is exfoliated. In this study, we have performed H+/He+ ion co-implantation on single crystal BaTiO3 and bonded to Si3N4/Si, a dissimilar substrate. The main purpose of this study is the investigation of the ion-induced layer transfer mechanism as a pathway toward high quality single crystal ferroelectric and electro-optic thin films. We report thermodynamic considerations for cavity nucleation and micro crack propagation. After ion implanted, isochronal annealing was performed to observed cavity nucleation, growth and blistering kinetics. The critical radius of cavity is considered by conventional fracture mechanics as a function of ion dose and annealing temperature. Thermodynamic calculation of the hydrogen-doped BaTiO3 for equilibrium composition in the cavity is obtained by Gibbs free energy minimization method. Bulk single crystal BaTiO3 was processed by high dose ion implantation. The ion implantation condition was 80 keV for H+ with a dose of 5E16/cm2 ~ 1E17/cm2. For He+, the energy was 115 keV with a dose of 1E17/cm2 for BaTiO3. Samples were bonded at room temperature (25°C). For cavity growth and subsequent layer splitting, isochronal annealing was performed at 300 ~ 500°C in a vacuum ambient of 1E-6 torr. Cavity nucleation and blistering phenomena were observed by optical microscopy and focused ion beam scanning electron microscopy (FIB-SEM). Cavity growth is also observed by in situ isochronal annealing in the FIB chamber. AFM was also used to characterize surface roughness and measured the size of surface blisters, cavity radius and height. Micro-Raman spectroscopy gave complementary information about damage structural or chemical disorder in the implanted layer. For structural analysis, TEM analysis was conducted. Blistered BaTiO3 single crystal pieces were set on a carbon coated TEM grid. For the oxide layer stoichiometry, RBS was performed before and after layer splitting with ion implantation. Elastic recoil detection (ERD) analysis was also conducted for hydrogen concentration depth profile.

4:10 PM

H7, Electric Field Cycling-Induced Oxygen Tracer Drift in PZT Thin Films for Ferroelectric Memories: *Lawrence F. Schloss*[1]; Paul C. McIntyre[1]; [1]Stanford University, Matls. Sci. & Engrg., 476 Lomita Mall, McCullough Bldg., Rm. 205, Stanford, CA 94305-4045 USA

Lead zirconate titanate (PZT) thin films are being developed commercially as the active layer within ferroelectric nonvolatile memory devices (FeRAM). Mechanistic models of the phenomena that limit reliable ferroelectric switching of PZT thin films are needed. In the pursuit of a model for ferroelectric fatigue, the loss of switchable polarization after repeated switching, we have studied the motion of oxygen in MOCVD-grown PZT thin films. These state-of-the-art films, exhibit very low switching voltages (< 1 V) and high switchable polarizations (> 30 $\mu C/cm^2$) in their unfatigued state. Through the introduction of the oxygen isotope, ^{18}O, as a tracer for ionic motion we have observed oxygen self-diffusion and electric field-induced oxygen drift. These observations are of interest in part because they allow one to test existing theories for ferroelectric fatigue which ascribe changes in the switching behavior of ferroelectric domains to motion of charged oxygen vacancies. Oxygen diffuses via the vacancy mechanism in perovskite structure metal titanates such as PZT. Therefore, measurements of oxygen tracer migration under bias allow for the analysis of oxygen vacancy drift. We incorporated the tracer isotope into the film through an exchange anneal and

measured the oxygen isotope concentrations with depth-resolved secondary ion mass spectroscopy (SIMS). Analysis of diffused-in ^{18}O SIMS profiles can be used to probe the initial oxygen vacancy distribution in the samples. We also report on the kinetics of tracer exchange between the PZT film and the testing environment that occur during electric field cycling used in fatigue testing of ferroelectric capacitors. Effects of sample pre-processing, specifically the thermal history, on oxygen drift and diffusion in these films will be highlighted. In addition we will report on the extent to which various top electrode materials, both metals and metallic oxides, affect oxygen drift during electrical fatigue stressing of PZT capacitors.

4:30 PM Student

H8, Ion Beam Etching of Lead Zirconate Titanate Films: *Steven J. Gross*[1]; Qingqi Zhang[2]; Srinivas Tadigadapa[1]; Susan Trolier-McKinstry[1]; Thomas N. Jackson[1]; [1]The Pennsylvania State University, Electl. Engrg., 121 Electl. Engrg. E., University Park, PA 16802 USA; [2]Geospace Research Inc., 550 N. Continental Blvd., El Segundo, CA 90245 USA

Lead zirconate titanate (PZT) is a material of great interest due to its excellent dielectric, piezoelectric and ferroelectric properties. PZT films have been investigated for use in electronic memory devices and capacitors, and more recently, as sensors and actuators in the integration of microelectromechanical systems (MEMS)[1,2]. In MEMS fabrication, a reliable and accurate means of pattern transfer is sought that is compatible with existing materials and processes. Wet etching of PZT is possible with strong bases or acids such as HF and KOH. Although wet etching can offer precise control with underlying etch-stop layers, the same etchant can also be detrimental to other materials. Also, wet etching is typically isotropic, and lateral control can become a concern as dimensions decrease; preferential etching along grain boundaries can exacerbate this problem. In contrast, ion milling or ion beam etching is a highly anisotropic process due to the purely physical nature of the etching[3]. One micron PZT samples were prepared by the sol-gel technique on Pt/SiO2/Si substrates and etched using Argon at energies of 1 keV, a beam current of 0.6 mA/cm2, a process pressure of 0.2 mTorr and an angle of incidence of 45°. At these conditions the etch rate of the PZT films was measured to be 22 nm/min. The simplest mask used was a Shipley 1827 positive photoresist 3µm thick hard baked 150°C for ten minutes. The resist mask can be removed by an oxygen plasma. Several experiments were performed to observe and quantify the effect of ion bombardment on the ferroelectric properties of the films. Films with no mask or top electrode were exposed to the beam for fifteen minutes at the conditions specified. A distorted polarization-electric field hysteresis loop was observed, with a shift in coercive field caused by an internal field, Ei , that increased from 4 kV/cm before etching to 84 kV/cm after etching. Annealing at 450°C in an air or oxygen ambient largely restored the ferroelectric characteristics and reduce the internal field to 8kV/cm. Samples protected by a mask, including the photoresist used for patterning, showed no radiation damage. [1]S. Trolier-McKinstry, J. Ceramics Society of Japan, 109(5), 2001. [2]P.F Baude, C. YE, D.L. Polla, MRS Symp. Proc., 310, 1993. [3]R.E. Lee, VLSI Electronics: Microstructure Science, Vol 8, Academic Press, 1984.

Session I: Low Dimensional Structures for Devices

Wednesday PM Room: Ballroom West
June 25, 2003 Location: Olpin Union Building

Session Chairs: Glenn Solomon, Stanford University, Stanford, CA 94305-4075 USA; James Merz, University of Notre Dame, Notre Dame, IN 46556-5602 USA

1:30 PM Student

I1, Characterization of MBE-Grown Silicon Germanium/Silicon Multiple Quantum Wells for Terahertz Detector Applications: *Pengcheng Lv*[1]; Samit K. Ray[1]; Ralph T. Troeger[1]; Thomas N. Adam[1]; Xin Zhang[1]; Chaoying Ni[2]; James Kolodzey[1]; [1]University of Delaware, Dept. of Electl. & Compu. Engrg., 140 Evans Hall, Newark, DE 19716 USA; [2]University of Delaware, Dept. of Matls. Sci. & Engrg., 201 Dupont Hall, Newark, DE 19716 USA

SiGe/Si quantum well structures have been studied extensively in the past decade for their potential applications in quantum well infrared photodetectors (QWIP). QWIPs operating at 3-5 mm and 8-10 mm have been realized. Extending the wavelength range to around 10 terahertz (30 mm) would be important for many applications, such as terahertz imaging, infrared astronomy and satellite mapping. Structures that can be used to detect such a long wavelength, however, were rarely reported in the literature. In this study, we report the growth and characterization of a multi-quantum well Si0.7Ge0.3 photodetector structure designed to operate in the terahertz range using heavy hole(HH) to light hole (LH) intersubband transition. A SiGe/Si multiple quantum well structure was grown by molecular beam epitaxy on Si(001) substrates at a relatively low growth temperature of 400°C.The quantum wells are nominally 1.6nm Si0.7Ge0.3, boron doped to have a sheet carrier concentration of 1.2e12 cm-2 ,sandwiched between 1nm Si barrier and further separated by 10nm Si0.9Ge0.1 spacer. High-resolution XRD rocking curve exhibiting the Pendellosung frings shows the growth of a good quality pesudomorphic structure. Reciprocal lattice mapping at the (004) reflection was used to characterize the epitaxial quality. Cross sectional transmission electron microscopy (TEM) is used to study the interfaces. Both techniques indicated the growth of a good quality epitaxial layer. Photodetector devices were fabricated by polishing the structure into a waveguide geometry and evaporating metal contacts. Current-voltage measurements without illumination at temperatures ranging from 10K-250K were performed. Thermionic emission with an activation energy of ΔE= 31meV was observed at Vb =0.1V, indicating that the Fermi energy lies 10 meV above the ground heavy hole (HH) state. Absorption measurements were performed with a fourier transform infrared spectroscopy (FTIR) using a DTGS-PE detector. Intersubband absorption at long wavelength (~30mm) was observed at cryogenic temperatures. The band structure was calculated with a 6 band k.p method,from which the absorption peaks were assigned. Theoretical absorption curves were calculated and compared with experimental data, good agreement was achieved. These results suggest the possibility of utilizing SiGe intersubband devices for terahertz detector operating at the long wavelength range.

1:50 PM

I2, Mid-Infrared Ge Quantum Dot Photodetector: *Fei Liu*[1]; S. Tong[1]; J. L. Liu[2]; K. L. Wang[1]; [1]University of California at Los Angeles, Device Rsch. Lab., Dept. of Electl. Engrg., Los Angeles, CA 90095-1594 USA; [2]University of California at Riverside, Dept. of Electl. Engrg., Riverside, CA 92521 USA

The 3-5um is one of the important windows for infrared detector applications due to low loss of atmosphere in this region.Because of large discontinuity in the valance band, the intersubband transition of holes from the ground state of dots to the continuum states can be designed for infrared detectors working in this regions. Ge/Si photodetector monolithically integrated on Si substrate has an advantage of being compatible with CMOS IC technology. Using quantum dot superlattices instead of multi-quantum wells, smaller photoconductive loss is antipated due to a reduced capture probability of photogenerated carriers by the dots. Another advantage of the quantum dot photodetector is related to the nonvanishing normal incidence absorption. In this presentation, experimental results on the Ge quantum dot mid-infrared photodetectors will be reported. The detector structure was grown at 540C on a double-side-polished Si (100) wafer with a boron doping of 11019cm-3. The active region consisted of 20 periods of Ge quantum dot layers separated by 20 nm Si barriers. Ge dots were grown under the Stranski-Krastanov mode. The boron doping density for the Ge layers were about 61018 cm-3. The embedded active superlattice region was separated by two Si(100nm) intrinsic spacer layers from the P+ Si contact layers (300nm). Mesa-type photodetectors were fabricated by standard photolithography. I-V characteristic of the sample at both 77K and 300K was shown to be symmetric versus the applied bias, indicating that the p-i-p structure had symmetric doping. Normal incidence photocurrent spectra of the sample were measured at about 50K for bias voltages ranging from 0.4V to 3V. As the bias increased, the intensity increased as the result of more efficient electrodes collection of photo-induced carriers at higher biases. The response peak was observed at around 2.5m with a bias of 0.4V.

With the increasing bias, redshift of the photocurrent maximum was observed. Because more holes were injected and occupied excited levels of quantum dots at higher bias, the increase of the hole density would shift all the energy levels to a highter value in a self consistent manner and the separation of the continuum and these quantized states red shifts. In order to achieve 3-5um detection, we carried out annealing at 700C and 900C for 5 minutes to promote Si/Ge intermixing. At bias voltage about 0.5V, peak photoresponse of 700C annealed sample shifted from 2.5um to 2.8um, peak for 900C annealed sample shifted to around 3.0um. As a result of interdiffusion between Ge and Si, the Ge content in the quantum dot decreased and the offset of the valance band was smaller. In summary, Mid-infrared Ge quantum dot photodetectors have been fabricated. All the results make Ge quantum dots on Si substrate a promising candidate for mid-infrared photodetectors.

2:10 PM

I3, Phase Diagram of the Stranski-Krastanov Mode for the SiGe/Si Heterostructure System and Application for Solar Cells with Self-Assembled Ge Quantum Dots: *Kazuo Nakajima*[1]; [1]Tohoku University, Inst. for Matls. Rsch., Katahira 2-1-1, Aoba-ku, Sendai, Miyagi 980-8577 Japan

The phase diagram of growth mode is a very effective guideline to grow the high-quality layer or quantum dots of SiGe on Si substrate. In this work, the strain, surface and interface energies of the SiGe/Si (SiGe grown on Si) heterostructure system were calculated for the Frank-van der Merwe (FM) growth mode (layer-by-layer growth on a substrate), the Stranski-Krastanov (SK) mode (the first layer remains smooth on a substrate and then clusters form on the top of the layers), and the Volmer-Weber (VW) mode (clusters form on a substrate). The free energies for each growth mode were derived from these three energies, and they were determined as a function of the composition and layer thickness of SiGe on Si substrate. By comparison of the free energies, the phase diagram of the FM, SK and VW growth modes for the SiGe/Si system was determined. The (111) and (100) surfaces were selected for this calculation. From the phase diagram for the (111) face, it was found for the growth of SiGe on Si that the layer-by-layer growth such as the FM mode was easy to be obtained when the Ge composition is smaller than about 0.5, and the island growth on a wetting layer such as the SK mode was easy to be obtained when the Ge composition is larger than about 0.5. The VW mode is energetically stable in the Ge-rich compositional range, but it is difficult for the VW mode to appear for the actual growth of SiGe on Si because the VW region is right above the SK region. Solar cells with self-assembled Ge quantum dots stacked in multilayer structure (i.e. 50 and 100 periods) were prepared in the SK or VW stable regions using a gas-source molecular beam epitaxial (MBE) method. Enhanced quantum efficiency in the infrared region was found for the solar cells with Ge dots by comparing with the solar cells without Ge dots. This result shows that electron-hole pairs generated in Ge dots can be efficiently separated by the internal electric field, and contribute to the currents without considerable recombination in Ge dots or at Ge/Si interfaces. The phase diagram of growth mode was determined for the SiGe/Si heterostructure system, and it is useful to know where the SK and VW regions appear. The solar cells with Ge dots grown in these regions were prepared, and it was found that they showed enhanced quantum efficiency by comparing with those without Ge dots.

2:30 PM

I4, Stark Shift in Multiple Quantum Well Structures Containing a Delta-Doping Superlattice for Amplitude Modulation: *Patricia Lustoza Souza*[1]; Christiana Villas-Boas Tribuzy[1]; Sandra Marcela Landi[1]; Mauricio Pamplona Pires[1]; Magnus Borgström[1]; [1]Pontifícia Universidade Católica do Rio de Janeiro, LabSem/CETUC, Rua Marquês de São Vicente 225, Rio de Janeiro, RJ 22453-900 Brazil

Recent demands for multiterabit communication require external optical modulators operating at low voltages. Amplitude modulators based on the Quantum Confined Stark Effect in III-V semiconductors multiple quantum well (MQW) systems are suitable for meeting these technological demands. One of the crucial requirements for modulation at high bit rates is that the change in absorption per applied voltage be as large as possible. In other words the Stark shift should be maximized. The larger the quantum well is, the larger the Stark shift. However, increasing the QW width decreases the oscillator strength for absorption. Thus, a compromise is imposed. As an alternative for increasing the Stark shift, Batty and Allsopp[1] have proposed the introduction of an nipi delta-doping superlattice in a MQW structure. GaAs/AlGaAs MQW structures have been grown with Si delta layers centered in the QWs and with C delta layers centered in the barriers. For applications in amplitude modulators, where the MQWs form the intrinsic active region of the device, it is crucial that the net doping corresponds to an undoped structure, so that the external electric field is essentially applied in the MQW region. Otherwise, no Stark shift can be observed. A balance of the electron and the hole concentrations in the delta layers is therefore needed. However, the efficiency of the p type doping depends on the n type doping level,[2] which renders an adequate charge balance difficult to be achieved and consequently, almost impossible to observe any Stark shift. In this communication, we report for the first time the experimental observation of a Stark shift for a GaAs/AlGaAs MQW structure containing an nipi delta-doping superlattice. Photocurrent measurements, which reveal the absorption properties of the structures, were carried out as a function of the externally applied reverse bias. From the obtained curves, the Stark shift was determined for an operation energy 30 meV below the fundamental bandgap. A Stark shift around 6 meV for an electric field of 58 KV/cm, equivalent to that of a reference undoped MQW sample, was measured. Even though this value is still a factor of two below that previously predicted,[1] it shows that it is possible to fabricate amplitude modulators using an nipi delta-doping superlattice in a MQW structure. Furthermore, from the photocurrent measurements, the chirp parameter was calculated using the Kramers-Krönig relations. In optical communication systems it is important that the chirp parameter, which measures the change in refractive index per change in absorption coefficient, be between 0 and -1 to compensate for the positive fiber dispersion. A chirp parameter within this range was obtained, contrary to the value of + 1.8 for the reference sample, showing that such device, as a whole, may have a better performance. [1]W. Batty and D. W. E. Allsopp, Electronics Letters 29, 2066 (1993). [2]C. V.-B. Tribuzy, M. P. Pires, R. Butendeich, S. M. Landi, P. L. Souza, G. E. Marques, A. C. Bittencourt and A. B. Henriques, Physica E 11, 261 (2001).

2:50 PM Student

I5, Fabrication and Speed-Power Characterization of Quantum Wire Switches with Nanometer-Scale Schottky Gate Control for GaAs Hexagonal BDD Quantum Circuits: *Miki Yumoto*[1]; Seiya Kasai[1]; Hideki Hasegawa[1]; [1]Hokkaido University, Rsch. Ctr. for Integrated Quantum Elect. & Grad. Sch. of Elect. & Info. Engrg., N13, W8, Sapporo 060-8628 Japan

Quantum devices will play important roles in next-generation ultra high-density, ultra high-speed and ultra-low power quantum LSIs beyond scaling limits of silicon LSIs. This is because they can realize a smallest possible power delay product (PDP) near the quantum limit. However, they are too sensitive against off-set charge and structural variations and too weak in current drivability to implement circuits based on the conventional logic gate architecture. To overcome this difficulty, we have recently proposed a hexagonal binary decision diagram (BDD) quantum circuit approach.[1] Here, BDD node devices for binary path switching are realized by quantum transport control of III-V hexagonal nanowire networks by nm-scale Schottky wrap gates (WPGs). The purpose of this paper is to fabricate BDD node devices using WPG-controlled GaAs nanowires and to characterize their speed and power performances. Single and integrated BDD node devices, each consisting of one entry- and two exit-branches, were fabricated on AlGaAs/GaAs nanowire Y-branch structures by MBE growth, EB lithography and wet chemical etching. Nanometer-scale Schottky gates were wrapped around two exit-branches to form Schottky WPGs. Path switching in quantum regime was realized by complimentary switching of exit-branches between zero-th and first steps of conductance quantization. Devices exhibited excellent d.c. gate control characteristics from low temperatures to room temperature. Clear conductance quantization at conductance levels close to $2e^2/h$ was observed at 1-5 K. The gate voltage dependence of the electron line density in the nanowire determined from gate-dependent Shubnikov-de-Haas oscillations gave a gate capacitance of 24 fF for the device with a gate length L_g = 630nm. This together with the observed quantized conductance indicated feasibility of switching in 2-3 GHz range. However, successful a.c. path switching could be directly confirmed only up to several ten MHz on a single device because of its small capacitance and high resistance. To directly confirm GHz operation, RF measurements were carried out on an integrated device where 90 branch switches were connected in parallel. Standard S-parameter measurements

using a HP network analyzer gave f_T = 1 GHz and f_{max} = 5 GHz for a device with L_g = 630 nm, and f_T = 2.5 GHz and f_{max} = 9 GHz for a device with L_g = 110 nm, directly showing feasibility of GHz clock operation for the hexagonal BDD circuits. Equivalent circuit analyses indicated that further improvements should be possible by control of surface states. The estimated PDP value was 10^{-18} J for a single branch switch with L_g = 630 nm. This is still much larger than the quantum limit value, but one order of magnitude better than that of the latest Si CMOS transistor with L_g = 20 nm. [1]S. Kasai and H. Hasegawa, IEEE Electron Device Lett. 23 (2002) 446.

3:10 PM Break

Session J: Low Dimensional Device Structures

Wednesday PM Room: Ballroom West
June 25, 2003 Location: Olpin Union Building

Session Chairs: Glenn Solomon, Stanford University, Stanford, CA 94305-4075 USA; James Merz, University of Notre Dame, Notre Dame, IN 46556-5602 USA

3:30 PM

J1, Spatial Ordering of InAs Quantum Dots in a Microdisk Cavity to Achieve Large Spontaneous Emission Enhancement: *Zhigang Xie*[1]; [1]Stanford University, Stanford, CA 94305 USA

Abstract not available.

3:50 PM

J2, Effect of Si-Delta-Doping on the Luminescence and Laser Properties of InP/InAlGaP Quantum Dots: *X. B. Zhang*[1]; R. D. Heller[1]; Russell D. Dupuis[1]; Gabriel Walter[2]; Nick Holonyak[2]; [1]The University of Texas at Austin, Microelect. Rsch. Ctr., PRC-MER-R9900, 10100 Burnet Rd., Austin, TX 78712 USA; [2]The University of Illinois at Urbana-Champaign, Ctr. for Compound Semiconductor Microelect., Urbana, IL 61801 USA

InP self-assembled quantum dots (SAQDs or simply QDs) on InGaP matrices have been studied by several research groups and on InGaAlP and InAlP matrices by the present authors. The threshold current density of InP/InGaP QD-based injection laser was found to increase dramatically with the temperature. The main reason is the thermal escape of carriers from the QDs. To overcome this problem, larger-bandgap confining layers are required. Lasers emitting in the red spectral region operating CW at 300K were realized by using In0.5(Al0.6Ga0.4)0.5P as the confining layer. Furthermore, by using an auxiliary InGaP quantum well (QW) coupled to the InP QDs through a thin InAlGaP "barrier" layer, the carrier collection efficiency and the operation of QD lasers can be markedly improved. However, due to the intrinsically small conduction-band offset, thermal escape of hot carriers from InP QDs is still a problem to overcome in order to improve the room-temperature laser operation. In this paper, we report on the growth of InP QDs on In0.5Al0.5P matrix with delta doping of Si atoms in the adjacent layer and we find a strong improvement in cathodoluminescence (CL) efficiency of the QDs. InP/In0.5Al0.5P QD samples are grown on (001) GaAs substrates by low-pressure metalorganic chemical vapor deposition (MOCVD). Si delta doping is symmetrically introduced in the lower and upper In0.5Al0.5P matrix layers with distance d away from the QD layer. Sheet carrier density, estimated from the uniform doping in In0.5Al0.5P epitaxial layers under the same conditions, is around 1.5´ 1013 cm-2. Four samples, one without the Si delta doping, and the other threes with the delta doping, whose d is 6, 20 and 40 nm, respectively, are examined in this study. We found that, for d=20 nm, the CL intensity of QDs can be improved by ~16 times. We speculate that the increased CL intensity is caused by the efficient capture of electrons from the reservoir of the delta-doped layer into the QDs, which, to some extent, counter balances the thermal escape of electrons from the QDs. A temperature-dependent CL study of InP QDs grown without Si delta doping shows a quenching of the CL at high temperatures, while delta doped QDs show an anomalous behavior. The QD integrated CL intensity increases with the temperature and then decreases after 200 K. This anomalous behavior is interpreted as caused by competition between two processes: (1) thermal activation of carriers out of the potential well introduced by delta doping and then capture by QDs, which enhances the CL intensity; and (2) quenching of the CL due to thermal activation of carriers out of the QDs. Effect of Si delta doping on laser operation is also studied.

4:10 PM Student

J3, InP Quantum Dot Coupled to InGaP Quantum Well Heterostructure for Room Temperature Continuous Wave Lasers Grown by Metalorganic Chemical Vapor Deposition: *Richard Dean Heller*[1]; X. B. Zhang[1]; Gabriel Walter[2]; Nick Holonyak[2]; David T. Mathes[3]; Robert Hull[3]; Russell D. Dupuis[1]; [1]The University of Texas at Austin, Microelect. Rsch. Ctr., PRC/MER 1.608E, Austin, TX 78712 USA; [2]The University of Illinois at Urbana-Champaign, Ctr. for Compound Semiconductor Microelect., Urbana, IL 61801 USA; [3]The University of Virginia, Dept. of Matls. Sci. & Engrg., Charlottesville, VA 22903 USA

III-P self-assembled quantum dot (SAQD) structures offer the ability to realize injection lasers operating in the visible wavelength region with superior performance characteristics, such as low threshold current density and high characteristic temperature. We have previously reported the device results of InP QD lasers grown by MOCVD that lased optically pumped pulsed at 300K and CW at 77K as well as low-threshold (Jth ~ 1.4 kA/cm^2) electrically pumped InP QD diode lasing. Further, we are able to improve performance dramatically by incorporating an InGaP quantum well coupled to the QD layers by a InAlGaP barrier layer due to resonant tunneling, better carrier collection, better thermalization of carriers, and lateral rearrangement of carriers in the QWs. We will describe the effects of coupling the InP QD states to the electronic states of InGaP QW. Optically and electrically pumped 300K lasing has been achieved using this unique active region design; these lasers show improved operation compared to the lasers having only QD-based active regions including lower threshold current densities. We have studied the morphology and QD density of the exposed SAQDs by AFM. We have used both tensile- and compressive-strained InGaP quantum wells to optimize the QD uniformity and density as well as by varying the thickness of the InGaP QW and InAlGaP barrier layer. We have improved the QD density from 1x10^{10} cm^{-2} to as much as 3x10^{10} cm^{-2} by doing this. Photoluminescence spectra were taken at 300K to determine the light-emitting characteristics of the $In_{0.49}Al_{0.51}P/In_{0.49}(Al_xGa_{1-x})_{0.51}P/In_xGa_{1-x}P$/InP QD+QW heterostructures (QDHs). 300K PL spectra from the InP QDHs exhibit PL emission in the visible orange and red spectral regions. These InP QD active regions have been incorporated into various laser separate-confinement active regions. We have achieved CW 300K laser operation of an $In_{0.49}Al_{0.51}P/In_{0.49}(Al_xGa_{1-x})_{0.51}P/In_{0.49}Ga_{0.51}P$/InP QD+QW laser diode at visible wavelengths (654 nm). We will show from recombination spectra that the gain peaks at the quantum dot state, thus further indicating the coupling of the quantum well states to the quantum dot states. In summary, we have grown and characterized InP SAQDs embedded in $In_{0.49}(Al_xGa_{1-x})_{0.51}P$ coupled to $In_xGa_{1-x}P$ QWs. The InP SAQDs grown by MOCVD at 720°C exhibit uniform morphology with a 5-10 nm dominant height and ~2x10^{10} cm^{-2} density for 7.5 ML. For $In_{0.49}Al_{0.51}P/In_{0.49}(Al_xGa_{1-x})_{0.51}P/In_{0.49}Ga_{0.51}P$/InP QD+QW injection lasers, we have achieved CW lasing at 654 nm at 300K with greatly reduced threshold current densities as low as 0.5 kA/cm^2. We believe this is the first CW 300K operation of a visible-wavelength InP QD laser. We will describe the growth and properties of these novel QD+QW injection lasers as well as compare to previously grown InP QD lasers.

4:30 PM Student

J4, Tunneling Between a Single Impurity and a Quantum Dot: *Erik M. Lind*[1]; Boel Gustafson[1]; Ines Pietzonka[1]; Lars-Erik Wernersson[1]; [1]Lund University, Solid State Physics, Box 118, Lund S-22100 Sweden

Tunneling spectroscopy is an highly useful way of investigating the properties of single low dimensional structures, such as quantum dots. Using a three dimensionally integrated resonant tunneling transistor (RTT)[1] we present data for the transport properties of electrons tunneling from a single impurity into a quantum dot.[2] The RTT consists of a tungsten gate placed 100 nm below and 30 nm above two GaAsP/GaAs resonant tunneling diodes (RTD). The upper RTD is grown on top of the metallic gate. The current through the transistor flows through a designed opening (500x500 nm) in the middle of the gate. For large applied biases, there are several peaks that appear in the current-voltage characteristics due to 2D resonant tunneling through the sub bands of each RTD. The peak current and peak voltage can be controlled by changing the gate

voltage.[1] For small applied biases, we observe lateral and vertical confiment effects. Due to the Schottky depletion around the gate and the two confining RTDs, an electrostatically defined quantum dot is formed between the two RTDs. From the background doping, the larger conducting area of the upper RTD contains a few donor atoms. A single impurity in a RTD is well known to form a bound state roughly 10 meV below the first sub band of the RTD. By applying a bias over the sample, we inject electrons from a single impurity in the upper RTD into the quantum dot formed between the two RTDs. This constitutes a 0D-0D system. We can thus probe the energy levels of the quantum dot by using the impurity as a truly 0D emitter state. When a dot state aligns with the impurity state, a very sharp current peak of a few pA can be detected, with a FWHM of a few mV. I-V measurements have been done with different applied magnetic fields (0-12T), different temperatures (0.3K-10K) and different gate voltages. The magnetic field dependent measurements can be fitted well by modeling the dot as a 2D harmonic oscillator, and taking into account that the angular momentum of the tunneling electrons has to be conserved. The FWMH of the peaks are only very weakly affected by the temperature, with a peak broadening that is smaller than kT. [1]E. Lind et. al., Appl. Phys. Lett. 81, 1905 (2002). [2]E. Lind et. al. submitted for publication.

4:50 PM

J5, Dependence of InAs Quantum Dots Optical Properties on Capping Materials: GaNAs Strain Compensating Layers (SCL) and GaAs Layers: X. Q. Zhang[1]; S. Ganapathy[1]; *Ikuo Suemune*[1]; B. J. Kim[2]; T. Y. Seong[2]; H. Machida[3]; N. Shimoyama[3]; [1]Hokkaido University, Rsch. Inst. for Elect. Sci., Kita-12, Nishi-6, Kita-ku, Sapporo 060-0812 Japan; [2]Kwangju Institute of Science and Technology, Ctr. for Frontier Matls. & Dept. of Matl. Sci. & Engrg., Kwangju 500-712 Korea; [3]Trichemical Laboratory, Uenohara 8154-217, Kitatsurugun, Yamanashi 409-01 Japan

InAs quantum dots (QDs) have been intensively investigated and several applications of the QDs are being pursued. Single photon emitters (SPE) based on QDs is one of the distinct applications which utilize the intrinsic nature of QDs. For such applications of SPE for quantum cryptography or quantum computation, the quantum efficiency of the SPE is one of the key issues to deal with single photons. In this regard, the optical quality and quantum efficiency of InAs QDs is the main concern. In this paper, the influence of the QDs capping layers will be discussed from the viewpoint of strain. It will be shown that the compensation of the compressive strain induced in InAs QDs with tensile-strained GaNAs cap layers[1,2] improve the luminescence efficiency as well as the homogeneity of the QDs. Samples were grown on GaAs (001) substrates by metalorganic-molecular-beam epitaxy (MOMBE). After a 100-nm-thick GaAs buffer layer was grown at 550°C, the substrate temperature was lowered to 400¡C and 2.0 monolayers (ML) of InAs were deposited. The transition from two-dimensional to the Stranski-Krastanow growth mode was confirmed with the reflection high-energy electron diffraction (RHEED) observations. Two stacks of InAs QDs with 10-nm-thick GaNAs or GaAs capping (spacer) layers were grown at the same substrate temperature. The dependence of the QDs on the capping materials will be mainly discussed. One sample examined is InAs QDs embedded in conventional GaAs capping layers. The other is InAs QDs embedded in GaN0.007As0.993 strain compensating layers (SCLs). In both cases, the QD states were clearly observed in their photoluminescence (PL) spectra, but the filling up to the higher states was more pronounced in the InAs QDs embedded in GaNAs SCLs. This shows the lower contribution of nonradiative recombination in the InAs QDs embedded in GaNAs SCLs, and this indicates the importance of the strain compensation of the compressive strain in InAs QDs with the tensile strain in the GaNAs SCLs. The integrated PL intensity from the InAs QDs is increased with the strain compensation, and about 5-times increase is observed by the capping with the GaNAs SCLs rather than GaAs. In the InAs QDs capped with GaNAs SCLs, the thermal activation energies estimated from the temperature dependence of PL intensities almost agreed with the energy separation of the PL peaks, while they were lower than the energy separation of the PL peaks in the InAs QDs capped with GaAs. This shows that in the latter case there remain some nonradiative recombination centers which lower the thermal activation energy and that the strain compensation is important to improve the optical quality of InAs QDs. [1]S. Ganapathy etal, 14th IPRM May 12-16, 2002, Stockholm, Conf. Proc. p. 557. [2]X. Q. Zhang etal, J. Appl. Phys. 92 (2002) 6813.

Session K: Spin Dependent (or Spintronic) Electronic Materials - II

Wednesday PM Room: 101
June 25, 2003 Location: Olpin Union Building

Session Chairs: Stefano Sanvito, Trinity College, Dept. of Physics, Dublin 2 Ireland; Chris Palmstrøm, University of Minnesota, Dept. of Chem. Engrg. & Matls. Sci., Minneapolis, MN 55455 USA

1:30 PM Student

K1, Magnetic Properties of Mg and Mn Co-Doped GaN Films Grown by PEMBE: *Min-Chang Jeong*[1]; Moon-Ho Ham[1]; Jae-Min Myoung[1]; [1]Yonsei University, Dept. of Matls. Sci. & Engrg., 134 Shinchon-dong, Seodaemun-gu, Seoul 120-749 Korea

Mg and Mn co-doped GaN thin films were grown on the GaN templates by plasma-enhanced molecular beam epitaxy (PEMBE) at different Mn effusion cell temperatures (T_{Mn} = 630, 650, 700°C) with fixed Mg effusion cell temperature, and their properties were analyzed. Scanning electron microscope (SEM) images show the number of pits on the films' surface decreased as Mn cell temperatures increased. The film grown at T_{Mn} = 700°C exhibited smooth surface morphology and high saturation magnetization (M_s). Secondary phases or clusters were not detected by X-ray diffraction (XRD). Moreover, the Mn and Mg concentrations measured by secondary ion mass spectrometry (SIMS) were uniform in the entire co-doped film thickness and the Mg concentration in the film was ~10^{18} atoms/cm^3. These XRD and SIMS measurements ensured Mn and Mg substituted for Ga. Even though Mg and Mn are the p-type dopants, the films exhibited n-type characteristics ($n \approx 10^{16} \sim 10^{17}$ cm^{-3}) by Hall measurement due to very low Mg and Mn concentrations in the films. The electrical property of Mn doped GaN films was n-type since Mn concentration in the films was not enough to compensate native defects in the GaN films. In the case of Mg dopant, only 1 ~ 2% of Mg in the films is ionized to act as acceptors at room temperature, so ionized Mg concentration in the films is also not enough to exhibit p-type conductivity. Room temperature ferromagnetism was confirmed by highly sensitive (~10^{-8} emu) alternating gradient magnetometer (AGM) measurement. The saturation magnetization of the films increased as Mn effusion cell temperature increased linearly, since the Mn concentration in the films increased with increasing Mn effusion cell temperature. The coercive forces of all the films were in the range of 60 ~ 80 Oe. Hence, Mn nano-clusters which exhibit superparamagnetic behaviors do not exist in the co-doped GaN films. SIMS and XRD measurements support that Mg and Mn co-doped GaN films are single phase showing room-temperature ferromagnetic ordering. Mg and Mn co-doped GaN films exhibited n-type conductivity and room temperature ferromagnetic ordering without secondary phases. From these properties, it is concluded that the room temperature ferromagnetic ordering of Mg and Mn co-doped GaN films is due to the interaction between electron spin and Mn magnetic moment in the low carrier density regime.

1:50 PM Student

K2, Electronic Properties of Epitaxial (In,Mn)As: *Steven J. May*[1]; Aaron J. Blattner[1]; Bruce W. Wessels[1]; [1]Northwestern University, Matls. Sci. & Engrg., 2220 Campus Dr., Evanston, IL 60208-3108 USA

InMnAs is a promising material for heterojunction spintronic devices. In an effort to elucidate the role of Mn, the electronic transport properties of ferromagnetic $In_{1-x}Mn_xAs$ alloys were investigated using temperature dependent Hall effect measurements. Epitaxial layers with Mn concentrations ranging from x<0.01 to x=0.2 were grown using metalorganic vapor phase epitaxy on semi-insulating GaAs(001) and InAs substrates. The magnetic properties of a sample (x=0.02) were examined using SQUID magnetometry and it was found to exhibit strong ferromagnetism with a Curie temperature of 330 K. Transport properties were measured from 77-300 K. All (In,Mn)As films investigated were p-type. For low Mn concentration sample (x<0.01 and p_{300K}=5.8x10^{18} cm^{-3})

a maximum in mobility of 95 cm^2/V-s at 150 K was observed. Upon increasing the temperature to 300 K the mobility decreased to 54 cm^2/V-s. The measured ionization energy for this sample was 16 meV, comparable to that previously measured for Mn doped Czochralski grown crystals (D. G. Andrianov et al. Sov. Phys. Semicond., 11 (1977) 738; E. I. Georgitsé et al. Sov. Phys. Semicond. 23 (1989) 469). An $In_{1-x}Mn_xAs$ sample with x=0.02 (p_{300K}=7.9x10^{17} cm^{-3}) exhibited different transport behavior. The Hall mobility was strongly temperature dependent with a maximum of 93 cm^2/V-s occurred at 200 K and decreased to 77 cm^2/V-s at 300 K. The acceptor ionization energy was determined to be zero. Upon further increasing the Mn concentration to x=0.2, MnAs nanoprecipitates were observed in the (In,Mn)As matrix. The alloy was semiconducting and p-type with a temperature independent carrier concentration, indicative of a degenerate semiconductor. The mobility increased with temperature from 22 cm^2/V-s to 38 cm^2/V-s and then remained constant up to 300 K. Other similar films with large Mn concentrations exhibited comparable behavior with Hall mobility up to 50 cm^2/V-s. The relatively high mobility indicates that these materials may be suitable for spintronic devices. Homoepitaxial, single phase, p-type (In,Mn)As films on n-type InAs(001) substrates have been grown by metalorganic vapor phase epitaxy. Diodes have been fabricated and p-n junction rectification has been observed at room temperature. Ferromagnetic properties of these layers are currently under study.

2:10 PM

K3, Room Temperature Ferromagnetic Properties of Mn-Doped InxGa1-xN: *Meredith Lynn Reed*[1]; Maria K. Ritums[1]; Mason J. Reed[1]; N. A. El-Masry[1]; S. M. Bedair[2]; J. M. Zavada[3]; [1]North Carolina State University, Matls. Sci. & Engrg., 234 Riddick Labs., Box 7907, Raleigh, NC 27695-7907 USA; [2]North Carolina State University, Electl. & Compu. Engrg., 232 Daniels Hall, Box 7911, Raleigh, NC 27695 USA; [3]Army Research Office, Research Triangle Park, NC 27709 USA

We report on the room temperature ferromagnetic properties of Mn-doped $In_xGa_{1-x}N$ with x < 0.15. $In_xGa_{1-x}N$ layers were grown via metal-organic chemical vapor deposition, while the Mn doping was performed by solid state diffusion of a surface Mn layer deposited by pulsed laser ablation. The easy axis of magnetization depends on the stress state of the $In_xGa_{1-x}N$ film. The easy axis rotates from in-plane to out of plane by changing the film thickness thus going from strained to fully relaxed films. For intermediate film thickness a transition region of partially relaxed film was identified with isotropic magnetic behavior. These ferromagnetic results are consistent with the strained and the relaxation process in this material system obtained from both optical and structural measurements.

2:30 PM

K4, Ferromagnetic GaMnAs and GaMnP Formed by Mn Ion Implantation and Pulsed Laser Melting: *M. A. Scarpulla*[1]; O. D. Dubon[1]; Kin M. Yu[2]; W. Walukiewicz[2]; O. Monteiro[2]; [1]University of California, Berkeley and Lawrence Berkeley National Laboratory, Berkeley, CA 94720 USA; [2]Lawrence Berkeley National Laboratory, Berkeley, CA 94720 USA

Dilute alloys of transition metals in semiconductor hosts, especially Mn alloyed in GaAs, continue to be intensely investigated for applications in spin-based electronics. The precise origin of ferromagnetism in these materials is unknown. This has generated interest in devising a versatile method to produce the widest possible variety of diluted magnetic semiconductors (DMSs), which, in general, exist at the kinetic limit of stability. Synthesis approaches have ranged from thermal evaporation and annealing to the most advanced thin-film deposition technique. For DMSs based on III-V semiconductors, low-temperature molecular beam epitaxy (LT-MBE) has been the synthesis method of choice. Recently we have formed thin films of ferromagnetic $Ga_{1-x}Mn_xAs$ and $Ga_{1-x}Mn_xP$ by Mn ion implantation into GaAs and GaP substrates, respectively, followed by pulsed laser melting. These films exhibit high fractions of substitutional Mn (over 50%) and are single-crystalline, traits that cannot be achieved using other non-MBE synthesis routes. $Ga_{1-x}Mn_xAs$ films produced using this method exhibit a ferromagnetic Curie temperatures, T_c, as high as 85 K, which approaches the T_c of 110 K typically observed in films grown by LT-MBE. Changing the semiconductor host from GaAs to GaP results in a $Ga_{1-x}Mn_xP$ film with a significantly lower Curie temperature. Unlike LT-MBE, the combined ion implantation and pulsed laser melting approach allows for the rapid prototyping of DMSs, thereby creating opportunities for the study of ferromagnetism in a wide range of materials. For example, guided by the Fermi-level-induced limitation on the Curie temperature of $Ga_{1-x}Mn_xAs$, we are undertaking investigations to further increase the T_c by using heavy n-type counter-doping of $Ga_{1-x}Mn_xAs$ via Te ion implantation as a remedy for the otherwise unavoidable creation of Mn interstitials at higher values of x. In such $Ga_{1-x}Mn_{1-x}Te_zAs_{1-z}$ alloys, it should be possible to achieve values of $x \equiv p_{max}+z$ where p_{max} is the maximum attainable free hole concentration. Although the hole concentration would still be "pinned" at p_{max} by the limit imposed on the Fermi level, the concentration of active Mn should increase in proportion to x, thus increasing T_c. We will discuss our investigations on the effect of co-alloying as well as potential applications of our synthesis technique toward the production of spintronic devices.

2:50 PM K5, Late News

Session L: Non-Destructive Testing and In-Situ Monitoring

Wednesday PM Room: 101
June 25, 2003 Location: Olpin Union Building

Session Chairs: Kurt Eyink, US Air Force, AFRL/MLPO, Wright Patterson AFB, OH 45433-7707 USA; Mark Goorsky, University of California-Los Angeles, Dept. of Matl. Sci. & Engrg., Los Angeles, CA 90095-1595 USA

3:30 PM

L1, SiC Epitaxial Film Characterization Using FTIR Spectroscopy and Improved Parameter Estimation: *Michael S. Mazzola*[1]; Janice P. Mazzola[2]; Swapna G. Sunkari[1]; Jeffrey L. Wyatt[1]; Yaroslav Koshka[1]; [1]Mississippi State University, Electl. & Compu. Engrg., Box 9571, Miss. State, MS 39762 USA; [2]SemiSouth Laboratories, Inc., 1 Research Blvd., Ste. 201, Starkville, MS 39759 USA

Film thickness, free carrier concentration, and free carrier mobility are critical figures of merit for silicon carbide epitaxial growth. Room temperature Fourier Transform Infrared (FTIR) reflectance spectroscopy can estimate these parameters non-destructively and provide high-resolution wafer mapping. Commercially available equipment has greatly simplified the application of this technique by coupling a high performance automated spectrometer with model-based data analysis and interpretation based on the personal computer. Multiple layers of homoepitaxy of varying doping concentration and type are common in device applications. The model-based analysis of reflectance spectra taken from these materials is complicated by two factors. First, the contrast between different layers is very small, due to the close similarity of the dielectric functions expected between epitaxial films of the same semiconductor. Second, the addition of multiple layers introduces many degrees of freedom, which complicates parameter extraction. While powerful numerical techniques run fast and efficient on modern computers, it is essential that low-order, well-conditioned models be used. In particular, we have observed that p-type SiC produces significantly degraded sensitivity as compared to n-type SiC. Where a n-type epi layer with a net free carrier concentration as low as 1 x 10^{18} cm^{-3} is reliably detected and its thickness estimated, a similarly doped p-type epi layer is often not detected with respect to an underlying lightly doped epi layer; and, if detected, its correct thickness is often ambiguous. This problem limits the application of this technique in technologically important applications, such as p-i-n diodes and bipolar junction transistors. A common modeling assumption appears to be the limiting factor. Typically, the contributions to the dielectric function from the phonons and the plasmons (i.e., free carriers) are assumed to be uncoupled. For example, a heavily doped epi layer is typically modeled with a fixed phonon contribution derived from undoped material and an adjustable plasmon contribution. This approach is relatively insensitive to the low conductivity that p-type SiC produces. Alternatively, we have empirically included the doping dependence of the phonon terms in the individual epi layers. With this approach, we have observed significantly enhanced sensitivity and improved parameter extraction from a 0.75-µm thick p^+ epi layer grown on a 2.42-µm n-type epi layer. The experimental results are

consistent with optical scattering by LO-phonon-plasmon-coupled modes.[1]
[1]H. Harima, S. Nakashima, and T. Uemura, J. Appl. Phys., 78, 1996 (1995).

3:50 PM

L2, Spectroscopic Ellipsometric Monitoring of Planar InAs Growth on GaAs(001): *Kurt G. Eyink*[1]; Larry Grazulis[1]; Krishnamurthy Mahalingam[1]; [1]Air Force Research Laboratory, AFRL/MLPS, 3005 P St., Ste. 6, Wright-Patterson AFB 45433-7707 USA

InAs growth on GaAs has considerable morphological variation depending on the growth conditions used during deposition. Growth, under conditions producing the 2x4 reconstruction, results in the formation of self-assembled quantum dot structures. In this paper, we are studying the changes in the ellipsometric signal in the range of 400-800nm, which result during the deposition of indium under the 4x2 metal stabilized conditions as well as the ultimate surface morphology. It has previously been reported that these conditions result in the formation of planar InAs up to thickness of 200nm.[1,2,3] AFM analysis of these surfaces showed a fingered morphology in agreement with earlier STM studies.[2,3] We have found that if we carried out these growths using MEE (migration enhanced epitaxy) that growth was severely limited in opposition to the previous STM studies.[2,3] A nominal 30 monolayers deposition resulted in four monolayers. Continuous MBE growth under 4x2 conditions allowed us to deposit 20-30nm thick films in approximately an hour using a beam equivalent pressure of 3x10-8 torr In and 1x10-7 torr overpressure of As4. The AFM images of the resulting surface showed large pits. Even with these large defects, the reflection high-energy diffraction maintained a 4x2 reconstruction with out a strong indication of 3D diffraction. The critical point structure was followed during the deposition and showed the formation of an InAs peak. Careful examination of the ellipsometric trajectory showed a change in the optical properties of the film after approximately 10 minutes of InAs growth. This change could be the formation of the pit structure or the relaxation of the film. A more detailed analysis will be given during the presentation.
[1]W. J. Schaffer, M. D.Lind, S. P. Kowalczyk, and R. W. Grant, J. Vac. Sci. Technol. B1(3), 688-695, (1983). [2]Q. K. Xue and T. Sakurai, Phys. Rev. B, Vol 57, No. 12, R6862-R6865. [3]Q. K. Xue, Y. Hasegawa, T. Ogino, H. Kiyama, and T. Sakurai, J. Vac. Sci. Technol. B15(40), 1270 1273 (1997).

4:10 PM Student

L3, Impact of Low Frequency Magnetic Field on the Electrical Characteristics of Shallow P+N Junctions: *Moustapha Abdelaoui*[1]; Malika Idrissi-Benzohra[1]; Halima Mehor[1]; Mohamed Benzohra[1]; François Olivie[2]; [1]LEMI - Université de Rouen, Rue Lavoisier, Mont Saint Aignan 76821 France; [2]LAAS - CNRS, 7 Ave. du Col. Roche, Toulouse 31077 France

The recent developments in embarked equipments (automotive and avionics systems), in particular the increased requirements for reduction of electronic system dimensions have as a consequence new serious dysfunction and failure. These problems are often caused by time-varying magnetic perturbations, especially low frequency (LF), generated by neighboring high-power electrical modules. So it appears necessary to study and analyze the coupling between the low frequency magnetic waves and the electrical characteristics of electronic components. This experimental work contributes to understand these phenomena and quantify their impact. The tests are performed on shallow P+N junctions formed by low energy B implantation -2x1015 cm-2 at 3 KeV- into a reference or preamorphized with high-energy germanium -1015 cm-2 at 2.2 MeV- n-type crystalline silicon. The preamorphization step was done at ambient or nitrogen temperature. A Rapid Thermal Annealing (RTA) for 15 s at 950°C was then used. The effect of the preamorphization step on the magnetic susceptibility of the junctions is highlighted by forward and reverse current-voltage characterizations. The different measurements were performed under a low frequency (0 to 1 kHz) magnetic field, of a magnitude ranging from 0 to 3000 G, with sample temperature varying between 100 and 300 K, using an Oxford Teslatron system. The results permit us to explore the transport mechanisms occurring across the junction, and study the effect of the magnetic field on the electronic transitions in such samples.

4:30 PM

L4, Using High-Resolution X-Ray Diffraction and X-Ray Topography to Pinpoint Defects in GaAs Wafers: *Christine H. Russell*[1]; Simon Bates[1]; Yauzo Wang[2]; [1]Bede Scientific Incorporated, 14 Inverness Dr. E., Ste. H-100, Englewood, CO 80112 USA; [2]Anadigics Incorporated, 141 Mount Bethel Rd., Warren, NJ 07059 USA

In this paper we present results comparing High-Resolution X-ray Diffraction (HRXRD) data to x-ray topography images collected on a Bede D1 diffractometer in a laboratory environment. Changes in the Full Width at Half Maximum (FWHM) value of the substrate peak are indications of material quality and correspond directly to defects seen with x-ray topography. Either technique can be used for monitoring bare substrate wafers or damage inflicted to a substrate by processing. In some of the samples examined, the changes in the FWHM were dramatic enough to be seen with an open detector. Mapping these changes across the wafer produced an "image" of the defective regions that correspond to defects seen with x-ray topography. This work will compare the two techniques (high-resolution x-ray diffraction and x-ray topography) used to characterize GaAs substrates and device wafers.

4:50 PM L5, Late News

Session M: Metal Contacts to Semiconductors

Wednesday PM Room: 102
June 25, 2003 Location: Olpin Union Building

Session Chairs: Tae-Yeon Seong, Kwangju Institute of Science & Technology, Semiconductor Thin Film Lab., Puk-gu, Kwangju 500-712 Korea; Suzanne Mohney, Pennsylvania State University, Dept. of Matls. Sci. & Engrg., University Park, PA 16802 USA

1:30 PM

M1, Thermodynamically Stable NiSi Ohmic Contacts to n-Type 6H-SiC: *Christpher Deeb*[1]; [1]Case Western Reserve University, Matls. Sci. & Engrg., 10900 Euclid Ave., White Bldg., Cleveland, OH 44106 USA

Thermodynamically stable, ohmic NiSi contacts were formed on n-type 6H-SiC at low temperature (300°C). Specific contact resistance was measured using the circular transmission line model (TLM). The average specific contact resistance of the NiSi/6H-SiC contact was 6.9×10^{-4} Ωcm^2. The contacts were formed through the solid-state reaction of a Ni layer with a low-pressure chemical vapor deposited (LPCVD) fugitive layer of amorphous Si. The resulting microstructure was examined using X-ray diffraction (XRD), conventional transmission electron microscopy (TEM), energy filtering TEM (EFTEM), and x-ray energy dispersive spectroscopy (XEDS). The NiSi layer was continuous, without interfacial voids, and well crystallized. There is no evidence of reaction with the SiC or liberation of carbon at the contact interface. These techniques were coupled with high resolution TEM to characterize the microstructure of the layer and any interfacial changes after annealing at 600°C in air for 300 hours. The specific contact resistance was lowered during the anneal into the 10^{-5} Ωcm^2 range. After the high-temperature aging, no reaction with the SiC occurred. Oxidation of the NiSi layer resulted in the formation of a pure SiO_2 scale, free of NiO. The resulting Si deficiency in the NiSi is accommodated by the precipitation of Ni_2Si. This oxidation behavior may account for the decrease in specific contact resistance.

1:50 PM Student

M2, Comparison and Optimization of Ohmic Contacts on p-Type Silicon Carbide: *Feroz Abdul Mohammad*[1]; Lisa M. Porter[1]; [1]Carnegie Mellon University, Matls. Sci. & Engrg., 5000 Forbes Ave., REH -149, Pittsburgh, PA 15213 USA

The wide band gap of SiC (2.3-3.2 eV depending on the polytype) makes it an ideal material for high-power, high-temperature and high-frequency devices. However, the fabrication of reproducible ohmic contacts with low contact resistances to p-type SiC is a critical problem for reliable performance. The traditional approach is to anneal an Al-based contact (e.g., TiAl) on highly doped SiC at temperatures between 900 and 1150°C. However we have observed Al-Ti contacts to have problems with morphology, oxidation and evaporation resulting from high processing and/or operating temperatures. In this study we report on the notable performance of Pt and Pt-Si based ohmic contacts and their optimization via the development of single-phase contacts. We have found that deposition of 1150 A° of Pt on 850 A° of Si on moderately-

doped p-type ($7x10^{18}$ cm^{-3}) SiC followed by annealing at 1100°C for 5 min. yielded PtSi contacts with an average contact resistance of 1.0 x 10^{-3} Ω cm^2, while incorporation of B in the Si layer can lower the contact resistance to the low 10^{-4} Ω cm^2 range. We expect the average contact resistance of these contacts on high-doped p-type (~1 x 10^{19} cm^{-3}) SiC to decrease to well within the 10^{-5} Ω cm^2 range and will perform these measurements in the near future. In comparison, Al-Ti (70-30 wt%) contacts annealed under the same conditions and deposited on the same SiC substrate yielded ohmic contacts with an average contact resistance of 3.2 X 10^{-3} Ω cm^2. In this presentation we will compare the contact resistance of Pt, Pt-Si and Al-Ti contacts as a function of the compositions and discuss optimization in terms of the morphologies and phases formed. We have found that by optimizing the single-phase PtSi contacts, we can yield more reliable, low resistance contacts with significantly improved stability.

2:10 PM

M3, Catalytic Graphitization and Ohmic Contact Formation on 4H-SiC: *Weijie Lu*[1]; William C. Mitchel[2]; Gerald R. Landis[3]; Tiffany R. Crenshaw[1]; Warren Eugene Collins[1]; [1]Fisk University, Dept. of Physics, 1000 17th Ave. N., Nashville, TN 37208 USA; [2]Air Force Research Laboratory, Matls. & Mfg. Direct., Wright-Patterson AFB, OH 45433 USA; [3]University of Dayton Research Institute, Dayton, OH 45469 USA

In this study, electrical contact properties and graphitic structures of metal/carbon/4H-SiC structures are investigated after annealing. Metals include Ni, Co, Cr, NiCr, Ti, W, Mo, Al, and Au. Ohmic contacts are formed on Ni, Co, Cr, and NiCr, with an interfacial carbon film on 4H-SiC (n-type, C-face, and the doping concentration of 1.8 x 1019cm-3) after annealing in vacuum for two hours at 800°C. On n-type 4H-SiC with Si-face and a doping concentration of 1.6 x 1018cm-3, only Ni/C/SiC and Co/C/SiC exhibit ohmic contact behavior. Raman spectroscopy and SEM are applied to examine the formation of graphitic structures. Ni and Co are well known as excellent graphitization catalysts. Raman spectra show a relationship between the formation of graphitized carbon and ohmic contact formation. The strong Raman bands at 1330, 1585, 2660cm-1, and a shoulder band at 1620cm-1 are formed on Ni/C/SiC, Co/C/SiC, and NiCr/C/SiC after annealing. The bands at 1330 and 1585cm-1 also are formed on Ti/C/SiC and Cr/C/SiC with weak intensities after annealing. No Raman bands in the range from 1000 to 3000cm-1 are detected for the other four samples: Al/C/SiC, Au/C/SiC, W/C/SiC, and Mo/C/SiC after annealing. SEM images show that the reacted morphological features on the annealed metal/carbon/SiC structures can be interpreted by the generally accepted catalytic graphitization mechanisms, which can be explained by the carbon diffusivity and the thermal stability of metal carbides. This study reveals that ohmic contact formation on SiC is related to the formation of graphitic structures. Metals act as graphitization catalysts which accelerate the formation of the nano-size graphitic structures, and better catalysts form better ohmic contacts on SiC.

2:30 PM Student

M4, WSix Schottky Contacts to Both n-SiC and n-GaN: *Jihyun Kim*[1]; S. J. Pearton[3]; G. Y. Chung[4]; C. R. Abernathy[3]; R. D. Briggs[2]; A. G. Baca[2]; F. Ren[1]; [1]University of Florida, Chem. Engrg., Chem. Engrg. Bldg., Gainesville, FL 32611 USA; [2]Sandia National Laboratories, Albuquerque, NM 87185 USA; [3]University of Florida, Matl. Sci. & Engrg., Gainesville, FL 32611 USA; [4]Sterling Semiconductor, Tampa, FL 33619 USA

Wide energy band gap based semiconductor SiC and GaN are suitable high ghigh tempearture applications; including gas sensors, high power electronics, and high frequency devices. One of the requirements for those applications is thermal stability of ohmic and Schottky contacts at high temperature. WSiX and W contacts deposited by sputtering have been used in GaAs technology successfully in self-aligned ion implantations and high temperature activation annealing process, which showed excellent thermal stability up to 900°C. W and WSi were sputtered on n-type SiC and GaN. The as-deposited contacts show evidence of high resistance and recombination-dominated carrier transport from current-voltage characteristics due to ion bombardment damage during the deposition. A post-deposition annealing was used to remove the damage. The annealing temperatures varied from 500°C to 1100°C. For 500°C annealing, a barrier height of 1.15 eV was obtained. The barrier height reduced after annealing above 700°C. The thermal stabilities of W and WSi contacts were compared to that of conventional Ni based Schottky for a range of measurmenet temperature from 25°C to 300°C using hot-chuck. There was no obvious difference of forward and reverse leakage currents at room temperature, however, the forward and reverse leakage currents of W based contacts were orders less that of conventional Ni rectifying contacts at 300°C. The thermal stability of a multiple-stake of metallization of Au/Ti/WSiX Schottky contacts were also studied with Auger Electron Spectroscopy. After 500°C anneals, a trace of Ti diffused to the surface of the metal surface and there is no Au or Ti diffusion through WSi. After 1000°C anneals, the Ti and Au were totally mixed. WSi still behaved as a excellent diffusion barrier, which confirmed that W based Schottky can be used as high temperature Schottky. W and WSi were also deposited on n-type GaN, similar thermally stable gate I-V characteristics as that for SiC were observed.

2:50 PM Student

M5, Low Resistance and Thermally Stable Re/Ti/Au Ohmic Contacts to n-ZnO: *Sang-Ho Kim*[1]; June O. Song[1]; Kyung-Kook Kim[1]; Tae-Yeon Seong[1]; [1]Kwangju Institute of Science and Technology, Dept. of Matls. Sci. & Engrg., 1 Oryong-dong, Puk-gu, Gwangju Korea

Zinc oxide (ZnO) has attracted considerable interest because of its potential for use in short wavelength devices, such as UV light emitting diodes, laser diodes and UV detectors. It has been shown that high contact resistance is one of major obstacles in realizing the long-lifetime operation of optical devices. Thus, in order to realise high-performance ZnO-based optical devices, it is essential to achieve highly reliable ohmic contacts which have both low resistance and thermal stability. Various contact systems have been investigated, including indium tin oxide (ITO), Ti/Au, and indium. However, these schemes suffer from thermal degradation upon annealing at elevated temperatures. Thus, from the viewpoint of device applications, it is important to achieve thermal stability as well as low resistance. In this work, we report on an investigation of the Re/Ti/Au scheme for the formation of thermally stable and low resistance ohmic contacts to n-ZnO:Al (n_d = $3x10^{18}$ cm^{-3}). The as-deposited Re/Ti/Au contact yields a specific contact resistance of $2.1x10^{-5}$ Ωcm^2. However, the electrical property is improved when annealed at temperatures of 300-500°C, producing a specific contact resistance of 10^{-7} Ωcm^2. Atomic force microscopy results show that the surface morphology of the contacts becomes slightly degraded as the temperature increase from room temperature to 500°C. The ohmic behaviour of the Re/Ti/Au contacts is also compared with that of the Ti/Au scheme. X-ray photoemission spectroscopy and Auger electron spectroscopy examinations are made to investigate ohmic formation mechanisms for the Re/Ti/Au contacts.

3:10 PM Break

3:30 PM

M6, Re-Examination of Barrier Heights between Metals and Se-Passivated n-Type Si(100): Shruddha Agarwal[1]; Darshak Udeshi[1]; *Meng Tao*[1]; Nasir Basit[1]; Eduardo Maldonado[1]; Wiley P. Kirk[1]; [1]University of Texas at Arlington, NanoFAB Ctr., Box 19072, Arlington, TX 76019 USA

An energy barrier characterizes the metal-semiconductor interface. Ideally the barrier height is determined by the difference between the metal work function and the semiconductor electron affinity. In reality, the barrier height is determined by the surface states present on the semiconductor surface, and is more or less independent of the metal work function. Surface states result from dangling bonds and strained bonds such as dimer bonds and strained back bonds. In this paper, we report a method to reduce surface states on the Si(100) surface using the valence-mending approach, i.e. a monolayer of selenium. Selenium is a Group VI atom and the structure of the Si(100) surface with a monolayer of selenium resembles that of the Si bulk crystal. With fewer surface states, the barrier height is more dependent on the difference between the metal work function and the Si electron affinity and less dependent on the surface states present on Si. The barrier heights of several metals, which are commonly used in the semiconductor industry, on Se-passivated Si(100) have been determined. Magnesium and titanium showed ohmic behavior on Se-passivated Si(100). The magnesium contacts on Se-passivated Si(100) were found to be thermally stable up to 375°C. Chromium, aluminum, and nickel were Schottky, with barrier heights of 0.25 eV, 0.08 eV, and 0.43 eV, respectively. Except nickel, these values closely resemble the ideal barrier heights, but are significantly different from the decades-old data on barrier heights. For example, the barrier heights of magnesium, titanium, aluminum, and chromium on bare Si(100) were reported to be 0.4 eV, 0.5 eV, 0.72 eV, and 0.61 eV, respectively. The ideal barrier heights of these metals on Si(100) are -0.63 eV, 0.04eV,

-0.01 eV, and 0.21 eV, respectively. Further studies are going on with nickel, and we also plan to investigate cobalt and platinum. The Schottky barrier heights were measured with the activation energy method. These results have implications in making ohmic contacts even on lightly-doped Si, and in enabling n-channel Si Schottky source/drain MOSFETs, a terahertz nanoelectronic device. In conclusion, our results demonstrate that, with the valence-mending approach, we can achieve almost ideal barrier heights between metals and Si(100).

3:50 PM

M7, Ohmic Contacts to n-GaSb and n-GaInAsSb: *Robin K. Huang*[1]; Christine A. Wang[1]; Michael K. Connors[1]; Christopher T. Harris[1]; Daniel A. Shiau[1]; [1]Massachusetts Institute of Technology Lincoln Laboratory, 244 Wood St., Lexington, MA 02420 USA

Low resistance contacts to GaSb-based materials are essential for high efficiency thermophotovoltaic (TPV) devices. Recently, there has been interest in monolithically interconnected module (MIM) TPV devices. For MIM TPV devices, low resistance ohmic contacts as well as a common n-type and p-type metallization are desirable. To date, most of the work performed on low resistivity contacts in this materials system has focused on GaSb as the contact layer. Since the Fermi level is pinned close to the valence band in GaSb, it is more difficult to obtain low resistance ohmic contacts to n-type layers. In this paper, n-GaInAsSb contact layers are investigated as an alternative to the conventional n-GaSb contact layers. Several series of samples with n-type GaInAsSb epilayers and reference n-type GaSb epilayers were grown by OMVPE, both on doped GaSb and on semi-insulating (SI) GaAs substrates. The samples had epilayer thicknesses in the range of 1 to 2 μm. The range of doping concentrations, as measured by the Hall method, ranged from low 10^{17} cm^{-3} to mid 10^{18} cm^{-3}. The transfer length method (TLM), originally proposed by Shockley, was used to determine both contact resistivity and sheet resistivity of mesa-etched samples. The Pd/Ge based metallization, which is a common n-type and p-type ohmic metallization for GaSb, was used to make ohmic contacts to the thin n-type epilayers. The effect of alloy temperature on contact resistivity was studied. It was found that the contact resistivity of the Pd/Ge metallization has a very sharp dependence on alloy temperature, showing a minimum at about 270°C. It was also determined that the sheet resistivity of the material can be influenced by the substrate conductivity, so that SI GaAs substrates, despite the lattice mismatch, are desirable for accurate determination of sheet resistivity. The GaInAsSb epilayers were found to have a slightly lower contact resistivity than that of similarly doped GaSb, which indicates that high quality ohmic contacts can be fabricated directly with the quaternary material. After alloying, contact resistivities as low as approximately $8x10^{-6}$ Ω-cm^2 have been measured for n-type GaInAsSb. Detailed experimental comparisons between contacts to GaSb and GaInAsSb epilayers, as well as applications to devices, will be presented.

4:10 PM Student

M8, Interfacial Reactions of Mn Thin Films on GaAs (100): *J. L. Hilton*[1]; B. D. Schultz[1]; C. J. Palmstrøm[1]; [1]University of Minnesota, Chem. Engrg. & Matls. Sci., Minneapolis, MN 55455 USA

Mn-based ferromagnetic materials have been extensively used for spin injecting contacts to GaAs. A number of Mn-based compounds have been grown epitaxially on GaAs, including ferromagnetic metals such as MnAs[1] and MnGa,[2] diluted magnetic semiconductors such as $Ga_{1-x}Mn_xAs$,[3] and digital alloys such as (Ga,Mn)As.[4] However, solid phase reactions between Mn thin films and GaAs have yet to be studied. This study examines the interfacial reactions between Mn thin films deposited in-situ on MBE-grown GaAs (100) epilayers using x-ray diffraction (XRD) and Rutherford backscattering spectrometry (RBS). Thick Mn films (>500Å) with 25Å Al caps were grown by molecular beam epitaxy at 25°C, and ex-situ post-growth anneals were performed in forming gas at temperatures of 200°C, 300°C, 400°C, and 500°C for times ranging from one to eight hours. Prior to annealing, the Mn films on GaAs appear from XRD and RHEED to be amorphous, and RBS indicates that no strong interfacial reactions occur during growth. After annealing for one hour at 200°C, small XRD diffraction peaks corresponding to a tetragonal Mn_2As-like phase and a tetragonal MnGa-like phase are observed. The intensities of these diffraction peaks increase for samples annealed for one hour at 300°C, and are found to increase further for samples annealed at 400°C. RBS data at both normal and grazing angles indicate that significant Mn-Ga-As reactions occur during anneals in excess of 200°C. The RBS and XRD data suggest that the initial reactions at low temperatures result in the formation of a ternary phase, which is also present after higher temperature anneals. Unreacted Mn remains on the surface of samples annealed at 300°C, but is no longer present in samples annealed at 400°C or higher. RBS spectra for samples annealed at 500°C suggest that the stoichiometry of the surface layers is no longer maintained and that arsenic dissociated from the surface during the anneals. Anneals in excess of one hour result in only minor variations of the XRD and RBS spectra for all temperatures below 500°C, indicating that the reactions may be self-limiting. RBS, XRD, and transmission electron microscopy (TEM) results on the nature and behavior of the reactions between Mn, Ga, and As at the metal-semiconductor interface will be presented. This research was supported in part by the ONR N/N00014-1-0233, DARPA N/N00014-99-1-1005, DARPA N/N00014-01-1-0830, and NSF/DMR-9819659. [1]M. Tanaka et. al., J. Vac. Sci. Technol. B 12, 1091 (1993). [2]M. Tanaka et. al., Appl. Phys. Lett. 62, 1565 (1993). [3]H. Ohno et. al., Appl. Phys. Lett. 69, 363 (1996). [4]R. K. Kawakami et. al., Appl. Phys. Lett. 77, 2379 (2000).

4:30 PM

M9, II-VI Ultra-Violet Detectors: Issues of Schottky Metal Contacts: Zhen Guo[1]; Wing Yan Law[1]; *Iam Keong Sou*[1]; [1]The Hong Kong University of Science and Technology, Dept. of Physics, Clear Water Bay, Kowloon, Hong Kong China

Ultraviolet (UV) photodetectors with high responsivities for wavelengths shorter than 400nm are very important for applications that require detection of UV radiation against strong visible or infrared backgrounds. Recently, we reported the high performance of two novel II-VI systems for UV radiation detection: ZnSSe-based detectors[1] and ZnMgS-based detectors,[2] in which a thin pure Au layer on top was used to form a Schottky contact to the active semiconductor materials. In this work, we will present the systematic studies on the dependence of the photoresponse of ZnSSe photodetectors on the use of different metals and the different means of metal deposition. Ni and Cr were expected to be a good replacement for pure Au as a Schottky contact for their good adhesive nature. We have farbricated and studied both Au/Ni and Au/Cr bilayer Schottky contacts in this work. However, the results of our studies show that the photoresponse curves of these devices suffer much lower visible rejection power as compared to devices with pure Au as Schottky contacts. With the help of the secondary ion mass spectroscopy technique, we have identified a serious diffusion of these metals into II-VI materials, as well as their ease of oxidization during deposition. Furthermore, we also detected the metal alloying in the Au/Cr contact. We have also studied the difference in photoresponse for the devices with pure Au as Schottky metal that was prepared by either thermal evaporation or sputtering technique. It was found that the devices with Schottky metal prepared by the sputtering technique shows a relatively more gradual turn on and a lower UV response in their photoresponse curves as compared to that of the devices with Schottky metal prepared by thermal evaporation. It was also found that higher the sputtering rate was used, worse the photoresponse performance was. This is believed to be related to the degree of damaging on the interface neighborhood caused by the highly energetic particles impacting the sample surface during the sputtering process. The built-in voltage, which reflects the Schottky barrier height, of the devices was measured. It was found that the reduction of the built-in voltage as compared to the ideal value is closely correlated to the imperfection of the Schottky contact described above. But the lowering of the built-in voltage itself cannot fully explain the observed photoresponse characteristics of the devices. A model was proposed in this work to take into account the defect states generated through either metal diffusion, alloying or sputtering damage. It is believed that these defect states significantly affect the photoresponse of the UV detectors through direct photo-excitation and assistant tunneling mechanisms in the visible spectral region. Acknowledgement: The work described in this abstract was substantially supported by a grant from the Research Grants Council of the Hong Kong Special Administrative Region, China (Project No. HKUST6149/99P). [1]I. K. Sou, Z. H. Ma, G. K.L. Wong, Appl. Phys. Lett. 75, 3707 (1999). [2]I. K. Sou, M. C.W. Wu, T. Sun, K. S. Wong, G. K.L. Wong, Appl. Phys. Lett. 78, 1811-13 (2001).

4:50 PM M10, Late News

Session N: Materials Integration: Wafer Bonding and Alternative Substrates - II

Wednesday PM Room: Auditorium
June 25, 2003 Location: Olpin Union Building

Session Chairs: Karl Hobart, Naval Research Laboratory, Washington, DC 20375 USA; Matthew Seaford, RF Micro Devices, Greensboro, NC 27409 USA

1:30 PM Student

N1, Scanning Photocurrent Measurements for the Nondestructive Evaluation of Waferbonded Interfaces: *Phil Mages*[1]; Justin Bickford[2]; L. S. Yu[2]; D. Qiao[2]; T. Suni[3]; K. Henttinen[3]; I. Suni[3]; S. S. Lau[2]; P. K.L. Yu[2]; [1]University of California, San Diego, Matls. Sci./ECE, MC 0418, 9500 Gilman Dr., La Jolla, CA 92093-0418 USA; [2]University of California, San Diego, ECE, MC 0407, 9500 Gilman Dr., La Jolla, CA 92093-0407 USA; [3]VTT Centre for Microelectronics, PO Box 1208, 02044 VTT Finland

Unlike bonding techniques using reactive interlayers or surface oxides, hydrophobically bonded samples allow for the creation of conductive bonded interfaces, which are often regarded as a being perfect enough interface to have little effect on the devices made from such material. This advantage of the hydrophobically bonded interface, however, carries with it also the need for evaluation of the electronic properties of the interface. Though techniques such as infrared transmission photography and Scanning Acoustic Microscopy (SAM) allow for the non-destructive, large-scale mapping of physical features, such as interfacial bubbles, these techniques give no information about the electronic behavior of the interface. To obtain this information wafers must often be diced and processed so as to isolate different sections of the wafer for conventional current-voltage analysis. Since larger scale production would benefit from the ability to scan the wafers without such processing, we have developed a promising technique for probing the electronic properties of the interface using a small light beam scanned across the whole area of the wafers. The basic technique consists of monitoring the steady-state photocurrent generated locally as the wavelength of the monochromatic light beam is varied at each position on the unbiased sample. Using this method we have reported the ability to detect different interface behavior in samples of p-type Si initially bonded hydrophobically in normal room air, as compared to identical samples bonded in a dry nitrogen ambient.[1] Our initial simplified model describes the variation of photocurrent in terms of the change in photon penetration depth vs. wavelength and interfacial band bending due to the presence of charged interface states. Considering the variation of recombination velocity at the interface due to differing interface state densities, we present a deeper interpretation that is more directly related to localized states likely produced during the bonding process. Using these models we discuss photocurrent data and maps collected on samples having different bonding histories, bias conditions and background photon densities. Besides showing the obvious advantages of being able to differentiate between two interfaces which appear identical under SAM, we present data showing how the photocurrent vs. wavelength scans using different bias/illumination conditions allow for more detailed investigation of the interface state populations at the interface. Variations of such data over the area of bonded wafers having slight interface inhomogeneities are displayed. [1]L. S. Yu, P. Mages et. al., Applied Physics Letters, To be published 17 February 2003.

1:50 PM Student

N2, Integration of Lattice-Mismatched Semiconductors with Si using SiO_2 CMP Layers and Wafer Bonding Ge/GeSi/Si Virtual Substrates: *Arthur J. Pitera*[1]; Gianni Taraschi[1]; Minjoo L. Lee[1]; Chris W. Leitz[2]; Eugene A. Fitzgerald[3]; [1]Massachusetts Institute of Technology, Dept. of Matls. Sci. & Engrg., 77 Massachusetts Ave., Rm. 13-4154, Cambridge, MA 02139 USA; [2]AmberWave Systems Corporation, 13 Garabedian Dr., Salem, NH 03079 USA; [3]Massachusetts Institute of Technology, Dept. of Matls. Sci. & Engrg., 77 Massachusetts Ave., Rm. 13-5153, Cambridge, MA 02139 USA

High-quality Ge and III-V semiconductors fabricated on Si can significantly improve the functionality of CMOS electronics while providing the economic benefits of monolithic device fabrication on large diameter wafers. The Ge/GeSi/Si virtual substrate is a versatile platform for such integration of low defect density Ge and III-V semiconductors with Si. However, in order to make this approach practical, the thick graded buffer between the Si substrate and integrated layer must be removed. Wafer bonding virtual substrates to Si provides a solution for fabrication of lattice-mismatched layers in close proximity to the Si substrate without the limitation of small Ge or III-V wafers that are used in traditional bulk wafer bonding. Until recently, the virtual substrate bonding approach has been limited by the ability to CMP Ge virtual substrates. To circumvent this problem, we have planarized our virtual substrates through a low-temperature-oxide (LTO) CMP layer, which could be readily CMPed prior to wafer bonding. The CMP layer also serves to protect the Ge surface during post-CMP and pre-bond cleaning. Use of oxide CMP layers results in a Ge or III-V/oxide/Si structure which could also be applied to Ge-on-insulator (GOI) electronics. Furthermore, by depositing the insulating layer on the seed wafer, the bond interface is isolated far away from the device region thereby minimizing carrier scattering. Since our layers are transferred using hydrogen-induced layer exfoliation, the surface of the transferred Ge film suffers mechanical damage during the process. To remove this damaged region we have developed a novel technique to strip the top layer of Ge using chemical etching and a strained Ge_xSi_{1-x} etch-stop layer. This approach provides extremely precise control of the transferred layer thickness allowing the possibility for future fabrication of ultra-thin GOI structures. We have determined that the thermal budget of buried $Ge_{0.6}Si_{0.4}$ etch-stop layers have a thermal budget of 650°C while maintaining a very high peroxide etch selectivity of >100:1 relative to Ge. In addition, densification of LTO on our Ge virtual substrates also has a temperature constraint of <650°C, therefore our film-transfer process has been tailored to stay within these thermal limitations. Current progress in device fabrication on these substrates will also be presented.

2:10 PM Student

N3, Stress Balance of Si/SiGe and SiO_2/SiGe on Compliant Substrates: *Haizhou Yin*[1]; K. D. Hobart[2]; S. R. Shieh[3]; T. S. Duffy[3]; F. J. Kub[2]; J. C. Sturm[1]; [1]Princeton University, Dept. of Electl. Engrg., E-Quad, Olden St., Princeton, NJ 08540 USA; [2]Naval Research Laboratory, Washington, DC 20375 USA; [3]Princeton University, Dept. of Geoscis., Princeton, NJ 08544 USA

There has been increasing interest in compliant substrates for integration of heterogeneous epitaxial materials. However, the compliancy mechanism is not yet well understood. In this talk, we report stress balance observed in epitaxial Si/SiGe bi-layers on a compliant borophosphorosilicate glass (BPSG). Such stress balance in epitaxial multilayers on a compliant substrate has not been previously observed. This work indicates that the compliancy, in this case, originates from the viscous flow of the BPSG, instead of defect formation as observed in graded SiGe buffers. Previous work has focused on a single SiGe layer on BPSG.[1, 2] Here we first verify a coherent interface between SiGe and Si films on BPSG during relaxation process. We then successfully predict strains in Si/SiGe and SiO_2/SiGe stacks upon equilibrium based on stress balance between the layers. These results show that defects do not play a role in the relaxation of SiGe on BPSG. A wafer with 30 nm fully strained $Si_{0.7}Ge_{0.3}$ relaxed 25 nm Si/200 nm BPSG was fabricated by wafer bonding and Smart-cut as in ref. 1. Square SiGe islands of edge length 30 μm were then patterned. Upon annealing to reduce the viscosity of BPSG and thus remove the mechanical constraint from the substrate, the compressively strained SiGe layer expands to lessen the strain and the Si layer is stretched to become tensile. The observation of the same increase in the strain of both layers clearly implies an absence of slippage or misfit dislocations between the Si and SiGe layers. In addition, the final strains of the annealed samples confirm equilibrium stress balance between the layers. The stress balance theory is further verified by examining the final strains of the SiGe and Si films for various Si layer thickness. Lateral shrinkage of SiGe/Si islands was also examined during the stress balance process. A 30 μm SiGe island on BPSG was initially fully relaxed by lateral expansion, followed by a deposition of a commensurately strained Si layer by chemical vapor deposition (CVD. After annealing to reach

equilibrium, stress balance again accurately predicts the final strains. Stress balance with an amorphous oxide layer was observed. A SiO_2 cap was deposited on a fully strained SiGe layer on BPSG by plasmas-enhanced CVD. The SiO_2/SiGe stack was patterned to 30 µm islands and annealed to reach an equilibrium state. Good agreement between experimental data and stress balance theory is again observed, with the elastic constant of oxide as the single fitting parameter. Such oxide caps are of direct technological interest because oxide caps stiffen the SiGe layers and prevent film buckling.[3] This reduces the amount of strain relaxation of the SiGe layers. However, this drawback can be overcome by multiple cycles of cap thinning and further annealing. Stress balance of Si/SiGe and SiO_2/SiGe on BPSG shows that defect formation does not play a role in the SiGe relaxation on BPSG. Therefore this can be used to produce high quality relaxed SiGe layers. This work is supported by DARPA and ARO. [1]K.D. Hobart, et. al. Journal of Electronic Materials, 29, 897 (2000). [2]H. Yin, et. al. Journal of Applied Physics, 91, 9716 (2002). [3]H. Yin, et. al. MRS Spring Meeting, San Francisco, CA (2002).

2:30 PM Student

N4, Adhesive Wafer Bonding of GaAs on Si and its Effect of SeS2 Treatments on the Structural Modification Changes of n-GaAs(100) Substrate: *Premchander Perumal*[1]; *Krishnan Baskar*[1]; Arivuoli Dhakshnamoorthy[2]; [1]Anna University, Crystal Growth Ctr., Chennai, Tamil Nadu 600025 India; [2]Anna University, School of Electrical and Electronics Engineering, Anna University, Guindy campus, Chennai, Tamil Nadu 600025 India

Gallium Arsenide treated with chalcogenide has attracted recently in Opto-electronics and photovoltaic applications. In the present study we report the characteristics of GaAs treated with Selenium(IV)sulfide. LEC grown n-GaAs(100) doped with silicon has been used as a substrate. The carrier concentration was 1.1x1018 cm-3. The substrate was ultrasonically cleaned with Tricholoethylene(TCE), Acetone, Methanol and deionised water. It was chemically etched in H2SO4: H2O: H2O2 (4:1:1) solution and then in HCl for one minute. Substrates were immersed into SeS2/CS2 chemical solution bath with specific timings of 5s, 10s, 15s respectively. All the passivated samples were annealed at 350°C. The group-VI elements, such as S and Se treatments have distinct advantages in wafer bonding and passivation technologies. Recent reports show that Se can be easily incorporated in GaAs by making use of dangling bonds on the surface and result in Ga-Se related phases. These stable phases were analyzed by X-ray diffraction (XRD), Photoluminescence (PL) and Scanning Electron Microscopy(SEM) measurements and the results will be presented in detail. The SeS2 captured layers on GaAs can reduce the disorder induced interface states when bonded with other substrates such as silicon. The low temperature wafer bonded compliant wafers were confirmed by SEM.

2:50 PM N5, Late News

3:10 PM Break

3:30 PM Student

N6, Wafer-Fused nAlGaAs-pGaAs-nGaN Heterojunction Bipolar Transistors: *Sarah Marie Estrada*[1]; Huili Xing[2]; Andrew Huntington[1]; Andreas Stonas[2]; Larry Coldren[2]; Steven DenBaars[1]; Umesh Mishra[2]; Evelyn Hu[2]; [1]University of California, Santa Barbara, Matls. Dept., Santa Barbara, CA 93106-5050 USA; [2]University of California, Santa Barbara, Electl. & Compu. Engrg. Dept., Santa Barbara, CA 93106 USA

Recently we reported the first AlGaAs-GaAs-GaN heterojunction bipolar transistor (HBT), a device that might combine the high-breakdown voltage of an nGaN collector with the high mobility of a more technologically mature AlGaAs-GaAs emitter-base. Because the high degree of lattice mismatch between GaAs (lattice constant of 5.65A) and GaN (3.19A) precludes an all-epitaxial formation of this device, we formed the GaAs-GaN heterostructure via wafer fusion, also called direct wafer bonding. Our initial device was formed by fusion at a high temperature (750°C) and demonstrated low output current (~100A/cm2) and low common-emitter current gain (0.5).[1] This talk will describe a systematic variation of fusion temperature (550-750°C) in the formation of the HBT, and will reveal the correlation between fusion temperature, base-collector leakage, and emitter-base degradation. With reduced fusion temperature, devices demonstrate improvements in leakage, output current (~1kA/cm2), and common-emitter current gain (>1). The AlGaAs-GaAs emitter-base was grown by molecular beam epitaxy. A sacrificial layer (0.5um) of undoped AlAs was grown on (100) n+GaAs substrate, followed by a contact layer (0.1um n+GaAs, 1e19 cm-3 Si), the device emitter (0.18um graded nAlGaAs, 5e17 cm-3 Si), and finally the device base (0.15um p+GaAs, 1e19 cm-3 C). Carbon, rather than beryllium, was chosen as the p-type dopant in order to minimize dopant diffusion during the high-temperature fusion procedure. The uid-GaN collector (nominal 5e16 cm-3 Si) was grown by metal-organic chemical vapor deposition on c-plane (0001) sapphire. The GaN and GaAs structures were fused at systematically varied temperatures (550-750°C) for one hour under a uniaxial pressure of 2 MPa in a nitrogen ambient. After removal of the GaAs substrate and sacrificial AlAs, emitter (1e-5 cm2) and base mesas (5e-5 cm2) were defined. Emitter contacts were NiAuGe, base contacts were ZnAu, and collector contacts were AlAu. Gummel plots and common-emitter I-V characteristics were measured. Additionally, we are studying HBT structures with a reduced base thickness of 100 nm and a setback layer of two different thicknesses (20 or 50 nm). By introducing a GaAs base-collector setback layer, we hope to shift the fused GaAs-GaN interface slightly into the collector, decreasing the barrier prior to the possible spike at the fused heterojunction. Also, by utilizing lower fusion temperatures, the device is less susceptible to dopant diffusion, which should allow the use of a thinner base. [1]Sarah Estrada, Huili Xing, Andreas Stonas, Andrew Huntington, Umesh Mishra, Steven DenBaars, Larry Coldren, and Evelyn Hu, Wafer-fused AlGaAs/GaAs/GaN heterojunction bipolar transistor, Applied Physics Letters 82 (5), 820-2 (2003).

3:50 PM

N7, Wafer-Bonding and Epitaxial Transfer of GaInAsSb/GaSb to GaAs Substrates for Monolithic Series Interconnection of Thermophotovoltaic Cells: *Christine A. Wang*[1]; D. A. Shiau[1]; P. G. Murphy[1]; P. W. O'Brien[1]; M. K. Connors[1]; R. K. Huang[1]; A. C. Anderson[1]; D. Donetsky[2]; S. Anikeev[2]; G. Belenky[2]; D. M. Depoy[3]; G. Nichols[3]; [1]Massachusetts Institute of Technology Lincoln Laboratory, 244 Wood St., Lexington, MA 02420 USA; [2]State University of New York, Stony Brook, NY 11794 USA; [3]Lockheed Martin Corporation, Schenectady, NY 12301 USA

Thermophotovoltaic (TPV) devices are of interest for power generation from thermal radiation, and both lattice-matched GaInAsSb/GaSb and lattice-mismatched InGaAs/InP epitaxial materials are being developed for 0.5- to 0.6-eV TPV cells. In order to build open-circuit voltage and reduce I2R losses, it is desirable to monolithically interconnect the TPV cells in series. Such interconnection requires electrical isolation of the epitaxial device layers from the substrate, which can easily be achieved for InP materials by epitaxial growth on a semi-insulating (SI) substrate. However, the small bandgap (0.72 eV) of GaSb precludes the attainment of SI GaSb substrates. Therefore, alternative approaches for electrical isolation must be developed. This work reports the wafer bonding and epitaxial transfer of GaInAsSb/GaSb TPV epilayer structures to SI GaAs handle wafers. GaInAsSb/GaSb TPV structures with a lattice-matched InAsSb etch-stop layer were grown by organometallic vapor phase epitaxy. The epitaxial layers were bonded to SI GaAs substrates using SiOx/Ti/Au. This dielectric/metal reflector serves as both the bonding layer and as an internal reflector, which can enhance the performance of the TPV cell and provide spectral control of below bandgap photons. The bonding layer was designed to provide high reflectivity while minimizing internal stress in the final structure. To complete the epitaxial transfer, the GaSb substrate was either chemically or mechanically thinned to remove over 80% of the GaSb substrate, and then the remaining GaSb and InAsSb etch-stop layer were removed by selective chemical etching. Characterization of the wafer-bonded and transferred GaInAsSb/GaSb epilayers by high-resolution x-ray diffraction indicates minimal residual stress. Furthermore, photoluminescence (PL) and time-resolved PL measurements show enhancement in optical efficiency and minority carrier lifetime. Finally, wafer-bonded GaInAsSb/GaSb/GaAs TPV cells were fabricated and monolithically interconnected in series. Nearly linear voltage building is reported. At a short-current density of 0.4 A/cm2, the open-circuit voltage for a single TPV device is 0.2 V, compared to 0.37 and 1.8 V for 2- and 10-junction devices, respectively. This paper will discuss the design, growth, fabrication, characterization, and performance of wafer-bonded GaInAsSb/GaSb/GaAs TPV devices.

4:10 PM Student

N8, III-V on Insulator Composite Substrates: *Sumiko Lynn Hayashi*[1]; Rajinder Singh Sandhu[2]; David Bruno[1]; Mike Wojtowicz[2]; Mark S. Goorsky[1]; [1]University of California, Los Angeles, Dept. Matls. Sci. & Engrg., 2521 Boelter Hall, 420 Westwood Plaza, Los Angeles, CA 90095

USA; [2]Northrop Grumman, Space Tech., 1 Space Park Dr., Redondo Beach, CA 90278 USA

To demonstrate the feasibility of creating III-V on insulator structures for subsequent epitaxial growth, an InP template layer was bonded to a semi-insulating GaAs substrate using intermediate silicon nitride layers. InP on GaAs structures offer a test case that can be compared directly to epitaxial growth on standard InP substrates. The pair also provides insight into bonding materials that exhibit different thermal expansion coefficients. An InP wafer is bonded to a GaAs wafer, where upon a thin InP layer is split off using hydrogen implantation. The implantation damage and surface roughness of the transferred InP layer is then removed with chemical mechanical polishing (CMP). The transferred InP layer may then be used as a template for epitaxial growth. This layer's quality is crucial for optimum device performance and its suitability for this application is investigated in this study. The InP layer after transfer to the GaAs substrate showed no strain as determined by x-ray reciprocal space mapping. The crystalline quality of the transferred InP layer was examined with triple axis x-ray diffraction (TAD) and double crystal x-ray topography. A TAD FWHM of 66 arcseconds for an InP layer that was exfoliated using hydrogen implantation shows that some residual damage remains, most likely due to the ion implantation process. Key parameters leading to a high quality transfer layer include bond quality, hydrogen implantation parameters, and CMP chemistry. Out-gassed SiN bonding layers were found to produce strong, uniform bonds. The layer transfer was accomplished by implanting a dose of 5x1016 H2+/cm2 at 150 keV. Double axis diffraction measurements, in correlation with TEM, were found to be a useful tool for understanding layer exfoliation kinetics. It was found that a lower temperature bond strengthening anneal (150°C) actually accelerates layer transfer at higher temperatures (300°C). Although material degradation of the InP layer occurred at annealing temperatures of 500°C, the bond interface was found to be stable by TEM. This material degradation was identified by double crystal x-ray topography as a cross-hatch dislocation array in the InP layer due to the difference in thermal expansion of InP and GaAs. Finally, planarization of the InP surface must be achieved with minimal subsurface damage, as determined in this study by triple axis x-ray diffraction. A CMP slurry of sodium hypochlorite and citric acid without abrasive particles produced smooth surfaces (RMS roughness = 0.2 nm) with minimal subsurface damage. The resultant structure may be used for subsequent device growth, and the process may be applied to other III-V on insulator structures.

4:30 PM Student

N9, $IN_{0.4}GaAs/IN_{0.2}GaAs$ Multi-Quantum-Wells Grown on Twist Bonded GaAs Compliant Substrates: *Yuanming Deng*[1]; P. Daniel Dapkus[1]; [1]University of Southern California, Dept. of Electl. Engrg. - Electrophysics, 3651 USC Watt Way, VHE309, Los Angeles, CA 90089 USA

Material growth on compliant substrates (CS) may permit integration of lattice-mismatched materials on commercially important substrates. In this paper, we report studies of the growth of InGaAs MQW structures with thick InGaAs buffer layers on thin GaAs CS. Atomic force microscopy, X-ray and PL were used to characterize the material. The compliant substrate was prepared by growing 300nm GaAs buffer layers, 100nm $Al_{0.8}GaAs$ etch stop layers and 10 or 20nm GaAs CS layers on GaAs (100) N+ wafers. The structure was turned over and bonded to GaAs (100) holding wafers with various twist angles from 0° to 58°. The wafer bonding was done in a hydrogen ambient at 500°C for 30 minutes. Pressure was applied to the wafers during bonding. After bonding, the top GaAs substrate was removed by mechanical polishing and spray etching. The $Al_{0.8}GaAs$ etch stop layer was removed in HCl solution right before the growth. A 300nm $In_{0.2}GaAs$ layer was grown on the compliant substrates as a buffer layer followed by 5 pairs of 8nm $In_{0.4}GaAs$/30nm $In_{0.2}GaAs$ QWs. The growth was done by LP-MOCVD at 600°C. The crystal orientation of the epi-layer on the compliant substrate was investigated by asymmetric X-ray diffraction. When the CS layer is a nominal 10nm thick GaAs layer, the crystal orientation is the same as the holding substrate. As the thickness of GaAs CS layer is increased to a nominal 20nm, the crystal orientation is same as the CS layer. The surface cross-hatch pattern observed by AFM agrees with this observation. The nominal CS thicknesses indicated above are the thicknesses before the wafer bonding process. A surface oxidization layer was removed before the bonding and before the growth sacrificing 2~3nm GaAs from the CS layer each time. As the result, we expect only 3~6nm of the GaAs was left in the case of 10nm GaAs CS. The crystal orientation suggests when the GaAs bonding layer is very thin, it may even realign to the holding substrate during bonding. Although the relaxation of the InGaAs structures on different CS layers observed by X-ray, were different from the reference sample (the same structure grown on the GaAs epi-ready wafer), there was no improvement in the photoluminescence (PL). We will also report on the use of a CS formed by bonding 10nm and 20nm GaAs CS layers onto a 300nm $In_{0.2}GaAs$ buffer layer grown on GaAs and onto a heavily ion implanted GaAs wafer. In this study, the best PL intensity was observed from the sample grown on the 10nm GaAs CS layer bonded to 300nm InGaAs. The PL intensity was 5 times higher than the reference sample. We will discuss our understanding of these observations.

4:50 PM

N10, Fabrication of AlN-Silicon-on-Insulator Structure and Computer Simulation of Self-Heating Effect: *Ming Zhu*[1]; Zhenghua An[1]; Qing Lin[2]; Zhengxuan Zhang[2]; Ricky K.Y. Fu[1]; Paul K. Chu[1]; Chenglu Lin[2]; [1]City University of Hong Kong, Dept. of Physics & Matls. Sci., Tat Chee Ave., Kowloon Hong Kong; [2]Chinese Academy of Sciences, Shanghai Inst. of Microsys. & Info. Tech., State Key Lab. of Functl. Matls. for Informatics, 865 Changning Rd., Shanghai 200050 China

Devices fabricated in silicon-on-insulator (SOI) are prone to inherent self-heating that limits the applicability of SOI materials in electronics where high power dissipation is expected. This is a consequence of the low thermal conductivity of the buried oxide layer in SOI devices. In this work, aluminum nitride (AlN) as a potential candidate for buried insulator material in SOI-structure was investigated to take advantage of its attractive properties including excellent thermal conductivity, high thermal stability, high electrical resistance, and coefficient of thermal expansion close to that of silicon. In our experiments, AlN films were deposited on 100mm silicon wafers by ion beam enhanced deposition (IBED) utilizing electron beam evaporation of Al and simultaneous bombardment by a nitrogen ion beam. The wafers were implanted with 20 kV N2+ and N+ (60% N2+, 40% N+) with an ion flux density of 25 μA/cm2. The evaporation rate of Al was adjusted between 0.5 and 5 Å/s and a base pressure of 1×10-3 Pa was established prior to deposition. The wafers were maintained at 700°C during implantation. The synthesized films were characterized by x-ray photoelectron spectroscopy (XPS), spreading resistance profiling (SRP), and atomic force microscopy (AFM). Experimental results indicated that AlN films with the best quality were fabricated at an Al evaporation rate of 0.5 Å/s, as manifested by the excellent dielectric property and a smoother surface with an RMS roughness value of 0.13 nm. The deposited film was subsequently bonded directly to a silicon wafer that had been implanted with hydrogen using a thermal treatment at 400-600°C. During this process, the implanted wafer split into two parts giving rise to an SOI structure and a donor wafer. Afterward the wafer cleavage and bonding, high-temperature annealing at 1100°C was performed for 1h to form the SOI structure composed of the AlN thin film as the buried layer. Cross-sectional TEM gave direct evidence of the formation of SOI structure. Spreading resistance profiling showed three distinct layers in the SOI structure including the top silicon layer, buried AlN, and substrate. Our experiments show the success of the thermal ion-cut process to form SOI with AlN as the buried dielectric. Using a two-dimensional device simulation program Medici (TMA, 2000), the high-temperature operation of SOI MOSFETs fabricated in AlN-SOI was investigated. A detailed electro-thermal transport model was used in the simulation. The performance of AlN-based SOI with that of SiO2-based SOI and conventional MOSFETs was also compared and it was found that the self-heating penalty of SOI could indeed be reduced using AlN-SOI.

Session O: Nitrides: Defect Reduction and Epitaxy

Thursday AM Room: Ballroom Center
June 26, 2003 Location: Olpin Union Building

Session Chairs: Russell Dupuis, University of Texas, Microelect. Rsch. Ctr., Austin, TX 78712-1100 USA; Christian Wetzel, Uniroyal Optoelectronics, Tampa, FL 33619 USA

8:20 AM Student

O1, Nanometer Scale Lateral Epitaxy Overgrowth of GaN Employing Block Copolymer Lithography: *R. R. Li*[1]; Dawei Ren[1]; Xingang Zhang[2]; Paul D. Dapkus[3]; M. E. Thompson[4]; C. K. Harrison[5]; P. M. Chaikin[6]; R. A. Register[7]; D. H. Adamson[8]; [1]University of Southern California, Matls. Sci., 3651 USC Watt Way, VHE 309, Los Angeles, CA 90089 USA; [2]Luminent Inc., 20550 Nordhoff St., Chatworth, CA 91311 USA; [3]University of Southern California, EE-Electrophysics Dept., 3651 USC Watt Way, VHE 314, Los Angeles, CA 90089 USA; [4]University of Southern California, Chmst. Dept., Los Angeles, CA 90089 USA; [5]National Institute of Standard and Technology, Polymer Div., Gaithersburg, MD 20899 USA; [6]Princeton University, Physics Dept., Princeton, NJ 08544 USA; [7]Princeton University, Chem. Engrg. Dept., Princeton, NJ 08544 USA; [8]Princeton Materials Institute, Princeton, NJ 08544 USA

Lateral epitaxy overgrowth (LEO) of GaN - to reduce the defect density of the GaN films in the regions where lateral epitaxy occurs over a dielectric mask - has been studied extensively for LEO patterns in the micron scale. Materials grown at the coalescence fronts are usually defective due to the large amount of strain built in during the growth of the thick GaN layers that are necessary for to achieve coalescence in micron-scale LEO. In this paper, we demonstrate GaN LEO at the nanometer scale, where smooth coalescence was obtained within 100nm of material growth. SiNx films deposited on MOCVD grown GaN were patterned with a hexagonally ordered array of nanoscale holes using block copolymer lithography. Selective nucleation of GaN inside the nanoscale holes was carried out to obtain arrays of GaN nanostructures, 20nm in diameter and 40nm center-to-center spacing. The selective area growth was then followed by nanoscale lateral epitaxy overgrowth (nano-LEO). The substrate temperature had to be lowered at the initial stage of nano-LEO in order to facilitate uniform growth of the nanostructures, after which it was increased to 1050°C to enhance lateral growth rate and realize the final coalescence. Only 100 nm of growth was required to achieve coalescence of the GaN surface, resulting in a smooth GaN surface. Defect reduction was confirmed by cross-sectional transmission electron microscopy (X-TEM) study and found to be around 75% by atomic force microscopy (AFM) measurement. The surface smoothness of the resultant GaN film was found to be of a RMS ~ 1nm for a 1µm x 1µm area scan using AFM, which is superior to a typical GaN buffer surface with a RMS of ~ 3nm for 1µmx1µm scan. Two step nano-LEO- two nano-LEO processes with one following the other- was also demonstrated as a potential way to further reduce the GaN defect density. Block copolymer lithography and MOCVD growth are batch processes so that nano-LEO is a promising approach to producing high quality, uniform, thin GaN film with sub-micron thickness across a standard 3 wafer surface.

8:40 AM

O2, Developing Cantilever Epitaxy of GaN for Advanced Devices: *David M. Follstaedt*[1]; Daniel D. Koleske[2]; Christine C. Mitchell[2]; Nancy A. Missert[3]; Paula P. Provencio[4]; Andrew A. Allerman[2]; [1]Sandia National Laboratories, Physl. & Chem. Scis. Ctr., MS 1056, Albuquerque, NM 87185-1056 USA; [2]Sandia National Laboratories, Physl. & Chem. Scis. Ctr., MS 0601, Albuquerque, NM 87185-1056 USA; [3]Sandia National Laboratories, Physl. & Chem. Scis. Ctr., MS 1415, Albquerque, NM 87185-1415 USA; [4]Sandia National Laboratories, Physl. & Chem. Scis. Ctr., MS 1421, Albuquerque, NM 87185-1421 USA

Cantilever epitaxy (CE) is being developed by our group to produce GaN on sapphire with low dislocation densities as needed for improved devices. The basic mechanism, seeding growth on sapphire mesas extending along [1-100] and growing cantilevers laterally until they coalesce, has been modified by introducing an initial growth step at 950°C. This step grows GaN over the mesa with two {11-22} facets on each side that form the shape of a house "gable". The facets turn threading dislocations from vertical to horizontal in order to reduce their density above the mesas. In addition, a GaN nucleation procedure that produces inherently lower densities of threading dislocations has been implemented. These techniques have allowed us to achieve densities as low as 2-3x10^7/cm^2 averaged across extended areas of GaN on sapphire, as determined with AFM, TEM and cathodoluminescence (CL). This density is about two orders of magnitude below that of conventional planar growths; these improvements suggest that locating wide-area devices across both cantilever and mesa regions will eventually be possible. However, a new defect was found in GaN grown with the modified techniques: cracks at cantilever coalescences with associated arrays of lateral dislocations. We have labeled these isolated regions "dark-block defects" because they are non-radiative and appear as dark rectangles in CL images. Characterization with SEM, AFM and TEM of cantilever material in defect areas indicates that they result from misorientations between the two cantilever sections being brought together. Recently, we have been able to grow material that does not have dark-block defects. Examination of many CE growths, both partial (uncoalesced) and fully coalesced, indicates two features that appear related to the presence of these defects. 1)There is a correlation between the uniformity of the gable formed during the 950°C step and the presence of misorientations that are indicated by steps on the surface of uncoalesced cantilevers and step edges at defected coalescence fronts. 2)The specimens without dark-block defects had {11-22} facets on the ends of cantilevers just prior to contact and coalescence. We are examining new growths designed to determine more exactly the conditions necessary to eliminate dark-block defects. Their elimination is expected to enhance optical emission and uniformity over millimeter-size areas. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under Contract DE-AC04-94AL85000.

9:00 AM Student

O3, Reduction of Dislocation Density in MOVPE GaN Films by ELOG Without Photolithography and Chemical Etching: *Xiaolong Fang*[1]; Yongqian Wang[1]; Hira Meidia[1]; Subhash Mahajan[1]; [1]Arizona State University, Chem. & Matls. Engrg., Tempe, AZ 85287-6006 USA

To achieve high performance and reliable devices such as laser diodes and field effect transistors, the reduction of threading dislocations (TDs) density in GaN layers is critical. In the standard two-step growth the TD density could not be reduced below ~1010 cm-2. The In-situ multiple-interlayer method has achieved a dislocation density of 107cm-2 after three pairs of nucleation layer and overlayer. This approach results in an increasing stress and may produce cracks in the overgrown GaN film. The ex-situ epitaxial lateral overgrowth (ELOG) technique has been the most effective technique to reduce TD density in GaN layer, as low as 106/cm2. Other techniques, such as facet-controlled epitaxial lateral overgrowth (FACELO), pendeo-epitaxy (PE), and cantilever epitaxy (CE), essentially apply the same principle as in ELOG. However, in addition to the high TD density directly over the seed region, highly defective regions were also observed near the mask edges, and the coalescence fronts over the mask region (trenches in CE technique). Furthermore, it will be advantageous if patterning can be achieved in the MOVPE reactor. We report an in-situ ELOG MOVPE GaN growth technique in this talk. This technique directly uses the low temperature nucleation layer (LT-NL) as the seed layer and an in-situ deposited silicon nitride (SN) layer as the mask. Since the SN layer is so thin, it will planarize the valleys of the LT-NL, leaving the bumps open and mask the valleys. GaN overgrowth would seed only those outcroppings. By this technique, ex-situ patterning procedures are avoided. Also avoided are defects characteristic of ELOG, due to the angstrom-size thick mask layer, nano-size windows and window separations. The open bumps and masked valleys were observed by AFM section analysis profiles and HREM cross-section specimens. The defects structures were characterized by TEM. For growths on both AlN or GaN nucleation layers with the SN layer, TD density was reduced to 2~4´108/cm2, approximately two orders of magnitude lower than that observed in the conventional two-step MOVPE growth of GaN. Using the SN/AlN/sapphire composite, there are alternatively distributed high TD density regions and low TD density regions in the GaN overlayer.

ELOG characteristic defect features including vertical dislocation bundles, horizontal dislocations (HD), wing tilting, surface pits, nano-pipes and sub-grain boundaries were observed in this GaN overlayer. However, with the GaN LT-NL, the threading dislocations were uniformly distributed, and very few HDs were observed. The GaN as-grown NL is much rougher than the AlN as-grown NL. Therefore the open bump separations of the GaN NL are much smaller than that of the AlN. This may avoid the wing tilting which occurs in GaN overgrowth on the AlN NL with the SN layer. The support of our work by AFOSR is greatly acknowledged.

9:20 AM

O4, Multiple Quantum Well AlGaN Structure Grown on Patterned Sapphire Substrate: *Mikhail E. Gaevski*[1]; Jian Ping Zhang[1]; Vinod Adivarahan[1]; Maxim Shatalov[1]; Jinwei Yang[1]; Grigory Simin[1]; M. Asif Khan[1]; [1]University of South Carolina, Electl. Engrg. Dept., 301 Main St., Columbia, SC 29208 USA

Epitaxial lateral overgrowth (ELOG) using patterned sapphire substrate was demonstrated to be a powerful method for increasing internal quantum efficiency as well as for improving light extraction in optical devices based on III-nitrides. One of the major problems in ternary AlGaN ELOG is a phase separation manifested by formation of Ga-rich phase in the laterally grown part of structure. The phase separation can strongly deteriorate the optical devices quality by shifting the buffer/cladding layers' absorption edge to the quantum well emission wavelengths. In the present work we report on growth and characterization of multiple quantum well (MQW) structure over patterned sapphire substrate using monochromatic cathodoluminescence (CL) and cross-sectional energy dispersion X-ray analysis (EDX). The patterned sapphire substrate contained arrays of pillars with circle-shaped tops were produced using photolithography and reactive ion etching. The pillars were 8 μm in diameter and 0.5 μm in height. Distance between centers of neighboring pillars was 12 μm. The MQW Al0.19Ga0.81N (80 Å)/Al0.14Ga0.86N (30 Å) structure with 2 μm thick n+-Al0.29Ga0.71N buffer layer was grown using a low-pressure metal organic chemical vapor deposition system.[1] The distinguishing feature of the study was CL registration from the substrate side. This method utilizing the CL registration geometry, which simulates closely the flip-chipped LED with light extraction through the substrate. From EDX study we have shown that minimized phase separation was achieved by using a low V/III ratio growth condition. The molar fraction of AlN varied over the buffer from 30% in vertical grown region to 25% in laterally overgrown one. This variation cannot affect the light propagation from MQW. High-resolution CL mapping and scans confirm the existence of minor phase separation. At the same time MQW emissions from the lateral grown areas increased up to 8 times, indicating a strong improvement of crystal quality. We also studied the depth distribution of the CL intensity. Similar behavior for depth dependences of CL intensity for vertical and lateral grown parts of the structure was observed. In both cases short wavelength CL-signal related to the AlGaN buffer monotonously increased with accelerating voltage while CL measured at 330 nm wavelength saturated at about 15 kV. This depth saturation behavior of the 330 nm emission further confirmed that it aroused from MQW. These results show that MQW AlGaN structures grown over patterned sapphire substrates are very promising to achieving superior crystal quality with minimized phase separation. [1]J. P. Zhang, M. Asif Khan, W. H. Sun, H. M. Wang, C. Q. Chen, Q. Fareed, E. Kuokstis, and J. W. Yang, Appl. Phys. Lett. 81, 4392 (2002).

9:40 AM Student

O5, InGaN/GaN Buried Heterostructure Formed by MOCVD Growth on Nonplanar Substrates: *Dawei Ren*[1]; Xingang Zhang[1]; Wei Zhou[1]; P. Daniel Dapkus[1]; Daniel H. Rich[2]; [1]University of Southern California, Compound Semiconductor Lab., 3651 Watt Way, VHE 313, Los Angeles, CA 90089 USA; [2]University of Southern California, Dept. of Matls. Sci., 3651 Watt Way, VHE 607, Los Angeles, CA 90089 USA

Growth of InGaN/GaN heterostructure with a high Indium content has been presenting some challenging problems, such as very low Indium incorporation rate and Indium phase segregation, which results in the formation of Indium droplets on the surface. In this paper, InGaN/GaN buried heterostructure was grown on top of lateral epitaxy overgrowth (LEO) nonplanar substrate, enhanced Indium incorporation as well as the reduction of Indium phase segregation have been demonstrated. 2 μm thick GaN planar buffers were grown on c-plane Sapphire substrate by MOCVD. Conventional photolithography created stripe pattern on these GaN buffers. Pattern opening was judiciously chosen along Sapphire [11-20] direction. We made use of the fact that selective growth of two adjacent GaN stripes results in the formation of pyramids that coalesce to form flat, low defective mesa by LEO. As shown by X-TEM, SEM and AFM, these LEO mesas have reduced defect density, faceted {1-101} sidewalls and a flat top whose width is determined by the original separation of the two stripes. InGaN/GaN Quantum Wells (QW) were grown on top of these nonplanar substrates and conventional planar substrate. Photoluminescence (PL) and Cathodoluminescence (CL) were primary tools to characterize these structures. Unlike on planar substrates, two distinct QW emission peaks were found in the spectrums on nonplanar LEO substrates, which exhibited the effect of selective growth of InGaN on the different regions of the nonplanar structures. CL images showed longer wavelength emission originated from mesa top, in other words, more Indium was incorporated into the active region on mesa top. Further comparison of QW wavelengths between mesa top and planar substrate indicated that much more Indium was incorporated on mesa top, which revealed that enhanced Indium incorporation was achieved by the growth on nonplanar LEO substrates. The amount of Indium incorporation enhancement was found to be related with the top width of LEO mesas. Meanwhile, detailed CL images showed that Indium phase segregation was compressed on top of mesa, which in contrast to on planar GaN buffer. Our findings of enhanced Indium incorporation and reduced phase segregation pave a promising way to realize high efficient green-yellow light emitters.

10:00 AM Break

10:20 AM Student

O6, Study on Sapphire Nitridation in Hydride Vapor Phase Epitaxy System: Nitridation Mechanism: Fransiska Dwikusuma[1]; Thomas F. Kuech[1]; [1]University of Wisconsin, Dept. of Chem. Engrg., 1415 Engineering Dr., Madison, WI 53706 USA

Nitridation of sapphire surface prior to GaN growth improves the material properties in metalorganic vapor phase epitaxy (MOVPE), molecular beam epitaxy (MBE), and hydride vapor phase epitaxy (HVPE) growth techniques. While the process of nitridation of sapphire within the MOVPE and MBE environments has been studied, there are few reports on systematic studies of the sapphire nitridation during HVPE. The growth environment and growth process in HVPE are substantially different from that in the MOVPE and MBE processes. The high temperature, isothermal environment with the high ammonia activity characterizes the nitridation and growth environments. The impact and mechanism of sapphire nitridation within the HVPE system can be expected to be different from the previous results obtained in MOVPE and MBE. During the nitridation, a surface compound, containing nitrogen, develops with the composition, structure, and the surface morphology after nitridation critically depending on the nitrogen source used and the nitridation conditions of temperature, pressure, flow rates, and carrier gas. In the present study, the nitridation of c-plane sapphire within the HVPE system was systematically studied as a function of time and ammonia partial pressure. The chemical state and morphology of sapphire surface after nitridation were characterized using an ex situ x-ray photoelectron spectroscopy (XPS) and an ex situ atomic force microscopy (AFM). During nitridation process, nitrogen was incorporated into the sapphire surface and the nitrogen content increased with nitridation time as well as with ammonia partial pressure. There were at least two different nitrogen chemical bonding states, which can be attributed to N-Al bonds and a complex intermediate bonding state involving Al, N, and O (N-O bonds). The N-Al intensity increased with nitridation time, while the N-O intensity remained approximately constant with nitridation time. The O 1s intensity decreased with nitridation time indicating that oxygen was depleted from the near-surface region. The nitridation can be modeled as a reaction-interdiffusion process between an inward motion of nitrogen and an outward motion of oxygen, and a reaction at the interface between the sapphire and surface layer. Nitrogen diffuses into the sapphire and substitutes for the O, forming a bond with Al. The diffusion of nitrogen in sapphire was complicated by the outward diffusion of the displaced oxygen. The XPS data suggests that outward diffusion of oxygen may be slower than the inward diffusion of nitrogen. The chemical diffusion coefficient for nitrogen in an AlN-Al_2O_3 matrix at 1100°C was estimated to be ~1.5-1.9x10^{-15} cm^2/s. A smooth surface morphology was found after nitridation with no significant changes in the surface RMS

roughness were measured for times up to 60 minutes when compared to the as-received sapphire.

10:40 AM

O7, Interface Interdiffusion and Chemical Reaction in GaN/Sapphire and AlGaN/Sapphire Heterojunctions: *Xiaoling Sun*[1]; Steve H. Goss[1]; Leonard J. Brillson[1]; David C. Look[2]; [1]The Ohio State University, Electl. Engrg., 205 Dreese Lab., 2015 Neil Ave., Columbus, OH 43210 USA; [2]Wright State University, Univ. Rsch. Ctr., Dayton, OH 45435 USA

The strong chemical interactions and large lattice mismatch between III-nitrides and sapphire can have a major impact on the electronic quality of epitaxial GaN or AlGaN films. In particular, donor impurity diffusion, alloying, and related defect formation can occur near the interface at the high (1150°C) growth temperatures. We have used low temperature (10K) micro-cathodoluminescence spectroscopy (CLS) in a UHV scanning electron microscope (SEM) and UHV secondary ion mass spectrometry (SIMS) to probe the electronic and chemical features at the HVPE GaN/sapphire and AlGaN/sapphire interfaces in cross section on a nanometer scale. Previously, we used cross sectional Auger electron spectroscopy (AES) of GaN/Al_2O_3 junctions to show that cross-diffusion of O, Al, and N take place on a sub-micron scale.[1] Here, we have obtained SIMS depth profiles in plan view as well as SIMS images and micro-CLS spectra in cross section of GaN/Al2O3 and AlGaN/Al_2O_3 interfaces. SIMS depth profiles and images reveal pronounced diffusion of O from sapphire 100 nm to several μm into GaN, depending on the thickness of the epilayer. Conversely, plateau concentrations of N can extend microns into the sapphire. SIMS images reveal clear evidence of chemical bonding between the AlGaN and Al_2O_3 constituents. These include AlN and GaO in the near interface region as well as complexes of GaON, AlGaO, AlGaN and AlGaON. CLS obtained at 10 keV with 50 nm beam diameter at 10 K reveal two broad features at ~3.5 eV and ~3.6 eV above the GaN band gap at the buried interface, whose precise energies vary with position. It is possible that these peaks are from the complexes mentioned above. Furthermore, the spatially-varying energies are due to variations in stoichiometry and bonding rather than any degenerate doping effects. At the AlGaN/sapphire interfaces, CLS also reveals two additional, above-band-gap peaks at somewhat higher energies of ~3.75 and ~3.8 eV that are likely due to similar complexes. These higher energies are consistent with interfacial alloys of higher Al concentrations since Al was incorporated during growth as well. While substantial differences in interface abruptness are measured for III-nitrides grown with different growth surface preparation, these results demonstrate that interdiffusion and alloying are common features of III-nitride/Al_2O_3 interfaces grown at the high temperatures employed for HVPE. [1]X. L. Sun, S. T. Bradley, G. H. Jessen, D. C. Look, R. J. Molnar, L. J. Brillson, J. Vacc. Sci. Tech. 2003, submitted.

11:00 AM

O8, The Chemistry and Kinetics of LiGaO2 Substrate Nitridation for the Optimization of GaN Epitaxial Growth: *Maria Losurdo*[1]; Giovanni Bruno[1]; April S. Brown[2]; Sangbeom Kang[3]; Tong-Ho Kim[3]; Alan W. Doolittle[3]; [1]Institute of Inorganic Methodologies and of Plasmas, IMIP-CNR, via Orabona, 4, Bari Italy; [2]Duke University, Dept. of Electl. & Compu. Engrg., 128 Hudson Hall, Durham, NC USA; [3]Georgia Institute of Technology, Atlanta, GA 30332 USA

LiGaO2 is an interesting alternative substrate for GaN epitaxial growth by both MOCVD and MBE because of its small lattice mismatch to GaN, and because it is readily etched enabling the transfer of a GaN thin film to another substrate. Many studies have shown that GaN films "delaminate" from the LGO after growth, and authors have attributed this phenomenon to poor adherence between the film and the substrate. Therefore, it is important to understand and investigate the interfacial properties of GaN/LiGaO2 substrates. Herein, we present data on the study of the chemistry and kinetics of LGO surface preparation for the growth of GaN. Many groups have investigated nitridation of the LGO surface by NH3 exposure in MOCVD and N2 plasma treatment in MBE. These studies concluded that a LiGaON mixed nitride-oxide is formed. It was believed to be the case that no buffer layer was needed for the growth of GaN on LGO because of the absence of significant lattice mismatch. However, GaN heteroepitaxial layers grown directly on nitrided LGO by MBE showed poorer characteristics in comparison to films grown with buffer layers. We have investigated in detail the chemistry and kinetics of the LGO nitridation at various temperatures and exposure times. We have found that the incorporation of nitrogen in the LGO, i.e., what is called nitridation, occurs with damage to the LGO. This damage can extend significantly into the LGO and explains why GaN directly on nitrided LGO has reduced quality. From our study on the characterization of the nitridation chemistry and kinetics of LGO performed in both MBE and MOCVD conditions using both N2, N2-H2 and NH3 plasmas at temperatures in the range 400-700°C, at time in the range 10s-1h, we found that a very narrow window of temperature and time exists in which two monolayers of GaN on LGO can be formed without any morphological and compositional damage of the LGO substrate. The GaN formation competes with a very fast in-diffusion of N- and H- atoms into the LGO substrate that is consequently damaged. We also show that during MOCVD the problem of LGO decomposition is not due, as reported, to the H2 carrier gas, but to the use of NH3 that can form lithium amide LiNH2, thus decomposing the LGO substrate. This reaction is avoided with the optimized nitridation for GaN MBE. We will present and discuss the complete chemistry and kinetics of LGO nitridation and its effect on the quality of GaN epitaxial layers. In situ RHEED and spectroscopic ellipsometry data are used to develop the nitridation kinetics and the impact of the process on the initial stage of GaN growth. This chemical analysis of the interaction of LGO with N- and H-atoms highlights that lattice match is not the only factor to consider in epitaxial growth, but also that the surface chemical reactivity of the substrate must be taken into account.

11:20 AM

O9, Identification of the Adducts Formed between Magnesocene ($MgCp_2$) and NH_3: Origin of the Memory Effect: *George T. Wang*[1]; J. Randall Creighton[1]; [1]Sandia National Laboratories, PO Box 5800, MS 0601, Albuquerque, NM 87185-0601 USA

The p-type doping of nitride materials is commonly achieved using magnesocene ($MgCp_2$) as the source compound. However, difficulties remain with controlling the incorporation of Mg during MOCVD film growth, which often exhibits memory effects. While the formation of an adduct between magnesocene and ammonia has been previously speculated, one has never been experimentally isolated or identified. We have spectroscopically observed and identified, for the first time, the adducts formed between magnesocene and ammonia. Density functional theory (DFT) quantum chemistry calculations have also been performed on the system to determine the structures and energetics of the reaction products. It was found that ammonia can form adducts with magnesocene in both 1:1 and 2:1 ratios, i.e. NH_3:$MgCp_2$ and $2NH_3$:$MgCp_2$, via NH_3 attack of the positively charged Mg center of $MgCp_2$. Adduct formation is reversible and the 1:1 and 2:1 products can be converted to one another by increasing or decreasing the NH_3 partial pressure. Both adducts are condensable at room temperature and their formation is the likely origin of the magnesium memory effects that have been observed during MOCVD of III-Nitride materials. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under contract DE-AC04-94AL85000.

Session P: Epitaxy I: Growth and Characterization

Thursday AM, June 26, 2003
Room: Ballroom East
Location: Olpin Union Building

Session Chairs: Jerry Woodall, Yale University, Dept. of Elect. Engrg., New Haven, CT 06520 USA; Gary Wicks, University of Rochester, Inst. of Optics, Rochester, NY 14627 USA

8:20 AM

P1, A Chemical and Kinetic Study of P-for-As Anion Exchange Reactions in GaAs/GaAsP Superlattice Structures: *April Susan Brown*[1]; Maria Losurdo[2]; Giovanni Bruno[2]; Terence Brown[3]; Gary May[3]; [1]Duke University, 128 Hudson Hall, Durham, NC 27708 USA; [2]IMIP-CNR, Bari Italy; [3]Georgia Tech, Atlanta, GA 30332 USA

The exchange of group-V atoms on a semiconductor surface affects the interface properties, in particular the composition and thickness, of epitaxially grown mixed anion heterostructures. So far, a deep understanding of the mechanisms and ultimate control of anion exchange has not been achieved. Most previously proposed kinetic models are based on a simple diffusion mechanisms. In this contribution, we investigate P-for-As anion exchange by characterizing a series of periodic GaAs/GaAsyP1-y superlattice (SL) structures created by exposure of a GaAs static surface to a phosphorus flux (P2) during MBE. Two different As4 fluxes are used: 2x10-6 and 4x10-6 T, during the growth of the GaAs layers resulting in a different GaAs surface reconstructions: (2x4) and diffuse (2x1), during the exposure. The effects of substrate temperature, P2-soak time and incident flux, and GaAs surface reconstruction on anion exchange have been studied and analyzed. Reflection High Energy Electron Diffraction (RHEED), high resolution x-ray diffraction, and spectroscopic ellipsometry (SE) have been used to determine the fraction of incorporated phosphorus and the thickness of the exchanged layer. SE (covering the 0.7 - 5.5 photon energies) was used to measure the SL pseudodielectric function and gives information on the compositions and thicknesses of the interface layers created during P2 exposure. The GaAs surface reconstruction has a strong impact on the extent (in terms of both P surface coverage and P indiffusion) of the P-for-As anion exchange. Furthermore, the relationships between the substrate temperature and P2 soak-time on anion exchange are also dependent on the GaAs surface reconstruction. In particular, it is found that the As-stable reconstruction (2x4) realized at the higher As4 flux, reduces the phosphorus surface coverage and hinders the phosphorus indiffusion. For this surface, incorporation of phosphorus is limited and almost independent of temperature for T • 470°C; the exchanged layer thickness increases slightly with P2 soak time. For this GaAs surface, a temperature of 520°C is found to be the threshold value for overcoming the kinetic barrier to phosphorus incorporation and P-for-As exchange. In contrast, for the less As-rich GaAs surface the P-for-As exchange and total P-incorporation is very large, penetrating into the entire GaAs epitaxial layer thickness (200Å) that is converted into a GaAs0.8P0.2 ternary compound. In this case, the phosphorus incorporation increases with temperature, but is almost independent on time of exposure of the surface to the P2 flux. These data indicate that the phosphorus diffusion is not kinetically limiting the anion exchange process. Therefore, a mechanism based solely on phosphorus diffusion is not adequate for explaining the P-for-As exchange, but the surface-based reactive process involving must also be included. The competitive formation of AsP compounds with temperature dependent desorption kinetics plays a significant role. In this framework, surface As is a sink for P, inhibiting the anion exchange. Other surface reaction processes include site availability and surface perfection (nanoscale flatness). A complete chemical and kinetic model including all the surface reactive steps will be given and discussed with the aim towards controlling the experimental parameters that govern the anion exchange and quality mixed anion heterointerfaces. The authors would like to acknowledge the Air Force Research Laboratories support of the project on Control of Anion Exchange During Molecular Beam Epitaxy.

8:40 AM

P2, Growth and Polarization Anisotropy Characterization of Ordered InGaAsP for Optical Fiber Applications: Stefan Neumann[1]; *Werner Prost*[1]; Jochen Spieler[2]; Robert Blache[2]; Evguenia Khorenko[1]; Gottfried H. Doehler[2]; Franz Josef Tegude[1]; [1]Universität Duisburg-Essen, Solid-State Elect. Dept., Lotharstr. 55, Duisburg D-47048 Germany; [2]Universität Erlangen-Nuernberg, Technische Physik 1, Erwin-Rommel-Str. 1, Erlangen D-91058 Germany

The polarisation mode dispersion (PMD) is limiting the transmission capacity of conventional multi-mode optical fibre. The on-line correction of PMD may become feasible if a dynamic polarisation dispersion measurement could trigger a PMD correction circuitry.[1] The near band-gap absorption anisotropy of ordered semiconductor layers is proposed here for polarisation sensitive devices and circuits at the wavelength of the optical fibre. In this work ordered GaInAsP lattice matched InP-substrate were grown by low-pressure metal-organic vapor-phase epitaxy at reduced growth temperatures. The quanternary composition is adjusted for for 1.3 µm and 1.55 µm applications. A non-gaseous source configuration has been used especially because of the better thermal decomposition of TBP compared to phoshine. This is a key component to realise a constant group-V composition in thick quaternary layers. The polarisation anisotropy of GaInAsP is attributed to a natural superlattice in [111]B and [111]A direction. The asymmetric ½ (115) x-ray reflection has been used to study the crystal structure of In0.75Ga0.25As0.5P0.5. A peak at 2Theta = 39.8° is observed clearly proving the existence of an atomic-scale superlattice along the [11-1] and [1-11] direction. The ordering effect results in a band gap reduction and in a splitting of the light and heavy hole states in the valence band. The splitting energy EVBS correlated to the degree of ordering. For various compositions, growth temperatures, and substrate tilts the valence band splitting energy EVBS is evaluated by electro absorption measurements.[2] A high degree of ordering is observed at 1.55 µm and the highest degree (EVBS = 25 meV) is obtained at 1.3 µm. The valence band splitting energy is even higher than found in the ternary material InGaAs on InP and InGaP on GaAs. These observations indicate a strong additional contribution of group-V ordering in the InGaAsP layers. PIN diode layers were grown incorporating a 700 nm thick ordered absorption layer. Their I-V characteristic exhibit a reverse breakdown voltage of 25 V. The ordered absorption layer results in high quantum efficiency of up to 0.2 A/W with up to 50% anisotropy for polarized light. A first polarization switch is fabricated combining two pin-diodes and a FET exhibiting 55 dB polarization contrast. These results indicate the high potential of this approach for on-line polarisation mode dispersion measurement. References: [1]H. Bülow; Core and ATM networks, NOC´97, Ed. D.W. Faulkner, A.L. Harmer, IOS Press 1997. [2]J. Spieler et al; Spontaneous Group III and V Superlattice Ordering in InGaAsP; Proc. 26th Internat. Conference on the Physics of Semiconductors, Edinburgh, July 29 - August 2, 2002.

9:00 AM

P3, Surface Structure and Stability of Pseudomorphic InGaAs Layers: *Joanna Mirecki Millunchick*[1]; Alexandru Riposan[1]; Bruce J. Dall[1]; Christopher A. Pearson[2]; Bradford G. Orr[3]; [1]University of Michigan, Matls. Sci. & Engrg., 2030 HH Dow, 2300 Hayward St., Ann Arbor, MI 48109 USA; [2]University of Michigan, Dept. of Compu. Sci., Engrg. Sci. & Physics, Flint, MI 48502 USA; [3]University of Michigan, Applied Physics, The Harrison M. Randall Lab., Ann Arbor, MI 48109 USA

The surface structure of a seemingly random alloy layer has a great impact on the compositional homogeneity and subsequent interface formation. For example, it has been suggested that random fluctuations in composition may initiate lateral composition that propagates through the remainder of the film. Furthermore, interfacial abruptness is greatly influenced by the step edge roughness. We studied the morphology and surface reconstruction of InxGa1-xAs alloy layers during growth and after annealing. Films of different compositions were grown by MBE on GaAs and InP to thicknesses less than the critical thickness for 3D islanding or misfit dislocation formation, and examined using in-situ Scanning Tunneling Microscopy (STM) and ex-situ Atomic Force Microscopy (AFM). The morphology of the as-grown lattice mismatched InGaAs layers (deposited on either InP or GaAs) is very flat (RMS<1ML over 4 ?m2). The surface reconstruction during growth was 2x3 according to RHEED, but the STM shows that surface is covered with a number of different reconstruction domains. Portions of the surface have the ?2(2x4) or ?2(2x4) reconstruction commonly observed in GaAs(001) and InAs(001) depending on the amount of In. However, the majority of the surface is comprised of an unusual (4x3) reconstruction. A model developed based on the STM data suggests that this (4x3) surface contains both anion and cation dimers. During annealing, it was found that the films may undergo a destabilization of the step structure. The surface of 25 ML thick In0.27Ga0.73As/GaAs films grown at T=486°C and As overpressure BEP=16x10-6 torr, for example, are first covered with large 2D islands. These islands initially grow upon annealing, but eventually dissolve. At the same time, the steps develop a pronounced undulation. As the anneal continues, the step undulations either form cusps which inject vacancy islands into the terrace. As the anneal progresses, the vacancy islands grow deeper and may inject strain relieving dislocations into the film. For high annealing temperatures and times, the amplitude of the step undulations grow larger than the terrace width, and the terraces break into discontinuous mesas. Continuum elasticity calculations show that the step destabilization is strain driven.

9:20 AM Student

P4, Surfactant Modified Lateral Growth and Surface Morphology of GaAs (001): *Ryan R. Wixom*[1]; Loren W. Rieth[1]; Gerald B. Stringfellow[1];

[1]University of Utah, Matls. Sci. & Engrg., 1495 East 100 S., Rm. 120 Kennecott, Salt Lake City, UT 84112 USA

Epitaxial growth on patterned and non-planar surfaces is necessary for the fabrication of many modern solid-state devices which integrate novel materials and low dimensional structures. Heteroepitaxy, pendeoepitaxy, and growth on patterned substrates all require an understanding, if not control, of lateral growth and morphological evolution. Typical GaAs organometalic vapor phase epitaxy (OMVPE) growth conditions result in anisotropic lateral growth which has significant technological implications when the shape and size of epitaxial patterns must be accurately controlled. The use of surfactants is emerging as a possible method of controlling surface processes during epitaxial growth. We have studied the use of Bi, Sb, and Te as surfactants to modify the lateral growth rate of GaAs on nominally (001) GaAs substrates patterned with 200 nm tall mesas of several different shapes. Optical and atomic force microscopy were used to characterize surface morphology and mesa evolution. Lateral growth rates where obtained by ex-situ measurement of mesa sidewall progression. Bi has the largest effect on lateral growth. A Bi/V ratio of 0.002 in the vapor increased the [110] lateral growth rate by 3.5 times while having no effect on the [bar-110] growth rate. Sb also increased the [110] growth rate by a factor of 2.8 at a Sb/V ratio of 0.005, and did not change the [bar-110] growth rate. Te does not have a significant effect on the lateral growth rates of GaAs. The large changes in lateral growth rate confirm that sticking coefficients at GaAs steps are extremely small and can be markedly affected by tiny changes in step energetics induced by surfactants. Surfactant mediated growth mechanisms were studied by quantitatively examining changes in step bunching, step spacing, wedding cake structures, etch pits, surface roughness, and the shape of mesa profiles. Samples grown without a surfactant on singular (001) substrates exhibit a mounded wedding cake like morphology. Layer by layer growth of the nominal surface is not favored, but appears to proceed by step flow from the sides of these mounds. The addition of Bi, Sb, and Te promote substantial morphological changes to the GaAs surface. Samples grown with Bi form 40 nm tall ridges on the surface which are aligned in the [110] direction. Sb elongates the mounds in the [110] direction, but the mounds remain distinct. Te reduces the RMS roughness an order of magnitude and smooths the mounds from 80 nm to just 6 nm in height. Te also reduces the bunched-step height, increases step spacing, and promotes the growth of a facet misoriented 1° from the nominal surface.

9:40 AM Student

P5, Experimental Studies and Modeling of Selective Area Growth of InP-Related Alloys by MOCVD: *Sang-Jun Choi*[1]; P. Daniel Dapkus[1]; Kostadin Djordjev[1]; Ryan Stevenson[1]; [1]University of Southern California, Depts. of Matls. Sci. & Electl. Engrg., 3651 USC Watt Way, VHE Rm. #309, University Park, Los Angeles, CA 90089-0243 USA

Studies of the selective area growth (SAG) of InAs, InP, GaAs, GaP, InGaAs, InGaP and InGaAsP by MOCVD have been carried out with goal of developing a CAD model of SAG for use in device design. The characteristics including growth rates, growth rate enhancement ratios in unpatterned areas and composition variations of InP-related materials were investigated by growing superlattice structures of InP/InGaAs, GaAs/InGaP and InP/InGaAsP on wafers patterned with dielectrics. The enhancement ratio of each binary compound showed that InAs had the largest ratio and GaP had the lowest ratio as follows. RInAs>RInP>RGaAs>RGaP. The enhancement ratio of InGaAs was greater than that of InGaP and almost the same as that of InGaAsP. The enhancement ratios and compositions of ternary and quaternary compound materials were calculated using the enhancement rate of each binary compound and compared with the measured data. The calculated data were matched well with the measured data. The enhancement ratio of alloys was also dependent on the composition of the unpatterned region. The composition of alloy compounds changed according to the dielectric mask widths. The indium component in quaternary alloy changed by 0.043% while arsine component changed by 0.012% for range of mask widths studied here. The relatively larger variation of group III components than group V components can be attributed to the high V/III ratio growth conditions. The composition variations introduced compressive strain into the selectively grown region, and the strain changes have been calculated. Two-dimensional gas phase diffusion models were used to simulate selective area growth, and the results were compared with the measured data. The gas phase diffusion constant, D, and the adsorption rate, k, were used as parameters in the modeling. The D/k values for the binary compounds were 45 μm for InAs, 65 μm for InP, 160 μm for GaAs and 300 μm for GaP, respectively. The D/k values for gallium binaries were much longer than indium binaries. This causes excess enhancement of the indium composition near the mask edges. The results from these binary compound studies can be utilized to simulate alloy compounds. Broad area laser devices were made by the selective area growth process and lasing wavelengths and threshold current densities were measured. The span of lasing wavelengths with respect to the unpatterned area over a range of dielectric mask widths up to 50 microns was 150 nm. The threshold current densities ranged from 250 to 500 A/cm2/well as the mask width varied. The threshold current density increased up to 1000 A/cm2/well when the mask width was 50 μm. We will also discuss the effects of various surface treatments on the performance of InGaAsP lasers formed by two-step selective area growth.

10:00 AM Break

10:20 AM

P6, Faceting and Lateral Overgrowth on a SiO_2-Masked GaAs Substrate - Dependence on Nanoscale Dimensions: *S. C. Lee*[1]; L. R. Dawson[1]; S. R.J. Brueck[1]; [1]The University of New Mexico, Ctr. for High Tech. Matls., Dept. of Electl. & Compu. Engrg., 1313 Goddard SE, Albuquerque, NM 87106 USA

Faceting and lateral overgrowth and coalescence of GaAs selectively grown by molecular beam epitaxy (MBE) on a nanoscale SiO_2-masked GaAs(100) substrate is reported. A 355-nm period, 2 dimensional array of circular holes was generated by interferometric lithography and dry-etching on a 45-nm thick SiO_2 film deposited on a GaAs substrate. Samples were prepared with hole diameter ranging from ~70- to 300 nm. Selective growth [1,2](growth temperature ~630°C and growth rate ~0.1 monolayer/s) corresponding to a 200-nm thick large-area GaAs deposition was performed. Fig. 1 shows top view scanning electron microscope (SEM) images of the SiO_2 mask (a) and the resulting GaAs film (b). Faceting and lateral overgrowth are clearly evident. As seen in Fig. 1(a), the initial mask holes are circular while the GaAs epitaxially grown on each hole (GaAs epi-island) is dominantly rectangular (top down) and pyramidal (sidewalls) evidencing a range of crystal faces. For this 200-nm thick deposition, partial coalescence between multiple epi-islands initiated in different holes is observed. Fig. 2 shows a top view SEM image of GaAs epi-islands grown under the same conditions on a similar mask with ~70- to 100-nm diameter holes. For these small holes, only the initiation of faceting on the surface of the nanoscale epi-islands is observed. The growth is clearly selective, with no deposition on the large-area SiO_2 surface, and the total growth thickness is strongly suppressed on comparison with both the large growth and the larger size hole growth. The height of the epi-islands in Fig. 2 is less than 100 nm which is considerably smaller than the deposition thickness. These results imply that, in contrast to large-area conventional growth, the resulting Ga sticking coefficients could be much less than unity for this case and the growth is highly suppressed by a significant loss or an insufficient supply of Ga atoms for this small area growth. Experimental details and growth mechanisms important for understanding nanoscale patterned MBE such as mass transport across the mask-substrate boundary will be discussed. Also, coalescence between adjacent, nanoscale GaAs epi-islands depending on the pattern and crystal direction will be discussed. [1]S. C. Lee, K. J. Malloy, and S. R.J. Brueck, J. Appl. Phys., 90, 4163 (2001). [2]S. C. Lee, K. J. Malloy, L. R. Dawson, S. R.J. Brueck, J. Appl. Phys., 92, 6567 (2002).

10:40 AM Student

P7, The Effect of N on Ordering in GaInP: *David Cook Chapman*[1]; Gerald B. Stringfellow[1]; Bong Joong Kim[2]; Tae Yeon Seong[2]; [1]University of Utah, Dept. of Matls. Sci. & Engrg., 122 S. Central Campus Dr., EMRO 304, Salt Lake City, UT 84112 USA; [2]Kwangju Institute of Science and Technology, Dept. of Matls. Sci. & Engrg., Kwangju 500-712 Korea

Surfactants have become an extremely useful tool for controlling the properties of epitaxial layers of both elemental and III-V semiconductors. Dramatic effects on microstructure, dopant incorporation, and alloy composition have been observed. These effects occur due to changes in bonding at the surface induced by small concentrations of surfactants. For example, GaInP grown by atmospheric pressure organometallic vapor phase epitaxy (OMVPE) typically exhibits $CuPt_B$ ordering; however, previous studies using isoelectronic surfactants larger than P in GaInP have reported a complete disordering of the lattice, with a consequent

increase in bandgap energy. Other studies have reported the production of an entirely different ordered structure. This paper reports the effects of N, an isoelectronic element smaller than P, as a surfactant on GaInP layers grown by OMVPE using dimethylhydrazine (DMHy) as the N source. In situ surface photoabsorption (SPA) measurements show a large change in the surface structure with the emergence of a lower energy peak and a significant decrease in the P dimer peak with increasing partial pressure of DMHy. Transmission electron microscopy (TEM) data show that N disorders GaInP layers grown on nominally (001) GaAs substrates. It is postulated that N disorders the GaInP layers by competing with P for surface sites. Furthermore, the surface N does not form dimers due to the large microscopic strain energy involved. Thus, surface N acts to reduce the driving force for ordering. Nitrogen also has a significant effect on the Ga/In ratio in the bulk. This is speculated to result from increased In evaporation due to the N covered surface. Photoluminescence (PL), X-ray diffraction (XRD), and secondary ion mass spectroscopy (SIMS) are used to estimate the amount of Ga, In, and N in the samples. The In decreases nearly 40% from that of the lattice matched alloy in samples grown at 620°C, V/III=40, and DMHy/V=0.6. Low temperature PL data confirm that the samples are Ga rich, showing a broad peak with an energy up to 80 meV higher than the bandgap of lattice matched disordered GaInP.

11:00 AM Student

P8, The Effect of Nitrogen on the Optical and Transport Properties of Ga0.48In0.52NyP1-y Grown on GaAs (001) Substrates: *Y. G. Hong*[1]; A. Nishikawa[1]; C. W. Tu[1]; [1]University of California, San Diego, Dept. of Electl. & Compu. Engrg., 9500 Gilman Dr., La Jolla, CA 92093-0407 USA

Recently, Ga0.52In0.48P lattice-matched to GaAs has received considerable attention due to its device applications, such as high-efficiency tandem solar cells and heterojunction bipolar transistors (HBTs). Nitrogen incorporation in III-V compound semiconductor results in large bandgap bowing. Recently we have shown that, by analyzing pseudomorphic Ga0.46In0.54NyP1-y /GaAs quantum-well photoluminescence (PL), nitrogen incorporation in Ga1-xInxP lowers the conduction band edge, resulting in a nearly zero conduction band offset when y~0.005. Thus, Ga1-xInxNyP1-y could be an ideal material for GaAs-based npn HBTs. We investigate optical and electron transport properties of Ga1-xInxNyP1-y lattice-matched to GaAs (001) substrates when (x-0.48) ~2.8y with a tunable band gap energies smaller than the Ga0.52In0.48P bandgap. Bulk Ga1-xInxNyP1-y (700nm) on GaAs (001) substrates were grown by gas-source molecular beam epitaxy (GSMBE) and characterized by high-resolution X-ray rocking curve (XRC), PL and Hall-effect measurement. The red shift of the room-temperature PL peak with nitrogen incorporation indicates a large bandgap bowing. 2% N reduces the bandgap by about 220 meV. Low-temperature PL shows significant line shape difference between the Ga0.44In0.56P and Ga0.44In0.56N0.01P0.99 sample. The nitrogen-containing sample has an asymmetric PL line shape with a large low-energy tail, indicating the presence of localized states. To investigate the electron transport properties of Ga0.48In0.52NyP1-y, Si-doped samples were grown with the same Si flux but different N2 flow rate. Hall measurements show a decreasing free electron concentration and mobility with increasing N concentration. In order to improve the sample quality, we rapid-thermal annealed (RTA) the samples for 10 seconds under N2 ambient. For the Ga0.48In0.52P sample, the free electron concentration decreases from 5.1x10 18 to 1.1x10 18 cm-3 as the RTA temperature is increased to 800 C, whereas, that of Ga0.48In0.52N0.005P0.995 decreases much faster, from 4.4x10 18 to 8.0x10 16 cm-3. The monotonic decrease with annealing temperature of GaInNP is opposite to the behavior of the hole concentration of GaInNAs as a function of annealing temperature. Recently, Yu et al.[1] proposed a model of mutual passivation between Si and N. Si is passivated by N through the formation of Si-N pairs because N is more electronegative than P (Pauling electronegativities of N and P being 3.04 and 2.19, respectively) and, thus, has a tendency to bind the free valence electron of Si. When Ga0.48In0.52NyP1-y is grown at a relatively low temperature (~450C) by MBE, Si atoms are randomly distributed in the Ga sublattice sites. During RTA at high temperatures, Si atoms have enough thermal energy to diffuse to be near N to form Si-N pairs. This passivation process results in a significant drop in the electron concentration in N-containing Ga0.48In0.52N0.005P0.995, but may provide an opportunity for electrical isolation of devices. [1]K.M. Yu, et al, Nature Materials, 1, 185 (2002).

11:20 AM

P9, Heteroepitaxial and Homoepitaxial Growth of ZnO{0001} Thin Films via Metalorganic Vapor Phase Epitaxy and their Characterization: *Robert F. Davis*[1]; Tim P. Smith[1]; Harmony McClean[1]; Bunmi T. Adekore[1]; David J. Smith[2]; [1]North Carolina State University, Matls. Sci. & Engrg., Box 7907, Raleigh, NC 27695-7907 USA; [2]Arizona State University, Physics & Astron., Ctr. for Solid State Sci., Box 1704, Tempe, AZ 85287-1704 USA

Epitaxial ZnO thin films have been grown on GaN(0001) epilayers and ZnO{0001} substrates via metalorganic vapor phase epitaxy at 450°C and 500°C and between 40 torr and 250 torr total pressure. Atomic force micrographs and X-ray photoelectron spectroscopy (XPS) results acquired from the heteroepitaxial films grown for progressively longer times revealed that the ZnO nucleated and grew via the Volmer-Weber (island) mode on the terraces of the GaN. Additional XPS analysis revealed that the shift in the position of the Ga3d core level following two minutes of growth was consistent with the Ga-O bond in Ga2O3. Thus the limited diffusion distances of the reactants at the low temperature of deposition and their further hindrance by micro-regions of gallium oxide were deemed the likely causes of the observed growth. Transmission electron microscopy revealed threading dislocations generated at the ZnO/GaN interface. Homoepitaxial films were grown on both O- and Zn-terminated, basal-plane-oriented ZnO wafers diced from boules produced by vapor phase transport. Maps of on-axis X-ray rocking curves obtained over these wafers revealed defined areas of width in the FWHM that ranged from <50 arcsec to >1050 arcsec, indicating the presence of tilted domains. This macrostructure was manifested in all the deposited ZnO films. The films grown on O-terminated ZnO surfaces were initially dense. However, they changed to a textured polycrystalline microstructure after ?100 nm and possessed a surface roughness of 7.3 nm. By contrast, the films grown on the Zn-terminated surface under the same conditions were fully dense, without texture and appeared to be monocrystalline with a significantly improved surface roughness of 3.4 nm. Cross-sectional transmission electron microscopy of the wafers revealed high densities of edge dislocations and stacking faults with associated Frank partial dislocations; the latter were located on the basal planes. Similar defects were also observed in the deposited films.

11:40 AM P10, Late News

Session Q: Materials Issues for Organic Optoelectronics and Transistors

Thursday AM Room: Ballroom West
June 26, 2003 Location: Olpin Union Building

Session Chairs: Tom Jackson, Pennsylvania State University, University Park, PA 16802-2701 USA; David Gundlach, IBM Zurich Research Laboratory, Ruschlikon 8803 Switzerland

8:20 AM

Q1, Organic Light Emitting Diodes with Laminated Electrodes: *Tae-Woo Lee*[1]; [1]Lucent Technologies, Bell Labs., Murray Hill, NJ 07974 USA

Abstract not available.

8:40 AM

Q2, Combinatorial Methods for Investigating the Effect of Layer Thickness and Doping on the Performance of Red Organic Light-Emitting Devices: *David J. Gundlach*[1]; Tilman Beierlein[1]; Heike Riel[1]; Siegfried Karg[1]; Walter Riess[1]; [1]IBM Research, Zurich Rsch. Lab., Saumerstrasse 4, Ruschlikon 8803 Switzerland

As a consequence of the multilayer structure used in fabricating OLEDs a careful balance of the electrical and electro-optical device characteristics is often required for suitable overall performance in applications like high information content displays. Recently it has been shown that a combinatorial approach to device fabrication is an efficient way to rapidly integrate candidate material sets, study device physics, and optimize performance.[1] Using such an approach we have fabricated efficient and

stable red, green, and blue devices that allow coverage of more than 90% of the NTSC color range with greater than 20 cd/A efficiency (white) at 300 cd/m^2. To demonstrate the usefulness of combinatorial methods for studying and optimizing devices we present data showing effect of carrier transport layer thickness and emission layer doping on device performance for red fluorescent OLEDs. Two sets of 50 devices were fabricated on a single substrate using a top emission device structure with Alq_3 as the emissive host layer doped with DCJTB (a derivative of the laser dye DCM) or double doped with rubrene and DCJTB. As the Alq_3:rubrene:DCM derivative system has been previously studied in detail, this material set serves as model system for this investigation.[2] From this direct comparison we show the complex interplay between electrical and optical effects in multilayer OLED structures. As interference effects influence the emission spectra of top emission devices we find that the spectra is most strongly influenced by the hole transport layer thickness. For devices of equal film thickness the incorporation of rubrene in the emissive layer was found to increases luminance by approximately 15% and red shift the emission spectra, consistent with previous reports.[2] However, for display applications a more useful comparison is made for devices with similar chromaticity since luminance is a measure of radiance weighted by the response of the human eye. For such a comparison we find that luminance can be increased by as much as 250% with double doping. The best double doped devices have luminance as large as 350 cd/m^2 at 20 mA/cm^2 (1.75 cd/A), CIE 1931 coordinates of x = 0.65, y = 0.35, and an extrapolated half-brightness lifetime of more than 15,000 hours at 10 mA/cm^2. Further improvements in device performance are made by incorporating a dielectric capping layer to improve light outcoupling and external efficiency, with capped double doped devices having luminance as large as 620 cd/m^2 at 20 mA/cm^2 (3.1 cd/A) and chromaticity similar to uncapped devices.[3] [1]T. A. Beierlein, et. al., Proc. of SPIE 4464, 178 (2002) [2]T. K. Hatwar, et. al., The 10th Int. Workshop on Inorganic and Organic Electroluminescence Digest, 31 (2000) [3]H. Riel, et. al., Appl. Phys. Let., 82, 466 (2003).

9:00 AM

Q3, Efficient, Fast Response and Color-Tunable Polymer Light-Emitting Devices: *Cheng Huang*[1]; Chun Yin[2]; Chang-Zheng Yang[2]; Wei Huang[3]; E. T. Kang[3]; [1]The Pennsylvania State University, Dept. of Electl. Engrg. & Matls. Rsch. Inst., 187 Matls. Rsch. Lab., University Park, PA 16802 USA; [2]Nanjing University, Dept. of Polymer Sci. & Engrg., Nanjing 210093 China; [3]National University of Singapore, Inst. of Matls. Rsch. & Engrg. & Dept. of Chem. Engrg. 117602 Singapore

Organic and polymer light-emitting devices (OLED and PLED) have brought about much activation in the area of electroluminescence (EL) and commercial displays. Efficient polymer light-emitting electrochemical cell (LEC) provides a new direction for use in flat-panel, full-color displays. However, the device performances still need to be improved. Since fast response speed is essential for LEC-type devices to find practical applications in large-area dynamic displays, research work in this aspect is important and meaningful. Also, achievement of color tunability in light-emitting devices is important for multicolor or full- color displays and various approaches for LED development have been tired. In the paper, two types of novel efficient, fast response and color-tunable polymer light-emitting cells based unique materials are designed, fabricated and characterized. A single-layer, single-ion transport light-emitting electrochemical cell (SLEC), ITO/MEH-PPV+SIC/Al, fabricated using the blend composite of MEH-PPV and polymer single-ion conductor (SIC), is the first LEC-type device that can be driven by ac (alternating-current) input voltage indicating its fast response speed. The fast light-emitting response of the SLEC was attributed to the single-ion transport property of the device. Because of the easy migration of the cations under the influence of the external electric field, the electron injection from the cathode to the luminescent polymer (with low electronic affinity) was enhanced quickly. The experimental results demonstrate that compared with the ionic conductivity, the transport mode of the ionic species is a more sensitive factor that dictates the response speed of LECs. A color-shifting phenomenon was also observed in the SLEC, the EL spectrum was greatly blue-shifted and expended (from orange to whitish). It possibly resulted from the interaction between naked and immobilized SO3- in the bulk of the polymer layer and the excitons in MEH-PPV. A bilayer, voltage controlled two-color, fast response light-emitting electrochemical cell has been successfully demonstrated. This two-color LEC consists of a poly[(2,5-bis(triethoxy)-1,4-phenylenevinylene)] (BTEO-PPV) layer and a poly[(2,5-bis(triethoxy)-1,4-phenylenevinylene)-alt-(1,4-phenylenevinylene)] (BTEOPPV-alt- PPV) layer, sandwiched between two electrodes. Due to the asymmetry of electron and hole injection and transport, the dynamic light-emitting p-n junction is closer to one of the electrodes (the cathode). Therefore, when the electrode at the BTEO-PPV side is wired as negative, the LEC emits the orange-red light from the BTEOPPV layer. On the other hand, when the electrode of the BTEOPPValt-PPV side is wired as negative, the bilayer LEC emits the yellow-green light of BTEOPPV-alt- PPV. The two distinct emission colors are identical to the EL colors obtained from single-layer LECs made from BTEO-PPV and BTEOPPV-alt- PPV, respectively. This is an indication that the light-emitting p-n junction of this bilayer device is completely within one polymer layer, and the width of the junction is less than the thickness of that polymer layer. The voltage-controlled two color light-emitting electrochemical cell is a novel light-emitting device which emits two completely different colors of light, and the two color LECs offer an important control of color and brightness: the color is controlled by the polarity and the brightness is controlled by the magnitude of the driving voltage. Also, finer phase morphology and rapid, effective transport of the ions during electrochemical doping result in faster turn-on response, and thereby extend the potential applications of polymer LECs to large-area, high pixel density, column-row addressable flat panel displays.

9:20 AM

Q4, Hall Effect Measurement of Low Mobility Organic Semiconductors: *Jeffery Robert Lindemuth*[1]; Qingye Zhou[2]; Karen Mulfor[2]; Jae Ryu[2]; [1]Lakeshore Cryotonics, 575 McCorkel Blvd., Westerville, OH 43021 USA; [2]Elecon Inc., 200 Turnpike Rd., Chelmsford, MA 01824 USA

Measuring the Hall coefficient and resistivity of low mobility material requires special care due to relatively low signal-to-noise ratios. Hall measurements for emerging organic semiconductor materials are especially difficult because of a lack of good ohmic contacts and high density of active traps, which greatly affect on the Hall coefficient. We have made dc and ac current Hall measurements on thin film samples of organic solvent based polythiophene derivatives. We will also compare these results with double ac Hall, that is both ac current and ac magnetic field on the same samples, to investigate non-ohmic and electrically active trap effects in the Hall measurements. The quality of the contact to the material was found to be very important to generate reproducable results. In this research, the contact quality is measured by two methods. The first is analyzing two terminal dc I-V characteristics. The second is to measure the resistivity and Hall coefficient at different drive currents. Furthermore, relatively high temperature dependence of the resistivity and hall coefficient of these samples requires precise temperature stability during the measurement as well as good field stability. The measurements we present here were conducted using a superconducting magnet system with temperature drifts of less than 10mK/min at 300K. Standard methods of measuring resistivity and Hall coefficient on van der Pauw samples were used. In addition, field reversal (in the dc field case), current reversal (in the dc current cases) and geometry averaging techniques are employed. By employing these techniques, we have successfully measured the mobility of the organic semiconductors, as high as 20 cm2/V.S. for both n-type and p-type materials in air. We will further address important testing parameters to be considered in van der Pauw/ Hall effect measurements of highly disordered organic semiconductor materials with the test results.

9:40 AM

Q5, Bias-Stress Effects in Polythiophene and Polyfluorene Thin-Film Transistors: *Alberto Salleo*[1]; Robert A. Street[1]; Michael L. Chabinyc[1]; Kateri E. Paul[1]; William S. Wong[1]; Raj B. Apte[1]; Beng S. Ong[2]; Yiliang Wu[2]; [1]Palo Alto Research Center, 3333 Coyote Hill Rd., Palo Alto, CA 94304 USA; [2]Xerox Research Centre of Canada, Mississauga, Ontario Canada

As the carrier mobility in polymer semiconductors has steadily increased over the years, devices based on these materials appear closer to commercial realization. Mobility alone, however, does not accurately predict device performance in service conditions. For instance, bias-stress (i.e. the progressive shift of the threshold voltage V_T as the device is operated) is particularly detrimental as it introduces uncertainties in the turn-on voltage of the transistor and a reduction in output current at fixed gate and drain voltages. In this work we characterize non-ideal behavior of polymer thin film transistors (TFTs). We studied high-performance regioregular polythiophene (PT) and poly (9,9-dioctyl-fluo-

rene co-biothiophene) (F8T2) with mobility in the range 10^{-2}-10^{-1} cm^2/V.s. A variety of gate dielectric materials and surface monolayers, shown to enhance carrier mobility in these materials, were compared, and measurements were also performed as a function of temperature. Comparable bias-stress induced current reduction was observed in both semiconductors on all dielectric surfaces, from which we conclude that bias-stress is a property of the semiconductor rather than the dielectric or the dielectric/semiconductor interface. The F8T2 devices remained stressed for a few days if kept in the dark. Because of the slow recovery, a V_T shift after consecutive measurements was observed: bias-stress thus consisted simply in removing mobile carriers from the channel without affecting their mobility. Under illumination, the devices recovered within a few minutes. The spectral sensitivity of the recovery process followed the optical absorption in the polymer. The PT devices on the other hand recovered within a few seconds in the dark at room temperature. These results suggest that the stress mechanism involves charge trapping in the semiconductor. We also observe that the magnitude of the stress effect is proportional to the square of the hole concentration, and propose that the physical mechanism is the formation of bipolarons. Under this hypothesis, the differences in bias-stress kinetics can be related to the relative bipolaron stability in the two polymers with implications in terms of materials design for polymer thin-film transistors. Because the onset of bias-stress is related to the hole concentration in the channel, its consequences on device design, fabrication and operation will be discussed as well.

10:00 AM Break

10:20 AM Invited

Q6, Pentacene Thin Film Transistors: From Film Growth to Applications in Sensors: *George Malliaras*[1]; [1]Cornell University, Matls. Sci., 327 Bard Hall, Ithaca, NY 14853-1501 USA

The growth of pentacene films on oxide surfaces plays a major role in determining the device performance. A combination of synchrotron x-ray diffraction and atomic force microscopy was used to probe this interface. In-plane diffraction from films down to one monolayer thick was observed, which allowed to probe the early stages of film growth. Depositions at various substrate temperatures and deposition rates were found to yield films with crystallite sizes from hundreds of nanometers to tens of microns. The performance of these films in thin film transistors was investigated. The scaling of the transistor characteristics down to nanometer size channel lengths is discussed. Finally, applications in sensors are demonstrated.

11:00 AM

Q7, Shadow Mask Patterned Pentacene Based Transponder Circuitry: *Paul F. Baude*[1]; David Ender[1]; Chris Gerlach[1]; Tommie Wilson Kelley[1]; Michael Haase[1]; Steve Theiss[1]; Dawn Muyres[1]; Tzu Chen Lee[1]; Dennis Vogel[1]; [1]3M, EITC, 201-1N-35, St. Paul, MN 55144 USA

We present pentacene based thin film transponder circuitry powered using near field coupled rf at 125 kHz and over 6 MHz. The circuits, formed on glass and plastic substrates, were patterned entirely using laser ablated polymeric shadow masks. Each layer of the circuit was vapor coated through the shadow mask except for a dielectric surface treatment that was spun-cast and not intentionally patterned. Mobilities on the order of 1 cm2/V-sec were achieved with the surface treatment, gate lengths are 20 µm, and the design rules are 30 µm (metal line widths). The circuit consists of a clock signal generated by a 7-stage ring-oscillator, and a load modulation stage comprised of a 5-stage output buffer. We employed a novel ac powering scheme to directly power the logic circuitry with the coupled rf energy, without the use of a diode rectification stage. Eliminating the thin film diode rectification stage and using the direct ac powering allowed for the use of higher radio frequencies, simplified the fabrication process and reduced the size of the transponder considerably. Sufficient load modulation of the rf field was obtained to externally detect the transponder's clock signal, thereby illustrating the circuit's use as a simple "1-bit" identification tag. This demonstration provides the basis for more sophisticated low-cost rf transponder circuitry using organic semiconductors.

11:20 AM Student

Q8, Stability of Pentacene Based Thin Film Transistors in an Acidic Ambient: *Karthik Shankar*[1]; Jonathan Andrew Nichols[1]; Thomas Nelson Jackson[1]; [1]The Pennsylvania State University, The Dept. of Electl. Engrg., Ctr. for Thin Film Devices, 121 Electl. Engrg. E., University Park, PA 16802 USA

There is considerable interest in the use of pentacene-based organic thin film transistors (OTFTs) for low cost electronics on flexible substrates.[1] The environmental stability of pentacene based thin-film transistors is relevant to their final applications. Previously it has been reported that exposure to oxygen under illumination may degrade the performance of pentacene OTFTs.[2] Exposure to some organic solvents was found to lead to a thin film phase transition that severely degrades the mobility of pentacene based OTFTs.[3] In addition, exposure to vapors of halogens such as Bromine and Iodine can lead to doping of the pentacene with greatly increased conductivity and significantly modified crystal structure film.[4] Here we have investigated the stability of pentacene transistors to exposure to vapors of concentrated HCl. We fabricated pentacene active layer OTFTs and investigated their characteristics before and after exposure to vapors of concentrated HCl. HCl vapor treatment resulted in a large positive shift in threshold voltage (20- 30V). Field effect mobility increased by up to 35%, but on/off current ratio and subthreshold slope were degraded. Devices with silicon oxide dielectric treated with octadecyltrichlorosilane had similar large changes in threshold voltage, but reduced mobility enhancement. The stability of post-HCl-treatment device characteristic changes was examined by modest temperature thermal annealing. Annealing at 60°C for 20 minutes caused the threshold voltage to shift to slightly more positive voltages but did not significantly affect the field effect mobility. [1]Hamers, R.J., Nature, Vol 412, Aug 2001. [2]Katz, H.E., Bao, Z.and Gilat, S.L., Acc. Chem. Res. 2001, 34, 359-369. [3]Gundlach, D.J., Jackson, T.N., Schlom, D.G., and Nelson, S.F., Applied Physics Letters, vol. 74, n. 22, pp. 3302-3304, May 1999. [4]Matsuo, Y., Sasaki, S., Ikehata, S., Synthetic Metals. Vol.121, Iss.1-3, pp.1383-4,2001.

Session R: Nanoscale Fabrication and Self Assembled Systems

Thursday AM, June 26, 2003 — Room: Theatre, Location: Olpin Union Building

Session Chairs: Paul Berger, The Ohio State University, Dept. of Electl. Engrg., Columbus, OH 43210-1272 USA; Supriyo Bandyopadhyay, Virginia Commonwealth University, Dept. of Electl. Engrg., Richmond, VA 23284 USA

8:20 AM Student

R1, The Growth of GaAsN Islands on InP: *Päivi Pohjola*[1]; Teppo Hakkarainen[1]; Markku Sopanen[1]; Harri Lipsanen[1]; [1]Helsinki University of Technology, Optoelect. Lab., PO Box 3500, HUT 02015 Finland

In recent years coherently strained Stranski-Krastanow-type islands have been extensively studied. As the research has mainly focused on compressively strained material systems, less is known about tensily strained islands. A novel tensily strained material system is GaAsN on InP. Both tensile strain and adding nitrogen reduce the band gap of binary GaAs, which can lead to type-I interface. In this study, we present GaAsN islands on InP by atmospheric-pressure metalorganic vapor phase epitaxy. The effect of growth temperature, annealing, and layer thickness on the island formation is discussed. Low-temperature photoluminescence (LT-PL) results are also presented. The samples were grown on an InP (100) substrate. First, a 100-nm-thick buffer layer of InP was deposited at 610°C. After this, a nominally 6-ML-thick GaAsN layer was epitaxially grown at the temperature range of 530-610°C. The TBAs/III and the DMHy/V ratios were 2 and 0.92, respectively. Some of the samples were annealed at 610°C for 20 s before cooling down. In these samples the layer thickness was 3-6 ML. For LT-PL measurements the samples were covered with a 25-nm-thick InP layer grown at 610°C. In the buried samples the nominal layer thickness and the DMHy/V ratio were 2-6 ML and 0.81-0.92, respectively. The TBAs/III ratio was 2. The atomic force microscope (AFM) images of the samples grown at 530-610°C showed no islands at the temperatures of 530-580°C and only few islands at the temperature of 610°C. However, in the sample grown at 610°C the surface was otherwise irregular. Furthermore, the increase in

the growth temperature has been reported to result in a lower nitrogen composition in a GaAsN layer.[1] To optimize the nitrogen concentration, the layers were grown at 530°C. To improve island formation, the samples were annealed at 610°C for 20 s before cooling down. Raising the temperature resulted in island formation with critical thickness between 3 and 4 ML. The LT-PL spectra of buried nominally 2-3-ML-thick GaAsN layers showed peaks at the energies of 1.26-1.36 eV. When the deposition thickness was 4 ML or more, an intensity maximum was found at 1.05-1.1 eV. This is suggested to be due to the 3D island formation. For comparison, a nominally 6-ML-thick GaAs layer showed a broad peak with the center energy at 1.28 eV. The GaAsN islands showed an improved luminescence at a lower energy. To study the effect of adding nitrogen on the optical properties of a GaAsN layer, the DMHy/V ratio was varied between 0.81 and 0.92. As the peak energy did not move with an increasing DMHy/V ratio, a clear evidence of the trasition type could not be obtained. [1]J. Toivonen et al., J. Cryst. Growth 221, 456 (2000); A. Ougazzaden et al., Appl. Phys. Lett. 70, 2861 (1997).

8:40 AM

R2, Ultra-High Dense InGaAsN:Sb/GaAs Quantum Dot Arrays Fabricated Non-Lithographically for Long-Wavelength Optical Devices: N. Kouklin[1]; J. Liang[1]; H. Chik[1]; M. Tzolov[1]; *J. M. Xu*[1]; J. B. Heroux[2]; W. I. Wang[2]; [1]Brown University, Div. of Engrg., Box D, Providence, RI 02912 USA; [2]Columbia University, Dept. of Electl. Engrg., New York, NY 10027 USA

Novel InGaAsN/GaAs quantum well material has been drawing attention for its possible application in long wavelength communication lasers, light sources and detectors. While successful demonstrations[1] of laser diodes based on this material have been recently reported, theoretically, it is expected that semiconductor lasers based on quantum dots would exhibit superior characteristics as compared to QW lasers. However, a strict control over size uniformity, ordering and packing density of dots would be normally required for achieving the improved device performances. In this connection, InGaAsN:Sb/GaAs quantum dots were successfully fabricated non-lithographically through imprinting patterning by using anodic nanopore membrane template and subsequent reactive ion etching (RIE). In this approach a self-organized array of nanopores with through pore openings of 50 nm diameters was used to deposit a metal nanodot array on top of an MBE grown lattice matched InGaAsN:Sb/GaAs multiple quantum well. Optimized RIE was next employed to selectively etch away the unmasked regions. The resultant structure is an 3D periodic regimented array of uniform 50 nm diameter, 6.7 nm thick InGaAsN quantum dots sandwiched between GaAs layers, shown on the SEM top view image of the surface, fig. 1. While nondestructive Raman scattering employed to assess the processing damage suggests some increase of the crystalline disorders induced by RIE, the photoluminescence from the dot arrays (PL) was readily observed at room temperature, fig. 2. We suggest, that enhancement of the electron-hole wave-function overlapping in the QDs results in the improvement of the PL intensities due to a much stronger hole localization, thus explaining the observed overall high luminescence efficiency. The red shift in the dot luminescence peak position is likely attributed to the reorganization of the surface bonding. Also the broadening of the dot PL peak was the same as in the as grown QWs, further proving high size uniformity of the dots. In conclusion, this study shows that highly-ordered, uniform and spatially arranged InGaAsN:Sb/GaAs quantum dot arrays can be easily synthesized through imprinting patterning by using anodic nanopore membrane template and RIE. The PL measurements also demonstrate good quantum efficiencies in the dots, thus making them particularly attractive for applications in improved long wavelength optical devices operating at room temperatures. [1]M. Kondow, T. Kitatani, M.C. Larson, K. Nakahara, K. Uomi, H. Inoue, J. of Crystal Growth, 188, 255, (1998).

9:00 AM

R3, Well-Aligned Zinc Oxide Nanodots Array on Patterned Substrates: *Shizuo Fujita*[1]; Sang-Woo Kim[2]; Masaya Ueda[2]; Teruhisa Kotani[2]; Shigeo Fujita[2]; [1]Kyoto University, Internatl. Innovation Ctr., Yoshida-Honmachi, Sakyo, Kyoto 606-8501 Japan; [2]Kyoto University, Dept. Elect. Sci. & Engrg., Yoshida-Honmachi, Sakyo, Kyoto 606-8501 Japan

Artificial control of self-assembled formation process to achieve ordered array of semiconductor nanodots is apparently a key technology to establish novel application of nanostructures toward actual devices in the future. In this paper we report the formation of well-aligned nanodots array of zinc oxide (ZnO), whose nanostructure is promising for the appearance of unique exciton effects supported by enhanced confinement of excitons of large binding energy (60meV in bulk ZnO), on SiO_2Si substrates patterned by focused ion beam (FIB) technology. Various line-and-space patterns were formed on 50-nm thick SiO_2 on Si (111) substrates by Ga-ion etching with FIB equipment, and then ZnO nanodots were fabricated by metalorganic chemical vapor deposition (MOCVD) using diethylzinc (DEZn) and nitrous oxide (N_2O) as source precursors at 500 to 700°C. The width of the lines formed by FIB was about 300nm, which was much larger than the beam diameter (23nm) because of the charging-up of insulating substrates. However, the cross section of the lines were V-shaped, indicating that the width at the bottom of the lines was sufficiently small as <50nm. The depths of the lines were changed between 5 and 50nm, which was smaller than the thickness of SiO_2, i.e., the bottom of the lines was always composed of SiO_2. Atomic force microscope (AFM) observation apparently demonstrated the selective formation of ZnO nanodots, e.g., 100-nm in diameter and 10-nm in height, along the bottom of the line if the depth of the line was larger than 10nm. This phenomenon may be associated with preferable nucleation of ZnO on the bottom of the lines compared to on the SiO_2 surface, and/or transport of precursors migrating on the SiO_2 surface into the bottom of the lines followed by the nucleation there. Cathodluminescence (CL) study revealed the ultraviolet emission from the nanodots. Detailed structural and optical characterizations of the nanodots, as well as the various alignments on different patterns, are now going on and are to be included in the presentation.

9:20 AM Student

R4, Ordered Arrays of InGaAs Nanostructures by Selective Area Growth or Modulated Self-Assembly Using Block Copolymer Lithography: *R. R. Li*[1]; P. D. Dapkus[1]; Zoonhoon Lee[2]; S. R. Nutt[2]; M. A. Quinlan[3]; B. E. Koel[3]; M. E. Thompson[3]; C. K. Harrison[4]; P. M. Chaikin[5]; R. A. Register[6]; D. H. Adamson[7]; [1]University of Southern California, Matls. Sci. Dept., 3651 USC Wattway, VHE 309, Los Angeles, CA 90089 USA; [2]University of Southern California, Matls. Sci., 3651 USC Wattway, VHE 416, Los Angeles, CA 90089 USA; [3]University of Southern California, Chmst. Dept., Los Angeles, CA 90089 USA; [4]National Institute of Standard and Technology, Polymer Div., Gaithersburg, MD 20899 USA; [6]Princeton University, Chem. Engrg. Dept., Princeton, NJ 08544 USA; [7]Princeton Materials Institute, Princeton, NJ 08544 USA

Quantum dots (QDs) have attracted attention for their potential as the active elements in addressable arrays for nanoscale computation and memory, and as dense arrays in the active regions of optoelectronic devices such as lasers and detectors. In many cases, the anticipated applications would benefit from ordered arrays of dots and arrays of dots with higher density and better uniformity than can currently be achieved with self assembled growth techniques. In this paper, we present a novel nanofabrication technique, with which ordered arrays of InGaAs-based compound semiconductor nanostructures were produced by selective area growth (SAG) or modulated self-assembly using metalorganic chemical vapor deposition (MOCVD). This nanofabrication process begins with defining hexagonally ordered holes, 20nm in diameter, 40nm center-to-center-spacing, with a density as high as 1011/cm2, in a thin layer of SiNx film deposited on GaAs (or GaAsP) surfaces by block copolymer lithograhy.[1] The patterned SiNx films were then used as the mask for SAG of (In)(Ga)As nanostructures on the GaAs surface. The as-grown nanostructure arrays inherit the physical arrangement and dimensions of the holes patterned into the SiNx mask film. The height and the composition of the nanostructures can be flexibly controlled. GaAs and InAs nanostructure arrays fabricated this way were studied by high-resolution cross-sectional transmission electron microscopy (HR-XTEM) and ex-situ reflected high energy electron diffraction (HREED) for structural information. The nanostructures were found to be single crystals with facets. No obvious defects were found at the growth interface according to the lattice images produced by HR-XTEM. The InAs nanostructures, after removing SiNx mask film, were then overgrown by GaAs and used as strain anchors for vertically aligned self-assembled InAs islands formation. Up to two layers of self-assembled InAs islands were demonstrated. Self-assembled InAs islands fabricated this way resemble the patterned nanostructures but with slightly worse size uniformity. The uniformity of these self-assembled islands can be further improved by carefully optimizing the growth parameters. To make the self-assembled process a single step growth, the same hole pattern was transferred into a thin layer of GaAs0.64P0.36, which was grown on a GaAs surface by

MOCVD, using the patterned SiNx layer as etching mask. As in SAG, the underlying GaAs surface was exposed in the holes. The resultant surface was then used for self-assembled InAs island formation. Due to the lattice mismatch between GaAs and the grown GaAsP, InAs islands tend to form inside the holes, resulting in hexagonally ordered InAs island array. Vertical alignment of another layer of InAs islands was demonstrated. In summary, dense, ordered, uniform InAs nanostructures were fabricated by selective area growth or modulated self-assembly. This nanofabrication technique opens new possibilities in today's nanotechnology. [1]R. R. Li et al., Appl. Phys. Lett., 76, 1689-91 (2000).

9:40 AM Student

R5, Biomolecular Nanomotor Motility in SU-8 Microchannels: *Lili Jia*[1]; Samira G. Moorjani[2]; Chung-Chen S. Kuo[1]; Thomas N. Jackson[1]; William O. Hancock[2]; [1]Pennsylvania State University, Electl. Engrg., 121 EE East, University Park, PA 16802 USA; [2]Pennsylvania State University, Bioengrg., 218 Hallowell Bldg., University Park, PA 16802 USA

Kinesin is a molecular motor that moves along microtubules, providing a model system for force generation that can be exploited for developing kinesin-powered nano- and micro-machines.[1] Microtubules are 25 nm diameter cylindrical polymers of the protein tubulin and can be micron or many microns long. Kinesins bind to microtubules and use the energy of ATP hydrolysis to walk unidirectionally along these tracks at speeds of nearly 1mm/s. A key requirement for extracting useful work from this system is to attain directional movement from microtubules moving over kinesin coated surfaces. Hiratsuka, et al, used microfabricated walls of patterned SAL601 photoresist on glass to localize motility and direct microtubule movements.[2] Here, we report the use of the epoxy-based photoresist SU-8 to pattern 1.5 mm deep microchannels on glass substrates. The channels were then functionalized with kinesin motor proteins, which transported microtubules along them. The patterned SU-8 limited motility to the glass surfaces (channel bottoms) and the steep channel walls (~90°) prevented microtubules from climbing out of the channels. In contrast to other photoresists used for this purpose[2], which require e-beam or deep UV exposure, SU-8 is easily available commercially and can be patterned lithographically using near UV radiation (350-400 nm). We find that motor binding to SU-8 and glass is similar, but motor activity is at least 100-fold lower on the SU-8, perhaps because the motor proteins denature on SU-8 surfaces. We have designed microchannels with a variety of patterns to direct the movement of microtubules, including patterns designed to give unidirectional motion. We have also functionalized deposited films including metals (Au, Pd) and dielectrics (SiO2, Si3N4) with kinesin and obtained microtubule motility comparable to that on glass surfaces. These results demonstrate that microelectronic-like processing can be used to fabricate structures to confine and direct biomolecular nanomotors. [1]J. Howard, "The Movement of Kinesin along Microtubules" Annu. Rev. Physiol. 58, pp. 703-729 (1996). [2]Y. Hiratsuka, T. Tada, K. Oiwa, T. Kanayama and T. Q.P. Uyeda, "Controlling the Direction of Kinesin-Driven Microtubule Movements along Microlithographic Tracks" Biophys. J., 81, pp.1555-1561 (2001).

10:00 AM Break

10:20 AM Student

R6, Lateral Nanogaps by Vertical Processing: *Karthik Shankar*[1]; Christopher Vincent Baiocco[2]; Thomas N. Jackson[1]; [1]The Pennsylvania State University, The Dept. of Electl. Engrg., Ctr. for Thin Film Devices, 121 Electl. Engrg. E., University Park, PA 16802 USA; [2]IBM, Microelect., Hopewell Junction, NY 12533 USA

Conducting electrodes separated by nanometer-size insulators or gaps are of interest for a variety of applications including ultra-short channel length FETs and devices for molecular electronics. True nanometer-scale electrode spacing is difficult to achieve using conventional lithographic techniques (including advanced optical and electron beam lithography) and a number of unconventional methods including break junctions,[1] electromigration,[2] scanning probe lithography,[3] advanced electron beam lithography[4] and electrochemical methods[5] for ultra-small gaps have been reported. We describe a method that employs straightforward chemical-mechanical polishing (CMP) with simple, conventional microfabrication steps to fabricate electrodes separated by nanometer-size insulators or gaps. The process begins by depositing a first layer and creating an edge of some type. This can be done either by etching or by depositing using a mask technique (for example, so-called lift-off patterning). It is not essential that the edge profile be vertical. Next a separation layer is deposited or created. This can be done by any of a variety of techniques including, evaporation, sputtering, or chemical vapor deposition, and can easily be controlled to nanometer dimension. The separation layer can be either conformal (same thickness everywhere) or non-conformal (different thickness in different regions). Next a third layer is deposited. Finally, CMP is used to remove the excess third layer to create the lateral nanostructure. Small area lateral nanostructures can then be completed by using conventional lithography to limit pattern the nanogap. For electrodes with nanometer gaps metals are used for the first and third layers and can be chosen for convenience in CMP. Using platinum and gold as the first and third layers, respectively, with aluminum oxide as the separation layer, we have fabricated nanogaps as small as about 6.5 nm. 2 micron wide 15 nm nanogaps are obtained at high yield (> 80%), limited by metal smearing during the CMP step. [1]M. A. Reed, C. Zhou, C. J. Muller, T. P. Burgin and J. M. Tour, "Conductance of a Molecular Junction", Science 278, 252-254 (1997). [2]H. Park, A.K.L. Lim, J. Park, A.P. Alivisatos, and P.L. McEuen "Fabrication of metallic electrodes with nanometer separation by electromigration", Appl. Phys. Lett. 75, 301 (1999). [3]T. Miyazaki, K. Kobayashi, T. Horiuchi, H.Yamada, K. Matsushige, "Fabrication of a nanogap on a metal nanowire using scanning probe lithography", Japanese Journal of Applied Physics (Part 1), 40(6B), 4365-7 (2001). [4]A. Bezryadina and C. Dekker, "Nanofabrication of electrodes with sub-5 nm spacing for transport experiments on single molecules and metal clusters", J. Vac. Sci. Technol. B 15(4), 793-799 (1997). [5]S. Boussaad and N.J.Tao, "Atom-size gaps and contacts between electrodes fabricated with a self-terminated electrochemical method", Applied Physics Letters, 80(13), 2398-400 (2002)..

10:40 AM Student

R7, 30-nm Period Gratings in Hydrogen Silsesquioxane Resist Fabricated by Electron-Beam Lithography: *Michael J. Word*[1]; Ilesanmi Adesida[1]; Paul R. Berger[2]; [1]University of Illinois at Urbana-Champaign, Dept. of Electl. & Compu. Engrg., 319 Micro & Nanotech. Lab., 208 N. Wright St., Urbana, IL 61801 USA; [2]The Ohio State University, Dept. of Electl. Engrg., 205 Dreese Lab., 2015 Neil Ave., Columbus, OH 43210 USA

Hydrogen silsesquioxane (HSQ) is a low-k dielectric with small molecular size that has been shown to be an effective high-resolution electron beam resist. Single isolated lines of less than 10 nm linewidth and grating patterns of 40 nm-periodicities with line/space ratio of 1:1 have been demonstrated in HSQ. The grating patterns were fabricated in very thin (30 nm-thick) HSQ films using 100 kV incident electron beam probe. There has been speculation that HSQ may provide a means of achieving grating structures with periodicities equal or better than the 32 nm NiAu metal lines that have been achieved using lift-off methods with thin films of polymethyl methacrylate (PMMA) resist. In this work, we have characterized thin HSQ films with atomic force microscopy (AFM). We have also investigated linewidths of isolated lines and the linewidths and periods of grating patterns using electron beam lithography. Our experiments were conducted in a JEOL 6000 FS at a beam energy of 50 kV, beam diameter of ~5 nm, and beam current of 20 pA. Using AFM tips with diameters down to 2 nm, we have determined that HSQ films as thin as 25 nm spun on silicon are morphologically smooth and essentially pin-hole free. With electron beam lithography, we have demonstrated lines as small as 6 nm in linewidth and grating structures with 30 nm-period. The grating period achieved represents the smallest demonstrated to date using conventional electron beam lithography. Results of linewidths for various period gratings will be presented and the writing strategy utilized to obtain these results will be discussed.

11:00 AM

R8, Pulsed Laser Annealing of Self-Organized InAs/GaAs Quantum Dots: *Subhananda Chakrabarti*[1]; Kaveh Moazzami[1]; Sasan Fathpour[1]; Pallab Kumar Bhattacharya[1]; Jamie D. Phillips[1]; Yuanyuan Lei[2]; Nigel Browning[2]; [1]University of Michigan, EECS, 1301 Beal Ave., Ann Arbor, MI 48109 USA; [2]University of Illinois, Physics, Chicago, IL 60607-7059 USA

Post-growth annealing of self-organized quantum dots (QD) has been studied previously with the goal of achieving improved size distribution, near zero-dimensional behavior, and enhanced optical and electrical properties. Conventional furnace or rapid thermal annealing (RTA) of these structures results in In-Ga interdiffusion, changing the QD size and shape. The associated modification of the electron and hole bound state energies presents problems for optoelectronic device applications targeting specific operating wavelengths. Pulsed laser annealing (PLA) with conventional excimer lasers may provide an attractive technique of an-

nealing quantum dots due to the short time scale of the laser pulses (~20ns). In this work, we have examined the optical and structural properties of self-organized InAs/GaAs QD annealed by pulsed laser annealing. The photoluminescence spectra and intersubband absorption spectra were measured for a series of annealing conditions in the context of application to quantum dot surface-emitting lasers and infrared photodetectors. The results have been compared with those obtained by RTA. A series of self-organized InAs/GaAs QD structures, designed for optical studies were grown by molecular beam epitaxy. The heterostructures had between 5 to 20 InAs QD layers, separated by 500Å GaAs barriers. The dot samples were annealed using an excimer laser at a wavelength of 248nm, pulse width of 20ns, and several pulse energies up to 400 mJ/cm^2. Heat flow calculations were performed for the annealing parameters and laser conditions to estimate the temperature profiles as a function of time and depth in the material. Photoluminescence (PL) spectra of samples annealed by PLA show a clear increase in peak intensity and integrated intensity for laser pulse energies of up to 270 mJ/cm^2, followed by a decrease for higher pulse energies. A factor of five improvement in the integrated intensity is observed for PLA, with no significant shift in peak spectral position or change in linewidth. We estimate that the reduction in PL intensity at higher fluences corresponds to the QD layers reaching temperatures near or above the melting point. Cross-sectional TEM studies indicate that the QD shape and size do not change with PLA. We observe similar behavior in intraband optical absorption studies on separate QD samples, where PLA shows an increase in absorption with insignificant change in spectral shape and peak energy position. In comparison, samples annealed by RTA show a clear blue shift of 50-110 meV in PL peak energy with increasing temperature, a reduction in PL linewidth of 10-30 meV, and a decrease in integrated PL intensity. We believe that differences in In-Ga interdiffusion and annealing behavior of defects during PLA and RTA distinguish the optical properties between the two cases. Results from experiments to verify this will be presented and discussed, together with application to devices. Work supported by ARO (MURI program).

11:20 AM Student

R9, A Systematic Study of SiGe Quantum Fortresses and Possible Applications to Quantum Cellular Automata: *Thomas E. Vandervelde*[1]; Piyush Kumar[2]; Takeshi Kobayashi[2]; Jennifer L. Gray[3]; Timothy L. Pernell[2]; Robert Hull[3]; John C. Bean[2]; [1]University of Virginia, Dept. of Physics, 382 McCormick Rd., Charlottesville, VA 22904 USA; [2]University of Virginia, Electl. & Compu. Engrg. Dept., 351 McCormick Rd., Charlottesville, VA 22904 USA; [3]University of Virginia, Matl. Sci. Dept., 116 Engineers Way, Charlottesville, VA 22904 USA

In this study we detail conditions that result in the generation and evolution of novel hetero-epitaxial surface structures in SiGe/Si created either by spontaneous self-assembly or by ion beam seeding. These self-assembled structures strongly resemble the proposed parameters for a Quantum Cellular Automata (QCA) unit cell. Specifically, we define the growth conditions (i.e. temperature, epi-layer thickness, Ge concentration, and growth rate) under which self-assembly of strain-stabilized quantum fortresses (QFs), quantum quadruplets (Q-Quads), and their precursors form. QFs are a more evolved version of Q-Quads, which consist of 4 small quantum dots (Q-Dots) clustered around a central square pit, one per side, where the individual islands have elongated laterally into rectangular walls on each side of the pit. This growth progression can be dissected into a series of surface features that evolve before and after the appearance of the above structures (e.g. <501> faceted pits and ridge-like constructions, respectively), each of which holds merit for potential technological applications. These kinetically limited configurations exist over a wide range of growth conditions, however they are destabilized by excessive adatom surface mobility or strain relaxation resulting from the introduction of misfit dislocations. To better characterize these self-assembled structures and their destabilization, we have systematically studied and are basing simulations on their basic parameters, including how their spacing, vertical, lateral, and angular dimensions change within this functional space. In addition to these simple array structures, the appearance of more unusual structures will also be discussed, including QFs that have undergone a coalescence process and multi-walled fortresses. The natural 4-fold symmetry of these structures holds great promise for future technological applications the exploration of interesting physics. One such natural application would be to use QFs in QCA based architectures. A fully developed QCA circuit requires arrays of QF-like structures, but nature only provides us with isolated randomly located QFs. To overcome this limitation we also report work directed at a guided self-assembly technique that relies on gently altering the substrate before growth. This is achieved using a 25 KeV in-situ Ga$^+$ focused ion beam to locally enhance Ga$^+$ concentration and alter the substrate's surface topography. The intent is to use the surfactant-like nature of low Ga doses, to cause local nucleation of Ge clusters without greatly disturbing surface topology. We also explore the effects of higher Ga$^+$ dosages, which cause the appearance of significant surface topology, on the localization of Ge cluster nucleation. This work, in part, was supported by NSF through FRG and MRSEC grants.

11:40 AM

R10, Morphological Evolution of $Si_{1-x}Ge_x$ Films Grown on Intentionally Pitted Si(100) Surfaces Using Molecular Beam Epitaxy: Qingfang Yao[1]; *Douglas Swenson*[1]; [1]Michigan Technological University, Dept. of Matls. Sci. & Engrg., 1400 Townsend Dr., Houghton, MI 49931 USA

Many potential applications of quantum nanostructures require that the structures adopt specific spatial configuration with respect to each other. One example of such an application is the quantum cellular automata (QCA) computing paradigm. The basic unit of this computational architecture comprises four semiconducting quantum dots arranged in a nanometer-scale square array. Here, we describe some recent work in which self-assembly of Si1-xGex thin films, grown by molecular beam epitaxy (MBE) on Si(100), leads to the spontaneous creation of these QCA "building blocks". This is accomplished by a three step fabrication procedure: codeposition of C and Si on the Si substrate, followed by Si buffer layer growth and ending with the codeposition of Si1-xGex at a substrate temperature of 550°C. The co-deposited C and Si form small (~ 1 nm high, ~ 20 nm diameter) discrete particles, which are probably b-SiC, on the substrate surface. Subsequent Si buffer layer growth leads to the formation of {105}-faceted pits, with square openings whose edges lie along <110> directions of the buffer layer surface. The pits are associated with the Si-C particles that lie under the layer; for a very thin buffer layer, the areal density of pits is the same as that of the SiC particles on the substrate surface prior to growth. Continued buffer layer growth leads to a reduction in areal density and an increase in size of the pits. In the final step, six Si1-xGex film compositions, ranging from 0.33 x 0.80, were codeposited on the pitted Si buffer layers. A series of related, self-assembled nanostructures was observed, ranging from: low domes that filled in the buffer layer pits (x = 0.33); to {105}-faceted pyramids which also filled in the pits (x = 0.4-0.5); to {105}-faceted pyramids that grew upward from the bottoms of the pits, but left large gaps between themselves and the pit walls (x = 0.6); to an array of four, hut-shaped islands, whose long faces were {105} facets, decorating the edges of the pits (x = 0.7); to a final configuration similar to that for x = 0.7, but in which each hut-shaped island split in two (x = 0.8). The morphology observed for the Si0.30Ge0.70 growth merits further study for possible use in QCA applications. Generally, the surface-to-volume ratios of the self-assembled structures increased progressively with increasing Ge content in the final growth layer. Overall, the evolution of observed structures may be rationalized in terms of thermodynamic arguments, where growth associated with a buffer layer pit is preferred owing to the possibility of reduced strain energy, and whereby as the strain energy associated with a Si1-xGex film increases (i.e., as x increases), the structures adopted by the Si1-xGex layers adopt progressively higher aspect ratios to relieve strain energy at the expense of creating additional surface energy by virtue of possessing greater surface areas.

Session S: High-K Dielectrics - I

Thursday AM Room: Saltair
June 26, 2003 Location: Olpin Union Building

Session Chairs: Patrick Lenahan, Pennsylvania State University, University Park, PA 16802 USA; Susanne Stemmer, University of California, Matls. Dept., Santa Barbara, CA 93106-5050 USA

8:20 AM

S1, Atomic Layer Deposition of Metal Oxide High-k Gate Dielectrics for MOSFETs and Carbon Nanotube Transistors: *Paul C. McIntyre*[1]; Hyoungsub Kim[1]; Ali Javey[2]; Baylor B. Triplett[1]; Hongjie Dai[2]; Krishna C. Saraswat[4]; [1]Stanford University, Matls. Sci. & Engrg., Rm. 243, McCullough Bldg., 476 Lomita Mall, Stanford, CA 94305-4045 USA; [2]Stanford University, Chmst., 476 Lomita Mall, Stanford, CA 94305-4045 USA; [4]Stanford, Electl. Engrg., CISX Bldg., Stanford, CA 94305 USA

Atomic layer deposition (ALD) is a versatile method of film growth that can be used to deposit a wide array of metals, metal oxides, and other inorganic thin films with sub-nanometer precision and near-perfect conformality over rough surface topography. These characteristics result from the layer-by-layer adsorption mechanism that is a defining attribute of ALD. In this presentation, the dielectric properties and structure of HfO2 gate dielectrics prepared by ALD on SiO2-passivated Si (100) substrates are reviewed. Results of detailed studies of HfO2 crystallization kinetics via transmission electron microscopy (TEM) and electrical characterization are presented. Ge-based semiconductor channels, which can be readily integrated on large-area Si wafers, are of interest for future-generation MOS devices because of germanium's high thermal mobilities for both holes and electrons. ALD synthesis of ZrO2 and HfO2 gate dielectrics on (100) Ge substrates is reported. The poor thermodynamic stability of GeO2 may avoid growth of an undesirable low-?Û oxide interface layer under the deposition conditions used to form the metal oxide high-?Û gate dielectric, in contrast to the typical situation for high-?Û deposition on Si. ALD growth of ZrO2 onto vapor-HF treated (100) Ge substrates from ZrCl4 precursors at 300?aC was found to produce an epitaxial gate dielectric. A <100> (100) ZrO2//<100> (100) Ge orientation relationship was observed over a large area fraction of the dielectric film. However, the large (~ 10%) lattice mismatch between the film and substrate resulted in the formation of a very high density of near-interface misfit dislocations. These defects may be responsible for the significant stretch out of the CV curves measured from shadow mask-defined Pt/ALD-ZrO2/Ge MOSCAPs. Prospects for ALD growth of alternative metal oxides with closer lattice matching to Ge (100) will be discussed. Preliminary data obtained from ALD-HfO2 gate dielectrics deposited onto Ge (100) substrates are reported. Finally, ALD growth of metal oxide gate dielectrics onto semiconducting single-wall carbon nanotube transistor structures is described, with emphasis on the nature of atomic layer deposition onto the nanotube surface and the resulting effects on device characteristics.

9:00 AM Student

S2, Charge Trapping in Atomic Layer Deposited Hafnium Oxide on Silicon: *Andrew Y. Kang*[1]; Patrick M. Lenahan[1]; John F. Conley[2]; [1]The Pennsylvania State University, Dept. Engrg. Sci. & Mech., 212 EES Bldg., University Park, PA 16802 USA; [2]Sharp Labs of America, 5700 NW Pacific Rim Blvd., Camas, WA 98607 USA

Dielectric charge trapping leads to shifts in the threshold voltage and is an important reliability issue for high-k films. Several very recent studies provide strong qualitative evidence that negative charge trapping appears to dominate in hafnium oxide HfO_2 dielectric films. Previous work by the authors observed large numbers of electron traps in HfO_2 films flooded with charge carriers by ionizing radiation under various gate bias conditions.[1] However, interface trap generation usually associated with charge trapping in SiO_2 films under similar conditions was not observed for the HfO_2 devices.[1] Zafar et al.[2] have quite recently observed positive threshold voltage shifts in nFET devices with atomic layer deposited (ALD) HfO_2 gate dielectric material under high electric field stressing, also indicating a lack of interfacial trap generation. Zhu et al.[3] have observed positive flatband voltage shifts for jet vapor deposited HfO_2 films. We have investigated charge trapping, capture cross sections, and trap densities in ALD HfO2 gate dielectric films on silicon. Electrons and holes were injected to the dielectrics at low oxide electric fields using filtered vacuum ultra-violet irradiation ($hc/\lambda = 10eV$) with oxides biased via the corona-ion technique. The ALD films were deposited on p-type substrates using 300 cycles of alternating pulses of $Hf(NO_3)_2$ and H_2O precursors. Samples received an in-situ, post deposition anneal in N_2 at 450°C for 60 seconds. The thickness of the HfO_2 film was 25.6 nm +/- 0.2nm. No metal was deposited, no other anneals were performed, and the sample did not receive a forming gas anneal. Initial results indicate the presence of large numbers of electron traps (~$3x10^{12}$ / cm^2) with large capture cross-sections (~$2x10^{-13}$> cm^2). Although the atomic scale structure of these traps are yet unknown, theoretical work by Foster et al.[5] suggest the possible role of interstitial oxygen as electron traps in HfO_2. We have initiated electron spin resonance measurements on HfO_2 films to further explore the atomic scale structure(s) of these dielectric traps. [1]A.Y. Kang, P.M. Lenahan, and J.F. Conley, Jr., IEEE Trans Nucl. Sci. 49, 2636 (2002). [2]S. Zafar, A. Callegari, E. Gusev, M.V. Fischetti, IEDM, 517 (2002). [3]W.J. Zhu, T.P. Ma, S. Zafar, and T. Tamagawa, IEEE Electron Dev. Lett. 23, 597 (2002). [4]A.S. Foster, A.L. Shluger, and R.M. Nieminen, Phys. Rev. Lett. 89, 225901-1 (2002).

9:20 AM Student

S3, Integration and Electrical Performance of Aluminum Oxide Thin Films Deposited by Low Temperature Metal Organic Chemical Vapor Deposition (MOCVD) for CMOS Gate Dielectric Applications: *Spyridon Skordas*[1]; Filippos Papadatos[1]; Steven Consiglio[1]; Eric T. Eisenbraun[1]; Alain E. Kaloyeros[1]; [1]The University at Albany-SUNY, Sch. of NanoScis. & NanoEngrg., 251 Fuller Rd., CESTM Bldg., Albany, NY 12203 USA

The electrical performance and integration of a low-temperature metal organic chemical vapor deposition (MOCVD) aluminum oxide (Al2O3) process is discussed. The MOCVD Al2O3 process employs an aluminum â-diketonate metal organic precursor [aluminum(III) 2,4-pentanedionate] and water as the metal and oxygen sources, respectively.[1] In this work, the electrical performance of the Al2O3 films in terms of dielectric constant and leakage current density is investigated as performance relates to specific key processing parameters and post-deposition annealing sequences. Al2O3 was deposited using MOCVD over a range of processing conditions on 1.0 nm SiON / Si(100) substrates. The samples were then separated in four splits, three of these splits were subjected to the following annealing conditions: a) forming gas anneal (FGA, 90% Ar, 10% H2) at 550°C for 30 min, b) rapid thermal annealing (RTA) in N2 at 700°C for 30 s, followed by FGA at 550°C for 30 min; and, c) O2 anneal at 550°C for 30 min followed by FGA at 550°C for 30 min. Metal-insulator-semiconductor (MIS) capacitor structures were fabricated, and the stacks featuring the as-deposited and annealed Al2O3/ SiON / Si(100) substrate stacks were characterized by capacitance-voltage (C-V) and current-voltage (I-V) measurements. Those stacks exhibiting the best electrical performance were subsequently coated with MOCVD-grown ruthenium oxide dots. The work function of the gate electrode and the thermal stability of the resulting gate stack were evaluated using electrical testing (capacitance-voltage and current-voltage measurements), and high resolution transmission electron microscopy (HR-TEM) combined with energy dispersive x-ray spectrometry (EDX). [1]S. Skordas, F. Papadatos, Z. Patel, G. Nuesca, E. Eisenbraun, E. Gusev, and A. E. Kaloyeros, Mat. Res. Soc. Symp. Proc. Vol. 716, p.183 (2002).

9:40 AM

S4, Experimental and Theoretical Analysis of HfO_2 Thin Film Growth by MOCVD: A. N. Vorob'ev[1]; I. Yu. Archakov[1]; O. V. Bord[1]; *Yu. N. Makarov*[1]; M. Reinhold[2]; M. Schumacher[2]; M. Heuken[2]; [1]STR GmbH, PO Box 1207, Erlangen D-91002 Germany; [2]AIXTRON AG, Kackertstr. 15-17, Aachen D-52072 Germany

Results of experimental and theoretical study of chemical vapor deposition (CVD) of HfO_2 thin films from tetrakis-diethylamido-hafnium $\{Hf[(N(C_2H_5)]_4 : Hf(NEt_2)_4\}$ diluted in octane will be presented. Ar and O_2 are used as carrier gas and oxidizer, respectively. Thermal decomposition and oxidation of the precursor are preliminarily investigated by mass spectrometric (MS) technique in a wide range of process parameters. No considerable dependence of $Hf(NEt_2)_4$ oxidation and decomposition on total pressure is found under typical operating conditions. As it follows from measured mass spectra, the precursor oxidation and decomposition are similar for both excess and lack of oxygen. Therewith, CO_2 is the predominant decomposition product, whereas H_2O peak intensities are negligible in oxygen lack. Comparative analysis of the mass spectra obtained at various temperatures shows that $Hf(NEt_2)_4$ oxidation and decomposition are most likely to be controlled by heterogeneous reactions. The HfO_2 growth rate is studied as a function of the susceptor temperature, total pressure and precursor flow rate in a showerhead reactor. Basing on the experimental data obtained, we suggest a process model assuming an additional loss of species responsible for HfO_2 growth due to particle formation in the gas phase. This model is indirectly supported by the data presented in.[1,2,3] The model is applied to the simulation of the high-k oxide MOCVD in Tricent® reactors. [1]Ohshita Y., Ogura A., Hoshina A., Hiira S., Machida H., J.Cryst.Growth, 233, 2001, P.292. [2]Yun J.-Y., Park M.-Y., Rhee Sh.-W., J.Electrochem. Soc., 146 (5), (1999),

P. 1082. [3]Balog M., Shieber M., Michman M., Patai S., J.Electrochem.Soc., 126 (7), (1979), P.1203.

10:00 AM Break

10:20 AM Student

S5, UV-Ozone Oxidized High-k Dielectrics on Si and Ge Substrates: *David Chi*[1]; Chi On Chui[2]; Shriram Ramanathan[1]; Baylor B. Triplett[1]; Krishna Saraswat[2]; Paul C. McIntyre[1]; [1]Stanford University, Matls. Sci. & Engrg., 476 Lomita Mall, McCullough Bldg., Stanford, CA 94305 USA; [2]Stanford University, Electl. Engrg., Ctr. for Integrated Sys., Stanford, CA 94305 USA

UV-ozone oxidation has been used to fabricate ultrathin metal oxide gate dielectrics on Si and Ge semiconductor substrates.[1, 2] This technique entails depositing a metal film on the substrate by, for example, UHV sputtering or e-beam evaporation, and exposing the film to pure oxygen in the presence of ultraviolet light which creates both atomic oxygen and ozone. These highly activated oxygen species produce enhanced low temperature oxidation kinetics for the metal layer. Kinetics of Zr and Hf oxidation on oxynitride or SiO2-passivated silicon substrates has been studied using XPS, HRTEM, and NRA. The maximum oxide thickness achievable using this technique are 50 Å and 35 Å for ZrO2 and HfO2, respectively (for oxidation at room temperature in an O2 pressure of 600 Torr). This represents a significant enhancement over the limiting oxide thickness during room temperature oxidation in pure molecular oxygen at comparable pressure. Electrical results obtained from Pt-electroded MOSCAP structures fabricated on Si substrates indicate an oxide with a high dielectric constant and low leakage current density. Capacitance-derived EOT values of 15 Å have been achieved for 28 Å UV ozone oxidized ZrO2 on 10 Å SiO2. The corresponding leakage current is in the 10^{-4} A/cm^2 range.[3, 4] As a semiconductor channel material for use in future scaled MOS transistors, Ge has the advantage of enhanced low-field mobility compared to Si. With the expected introduction of deposited high-k dielectrics in MOS technology, the poor quality and stability of GeO_2 may no longer be a significant obstacle to development of Ge-channel field effect transistors. Growth of ZrO_2--based gate dielectrics on Ge (100) substrates is reported in this presentation. HRTEM of UV-ozone oxidized ZrO2 on Ge indicates a sharp interface between the oxide and the substrate. However conventional TEM is not well-suited for identifying a Ge oxide layer in this system due to the closeness in atomic number of Zr and Ge. XPS spectra suggest the presence of a substoichiometric Ge oxide phase at the ZrO2/Ge interface. Depth profiling using angle-resolved XPS and MEIS have been performed on multiple ZrO_2Ge gate stacks. Results indicate that the thickness of the Ge oxide layer is dependent upon the ZrO_2 overlayer thickness, suggesting that the interfacial layer can be controlled through the oxidation conditions. Electrical testing results obtained from ZrO_2Ge MOSCAPS and MOSFET devices will be summarized. A systematic comparison of UV-ozone oxidized dielectrics grown upon Si and Ge will be presented. Key differences including oxidation kinetics and electrical properties will be highlighted. [1]S. Ramanthan et al, Appl. Phys. Lett. 79, 2621-23 (2001). [2]C.O. Chiu et al, IEEE Electron Dev. Lett. 23, 473-75 (2002). [3]S. Ramanathan and P.C. McIntyre, Appl. Phys. Lett. 80, 3793-95 (2002). [4]S. Ramanathan, et al, J. Appl. Phys. 91, 4521-27 (2002).

10:40 AM

S6, Modeling of the Accumulation Capacitance in the Case of High-K Gate Dielectrics: *Samares Kar*[1]; [1]Indian Institute of Technology, Dept. of Electl. Engrg., Kanpur, Uttar Pradesh 208016 India

A new approach, which is simple and therefore facilitates efficient (in terms of time and effort) calculations, is proposed for mathematical representation in closed form of the accumulation capacitance of MIS (Metal-Insulator-Semiconductor) structures having high-K(high dielectric constant) materials as the gate dielectric. This representation has been shown to be very useful in accurately extracting the gate dielectric capacitance, C_{di}, the quantization index, β, the surface potential against the applied bias, φ_s(V), and the interface trap density, D_{it}, near the majority carrier band edge. Usually, the MIS capacitance-voltage (C-V) characteristic is modeled, by a simultaneous solution of the Poisson's and Schroedinger's equations. Many assumptions are made in such a model, that typically include: (1) The interface trap capacitance, C_{it}, is negligible in strong accumulation at 100 kHz/1 MHz. (2) The interface trap charge density is negligible in strong accumulation. (3) The bulk gate dielectric trap charge density, Q_{bt}, is negligible. (4) An infinite potential barrier is assumed at the silicon/dielectric interface. There can be justifiable concerns regarding each of these assumptions: (1) The interface and the bulk dielectric trap densities are high in the case of high-K gate dielectrics. Further, D_{it} can be much higher near the band edges than at midgap, and the corresponding Q_{it} can be too large in accumulation to neglect. It can be easily shown that the interface traps are likely to follow the 1 MHz ac signal in accumulation, and hence, the interface trap capacitance, C_{it}, cannot be neglected. (2) Assumption, of an infinite potential barrier at the interface, is questionable, as the conductance and valence band offsets are in many cases around 2 eV or even less. (3) In the case of gate dielectric stacks/laminates and mixed gate dielectrics, determination of the physical parameters (necessary for calculating C_{di}) will be difficult. The only assumption made in the proposed approach is that both the space charge and the interface trap capacitances are exponential functions of $\beta\varphi_s$, where φ_s is the surface potential. The validity of the proposed approach was confirmed experimentally by applying to different high-K gate dielectrics with varying band offsets and equivalent oxide thickness (EOT varying between 0.48 and 1.5 nm). The experimental $(C^{-1}dC/dV)^{1/2}$ versus C, C^{-1} versus $(dC^{-2}/dV)^{1/2}$, and ln C_p ($C_p = C_{sc} + C_{it}$) versus φ_s were consistently very linear without any exception. Values of C_{di} and the constant β were obtained from the slopes of these linear plots. The ratio $(\beta)/(\beta_{classical})$ ($\beta_{classical} = q/2kT$) can be considered to reflect the extent of quantization. The experimental φ_s versus bias for the accumulation regime was obtained by integration of $(1\text{-}C/C_{di})$ with respect to V. The interface trap density D_{it} and capture cross-section versus energy were obtained from the conductance-frequency-voltage data.

11:00 AM Student

S7, Development of Hybrid TiAlOx Layer as a Novel High-k Gate Oxide: Wei Fan[1]; Sanjib Saha[1]; John A. Carlisle[1]; R. P.H. Chang[2]; *Orlando Auciello*[1]; [1]Argonne National Laboratory, Matls. Sci., 9700 S. Cass Ave., Argonne, IL 60439 USA; [2]Northwestern University, Matls. Sci. & Engrg., 2220 N. Campus Dr., Evanston, IL 60208 USA

According to the technology roadmap for the semiconductor industry, alternative gate oxides with equivalent oxide thickness (EOT) of less than 1.5 nm are critical to satisfy the requirements of sub-100 nm MOSFET devices. Among high-k metal oxides, TiO_2 has attracted much interest because of its high dielectric constant (>50). However, the use of TiO_2 thin films as gate dielectric was hampered primarily due to its high leakage current. On the other hand, intensive studies have been carried out on Al_2O_3, due to its large band gap (8.8 eV) and thermodynamic compatibility with Si. However, Al_2O_3 exhibits a relatively low dielectric constant compared with other current leading high-k gate oxides. Therefore, we determined that a hybrid structure including Al_2O_3 and TiO_2 might create a novel material with high dielectric constant, low tunneling current, and relatively high band gap (US patent pending). We present here our latest results on investigating $TiAlO_x$ as an alternative gate oxide material for CMOS devices. Ultra-thin TiAl films were grown on n-Si (100) by sputter deposition with a physical thickness of 5-20 nm. In-situ oxidation was then performed by using both molecular oxygen (P=$1.0x10^{-3}$ Torr) and atomic oxygen sources (P=$1.0x10^{-4}$ Torr). The formed $TiAlO_x$ exhibited amorphous structure, as revealed by XRD and TEM analysis. XPS spectrum clearly showed that a full oxidation of TiAl was achieved at 500°C using both oxygen sources. However, the $TiAlO_x$ layer formed through atomic oxygen annealing presented a leakage current 150 times lower than the one with molecular oxygen annealing. The high reactivity of O atoms, rather than O_2 molecules, is expected to reduce the oxygen deficiency within the $TiAlO_x$ layer, which contributes to the dielectric leakage. Since both Ti and Al have more negative oxide formation energies than Si, the presence of Ti and Al atinterface with Si greatly reduces the formation of interfacial SiO_x. This has been confirmed by in-situ XPS depth profile, which showed only a small signal of Si^{4+} state at the oxide/semiconductor interface. The amorphous $TiAlO_x$ layer exhibited high permittivity (~30), which was much larger than SiO2 (ε_r=3.9) and Al_2O_3 (ε_r=9). The leakage current density of the $TiAlO_x$ layer formed via atomic oxygen exposure was about $1.2x10^{-2}$ A/cm^2 with EOT of 1.5 nm and negligible hysteresis. After post deposition annealing with the top gate electrode in place, the leakage was further improved and reached $3.8x10^{-6}$ A/cm^2, which is ~10^6 times lower than thermal SiO_2 with the same EOT. These results demonstrate that $TiAlO_x$, the hybrid oxide layer developed by us, provides a good alternative gate oxide to meet the requirements of sub-100nm MOSFET devices. This work was supported by the US Department of Energy, BES-Materials Sciences, under Contract W-31-109-ENG-38.

11:20 AM Student

S8, Improved Electrical Properties of SONOS-Type Flash Memory Using High-k Dielectric as Charge Trapping Layer and Blocking Layer: *Sangmoo Choi*[1]; Hyunsang Hwang[1]; Myungjun Cho[1]; [1]Kwangju Institute of Science & Engineering, Dept. of Matls. Sci., 1 Oryong, Puk-Gu, Kwangju 500-712 Korea

SONOS-type flash memory based on localized charge storage in charge trapping layer (Si3N4) has been investigated because of its better scalability, endurance and less power consumption. It is known that the high-k gate dielectrics such as HfO2 and Al2O3 exhibit a significantly lower leakage current density than those of SiO2, and Si3N4 at the same equivalent oxide thickness. By using high-k materials as an alternative to blocking oxide and trapping layer, both the fast write/erase speed and long data retention can be obtained. In this paper, we report on the improved electrical properties of SONOS-type flash memory using high-k materials, such as Al2O3 and HfO2, as a blocking oxide and trapping layer. To investigate the effect high-k blocking oxide, Al2O3 layer was deposited on SiO2/SiN stack using RF magnetron sputtering. For comparison, HfO2 layer was also deposited on SiO2/SiN as a blocking layer. To understand the impact of high-k trapping layer as an alternative to Si3N4, HfO2 was deposited as a trapping layer on top of tunneling SiO2, followed by Al2O3 as a blocking layer. MOS capacitors with 150nm-thick Pt-electrode were fabricated. Compared with conventional ONO stack, the improved write/erase speed was accomplished by using Al2O3 and HfO2 as alternatives to blocking oxide. Although the SiO2 tunnel oxide thickness was thicker than 3nm, SiO2/SiN/Al2O3 (ONA) stack shows the flat-band voltage shift of 2V at the conventional stress condition (write: Vg= +8V for 1ms, erase: Vg= -8V for 1ms). The extrapolated memory window after 10 years was more than 1.5V. In case of SiO2/SiN/HfO2 (ONH) stack, the observed write speed was higher than that of ONA stack. The enhanced retention characteristics of erased cell were also observed. However, the observed memory window of ONH was smaller than that of ONA due to the lower conduction band offset of HfO2. To avoid this problem, the SiO2/SiN/Al2O3/HfO2 (ONAH) stack was also prepared to obtain higher write/erase speed and longer data retention. We also investigated the electrical properties of SiO2/HfO2/Al2O3 (OHA) stack to obtain better write/erase speed with large memory window. The flat-band voltage shift of more than 2.5V was obtained (write: Vg= +8V for 1ms, erase: Vg= -8V for 1ms). The extrapolated memory window after 10 years is more than 1V. We also found excellent retention characteristic of OHA stack layer using lanthanide doped HfO2 layer. In summary, we have investigated the effect of high-k dielectric on electrical characteristics of SONOS type memory device. An excellent programming/erase speed and retention characteristics were obtained by using high-k dielectric for blocking oxide and trapping layer. Acknowledgment: This work was supported by Tera-level Nano Device Project.

11:40 AM

S9, Aluminum Oxide Layers as Potential Components for Crested Tunnel Barriers: *Elena Cimpoiasu*[1]; S. K. Tolpygo[1]; X. Liu[1]; N. Simonian[1]; Yu. A. Polyakov[1]; J. E. Lukens[1]; K. K. Likharev[1]; [1]SUNY Stony Brook, Physics & Astron., Stony Brook, NY 11794 USA

Theoretical results[1, 2] indicate that tunneling transparency of layered ("crested") barriers, with the potential height peaking in the middle, can be more sensitive to applied voltage than that of the usual (uniform) barriers. The implementation of such barriers would enable high speed/high density nonvolatile semiconductor memory applications.[3] One of the most promising materials for crested barrier layers is aluminum oxide. Unfortunately, despite the fact that these oxides are intensively explored as potential gate dielectrics, literature gives broadly scattered data for their tunneling parameters. The goal of this work was to explore properties of thermally-grown and plasma-grown AlOx (both as-oxidized and post-annealed) as possible material for creased barrier layers. We fabricated two batches of niobium-trilayer (Nb/Al/AlOx/Nb) junctions with (a) barriers thermally grown at room temperature in 100 torr oxygen for 40 hours (b) barriers grown in rf oxygen plasma for 3 min at 100 mtorr oxygen. After fabrication, some chips from each wafer were rapid thermal annealed at 400°C for 30 s. The oxide layers where rather uniform and featured high breakdown fields (above 10 MV/cm.) Measured dc I-V curves were fitted with results of a specially developed computer program that calculates tunneling through barriers with arbitrary potential profile, with account of electron energy relaxation in the classically allowed region, and band bending due to the partial penetration of electrons under the tunnel barrier. We found that annealing leads to a substantial increase of the height and thickness of thermally grown barriers, crudely from 1.9 to 2.7 eV, and from 1.5 to 2.2 nm, respectively, and also to an increase of the average hard breakdown voltage from 1.6 to 2.6 eV. On the other hand, the plasma-grown barriers are very weakly affected by post-annealing. Using the recovered barrier parameters, we have calculated expected properties of possible crested barriers consisting of (i) a plasma-grown and a thermally-grown Al oxide, and (ii) a plasma-grown layer with SiO2. The results show that the former combination may give an increase of the floating barrier recharging time by approximately two orders of magnitude in comparison with a uniform SiO2 layer providing the same retention time. A slightly smaller improvement may be achieved for the latter option, provided that the dielectric constant of our Al2O3 layers is closer to 5 [4] than to the usually quoted value ~10. The generous help of X. Wang with RTA, and useful discussions with J. Cosgrove and T.-P. Ma are gratefully acknowledged. This work was supported in part by AFOSR, NRL, and ONR. [1]K. K. Likharev, Appl. Phys. Lett. 73, 2137 (1998). [2]J. D. Casperson, L. D. Bell, H. A. Atwater, J. Appl. Phys. 92, 261 (2002). [3]K. K. Likharev, IEEE Circuits and Devices 16, 16 (2000).

Session T: Contacts to Group III Nitrides

Thursday AM Room: Panorama East
June 26, 2003 Location: Olpin Union Building

Session Chairs: Suzanne Mohney, Pennsylvania State University, Dept. of Matls. Sci. & Engrg., University Park, PA 16802 USA; Timothy Sands, Purdue University, Sch. of Matl. Engrg., W. Lafayette, IN 47906 USA

8:20 AM Student

T1, Formation of Low Resistance and Transparent Ohmic Contacts to p-Type GaN using Transparent Conducting Oxides: *June O. Song*[1]; Kyoung-Kook Kim[1]; Tae-Yeon Seong[1]; [1]Kwangju Institute of Science & Technology, Dept. of Matls. Sci. & Eng., 1 Oryong-dong, Puk-gu, Gwangju 500-712 Korea

GaN-based light emitting diodes (LEDs) operating in the green, blue, and ultraviolet range of the optical spectra are of great technological importance. In order to further improve such devices, it is essential to develop highly reliable ohmic contacts to p-GaN, especially for high power LED operation. Thus, in order to fabricate high-quality ohmic contacts to p-GaN, various metallization schemes, such as Ni/Au, Pt/Ni/Au, Ni/Pt/Au and Pt/Au, have been widely investigated, among which the Ni/Au contacts are most popular. The main concept of the NiAu scheme is to oxidize Ni and to form p-type NiO with a high carrier concentration in order to reduce interfacial contact resistances. However, Au-based contacts generally have poor thermal stability, leading to poor device reliability. Thus, to improve the reliability of optical devices, transparent conducting oxide (TCO), such as indium tin oxide (ITO), has been successfully used. It was shown that the use of ITO (250 nm) is effective in improving the electrical and optical properties of ohmic contacts to p-GaN. In this work, we investigate the TCO schemes for use in forming low resistance and transparent ohmic contacts to p-GaN (5×10^{17} cm^{-3}). The electrical properties of the contacts are investigated as a function of annealing temperature, time, and ambient. The as-deposited contact shows non-ohmic behaviour. It is, however, shown that the contact schemes yield specific contact resistances as low as 6.23×10^{-6} Ωcm^2 and light transmittance higher than 76% at wavelengths in the range of 400-550 nm when annealed at 400-550°C for 2-5 min in air ambient. Based on the results obtained from x-ray photoemission spectroscopy and Auger electron spectroscopy examinations, ohmic formation mechanisms for the oxidized contacts are described and discussed.

8:40 AM

T2, Effects of Oxidation of Ni/Pt and Ni/Pt/Au p-Contacts on Performance of InGaN/GaN Multiple-Quantum Well Light-Emitting Diodes: *Chul Huh*[1]; William J. Schaff[1]; Lester F. Eastman[1]; Seong-Ju Park[2]; [1]Cornell

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High-quality and uniform metal contact to nitride semiconductors is one of key factors to realize high performance nitride-based optoelectronic devices as well as high-quality film growth. Especially, low-resistance ohmic contacts to p-type GaN are crucial to improve the performance of light-emitting diodes and laser diodes as well as electronic devices. Because of the difficulty to obtain high hole concentrations in p-type GaN and the absence of a metal with a sufficiently high work function compared to the work function of p-type GaN (sum of the band gap and electron affinity), a low-resistance ohmic contact to p-type GaN is difficult to achieve. An interesting method for lowering the contact resistivity is the oxidation of metal film on p-type GaN surface by annealing in oxygen or air environment instead of nitrogen ambient commonly used. It was reported that a low specific resistance with high transparency was obtained by oxidizing a Ni/Au film on p-type GaN due to the formation of p-NiO. In this study, the effects of oxidation of Ni/Pt and Ni/Pt/Au p-contacts on electrical and optical performance of InGaN/GaN multi-quantum well light-emitting diodes were investigated. For LEDs with oxidized Ni/Pt/Au p-contact, the forward current-voltage characteristics and light-output performance of LEDs were enhanced compared to those of LEDs with Ni/Pt/Au p-contact annealed in nitrogen ambient. Moreover, the leakage current under reverse voltage was also suppressed. This can be attributed to the surface and side wall passivation by oxygen. In case of Ni/Pt contact, on the other hand, for LEDs with oxidized contact, the electrical and light-putput performance was almost same as that of LEDs with contact annealed in nitrogen ambient. It was found that, for both cases of Ni/Pt and Ni/Pt/Au contacts, NiO phase was formed after annealing in air environment, which was confirmed by using X-ray diffraction technique. However, NiO phase formed resulted in a different effect on ohmic contact to p-type GaN in both cases. This difference might be due to the existence of Au overlayer on Ni/Pt metal film.

9:00 AM Student

T3, Surface Treatment of n-GaN for Ohmic Contact Formation: *Deepak Selvanathan*[1]; Vipan Kumar[1]; Ilesanmi Adesida[1]; [1]University of Illinois, Micro & Nanotech. Lab., 319 MNTL, 208 N. Wright St., Urbana, IL 61801 USA

The III-V nitride wide-band-gap direct semiconductors have been used to fabricate blue LEDs, laser diodes and high-power electronic devices. Recent developments in the crystal quality have enhanced the importance of the GaN devices for optoelectronic as well as high temperature electronic applications. Besides good quality material, device technology requires low resistive, thermally stable ohmic contacts to achieve high performance GaN-based devices. Several reports have been published on surface treatment on AlGaN/GaN layers prior to metallization to improve the ohmic characteristics of the contacts. These treatments include immersing the layers in various etchants such as Buffered Oxide Etch (BOE), NH_4OH and HCl heated to very high temperatures. However, many of these techniques are not compatible with device fabrication steps, as the photoresist cannot withstand such harsh conditions. In this work, we present surface treatment techniques on n-GaN that are compatible with device processing steps. In this paper, we study the surface of the n-GaN layers after $SiCl_4$ plasma treatment and then cleaned in various etchants such as NH_4OH, HCl and BOE kept at ambient temperature for 2 min. From the XPS measurements, we find the O 1s peak intensity is minimum in the sample treated with BOE. The sample treated with $SiCl_4$ plasma exhibits higher O/N ratio when compared with that seen in the as-grown sample indicating an increase in oxide at the surface after plasma treatment. This can be attributed to the creation of N vacancies during the plasma treatment and the substitution of O in these sites. The O/N ratio is increased in the sample treated with NH_4OH while it decreases in the sample treated with HCl. Also in the $SiCl_4$ plasma treated samples, Ga 3d peak shows a peak shift of about 0.2 eV towards higher binding energies. This indicates a shift of the Fermi level towards conduction band at the surface thereby increasing the electron concentration at the surface. Hence BOE is the most suitable etchant to remove the native oxide from the surface of n-GaN layers. To study the rate of oxide re-growth on the n-GaN layers after surface cleaning, $SiCl_4$ plasma treated samples were cleaned in BOE for 2 min and then were left exposed to ambient atmosphere. The sample surfaces were characterized using XPS and the results indicate a O/N ratio increased from 0.12 in the sample cleaned in BOE to a value of 0.29 in the sample that was cleaned in BOE and then exposed to ambient atmosphere for 24 h. Comprehensive results will be presented on the efficiency of the various surface treatments and also the mechanism of various surface treatments will be discussed.

9:20 AM Student

T4, The Study of n-Ohmic Contact in III-Nitride Semiconductor for High Temperature Applications with the Use of W and WSi: *Ben Luo*[1]; Brent Gila[2]; Cammy Abernathy[2]; Fan Ren[1]; Stephen Pearton[2]; A. G. Baca[3]; R. D. Briggs[3]; D. Gotthold[4]; R. Birkhahn[4]; B. Peres[4]; [1]University of Florida, Chem. Engrg., Gainesville, FL 32611 USA; [2]University of Florida, Dept. of Matls. Sci. & Engrg., Gainesville, FL 32611 USA; [3]Sandia National Laboratories, Albuquerque, NM 87185 USA; [4]EMCORE, Somerset, NJ 08873 USA

Device based on III-Nitride materials have been shown outstanding advantages such as high reverse breakdown voltage, and large current drive capacity for microwave power amplifiers in military and wireless communication applications. In order to minimize significant heat generation under high power operation, effective control of resistant stability becomes an important issue to prevent unexpected device degradation. Metal combination, Ti/Al, followed by either Pt/Au or Ni/Au is the most common use for n-ohmic contact in III-Nitride. Other metal schemes such as V/Al/Pt/Au or Ta/Ti/Al are also studied to achieve either low contact resistance or specific contact resistance, respectively. However, there is no significant study on the stability of n-type ohmic metal in high temperature region. MOCVD grown AlGaN/GaN HEMT structure was used in this high temperature ohmic contact study. Conventional Ti/Al/Pt/Au metal scheme was deposited in E-beam evaporator as control experiment. W or WSi were added by sputter system after E-beam Ti/Al/Pt and followed by final metal deposition Ti/Au. Transmission line measurement (TLM) after rapid thermal anneal (RTA) at varied temperatures for 45sec in nitrogen ambient was performed to obtain contact resistance and specific contact resistance. From TLM measurement, the insertion of WSi not only helps to reduce specific contact resistance but also improve the morphology of the contact and sharpness of the contact edge definition. The contact resistance was improved by 8 Ω-mm from 12.5 Ω-mm while the specific contact resistance was reduced from 1×10^{-5} Ω-cm^2 to 6×10^{-6} Ω-cm^2, respectively. From our preliminary Auger depth profile of the contact, WSi showed great thermal stability and there was no metal mixing observed from metals below and above WSi. The results of thermal and current stress data of WSi and W based contacts will be presented in the meeting.

9:40 AM Student

T5, Optimization of AlGaN/GaN HEMT Sunken Ohmic Contacts: Haiting Wang[1]; Lip Khoon Li[1]; Leng Seow Tan[1]; Eng Fong Chor[1]; [1]National University of Singapore, Electl. & Compu. Engrg., Ctr. for Optoelect. 117576 Singapore

In our study, the sunken ohmic contacts have been used to bring metal closer to the two-dimensional electron gas (2DEG) channel of a HEMT structure by etching off a portion of the top layers in the source and drain region. HEMTs with different etching depths for the sunken contacts have been fabricated to optimize the device performance. We have found that the best device IV characteristic is achieved when the sunken contacts are deposited within the AlGaN donor layer at a distance several nanometers above the AlGaN/GaN interface. The trend of IV characteristic with etched depth of the sunken contacts agrees well with that of the specific contact resistance obtained by linear transmission line method (LTLM) measurements, reported previously by our research group. We have also carried out simulations of device electrical characteristic with an aim to explain the experimental observations. As far as we know, there have not been many reports on the simulation of AlGaN/GaN HEMTs. We have performed our simulations using PISECS. The results indicate that the device performance improves gradually when the sunken contacts are brought closer to the 2DEG channel. However, this trend becomes invalid when the sunken depth is beyond the AlGaN donor layer. In fact, when the sunken contacts protrude into the 2DEG channel, the device performance degrades seriously. Simulations have demonstrated the occurrence of current crowding at the lateral sidewall of metal contacts because of the loss of 2DEG under the sunken contacts. Optimal performance is also not achieved with shallow sunken depth (i.e., at the surface or within the AlGaN barrier layer). There is a relative large voltage drop within these top layers, prior to the current reaching the 2DEG channel. The device operates in the most desirable condition

when the sunken contacts are within the AlGaN donor layer. This result correlates very well with the experimental measurements. The main current component is mostly likely the tunneling current from the metal contacts to 2DEG. Hence, the improved tunneling effect by increasing the doping concentration of the source/drain region using ion-implantation could be expected. This has been investigated by means of simulation. The results demonstrate an improved current density for the device. Experimental work to enhance the HEMT device performance further using a combination of sunken and implanted ohmic contacts is currently being pursued. In summary, both experimental and simulation results have shown that by optimizing the etched depth of the sunken ohmic contacts for the source and drain of HEMT, the contact resistance can be minimized, thus leading to optimized device IV characteristic. In addition, simulation has indicated that a further improvement is possible by increasing the doping concentration of the source/drain region underneath the sunken contacts.

10:00 AM Break

10:20 AM Student

T6, Compositional Shift of III-Nitride Alloy Semiconductors Induced by Reaction with Metallic Thin Films: *Brett A. Hull*[1]; Suzanne E. Mohney[2]; Uttiya Chowdhury[3]; Russell D. Dupuis[4]; Hai Lu[5]; William J. Schaff[6]; [1]The Pennsylvania State University, Matls. Sci. & Engrg., 206A Steidle Bldg., University Park, PA 16802 USA; [2]The Pennsylvania State University, Matls. Sci. & Engrg., 109 Steidle Bldg., University Park, PA 16802 USA; [3]The University of Texas at Austin, Electl. & Compu. Engrg., Austin, TX 78758 USA; [4]The University of Texas at Austin, Electl. & Compu. Engrg., 10100 Burnet Rd., Bldg. 160, PRC-MER-R9900, Austin, TX 78758 USA; [5]Cornell University, Electl. & Compu. Engrg., Ithaca, NY 14853 USA; [6]Cornell University, Electl. & Compu. Engrg., 415 Phillips Hall, Ithica, NY 14853 USA

The development of electronic and optoelectronic devices based on the III-nitride semiconductors has been rapid. However, the increasing utilization of the III-nitride alloys (including AlGaN, InGaN, AlInN, and AlGaInN) calls for further advances in our understanding of the contact metallurgy of both ohmic and Schottky contacts to these ternary or quaternary alloys. The interfacial reactions between the III-nitride alloys of $Al_xGa_{1-x}N$ or $Al_xIn_{1-x}N$ and the late transition metals were studied in this investigation. X-ray photoelectron spectroscopy (XPS) analyses of $Al_{0.47}Ga_{0.53}N$ epitaxial film surfaces that were revealed by wet chemical etching following reaction with thin films of Ni, Pd, or Au indicated that the AlGaN directly beneath the reaction interface shifted to an Al-enriched composition, which we estimate to be as high as x = 0.79 for a Ni/$Al_{0.47}Ga_{0.53}N$ contact annealed at 850°C for 2 minutes in N_2. Compositional profiles of thin cross-sections of annealed Ni/$Al_{0.47}Ga_{0.53}N$ samples were also obtained with scanning transmission electron microscopy (STEM), which provided further evidence that the near-interfacial layer within the $Al_{0.47}Ga_{0.53}N$ was significantly enriched in Al, while Ga was preferentially incorporated into the Ni film. Furthermore, preferential outdiffusion of In from $Al_{0.25}In_{0.75}N$ was observed by XPS compositional depth profiling of a Ni/$Al_{0.25}In_{0.75}N$ sample annealed at 500°C for 30 minutes. The observed III-nitride alloy compositional shifts in annealed metal/AlGaN and Ni/AlInN contacts are consistent with thermodynamic modeling. This modeling indicates that a compositional shift of the ternary III-nitride alloys towards the more stable of the two binary components is favored during reaction with the late transition metals, leading to enrichment of the semiconductor alloys with Al. Any compositional shift induced by interfacial reaction with metallic thin films can be expected to impact the electrical properties of the contacts due to the strong dependence of the band gap and electron affinity on the III-nitride alloy composition. Furthermore, compositional shifts may induce polarization effects that would further influence the electrical properties of the contacts.

10:40 AM

T7, Improvement of Schottky Characteristics by Insertion of Refractory Metal into Ni/Au Electrodes on n-(Al)GaN with Thermal Annealing: *Naruhisa Miura*[1]; Takuma Nanjo[1]; Muneyoshi Suita[1]; Toshiyuki Oishi[1]; Yuji Abe[1]; Tatsuo Ozeki[1]; Hiroyasu Ishikawa[2]; Takashi Egawa[2]; Takashi Jimbo[2]; [1]Mitsubishi Electric Corporation, Advd. Tech. R&D Ctr., 8-1-1, Tsukaguchi-Honmachi, Amagasaki, Hyogo 661-8661 Japan; [2]Nagoya Institute of Technology, Rsch. Ctr. for Micro-Struct. Devices, Gokiso, Showa, Nagoya 466-8555 Japan

Recent advancement in GaN-related electronic devices demonstrates their great potential for high power and high frequency applications in virtue of GaN robust material stability. High quality Schottky gate contact in AlGaN/GaN high electron mobility transistors (HEMTs) is one of the key issues to be realized. While metals such as Pt, Pd, Au or some alloys are available in the Schottky electrodes, Ni is widely utilized, which would be due to its physical properties such as good adhesion to nitrides or relatively high work function that realizes high Schottky barrier. However, further reduction of the gate leakage current is strongly desired for the operation at high voltage bias with low noise. In this work, we investigate insertion of a metal into the Ni/Au Schottky electrode which possesses high work function and/or high melting point as well as the thermal annealing effects on the electrical properties of the Schottky diodes. Insertion of Pt or Ir followed by the annealing at 500°C was found to be very effective to improve the Schottky characteristics such as the reduction of the leakage current. The diodes were fabricated on n-GaN (n=1E17cm^{-3}) epitaxial layer grown by MOCVD. Circular Schottky electrode of Ni(10nm)/x(30nm)/Au(300nm) was surrounded by Ohmic contact of Ti(25nm)/Al(500nm). The x stands for the inserted metal of Pt, Pd, Ir, Au or Mo. They were subjected to the rapid thermal annealing (RTA) for 5 minutes in nitrogen ambient. Before the RTA, any difference in electrical characteristics was not observed regardless of the difference in inserted metal. This suggests that Ni governed the electron transport since each Schottky electrode contacted with n-GaN by thin Ni layer. However, thermal treatment at 500ºC noticeably changed their electrical characteristics, such that the diodes containing Pt or Ir showed drastically low leakage current at reverse voltage bias whereas those with Mo showed leaky behavior. This peculiar result was well characterized by the relation to the work function of the inserted metals in terms of the effective barrier height as well as the leakage current. Namely, the inserted metal was made to contact with n-GaN by RTA. Furthermore, the thin Ni layer was found to be inevitable, as the diodes consisted of Ni/Pt(Ir)/Au Schottky electrodes had superior electrical characteristics than the non-Ni diodes of Pt(Ir)/Au after the RTA. This technique was confirmed to be successfully applicable to AlGaN/GaN HEMT. We employed the Ni/Pt/Au structure as a gate electrode, which contacted with $Al_{0.26}Ga_{0.74}N$ as a barrier layer. The gate leakage current reduced by as much as four orders of magnitude in comparison with the pre-annealed device, while transconductance of the transistors was not degraded.

11:00 AM Student

T8, High Temperature GaN Based Schottky Diode Gas Sensors: *Jihyun Kim*[1]; B. P. Gila[2]; C. R. Abernathy[2]; S. J. Pearton[2]; A. G. Baca[3]; R. D. Briggs[3]; G. Y. Chung[4]; F. Ren[1]; [1]University of Florida, Chem. Engrg., Chem. Engrg. Bldg., Gainesville, FL 32611 USA; [2]University of Florida, Matls. Sci. & Engrg., Gainesville, FL 32611 USA; [3]Sandia National Laboratories, Albuquerque, NM 87185 USA; [4]Sterling Semiconductor, Tampa, FL 33619 USA

There is great interest in development of wide-bandgap gas sensors, because it can operate at elevated temperature. Increasing regulations on the release of gases and other materials into the environment have focused attention in the development of advanced sensors. The applications include fuel leak detection in automobiles and aircraft, fire detectors, exhaust diagnosis and emissions from industrial processes. Especially GaN gas sensors can be integrated with UV detectors. It was known that the introduction of hydrogen to Schottky diodes changed the barrier height. The detection mechanisms for hydrogen are 1) dissociation of H2 on the surface of a catalytic metal, 2) diffusion into metal 3) the formation of a dipole layer at the interface between metal and semiconductor 4) lowering the barrier height. The dominant mechanism depends on metal contacts, hydrogen concentration and detection temperature. Current Si based gas sensor can detect hydrogen on the order of ppm, however, it is limited to low temperature applications. We demonstrated moderate high temperature (200-250°C) hydrogen gas sensors with GaN and SiC based Schottky diodes using Pd and Pt as Schottky contacts. The Pd and Pt metal Schottky contacts showed good detection sensitivity to not only hydrogen gas, but also CF4. The forward current of both Pd-GaN and Pt-GaN Schottky diodes increased significantly upon introduction of H2 in to a N2 ambient. By analyzing of diode current-voltage characteristics as functions of detection temperature, the gate current increase, when it exposed to H2 or CF4, is due to a decrease of effective barrier height. For introducing 10%H2 into a N2 ambient, the effective barrier height of Pd on GaN was lowered by 50~70 meV over the tem-

perature range 298~423K and the effective barrier height of Pt on GaN decreased by 30~60meV over the range 443~473K. The decection sensitivity was studied by cycling ambients from nitrogen to 10% hydrogen and back to nitrogen, an excellent reproducible barrier-height change was obtained. However, the Pt and Pd Schottky diodes failed sensing hydrogen gas over 400°C because the contact lost Schottky characteristics. We also investigate thermal stability of W-based Schottky metals for high temperature (>400°C) gas sensing. Schottky characteristics were observed for Au/Ti/W/SiC up to 900°C annealing. The measuremental set-up, forward current-voltage characteristics in both Pt-based and Pt/W-based gas sensors, and time response data will also be presented.

11:20 AM

T9, Study of Schottky Contacts on Strained AlGaN/GaN Heterostructures: *Zhaojun Lin*[1]; George R. Brandes[2]; Wu Lu[1]; [1]The Ohio State University, Dept. of Electl. Engrg., 205 Dreese Lab., 2015 Neil Ave., Columbus, OH 43210 USA; [2]ATMI, Danbury, CT 06810 USA

For an AlGaN/GaN HFET, a thermal stable Schottky gate contact with a large barrier height is always desirable to achieve low gate leakage current, high breakdown voltages, and high turn-on voltages. It has been shown that piezoelectric and spontaneous polarization exerts a substantial influence on the concentration and distribution of free carriers in strained AlGaN/GaN HFET heterostructures.[1, 2] So far, investigations have been focused on Schottky contacts on bulk GaN and AlGaN,[3] where the piezoelectric polarization effects are not existed. In addition, barrier heights of Schottky contacts on strained AlGaN/GaN heterostructures can not be determined by conventional thermionic emission theory because of the existence of strong polarization piezoelectric effect. In this work, a method to determine barrier heights of Schottky contacts on AlGaN/GaN heterostructures using capacitance-voltage (C-V) measurements is proposed. Based on measured C-V characteristics of Ir, Ni and Re Schottky contacts, two dimensional electron gas (2DEG) sheet carrier concentrations at AlGaN/GaN interface are determined. According to the relationship between 2DEG sheet carrier concentrations and Schottky barrier heights,[4] the barrier heights of Ir, Ni and Re Schottky contacts on strained Al0.25Ga0.75N/GaN heterostructures are determined to be 1.12 eV, 1.27 eV and 1.68 eV, respectively. The results show that the barrier height is lower for a Schottky contact with a higher metal work function, which is contrary to Schottky contacts on bulk AlGaN or GaN. It is attributed to that electrons in metal with a lower work function have stronger coupling to AlGaN surface donor electrons, which results in larger influence on the characteristics of AlGaN surface states and affect directly on 2DEG sheet carrier concentration. The measured I-V characteristics of Ir, Ni and Re Schottky contacts are consistent with the calculated 2DEG sheet carrier concentrations and barrier heights. To our knowledge, this is the first report on determination of barrier heights of Schottky contacts on strained AlGaN/GaN heterostructures using C-V measurements. [1]Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, and L. F. Eastman, J.Appl. Phys. 85, 3222 (1999). [2]Ambacher, B. Foutz, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, A. J. Sierakowski, W. J. Schaff, and L. F. Eastman, J. Appl. Phys. 87, 334 (2000). [3]L. S. Yu, D. J. Qiao, Q. J. Xing, S. S. lau, K. S. Boutros, and J. M. Redwing, Appl. Phys. Lett. 73, 238 (1998). [4]E. T. Yu, G. J. Sullivan, P. M. Asbeck, C. D. Wang, D. Qiao, and S. S. Lau, Appl. Phys. Lett. 71, 2794 (1997).

11:40 AM T10, Late News

Session U: SiC: Growth and Characterization

Thursday AM, June 26, 2003
Room: Auditorium
Location: Olpin Union Building

Session Chairs: Laura Rea, U S Air Force Research Laboratory, WL/MLPO, Wright Patterson AFB, OH 45433-7707 USA; Michael Capano, Purdue University, Sch. of Electl. & Compu. Engrg., W. Lafayette, IN 47907-1285 USA

8:20 AM Student

U1, Electro-Chemical-Mechanical Polishing of Silicon Carbide: *Canhua Li*[1]; Ishwara Bhat[1]; Rongjun Wang[1]; Joseph Seiler[1]; [1]Rensselaer Polytechnic Institute, ECSE Dept., 110 8th St., Troy, NY 12065 USA

An atomically smooth and defect-free substrate surface is important for obtaining good epitaxial layers. Processing induced defects such as scratches generated by lapping and polishing are the primary contributors to unwanted inclusions in SiC epitaxial films. At present, commercially available substrates are all mechanically polished using hard abrasives such as diamond polishing compounds.[1] This method can usually provide a fast removal rate (1~3µm/hr with 1µm size diamond slurry). However, since diamond abrasives achieve materials removal through plastic deformation, a damaged subsurface layer containing dislocations is unavoidable.[2] In contrast, chemical mechanical polishing (CMP) combine mechanical polishing with a chemical etching action, and can achieve defect free surfaces. Several CMP techniques have been reported[2,3] and one of them is using concentrated colloidal silica slurry with a high alkalinity (PH>10) at elevated temperature (~55°C). However, normal CMP techniques have very low removal rate (0.1-0.2µm/hr at elevated temperatures). Because of this, CMP is only used as the final polishing step. The purpose of this study is to investigate a new polishing method that can potentially provide a much faster polishing rate with minimal subsurface damage. The idea of this process is to combine anodic oxidation with normal CMP technique. Anodic oxidation and anodic etching of SiC have been studied by a few researchers before using HF or HCl solutions. Use of HF solutions can result in very rough surface, probably porous SiC. Restelli et. al also showed that KNO3 solution can even be used as electrolyte to oxidize SiC.[4] So if we anodically oxidize the SiC surface while removing the oxide using oxide CMP, a damage free "smooth" surface and a high removal rate might be achieved simultaneously. We investigated the use of this new electrochemical mechanical polishing (ECMP) technique for the removal of subsurface damage on commercially available SiC wafers. Hydrogen peroxide (H2O2) and potassium nitrate (KNO3) were used as the electrolytes while using colloidal silica slurry as the polishing medium for removal of the oxide. The current density during the polishing is varied from 1mA/cm2 to over 50mA/cm2. Even though high polishing rate can be achieved using high current density, the oxidation rate and the oxide removal rate need to be properly balanced to get smooth surface after polishing. The optimum surface can be achieved by properly controlling the anodic oxidation current as well as the polishing rate. At higher current flow (>50mA/cm2), the final surface was rough where as smoother surface was obtained when the current flow was in the vicinity of 1mA/cm2. Since the colloidal silica slurry is softer than SiC, the polishing process will only remove the oxide formed without introducing any subsurface damage. Full details on the ECMP process as well as the characterization of the surface by AFM will be presented. [1]W.C. Mitchel et al, Material Science Forum Vols. 338-342 (2000) 841-844. [2]L. Zhou et al., J. Electrochem. Soc., Vol. 144, No. 6, June 1997 L161-L163. [3]S. Johansson et al., J. Am. Ceram. Soc., 75, 189 (1992). [4]Restelli, A. Ostidich and A. Manara, Thin solid films, vol. 23, no.1 p23-29, 1974.

8:40 AM

U2, Large Diameter High Purity Semi-Insulating 4H-SiC Substrates for Microwave Device Applications: *D. P. Malta*[1]; J. R. Jenny[1]; M. F. Brady[1]; St. G. Müller[1]; A. R. Powell[1]; V. F. Tsvetkov[1]; H. McD. Hobgood[1]; R. C. Glass[1]; C. H. Carter[1]; [1]Cree, Inc., 4600 Silicon Dr., Durham, NC 27703 USA

Large diameter, high purity semi-insulating (HPSI) 4H-SiC crystals with diameters up to 100 mm have been grown by the seeded sublimation growth technique. Micropipe densities in HPSI boules were less than 100 cm^{-2} in 100 mm diameter boules and less than 5 cm^{-2} in 75 mm diameter boules. Typical residual boron and nitrogen concentrations were $5x10^{15}$ cm^{-3} and $9x10^{15}cm^{-3}$, respectively, with no detectable elemental deep level impurities as measured by secondary ion mass spectroscopy. Wafers cut from these crystals showed semi-insulating behavior with resistivities consistently $>10^9$ ohm-cm. Hall effect, deep level transient spectroscopy and electron paramagnetic resonance data suggest that the semi-insulating behavior originates from deep levels associated with intrinsic point defects. This work was supported in part by the Defense Advanced Research Projects Agency (DARPA) under contract #N00014-02-C-0306 and the Title III office under contract #F33615-99-C-5316.

9:00 AM

U3, Electrical Characteristics of 4H-SiC Epitaxial Layers Grown by Chemical Vapor Deposition on Porous SiC Substrates: *Zhaoqiang Fang*[1]; David C. Look[1]; Ramya Chandrasekaran[2]; Shailaja Rao[2]; Stephen E. Saddow[2]; [1]Wright State University, Semiconductor Rsch. Ctr., 3640 Colonel Glenn Hwy., 248 Fawcett Hall, Dayton, OH 45435 USA; [2]University of South Florida, Electl. Engrg. Dept., 4204 E. Fowler Ave., ENB 118, Tampa, FL 33620 USA

Porous SiC (PSC) has been an object of interest for reducing defects in epitaxial SiC layers grown on PSC substrates. In this study, electrical characteristics of 4H-SiC epitaxial SiC layers grown on PSC substrates and on standard n+- SiC substrates have been compared by using temperature-dependent current-voltage (I-V), capacitance-voltage (C-V) measurements, and deep level transient spectroscopy (DLTS). A PSC layer, with a thickness of 3.3 μm, was formed by surface anodization of a standard n+-SiC substrate. Approximately 4.6-μm thick 4H-SiC epitaxial layers were simultaneously grown on both standard (STD) and PSC substrates by chemical vapor deposition. Schottky barrier diodes (SBDs) were fabricated by using Ni/Au Schottky contacts on top of the epitaxial layers and Ni/Ti/Au ohmic contacts on the backs of the substrates for both SiC-on-STD and SiC-on-PSC layers (correspondingly, the SBDs are called STD SBDs and PSC SBDs). At T>300 K, the thermionic emission conduction mechanism dominates forward I-V characteristics for both SBDs. Ideality factor and series resistance, extracted from straight-line portions and high-current portions (up to 200 A/cm^2) of the I-V curves at 300 K, respectively, are about 1.38 and 3.3 x 10^{-3} Ω-cm^2, and show no significant difference for the two kinds of SBDs. Interestingly, for many PSC SBDs, an extra conduction mechanism or conduction path, shown as one or two current plateaus, can be clearly observed in the low-current portions of the forward I-V characteristics at T<300 K, or even at 300 K for some PSC SBDs with larger contact areas. Carrier concentrations, determined by C-V measurements from 100 to 400 K, are found to be about 2 x 10^{16} cm^{-3} for both kinds of SBDs and show little temperature dependence. Schottky barrier heights at 300 K, deduced from C-V data, are found to be 1.3 eV for most of the SBDs and are in agreement with literature data. At least, four electron traps, i.e., B (0.75 eV), C (0.63 eV), D (0.40 eV), and E (0.16 eV), can be found in the epitaxial 4H-SiC layers (or bulk regions) of both SBDs by DLTS characterizations. Trap E, with a trap concentration of ~1 x 10^{14} cm^{-3} and having a possible point defect nature, is a dominant trap in both SBDs. However, a huge broad DLTS peak at ~400 K (trap A) can be observed in the surface region of the epitaxial layers for both SBDs, and might be due to surface damage. The possible nature of the extra conduction mechanism found at low temperatures in PSC SBDs and the nature of the observed traps will be discussed. Based on the I-V, C-V, and DLTS data, we conclude that the electrical qualities of 4H-SiC epitaxial layers grown on PSC substrates are comparable with those grown on STD substrates.

9:20 AM Student

U4, Studies of Pore Morphology Modification in Porous SiC during High-Temperature Processing: *Jie Bai*[1]; Michael Dudley[1]; Pelagia-Irene Gouma[1]; Marina Mynbaeva[2]; [1]Stony Brook University, Matls. Sci. & Engrg., Stony Brook, NY 11794-2275 USA; [2]Ioffe Physico-Technical Institute, St. Petersburg 194021 Russia

Porous SiC is reputed to have potential as a substrate which can lead to improved (lower defect density) SiC and GaN epitaxy. The morphology of the pores can play an important role in the epilayer quality. It has been previously observed that pore morphology can be modified during high temperature processing. This paper presents the results of a study of pore modification in SiC during high-temperature processing. As received 6H and 4H porous SiC wafers were cleaved and polished and observed by SEM, Synchrotron X-ray Topography and High Resolution X-ray Diffraction prior to and following a high temperature anneal. In situ TEM during annealing was also carried out. Annealing temperatures were chosen in the range from 500°C to 2100°C which covers typical processing temperatures for these materials. Dramatic modification of pore morphology was observed at high temperatures. After the high temperature heat treatment, the pores were observed to become less interconnected and the size of the pores was observed to become larger without significant change in the overall porosity.

9:40 AM

U5, Study of Bulk Wet Etching and Optical Properties of Porous 6H-SiC: *Tim K. Hossain*[1]; Tilghman L. Rittenhouse[2]; Paul W. Bohn[2]; Marcus Alfred[3]; James Lindesay[3]; Ilesanmi Adesida[1]; [1]UIUC, ECE, 208 N. Wright St., Urbana, IL 61801 USA; [2]UIUC, Chmst. Dept., Urbana, IL 61801 USA; [3]Howard University, Physics Dept., 2355 Sixth St. NW, Washington, DC 20059 USA

The distinctive properties of SiC makes it a technologically important material for electronic devices which operate at high temperature, high power, and high frequency.[1] Optical devices fabricated from SiC such as blue-light-emitting diodes (LED) and UV photodiodes are also in a state of extensive development.[2] However, due to the indirect band-gap character, the intensity of the LED is very low, therefore, enhancement of the luminescence is strongly desired for applications such as display devices. It is known that porous Si fabricated by photoelectrochemical (PEC) etching exhibits intense visible luminescence at room temperature.[3] Therefore, porous SiC formed by PEC etching may also show better luminescence properties than those of the original SiC. In this paper, we present SEM, PL, CL and Raman studies of porous SiC to analyze its luminescence properties. The experiments were carried out on single-crystal n-type 6H-SiC wafers. The SiC sample was placed into a Teflon electrochemical cell, along with a Pt wire counter electrode and a saturated calomel reference electrode. Dilute HF was employed as the etching solution. The SiC sample was illuminated by UV light for an hour and was biased at different voltages. The UV light was focused down to a 2-cm^2 spot with a power density of 125 mW/cm^2. The maximum etch rate obtained was approximately 200 nm/min. Various SiC structures with intriguing networks of pores have been obtained. The formation of nanoporous SiC will be discussed in the light of our experiments. Cathodoluminescence (CL) and photoluminescence (PL) studies were conducted to study the luminescence properties of the nanoporous SiC produced. Intense blue-green luminescence with peak energy of around 2.7 eV which, is below the band gap of crystalline 6H-SiC (2.86 eV) at room temperature, was observed. Porous SiC shows much stronger luminescence intensity than the bulk SiC. Also, Raman studies were conducted in order to characterize the porous morphology and a model has been constructed to calculate the pore sizes. Our experimental results suggest that the surface region of porous SiC is responsible for the intense blue-green luminescence.

10:00 AM Break

10:20 AM

U6, Growth and Characterization of Intentionally Al Doped 3C-SiC on Step Free 4H-SiC and 6H-SiC Mesa Substrates: *Andrew J. Trunek*[1]; David J. Spry[1]; Phillip G. Neudeck[2]; J. A. Powell[3]; [1]Ohio Aerospace Institute, 5510(OAI), 21000 Brookpark Rd., MS77-1, Cleveland, OH 44135 USA; [2]NASA GRC, 5510, 21000 Brookpark Rd., MS77-1, Cleveland, OH 44135 USA; [3]Sest, 21000 Brookpark Rd., MS77-1, OH USA

This paper reports on an initial demonstration of intentional Al-doped stacking- fault (SF) -free 3C-SiC grown heteroepitaxially on atomically flat 4H-SiC and 6H-SiC mesa substrates. Commercially available 4H-SiC and 6H-SiC on-axis wafers are initially patterned with an array of hexagonally shaped mesas by reactive ion etching (RIE). The mesas were rendered free of atomic steps then 3C-SiC was grown heteroepitaxially on the step free mesas using "Step Free Surface Heteroepitaxy" process.[1] Hexagonal substrates, both n type and p type, were used for the mesa structures. The Al doping level was rapidly transitioned from 2E18 cm-3 to 2E17 cm-3 during growth of the 3C-SiC film. 3C-SiC was grown to a thickness in excess of 4 micrometers, which is far beyond the theoretically calculated critical thickness of fully strained 3C-SiC on 4H-SiC.[1] The samples were dry-oxidized to identify any SF's and double positioning boundaries (DPB's) in the 3C-SiC films. The levels of Al doping were verified by comparison to 8° off axis 4H-SiC witness samples. SIMS analysis and parametric testing of Schottky diodes were used to corroborate the results. Following a wet etch to open patterned vias in the oxide, 50 nm Ti/150 nm Ni Schottky contacts were E-beam deposited onto the p-type 3C-SiC mesa films. Devices without stacking faults consistently exhibited excellent reverse blocking characteristics, with leakage currents slowly increasing from around 1 microamp/cm2 at 20 V reverse bias to around 100 milliamps/cm2 at 85 V reverse bias. Initial capacitance-voltage measurements of the Schottky diodes indicate acceptor doping near 2E17 cm-3 and a built-in voltage near 1.7 V. The peak electric field calculated from these measurements is around 2.5 MV/cm. This electric field is believed to be the highest ever reported for a 3C-SiC Schottky diode at 0.1 A/cm2 reverse leakage current density, essentially equivalent to the highest breakdown fields previously reported in 3C-

SiC pn junction diodes.[2] These results indicate that 3C-SiC mesa heterofilms can be p-type doped at concentrations required to make viable devices while maintaining high film quality free of stacking fault defects. [1]P. Neudeck et al., Mat. Sci. Forum, vol. 389-393, p. 311 (2002). [2]P. Neudeck et al., IEEE Trans. Electron Devices, vol. 41, p. 826 (1994).

10:40 AM

U7, Surface Characterization of 3C-SiC Mesa Heterofilms: Evidence for Growth by Edge/Corner Nucleation Mechanism: *Philip G. Neudeck*[1]; Andrew J. Trunek[2]; J. Anthony Powell[3]; David J. Spry[2]; [1]NASA Glenn Research Center, 21000 Brookpark Rd., MS 77-1, Cleveland, OH 44135 USA; [2]OAI, 21000 Brookpark Rd., MS 77-1, Cleveland, OH 44135 USA; [3]Sest, Inc., 21000 Brookpark Rd., MS 77-1, Cleveland, OH 44135 USA

This paper presents the first detailed observations of unique surface morphologies of 3C-SiC films grown on 4H/6H-SiC mesas by the step-free surface heteroepitaxy technique.[1] The top surfaces of 3C-SiC films were extensively studied by optical microscopy and atomic force microscopy (AFM) as both film thickness (i.e., growth time) and growth temperature (i.e., terrace nucleation rate) were varied following complete coverage of each 4H/6H mesa by an initial 3C-SiC film. Almost all surface steps observed by AFM were 0.25 nm, the height of a single Si-C bilayer. However, strikingly different step patterns were observed, suggesting that radically different processes dominate the nucleation of new 3C-SiC bilayers on top of existing 3C-SiC film surfaces. For 3C film growth temperatures around 1400-1450C, step patterns indicate that growth proceeds via two-dimensional (2D) terrace nucleation of new bilayers followed by stepflow expansion and island coalescence. Preferred nucleation sites, sometimes observed in both thin and thick 3C-SiC films, lead to the formation of triangular growth hillocks with concentric (not spiral) steps on the 3C-SiC film surface. Defect-preferential molten potassium hydroxide etching suggests that isolated line dislocations are responsible for the triangular hillock formation. At 3C film growth temperatures around 1600-1650C, there is no evidence of 2D nucleation, consistent with previously observed 4H- and 6H-SiC results.[2] However, in sharp contrast to step-free 4H/6H-SiC surfaces that formed in T > 1600C growth conditions, well-ordered trains of 0.25 nm height steps were observed to propagate inward from outer mesa edges of the 3C-SiC film surface. This enabled thick 3C-SiC heterofilms (some completely free of etch pits) to be grown at high temperatures without 2D nucleation, and prevented formation of step-free 3C-SiC mesa surfaces analogous to step-free mesa surfaces previously achieved in 4H/6H-SiC.[2] We propose a growth model in which the symmetry and bonding of 3C-SiC relative to the mesa edge facilitates an edge/corner nucleation of new bilayers on the 3C-SiC growth surface. We also report the observation of stacking faults on as-grown 3C-SiC surfaces by AFM. Accelerated high temperature 3C-SiC growth rates were observed when mesas happened (occasionally) to contain stacking faults. The observed surface morphology on such mesas suggests a strong growth interaction between defect-assisted nucleation and edge/corner nucleation. [1]P. Neudeck et al., Mat. Sci. Forum, vol. 389-393, p. 311 (2002). [2]J. A. Powell et al., Appl. Phys. Lett. vol 77, no. 10, p. 1449 (2000).

11:00 AM

U8, Hot-Wall CVD Epi-Growth of 4H-SiC using PVT Buffer Layer: *Ying Gao*[1]; Zehong Zhang[2]; Xianyun Ma[2]; Yuri Khlebnikov[1]; Tangali Sudarshan[2]; [1]Bandgap Technologies, Inc., 1428 Taylor St., Columbia, SC 29201 USA; [2]University of South Carolina, Dept. of Electl. Engrg., Columbia, SC 29208 USA

11:20 AM Student

U9, Experimental Investigation and Simulation of Si-Droplets Formation during SiC CVD Epitaxial Growth and Implant Annealing Processes: *Yingquan Song*[1]; Galyna Melnychuk[1]; Yaroslav Koshka[1]; Michael S. Mazzola[1]; Jeffery L. Wyatt[1]; Hrishikesh Das[1]; Charles U. Pittman[2]; [1]Mississippi State University, Dept. of Electl. & Compu. Engrg., Box 9571, Mississippi State, MS 39762 USA; [2]Mississippi State University, Dept. of Chmst.., Box 9573, Mississippi State, MS 39762 USA

Appearance of silicon droplets due to supersaturation of Si-vapor generated in the gas phase via chemical decomposition of silane is an important issue for both SiC epitaxial growth and silane overpressure-based implant annealing of SiC. Possible consequences of the droplet formation are depletion of the Si growth species and resulting reduction of the SiC epitaxial growth rate, modification of the growth rate along the gas flow direction, insufficient or excessive supersaturation of the Si vapor during annealing, deposition of droplets at the growth or annealing surface, etc. Droplet growth and evaporation, as well as dependence of these processes on the gas flow velocity, pressure, and temperature should be accounted for in order to reliably define the optimal process window for epitaxial growth or implant annealing. In this work, a model for the droplet formation was developed and incorporated in commercial computational fluid dynamics simulation software. The model treats droplet formation from supersaturated silicon vapor as a gas phase reaction with reaction rate calculated using the classical nucleation theory. Surface reactions at the growth or annealing surface were defined to account for silicon droplet deposition. The experimental verification of the model was initially conducted through a direct observation of the droplet cloud above the heated susceptor. An extreme case of the droplet growth and deposition was realized by providing a significant silane overpressure during implant annealing in the hot wall CVD reactor. The rate of droplets deposition at different locations of the susceptor was experimentally determined by observing the surface morphology of SiC samples under the microscope. The simulation model was calibrated to provide good correlation between simulation and experiment for such important characteristics as droplet deposition rate and droplet-related morphology degradation, the region of the maximum droplet deposition on the susceptor, and morphology degradation (e.g., step bunching) due to insufficient Si-vapor overpressure above the annealing surface. The new simulation tool was found to be extremely useful for the new epitaxial growth and implant annealing process development.

11:40 AM U10, Late News

Session V: UV and Visible Nitride Emitters

Thursday PM
June 26, 2003

Room: Ballroom Center
Location: Olpin Union Building

Session Chairs: Russell Dupuis, University of Texas, Microelect. Rsch. Ctr., Austin, TX 78712-1100 USA; Andrew Allerman, Sandia National Laboratories, Albuquerque, NM 87185 USA

1:30 PM Student

V1, Ternary AlGaN-Based LEDs Emitting at 292 nm: *Ting Gang Zhu*[1]; Uttiya Chowdhury[1]; Michael M. Wong[1]; Dongwon Yoo[1]; Russell D. Dupuis[1]; [1]The University of Texas at Austin, Microelect. Rsch. Ctr., 10100 Burnet Rd., Bldg. 160, Austin, TX 78758 USA

Recently, wide-bandgap nitride semiconductor materials have attracted more attention for deep ultraviolet (UV) optoelectronic devices applications. In this study, we report on fabrication of ternary AlGaN-based UV-LED emitting at 292 nm from epitaxial layers grown using low-pressure metalorganic chemical vapor deposition (LP-MOCVD) in an EMCORE TurboDisc D125 UTM high-speed rotating-disk reactor. The epitaxial layers were grown on both-side polished c-plane sapphire substrate and light was extracted from the back-side of the sapphire substrate. The device structure implemented a low resistivity window n-layer in order improve light extraction while maintaining a low bottom spreading resistance. Resistivity map on as grown device epitaxial structure yielded a sheet resistivity of ~3000 Ù/• for ~360 nm thick Al0.52Ga0.48N:Si+ n-contact layer. The active region consists of three 10nm Al0.48Ga0.52N:Si barriers with 5nm Al0.48Ga0.52N:Si well for the three QW structure; The p-side cladding structures includes 20nm Al0.52Ga0.48N:Mg and 20nm Al0.40Ga0.60N, and a 25nm GaN:Mg is followed as p-contact cap layer. The epitaxial layers were fabricated into 80-500 µm diameter mesa-structure diodes using standard nitride processing technologies. Ni/Au metalization scheme was used for the p-contact and Ti/Au was used for n-contact fabrication. Diode I-V characteristics shows differential resistances of 100-130W. As-grown device structures displayed strong room-temperature cathodoluminescence response. The DC electroluminescence (EL) spectra under low current injection exhibited sharp peak near the QW bandedge (l~290nm) with linewidth of 9nm and a second peak centered around 363nm. Contrary to the results reported in literature, this second peak is not defect related emission, instead we believe

this second peak is due to carrier recombination in the p-GaN cap layer. As the injection current increase, the 290nm emission peak start dominating while the 363nm peak is diminishing. The investigation of modifying current block layer to eliminate the cap layer recombination will be presented. To further improve the device performance, we have implemented a multiple low-temperature buffer layer (LTBL) scheme which was growing a 1.2 µm thick Al0.52Ga0.48N:Si- template layer before growth of the device structure. This approach not only could help to reduce the threading dislocation density in the device which is expected to improve luminescence properties but also to relieve the current crowding to enhance device characteristics. Our study of the contact geometry effect on the device optical performance has been confirmed the conductivity of n-layer plays a key role in the UV emitter device performance. The device with LRBL shows EL emission peak at 292nm under DC excitation. The light output power measurements were made from the bottom of the device using a bare-chip geometry configuration. Measurements at I=13A/cm2 produced a light output intensity of 2mW measured with a calibrated Si p-i-n photodiode. Comparative studies of the performance of devices with heavily Si, lightly Si and Mg doped QW active regions will also be discussed.

1:50 PM

V2, Deep Ultra Violet Light Emitting Diodes Based on Short Period Superlattices of AlN/AlGaN: *Sergey A. Nikishin*[1]; Vladimir V. Kuryatkov[1]; Boris A. Borisov[1]; Gela D. Kipshidze[1]; Anilkumar Chandolu[1]; Mark Holtz[2]; Henryk Temkin[1]; [1]Texas Tech University, Nano Tech Ctr./Dept. of Electl. & Compu. Engrg., Box 43102, Lubbock, TX 79409 USA; [2]Texas Tech University, Nano Tech Ctr./Dept. of Physics, Lubbock, TX 79409 USA

We report optical and electrical properties of deep ultra violet (UV) light emitting diodes (LEDs) based on short period superlattices (SPSLs) of $AlN/Al_xGa_{1-x}N$ (x = 0.04-0.08) grown by gas source molecular beam epitaxy with ammonia. Details of growth procedure and device processing have been described previously[1,2]. Device structures consist of a 50 nm - thick AlN nucleation/buffer layer deposited on sapphire, followed by a ~ 1 µm thick Si-doped buffer layer of uniform AlGaN or AlN/AlGaN SPSL transparent at wavelengths longer than 250 nm. The active structure, including the p-n junction, with a thickness of ~ 0.7 µm was grown over this transparent buffer layer. The thickness of the well was varied from 0.5 nm to 1.25 nm and the thickness of the barrier was varied from 0.75 nm to 2 nm, and determined ex situ using X-ray diffraction. We show that carrier concentrations are strongly dependent on the barrier/well thickness ratios and the absolute values of barrier (well) thicknesses. The n- and p-type SPSLs were doped with Si derived from silane and Mg evaporated from effusion cell, respectively. For SPSLs with edge luminescence at (255-280) nm we obtain electron concentration in the range of $(1x10^{18} - 2x10^{19})$ cm^{-3} with mobility of (30-10) cm^2/Vs and hole concentration of $(2x10^{17} - 1x10^{18})cm^{-3}$ with mobility of (7-4) cm^2/Vs, at room temperature. Hall resistivities are very weakly temperature dependent. LEDs based on these superlattices and operating in the range of (260-280) nm exhibit turn-on voltages in the range of (3.5-6) V and support dc current densities in excess of 500 A/cm^2 at room temperature. We will discuss electrical and optical properties of our LEDs focussing on the contrasts between devices grown on different buffer layers. Influence of barrier/well thickness fluctuations and incorporation of In into well material on the output power of LEDs will be also discussed. This work is supported by DARPA, NSF (ECS-00700240 and ECS-9871290), SBCCOM, and the J. F. Maddox Foundation. [1]G. Kipshidze, V. Kuryatkov, B. Borisov, S. Nikishin, M. Holtz, S. N. G. Chu, and H. Temkin, Phys. Stat. Sol. (a), 192, 286 (2002). [2]K. Zhu, V. Kuryatkov, B. Borisov, G. Kipshidze, S. A. Nikishin, H. Temkin, and M. Holtz, Appl. Phys. Lett. 81, 4688 (2002).

2:10 PM

V3, OMVPE Growth and Characterization of AlGaN for Ultraviolet Optoelectronics: *Maria Gherasimova*[1]; X.-L. Wang[1]; G. Cui[1]; J. Su[1]; J. Han[1]; E. Makarona[2]; H. Peng[2]; Y. He[2]; Y.-K. Song[2]; A. V. Nurmikko[2]; [1]Yale University, Dept. of Electl. Engrg., PO Box 208284, New Haven, CT 06520 USA; [2]Brown University, Div. of Engrg., 182 Hope St., Providence, RI 02912 USA

The intense attention in III-nitride research towards ultraviolet light emitting diodes (UV LEDs) with emission wavelength below 360 nm is fuelled by potential applications including chemical/biochemical analysis, solid-state lighting, high density optical storage, and possibly covert communication. As has been demonstrated in the visible LEDs on sapphire (Steigerwald et al., IEEE J. Selected Topics in Quantum Electronics, v8, p310 (2002)), flip-chip bottom-emitting device is a preferred configuration for enhanced light extraction and power dissipation. As the emission wavelength from UV active region is extended below 360 nm, there is a crucial need for developing transparent AlGaN templates on sapphire with crystalline quality comparable to that achieved in GaN templates. The use of low temperature (LT) AlN buffer was demonstrated to be effective in reducing the mismatch strain and alleviating cracking (Han et al., MRS Internet J. Nitride Semicond. Res. 4S1, G7.7 (1999)). However, it was pointed out (Amano et al., phys. stat. sol. (b) 216, p683 (1999)) that AlGaN grown on LT AlN exhibits a high density of dislocations. Wang et al. (Appl. Phys. Lett., v81, p604 (2002)) reported the use of an AlN/AlGaN superlattice as a dislocation-blocking layer. In this work, we will report our study of AlGaN growth on AlN prepared through a two-step growth process, conducted in order to synthesize a template capable of supporting UV device structures. Growth of high temperature (1150 C) AlN on sapphire and silicon carbide substrates was investigated in this work. In particular, we studied the effect of the V/III ratio and the introduction of the LT AlN buffer layer on the film morphology. Direct nucleation of AlN on sapphire at high temperature leads to a rapid formation of three-dimensional islands, while the insertion of a LT AlN buffer (500 C) results in the planarization of AlN surface, leading to the emergence of the step-flow growth mode during subsequent deposition of AlGaN. Structural properties of the AlGaN films were investigated by AFM, TEM, and XRD. Threading dislocation densities are estimated to be on the order of 5E9 cm-2 for 2.5 µm thick AlGaN layers. UV LEDs containing quaternary AlGaInN quantum wells in the active region were successfully grown on AlGaN templates and exhibited emission wavelengths below 340 nm. In addition, the template was shown to support room temperature amplified spontaneous emission at 338 nm in an optically pumped separate-confinement heterostructure. The authors acknowledge the support of DARPA SUVOS under the direction of Drs. Steve Russel and John Carrano.

2:30 PM

V4, Growth of High Quality AlGaN Layers on Single Crystal Bulk AlN Substrates: *Qhalid Fareed*[1]; Rakesh Jain[1]; Remis Gaska[1]; Edmundas Kuokstis[2]; Jin Wei Yang[2]; M. Asif Khan[2]; Gintautas Tamulaitis[3]; Ibrahim Yilmaz[3]; Michael Shur[3]; Leo Schowalter[4]; [1]Sensor Electronic Technology, 1195 Atlas Rd., Columbia, SC 29223 USA; [2]University of South Carolina, Dept. of Electl. Engrg., 301 S. Main St., Columbia, SC 29208 USA; [3]Rensselaer Polytechnic Institute, Dept. of ECSE, Troy, NY 12180 USA; [4]Crystal IS Inc., Latham, NY 12110 USA

Recently, we demonstrated that single crystal bulk AlN substrates are very promising for the development of AlGaN-based deep ultraviolet emitters and Heterostructure Field Effect Transistor. In this paper, we will report on the growth and characterization of high Al-content AlGaN layers over single crystal C-face and A-face bulk AlN substrates using low-pressure metal organic chemical vapor deposition. The bulk AlN substrates were grown using a physical vapor transport technique by Crystal IS, Inc. AlxGa1-xN epitaxial layers with Al-fraction ranging from 0.5 to 1.0 (AlN) have been grown on C-plane and A-plane, off-axis (from 2° to 20°) bulk AlN substrates. Trimethyl aluminum (TMAl), trimethyl gallium (TMG), triethyl gallium (TEG) and ammonia (NH3) were used as precursors. The calculated growth rate was from 0.1 micron/hour to 0.2 micron/hour, and the thickness of the epitaxial layers was from 0.3 micron to 0.7 micron. The layers were characterized using X-ray diffraction, photoluminescence (PL) and atomic force microscopy. X-ray rocking curve measurement show high quality of the epitaxial layers with low full width half maxima (FWHM). X-ray reciprocal space mapping results showed the mosaic structure with small grain boundaries with broadening along ω-2θ direction and broadening due to thin layers along ω direction. Atomic force microscopy measurement showed the smooth morphology with steps flow on the surface. The root mean square (rms) roughness of the samples was found to be 2-3nm. Our preliminary results showed that density of pits was consistently lower in AlGaN layer grown on A plane substrates. PL measurements have been performed on the AlGaN epitaxial layers with peak wavelength ranging from 200-270nm for Al composition (x = 0.5-1.0). Temperature and excitation dependent measurements have been carried out on these samples. With temperature decrease, the PL peak maximum shifted only by approximately 1 nm from 208 nm at 300 K to 207 nm at 8 K for AlN homoepitaxial layers. The detailed measurements of photoluminescence in a wide range of optical excitation power (upto 1-2MW/cm^2) will be discussed.

2:50 PM Break

3:10 PM

V5, High Optical Quality InGaN/GaN Multiple Quantum Disks on GaN Nano-Columns Grown by rf-Plasma Assisted Molecular Beam Epitaxy: *Akihiko Kikuchi*[1]; Katsumi Kishino[1]; [1]Sophia University, Electl. & Elect. Engrg., 7-1, Kioi-cho, Chiyoda-ku, Tokyo 102-8554 Japan

InGaN/GaN multiple quantum disks (MQDs) were grown on self-organized GaN nano-columns by rf-plasma assisted molecular beam epitaxy (rf-MBE) for the first time. By optimizing the growth conditions, optical property of the GaN nano-columns was drastically improved. The room temperature photoluminescence (RT-PL) intensity of GaN nano-columns was over 10 times stronger than that of metalorganic chemical vapor deposition (MOCVD) grown GaN film. The PL peak wavelength of the InGaN MQDs ranged from 450 to 600nm and the intensity was comparable to that of the GaN nano-columns. The self-organized GaN nano-columns, which were reported by our group in 1997,[1] are high-density columnar single crystalline GaN with c-axis perpendicular to the substrate surface. The typical diameter of the nano-columns is 40-80nm and the density is 1-2E10cm-2. The GaN nano-columns were grown on (0001) sapphire substrates at 850°C by rf-MBE. The growth conditions were optimized changing the AlN buffer layer thickness and V/III supply ratio. RT-PL spectra of the undoped GaN nano-columns (diameter = 80nm, height = 2.0μm) and an undoped MOCVD-GaN film (thickness = 3.75μm, threading dislocation density = 3-5E9cm-2) were compared under 325nm He-Cd laser (1.3W/cm2) irradiation. The peak wavelength of the nano-columns was 363.2nm and of MOCVD-GaN was 361.6nm. From the PL peak position, we can note that the nano-columns were nearly strain free. The PL peak intensity of nano-columns was over 10 times stronger than MOCVD-GaN one. Such a high emission efficiency suggesting that threading dislocations are not existent in the nano-columns and the surface non-radiative recombination rate is relatively low. For the GaN nano-columns, higher excitation PL measurement was also carried out using 355nm Nd:YAG laser (10kW/cm2 - 10MW/cm2). With increasing the excitation power, the intensity of 363nm emission was gradually saturated and a new peak appeared at 370.4nm (FWHM = 24meV) around 700kW/cm2. The intensity of the new peak was rapidly increased at 1.4MW/cm2 and saturated around 10MW/cm2. The origin of this peak is under investigation. For the growth of InGaN MQDs, 8 pairs of InGaN(3nm)/GaN(5nm) were grown at 750°C subsequently to the GaN nano-columns. Formation of InGaN/GaN nano-columns, that is MQD, was confirmed by SEM observation. For the InGaN MQD (thickness = 3nm, diameter = 70nm), strong RT-PL emission was observed. The peak wavelength was ranged from 450nm to 600nm. The intensity was almost comparable to that of the GaN nano-columns. These results indicate that the nitride nano-columns are new kinds of attractive materials for high efficiency and wide wavelength range optical devices. This study was supported by NEDO Industrial Technology Research Grant Program #02A23041d. [1]M. Yoshizawa et. al., Jpn. J. Appl. Phys. 36 (1997) L459-L462.

3:30 PM Student

V6, Mg Fluctuation in p-GaN Layers and its Effects on InGaN/GaN Blue Light-Emitting Diodes Dependent on p-GaN Growth Temperature: *Chi Sun Kim*[1]; *Hyun Kyong Cho*[1]; *Min Ki Yoo*[1]; *Chang-Hee Hong*[1]; [1]Chonbuk National University, Semiconductor Physics Rsch. Ctr./Dept. of Semiconductor Sci. & Tech., 664-14 Duckjin-Dong, Duckjin-Gu, Chonju, Chollabuk-Do 561-756 S. Korea

Device performance of InGaN/GaN multi-quantum-well light-emitting diodes (LEDs) dependent on p-GaN growth temperature was investigated with current-voltage characteristics and output power measurements. Operating voltage at 20 mA decreased slightly with increasing the growth temperature of p-GaN layer whereas output power increased about 40%. However, reverse voltage at -10 μA enhanced up to 1080°C and then decreased sharply from 1110°C. For more deep and accurate research applicable to LEDs, 0.4-μm-thick Mg-doped p-GaN layers with different growth temperatures from 1030°C to 1160°C were grown on 1.3-μm-thick undoped GaN layers with constant growth conditions. All samples in this work prepared by metal-organic chemical vapor deposition. Electrical and optical properties and surface morphology were studied by capacitance-voltage (C-V), temperature-dependent and excitation power-dependent photoluminescence (PL), cathodoluminescence (CL), optical microscopy and atomic force microscopy (AFM) measurements with comparing the actual Mg concentration ([Mg]) measured by secondary ion mass spectroscopy (SIMS). Acceptor concentration was increased with the growth temperature up to 1080°C, but it was decreased sharply over 1110°C. It indicates that LED performance is enhanced with increased acceptor concentration as the p-GaN growth temperature increased up to some point. Surface morphologies are similar in samples grown at from 1030°C to 1080°C, but much polygonal or hexagonal hillocks are obviously shown in the sample grown at 1110°C and they increases in size at 1160°C. Room temperature PL spectra of p-GaN/undoped GaN samples show two dominant emission peak energies around 3.1 eV at below 1080°C and 2.9 eV at over 1110°C. The intensity of 3.1 eV band is increased with the growth temperature. However, over the growth temperature of 1110°C, 2.9 eV band is dominantly increased and 3.1 eV band is quenched. In SIMS data, the average [Mg] of the p-GaN/undoed GaN with various growth temperatures was similar within the error of 6% as standard deviation value, however the fluctuation of [Mg] was increased with increasing the growth temperature. The fluctuation of [Mg] reaches 40% and spatially high [Mg] regions in depth were observed in the sample grown at 1160°C. Based on these results including PL data, it seems that the 2.9 eV band is resulted from mainly a donor to acceptor pair recombination involving isolated Mg acceptors and spatially separated deep Mg-related donors. It means that the concentration of the Mg-related donor increases while the acceptor concentration decreases with increasing the growth temperature even though the average [Mg] is nearly unchanged and there are spatial regions with high Mg-related donors. It is in line with optical microscopy and AFM images. Partially, a potential fluctuation model and deep impurity band model are introduced for analysis of the behaviors of device performance.

3:50 PM

V7, Mg Doping of AlGaN and GaN Epitaxial Layers Grown by MOVPE: *Chak-wah Tang*[1]; Tingjie Chen[1]; Lisheng Yu[1]; Yugang Zhou[1]; Kei May Lau[1]; [1]Hong Kong University of Science & Technology, EEE Dept., Clear Water Bay, Kowloon Hong Kong

Low resistivity and high hole-concentration of p-type III-nitride compound semiconductor are very important for high efficiency blue or violet optical devices. We have grown magnesium-doped AlxGa1-xN alloys (x=0.107) in an AIXTRON 2000HT MOVPE system and performed various characterization. Al composition is determined by High Resolution X-Ray Diffractometer (HR-XRD). Surface morphology was analyzed by AFM. SIMS for atom profile analysis and low temperature Photoluminescence (PL) under different excitation power were also studied. The films were deposited at 1040°C on ~0.9μm undoped GaN buffer layers. Hall Effect Measurements was performed at room temperature the best Al0.1Ga0.9N layers show an average hole concentration of 3E17 cm-3 and Mobility of 2.97 cm2/V-s after Mg-activation by Rapid Thermal Annealing (RTA) at 850°C for 15mins. Layers exhibited low resistivity ~7 Ohm-cm. AFM images show a root mean square (RMS) surface roughness of 0.175nm Ra across a 4ìm2 area indicating an excellent surface morphology.[3] From PL measurement, three peaks can be observed at 3.15, 3.25 and 3.47eV. The former two peaks presumably are related to the band-to-impurities transitions from the neutral Mg acceptors with free electrons recombination.[4] SIMS data suggests the Mg-doped efficiency increases as the AlGaN thickness is increased. For Mg-doped GaN films, we have grown the epilayers with various Cp2Mg flow rates at 1055°C. The highest hole concentration, 7.9E17 cm-3, was obtained with activation at 950°C for 45 seconds, with a corresponding mobility of 7 cm2/V-s and a resistivity of 1.1 ohm-cm. From CTLM pattern measurements, samples activated at 950°C for 5 seconds have the best linearity in I-V characteristic and lower sheet resistance. From PL measurement, the dominant PL line around 2.77eV was observed at room temperature. We found that the PL intensity of the sample was enhanced more than ten fold after activation at 700°C for 10mins,[5] and the dominant peak position was slightly blue shifted. The FWHM of the emission peak became narrower[5] than the as-grown or other samples with different annealing condition. These results of single p-layers provide critical information for the optimization of junction device designs. References: [1]C.J. Eiting et al., J. Electronic Materials, Vol.27 (1998) No.4, p.206. [2]Maki Katsurgawa, S. Sota, M. Komori, J. Crystal Growth 189/190 (1998) 528-531. [3]C.Q. Chen et al, Appl. Phys. Lett. 81 (2002) No.6, p.4961. [4]J. Li et al., Appl. Physics Lett. 7(80) 2002 p.1210. 5. J. K. Sheu et al., J. Appl. Phys. 84 (1998) No.8, p.4950.

4:10 PM Cancelled

V8, InGaN/GaN Blue LEDs Fabricated on <11-20> Patterned Sapphire Substrates: *Tzu-Chi Wen*[1]; S. J. Chang[1]; Y. K. Su[1]; C. S. Chang[1]; Y. C. Lin[1]; S. C. Shei[2]; [1]National Cheng Kung University, Inst. of Microelect. & Dept. of Electl. Engrg., 1 University Rd., Tainan 70101 Taiwan; [2]South Epitaxy Corporation, No. 16 Da Shuen 9th Rd., Tainan Sci.-Based Industl. Park, Hsin-Shi 741 Tainan County

Conventional GaN-based LEDs are grown on top of sapphire substrates with a low temperature GaN or AlN nuclear layer. Although the introduction of low temperature GaN or AlN nuclear layer could significantly improve the crystal quality of the subsequent GaN epitaxial layer, threading dislocation density in the order of 109-1012cm-2 will still remain in the sample due to the large difference in lattice constant and thermal expansion coefficient between sapphire and GaN. Recently, it has been reported that one can also reduce the threading dislocation density in GaN by growing GaN epitaxial layers on top of patterned sapphire substrates. By using the patterned sapphire substrates, Tadatomo et. al. have successfully fabricated high output power nitride-based ultraviolet LEDs with a large external quantum efficiency.[1] In this study, we prepared nitride-based blue light-emitting diodes (LEDs) prepared on <11-20> patterned sapphire substrates and conventional un-patterned sapphire substrates were both fabricated. The optical properties and the reliabilities of these fabricated LEDs will be reported. Samples used in this study were all grown on c-face (0001) 2-inch sapphire (Al2O3) substrates in a vertical MOCVD system. Prior to the growth, patterned sapphire substrates were prepared. We first deposited a 500nm-thick Ni layer on top of the sapphire substrates. Standard photolithography was then used to define parallel stripes along the <11-20> direction. Conventional GaN-based LED chip process was performed. The output power was measured using the molded LEDs with the integrated sphere detector from top of the devices. It was found that although the EL peak positions of these two LEDs were about the same, the EL intensity of LEDs grown on <11-20> patterned sapphire substrates was about 40% larger. It was found that the output power at 20mA was 3.44mW and 4.88mW for LEDs fabricated on conventional and <11-20> patterned substrates, respectively. The larger EL intensity observed from LEDs grown on <11-20> patterned substrates could be attributed to the smaller defect density and/or the formation of micro surface roughness, which can be observed by atomic force microscopy (AFM). Life test of the fabricated LEDs were also measured by injecting a 20mA current into the LEDs for 1000 hours. It was found that LEDs fabricated on <11-20> patterned substrate are at least as reliable as LEDs fabricated on conventional un-patterned sapphire substrates. Reference: [1]K. Tadatomo, H. Okagawa, T. Tsunekawa, T. Jyouichi, Y. Imada, M. Kato, H. Kudo and T. Taguchi, Phys. Stat. Sol. (a), Vol. 188, No. 1, pp. 121-125, 2001.

4:30 PM Cancelled

V9, Nitride-Based LEDs with Si-Doped In0.23Ga0.77N/GaN Short-Period Superlattice Tunneling Contact Layer: *Tzu-Chi Wen*[1]; W. C. Lai[1]; S. J. Chang[1]; Y. K. Su[1]; L. W. Wu[1]; J. K. Sheu[1]; J. M. Tsai[2]; [1]National Cheng Kung University, Inst. of Microelect., Dept. of Electl. Engrg., 1 DaSheu Rd., Tainan 701 Taiwan; [2]South Epitaxy Corporation

Poor ohmic contact at metal/p-GaN interface is the major problem that led to LEDs with limited performance. In order to achieve high performance nitride-based LEDs, it is required to reduce contact resistance. Conventional nitride-based LEDs use semi-transparent Ni/Au on Mg-doped GaN as the p-contact material. However, the operation voltage of such LEDs is still high due to the low Mg ionization percentage. The low Mg ionization percentage will result in a highly resistive top p-GaN layer and a large metal/p-GaN contact resistance in nitride-based LEDs Thus, the doping concentration in the top p-GaN contact layer could be important in conventional nitride-based LEDs. Recently, we have demonstrated low operation voltage nitride-based LEDs with an n+-InGaN/GaN short period superlattice (SPS) tunneling contact layer. By growing such SPS structure on top of the p-GaN cap layer, one could achieve a good "ohmic" contact through tunneling when the n+(InGaN/GaN)-p(GaN) junction was properly reverse biased. In this study, GaN-based LEDs with Si-doped n+ InGaN/GaN SPS tunneling contact top layer were fabricated. A detail analyzes the electrical of LEDs with and without SPS will be reported. Furthermore, in order to study the influences of p-doping concentration on the LED performance, we also adjusted the CP2Mg flow rate from 100 to 180sccm during the growth of p-type GaN layer. It was found that the sheet resistance was around $2x10^5$ Ohms/sq for all samples used in this study. For samples with SPS tunneling contact layer, such a result indicates that the sheet resistance is almost independent of the CP2Mg flow rate when we grow the underneath p-type GaN layer. It also indicates that the insertion of the SPS tunneling contact layer will not change the measured sheet resistance. Furthermore, the specific contact resistance for the SPS top and p-type GaN top contact layer is 5.8×10^{-2} Ohms-cm2 and 1.47 Ohms-cm2, respectively. It was also found that the forward was 3.4 V and 3.75 V for the LED with and without SPS layer, respectively. The forward voltage is significantly reduced by using a Si-doped n+-InGaN/GaN SPS structure instead of high-resistivity p-type GaN as a top contact layer. Moreover, the LED operation voltage is almost independent of the CP2Mg flow rate when we grow the underneath p-type GaN layer. However, the EL intensity of LEDs with higher CP2Mg flow rate was larger than LEDs with lower CP2Mg flow rate. We found that even though the EL intensity of sample with lower CP2Mg flow rate is the smallest among the five LEDs with SPS tunneling contact layer, such a value was still much larger than the EL intensity observed from conventional LED without SPS under the same 20mA current injection.

Session W: Epitaxy II: Metamorphic Growth and Integration

Thursday PM, June 26, 2003
Room: Ballroom East
Location: Olpin Union Building

Session Chairs: Archie Holmes, University of Texas, Austin, TX 78758-4445 USA; Kei-Mai Lau, Hong Kong University of Science & Technology, Dept. of Electl. & Elect. Engrg., Clear Water Bay, Kowloon Hong Kong

1:30 PM Student

W1, Lower Surface Defect Densities and Improved Electrical Properties if InAs Epilayers Grown on GaP Substrates: *Aristo Yulius*[1]; [1]Yale University, Dept. of Electl. Engrg., New Haven, CT 06520 USA

Abstract not available.

1:50 PM Student

W2, Metamorphic InAs Bipolar Junction Transistors on GaAs and InP Grown by Molecular Beam Epitaxy: *Xiaohua Wu*[1]; Kent L. Averret[2]; Mike W. Koch[3]; Gary W. Wicks[3]; [1]University of Rochester, Dept. of Physics & Astron., Rochester, NY 14627 USA; [2]Air Force Research Laboratory, Wright Patterson AFB, OH 45433 USA; [3]University of Rochester, The Inst. of Optics, Rochester, NY 14627 USA

Large mobilities and electron saturation velocity make InAs a promising material for high speed devices. Additionally, the low band gap is useful for low power applications. The development of a high frequency transistor is dependent on the insulating quality of the substrate. Presently, no semi-insulating substrates that are lattice-matched to InAs exist. This necessitates metamorphic growth of InAs bipolar junction transistors (BJTs) on semi-insulating substrates, such as InP or GaAs. Most other metamorphic research has employed graded buffer layers to gradually move from the substrate lattice constant to that of the metamorphic layers. This work, however, has used the simpler approach of growing InAs buffer layers directly on the GaAs or InP substrate with no grading. The metamorphic InAs BJTs examined here exhibit room temperature common emitter current gains (β) comparable to those grown lattice-matched on InAs substrates. Surprisingly, the current gains of the devices were found to be insensitive to the quality of the metamorphic growth, as all the metamorphic devices examined, as well as the lattice-matched device on InAs, had β values near 70. However other characteristics, such as leakage current and surface roughness, were found to be sensitive to the quality of the metamorphic growth. Furthermore, neither surface roughness nor leakage current was as good in any of the metamorphic devices as it was in the lattice-matched growths. It was found that the thickness of the InAs buffer layer has an important effect on the quality of the metamorphic material. Thicker buffers, on both GaAs and InP substrates, produce smaller leakage currents and smoother surfaces.

As the buffer thicknesses are increased from 1 to 5 microns, the leakage currents decrease by a factor of 3. However, even with 5 micron thick buffers, the leakage currents are still more than 5x larger than those of lattice-matched growths. The same 1 to 5 micron increase of buffer thickness causes a 3x reduction in rms surface roughness, as measured by atomic force microscopy. Again, however, even the thickest buffer growths are still worse by a factor of at least 2.5 in comparison with the lattice-matched growths, which have rms roughnesses of 0.27 nm. The choice of substrate also influences the leakage currents of the metamorphic growths. InAs BJTs grown metamorphically on GaAs typically exhibit leakage currents that are twice as large as those of similar BJTs grown on InP. The explanation is probably related to the fact that GaAs has a larger lattice mismatch with InAs than does InP. The results of this work strongly suggest that high speed InAs BJTs should be feasible in metamorphic growths on either GaAs or InP substrates.

2:10 PM Student

W3, 2 Micron Emission from InAs Quantum Dashes Grown on a GaAs Substrate Using AlGaAsSb Metamorphic Buffers: *Ganesh Balakrishnan*[1]; Thomas J. Rotter[1]; Andreas Stintz[1]; L. R. Dawson[1]; Kevin J. Malloy[1]; D. L. Huffaker[1]; [1]University of New Mexico, CHTM, 1313 Goddard SE, Albuquerque, NM 87106 USA

We have used an AlGaAsSb metamorphic buffer layer to extend the emission wavelength of InAs quantum dashes grown on GaAs. Ground-state photoluminescence at wavelengths >2 μm is observed. We are able to reduce the mismatch between the InAs QD material and the surrounding matrix by using an AlGaAsSb metamorphic buffer that grades the lattice parameter from 5.653 Å (GaAs) to 5.869 Å (InP).[2] The dashes formed are 3-4 nm in height, 50-300 nm in length and 30 nm in width. These results are consistent with InAs quantum dashes grown on InGaAs lattice matched to InP.[1] Experimental Details: The structure is grown by molecular beam epitaxy on a GaAs substrate. Growth is initiated on a series of GaAs/AlGaAs layers, followed by the metamorphic buffer. The AlGaAsSb buffer is initially lattice matched to GaAs and then step graded to $Al_{0.5}Ga_{0.5}As_{0.54}Sb_{0.46}$ in sixteen steps where the Sb composition is increased by 3% in each step. The final relaxed lattice constant is 5.87 Å, as determined by X-ray diffraction. A 2 μm thick layer of $In_{0.53}Ga_{0.47}As$ was grown on the step graded buffer. For photoluminescence, a core layer of $In_{0.53}Al_{0.10}Ga_{0.37}As$ containing the active region was grown and capped with 100 Å $In_{0.53}Ga_{0.47}As$. This active region has been successfully used in 2 μm lasers grown on InP and is described in 1. The entire structure was grown at 490°C, except for the initial GaAs/AlGaAs grading layer, which was grown at 560°C. Room temperature photoluminescence shows the intensity maximum at 2022 nm, similar to the structures grown on InP.[1] An atomic force microscopy (AFM) image was taken from a structure with only the first layer of quantum dashes grown. It resembles the quantum dashes obtained by growing a similar structure on InP.[1] Structures are currently being grown to obtain lasers emitting at 2 μm. [1]InP Based Quantum Dash Lasers with 2 Micron Wavelength. Thomas J. Rotter, Andreas Stintz, and Kevin J. Malloy. Center for High Technology Materials, University of New Mexico, Albuquerque, NM. IEE Proceedings - Optoelectronics, conference proceedings for MIOMD V, September 2002. [2]1.6 Micron Emission from InAs Quantum Dots Grown on a GaAs Substrate Using an AlGaAsSb Metamorphic Buffer. G. Balakrishnan, L.R. Dawson, D.L. Huffaker Center for High Technology Materials, University of New Mexico, Albuquerque, NM. MRS proceedings, Fall 2002.

2:30 PM Student

W4, "Arsenic Free" Infrared Photovoltaic Detectors with Metamorphic InAlSb Digital Alloy Buffer Layers: *Elena A. Plis*[1]; Paul Rotella[1]; Sunil Raghavan[1]; L. R. Dawson[1]; Sanjay Krishna[1]; D. Le[2]; C. P. Morath[2]; [1]University of New Mexico, Ctr. for High Tech. Matls., 1313 Goddard NE, Albuquerque, NM 87106 USA; [2]Kirtland Air Force Base, Air Force Rsch. Lab. (AFRL/VSSS), 3550 Aberdeen Ave. SE, Bldg. 426, NM 87117 USA

Recent development in the epitaxial growth methods have led to an improvement in the performance of devices grown on GaSb substrates, especially those which exploit the mid-infrared (IR) atmospheric transmission window (3-5 mm). However, almost all the devices grown so far require the use both As and Sb elements to satisfy lattice-matching condition to GaSb. Moreover, the type-II band alignment in the InAs/(Ga,Al)Sb system leads to a reduced oscillator strength due to insufficient overlap of the electron-hole wavefunctions. If the lattice-matching condition is relaxed using a metamorphic buffer layer, type-I (In,Ga,Al)Sb based devices can be grown on GaSb. The significant bowing along the InGaSb tie-line ensures that IR devices can be grown on GaSb substrate using only one group V element in the heterostructure. Also, the type-I alignment of the bandstructure in this system would ensure the efficient localization for electrons and holes. In this paper, we report the growth of room temperature In0.47Ga0.53Sb photovoltaic detectors (lcut-off ~3 mm) on a graded InAlSb metamorphic buffer layer that was grown using a novel digital alloy (DA) technique that effectively filters the dislocations caused by the lattice mismatch between the substrate and the buffer layer. The DA buffer was grown by solid source molecular beam epitaxy (MBE) using a cracked antimony source. It consisted of alternating thin (tens of Å) layers of Al1-yInySb and Al1-zInzSb. The values for y, z, and the thickness of the layers are chosen to provide the desired average indium content. After the growth of a suitable number of periods of such material (about 5000 Å), the thickness ratio was altered to increase the average indium content, usually in steps of about 9%. The resulting buffer structure consists of a series of regions with indium content of 0, .09, .18, .27, .36, each of which is composed of thin layers of the two different compositions of AlInSb. Viewing the TEM images of many regions of the sample, we estimate the dislocation density to be less than 2´107/cm2. To further investigate the quality of the buffer layer, a simple In0.47Ga0.53Sb homojunction photovoltaic detector was grown on a similar DA buffer layer. Spectral response of this structure is represented. At 100K, a peak responsivity of 2.6A/W (Vb=-0.12V) was obtained, which corresponds to an external quantum efficiency of 71%.

2:50 PM Student

W5, Carrier Recombination in Metamorphic InAsP/InGaAs Double Heterostructure Grown on Off-Cut and On-Axis InP Substrates: *Yong Lin*[1]; Mantu K. Hudait[1]; Steven W. Johnston[2]; Steven A. Ringel[1]; [1]The Ohio State University, Electl. Engrg., 205 Dreese Lab., 2015 Neil Ave., Columbus, OH 43210 USA; [2]National Renewable Energy Laboratory, Golden, CO 80401 USA

Low band-gap (0.5-0.6eV) InGaAs (In composition>53%) grown on InP substrates is receiving interest for device applications that include ultra-speed electronics devices that can exploit the high carrier mobility and high band offset energies that are possible, as well as infrared opto-electronics and energy conversion devices that reach beyond 2μm. To achieve such structures requires the growth of high-quality, relaxed InGaAs with an equilibrium lattice constant well in excess of that of InP substrates. In recent work, we have shown that step-graded InAsP buffer layers on InP, where the anion component is varied to enlarge the lattice constant, have demonstrated superior morphology and lower dislocation density for subsequent metamorphic InGaAs growth, as compared with using InAlAs graded buffer layers. In this presentation, we will quantify the impact of InAsP buffer design and InP substrate misorientation on the electronic quality of metamorphic InAsP/InGaAs double heterostructures (DH) by analyzing the ultrahigh-frequency photoconductive decay (UFPCD) response obtained from these DH structures. Correlations with the strain relaxation properties using triple axis x-ray diffraction (TA-XRD) and with surface morphology features will also be made as a function of misorientation of the (001) InP substrate. InAsP step graded buffers were grown using solid source molecular beam epitaxy with an average grading rate of 20% As/ μm. A final layer composition of $InAs_{0.32}P_{0.68}$ was chosen, representing a misfit of ~ 1% with respect to the InP substrate. The thickness of undoped $InAs_{0.32}P_{0.68}$ barrier layers and lattice matched $In_{0.69}Ga_{0.31}As$ active layers in the DHs are 3 nm and 2 μm, respectively. Identical structures were grown on both 2° off-cut and on-axis (001) InP substrates. The growth temperature was controlled at around ~485°C. P_2 and As_2 were used as the P and As sources in the growth of InAsP and InGaAs layers. Growth was monitored by reflection high energy electron diffraction (RHEED). 2x4 RHEED patterns were observed all the time during the growth. Nomarski images revealed that the crosshatch pattern on 2° off-cut sample is more pronounced than that on on-axis sample. The lifetime measurements were carried out by UFPCD technique at room temperature. With the incident wavelength of 2μm, the lifetime was determined to be 4.8μs and 3.8μs for the 2° off-cut and on-axis substrates, respectively, from the UFPCD curves. These high carrier lifetimes demonstrates that the InAsP step graded buffers on both substrates have very good quality and the room temperature lifetime of sample on 2° off-cut substrate is very close to that on on-axis substrate. Reciprocal space maps by TA-XRD are currently being acquired and the differences of strain relaxation using both types of substrates, and the correlation of these results with the lifetime data will be presented.

3:10 PM Break

3:30 PM Student

W6, Segmented Growth Optimization and Chemical-Mechanical Polishing of InAlAs Graded Buffer Layers for InAs-Based Device Structures: *Atif M. Noori*[1]; Randy S. Sandhu[1]; Sumiko L. Hayashi[1]; Erik D. Meserole[1]; Abdullah Cavus[2]; Cedric Monier[2]; Randy Hsing[2]; Donald Sawdai[2]; Mike Wojtowicz[2]; Tom R. Block[2]; Augusto Gutierrez-Aitken[2]; Mark S. Goorsky[1]; [1]University of California, Los Angeles, Matls. Sci. & Engrg., Sch. of Engrg. & Appl. Sci., 2521 Boelter Hall, Los Angeles, CA 90095-1595 USA; [2]Northrop Grumman Space Technology, One Space Park, Redondo Beach, CA 90278 USA

Virtual substrates for large lattice parameter structures with semi-insulating bulk properties can be produced through the graded buffer layer formation of In(x)Al(1-x)As layers. We demonstrate that through graded buffer growth and chemical polishing, structures can be created with fully relaxed template layers with surface r.m.s roughness of about 0.5 nm. The composition of the InAlAs film is initially lattice-matched to the semi-insulating InP substrate and graded to InAs during molecular beam epitaxial growth. However, in this study the InAlAs buffer layer was subdivided into 3 segments. The strain relief, as determined through x-ray reciprocal space mapping, was maximized for each segment. This approach allowed for enhanced dislocation propagation in the buffer along with a minimization of surface roughness (as seen with atomic force microscopy). Plan view and cross-section transmission electron microscopy images show a clean crosshatch pattern of interfacial misfit dislocations and a surface threading dislocation density of less than 10^6 cm^-2 (below the detection limit of plan view TEM). To reduce the surface roughness of the completely relaxed structures, chemical-mechanical polishing (CMP) was used. An optimized NaOCl based solution was found to produce a smooth surface with minimal surface scratches and subsurface damage. Triple axis x-ray rocking curve measurements on separate CMP-processed InAs substrates confirmed that very little polishing damage was introduced. Epitaxial regrowth of device structures shows a considerable enhancement of the surface quality when the CMP process is used. This improved surface roughness is necessary for further lithographic processing.

3:50 PM Student

W7, Correlation of Minority Carrier Electron and Hole Lifetimes and the Reverse Saturation Current Density in GaAs Diodes Grown on Ge/SiGe/Si Substrates: *Carrie L. Andre*[1]; Maria Gonzalez[1]; Dave M. Wilt[2]; Eric B. Clark[2]; Arthur J. Pitera[3]; Minjoo L. Lee[3]; Eugene A. Fitzgerald[3]; Mark Carroll[4]; Matthew Erdtmann[4]; John A. Carlin[4]; Brian M. Keyes[5]; Steven A. Ringel[1]; [1]The Ohio State University, Dept. of Electl. Engrg., 205 Dreese Lab, 2015 Neil Ave., Columbus, OH 43210 USA; [2]NASA Glenn Research Center at Lewis Field, Photovoltaic & Space Environ. Branch, MS 302-1, 21000 Brookpark Rd., Cleveland, OH 44135 USA; [3]Massachusetts Institute of Technology, Dept. of Matls. Sci. & Engrg., 60 Vassar St., Cambridge, MA 02139 USA; [4]AmberWave Systems, 13 Garabedian Dr., Salem, NH 03079 USA; [5]National Renewable Energy Laboratory, MS-3215, 1617 Cole Blvd., Golden, CO 80401 USA

Recent work has shown that GaAs layers with threading dislocation densities below $1x10^6$ cm^{-2} are attainable on silicon substrates through the use of relaxed, compositionally graded, SiGe buffer layers up to 100% germanium. While prior materials studies have focused on the characterization of n-type GaAs, the effects of threading dislocations (TDs) on the properties of p-type III-V compounds must also be understood in order to fully assess the impact of TDs on a variety of III-V devices implemented on SiGe substrates. Hence, we report the first study of electronic properties of p-type GaAs and n+/p GaAs diodes grown on SiGe substrates. These results are compared with prior results concerning n-type GaAs and p+/n GaAs diodes, from which a unifying model on the impact of TDs on n+/p and p+/n configured minority carrier devices is developed. Graded, p-type, relaxed SiGe layers grown on Si substrates were grown by both ultra-high vacuum and low-pressure chemical vapor deposition. The impact of chemical mechanical polishing (CMP) was evaluated, resulting in a set of substrates with different threading dislocation densities (TDDs) in the fully relaxed Ge cap layer. Plan-view electron beam induced current images of GaAs diodes indicate an approximate threading dislocation (dark spot) density of $1x10^6$ cm^{-2} (with CMP) and $4x10^6$ cm^{-2} (without CMP) which compares with etch pit density measurements performed on the SiGe substrates. P-type InGaP/GaAs DHs were grown on these SiGe substrates to determine the electron minority carrier electron lifetime in p-type GaAs as a function of TDD using time resolved photoluminescence. For samples with a p-type dopant concentration of $2x10^{17}$ cm^{-3}, extracted minority carrier electron lifetimes were 0.75 ns and 2.0 ns, with corresponding minority carrier electron diffusion lengths of 1.3 µm and 4.0 µm, for substrates with TDDs of $4x10^6$ cm^{-2} and $1x10^6$ cm^{-2}, respectively. However, due to the higher mobility of electrons, the minority carrier electron lifetime for a TDD of ~$1x10^6$ cm^{-2} is a factor of 5 lower than that previously achieved for holes (10 ns). The disparity in carrier lifetimes has a direct impact on p+/n versus n+/p GaAs diode properties in spite of the identical TDD values. P+/n GaAs diodes are found to have superior I-V properties (factor of 7 smaller saturation current density) than n+/p configured diodes for identical doping concentrations, which is attributed to the dominance of depletion region recombination for GaAs diodes and the role of minority carrier lifetimes within this current mechanism. From these results, a unifying model will be presented, which predicts a preferred junction polarity exists for minority carrier III-V devices that are grown on virtual substrates with low, but non-negligible residual dislocation densities.

4:10 PM Student

W8, Low Temperature MBE-Grown GaAs on Silicon Substrates for Ultra-Fast Photoconductive Switches Application: *Kai Ma*[1]; Ryohei Urata[1]; James S. Harris[1]; David A.B. Miller[1]; [1]Stanford University, Solid State & Photonics Lab., CIS Bldg., Rm.126X, Via Ortega, Stanford, CA 94305 USA

GaAs was grown on silicon substrates by molecular beam epitaxy (MBE) at low substrate temperatures. Mainly due to the presence of 1-2% excess arsenic, low temperature grown GaAs material (LT-GaAs) has demonstrated a good combination of short carrier lifetime and reasonably high carrier mobility, as well as high dark resistivity, making it ideal for ultrafast photoconductor applications. Integration of high-speed LT-GaAs phonoconductive switches with Si CMOS integrated circuits, thus taking advantage of each technology's strengths, is one of the key elements in our approach to achieve an ultra-fast CMOS/optoelectronic analog-to-digital (A/D) conversion system with photoconductive sampling. Our ultimate goal is to monolithically integrate LT-GaAs photoconductive switches with completely fabricated CMOS circuits. The unique requirement of our work is that the whole growth process, including the silicon wafer surface cleaning process prior to the film growth, needs to be done at temperatures lower than Si-Al eutectic temperature. Adopting low temperature process would avoid damaging the metallic interconnects and limit dopants redistribution. This approach has minimum fabrication perturbation so that problems associated with finishing the final level metallization of silicon circuits after growing GaAs devices could be avoided. Various silicon wafer surface-cleaning methods were explored. In situ refractive high energy electron diffraction (RHEED) study indicated that a (2X1) reconstructed silicon surface was achieved at a substrate temperature as low as about 500°C. MSM photoconductive switches were fabricated on the LT-GaAs epilayers by depositing a titanium/gold Schottky contact and using a standard lift-off process. Time-resolved electro-optic sampling technique was used to characterize the responsivity and carrier lifetime of LT-GaAs. 1-2 picosecond lifetimes were achieved and the quantum efficiency was comparable to that achieved for LT-GaAs grown on GaAs substrates. Material properties including AFM, TEM and XRD study will also be presented.

4:30 PM

W9, Ge Overgrowth of Oxidized and Reduced Ge/Si Islands: *Vilma Zela*[1]; Anders Gustafsson[1]; Werner Seifert[1]; [1]Lund University, Solid State Physics, Box 118, S- 22100, Lund Sweden

The growth of high quality Ge epilayers on a single crystalline silicon substrate is of great technological interest. Unfortunately, pure Ge growth beyond a critical thickness (on the order of a few nanometers) results in high misfit and threading dislocation density due to a large lattice mismatch (4%). Threading dislocations deteriorate the physical and electrical properties of the material and can lead to premature device failure and poor performance. Much effort has been done to eliminate the threading dislocations in lattice mismatch epitaxy, for instance by: (i) thermal annealing, (ii) strained layer superlattice "filtering", (iii) growth of a thick buffer layer graded in alloy composition, (iv) selective area growth with thermal annealing cycles, and (v) combination of substrate patterning and epitaxial lateral overgrowth, ELO. In general, these methods are not only time- and material- consuming but also expensive, especially when lithographic processes are involved. In the this work we

study the growth of Ge over oxidized and reduced Ge/Si islands, in an Ultra High Vacuum - Chemical Vapour Deposition (UHV-CVD) reactor. The idea is to use self- assembled Ge/Si islands as crystal seeds for ELO, thus opening the way to a potential novel method to grow strain-free Ge layers on Si. Our approach is simple and no lithographic steps are utilized. It is based on a limited number of steps, with all, except oxidation, carried out in the same growth environment. In the first step, using the Stranski-Krastanov (SK) growth mode, the Ge/Si (100) islands are grown applying a stepwise growth. This achieves a unimodel dome shaped island population. In the second step the structure is oxidized and both the islands (consisting mainly of Ge) and the area between them (mainly Si) undergo this oxidation. Then, in the third step the structure is selectively reduced in H2 atmosphere, resulting in islands where Ge is recovered from GeOx, whereas the SiOx remains unaffected. Finally, the structure with the Ge crystal seed islands and the SiOx in the area in between is laterally epitaxially overgrown. Our results demonstrate that under certain conditions the oxidized and reduced Ge/Si (100) islands can transfer the epitaxial information from the island to the overgrown material. We found that a thin layer of native oxide, formed when the material is exposed to air at room temperature, is sufficient for our purpose. The Transmission Electron Microscope (TEM) images suggest that the nucleation starts at the reduced top areas of the islands, where the Ge content is the highest.

4:50 PM

W10, Quantification of Substitutional Carbon and Oxygen's Affect on the Electron Minority Carrier Lifetime in Pseudomorphically Strained SiGeC: *Malcolm S. Carroll*[1]; Clifford King[2]; [1]Agere Systems, 217 Prospect Ave., 14-3B, Cranford, NJ 07016 USA; [2]Noble Device Technologies, New York, NY 10013 USA

Substitutional carbon incorporation into the SiGe heterojunction bipolar transistor (HBT) has allowed the base thickness to be thinned while maintaining high boron concentrations within the SiGe base, because of its effect on boron diffusion, allowing continued scaling of SiGe HBTs for increased ft and fmax.[1] For future low power and low noise applications, increased boron concentrations and thinner base widths will be required in the HBT, which will require increasingly high concentrations of carbon incorporation (>$1x10^{20}cm^{-3}$). Because the minority carrier lifetime is qualitatively observed to decrease with increasing carbon and little quantitatively is known about the effect of substitutional carbon on the electron minority carrier lifetime in SiGe, it remains unclear whether increasing carbon will lead to non-negligible contributions to the electrical characteristics of future HBTs (e.g. recombination-generation in the emitter-base space charge region[2]). In this work, photoconductance measurements of undoped and doped $Si/Si_{0.7-x}Ge_{0.3}C_x$ heterostructures are used to quantitatively measure the effect of substitutional carbon and oxygen on the electron minority carrier lifetime in SiGe layers. The photoconductance of pseudomorphically strained (100) $Si/Si_{0.7-x}Ge_{0.3}C_x$ test structures grown epitaxially by rapid thermal chemical vapor deposition (CVD) were measured using an inductively coupled non-contact technique.[3] Carbon, oxygen, and germanium concentration profiles of the test structures were obtained using secondary ion mass spectrometry (SIMS) to correlate observed lifetimes to carbon and oxygen concentrations in the SiGe layers. The carbon concentrations were found to be ~100% substitutional measured by x-ray diffraction and SIMS. The $Si_{0.7-x}Ge_{0.3}C_x$ layers, furthermore, were found to have an increasingly high unintentional incorporation of oxygen (~ 0.005 * [C]), which is not unusual for CVD grown SiGeC layers.[4] Simulations of the photoexcited electron and hole concentrations in the $Si/Si_{0.7-x}Ge_{0.3}C_x/Si$ heterostructures during the photoconductance measurement are used to extract the electron minority carrier lifetime in the $Si_{0.7-x}Ge_{0.3}C_x$ layer from the measured decay lifetime of the entire heterostructure's photoconductance. The average electron recombination lifetime for the $Si/Si_{0.7}Ge_{0.3}$ layers was found to be 2.2 microseconds (μs). The minority carrier lifetime dependence of the $Si/Si_{0.7}Ge_{0.3}$ layer on the oxygen concentration was then examined and found to be extremely sensitive becoming shorter than 0.1 μs in layers with only as much as $3x10^{19}$ cm^{-3} oxygen. A much weaker dependence is observed on increasing substitutional carbon (and oxygen) monotonically shortening to 0.12 μs in the highest carbon content layer with $4x10^{20}$ cm^{-3} carbon and $2x10^{18}$ cm^{-3} oxygen. The reduced minority carrier lifetime in the $Si_{0.7-x}Ge_{0.3}C_x$ layers is found to correlate to the increasing oxygen background with a similar dependence as that in layers without carbon suggesting that the presence of oxygen (not carbon) is sufficient to explain the reduced minority carrier lifetime in the $Si_{0.7-x}Ge_{0.3}C_x$ layers. Finally, lifetimes in SiGe epitaxial layers grown on silicon substrates with varying qualities of in-situ clean are found to be extremely sensitive to contamination (carbon and oxygen) at the $Si/Si_{0.7}Ge_{0.3}$ interface demonstrating the utility of the photoconductance measurement as an inexpensive and rapid tool for monitoring SiGe epitaxial film quality. [1]J.-S. Rieh, et al. "SiGe HBT with Cut-off Frequency of 350 GHz", in IEDM Tech. Dig., Dec. (2002). [2]L. D. Lanzerotti, J. C. Sturm, E. Stach, R. Hull, T. Buyuklimanli, and C. Magee, Appl. Phys. Lett., vol. 70, pp. 23, 1997. [3]D. E. Kane and R. M. Swanson, "Measurement of the Emitter Saturation Current by Contactless Photoconductivity", presented at Transactions IEEE Photovoltaic Specialist, Las Vegas, 1985. [4]M. Carroll and J. C. Sturm, "Thermal Stability and Incorporation of Substitutional Carbon far above Solid-Solubility in Si1-xCx and Si1-x-yGexCy Layers Grown by Chemical Vapor Deposition using Disilane", Materials Research Symposium Proceedings, San Fransisco, Spring 2002.

Session X: Narrow Bandgap Antimonides and Arsenides

Thursday PM, June 26, 2003
Room: Ballroom West
Location: Olpin Union Building

Session Chairs: Ralph Dawson, The University of New Mexico, Ctr. for High Tech. Matls., Albuquerque, NM 87106 USA; Robert Biefeld, Sandia National Laboratories, Albuquerque, NM 87185-0601 USA

1:30 PM

X1, Correlation of Growth Conditions with Photoluminescence and Lasing Properties of Mid-IR Antimonide Type-II "W" Structures: *Chadwick L. Canedy*[1]; William W. Bewley[1]; Chul Soo Kim[1]; Mijin Kim[1]; Igor Vurgaftman[1]; Jerry R. Meyer[1]; [1]Naval Research Laboratory, Code 5613, 4555 Overlook Ave. SW, Washington, DC 20375 USA

"W" laser structures with four-constituent type-II active regions have displayed higher cw and pulsed operating temperatures than any other interband III-V lasers emitting at wavelengths beyond 3 microns. While the strong sensitivity of the laser performance to MBE quality is quite well known, optimization of the antimonide growth remains an ongoing challenge. To address this issue, we have carried out a detailed study of how the growth conditions correlate with a variety of evaluation figures of merit based on the photoluminescence (PL) and lasing properties. A Riber 32P MBE was used to deposit a number of W test structures with the same active region [InAs(18 Å) /$Ga_{0.7}In_{0.3}Sb$(34 Å)/ InAs(18 Å) / $AlAs_{0.11}Sb_{0.89}$(234 Å), for which λ = 3.6-3.8 microns at 78 K] on GaSb substrates with lattice-matched $AlAs_{0.08}Sb_{0.92}$ digital-alloy buffer layers. PL samples had 5 QWs, while laser samples had 10 QWs. The laser samples also had thicker $AlAs_xSb_{1-x}$ buffer layers (2.5 mm), which served as bottom optical claddings, and also 0.5-micron-thick GaSb separate confinement layers above the active regions. Interpretation of the results was simplified considerably by the finding that the PL intensity at 78 K correlated quite strongly with all of the other figures of merit. That is, higher PL intensity at 78 K nearly always implied higher PL intensities at 5 K and 300 K, narrower PL linewidth at 5 K (dominated by scattering and inhomogeneous broadening), narrower lasing linewidth, lower lasing threshold, and higher optical-pumping power-conversion efficiency. One surprising conclusion was that the optimal PL integrated intensities and linewidths were obtained for growth temperatures in the 475-500°C range, which is considerably higher than the substrate temperatures used in most previous type-II antimonide laser growths at NRL and elsewhere. For the optimal growth, the PL linewidth decreased from 240 nm at 78 K to 120 nm at 5 K. A comparison with the theoretical spontaneous emission spectrum at low temperatures then allows us to establish an upper bound of 5 meV for the inhomogeneous energy broadening. This may be compared with an energy difference of 30 meV that would result from a single-monolayer fluctuation of the InAs QW width. Thus whereas previous STM characterizations have clearly shown the presence of mono-

layer-scale steps at the QW interfaces, our results confirm that on the scale of the electron de Broglie wavelength the average QW width remains quite uniform, laterally as well as vertically (from QW to QW along the growth axis). Other preliminary results include the findings that to force InSb-like interface bonds in the active QWs is detrimental to the laser performance, and that a growth rate of 1 ML per second is preferable to half that rate. Although the laser samples were all grown at the non-optimal lower substrate temperature, they nonetheless yielded much lower lasing thresholds (< 200 W/cm^2 at 78 K), much longer Shockley-Read lifetimes (> 20 ns at 78 K, from the threshold analysis), and much lower internal losses (< 5 cm^{-1} at 78 K, from a cavity-length study) than were ever observed previously for NRL laser samples without an optical pumping injection cavity (OPIC) or integrated absorber geometry.

1:50 PM Student

X2, Interrelationships in the Electronic and Structural Characteristics of AlGaAsSb-InAs HEMT Structures: *Gregory Edward Triplett*[1]; April S. Brown[2]; Gary S. May[1]; [1]Georgia Institute of Technology, Electl. & Compu. Engrg., 791 Atlantic Dr., NW, Atlanta, GA 30332-0269 USA; [2]Duke University, Dept. of Electl. & Compu. Engrg., 128 Hudson Hall, Box 90291, Durham, NC 27709 USA

AlxGa1-xAsySb1-y -InAs HEMT devices are promising for high frequency and low power applications. While research has been directed towards the understanding and control of the electronic properties of these structures for many years, questions still remain on the optimization and role of the inverted heterojunction interface in the quantum well channel and on the origin and control of the charges in the structures-including channel charges and "parasitic" charges distributed through the structure and at the surface. Herein, we report on experiments that illuminate the relationships between structural variations and the electronic properties. In this work, formation of the inverted interface in HEMT structures, with emphasis on the role of the initial indium monolayer(s), is examined as it correlates with electron mobility and channel strain. MBE growth conditions at the inverted interface of a 15 nm channel structure, including substrate temperature and indium barrier thickness, are explored. Results show that formation of the inverted interface is important as it relates to 300°K and 77°K mobility, albeit in different ways. For instance, more indium (~3-ML) at 467°C is needed for high 77°K (>135,000 cm2/V/s) mobility, presumably due to desorption of indium during the interface formation. The optimal amount of indium is temperature dependent. Alternatively, less indium (=1-ML) at 467°C is needed to attain high 300°K (~32,000 cm2/V/s) mobility. At the InAs-on-AlSb interface, formation of InAs wires is also observed using atomic force microscopy measurements. These wires may be similar in origin to those reported in[1, 2], which result from mismatch at the interface. Strain in the InAs quantum well channel was measured with x-ray diffraction and was demonstrated to vary with the inverted interface growth conditions. Results, which varied from 0.02% to 0.33%, showed that the presence of more indium at the inverted interface enhances the strain relief driven by the channel mismatch with respect to the AlGaSb buffer layer. Obtaining high mobility at low charge in InAs/AlSb-based HEMT structures is also challenging. These structures characteristically exhibit higher mobility (30k cm2/V/s) with higher sheet charge (1012/cm2). In an effort to observe the conductivites over a wide range of carrier densities, HEMT structures with Al0.8Ga0.2AsySb1-y buffer and cap layers, as well as thinner (100Å) channels, were examined. Two sets of experiments examined buffer and barrier growth temperatures and cap thickness. Results demonstrate that the structural and transport properties are very sensitive to growth conditions. Al0.8Ga0.2AsySb1-y barriers grown at temperatures of 430< Ts <475°C, compared to temperatures Ts>475°C, resulted in higher 300K mobility. Also, arsenic composition in the buffer layers increased from 9 to 16% for buffer temperatures 430-520°C. The best-observed mobilities with corresponding 2-D carrier densities for each set of experiments were μ=10.5k cm2/V/s, ns=2.4e11/cm2 and μ=4.2k cm2/V/s, ns=7.8e10 /cm2. These observations are important because arsenic composition in AlxGa1-xSb enhances the ability to alter the strain in the quantum well as well as modify Schottky barrier characteristics. [1]D. W. Stokes, R. L. Forrest, J. H. Li, S. C. Moss, B. Z. Nosho, B. R. Bennett, L. J. Whitman, and M. Goldenberg, "Lateral Composition Modulation in InAs/GaSb Superlattices," Journal of Applied Physics, vol. 93, pp. 311-315, 2002. [2]B. Z. Nosho, B. R. Bennett, L. J. Whitman, and M. Goldenberg, "Spontaneous Growth of an InAs Nanowire Lattice in an InAs/GaSb Superlattice," Applied Physics Letters, vol. 81, pp. 4452-4454, 2002.

2:10 PM Student

X3, Interdiffusion Studies of Al and Ga in AlSb/GaSb Quantum Wells: *M. Gonzalez Debs*[1]; J. G. Cederberg[2]; R. M. Biefeld[2]; T. F. Kuech[1]; [1]University of Wisconsin, Madison, Dept. of Chem. Engrg., Madison, WI 53706 USA; [2]Sandia National Laboratories, Albuquerque, NM 87185-0601 USA

The electronic structure of multilayer semiconductor heterostructures is affected by the detailed compositional profiles throughout the structure and at critical interfaces. The thermal processing of materials can therefore affect the properties through the interdiffusion between layers of differing composition. This interdiffusion can place limits both on the processing time and temperatures as well as the range of compositional profiles that can be achieved in these structures. The '6.1 Angstrom' semiconductors must be prepared and processed at low temperatures due to their low melting points and associated defect populations. We have studied the interdiffusion of AlSb/GaSb multi-quantum wells to both characterize the rate of diffusion as well as understand the underlying mechanisms of interdiffusion. Interdiffusion of Al and Ga across the AlSb/GaSb interfaces was studied by rapid-thermal annealing multi-QW structures over a temperature range of 550 to 675°C for 30 to 9000 seconds and were coated with SiNx to prevent Sb sublimation during the thermal anneals. These samples were initially grown by Metal-Organic Chemical Vapor Deposition. Structures analyzed for this study consisted of 10-period multiple quantum wells of GaSb films separated by AlSb barriers, with GaSb(100) as the substrate material. A typical structure contained 12.9 nm GaSb wells separated by 3.3 nm AlSb barriers. The 77K photoluminescence (PL) was measured before and after the thermal anneals and the first order (n=1) electron to heavy-hole transition was monitored. These PL spectra exhibited blue energy shifts in the peak position as a function of time and temperature. The chemical diffusion coefficient between the AlSb\GaSb diffusion couple was quantitatively determined by fitting the observed PL peak shifts to the solution of the Schrödinger equation, using a potential derived from the solution of the diffusion equation, to quantify these interband transition energy shifts. The diffusion coefficient was described by an Arrhenius behavior with respect to temperature. The concentration at x=0 was determined from the PL peak position for each anneal, and the diffusion coefficient at each annealing temperature was determined from the concentration profile. The value of the diffusion coefficient ranged from 5.2x10^{-4} nm^2/s to 0.12 nm^2/s over the conditions studied. The interdiffusion process for these structures was characterized by an activation energy of ~2.6 eV. The composition dependence of the diffusion coefficient and the implications for device structures will be presented.

2:30 PM

X4, Control of As Cross-Contamination in InAs/GaSb Superlattice IR Detectors: *Eric M. Jackson*[1]; Georo Boishin[2]; Ed H. Aifer[3]; Brian R. Bennett[3]; Lloyd J. Whitman[3]; [1]SFA, 9315 Largo Dr. W., Largo, MD 20774 USA; [2]Nova Research, Inc., Alexandria, VA 22308 USA; [3]Naval Research Laboratory, Washington, DC 20375 USA

InAs/In(x)Ga(1-x)Sb type II superlattice-based IR detectors have the potential to outperform mercury cadmium telluride in the long and very long wavelength regimes. For this reason, considerable effort has been devoted to optimizing MBE growth conditions. One of the unavoidable difficulties of growing these superlattices is cross-contamination of the group V elements. Arsenic is particularly troublesome since it tends to build up a background pressure which can vary from system to system, growth to growth and even within a single growth. However, if it can be controlled, it also presents an opportunity to fine-tune the average lattice constant. Here we present the results of a study of As cross-contamination in InAs/GaSb films. Superlattices with periods consisting of 13 monolayer (ML) InAs on 13 ML GaSb were grown by solid source molecular beam epitaxy. InSb interfaces between the bulk layers were forced by migration enhanced epitaxy. Cracking cells were used for the anions, yielding As2 and Sb2 molecules. The arsenic content of the films was varied by changing the valve setting on the As cracker with the shutter closed during GaSb growth. The superlattices were studied using cross sectional scanning tunneling microscopy (XSTM) in addition to x-ray diffraction (XRD). The excess As may incorporate at the interface or within the bulk of the GaSb layer. While the lattice constant, determined from XRD, is sensitive to the average quantity of As in the GaSb, XSTM can resolve the presence of As in the bulk layers. Thus, the combination of the two techniques allowed us to determine strain effects and location

of the excess As. Excess As was seen to incorporate within the GaSb layer, while the lattice parameter varied linearly with increasing As/In ratio.

2:50 PM Student

X5, Microstructure of Lateral Epitaxially Overgrown InAs Thin Films: *G. Suryanarayanan*[1]; A. A. Khandekar[2]; T. F. Kuech[3]; S. E. Babcock[4]; [1]University of Wisconsin, Madison, Matls. Sci. Prog., 1509 University Ave., #201A MSE Bldg., Madison, WI 53706 USA; [2]University of Wisconsin, Madison, Dept. of Chem. Engrg., 1415 Engrg. Dr., 2014 Engrg. Hall, Madison, WI 53706 USA; [3]University of Wisconsin, Madison, Dept. of Chem. Engrg. & Matls. Sci. Prog., 1415 Engrg. Dr., 2014 Engrg. Hall, Madison, WI 53706 USA; [4]University of Wisconsin, Madison, Dept. of Matls. Sci. & Engrg. & Matls. Sci. Prog, 1509 University Ave., Madison, WI 53706 USA

InAs-based high-speed electronics can suffer from high densities of misfit-derived extended defects that are due to the lack of suitable lattice-matched semi-insulating (SI) substrates for this material. Lateral epitaxial overgrowth (LEO), a derivative of selective area overgrowth, has proven effective in reducing the density of misfit-derived defects in other heteroepitaxial systems such as GaN/Sapphire and GaSb/GaAs. Its efficiency for defect reduction in InAs grown on SI-GaAs, the present day substrate of choice, was explored in this study. Epitaxial InAs films were grown by LEO using trimethyl indium and arsine as precursors at 700°C with a V/III ratio of 80 by metalorganic chemical vapor deposition on patterned (100) GaAs substrates that were masked with 120 nm of CVD SiO_2. Two different types of mask patterns were used to investigate the growth characteristics and microstructure of the LEO material. LEO substrates with a 'wagon wheel' pattern allowed direct identification of (1) the fast lateral growth directions and (2) the favored sidewall orientations as a function of window orientation all in one growth run. The dominant sidewall facets were of the {111}, {121}, {311} and {011} types and depended on the orientation of the stripe. Upon identification of the <110> fast growth directions, subsequent LEO substrates had parallel stripe-shaped windows oriented along the <110> directions with openings 0.4, 0.6, 0.8, 2 and 5 μm wide and a pattern period of 10 μm. InAs (400) x-ray rocking curves for the LEO samples with sub-micron window widths were a factor of twenty or more narrower and relatively structureless when compared to those obtained from a control film grown directly on an unpatterned GaAs wafer. Multiple peaks indicative of multiple InAs crystal orientations, each tilted relative to the substrate by a few degrees, were observed in the rocking curves from the control sample. In stark contrast, single peaks consistent with no crystallographic tilt relative to the GaAs wafer were characteristic of the InAs grown on the sub-micron LEO substrates. The mosaic spread of the LEO was reduced to ~300-700 arcsec for sub-micron window LEO InAs. Cross-sectional TEM of the LEO material showed a dramatic reduction of dislocation density from $>10^{11}$ cm^{-2} in the control to ~10^7 cm^{-2} in the thicker parts of the 3μm thick film and amelioration of the columnar grains and associated low-angle grain boundaries that threaded the control film. A defect structure similar to that observed in the control was observed within windows and in the first 0.1 μm of film immediately above the windows. Most interestingly, however, this defective material was confined to the immediate vicinity of the window when the window opening was less than 1 μm. Dramatic defect reduction was realized in the rest of the film.

3:10 PM Break

3:30 PM

X6, Etch Characteristics of the Group-III Antimonides Using BCl3/Cl2 in Inductively Coupled Plasma (ICP) Dry Etching: *Carlos J. Monroy*[1]; Fred Semendy[1]; Phillip Boyd[1]; Fred Towner[2]; [1]US Army Research Laboratory, Electro Optics & Photonics/IR Matls., 2800 Powder Mill Rd., Adelphi, MD 20783 USA; [2]Maxion Technologies, Inc., 2800 Powder Mill Rd., Adelphi, MD 20783 USA

The group-III antimonides are predominant materials that have attracted much interest in recent years for the fabrication of opto-electronic devices that operate in the 1.6-5μm wavelength range. Inductively Coupled Plasma (ICP) play an important role in the dry etching of the antimonides providing high etch rates, reliable pattern transfer and improved anisotropic profiles. The etch characteristics of the group-III antimonides were measured as a function of gas combination of BCl3/Cl2, ICP power, Cathode power and pressure variation. It was noted that as the Cl2 flow was incremented in the (BCl3/Cl2)%, there was an increase in the etch rate of GaSb from 0.37-0.581μm, and the etch selectivity over photoresist was diminished. This data implies that this process is completely dominated by chemical reaction. As the ICP power was varied from 400 to 750W, the etch rate had a substantial increase from 0.35-0.65μm. This significant increase in the etch rate, is because at higher inductive power more chlorine radicals are created and the ion flux is increased, and both the physical and chemical etch components are enhanced. Selectivity of photoresist was decreased, and the sidewall angle of the mesa being etched changed from 64° to 32° respectively implying that, anisotropy and selectivity are highly degraded at higher ICP power because of the energetic ion bombardment. On the other hand, when changing the Cathode power from 100 to 200W, in increments of 25W, it was seen that the etch rate changed from 0.27-0.40μm, while anisotropy improved reaching a saturation angle of 70°. In contrast, the etch selectivity of photo resist decreased even further than when the ICP power was varied. When chamber pressure was varied from 3.5 to 8 mTorr, the etch rate decreased from 0.37-0.31μm/min. This decrease in etch rate at high pressure is due to the fact that the mean free path the ions have to travel is shorter, and the plasma is denser; and therefore the kinetic energy of the ions is lower, causing more collisions. It was also observed that, anisotropy was reduced while the selectivity of photo resist was improved.

3:50 PM Student

X7, Characterization of Contact Resistivity on InAs/GaSb Interface: *Yingda Dong*[1]; Dennis W. Scott[1]; Arthur C. Gossard[1]; Mark J.W. Rodwell[1]; [1]University of California, Santa Barbara, Dept. of Electl. & Compu. Engrg., Santa Barbara, CA 93106 USA

In SiGe BJTs, growth of a polysilicon extrinsic base over a dielectric spacer reduces the capacitance between the base and the collector (C_{BC}). In InP heterojunction bipolar transistors (HBTs), the same technique can be applied, with low resistivity polycrystalline material employed as the extrinsic base layer and buried SiO_2/SiN surrounding a collector pedestal. P-type polycrystalline GaSb is potentially a good candidate to be used as an extrinsic base material, but its bulk resistivity is still relatively high compared with n-type polycrystalline InAs, which has demonstrated very low bulk and metal contact resistivity. In this work, we propose to use p-type GaSb capped with n-type InAs as the extrinsic base layer. It has been widely known that InAs-GaSb heterostructure forms a broken-gap band lineup and it is possible for the p-type GaSb's valence band electrons to transfer into the conduction band of the neighboring n-type InAs, giving rise to an ohmic p-n junction. The electronic properties of InAs-GaSb heterostructure have been studied extensively, but most studies have focused on the negative differential resistance in this material system. In this paper, we examine the contact resistivity on the n-type InAs/p-type GaSb interface at low current density ($<10^4$ A/cm^2) and its dependence on the doping densities on both sides of the junction. A series of test samples were grown on semi-insulating InP wafers in a Varian Gen II MBE system. The test structure consisted of a 500Å GaAsSb layer (lattice matched to InP), a 400Å layer grading from GaAsSb to GaSb, and a 100Å GaSb layer. These three layers were doped with carbon. A top 1000Å Si-doped InAs layer was then grown. This layer structure was designed for the extrinsic base of an HBT, therefore the total layer thickness was constrained by process design considerations. The doping density in GaSb layer was varied from 2E19cm^{-3} to 8E19cm^{-3}, while in the neighboring InAs layer it was varied from 1E17cm^{-3} to 5E19cm^{-3}. The lowest contact resistivity on the InAs-GaSb interface was 4.2E-7 O-cm^2, obtained for the sample with the highest doping densities on both sides of the junction. Two reference samples were grown and tested for comparison. The first reference sample with a p+InAs/n+InAs tunneling junction showed an interfacial contact resistivity of 1.3E-5 O-cm^2 between the p-n interface, one order of magnitude higher than those of InAs/GaSb samples. The second reference sample consisted of a thin AlSb barrier layer displaced from an n-type InAs / p-type GaSb interface and the interfacial contact resistivity obtained was 5.4E-7 O- cm^2. The lowest contact resistivity obtained, 4.2E-7 O- cm^2, can be compared to that between metal and highly p-doped InGaAs, where values of 1E-7 O-cm^2 to 1E-6 O-cm^2 have been obtained. With moderate reduction in the interfacial resistance, p-type GaSb capped with n-type InAs can be employed as an extrinsic base material in InP HBTs, or in other device structures where low access resistance is required.

4:10 PM

X8, Non-Contact Determination of Free Carrier Concentration in n-GaSb and n-GaInAsSb: *J. E. Maslar*[1]; W. S. Hurst[1]; C. A. Wang[2]; D. A. Shiau[2]; [1]NIST, CSTL, 100 Bureau Dr., Stop 8360, Gaithersburg, MD 20899-8360 USA; [2]Massachusetts Institute of Technology Lincoln Labs, Lexington, MA 02420-9108 USA

GaSb-based semiconductors are of interest for mid-infrared optoelectronic and high-speed electronic devices. Accurate determination of electrical properties is essential for optimizing the performance of these devices. However, electrical characterization of these semiconductors is not straightforward since semi-insulating (SI) GaSb substrates for Hall measurements are not available. In this work, the capability of Raman spectroscopy for determination of the majority carrier concentration in n-GaSb and n-GaInAsSb epilayers was investigated. Raman spectroscopy offers the advantage of being non-contact and spatially resolved. Furthermore, the type of substrate used for the epilayer does not affect the measurement. However, for antimonide-based materials, traditionally employed Raman laser sources and detectors are not optimized for the analysis wavelength range dictated by the narrow band gap of these materials. Therefore, a near-infrared Raman spectroscopic system, optimized for antimonide-based materials, was developed. Epilayers were grown by organometallic vapor phase epitaxy with atomic Te doping levels in the range 2 to 80 x 1017 cm-3, as measured by secondary ion mass spectrometry. For a particular nominal doping level, epilayers were grown both lattice matched to n-GaSb substrates and lattice-mismatched to SI GaAs substrates under nominally identical conditions. Single magnetic field Hall measurements were performed on the epilayers grown on SI GaAs substrates, while Raman spectroscopy was used to measure the carrier concentration of epilayers grown on GaSb and the corresponding SI GaAs substrates. Compared to Hall measurements, Raman spectra indicated that both GaSb and GaInAsSb epilayers grown on GaSb substrates have higher free carrier concentrations than the corresponding epilayers grown on SI GaAs substrates under nominally identical conditions. This is contrary to the assumption that for nominally identical growth conditions, the resulting carrier concentration is independent of substrate, and possible mechanisms will be discussed.

4:30 PM Student

X9, A Novel Approach to Enhancing the Polishing Process of InP or GaSb-Based Wafer Substrates for Large-Scale Manufacturing: *Frank F. Shi*[1]; *K. Y. Cheng*[1]; K. C. Hsieh[1]; [1]University of Illinois, Micro & Nanotech. Lab., 208 N. Wright St., Dept. of Electl. Eng., Urbana, IL 61801 USA

The increasing growth and strong demand in microelectronic market combined with the September 11th issue require both industrial communities and governments to actively search for new materials and devices that have the capabilities for ultrahigh-speed and low-power-consuming integrated circuits for the next generation digital and light-wave communications. Indium phosphide (InSb) and gallium antimonide (GaSb), due to their high electron mobilities coupled with unique band structures, have become the two major candidates responsible for the next generation high-performance optoelectronic applications. For instance, InP/InGaAsP-based 1.31 μm and 1.55 μm long wavelength semiconductor lasers have been the workhorse for high-speed fiber optic communication and their role in communication becomes increasingly important as the demand in broadband applications increase rapidly. In the mean time, the prototype GaSb-based devices made by Rockwell, operating from a few hundred Gigahertz (~E9/s) through to Terahertz(~E12/s) frequencies, have already shown the highest operating frequency with the lowest turn-on voltage and electrical noise of any known semiconductor devices. However, InP and GaSb-based semiconductors do present a unique set of challenges for high volume manufacturing because of their special material properties. Both InP and GaSb themselves are very brittle materials and extremely difficult to handle during processing. Fabrication of advanced semiconductor optoelectronics typically requires thinning the backsides of wafers to about 150~90μm to form the bottom mirror. And after wafer thinning, there are still a few processing steps, such as metalization, photolithography/etching, and cleaving. Therefore, it remains a tremendous challenge to process entire InP or GaSb wafers without cracking. To date, InP-based device manufacturers still have no standard methodology to handle the thinner InP wafers. To address the above issues, we recently designed and developed a novel approach to polishing and handling fragile compound semiconductor wafers, particularly 2-inch InP or GaSb wafers, by using a double-layered Gel-Pakä polymer film as a host substrate on a vacuum polisher. The new approach avoids the traditional waxing process during wafer polishing, and provides a technique to significantly reduce the surface contamination and device damages frequently caused by waxing process on a fragile semiconductor wafer, and considerably improves the wafer surface thickness control during polishing. Using the new approach, one can easily handle and clean the thinned InP or GaSb wafers without wafer cracking. By totally eliminating about 20%~30% process steps, the new approach can significantly reduce through-put time and enhance the device yield as well as the polishability of InP or GaSb-based wafers. From X-ray Photoelectron Spectroscopy (XPS) study, the wafer surface attached with Gel-Pakä polymer films shows no surface contaminations from the organic host substrate.

Session Y: Molecular Electronics and Nanotubes

Thursday PM Room: Theatre
June 26, 2003 Location: Olpin Union Building

Session Chairs: David Janes, Purdue University, Dept. of Electl. Engrg., W. Lafayette, IN 47907-1285 USA; Ray Tsui, Motorola Laboratories, Physl. Scis. Rsch. Labs., Tempe, AZ 85284 USA

1:30 PM

Y1, Realization of "Molecular Enamel Wire" Concept for Molecular Electronics: *Rodion Vladimirovich Belosludov*[1]; Hiroyuki Sato[1]; Amir Abbas Farajian[1]; Hiroshi Mizuseki[1]; Yoshiyuki Kawazoe[1]; [1]Tohoku University, Inst. for Matls. Rsch., Katahira 2-1-1, Aoba-ku, Sendai, Miyagi 980-8577 Japan

For application to molecular wire the conducting polymers is one of the attractive materials. However, the carrier mobility is limited by structural disorder of conducting polymer and hence, in metallic state, it limits the electrical conductivity. Therefore, it would be better if the long single polymer chain can be covered by relatively bulky insulating structures and hence formed a molecular enamel wire. The "molecular enamel wire" concept, in which insulators are placed around conducting center, was first proposed by Wada et al.[1] They also suggested that the "molecular enamel wire" concept should make multi-level wiring possible because it can prevent any possible shorts between the wiring and would be one of the key concepts for realizing a high performance molecular supercomputer. One of the possible approaches for realization of this concept is the formation of inclusion complex in which the polymer chain located into the molecular nanotube based on cyclic cyclodextrin molecules. Here the structural, electronic properties and current transport characteristics of different polymers covered with cyclodextrin molecules have been investigated using quantum mechanical simulations. Moreover, density functional calculations have been performed to investigate the effect of metal contacts on the electronic structure of a molecular enamel wire.[2, 3] Thus, the results of calculations showed that the structure of polythiophene into CD molecular nanotube has near-planar geometry, with the electronic configuration of the optimized structure being practically same as the one in the planar conformation. It has also been found that in this case, there is no charge transfer between polymer fragment and frameworks of CDs. The doping effect on the geometric and electronic properties of conducting polymers encapsulated by CDs has been also investigated. Thus, the single chain of polyaniline in metallic form can be covered with the insulator CD molecular nanotube. Attached Au clusters do not modify the electronic properties of the polymer chain and hence do not affect the conductance properties of the studied molecular wires. Obtained results suggest that the CD molecules can be used as insulated molecular nanotubes for stabilization of the isolated near-planar configuration of single polymer chain. [1]Y. Wada, et al., Jpn. J. Appl. Phys. 39 (2000) 3835, and references therein. [2]R.V. Belosludov, et al., Jpn. J. Appl. Phys. 41 (2002) 2739. [3]R.V. Belosludov, et al., Jpn. J. Appl. Phys. in press.

1:50 PM Student

Y2, Measuring Electronic Conduction in DNA Attached to Au-Electrodes: *Sugata Bhattacharya*[1]; David B. Janes[1]; Gil Lee[2]; Jaewon Choi[1]; Saurabh Lodha[1]; Alejandro Bonilla[2]; [1]Purdue University, Sch. of Electl. & Compu. Engrg., 465 Northwestern Ave., W. Lafayette, IN 47906 USA; [2]Purdue University, Sch. of Chem. Engrg., 1283 CHME Bldg., W. Lafayette, IN 47906 USA

DNA has emerged as a central material in bionanotechnology because of the ability to design and synthesize sequences that can self-assemble into 3D structures. Characterization of double stranded DNA in solution indicates that DNA is capable of transporting charge and has generated a great deal of interest in the possibility of using DNA as an electronic material. In order to address the associated issues, it is important to characterize and understand electron transport in DNA. Experimental studies of electronic conduction in DNA report widely varying electronic properties and debate is open on DNA electron transfer/transport mechanisms. Most previous DNA conduction studies have been done on relatively long DNA, without specific end groups to bond to the contacts. Because of this, the contact resistance, and general nature of the contact to the DNA, has been poorly controlled. We have advanced work towards quantifying the electrical conductivity of DNA oligonucleotides by studying the conductivity of 18 base pair long (approx. 5 nm) guanine rich double stranded DNA attached to gold electrodes. The oligonucleotides used here have been synthesized using thiol (-SH) end groups that can form strong bonds to gold surfaces. In the molecular electronics field, these end groups are generally considered to be "alligator clips" that can provide strong electrical coupling to the contacts. A number of different strategies to microfabricate electrodes with suitable gap spacings have been developed. We have tried to fabricate nanoelectrodes using electromigration, which yielded useable devices, but the gaps obtained were not reliable. Next we fabricated Step-Break junctions in which the gap was created due to the shadow region of an overhanging metal during evaporation. We are planning to also study gaps created by cutting a wire with an AFM diamond tip, as well as using electrodeposition to get controllable gaps between the electrodes. For a number of devices, conductivity between the contact pads increases significantly following exposure to a solution containing the DNA double strands. This increase in conductivity is thought to be due to electronic conduction through DNA double strands which are bonded to the two contacts. The measurements were performed on dry electrodes and in a 80% humidity atmosphere. Blank measurements included electrodes treated with salt only and electrodes rinsed with DI water and they were consistent with DNA being responsible for the increase in conductivity. For biases between -200 and +200 mV the behavior is Ohmic and for higher voltages (up to 1V) the current seems exponential on the bias. The currents observed were typically in the range of 2 to 400 nanoamperes.

2:10 PM

Y3, Nature of Electrical Contacts in Au-Octanedithiol-GaAs Diodes: *Julia W.P. Hsu*[1]; David V. Lang[1]; Y. L. Loo[1]; Krishnan Raghavachari[2]; [1]Lucent Technologies, Bell Labs., 600 Mountain Ave., Rm. 1D368, Murray Hill, NJ 07974 USA; [2]Indiana University, Chmst. Dept., Bloomington, IN 47405 USA

We examine how the top Au electrode fabrication method affects the properties of electrical contacts in Au-octanedithiol-GaAs diodes. A novel printing technique, nanotransfer printing (nTP), was applied to make patterned Au contacts on top of the dithiol layer deposited on n+ GaAs substrates. The nTP process occurs at room temperature under ambient conditions, and is purely additive so that the molecules are not subjected to physical or chemical stress. Furthermore, nTP is capable of producing nanometer-size features over centimeter-size areas. Unlike devices in which Au contacts are fabricated by direct evaporation onto dithiol-coated n+ GaAs (evaporated junctions), the nTP diodes contain no direct contact between the top and bottom electrodes. To understand the nature of the electrical contact in these molecular junctions, we performed current-voltage (I-V), capacitance-voltage (C-V), and internal photoemission (IPE) experiments. The current levels in the nTP junctions are five orders of magnitude lower than the evaporated junctions. Small regions of ohmic contact (low barrier height) are the cause of high current levels measured in the evaporated junctions. Furthermore, the evaporated junctions show quadratic energy dependence in the IPE yield that is characteristic of metal-semiconductor Schottky barriers; the measured barrier height of 0.7 V is consistent with Au-GaAs contacts. In contrast, the IPE yield of the nTP junctions depends exponentially on E, signifying electron emission from a disordered material. Thus, fundamentally different transport mechanisms are at work depending on the fabrication of the contacts. Our results imply that electrical transport in nTP devices occurs primarily through 1,8-octanedithiol, while conduction in devices fabricated by conventional evaporation is dominated by direct Au/GaAs contacts even though the molecular layer was deposited the same way in both cases. To understand the experimentally observed transport behavior in the nTP diodes, electronic structure calculations are performed to obtain the molecular electronic level positions. Charge transfer occurring via chemical bonding and band alignment across the molecule-semiconductor and molecule-metal interfaces will be discussed.

2:30 PM Student

Y4, Metal-Molecules-Metal Devices with Preformed Metal Contact Structures: *Jaewon Choi*[1]; David B. Janes[1]; Saurabh Lodha[1]; Yi Chen[1]; Henny Halimun[1]; Subhasis Ghosh[2]; Scott Burns[3]; Clifford P. Kubiak[3]; [1]Purdue University, Sch. of Electl. & Compu. Engrg., 1285 EE Bldg., W. Lafayette, IN 47907-1285 USA; [2]Jawaharlal Nehru University, Sch. of Physl. Scis., New Delhi 110-067 India; [3]University of California at San Diego, Dept. of Chmst. & Biochmst., San Diego, CA 92121 USA

Organic molecules have attracted much interest as future electronic components, due to their self-assembly properties and novel functionalities. The way to make a proper contact structure for those molecules is still a key issue for realizing practical molecular electronic devices. This presentation will describe several approaches for fabricating suitable contact structures and present measured current-voltage relationships for several molecular systems studied to date. A relatively simple way to make two metal contacts by using break junction with electromigration would be described first, along with the conduction experiments using this structure. The gap distance between electrodes was approximately estimated by the tunneling conduction through pre-self-assembled structure. Several molecules were successfully self-assembled and measured for conduction. Frequently, symmetric and highly conductive current-voltage (I-V) curves were measured. The lack of a conduction gap in these I-V curves implies a high degree of coupling between the molecules and the contacts. Two of the measured molecules, 1,4-benzenedithiol and 1,4-benzenedimethanethiol (XYL), will be used as representative examples. The former one showed higher conductivity, as expected from mesoscopic theory. The data on XYL showed an approximate quantization of conductivity, which is believed to correspond to conduction through small, integer numbers of molecules in these measurements. The conductivity of porphyrindithiol molecules, which are candidates for gas sensing elements, was also measured using this structure. To get around the problem of low yield and poor uniformity for the break junction formed electromigration, a new scheme of making lateral electrodes to molecules has been developed. Using the automatic shadow of a thick metal layer, which is used as one electrode, a second electrode can be fabricated by evaporating with an overlap onto the previous electrode, resulting in a narrow gap at the edge of the first electrode. For the electrodes fabricated to date, the gap distance appears to be on the order of 5 nm, as evidenced by our success in bridging the gaps using assemblies consisting of 5 nm gold cluster and molecules. This new lateral contact structure can provide the capability to make hetero material contacts to molecules and therefore to control the degree of coupling between the contact metals and molecules. Using this approach, it should be possible to realize room temperature quantum phenomena in molecular devices, as is observed in scanning probe microscopy experiments, in which one contact is coupled relatively weakly to the molecules. The structure can also provide an effective gate, which can provide a means to modulate the molecular conduction.

2:50 PM

Y5, Clocked Molecular Quantum-Dot Cellular Automata: *Craig S. Lent*[1]; Beth Isaksen[1]; Enrique Blair[1]; Marya Lieberman[2]; [1]University of Notre Dame, Electl. Engrg., 275 Fitzpatrick Hall, Notre Dame, IN 46556 USA; [2]University of Notre Dame, Dept. of Chmst. & Biochmst., Notre Dame, IN 46556 USA

Computers dating back to those composed of electromechanical relays have relied on encoding binary information in the on or off state of a current switch. While this has been remarkably successful, it may not be the appropriate paradigm for realizing single-molecule devices. The quantum-dot cellular automata (QCA) approach to molecular electronics involves using charge configurations within molecules to encode bit

information. No current flows through the molecule. This QCA approach has substantial advantages over molecular electronic devices in which molecules are used as miniature current gates or current-carrying wires. Power dissipation can be greatly reduced and true power gain is possible. Prototype QCA devices using single-electron switching have been demonstrated using small metallic dots at low temperatures. Devices as complex as shift registers have been made and power gain has been measured experimentally. We describe how this approach to molecular electronics can support general-purpose computation and show the classes of molecules that we are studying as candidate QCA cells. We present ab initio quantum-chemistry calculations of simple molecules which act as clocked molecular QCA cells. The intrinsic bistability of the molecular charge configuration results in dipole or quadrupole fields which couple strongly to the state of neighboring molecules. We show how clocked control of the molecular QCA can be accomplished with a local electric field and lay out the "roadmap" towards integration of these molecules in large-scale circuits. Molecular QCA layers can be viewed as a new class of "digital material," which encodes and processes information with internal molecular degrees of freedom.

Session Z: High-K Dielectrics - II

Thursday PM Room: Saltair
June 26, 2003 Location: Olpin Union Building

Session Chairs: Paul McIntyre, Stanford University, Dept. of Matls. Sci. & Engrg., Stanford, CA 94305-2205 USA; G. Lucovsky, North Carolina State University, Physics Dept., Raleigh, NC 27695-8702 USA

1:30 PM Invited

Z1, Spectroscopic Studies of the Electronic Structure of Transition Metal and Rare Earth High-K Gate Oxides: *G. Lucovsky*[1]; G. B. Rayner[1]; G. Appel[1]; Yu Zhang[1]; J. L. Whitten[2]; J. H. Haen[3]; D. G. Schlom[3]; J. L. Freeouf[4]; R. Uecker[5]; P. Reiche[5]; [1]North Carolina State University, Dept. of Physics, Raleigh, NC 27695-8202 USA; [2]North Carolina State University, Dept. of Chmst., Raleigh, NC 27695 USA; [3]Pennsylvania State University, Dept. of Matls. Sci. & Engrg., University Park, PA 16802 USA; [4]OGI, Dept. of Electl. & Compu. Engrg., Portland, OR 97291 USA; [5]Institute of Crystal Growth, Berlin Germany

The electronic structures of transition metal, Tm, and trivalent rare earth, Re, binary (TmOx and Re2O3) and ternary mixed oxides (TmRexOy) are qualitatively different from those of silicon oxide, silicon nitride, and silicon oxy-nitride single-phase alloys (or solid solutions, hereafter designated as alloys). The lowest conduction band states are associated with localized anti-bonding d*-states of the Tm/Re atoms, rather than extended Si 3s*-states, and/or O/N 2p*-states. The properties of these localized d*-states for Tm/Re binary and ternary oxides including a) Y2O3, TiO2, ZrO2, and HfO2, b) Zr silicate and Hf aluminate alloys alloysmixtures, (ZrO2)x(SiO2)1-x and (HfO2)x(Al2O3)1-x, respectively, and c) LaAlO3, DyScO3, GdScO3, and SmScO3 compounds, have been studied by several complementary photon and electron spectroscopies, including X-ray photoelectron spectroscopy (XPS), Auger electron spectroscopy (AES), X-ray absorption spectroscopy (XAS), and spectroscopic ellipsometry (SE). Based on quantitative agreement between a) the Zr silicate anti-bonding state electronic structure obtained from Zr M2,3 and O K1 XAS spectra, and b) ab initio calculations on small clusters, the ordering and overlap of anti-bonding Zr 4d*, and 5s* states, and Si 3s* states in the O K1 spectra has been shown to 'replicate' significant features of the conduction band electronic structure that determine band-offset energies at Si/(ZrO2)x(SiO2)1-x-Zr silicate interfaces. These relationships have recently been extended to Re ternary oxide compounds, including LaAlO3 and GdScO3, through direct comparisons between O K1 XAS spectra, and band edge optical absorption constants obtained from analysis of SE measurements extending to 9 eV. These comparisons yield qualitatively different behaviors for Tm/Re silicate and aluminate alloysmixturesalloys containing a single Tm or Re species, and the Re-Tm ternary mixed oxide phases containing both Tm and Re species. As a direct result of near-neighbor interactions between Tm and Re d-states induced by bonding to a common O atom, ternary oxide minimum bandgaps, and hence conduction band offset energies are generally increased in oxide phases containing both Tm and Re species. This identifies new and technologically important opportunities for band gap 'engineering' at the atomic scale. For example, relative energy shifts of coupled Re and Tm d*-states are important for the ultimate scaling of CMOS devices since they increase the effective band gaps/offset energies for ternary oxides containing highly polarizable Sc, Ti, Nb, and Ta atoms above what had previously been proposed as a disabling limitation that had been inferred from the band gaps and/or band offset energies of their respective binary oxides.

2:10 PM Cancelled

Z2, Characterization of HfO2 Films for High-k Gate Application: *Joseph Kulik*[1]; Ran Liu[1]; N. V. Edwards[1]; S. Zollner[1]; R. Gregory[1]; X. D. Wang[1]; D. Werho[1]; D. Triyoso[2]; [1]Motorola, Inc., Process & Matls. Characterization Lab., 2100 E. Elliot Rd., MD EL622, Tempe, AZ 85284 USA; [2]Motorola, Inc., Advd. Products R&D Lab., 3501 Ed Bluestein Blvd., MD K20, Austin, TX 78721 USA

Currently there is still no clear front runner for the next alternative gate dielectrics despite extensive efforts. Much of the material research and integration development are focused on transition metal oxides and silicates, rare earth metal oxides and other oxides. This paper will present some recent results on materials and physical properties of HfO2 films grown on Si by atomic layer deposition (ALD). Extensive structural, compositional, and optical characterization has been carried out using transmission electron microscopy (TEM), atomic force microscopy, Rutherford backscattering spectrometry, Auger electron spectroscopy, X-ray diffraction, X-ray photo-electron spectroscopy, and optical spectroscopy (UV-Raman spectroscopy, spectroscopic ellipsometry, and IR transmission spectroscopy). Issues related to impurities, interfacial layers, and thermal stability will be addressed. A new characterization method, tunneling AFM, has also been developed to correlate electrical "hot spots" with film structures. Particular attention is given to the interface between the Si substrate and the HfO2 film, and we demonstrate the growth of films with no detectable interfacial layer. Electron energy loss spectroscopy with a 1-nm probe in the TEM is used to characterize these interfaces. Emphasis is placed on the spectral fine structure at the O K-edge and differences between fine structure observed at the interface as compared with that observed in the HfO2 film. Additional emphasis is given to the Si L-edge and possible differences in fine structure between the interface and the substrate.

2:30 PM Student

Z3, Transmission Electron Microscopy Investigations of the Structure and Stability of Gate Dielectrics: *Yan Yang*[1]; Zhiqiang Chen[1]; Lisa F. Edge[2]; Hao Li[3]; Y. Wei[3]; K. Eisenbeiser[3]; Darrell G. Schlom[2]; Susanne Stemmer[1]; [1]University of California, Matls. Dept., Santa Barbara, CA 93106-5050 USA; [2]Pennsylvania State University, Matls. Sci. & Engrg., Matls. Rsch. Inst. Bldg., University Park, PA 16802-6602 USA; [3]Motorola, Physl. Sci. Rsch. Lab., Tempe, AZ 85284 USA

Results on the stability and interface structure of LaAlO3 (LAO) and ZrO2 dielectric thin films on silicon, currently under investigation to replace SiO2 as a gate dielectric in CMOS, will be presented. LAO is of interest as an epitaxial gate dielectric because of its high dielectric constant, its favorable bandgap lineup with Si and its reasonable lattice match to Si. ZrO2 has been investigated extensively as an amorphous or polycrystalline gate dielectric. ZrO2 has been shown to form silicides during or after poly-Si gate electrode deposition. We present experimental studies on the mechanisms of zirconium silicide formation. High-resolution analytical capabilities are essential in analyzing the stability of these ultra-thin layers. We use high-resolution transmission electron microscopy (HRTEM), electron energy-loss spectroscopy (EELS) and atomic resolution Z-contrast imaging in scanning transmission electron microscopy (STEM). To investigate LAO stability, Si films were grown by molecular beam epitaxy (MBE) under UHV conditions and temperatures at or above 800°C on single crystal LaAlO3 substrates and annealed under a variety of annealing conditions. Results show that interfaces between Si and LAO are stable and free of reaction layers up to 1026°C. Using STEM Z-contrast imaging we analyze the atomic structure of the Si/LAO interface. For ZrO2 thin films, we analyze silicide formation mechanisms as a function of oxygen deficiency. Thermodynamic analysis shows that the silicide formation for oxygen nonstoichiometry greater

than 0.3% the silicide reaction will proceed. Experiments analyzing silicide formation as a function of deposition and annealing conditions will be presented. This research is sponsored by the SRC/Sematech Front End Process Center.

2:50 PM Student

Z4, Spin Dependent Recombination at Deep Level Centers at the 4H Silicon Carbide/Silicon Dioxide Interface: Nathaniel A. Bohna[1]; *David J. Meyer*[1]; Patrick M. Lenahan[1]; Aivars Lelis[2]; Robert S. Okojie[3]; [1]The Pennsylvania State University, Dept. Engrg. Sci. & Mech., 212 EES Bldg., University Park, PA 16802 USA; [2]US Army Research Laboratory, 2800 Powder Mill Rd., Adelphi, MD 20783 USA; [3]NASA-Glenn Research Center, 21000 Brookpart Rd., Cleveland, OH 44135 USA

SiC devices are potentially superior to conventional silicon based devices in high temperature and high power applications.[1, 2] Previous studies have identified impurity and intrinsic defects in SiC materials; however, virtually nothing is known about the physical or chemical nature of the specific point defects that limit the performance of SiC devices. In this study we focus on deep level defects at the SiO2/SiC interface in SiC-based MOSFETs. We have utilized a particularly sensitive form of electron spin resonance (ESR) called spin dependent recombination (SDR)[3] to identify deep level traps at the interface of 4H silicon carbide and SiO2 gate dielectrics in SiC MOSFETs. To the best of our knowledge, these are the first SDR measurements ever made on SiC based devices. SDR is an ESR detection technique many orders of magnitude more sensitive than conventional ESR, which is exceptionally well suited to characterize interface defects in semiconductor devices. The technique is similar to conventional ESR: a sample is simultaneously exposed to microwaves and a large magnetic field. Unlike conventional ESR, the resonance measurement involves changes in current flowing through the device. We have applied the technique to SiC MOSFETs that have been configured as gate controlled diodes. At moderate forward bias voltage, and with appropriate gate potential, the device currents are dominated by recombination events at the SiC/dielectric interface. When the ESR resonance condition is satisfied in the cavity, the change in recombination current is measured at the interface due to deep level traps. We have made SDR measurements over a wide range of gate and source/drain junction bias of the gate-controlled diodes. We observe very strong SiC/SiO2 defect signals, centered near g=2.000, apparently involving several as yet poorly resolved lines. A limited series of observations at various orientation of the "c" axis versus the magnetic field strongly suggests that the dominating defect involves unpaired electrons on carbon atoms. The spectra exhibit a dependence on gate voltage that very closely correlates to the recombination current in the diode as a function of gate bias. This result strongly suggests that the observed defects play a dominating role in the SiC/SiO2 interface density of states. Over the next few months, careful measurements will be conducted to fully characterize the spectra as a function of crystallographic orientation with respect to the magnetic field. These measurements will allow a much more detailed and definitive identification of these defect centers. [1]P.G. Neudeck etal, Proc. IEEE, 90, 1065-1076 (2002). [2]S.K. Powell etal, Semiconductor Device Research Symposium, 572-574A (2001). [3]D.J. Lepine, Phys. Rev. B, 6, 436-441 (1972).

3:10 PM Break

3:30 PM Cancelled

Z5, Effect of SiOx Content on Electrical and Morphological Properties of HfSiOx Thin Films: *Koray Karakaya*[1]; Dave H.A. Blank[1]; [1]University of Twente, MESA+ Rsch. Inst., PO Box 217, Enschede 7500AE The Netherlands

We have investigated the morphological and electrical properties $HfSiO_x$ thin films with SiO_x content of 10-20-50% (at.) respectively. Targets are prepared by mixing high purity HfO_2 and SiO_2 powders and sintered at oxygen atmosphere. Film deposition has been done at different temperatures, varies from room temperature to 500°C, on hydrogen passivated and chemical oxide silicon substrates, by UHV pulsed laser deposition system equipped with high pressure RHEED. KrF laser with a pulse duration of 10 ns is used for ablation. Films grown on HF dipped substrates are deposited under Ar and films grown on chemical oxide substrates are deposited under oxygen pressure. Substrate properties are checked before deposition by RHEED and also film growth is monitored in situ by means of high pressure RHEED system. Electrical (C-V and I-V) and morphological properties of films are examined before and after annealing.

3:50 PM

Z6, Combinatorial Ternary Phase Diagramming for Discovery of New Gate Materials and their Characterizations: *T. Chikyow*[1]; P. Ahmet[2]; K. Nakajima[2]; N. Okazaki[2]; K. Fujimoto[2]; M. Watanabe[2]; K. Hasegawa[3]; T. Tamori[3]; T. Hasegawa[3]; T. Aoyama[3]; H. Koinuma[3]; [1]COMET-NIMS, National Institute for Material Science, Nanomatl. Rsch. Labs., 1-2-1 Sengen, Ibaraki, Tsukuba 305-0047 Japan; [2]COMET-NIMS, National Institute for Material Science, Advd. Matl. Labs., 1-1 Namiki, Tsukuba, Ibaraki 305-0044 Japan; [3]Tokyo Institute of Technology, Matls. & Structures Lab., 4259 Nagatsuta, Midori-ku, Yokohama 226-8503 Japan

A ternary phase diagramming for discovering new gate insulator was demonstrated using combinatorial synthesis and characterization and HfO2-based ternary oxide was found as a new gate insulator which had stable amorphous structure with higher dielectric property. For the increasing number of MOS transistors on Large Scale Integrated Circuit (LSI), materials which have been used in the device is closing to their physical limitation. Especially gate oxide material becomes the most serious problem and a lot of efforts have been made to find new candidates of having higher dielectric property. The requirements for the new materials are 1) higher dielectric property, 2) amorphous material 3) low interfacial states at oxide/Si interface. As the candidate, HfO2 or ZrO2 has been proposed and the property has been investigated. The problem of these materials is that they tend to be crystalline around 300 C and have rather poor electric property. To avoid the crystallization, a mixing with another oxides have been tried. However the answer is not found yet. To discover a stable amorphous oxide of higher dielectric, the ternary phase diagramming is expected to be effective. For this purpose, newly designed combinatorial growth system is developed. In this system, with a substrate rotation and a computer controlled moving mask system, a ternary phase diagramming and binary phase diagramming are demonstrated simultaneously on a substrate. Dielectric properties are characterized by scanning microwave microscope and structures are investigated by combinatorial x-ray measurement system and transmission electron microscopy combine with micro sampling technique. Throughout the experiments, newly designed combinatorial synthesis system was proved to be effective in discovering new gate insulator.

Session AA: AlGaN/GaN HEMTs: Growth

Thursday PM Room: Panorama East
June 26, 2003 Location: Olpin Union Building

Session Chair: Andrew Allerman, Sandia National Laboratories, Albuquerque, NM 87185 USA

1:30 PM Student

AA1, Correlation Between Dislocation Density and Mobility of GaN Based HEMTs: *Allen M. West*[1]; Stephen R. Lee[1]; Andrew A. Allerman[1]; Daniel D. Koleske[1]; Steven R. Kurtz[1]; Karen E. Waldrip[1]; Jeffrey J. Figiel[1]; Cammy R. Abernathy[2]; [1]Sandia National Laboratories, PO Box 5800, MS 0601, Albuquerque, NM 87185 USA; [2]University of Florida, Matls. Sci. & Engrg., 100 Rhines Hall, PO Box 116400, Gainesville, FL 32611-6400 USA

Gallium nitride based high electron mobility transistors (HEMTs) demonstrate tremendous promise in terms of power density at high frequencies. For example, GaN HEMTs grown on silicon carbide (SiC) have already demonstrated power densities >10 times that of GaAs HEMTs, and there is promise of further improvements as the technology develops. A significant factor currently limiting GaN HEMT device performance is the high dislocation density associated with GaN films grown heteroepitaxially on SiC. Threading dislocations in the GaN limit mobility by trapping electrons in the HEMT channel. The purpose of this study is to evaluate the correlation between dislocation density and mobility and to compare methods for measuring dislocation density using X-ray diffraction (XRD). Since XRD methods are both non-destructive and quick relative to transmission electron microscopy (TEM), larger numbers of films are readily studied. Here, a series of XRD scans have been performed on ten samples grown by metal-organic chemical vapor depo-

sition (MOCVD) under various conditions. The mobility of the HEMTs range from 327 cm2/V-s to 1830 cm2/V-s. XRD analysis was performed for (0002), (0004), and (0006) symmetric scans, as well as (10-11) and (20-22) asymmetric scans in skew-symmetric geometry. The symmetric scans give both the variation in tilt of the GaN epilayer, and the lateral coherence length due to threading dislocations with a screw component; while the asymmetric scans give the variation in twist of the GaN epilayer, and the lateral coherence length due to threading dislocations with both screw and edge components. From these, threading dislocation densities were calculated using two separate models. The first is to derive dislocation density from the measured tilt and twist widths using the methods previously summarized by Metzger et al.[1] The second method is to use coherence length as a direct measurement of average dislocation spacing. We will present a comparison of the two methods of treating the XRD data. Correlation of dislocation density measurements with mobility data clearly indicates that mobility decreases with increasing dislocation density. More importantly, room temperature mobilities >1800 cm2/V-s require threading dislocation densities <1x109 cm-2 in the GaN channel. Ongoing research will compare the measured dislocation density from XRD with atomic force microscopy (AFM) measurements. The AFM morphology will also be correlated with mobility and device performance. Finally, TEM comparisons are in progress for benchmarking purposes. Progress towards correlating XRD, AFM, and TEM results for dislocation density will be reported. [1]Metzger et al., Phil. Mag. A 77, 1013 (1998). Sandia National Laboratories is a multi program laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the Department of Energy under Contract DE-AC094-94AL85000.

1:50 PM Student

AA2, Improved Performance of AlGaN/GaN HEMTs Grown by Metalorganic Chemical Vapor Deposition: *Michael M. Wong*[1]; Uttiya Chowdhury[1]; Raymond Kirk Price[2]; Ting Gang Zhu[1]; Dongwon Yoo[1]; Milton Feng[2]; Russell D. Dupuis[1]; [1]The University of Texas at Austin, Microelect. Rsch. Ctr., 10100 Burnet Rd., Bldg. 160, Austin, TX 78758 USA; [2]The University of Illinois at Urbana-Champaign, Ctr. for Compound Semiconductor Microelect., 208 N. Wright St., Urbana, IL 61801 USA

For AlGaN/GaN microwave-power HEMTs, a high current gain cutoff frequency along with a high saturation current is of essential importance for high-frequency and high-power device applications. Conventional modulation-doped AlGaN/GaN HFET structures have been extensively studied. However, other HFET device elements, such as delta-doping and binary barriers, can potentially improve the high-power transistor electrical characteristics. In this study, we present the results of a series of devices utilizing various novel epitaxial device structures. We demonstrate devices that exhibit high mobility-sheet charge product, a large maximum drain current, a high frequency response, and large transconductance values. The AlGaN/GaN heterostructures of this work are grown by low-pressure metalorganic chemical vapor deposition on 2.0 in. diameter 6H n-type and 4H semi-insulating SiC, and sapphire substrates. From DC device comparisons, there is a clear advantage in using SiC substrates. The use of a thin AlN barrier layer at the AlGaN-GaN interface can increase the effective conduction band offset to increase the sheet charge density without reducing the mobility, and reduce alloy scattering, resulting in a large $n_s\mu$ product. In addition, delta doping can be used to further increase the charge density in the 2DEG. An AlGaN/AlN/GaN structure utilizing both these features resulted in 300K Hall mobility of 1,058 cm^2/V-s and a sheet carrier density of 2.35×10^{13} cm^{-2}, yielding a large $n_s\mu$ product of ~2.5×10^{16} /V-s. This structure should be capable of high-speed operation at high power densities. Furthermore, the use of the AlN binary compound barrier was studied in modulation doped structures (i.e., MODFETs). In a MODFET structure without using an additional AlN barrier layer, the room temperature Hall measurements resulted in a mobility of 863 cm^2/V-s and a sheet carrier density of 2.05×10^{13} cm^{-2}, yielding an $n_s\mu$ product of ~1.8×10^{16} /V-s. When the binary barrier was inserted in the MODFET design, the mobility and sheet carrier density increased to 1335 cm^2/V-s and 2.10×10^{13} cm^{-2}, respectively. This resulted in a high $n_s\mu$ product of ~2.8×10^{16} /V-s. Devices have been fabricated and tested. For the delta-doped, binary barrier structure, devices with gate lengths varying from 0.5 µm to 0.15 µm were processed. We have achieved peak DC transconductances g_m~330 mS/mm with maximum current densities I_{DSmax}~1.8 A/mm at V_G=+1 V, with L_G = 0.15 µm. High-frequency measurements yielded an extrapolated (20 dB/decade) f_t=70 GHz and f_{max}=115 GHz. We will also report on the performance comparison for the MODFET devices.

2:10 PM Student

AA3, AlGaN/GaN HEMTs on Si Substrates: Influence of Layer Structure on Device Performance: *Peter Javorka*[1]; Juraj Bernát[1]; Yilmaz Dikme[2]; Alfred Fox[1]; Michel Marso[1]; Rolf Jansen[2]; Michael Heuken[3]; Hans Lüth[1]; Peter Kordos[1]; [1]Institut für Schichten und Grenzflächen, Rsch. Ctr. Jülich, Jülich D-52425 Germany; [2]Institut für Theoretishe Elektrotechnik, RWTH Aachen, Aachen D-52074 Germany; [3]Aixtron AG, Aachen D-52072 Germany

The influence of layer structure on the performance of AlGaN/GaN/Si HEMTs was investigated. The structures were grown on Si(111) substrates by LP-MOVPE[1]. They are polarization-based undoped (25 nm AlGaN on top of GaN) as well as conventionally doped (25 nm total thickness of spacer+carrier-supply+cap layers, Si doping density 2E18-1E19 cm^{-3}), all with 25-30% Al content in the AlGaN. Multifinger HEMTs with gate lengths of 0.3-0.7 µm and total gate widths of 100-400 µm were prepared by conventional processing steps[2]. Hall-effect measurements yielded sheet carrier concentrations of (0.8-1.3)E13 cm^{-2} with carrier mobilities up to 1280 cm^2/Vs. The performance of the prepared devices was studied by DC, CV and microwave small-signal (scattering parameters) characterization as well as by large-signal (load-pull) measurements to evaluate the output power at 2 GHz, all using an on-wafer probe setup. The DC characterization shows that the devices with (2-5)E18 cm^{-3} doping exhibit a higher drain saturation current density (~0.8 A/mm at VG = +1 V) and peak extrinsic transconductance (~220 mS/mm) than those on undoped and 1E19 cm^{-3} doped structures. On the other hand, the breakdown voltage decreases with increasing doping density, ~90 V for undoped and ~45V for 1E19 cm^{-3} devices at the same source-drain separation. The small-signal measurements yielded a unity gain cutoff frequency f_T of 16.5, 25 and 35 GHz (the pad parasitics de-embedded) for 5E18 cm^{-3} devices with 0.7, 0.5 and 0.3 µm gate lengths, respectively. Devices with another doping density show up to 30% lower f_T-values. The f_{max}/f_T ratio increases from ~1 to 1.5 when the gate length increases from 0.3 to 0.7 µm. This behavior was observed also previously[2]. The microwave power capability of a HEMT relates to its DC parameters as $P_{rf} = (\Delta V \times \Delta I)/8$, where ΔV is the difference between the source-drain breakdown and knee voltages, ΔI is given by the maximum drain current. Thus, better power performance should be expected for undoped (higher V_{br}) and/or lower doped (higher $I_{D,sat}$) devices. However, 2-3 times higher power densities and higher PAE´s at 2GHz are obtained on devices with higher doping, which correlates with the product of V_{br} and $I_{D,sat}$. On the other hand, this underlines an advantage of doped structures for GaN-based power devices. [1]Y. Dikme et al., J. Cryst. Growth 248, 578 (2003); [2]P. Javorka et al., Electron. Lett. 38, 288 (2002).

2:30 PM Student

AA4, The Influence of Layer Parameters on the 2DEG Density in AlGaN/GaN Heterostructures: *Stefan Karl Davidsson*[1]; Manjula Gurusinghe[2]; Thorwald Andersson[2]; Herbert Zirath[1]; [1]Chalmers University of Technology, Dept. of Microelect., Microwave Elect. Lab., Göteborg 412 96 Sweden; [2]Chalmers University of Technology, Dept. of Microelect. & Nanosci., Appl. Semiconductor Physics, Göteborg 412 96 Sweden

We have studied the energy levels and the charge density of the two-dimensional electron gas (2DEG) in AlGaN/GaN heterostructures. The charge confinement was calculated using a one-dimensional Schrödinger-Poisson model. The simulations used the Al-content in the AlGaN layer, the thickness of the AlGaN layer and the unintentional doping in the GaN buffer layer as input parameters. The calculated 2DEG densities were compared to measured values of AlGaN/GaN samples characterized by electrical measurement. The calculations showed that the Al-content in the AlGaN barrier layer is the key parameter when determining the energy states in the quantum well. By raising the aluminium content the bandgap offset and polarization charge at the heterostructure interface increase, which lead to tighter electron confinement. The influence of the AlGaN layer thickness on the 2DEG properties was less pronounced. The density increases with AlGaN thickness, even though the dependence is weaker than for the Al-content. The upper limit for the thickness is given by the critical layer thickness of AlGaN grown on GaN. For thin layers the electrons in the 2DEG can tunnel through the AlGaN layer. Therefore, this effect sets a lower limit on the layer thickness. The third parameter that has been considered in the simulations is the unintentional doping in the GaN buffer layer. A higher doping resulted in a higher

electron density in the 2DEG. In the experimental part AlGaN/GaN heterostructures were grown by molecular beam epitaxy and characterized by Capacitance-Voltage and Hall effect measurements. A general result was that the samples had large 2DEG densities, above $1.5x10^{13}$ cm^{-2}. To simulate such values, the influence of the unintentional doping had to be considered. For an Al-content of 40% and a 40 nm AlGaN layer the measured 2DEG density was $2.5x10^{13}$ cm^{-2}. This value was simulated for a doping of $2x10^{18}$ cm^{-3}. To investigate the unintentional doping, Capacitance-Voltage and Hall measurements were performed on GaN samples, which had been grown at the same conditions as the AlGaN/GaN samples. The doping was measured to 10^{18} cm^{-3}, which is in accordance with the asserted value used in the simulation. In samples with aluminium concentrations from 20% to 40%, the 2DEG density increased with aluminium content. The AlGaN thickness was either 20 or 40 nm. The measurements showed a higher 2DEG density for the thicker layer, with an increase in accordance with calculations. In conclusion, when the unintentional doping level is treated as a crucial parameter in the AlGaN/GaN heterostructure, the experimental results for our samples can be accurately described by a one-dimensional Schrödinger-Poisson model.

2:50 PM

AA5, Bow Reduction of AlGaN/GaN HEMT Structures Using Interlayers by MOVPE: *Masahiro Sakai*[1]; Takashi Egawa[2]; Hiroyasu Ishikawa[2]; Takashi Jimbo[2]; [1]Nagaya Institute of Technology, Rsch. Ctr. for Micro-Struct. Devices (On leave from NGK Insulators, Ltd.), Gokiso-cho, Showa-ku, Nagoya, Aichi 466-8555 Japan; [2]Nagaya Institute of Technology, Rsch. Ctr. for Micro-Struct. Devices, Gokiso-cho, Showa-ku, Nagoya, Aichi 466-8555 Japan

Sapphire or SiC substrates are widely used for the growth of nitride-based devices. However, the epitaxial wafer largely bows after the growth due to the thermal expansion coefficient mismatch between substrate and epitaxial film. Large bowing of epitaxial wafers brings about the difficulty in the device photolithography process. For the mass-production of nitride-based electronic devices, large diameter epitaxial wafers larger than 100 mm must be processed. However, the growth on large diameter substrates causes increased bowing of epitaxial wafers. So far, bow reduction of epitaxial wafers has not been taken a proactive approach. In this paper, we studied the MOVPE growth of AlGaN/GaN heterostructures with interlayers as a method for reducing the epitaxial wafer bowing, using 50-mm-diameter sapphire substrates. The epitaxial layer consists of, from bottom to top, a 30-nm-thick low-temperature GaN buffer layer, an undoped GaN layer, an interlayer, an undoped GaN layer, a 7 nm undoped $Al_{0.26}Ga_{0.74}N$ spacer layer, a 15 nm Si-doped $Al_{0.26}Ga_{0.74}N$ supply layer with the doping level of 4×10^{18} cm^{-3} and a 3 nm undoped $Al_{0.26}Ga_{0.74}N$ barrier layer. The total thickness of the GaN layer with interlayers was 3 µm. The position and thickness of the interlayer in the GaN layer has been varied. The diameter of sapphire substrates is 50 mm, the orientation is c-face and the thickness is 330 µm. Most interlayers including indium have the effect of suppressing the bowing. We found that InGaN/GaN multilayer was the most effective for reducing the bowing. While the bowing value of 3-µm-thick GaN films was approximately 30 µm, the InGaN/GaN multilayer with ten periods in GaN layers grown on sapphire substrates suppressed the bowing approximately up to 9 µm. Here, the bowing value was measured at the center of the epitaxial wafer. When the InGaN/GaN multilayer was used as the interlayer, better surface morphology was realized compared with the InGaN single layer. The electron mobility was 1083 cm^2/Vs with the sheet carrier concentration N_s of 1.1×10^{13} cm^{-2} at room temperature and 4997 cm^2/Vs with N_s of 1.1×10^{13} cm^{-2} at 77K. In addition, the sheet resistance of the samples with interlayers did not change so much. The full width at half maximum of the X-ray rocking curve was 259 arcsec for the (0004) reflection. The crystalline quality of the present GaN film with interlayers found to be satisfactory and the same quality of the GaN film without the interlayers was obtained. In conclusion, we studied the bow reduction effect of the interlayers in AlGaN/GaN HEMT structures on sapphire substrates. InGaN/GaN multilayers are promising as the interlayer for the suppression of epitaxial wafer bowing.

Session BB: SiC: Defects, Processing and Devices

Thursday PM Room: Auditorium
June 26, 2003 Location: Olpin Union Building

Session Chairs: Philip Neudeck, NASA Glenn Research Center, Cleveland, OH 44135-3127 USA; Robert Stahlbush, Naval Research Laboratory, Washington, DC 20375 USA

1:30 PM

BB1, Dependence of Stacking Fault Growth on Current Density and Stress in SiC PiN Diodes: *R. E. Stahlbush*[1]; M. Fatemi[1]; M. E. Twigg[1]; J. B. Fedison[2]; J. B. Tucker[4]; S. D. Arthur[4]; S. Wang[3]; [1]Naval Research Laboratory, Code 6813, Washington, DC 20375 USA; [2]General Electric, Global Rsch. Ctr., Niskayuna, NY 12309 USA; [3]Sterling Semiconductor, Danbury, CT 06810 USA

A major problem with SiC bipolar power devices is the formation of stacking faults during device operation. The stacking faults degrade the minority carrier lifetime and increase the forward voltage drop, Vf. Furthermore, the formation of stacking faults is erratic. For example, PiN diodes from the same wafer can have Vf drift that varies more than order of magnitude. There are also strong temporal variations. In some cases the onset is immediate, while in other cases the onset is delayed. In this presentation, much of this complicated behavior is explained by variations of the local stress and how the combination of stress and current density affects the growth of individual stacking faults. During forward bias, all of the current passing through the drift region results in electron-hole recombination and this recombination drives the stacking fault growth. There is evidence that stress plays a dual role. Depending on the local stress field, it can either promote or impede the stacking fault growth. TEM analysis has shown that all of the stacking faults that grow during PiN diode operation are Shockley type. This type is not a coalescence of vacancies or interstitials, but rather a shear displacement in response to the local stress. With light emission imaging the growth of individual stacking faults can be monitored during device operation. In PiN diodes, we have previously observed that some stacking faults continue growing until they span the device while others are pinned after their initial growth. The pinning was attributed to a local stress barrier. Increasing the current density can often force the growth to restart. We suggest that the growth of individual stacking faults is linear with the recombination if the recombination rate is sufficiently large to overcome local stress barriers to growth. We will show examples of stacking fault growth in which the growth is linear with the charge passed through the diode as the current density varies more than an order of magnitude. In these examples, the potential barriers are sufficiently small so that the stacking fault growth is not impeded through the range of current densities. In other examples, pinned stacking fault growth resumes after momentarily increasing the current density and continues after dropping the current density to its original value. We are also in the process of making localized strain measurements using double crystal x-ray rocking curve technique. The measurements are confined to small area (100 x 100 µm) making it possible to compare regions with stacking fault pinning to regions without pinning.

1:50 PM

BB2, Partial Dislocations and Stacking Faults in 4H-SiC PiN Diodes: *Mark E. Twigg*[1]; Robert E. Stahlbush[2]; Mohammad Fatemi[2]; Jeffrey B. Fedison[3]; Jesse B. Tucker[3]; Steven D. Arthur[3]; Shaoping Wang[4]; [1]Naval Research Laboratory, Code 6812, Elect. Sci. & Tech. Div., 4555 Overlook Ave. S.W., Washington, DC 20375 USA; [2]Naval Research Laboratory, Elect. Sci. & Tech. Div., 4555 Overlook Ave., S.W., Washington, DC 20375 USA; [3]General Electric Global Research Center, Niskayuna, NY 12309 USA; [4]Sterling Semiconductor, Danbury, CT 06810 USA

Using plan-view and cross-sectional transmission electron microscopy (TEM), we have identified many of the features of stacking faults that grow during the bias of 4H-SiC PiN Diodes. Plan-view TEM has

proved particularly useful, in that the partial dislocations bounding the stacking fault can be identified. In particular, partial dislocations threading from the top to the bottom of the 4H-SiC layer can be uniquely determined using dislocation parity analysis. Thus far, four stacking faults have been identified as faulted 60° dislocations. All four of these faulted dislocations are bound by Si-core partials, with the separation between partials ranging from 10-20 microns. Stacking faults with hundreds of microns between bounding partials were assumed to be partial dislocation loops, and were large enough that they were seen to expand during light emission imaging (LEI) of the biased PiN diode. The expansion of these partial dislocation loops was found to be consistent with the action of Peach-Koehler forces on partial dislocations responding to tension or compression in vicinally-grown 4H-SiC films. That these faulted loops were seen to respond to tension as well as compression indicates that the leading partials of this faulted dislocations loops could be either Si-core or C-core. In order to more completely determine the structure of these dislocation loops, we will study loops at earlier stages of electrically-driven growth. Faults at an earlier stage of growth have the advantage that the bounding partials are sufficiently close together to facilitate the viewing of both partials in plan-view TEM. It may also be important to determine the structure of the fault before it has run its course through the foil.

2:10 PM

BB3, Study of Forward Voltage Drop Degradation in Diffused SiC PIN Diodes: *Stanislav Soloviev*[1]; Dmitry Cherednichenko[1]; Ying Gao[2]; Yuefei Ma[1]; Alexander Grekov[1]; Tangali S. Sudarshan[1]; [1]University of South Carolina, Electl. Engrg., 301 S. Main St., Swearingen Bldg., Columbia, SC 29208 USA; [2]Bandgap Technologies, Inc.

The degradation of diffused SiC PIN diodes during forward-biased operation has been studied in this work. The PIN diodes have been formed by selective diffusion of aluminum and boron into a 4H-SiC substrate with a 10 µm thick epilayer doped by nitrogen up to $5x10^{15}cm^{-3}$. The diffusion was carried out at a temperature of 2000°C in argon ambient. The high-density graphite crucible was charged with silicon carbide powder mixed with elemental boron and Al_4C_3 as the source of acceptor dopants. The standard photolithography process was employed to fabricate the planar p-n diode structures. The forward voltage drop, V_f, and the emitted electroluminescence spectra vs. time were measured simultaneously during the degradation test under an applied current density of $100A/cm^2$ at the temperatures 75, 100 and 150°C. The initial forward voltage drop was 3.5 V and it began to quickly increase over a specific period of time dependent on the diode temperature. The above studies allowed us to estimate the effective activation energy of the degradation process, which was about 0.1 eV. The electroluminescence spectra measured before diode degradation, exhibited one characteristic peak at the wavelength of 483 nm, which is associated with donor-acceptor pair recombination. However, a new peak with a wavelength of 428 nm in the EL spectra appeared as V_f increased. Moreover, the intensity of this peak increased steadily with the increase in V_f. Analysis of the I-V characteristics showed that diode series resistance increased ten-fold due to degradation. Considering that the increasing of series resistance is associated with electron trap generation in the n^--base region, the concentration of the generated trap centers as well as their position in bandgap were estimated based on the equation of electrical neutrality and the temperature dependence of diode series resistance RS. The calculations have shown that the concentration of the electron trap centers was about $5x10^{15}cm^{-3}$and their energy level in bandgap, ΔE_t, was about 0.4±0.1 eV. Based on analytical calculations, it was shown that impurity concentration gradients induce lattice stresses due to different radii of dopant and host atoms. If the value of the stresses exceeds the stress yield (~1 MPa for SiC), mismatch dislocations might be generated. During the PIN diode degradation test, the residual stresses might generate additional electrically active broken chemical bonds. These broken bonds can be carrier traps, which might result in series resistance increase during PIN diode operation. Calculations of the broken bond density, based on the concentration profiles of the given dopant atoms, were in agreement with that obtained from analysis of I-V characteristics described above.

2:30 PM

BB4, Vanadium, Carbon Vacancies, and Boron in Semi-Insulating SiC: *Mary Ellen Zvanut*[1]; Valeriy Konovalov[1]; William W. Mitchel[2]; William D. Mitchell[3]; [1]University of Alabama at Birmingham, Physics, 1300 University Blvd., 310 CH, Birmingham, AL 35294-1170 USA; [2]Air Force Research Laboratory, AFRL/MLPS, 3005 P St., Rm. 243, Wright Patterson AFB, OH 45433-7707 USA

Understanding the role of electrically active point defects is important for developing semi-insulating (SI) SiC substrates for electronic applications. We have investigated the carrier activation energy (Ea) and types of uncompensated point defects in SiC grown by two of the methods presently used to form SI substrates, vanadium-doping and high purity sublimation (HPSI). The activation energy for all the samples indicates that the conductivity is determined by deep level defects; however, Ea varies between 1.1 and 1.6 eV. Electron paramagnetic resonance (EPR) data reveal the species responsible for Ea, and photo-induced EPR demonstrates charge transfer between the boron acceptor and additional deep levels. Ea was calculated from the temperature dependence of the carrier concentration or Hall resistivity measured between 400 and 900 K. EPR spectra were measured at 4K in the dark and after illumination at selected wavelengths. SIMS was used to measure the vanadium concentration. The vanadium concentration in the intentionally doped samples are 4x1017, 6x1016 and 4x1016 cm-3 and Ea is 1.1, 1.1, and 1.6 eV, respectively. In the HPSI samples, 6x1015 cm-3 V were detected and Ea =1.2-1.5 eV. Neither the SIMS data nor Hall results provide any information about the defect responsible for diverse values of Ea. Our EPR measurements performed prior to illumination, when the spectrum should represent only those centers that remain uncompensated, give some clarification for these diverse Ea values. At least 1016 cm-3 V3+ is seen in the wafers for which Ea=1.1 eV. Although the role of this species is not yet clear, the presence of V3+ suggests that the Fermi level is above the 1.6 eV V5+/4+ level, consistent with the lower Hall activation energy of 1.1 eV. No vanadium EPR signal is detected and 1014 cm-3 uncompensated carbon vacancies (Vc) are found in the HPSI samples (Ea=1.2-1.5 eV). Photo-induced EPR measurements of HPSI SiC reveal a decrease in the density of carbon vacancies and simultaneous increase in boron acceptors after optical illumination at energy greater than 1 eV. Since the energy required to capture a hole by boron is known to be only 0.3-0.4 eV, the photo-threshold must represent electron excitation from the shallow acceptor or valence band to Vc. This places a carbon vacancy level at E-Ev=1-1.5 eV, a range inclusive of Ea. A photo-induced boron threshold at 1.3 eV is also observed in the intentionally vanadium-doped samples. Since Hall results show that the V-doped material is n-type, the photo-EPR threshold and Ea cannot represent the same process. Rather, the boron threshold indicates the presence of levels energetically below that detected in the Hall measurements. We will discuss the likely charge transfer mechanisms between boron and other deep levels in V-doped and high purity semi-insulating SiC. The work is supported by AFOSR (WPAFB) and Dr. Colin Wood, ONR (UAB).

2:50 PM Student

BB5, Traps in Double Implanted 4H-SiC Diodes: *Souvick Mitra*[1]; Mulpuri Venkata Rao[1]; Nick Papanicolaou[2]; Ken Jones[3]; O. Wayne Holland[4]; [1]George Mason University, Dept. of Electl. & Compu. Engrg., 4400 University Dr., MSN 1G5, Fairfax, VA 22030 USA; [2]Naval Research Laboratory, 4555 Overlook Ave. SW, Washington, DC 20375 USA; [3]Army Research Laboratory, Adelphi, MD 20783-1197 USA; [4]University of North Texas, Dept. of Physics, Denton, TX 76203-4127 USA

Double implantation technology consisting of deep MeV energy range acceptor/donor ion implantation followed by shallow keV range donor/acceptor implants is necessary for making complementary field effect transistors and high power devices such as thyristors and IGBTs. It is, therefore, very important to study and characterize the deep level defects created by the double implantations, which might limit the device performance. Despite the importance of the n^+-p/ p^+-n junction created by double implantation technology and its application to power switching device operation, to our knowledge there have not been any reports on DLTS characterization of double implanted diodes made in 4H-SiC. In this work, planar n^+-p and p^+-n junction diodes fabricated in 4H-SiC epitaxial layers using double implantation technology (successive selective area, multiple energy acceptor and donor implants) were characterized for their deep level behavior through capacitance Deep Level Transient Spectroscopy (DLTS). Either Al or B was used as the acceptor species and N or P as the donor species with all implants performed at 700°C and annealed at 1600-1650°C with an AlN protection cap. Ni and Ti/Al were used as the ohmic contacts for n- and p- type regions, respectively. The high leakage current behavior of the p^+-n junction diodes is correlated with a higher magnitude of trap concentrations in these de-

vices, compared to the n^+-p diodes. Implant damage created by higher dose Al implantations of p^+-n diodes compared to the lower dose N implantations of n^+-p diodes is believed to be responsible for a high trap concentration and a high reverse leakage current density in the p^+-n diodes. Higher Al doses are required due to a higher ionization energy of Al in SiC. All of the nitrogen implanted diodes showed a prominent peak at E_V + 0.5 eV, which is identified as a trap created due to nitrogen-defect complex center. The trap concentration has the highest value near the metallurgical junction of the diodes, which clearly shows the role of implantation-induced damage in the formation of this peak. For all Al implanted diodes, two prominent peaks at ~ E_C - 0.27 eV and ~ E_V + 0.42 eV, originated from Al-defect complex centers are observed. Also a prominent boron related D- center trap at ~ E_V + 0.63 eV is seen in DLTS spectrum of all diodes, except for devices with a phosphorus implanted deep donor region. In phosphorus implanted diodes, three distinct peaks at ~ E_V + 0.6 eV, E_V + 0.7 eV and E_V + 0.92 eV are observed. The deep center at E_V + 0.7 eV can be attributed to a point defect. Higher trap concentrations in p^+-n diodes compared to the n^+-p diodes led to a higher reverse leakage currents in p^+-n diodes.

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BB6, Silicon Carbide-Oxide Interfaces: The Role of Charged Defects on High Temperature Device Performance: *Ruby Nandini Ghosh*[1]; Peter Tobias[1]; Brage Golding[1]; [1]Michigan State University, Ctr. for Sensor Matls., 2167 Biomed Phys. Scis., E. Lansing, MI 48824-2320 USA

Devices based on the wide band gap semiconductor silicon carbide have the potential to operate in high temperature environments; application include control electronics for turbines and chemical sensors for power plant emissions. The performance of SiC based metal-oxide-semiconductor (MOS) devices in these environments will depend on electronic processes at the constituent interfaces within the structure. From in-situ measurements at high temperature (up to 800K), we show that the presence of charged states at the oxide-SiC interface significantly influences gate control of the semiconductor carrier concentration. Since hermetically sealed packaging technology is not widely available for electronic components operating at temperatures above 650K, we investigated the effect of ambient gases on SiC MOS structures at high temperature. The devices were characterized via capacitance - voltage spectroscopy in a system that allows for pA and fF measurements up to 900K in a controlled gas environment. In a reducing ambient the interface state density (Dit) in the upper half of the bandgap is that of an ideal capacitor, within our experimental uncertainty, with an approximately constant 1 E 11 states/cm2 -eV in the energy range 0.3eV < Ec - E < 0.9eV. In an oxidizing environment the interface state density is significantly higher, and a strong function of the position of the Fermi energy (Ef) within the band gap. As Ef is swept from midgap to the conduction band edge, the magnitude of Dit increases and the lifetime of the interface states also becomes longer by orders of magnitude. We show that the optimum bias point with respect to device stability and device-to-device repeatability for SiC MOS devices is near midgap. When Ef is positioned near the conduction band, charging and discharging from slow interface states leads to long term variations in the MOS capacitor bias. Our results are valid for SiC n-type field-effect structures in general. They have been observed on both the 4H and 6H polytypes, and are independent of the specifics of device fabrication processes such as the oxidation (wet or dry) and metallization (sputtered or e-beam deposited). We discuss how environmentally induced changes in interface state density, affect the design of drift free MOS devices operating in harsh, high temperature ambients.

3:50 PM

BB7, Reduction of the Interface Trap Density of the 4H-SiC (11-20)/ SiO2 Interface: *Sarit Dhar*[1]; [1]Vanderbilt University, Interdisciplinary Matls. Sci., PO Box 1807, Sta. B, Nashville, TN 37235 USA

Low inversion layer mobilities in 4H-SiC MOSFETs have been a major issue in the development of reliable SiC MOS power devices. Until recently, MOSFETs built on the conventional (0001) Si terminated face of 4H-SiC have typically shown exceptionally low inversion channel mobilities (μ_{inv}~0.1-25 cm^2/Vs). Such low mobilities were attributed to the presence of a high density of acceptor like interface states (D_{it}) present very close to the band edges of 4H-SiC (E_g=3.2eV). In more recent studies[1], it has been shown that a nitric oxide (NO) post oxidation anneal (POA) can reduce the D_{it} at the conduction band edge by an order of magnitude (from D_{it}~$10^{13}cm^{-2}eV^{-1}$ to D_{it}~$10^{12}cm^{-2}eV^{-1}$) with a corresponding improvement in mobility. Reports by other groups[2] have indicated improved inversion layer mobilities on MOSFETs built on (11-20) oriented substrates using wet oxidation only, without any NO POA. In this paper, we report the first interface state density measurements on MOS capacitors fabricated by dry oxidation, with NO POA on the (11-20) crystal face of n-4H-SiC and compare to the conventional (0001) Si terminated face. The study of the oxide/(11-20) interface is relevant not only to device fabrication on (11-20) substrates but also for the development of (0001) UMOSFETs; where the gate is "U" shaped and the inversion channel may lie along a (11-20) crystal face. Our results show that interface densities on the (0001) and (11-20) are similar before and after the NO passivation, in the $10^{13}/cm^2eV^{-1}$ range near the conduction band. The NO POA results in a significant reduction of(D_{it}) near the conduction band edge for the (11-20) face; the reduction being similar in extent to that observed for the (0001) face. Close to conduction band, the density of defect traps decreased from ~$10^{13}/cm^2eV^{-1}$ to ~$10^{12}/cm^2eV^{-1}$ via the NO POA. The similarity of passivation behavior between these two faces suggests that the physical nature of defects is similar for the dry-oxide/(0001) and the dry-oxide/(11-20) interfaces. In addition, we have observed and quantified the nitrogen incorporation at or near the interface resulting from the NO POA, using Medium Energy Ion Scattering (MEIS). The ability to quantify the interfacial nitrogen content and correlate with the reduction of (D_{it}) suggests a cluster model for the nature of the interface traps. [1]G. Y. Chung et. al., Appl. Surf. Sc. 184(2001) 399. [2]H. Yano et.al., Jn. Appl. Phys. 78(2001) 374.

4:10 PM Student

BB8, The Influence of Processing Steps on Reverse-Bias Characteristics of 4H-SiC Schottky Barrier Diodes: *Kelly A. Neely*[1]; [1]Sandia National Laboratory, Advd. & Exploratory Sys. (2131), PO Box 5800, MS0482, Albuquerque, NM 87185-0482 USA

Silicon carbide (SiC) Schottky barrier diodes have been commercially available for about two years. Even though Schottky diodes are available, these devices are limited to currents of a few amperes. Since device size must increase if diodes are to handle larger currents, the reason for the limitation on current is the decreasing diode yield as diameter increases. Our observations and experiments have identified two causes reponsible for decreasing diode yield as diode dimensions are scaled up: (i) poor performance related to non-optimized processing conditions and, (ii) morphological defects on 4H-SiC epilayers. This presentation is primarily concerned with processing-induced device performance. Specially, the purpose of this study is to investigate how processing variations affect the current-voltage characteristics of 4H-SiC Schottky diodes. Schottky diodes used in this study were fabricated on epi-wafers consisting of a 10?Ým-thick, n-type epilayer with an approximate doping of 5x1015 cm-3. Boron implantation and subsequent annealing were used to terminate the diodes. Nickel Schottky and backside ohmic contacts were applied to complete device fabrication. Diode diameters ranged from 140 to 440 ?Ým. Processing variations considered in this presentation are (1) the effect of a blanket reactive-ion-etch (RIE), (2) the effect of a passivation oxidation, (3) variations in post-implant anneal temperature, and (4) variations in the depth of the boron implanted edge termination. The reverse bias leakage current was found to decrease by three orders of magnitude at 1000 V reverse bias when a blanket RIE was applied to the epilayer surface. Conversely, the growth of a passivation oxide following the post-implant annealing led to catastrophic results with all devices breaking down well below 1000 V. Variation in the post-implant anneal temperature from 1050°C to 1450°C showed only a slight effect on the reverse bias characteristics of the Schottky diodes. A reverse-bias current density of approximately 10-3 A/cm2 was observed at 1000 V for all annealing temperatures. Variations in reverse characteristics with diode size are observed within this study. Best device results were seen to vary little with diameter, but the data scatter increased markedly with diameter. Explanations based on surface defect distributions for all device results discussed are presented.

4:30 PM

BB9, 16.8 mΩcm², 600 V, Normally-Off Planar Power ACCUFET in 4H-SiC: *Saichirou Kaneko*[1]; Masakatsu Hoshi[1]; Satoshi Tanimoto[1]; Tetsuya Hayashi[1]; Hideaki Tanaka[1]; [1]Nissan Motor Company, Ltd., Elect. & Info. Tech. Rsch. Lab., 1 Natsushima-cho, Yokosuka-shi, Kanagawa 237-8523 Japan

Specific on-resistance of 4H-SiC power MOSFETs fabricated to date has been quite high due to low channel mobilities. Adopting an accumulation channel is one conceivable way of increasing the channel mobility. However, several planar SiC power MOSFETs incorporating the accumulation channel (ACCUFET) were normally-on devices in previous studies.[1,2] In this work, we experimentally demonstrated a low on-resistance planar power 4H-SiC ACCUFET possessing a normally-off characteristic. The device exhibited a specific on-resistance of 16.8 mΩcm^2 with a blocking voltage of 600 V. This on-resistance is the lowest reported to date for normally-off planar power MOSFETs in 4H-SiC. The device was fabricated on a 10-µm thick n-type epilayer (Nd - Na = 1.0E16 cm^{-3}) grown on a 4H-SiC n$^+$-type substrate. Source regions were formed by phosphorous implantation. P-wells were made by aluminum implantation at 800°C, with dose/energy of 5.0E13 cm^{-2}/360 keV. Nitrogen ions were also implanted at 800°C into the channel region to form the accumulation channel. The implanted dose was 7.4E12 cm^{-2}, and the thickness of the accumulation channel was 0.2 µm. All the implants were activated at 1600°C. The gate oxide was formed by growing a 20-nm-thick thermal SiO_2 at 1100°C in dry O_2, followed by deposition of a non-doped silicate glass (NSG) to obtain a better MOS interface.[3] The gate oxide was then annealed and the thickness finally became 55 nm. Polysilicon was deposited and doped as the gate electrode. The ohmic contacts for the source and p-well contacts were formed with Ni. A 2-µm aluminum layer was patterned as the final metal layer. This device has a channel length of 2 µm and a p-well spacing of 3 µm for a cell pitch of 17 µm. The active area is 0.00171 cm^2 (423 µm times 404 µm). The device is normally off, showing a threshold voltage of 2.0 V. As for BVdss, the device was capable of blocking 600 V. The specific on-resistance of the device was determined to be 16.8 mΩcm^2 at a gate voltage of 23 V (oxide field of 4.2 MV/cm). The peak channel mobility was 151 cm^2/Vs, which was measured on a lateral simple ACCUFET in the implanted p-wells. The low on-resistance value of 16.8 mΩcm^2 was attributed to this high channel mobility obtained from the normally-off ACCUFET. [1]A. Agarwal, et al., Proceedings of 2001 ISPSD, pp. 183-186, (2001). [2]F. Nallet, et al., Proceedings of 2002 ISPSD, pp. 209-212, (2002). [3]S. Kaneko, et al., Mater. Sci. Forum, 389-393, pp. 1073-1076, (2002).

4:50 PM BB10, Late News

Session CC: Nitrides: Substrates and Properties

Friday AM Room: Ballroom Center
June 27, 2003 Location: Olpin Union Building

Session Chairs: Joan Redwing, Pennsylvania State University, University Park, PA 16802-5006 USA; Thomas Myers, West Virginia University, Morgantown, WV 26506 USA

8:20 AM

CC1, HVPE-GaN Thick Films for Quasi-Substrate Applications: Strain Distribution and Wafer Bending: *T. Paskova*[1]; E. Valcheva[1]; V. Darakchieva[1]; P. P. Paskov[1]; I. G. Ivanov[1]; B. Monemar[1]; T. Bötcher[2]; D. Hommel[2]; [1]Linköping University, Dept. of Physics & Measurement Tech., Linköping S-581 83 Sweden; [2]University of Bremen, Inst. of Solid State Physics, Bremen D-28334 Germany

A high quality thick HVPE-GaN layer may be used either as a template, residing on the widely used sapphire substrate, or as a free-standing quasi-substrate for consequently grown device structures. The GaN community has recently paid a significant attention on the second application of the HVPE technique hoping to overcome the biggest problem in the GaN technology, namely the lack of a native substrate. The HVPE together with laser lift-off technique used for substrate delamination have been demonstrated to enable large area good quality free-standing GaN films. However, a critical remaining question is the structural and optical quality of the films after the laser lift-off. In this work we present our current understanding of the key growth-related properties of thick HVPE-GaN films relevant for the quasi-substrate application, as well as the substrate delamination-induced changes in the properties. For this study, we prepared free-standing HVPE-GaN films with different thicknesses. The HVPE-GaN films were initially grown either directly on sapphire or using undoped MOCVD-GaN templates. These thick crack-free GaN films were separated from the sapphire substrates by a lift-off process utilizing the third harmonic of Q-switched YAG:Nd laser. A variety of characterization techniques was employed to study in a comparative way the physical properties of as-grown GaN thick films and the same films after the substrate separation. Precise investigation of both faces of the free-standing films was performed. The spatial uniformity of the strain distribution was also studied by PL mapping over 2" wafers. We find a significant difference in the bending of the as-grown and free-standing films. This is strongly related to the thicknesses of the films and sapphire substrates, as well as to the conditions of the lift-off process. A comparison between the distributions of defects and strain present in the GaN free-standing films before and after the delamination process is made. The results are critically analyzed aiming to reveal a relation between the strain distributions and the wafer bending and to attribute the observed peculiarities either to the growth or to the laser lift-off process. The possibilities for optimizations of the processes to further improve the uniformity of the film characteristics and to reduce the bending of the free-standing HVPE-GaN films will be discussed.

8:40 AM

CC2, Strain Reduction for Crack-Free Growth of AlGaN on Porous GaN: *Qhalid Fareed*[1]; M. Asif Khan[1]; Vinod Adivarahan[1]; R. Molnar[2]; [1]University of South Carolina, Dept. of Electl. Engrg., 301 S. Main St., Columbia, SC 29208 USA; [2]Massachusetts Institute of Technology Lincoln Labs, Lexington, MA 02173 USA

The AlxGa1-xN material system with its wideband gap tunability from about 3.4 to 6.2 eV is ideally suited for the development of deep ultraviolet (UV) optoelectronic devices. One of the key requirements for such devices is high quality (low defects) thick AlxGa1-xN layers with high Al-mole fractions (x>0.3). Such AlGaN layers over sapphire, SiC or GaN substrates are under compressive or tensile strain and crack when the critical thickness dc (typically 1 ìm for AlGaN with x > 0.2) is exceeded. We will report on an innovative approach to grow high-Al AlGaN layers over GaN with thickness values well in excess of dc. Our approach centers on making the GaN layer porous prior to the deposition of the AlGaN overlayer. Subsequently thick (d >dc) AlGaN layers are deposited on the porous GaN film (PO-GaN) by metalorganic chemical vapor deposition (MOCVD). In our experiments we created extremely deep pores (t >30 µm) in HVPE GaN films, with thickness in excess of 50µm over (0001) sapphire substrates. Ultraviolet radiation-enhanced chemical etching using an HF:H2O2 solution was used for the pore creation process. We optimized AlGaN growth conditions in order to enhance lateral growth and achieve the formation of air-bridges between the PO-GaN and AlGaN layers. Due to the porous nature of the underlying GaN, the strain in the AlGaN layer is significantly reduced making it possible to grow crack-free, thick (close to 3 ìm) Al0.18Ga0.82N epitaxial layers (well over the normal critical thickness limit). X-ray diffraction studies indicate that compressive strain in PO-GaN template is caused by the strain sharing between PO-GaN and AlGaN layers. Room temperature photoluminescence study of the layers shows that the band-to-band emission is approximately 2 times stronger than in AlGaN grown on H-GaN and almost 50 times stronger than in AlGaN layers deposited on the conventional MOCVD GaN. The obtained results demonstrate that growth of AlGaN on PO-GaN is very promising for UV emitter applications. In this paper we will present detailed results of growth and characterization using X-ray, PL, AFM and TEM. In addition the use of these porous grown templates for multiple quantum light-emitting diodes will also be discussed.

9:00 AM Student

CC3, Asymmetric Strain in III-N Resulting from the Substrate with Direction-Dependent Thermal Expansion Coefficients: *Sa Huang*[1]; Sangbeom Kang[1]; William Alan Doolittle[1]; April S. Brown[2]; [1]Georgia Institute of Technology, Sch. of Electl. & Compu. Engrg., Microelect. Rsch. Ctr., 791 Atlantic Dr., Atlanta, GA 30332 USA; [2]Duke University, Electl. & Compu. Engrg., 128 Hudson Hall, Durham, NC 27706 USA

LiGaO2 (LGO) is a useful substrate for GaN because of a smaller lattice mismatch than other substrate materials. However, LGO possesses a lattice match that is asymmetric within the growth plane. GaN thin films on LiGaO2 (LGO) were grown over a thickness range of 50 Å to 1µm. X-ray diffraction was employed to measure the lattice constants of the films. It was found that there is asymmetric stress in GaN along the a and

b axis of LGO. Along the a axis of LGO, the lattice constant relaxes as the film thickness increases, while along the b axis and c axis, lattice constants are compressed. This could be explained that when the film is strained, the lattices along the b axis are elonged, and the ones along the a axis are compressed because of the structure of LGO. Thus, when relaxed, the two lattice constants of GaN projected onto the LGO a and b lattice vectors, show compression and tension respectively. Upon cooling after growth, the difference in the coefficients of thermal expansion (CTE) results in added compressive strain along both the a- and b-axis of LGO. Considering thermal stress, along the a-axis, the strain caused by lattice mismatch in the thinnest film is dominant. As the film thickness increases, the lattice-mismatch stress decreases and finally, it is almost compensated with the thermally induced strain. Along the b-axis, the thermal strain is dominant for the thinnest film. For the relaxed film, the thermal strain is less than lattice-mismatch stress, and the whole strain is tensile. The strain along the c axis is compressive and increased with thickness increasing. The critical thickness is also determined experimentally to be 40Å.

9:20 AM Student

CC4, III-Nitride Growth on Lithium Niobate: Polarity Control by Electrostatic Boundary Condition: *Gon Namkoong*[1]; W. Alan Doolittle[1]; Alexander Carver[1]; Walter Henderson[1]; Dieter Jundt[2]; April S. Brown[3]; [1]Georgia Institute of Technology, Sch. of Electl. & Compu. Engrg., MIRC, 791 Atlantic Dr. N.W., Atlanta, GA 30341 USA; [2]Crystal Technology, Inc, Palo Alto, CA 94303 USA; [3]Duke University, Durham, NC 27708 USA

We discuss the use of a novel substrate for III-Nitride epitaxy, Lithium Niobate. It is shown that Lithium Niobate (LN) has a smaller lattice mismatch (6.8%) to GaN than sapphire and can be used to control the polarity of III-Nitride films grown by plasma assisted molecular beam epitaxy, enabling polarization engineered structure. Results from initial growth studies are reported including using various nitridation/buffer conditions along with structural and optical characterization. GaN has been successfully grown on (0001) oriented lithium niobate using a plasma assisted molecular beam epitaxy system. Structural crystal quality has been evaluated by reflection high energy electron diffraction (RHEED), reciprocal space mapping and omega-two theta X-ray diffraction using a Philips MRD system while optical quality was investigated by photoluminescence. The polarity of the films was investigated using a phosphoric acid based solution Polarity of GaN epitaxial layers can be controlled by choice of orientation of lithium niobate: Ga-polarity on (0001) and N-polarity on (000-1) lithium niobate. Moreover, the patterned, polarized substrates, such as periodic poled lithium niobate provides the lateral control of the polarity of subsequent GaN epitaxial layers. Hot phosphoric acid etching of such a film resulted in etching modulated by the period of the periodically poled lithium niobate domains. Laterally engineered polarity heterojunction structures can be used for dramatic luminescence enhancement due to the recombination of hole-electron at the boundary observed by Stutzmann et al.[1] [1]M. Stutzmann, O. Ambacher, M. Eickhoff, U. Karrier, A. Lima Pimenta, R. Neuberger, J. Schalwig, R. Dimitrov, P. J. Schuck, and R. D. Grober, Phys. stat. sol. (b), 228, No 2, p. 505-512, (2001).

9:40 AM

CC5, Homoepitaxy of Nitride Films on Bulk Nitride Substrates and Sapphire-Based Templates by MOCVD: *Dae-Woo Kim*[1]; Seungjong Lee[1]; A. Pechnikov[2]; L. Shapovalova[2]; V. Soukhoveev[2]; Alexander S. Usikov[2]; Vladimir A. Dmitriev[2]; Subhash Mahajan[1]; [1]Arizona State University, Chem. & Matls. Engrg., Tempe, AZ 85287-6006 USA; [2]TDI, 12214 Plum Orchard Dr., Silver Spring, MD 20904 USA

The group III nitrides are promising materials for the fabrication of efficient blue light-emitting diodes, laser diodes, and high-temperature/high-power electronic devices because they have a direct wide band gap and a high saturation electronic velocity. A lot of progress has been achieved in the development of GaN-based devices over the last decade. In the absence of a suitable substrate, the nitride materials are routinely grown on sapphire and SiC substrates, which present a large lattice mismatch to GaN. However, the mismatch in lattice constants and thermal expansion coefficients between the group III nitrides and the available substrates induce a high density of dislocations and strain which limit the efficiency and life time of devices. Using homoepitaxy technique, two-dimensional step-flow growth of GaN can be achieved without the additional deposition steps such as surface nitridation, thin low-temperature nucleation films, or thick buffer layers and also GaN device structure can be grown directly on GaN substrate. For laser diode, laser cavities can be fabricated with cleavage facets instead by time-consuming reactive ion etching process, which also induce the defect states on the surface of epitaxial layer. In addition, the GaN substrate can be doped n or p-type, providing significant simplification in device fabrication processing and circuit integration. In this study, homoepitaxial growth of GaN and AlN on respective templates and bulk wafers has been investigated. Nitride templates and bulk wafers were provided by TDI (Technologies and Devices International). GaN and AlN homoepitaxial layers were grown in Aixtron horizontal-type MOCVD (Metal Organic Chemical Vapor Deposition) system. Ammonia (NH3) and trimethylgallium (TMGa) were the component precursors for GaN growth. Ammonia (NH3) and trimethylaluminum (TMAl) were the component precursors for AlN growth. Purified hydrogen was used as a carrier gas. It was found that an optimum pretreatment of the substrate surface prior to growth is extremely important for high quality of homoepitaxial layer. Layers grown without the pretreatment cracked and delaminated from the templates. Also, an improper pretreatment induced a lot of pits on the substrate surface and caused very rough surface of epitaxial layer. The cross-sectional TEM results revealed that the dislocation density of GaN-template/sapphire interface was $6X10^{10}cm^{-2}$ and it decreased with layer thickness. GaN homoepitaixal layer has a dislocation density of $4X10^{8}cm^{-2}$. The detailed experimental procedure and results of homoepitaxy on bulk substrates and sapphire-based templates will be presented and also the reduction mechanism of dislocation density will be discussed.

10:00 AM Break

10:20 AM Student

CC6, Growth of High-Quality AlN Single Crystals by Sublimation: *Rafael Dalmau*[1]; Raoul Schlesser[1]; Zlatko Sitar[1]; [1]North Carolina State University, Dept. of Matls. Sci. & Engrg., 1001 Capability Dr., RB 1, Campus Box 7919, Raleigh, NC 27695-7919 USA

AlN crystals were grown in a dedicated, resistively heated reactor at temperatures up to 2300°C and in nitrogen atmosphere (400 to 600 Torr) under quasi-stagnant conditions (100 sccm) using an AlN powder source. The morphology of crystals grown by spontaneous nucleation was found to strongly depend on growth temperature and contamination in the reactor. The choice of reaction crucibles was found to crucially influence contamination levels in the growth environment and all aspects of crystal growth, including nucleation, coalescence, and resulting crystal morphology. Spontaneously grown AlN single crystals up to 5 mm in size were extensively characterized. X-ray diffraction (XRD), transmission electron microscopy (TEM), as well as X-ray topography studies evidenced that these crystals were of excellent quality, featuring average dislocation densities on the order of 1000 per square centimeter, with extended areas virtually dislocation-free. High-resolution X-ray diffraction showed rocking curves as narrow as 7 arcsec. Seeded growth on similar spontaneously nucleated crystals yielded up to centimeter-size single crystals without a noticeable degradation of crystal quality. Depending on the choice of crucible materials, crystals were optically clear or tinted orange. Orange coloration was observed when crystals were grown in refractory metal crucibles. In an effort to evaluate and optimize the growth process on larger area seeds, growth of thick, single crystalline AlN was conducted on 6H-SiC seeds. SiC wafers were initially coated with a 300 nm AlN epilayer grown by metal-organic chemical vapor deposition (MOCVD). This layer was intended to protect the SiC surface from premature decomposition in the high temperature, Al-containing growth environment, and to promote two-dimensional growth of AlN. Sublimation experiments were conducted at relatively moderate temperatures (typically 1850°C seed temperature) in an effort to preserve the integrity of the SiC seeds during the initial growth stage. Subsequently, the AlN growth rate was gradually increased by increasing the seed temperature to 2000°C. Millimeter-thick AlN crystals free of cracks were prepared on inch-sized SiC seeds. XRD characterization evidenced that the AlN grew in the direction of the SiC seed. The knowledge gained from these large-area growth results will ultimately be beneficial to the further development of larger-size and higher-quality AlN single crystals grown from AlN seeds. Details on the optimization of this process, as well as characterization data will be presented.

10:40 AM

CC7, Near-Band-Edge Photoluminescence Dynamics in AlN Epilayers Grown on A-Plane Single Crystal Bulk AlN: *Edmundas Kuokstis*[1]; Jinwei Yang[1]; Asif M. Khan[1]; Qhalid R.S. Fareed[2]; Remis Gaska[2]; Michael S. Shur[2]; [1]University of South Carolina, Dept. of Electl. Engrg., 301 Main St., Columbia, SC 29208 USA; [2]Sensor Electronic Technology, Inc., 1195 Atlas Rd., Columbia, SC 29209 USA

We studied near-band-edge (NBE) photoluminescence (PL) dynamics of high quality homoepitaxial AlN layers grown on A-plane single crystal bulk AlN substrates. The epilayers were deposited using low-temperature metalorganic chemical vapor deposition technique. The bulk AlN substrates were grown using a physical vapor transport technique by Crystal IS, Inc. Trimethyl aluminum, trimethyl gallium, triethyl gallium and ammonia were used as precursors. The calculated growth rate was approximately 0.1 mm/hour and the thickness of the epitaxial layers was close to 0.7 mm. X-ray rocking curve along (1120) and (0002) planes were measured using high resolution X-ray diffractometer. The full width at half maximum (FWHM) along (1120) and (0002) planes are 54 arc sec and 195 arc sec, respectively, pointing to a high quality of the epitaxial layers. We have used excimer laser pulses (λ = 193 nm, τ = 8 ns, f = 10-100 Hz) as an excitation source. PL experiments were carried out in a wide range of temperatures from 8 to 300 K and excitation power densities from 0.0008 to 1.0 MW/cm^2. We observed clear difference between NBE dynamics at low (< 100 kW/cm^2) and high (> 100 kW/cm^2) excitation powers in the entire temperature range. At low excitation and low temperatures (< 200 K) the NBE PL spectra consist of the line caused by radiative recombination of free excitons and a few (up to 3 at 8 K) equidistant lines separated by ~100 meV which is close to LO phonon energy in AlN indicating participation of those phonons in the recombination process. At higher temperatures (> 200 K) a fine structure of the PL spectrum is washed out presumably by competing band-to-band recombination and, therefore, PL spectrum consists of just one broad emission band. A similar transition from exciton emission to electron-hole plasma radiative recombination was also observed at high excitation. We attribute this behavior of NBE emission spectra to Mott-transition in exciton system. The extracted value of nonequilibrium carrier concentration for Mott-transition in AlN was close to ~10^{19} cm^{-3}. NBE PL spectra dominated by electron-hole plasma recombination broadens and shifts to longer wavelengths with increase in the optical excitation. The FWHM of the PL spectra at 8K increased from 40 meV at low excitation to 180 meV at 1 MW/cm^2. The respective FWHM values at 300K were 140 meV and 280 meV. The change of emission mechanisms was also confirmed by integrated PL intensity dependence on the excitation. We explain the observed NBE dynamics at high excitation by many-body effects in high-density nonequilibrium carrier system. We will present a detail discussion of these mechanisms and their role in deep ultraviolet optoelectronics applications.

11:00 AM

CC8, Effect of Growth Condition on Structural Properties of AlN Epitaxial Layer: *David W. Weyburne*[1]; *Qing S. Paduano*[1]; Janusz Kozlowski[2]; J. Serafinczuk[2]; Zuzanna Liliental-Weber[3]; [1]Air Force Research Laboratory, SNHC, 80 Scott Dr., Hanscom AFB, MA 01371 USA; [2]Wroclaw University of Technology, Janiszewskiego 11/17, 50-372, Wroclaw Poland; [3]Lawrence Berkeley National Laboratory, One Cyclotron Rd., Berkeley, CA 94720 USA

A two-step pressure process was recently developed to deposit high quality AlN layers by MOCVD. The best AlN layers had FWHM value of ~340 sec and ~650 sec for (0002) and (10-12) rocking curves respectively. These FWHM values are approaching those of good quality GaN. Layers with thicknesses ranging from 0.3µm to 4µm deposited directly on c-plane sapphire showed no cracks on the surface of the films. A detailed X-ray diffraction study was undertaken to study the effect of growth condition on the layer structural properties such as tilt and twist mosaicity. The characterization methods used in this study include reciprocal space mapping, rocking curves (ω-scan), triple-axis scans (2ϑ-ω) and azimuth angle scans (ϕ-scan), using symmetric, quasi-symmetric configurations. The twist mosaicity has been shown to correlate well with the edge-type threading dislocation density for GaN. It was found that low twist often indicates low edge dislocation density, and in turn higher electron mobility. However, the methods reported in the literature to characterize twist vary from group to group. While some measured FWHM values on the (10-12) or the (11-20) rocking curve with quasi-symmetric or symmetric geometry, others used asymmetric (11-24) or (10-15) diffraction. We believe the evaluation of twist is meaningful only if the variation of the FWHM of these rocking curves as a function of the inclination angle of the lattice plane is taken into account. For the present study, we measured ω-scans and ϕ-scans using quasi-symmetrical geometry on a family of lattice planes (10-1l) with l = 1,2...5, and (20-21) plane with inclination angle close to 75°. The FWHM values from both ω-scans and ϕ-scans were plotted as functions of inclination angle with respect to surface normal. By extrapolating the angular distribution of FWHM to 90° inclination angle, where FWHM is converging for both the ω-scans and ϕ-scans, the twist angle can be estimated. The twist mosaicity was found to be sensitive to the substrate nitridation condition. With optimized nitridation, the best AlN layer obtained has a twist angle about 0.2°. The corresponding edge-type threading dislocation density was estimated to be 1.2x10^9/cm^2. For comparison, the threading dislocation density was measured by cross-section TEM. To evaluate tilt angle, we measured (0002) reciprocal space maps, ω-scans and 2ϑ-ω-scans as well as (11-24) and (10-15) under asymmetric geometry. From the 2-D intensity map, the component of tilt and the component of lateral correlation length were estimated. Corresponding (11-24) and (10-15) rocking curves showed very narrow peak of FWHM about 200-250 sec. The tilt angle was found to be sensitive to the deposition pressure. By reducing growth pressure to 40 torr, we obtained layers with tilt angle less than 0.05°.

11:20 AM

CC9, Growth Mode Control of GaN by Si using Si-Irradiation Technique in rf-MBE: *Xu Qiang Shen*[1]; Toshihide Ide[1]; Mitsuaki Shimizu[1]; Hajime Okumura[1]; [1]National Institute of Advanced Industrial Science and Technology, Power Elect. Rsch. Ctr., Central 2, 1-1-1, Umezono, Tsukuba, Ibaraki 305-8568 Japan

III-nitride materials have been extensively studied due to their potential applications in optical and electronic devices. In order to obtain high-quality GaN-based heterostructures for device applications, a flat surface and low-density dislocation are two key factors. In the case of MBE, rough surface morphology and high dislocation density are still the main problems. Recently, Si-irradiation technique has been proposed to realize a stepped surface morphology of GaN and to reduce the dislocation density in the film.[1] However, the role of Si is not well-understood at present. In this paper, we report the results of Si effect in Si-irradiation technique during the rf-MBE GaN growth. In situ RHEED, SIMS, AFM, HRXRD and cross-sectional TEM characterizations are carried out to study the Si roles. The growth of GaN films was carried out by rf-MBE. Details of Si-irradiation technique have been reported elsewhere.[1] In order to study Si roles, we changed the Si amount during the Si-irradiation process and compared the growth behaviors of GaN with respect to the different irradiated-Si amounts. The Si amount was changed from 4.0x1013 to 1.5x1015 atoms/cm2 using the effusion cell of Si with different flux intensities. It was observed by In situ RHEED that Si controls the growth mode of GaN. When the irradiated Si amount was low (less than 3.0x1014 atoms/cm2), the RHEED of the re-grown GaN kept the streaky pattern, indicating that the 2-dimensional growth of GaN was maintained. However, when the irradiated Si amount exceeded the above value, the RHEED of re-grown GaN firstly changed from a streaky pattern to a spotty one within a few seconds, then the pattern came back to a streaky one again. The above results indicate that Si can modify the growth mode of the re-grown GaN by controlling the irradiated-Si amount. AFM results showed that irradiated-Si amount influenced GaN surface morphologies. When the irradiated-Si amount is small, straight steps without spiral features on the surface could be observed. However, many spiral steps existed on the GaN surface when the irradiated-Si amount is large. The spiral growth feature is resulted from the initial growth mode change of the re-grown GaN as described above. HRXRD results showed that the film-quality of GaN becomes poor with more Si amount. HRTEM observations illustrated that irradiated-Si preferred to form Si-related clusters in the irradiated interface, which can modify the growth mode and stop the propagation of threading dislocations in the GaN film. Details will be discussed. [1]X.Q. Shen et al. Jpn. J. Appl. Phys. 41 (2002) L1428.

11:40 AM CC10, Late News

Session DD: Epitaxy III: Devices

Friday AM Room: Ballroom East
June 27, 2003 Location: Olpin Union Building

Session Chairs: Archie Holmes, University of Texas, Austin, TX 78758-4445 USA; Abbas Torabi, Raytheon RFC, Andover, MA 01810 USA

8:20 AM Student

DD1, Monolithic Integration of AlGaInP Light Emitting Diodes on Si Substrates: *O. Kwon*[1]; J. J. Boeckl[1]; M. L. Lee[2]; A. Pitera[2]; E. A. Fitzgerald[2]; S. A. Ringel[1]; [1]The Ohio State University, Dept. of Electl. Engrg., 2015 Neil Ave., Columbus, OH 43210 USA; [2]Massachusetts Institute of Technology, Dept. of Matls. Sci. & Engrg., 77 Massachusetts Ave., Cambridge, MA 02139 USA

III-V optoelectronic integration on silicon-based integrated circuits has been challenged for decades by fundamental mismatches in lattice constant, thermal expansion coefficient and crystal structure. Recent work on graded SiGe, relaxed buffers has opened a new window of opportunity for success, however, with the demonstration of low threading dislocation densities over large wafer areas that recently led to the demonstration of device-quality GaAs grown on SiGe/Si substrates and efficient GaAs/Si solar cells. In this paper, the successful integration of AlGaInP based multi-quantum well light emitting diodes (MQW-LED) on SiGe/Si substrates, using solid source molecular beam epitaxy (SSMBE), is presented. Three identical MQW-LEDs have been grown on n type GaAs, Ge, and Ge/SiGe/Si substrates and processed for comparison purposes. In order to examine optimum growth conditions for the $Ga_{.51}In_{.49}P$ active layer, X-ray diffraction and photoluminescence (PL) have been performed on various samples grown under different group III / P flux ratios at a pre-optimized growth temperature, 490°C. Precise lattice match and composition were confirmed from X-ray analysis and the $Ga_{.51}In_{.49}P$ sample grown at 1/6 flux ratio generates the highest excitonic luminescence from 19K low temperature PL. In order to maximize light extraction from LED, resonant cavity structures have been introduced. A one-• thick AlGaInP optical cavity consisted of four 80Å thick $Ga_{.51}In_{.49}P$ quantum well active regions surrounded by $Al_{.5}Ga_{.5})_{.51}In_{.49}P$ as both 60Å thick barrier and 780Å thick spacer layers that were doped with Si at the n-side and Be at the p-side. The cavity was sandwiched between an n-type bottom Distributed Bragg Reflector (DBR) of 18 periods (~97% reflectivity) and a p-type top DBR of 5 periods (~74% reflectivity), where DBR was made of a combination of AlAs and $Al_{.5}Ga_{.5}As$ with a quarter • thickness. Both n and p DBRs were doped in the range of $2x10^{18}$ cm^{-3}, respectively. A room temperature emission wavelength of 655nm was obtained from fully processed devices for each of the substrates by electroluminescence (EL). Maximum optical powers measured on top of 300 μm × 300 μm surface emitting MQW-LEDs were 7.33 μW from the LED on Si, 7.22 μW from the LED on Ge, and 4.55 μW from the LED on GaAs substrates under 50mA injection current, respectively. Detailed comparison of material and device characteristics on the various substrates will be presented, including PL and EL spectra, TEM images, EL images of operating devices, light vs. current and current vs. voltage results.

8:40 AM Student

DD2, Planarized Regrowth Technology for Vertically Stacked Waveguides using Metalorganic Chemical Vapor Deposition: *Seung-June Choi*[1]; Wilson Lin[2]; Sang Jun Choi[1]; P. Daniel Dapkus[1]; Giora Griffel[2]; Ray Menna[2]; John Connolly[2]; [1]University of Southern California, EE-Electrophysics, 3651 USC Watt Way, VHE 302, Los Angeles, CA 90089 USA; [2]Princeton Lightwave, Inc., 2601 Rte. 130 S., Cranbury, NJ 08512 USA

At present, a variety of MOCVD growth techniques, including selective area growth (SAG) and regrowth, are in use to meet the sophisticated demands for photonic integrated circuitry. One of the most challenging tasks is to realize planar vertically stacked layers built on buried heterostructure (BH) mesas to enable 3-dimensional construction of multiple semiconductor waveguides in photonic integrated circuits. It is very difficult to planarize layers regrown on mesas or rib-type waveguides using conventional MOCVD, since the non-planarity of the initial surface is usually transferred through the layers in the regrowth process. In this paper, we demonstrate a planarized regrowth technology achieved by a two-step regrowth process using LP-MOCVD. To initiate the process, a 400 nm thick InGaAsP layer was grown on an (001) oriented InP substrate, followed by a SiN layer deposited as a masking layer. Stripe waveguide patterns were defined along the [110] direction by photolithography and methane-based RIE. The resultant mesas were 1 micron wide and 400 nm high, having vertical sidewalls as steep as 87°. The closest separation between the neighboring mesas was 8 microns. Once the waveguides to be buried were formed, the polymers formed on the sidewalls during the etching were cleaned by an oxygen plasma treatment. The SiN mask was left on the mesa for the first regrowth step. The first regrowth is to fill the empty regions between the mesas with InP. The V/III ratio was varied from 340 to 240 to see the effect of the PH3 partial pressure on the growth behavior while the growth temperature was maintained at 690¢ªC. Low V/III ratio is preferable to avoid a sloped overgrowth along the dry-etched mesas, since it enhances the surface migration of the group-III species. However, voids appeared along the mesa sidewalls when the V/III ratio was lower than 280. The SiN layer was removed after the first regrowth step. The second regrowth is to build vertically stacked layers on the buried mesas. In this study, a set of InP/InGaAsP/InP layers was grown on the BH waveguides to produce waveguides used in vertically coupled microresonators. The best-planarized wafer was obtained from samples that were filled with InP at V/III = 291. The subsequent epitaxial structures are quite planar as witnessed by the successful fabrication of vertically coupled microresonators devices in which the buried waveguides are used as input and output busses and the regrown waveguide layers are used to fabricate the microresonator. Detailed characterization of the surface planarity and the effects of the V/III ratio will be presented. In conclusion, planar, vertically stacked waveguides are obtained on BH mesas by conducting a two-step regrowth process. This approach is also potentially important for any buried waveguide technology where subsequent surface planarity matters.

9:00 AM Student

DD3, Semiconductor Optical Amplifier and Electroabsorption Modulator Monolithically Integrated via Selective Area Growth: *Ryan A. Stevenson*[1]; Sang Jun Choi[1]; Kostadin Djordjev[1]; P. D. Dapkus[1]; [1]University of Southern California, Compound Semiconductor Lab., University Park, 3651 USC Watt Way, VHE 302a, Los Angeles, CA 90089-0243 USA

Selective area growth (SAG) by metal-organic chemical vapor deposition (MOCVD) has proven to be a key technology in the realization of photonic integrated circuits (PICs). With SAG, localized bandgap control across the surface of a wafer can be achieved in a straightforward manner. In this work we demonstrate the monolithic integration of a semiconductor optical amplifier (SOA) and an electroabsorption modulator (EAM) in the InP/InGaAsP system. This device is important in the realization of insertion-lossless modulators and mode-locked lasers. SAG involves depositing a dielectric mask pattern with a certain width and spacing between masks. Crystal growth does not occur on the dielectric, which results in growth rate enhancement and compositional changes, primarily on the group III sub-lattice, of the material grown in the separation region between masks. For a quantum well active region, this results in thicker wells with increased In content. The bandgap of the SAG regions, therefore, is red-shifted relative to the plain areas, and can be controlled by adjusting the width of the SiNx patterns. The mask design used here includes SiNx patterns that are ten and fifteen microns wide with a fifteen micron separation. The SOA section of the device is fabricated from selectively grown material, while the EAM section is formed from the plain-area region of the wafer. For the mask patterns mentioned above, we obtain SAG amplified spontaneous emission (ASE) peaks of 1550nm and 1565nm respectively when the plain-area photoluminescence (PL) is targeted at 1490nm. Thus the unbiased EAM active region is transparent to the SOA active region. The plain-area active region is grown to be a strain-compensated structure. Strain compensation is lost, however, in the SAG regions due to the increase in concentration of group III species. Thus all of the active region layers become more compressively strained as the SAG mask widths increase. Studies of threshold currents vs. SAG mask widths of broad-area lasers made from SAG material show no significant increase in threshold current for mask

widths up to 30 microns. This indicates that the increases in total strain in the SAG regions for the mask patterns used here do not have detrimental effects to device performance. Device performance was also characterized. The peak chip gain was measured at 20dB above transparency when biased to saturation. The absorption spectrum of the EAM was determined by measuring photo-generated current as a function of wavelength. The absorption peak was found to occur at 1495nm. In summary, an SOA and EAM have been monolithically integrated by utilizing the localized bandgap-engineering capabilities of selective area growth. SOA gain spectrums can be tailored to specific wavelengths and can be adjusted relative to the EAM spectrum by controlling the SAG mask dimensions.

9:20 AM Student

DD4, Long-Wavelength GaAsSb Quantum Well Heterostructures Laser Grown by Metalorganic Chemical Vapor Deposition: *Min-Soo Noh*[1]; Ying-Lan Chang[2]; Gabriel Walter[3]; Nick Holonyak[3]; Russell D. Dupuis[1]; [1]The University of Texas at Austin, Electl. Engrg., Microelect. Rsch. Ctr., 10100 Burnet Rd., Bldg. 160, Austin, TX 78758 USA; [2]Agilent Technologies Inc., Agilent Labs., 3500 Deer Creek Rd., Palo Alto, CA 94304 USA; [3]The University of Illinois at Urbana-Champaign, Ctr. for Compound Semiconductor Microelect., Urbana, IL 61801 USA

Semiconductor laser diode emitting at l~1.3µm is recognized as one of the most important optoelectronic devices because it has been used for high-bit-rate optical fiber communications. Recently, Vertical Cavity Surface Emitting Lasers (VCSELs) operating at the wavelength and grown on GaAs substrates have been attracting great interest for high-performance, low-cost communication system applications. For the purpose, GaAsSb as a QW active material has been studied intensively. Although there are several problems in growing GaAsSb on GaAs such as the wide range of miscibility gap (0.2<Sb<0.8) expected for typical growth conditions, the Type-II band alignment of the GaAsSb/GaAs heterojunction, and the large lattice mismatch (~2.7%) for $GaAsSb_{0.35}$/GaAs, the strain-controlled GaAsSb QW heterostructures with higher bandgap barrier materials grown on GaAs substrates can be good candidates. We have previous reported the effect of higher bandgap barrier materials such as GaAsP and InGaP. The photoluminescence (PL) intensities of the QW-SCH structures have improved a lot. It is attributed to the Type-I band alignment between GaAsSb QW and the barriers and strain-compensation effect in the active regions. Both effects are preferable to get a better electrical confinement in QW lasers. We have studied the material and optical quality of the DQW-SCH test structures by high-resolution XRD and room temperature PL. These samples have been fully grown by low pressure MOCVD. The growth temperature and growth rate for the active region are 580°C and 170Å/min. We have used various compositions of tensile strained 300Å thick $GaAs_{1-x}P_x$ as barrier material to optimize PL wavelength and intensity in our structure. We have improved the PL intensity with 20% P composition of GaAsP. Based on the optimized active condition, we have grown GaAsSb double-quantum-well graded-index-separate-confinement heterostructure (DQW-GRINSCH) laser. As n-type and p-type dopants, Si_2H_6 and CBr_4 have been employed. The broad-area (60µm-wide metal pattern) $GaAsSb_{0.3}/GaAsP_{0.2}$ DQW laser has lased at 300K with pulsed operation (0.4µs pulse width and 0.1% duty cycle). The lasing wavelength has been observed at 1.204µm. Threshold current density for 500µm cavity length and 60µm metal width laser was 982A/cm^2. And the threshold current density of 281A/cm^2 for the infinite cavity length was extrapolated from inverse cavity length vs. J_{th} plot. In summary, we have grown and characterized strain-compensated GaAsSb QWs using GaAsP as barrier material. We observed great improvement of PL intensity in these samples. For $GaAsSb_{0.30}$ DQW GRIN-SCH broad area laser with $GaAsP_{0.20}$ barrier grown by MOCVD at 580°C, we have achieved pulsed lasing at 1.204µm at 300K. Maximum output power reached up to 25mW. We will show more detail growth conditions as well as further laser results.

9:40 AM Student

DD5, Effects of Silicon Complexes on Tunnel Junctions for Vertical Epitaxial Integration: *Jizhi Zhang*[2]; Kei May Lau[1]; Neal Anderson[2]; [1]Hong Kong University of Science & Technology, EEE Dept., Clear Water Bay, Kowloon Hong Kong; [2]University of Massachusetts, Amherst, ECE Dept., Amherst, MA 01003 USA

Properties of tunnel (Esaki) junctions are important considerations in vertical epitaxial integration of multi-pn-junction devices such as tandem solar cells and multi-active-region lasers.[1] We reported the integration of a semiconductor cooler and a laser diode monolithically using a tunnel junction.[2] Preliminary calculations showed that the lowest zero-bias resistance of the junction, corresponding to carrier concentrations above 3 X 10^{19} cm^{-3} on both n and p sides, are needed for meaningful application of this device. In the fabrication of GaAs tunnel junctions, however, the electron concentration in the n-side can rarely reach 1 X 10^{19} cm^{-3} at normal growth temperatures (650°C) by MOCVD. The tunnel junctions were grown at 100 mbar by MOCVD in a horizontal reactor. They were formed by growing the n-type GaAs layer at 700°C on n-type substrates with input V/III ratio of 202, followed by a deposition of p-type GaAs at 550°C with input V/III ratio of 25. Under the same growth conditions, Hall electron concentration measured in single n-layers reached a maximal value of 8.76 X 10^{18} cm^{-3} with a silane/TMG mole ratio of 0.11. Further increase of silane resulted in a decreased concentration due to auto-compensation. With the CCl_4 flow rate fixed to give a hole concentration of 1.2 X 10^{20} cm^{-3}, tunnel junctions were grown with the silane flow rate for the n-GaAs changing from 0.11 to 1.92 silane/TMG mole ratio. The electron concentration decreased from 8.76 to 1.25 X 10^{18} cm^{-3} correspondingly, indicating the donor levels are deeply auto-compensated in these layers. The lowest value of zero-bias specific resistance, 9.59 X 10^{-5} ohm·cm^2 (to our knowledge the lowest reported for GaAs tunnel junctions grown at high temperature for stability) was obtained from a junction with an n-type layer having an electron concentration of 5.76 X 10^{18} cm^{-3}, which is in the middle of the data set. Tunneling current characteristics in the measured forward-biased I-V curves show marked current transitions from band-to-band tunnel current to the excess current regimes.[3] The voltages of the transitions can be related to a deep level around 350 meV below the conductance band edge caused by silicon complexes, thereby allowing carrier tunneling through these states. Combination and competition of these two currents resulted in an optimal silane flow rate for the lowest zero bias resistance of the junction. [1]WeiLing Guo, et al, Opt. Eng. 41, pp2391 2002. [2]Jizhi Zhang, et al, J. Electron. Mater. JEM30(7) 2001, EMC Program, p2. [3]S.M. Sze, Physics of Semiconductor Devices, Chapter 9, 1981.

10:00 AM Break

10:20 AM Student

DD6, InAs/GaP/InGaP High-Temperature Power Schottky Rectifier: *An Chen*[1]; Aristo Yulius[1]; Jerry M. Woodall[1]; [1]Yale University, Dept. of Electl. Engrg., PO Box 208284, New Haven, CT 06511 USA

We have fabricated a thermally stable Schottky power rectifier with high breakdown voltage using InAs/GaP/InGaP. Due to the metallurgical changes at the interface during heat treatment, thermal stability has been an important issue for the metal-semiconductor Schottky rectifiers for high-power, high-temperature applications. The InAs/GaP heterojunction has been shown to have near-ideal Schottky-barrier like diode characteristics. Recently, Jeon et al reported that InAs/GaP Schottky rectifiers are more stable than metal-GaP structures at high temperature. This is because the large lattice mismatch at the InAs/GaP junction will suppress the atomic inter-diffusion across the interface. For power devices, InGaP has better figure-of-merit than GaP. Therefore we have studied the InAs/InGaP junction. We have found that the direct growth of InAs on InGaP failed to be rectifying, probably due to the In-rich interface that occurs during MBE. To avoid this problem, we designed a structure with a thin GaP interface layer between the InGaP and the InAs. The samples were grown by MBE. A lightly doped InGaP layer (n=3E16) was grown on a GaAs substrate and was graded to GaP through a thin composition grading layer (20nm), followed by a 50nm InAs layer (n=1E20). A 5nm InAlAs cap layer was grown to prevent the decomposition of the InAs layer during heat treatment. The rectifying junction exists at the InAs/GaP interface. Au/Ti was the ohmic contact to the InAs layer. For comparison, Au/Ti was evaporated directly on the InGaP surface to make the metal-semiconductor rectifier. The forward I-V curve of the InAs/GaP/InGaP diode is linear on semi-logarithm scale over six orders of magnitudes. The ideality factor is 2.3. The barrier height of InAs/GaP/InGaP is 0.96eV, which is very close to the barrier height for InAs/GaP reported by Chen et al. The InAs/GaP/InGaP diode has higher breakdown voltage and lower leakage current at high reverse voltage region than the AuTi/InGaP diode. The maximum parallel plane electric field achieved is about 0.6MV/cm for the InAs/GaP/InGaP, compared to the 0.4MV/cm for the AuTi/InGaP. The high ideality factor (2.3) of the InAs/GaP/InGaP rectifier was suspected to be due to the defects in the grading layer between InGaP and GaP. To test this assumption, a Ni/GaP/InGaP diode was made by removing the InAs layer. It showed very similar character-

istics to the InAs/GaP/InGaP diode. Both the InAs/GaP/InGaP diode and the AuTi/InGaP diode were annealed under nitrogen ambient in a rapid thermal anneal at 300C for 1 minute, and then in a furnace anneal at 300C for 10 minutes. The InAs/GaP/InGaP diode showed no difference before and after the thermal anneal in both the forward and reverse I-V. In contrast, the AuTi/InGaP diode lost the diode characteristics after the furnace anneal. The results of the improved structures under investigation will be presented.

10:40 AM Student

DD7, Optimization of Metalorganic Chemical Vapor Deposition of AlGaN/GaN Heterostructures for High Electron Mobility Transistors: *Yugang Zhou*[1]; Chak-wah Tang[1]; Kei May Lau[1]; [1]Hong Kong University of Science and Technology, Photonics Tech. Ctr., Dept. of Electl. & Elect. Engrg., Clear Water Bay, Kowloon Hong Kong

Optimization of metalorganic chemical vapor deposition of AlGaN/GaN heterostructures for high electron-mobility transistors (HEMTs) was investigated using an Aixtron 2000HT system. The basic structure consists of an 2.5 μm undoped GaN buffer layer, an undoped-$Al_xGa_{1-x}N$ spacer layer varying from 3 to 8 nm, followed by an Si-doped-$Al_xGa_{1-x}N$ (n-AlGaN) layer, and an 2 nm undoped-$Al_xGa_{1-x}N$ cap. Strong correlation between the undoped GaN buffer and device performance was found. Initial growth conditions to optimize the GaN layer were adjusted using the in-situ monitoring of surface reflectivity vs. time. Room temperature Hall measurements were conducted after removal of the AlGaN layers. With the optimized growth conditions, a resistivity of 450 ohm-cm was achieved for the GaN layer. A full width at half maximum (FWHM) of 260 arcsec was found in the omega-scan of the GaN (0002) diffraction peak. For the samples with the highest resistivity, the minimum reflectance measured in the initial stage of the high temperature growth is a very good indicator of layer resistivity and therefore HEMT characteristics. The XRD results were not strongly correlated to the electrical properties. AFM results show that the surface morphology of the AlGaN/GaN heterostructures is mainly determined by the Al composition and V/III ratio, and does not affect the $n_s\mu$ of the 2DEG very much. With the standard structure and x = 0.32, the n-AlGaN doped at about $5x10^{18}$ cm^{-3}, n_s is about $2x10^{13}$ cm^{-2} with a corresponding mobility of around 850 cm^2/Vs. A slightly lower n_s ($1.5x10^{13}$ cm^{-3}) results in higher mobility (1070 cm^2/Vs), and the $n_s\mu$ keeps almost the same. Parallel conduction in the AlGaN layer was observed in the sample with an 8-nm-thick spacer, which is caused by the conduction band bending in the AlGaN layer. The above results suggest that: (i) 3nm spacer is sufficient to eliminate ionized impurity scattering, (ii) too heavy doping with too thick AlGaN layer may cause parellel conduction in the doped AlGaN layer. [1]S. Keller, G. Parish, P. T. Fini, S. Heikman, C.-H. Chen, N. Zhang, S. P. DenBaars, U. K. Mishra, and Y.-F. Wu, J. Appl. Phys. 86, 5850(1999). [2]J. Han, T.-B. Ng, R. M. Biefeld, M. H. Crawford, and D. M. Follstaedt, Appl. Phys. Lett. 71, 3114(1997). [3]C. Weisbuch and B. Vinter, Quantum Semiconductor Structures: Fundamentals and Applications (Academic, 1991), pp.129-131.

11:00 AM

DD8, Stability of AlGaN/GaN HEMT Epitaxial Wafers: *David William Gotthold*[1]; Ronald Birkhahn[1]; Shiping P. Guo[1]; Brian Albert[1]; Boris Peres[1]; [1]EMCORE Corporation, 145 Belmont Dr., Somerset, NJ 08873 USA

AlGaN/GaN HEMTs show great promise for high power and high frequency amplifiers. However, before these devices can move out of the lab and into useful systems, their reliability must be improved. Until recently, all the reliability research has primarily been on devices, but recent work at Emcore has revealed significant long term aging effects that occur in the AlGaN epitaxial material, without any device processing. Over a time period ranging from days to months, the sheet resistance of the as-grown wafers slowly increases from < 400?Ç/¡¼ to as high as 5000?Ç/¡¼. The effects of aluminum concentration, AlGaN barrier thickness, nucleation layer growth, capping layers, substrate polish, substrate quality, and storage environment have all been studied. It is clear that the overall AlGaN strain, as determined by Al content and barrier thickness, is the primary factor in determining epitaxial material lifetime, however most of the other listed parameters appear to have an effect on the degradation rate. By limiting the aluminum composition to ?T 30% and barrier thickness to ?T 23nm, epitaxial structures that are stable over the timeframe of this study (6 months) have been produced. However, the longer-term stability of this material is still in question.

11:20 AM

DD9, Study of Collector-Up AlGaN/GaN HBTs Grown by Metalorganic Chemical Vapor Deposition: *Uttiya Chowdhury*[1]; Ting Gang Zhu[1]; Michael Ming Wong[1]; Dongwon Yoo[1]; Milton Feng[2]; Peter Asbeck[3]; Russell D. Dupuis[1]; [1]The University of Texas at Austin, Microelect. Rsch. Ctr., 10100 Burnet Rd., Bldg. 160, Austin, TX 78758 USA; [2]The University of Illinois at Urbana-Champaign, Ctr. for Compound Semiconductor Microelect., 208 N. Wright St., Urbana, IL 61801 USA; [3]University of California at San Diego, Dept. of Electl. & Compu. Engrg., MC 0407, 9500 Gilman Dr., La Jolla, CA 92093-0407 USA

A novel HBT structure in collector-up configuration was studied in order to eliminate polarization effects in emitter-base AlGaN/GaN heterojunction. The epitaxial structures are grown by low-pressure metalorganic chemical vapor deposition (LP-MOCVD) on 2.0 in. diameter c-plane sapphire and 6H n-type SiC substrates. With standard MOCVD growth of nitrides on c-plane substrate with Ga-face on top, if the device is grown in emitter-up configuration, then a 2-dimensional electron gas (2-DEG) forms at the emitter-base heterojunction which has been proposed to be detrimental to device operation. This supplies the motivation for the study of an alternate collector-up configuration. The device structure consists of, from the substrate side, a 2 μm n+ -GaN as emitter contact layer, a 50 nm graded alloy composition (x=0-0.1) $Al_xGa_{1-x}N$ layer, a 150 nm n-$Al_{0.1}Ga_{0.9}N$ emitter layer, a 150 nm p-GaN:Mg base and finally a 300 nm n+ -GaN collector layer. The epitaxial structure was grown in two-step in order to reduce the Mg memory effects. The layers up to the base were grown in the first step, after which the chamber was baked extensively under hydrogen shroud flow to get rid of residual Mg. The collector layer was then regrown over the entire wafer (not selectively). The epitaxial sample was annealed in-situ in a nitrogen ambient in order to activate the Mg acceptors. The carrier concentrations for the emitter, base and collector were estimated to be $n\sim5\times10^{18}$, $p\sim5\times10^{17}$ and $n\sim2\times10^{19}$ cm^{-3}, respectively, while the concentration in the collector contact layer was $n\sim2\times10^{19}$ cm^{-3}. Secondary-ion mass spectroscopy (SIMS) measurement showed sharp concentration profile for Si and reasonably sharp profile for Mg dopant. Standard HBT device fabrication procedure was employed which consisted of two-mesa etching and two-metallization processes. The metallization scheme used for the emitter and collector was Ti/Au and Ni/Au metallization was used to form the base contact. The fabricated devices were then measured using standard computer based semiconductor parameter analyzer hardware. The emitter-base junctions of fabricated devices showed a low forward resistance, while the base-collector junction exhibited a somewhat high leakage current. We attribute this leakage current to the increased defect density arising from regrowth over high Mg-content p-layer. From the fabricated devices, we were able to obtain the common-emitter current voltage (I_C-V_{CE}) family of curves. Our preliminary data shows a collector-emitter offset voltage V_{CEoff}=4.5 V, and a collector-emitter breakdown voltage >20 V. The current gain, computed by dividing the change in collector current at a given V_{CE} by the change in the base current, was about β=1.5. The study also includes variation of structural parameters of the device and comparison of device performance.

11:40 AM DD10, Late News

Session EE: Low-Dimensional Structures: Quantum Dots and Wires

Friday AM
June 27, 2003

Room: Theatre
Location: Olpin Union Building

Session Chairs: James Merz, University of Notre Dame, Notre Dame, IN 46556-5602 USA; Mark Miller, University of Utah, Salt Lake City, UT 84112-0506 USA

8:20 AM

EE1, The Growth Behaviours of Aligned ZnO Nanowires on Si, Sapphire, and GaN Substrates by Carbothermal Reduction and Thermal CVD Methods: Hyun-Gi Hong[2]; Jung Inn Sohn[2]; *Seonghoon Lee*[1]; [1]Seoul

National University, Chmst. & Molecular Engrg., San 56-1, Shillim-Dong, Seoul 151-747 Korea; [2]Kwangju Institute of Science and Technology, 1 Oryong-Dong, Puk-Ku, Kwangju 500-712 Korea

Zinc oxide nanowires were grown on silicon, sapphire, and gallium nitride substrates by thermal chemical vapor deposition (CVD) and their structural and optical properties were examined using scanning electron microscopy (SEM), transmission electron microscopy (TEM), X-ray diffraction (XRD), and photoluminescence (PL) spectroscopy. The catalyst metal films are deposited using a pulsed laser deposition (PLD) technique under a pressure of 10-6 Torr. The metal thin film was converted into nanoparticles during CVD growth. Carbothermal reduction was used to vaporize the zinc and oxygen vapor easily, and source gases were reacted via the catalyst metal particles at 950°C by a Vapor-Liquid-Solid mechanism. In order to observe the orientation and alignment of zinc oxide nanowires, SEM and TEM images were obtained, which show that the growth direction of the zinc oxide nanowire depends on substrates because of differences in substrate crystal structure and lattice mismatch with zinc oxide. Gallium nitride was found to be a particularly good substrate for aligning the zinc oxide nanowires. The size of the zinc oxide nanowires is 20 to 100nm in diameter and a few micrometers in length. XRD pattern shows that the zinc oxide has a wurtzite structure. PL analysis shows a strong 379nm emission with full width at half maximum (FWHM) of 52.09 meV at an excitation wavelength of 325nm and an excitation power of 20mW.

8:40 AM

EE2, Microcharacterization of Size-Selected, Colloidal InP Quantum Dots and Rods: *S. P. Ahrenkiel*[1]; O. I. Micic[1]; J. M. Nedeljkovic[1]; A. J. Nozik[1]; [1]National Renewable Energy Laboratory, 1617 Cole Blvd., Golden, CO 80401 USA

Semiconductor nanoparticles offer numerous possibilities for optical emission and absorption at discrete wavelengths. The influences of quantum effects become more pronounced as the particle size is reduced, but the synthesis and characterization of such extremely small nanoparticles become increasingly challenging. We have examined InP quantum dots and rods with a range of sizes produced by colloidal chemistry from various organometallic precursors. The optical spectra from these materials are drastically altered with respect to bulk material by the quantum confinement of charge carriers. The structure and crystallography of larger InP nanoparticles are quite easily examined using transmission electron microscopy (TEM). Colloidal InP dots with sizes greater than about 40 Å show strong crystallinity, and ordering into close-packed arrangements can be induced by self-assembly mechanisms. Large InP rods, or fibers, with diameters ranging from 50 Å to several hundred Å, grow in the cubic (111) orientation from metallic In nucleation centers. The In spherules provide a means to control the diameter of the resultant InP products. However, the structural properties of extremely small InP dots and rods are difficult to probe using conventional TEM. Nonetheless, dots with sizes below about 30 Å are resolved that show narrow size distributions and weak indications of ordered packing. InP rods with 30 Å diameter and aspect ratios of ~10 are evident, but the degrees of crystallinity in these very small dots and rods remain difficult to ascertain. This work demonstrates an extension of the available length scale for the synthesis of colloidal InP nanoparticles.

9:00 AM

EE3, Observation of Multiple Negative Differential Resistances in Semiconductor Quantum Wires Self Assembled in Porous Alumina Templates: *Supriyo Bandyopadhyay*[1]; Sandipan Pramanik[1]; [1]Virginia Commonwealth University, Electl. Engrg., 601 W. Main St., Richmond, VA 23284 USA

We have observed muliple peaks in the current voltage characteristics of CdS nanowires of diameter 50 nm produced by electrodeposition of CdS in the pores of an anodic alumina film. These peaks have been observed at room temperature at voltages of less than 1 Volt. The origin of these peaks is believed to be linked with sequential hopping between CdS grains in the nanowire. High resolution TEM microsocpy has revealed that the nanowires typically consist of 40 nm grains separated by 10 nm amorphous regions that act as weak links. The observation of negative differential resistance in these structures is very significant since these are self ordered arrays of vertical quantum wires separted from each other by insulating barriers. This configuration is isomorphic with a nanoscale neuromorphic network proposed by a number of groups over the last five years [see, for example, Roychowdhury, Janes and Bandyopadhyay, Proc. of the IEEE, Vol 85,(1997)]. The observed negative differential resistance is sufficient to allow these structures to operate as nanoscale image processors and associative memory.

9:20 AM

EE4, One Unit Cell Width Ferroelectric Domains: *Shlomo Berger*[1]; Yariv Drezner[1]; [1]Technion, Matls. Engrg., Haifa 32000 Israel

Nanometer-sized ferroelectric domains, having a width of one unit cell, are observed in ultra-thin BaTiO3 films (2-7nm thick) using high resolution TEM. The nano-domains are arranged in multi-domains structures. This finding violates two well established concepts of a critical size below only single domain structures exist and a critical size below ferroelectricity disappears. Only 1800 domains and 900 domain boundaries are present in the nano-multi-domains structures. Most of the domains (type I) are oriented in parallel to the film plane and stabilized by a tensile stress higher than 0.6GPa. Few domains (type II), having the same width, are bended out of the film plane as a mean of strain relaxation. The bending angle is correlated with the domain length and the crystallographic planes of the tetragonal unit cell. The film exhibits ferroelectric behavior in either vertical or parallel directions to the film plane characterized by a polarization hysteresis loop. In the vertical direction the remanent polarization is of about 3nC/cm2 and the coercieve field is equal to 0.7 MV/cm. In parallel to the film plane the remanent polarization is higher by a factor of two while the coercive field is of about the same value compared to that of the vertical direction. Two temperature-dependent peaks of the dielectric constant were observed; a broad peak that spans between 60-800C and a narrow peak between 105-1100C. These peaks are attributed to two Curie points associated with the two observed types of ferroelectric multi-domains structures. The type II nano-domains are expected to have the lower Curie temperature since the tensile stress in the film decreases their tetragonal unit cells leading to a shift of the Curie point to a lower temperature. The higher Curie temperature, which is attributed to the type I domains, is still lower by about 200C than that of thermodynamically stable BaTiO3 bulk material. Thermodynamic criterions for the formation of nano-domains having one unit cell are given. Based on these criterions, such nano-domains can be formed within a narrow energetic window determined by strain, polarization, and depolarization energies.

9:40 AM

EE5, MBE-Grown Fe Ferromagnetic Quantum Dots: Yesha Zheng[1]; *Tak Ki So*[1]; Ning Wang[1]; Iam Keong Sou[1]; [1]The Hong Kong University of Science and Technology, Dept. of Physics, Clear Water Bay, Kowloon, Hong Kong China

Even though self-organized semiconductor quantum dots have had a history close to a decade, research on self-organized magnetic quantum dots has only been initiated for about a year. The quantum size effects of these magnetic nano-size materials may offer novel physical properties and also may open a new area in spintronics applications. Since there is a suitably large lattice-mismatch (about 5%) between Fe (twice of its lattice constant) and ZnS, one should expect the formation of self-assembled Fe quantum dots if a nanoscale Fe film is deposited on a smoothed ZnS surface. This talk will present the studies on a novel Fe quantum-dot system grown on ZnS/GaP(100) substrates by MBE. Three samples with Fe coverage of 0.45 (QD1), 0.82 (QD2) and 1.7 (QD3) ML were grown at 180°C. High-resolution transmission electron microscopy (HRTEM) imaging (both plan-view and cross-section) and diffraction techniques have revealed their micro-structure. Due to its low Fe coverage, QD1 does not show any Fe finger prints in its electron diffraction, however, its HRTEM plan-view images revealed that Fe QDs do exist in this sample with average diameter around 5 nm and a dot-spacing also around 5 nm. These dots are single crystalline with round bases however they are misaligned with each other (with different azimuthal rotation angles). The cross-section images of QD1 indicate that these QDs are of conical shapes. The resulting electron diffraction patterns of QD2 clearly show Fe characteristic spots embedded in the standard diffraction pattern of the ZnS buffer, indicating the Fe QDs are also single crystalline however they seem to be highly aligned with each other. The HRTEM images of QD2 indicate that the size of these dots is much larger with average diameter around 25 nm and a dot-spacing also around 25 nm. Their shapes are not round and seem to be resulted from coalescence of multi-dots. With the largest Fe coverage among the three samples, QD3 shows cloudy Fe islands with irregular shapes in its plane-view images. Its electron diffraction displays incomplete Fe ring structures indicating the

existence of some preferential orientations. In this talk, we will present a model to explain the above observations on the structural development of Fe QDs as a function of Fe coverage.

10:00 AM Break

Session FF: Silicon/Germanium Low-Dimensional Structures

Friday AM Room: Theatre
June 27, 2003 Location: Olpin Union Building

Session Chairs: Mark Miller, University of Utah, Salt Lake City, UT 84112-0506 USA; James Merz, University of Notre Dame, Notre Dame, IN 46556-5602 USA

10:20 AM Student

FF1, Ordering of Self-Assembled Ge Islands on Photolithographically Patterned Structures on Si (001): *Bin Yang*[1]; Arthur R. Woll[2]; Feng Liu[3]; Max G. Lagally[1]; [1]University of Wisconsin, Madison, Madison, WI 53706 USA; [2]Cornell University, Chess, Ithaca, NY USA; [3]University of Utah, Dept. of Matls. Sci. & Engrg., Salt Lake City, UT 84112 USA

We report ordering of self-assembled Ge quantum dots (QDs) on patterned structures on Si (001) without using complicated lithography. Starting from stripes and mesas fabricated by conventional lithography and plasma etching, we prepare Si stripes with narrow ridges and mesas with humped edges via high-temperature annealing. After this annealing step, we perform CVD growth at 650°C at a low growth rate (0.8ML/min). Deposited Ge self-assembles into coherent nanocrystals that align along the narrow ridges of the stripes and the sloped mesa edges. The self-assembled quantum dots, characterized by atomic force microscopy (AFM) and scanning electron microscopy (SEM), are on average 300 nm wide and 50 nm high after about 25 ML Ge deposition. This process avoids complicated lithography that is generally necessary to achieve alignment at the dimension of hundreds of nanometers. High-temperature annealing modifies the surface morphology and thus the elastic-energy distribution along the surface after 3ML Ge is deposited. Our continuum calculations show that the surface chemical potential achieves a local minimum at the stripe ridges and mesa edges because of elastic strain relaxation after 3ML Ge is deposited. Ge atoms diffuse preferentially in the chemical potential gradient and nucleate at the chemical-potential minimum to form 3D Ge QDs. The 1D nature of the strain field at stripes and edges promotes the 1D ordering of the 3D QD Ge islands. These results provide a simple process to create and control ordered preferential nucleation sites for QDs via mass transport on the substrate that may lead to eventual practical applications of Si/Ge QD arrays. Supported by ONR and NSF.

10:40 AM

FF2, Growth of Chemically Vapor Deposited Ge Nanowires on Si(001): *Ted Kamins*[1]; [1]Quantum Science Research, Hewlett-Packard Labs., Palo Alto, CA 94304 USA

Abstract not available.

11:00 AM

FF3, Silicon Nanowires Grown by Vapor Phase Epitaxy: *Sun-Gon Jun*[1]; *Mark S. Miller*[1]; [1]University of Utah, Matls. Sci. & Engrg., 122 S. Central Campus Dr., Rm. 304, Salt Lake City, UT 84112-0560 USA

Micrometer and nanometer scale crystalline whiskers have been grown via several methods since Wagner reported the vapor-liquid-solid mechanism of silicon whiskers in 1964. Recent results on nanoscale whiskers from several groups in a number of materials systems have renewed interest in expectation of engineering nano-electrical and nano-optical devices. We grew silicon nanowires, nanowhiskers, by vapor phase epitaxy (VPE) on Si (111) surfaces using gold as a catalyst. The growth relies upon a vapor-liquid-solid mechanism. Most of the results we present here are for atmospheric pressure growth using dilute silane in hydrogen mixtures, varying the temperature, concentration, a flow rate. For comparison, we also report more limited results using silicon tetrachloride at atmospheric pressure and silane at low pressure. Most of the nanometer scale Au catalysts were created by depositing thin layers of Au on Si that upon heating to 350°C or above broke up into molten Au-Si droplets. The size and shape of these droplets play a dominant role in determining the resulting nanowire morphology. The atmospheric silane concentrations were varied from 0.001% to 1%, the temperature from 400°C to 600°C, and the flow from 100 to 1500 sccm. The SiNWs, observed by transmission electron microscopy and scanning electron microscopy, exhibit growth defects that include bending and kinking. The wire sizes ranged from 30 nm to 300 nm, with lengths from 100 nm to 20 μm, depending on catalyst size and growth conditions. Increasing the temperature leads to a broader distribution of wire widths and a faster growth rate.

11:20 AM

FF4, Strong Near-Infrared Photoluminescence and Absorption from Si/SiGe Type-II Multiple Quantum Wells on Bulk Crystal SiGe Substrates: *Shuran Sheng*[1]; Nelson L. Rowell[2]; Sean P. McAlister[1]; [1]Institute for Microstructural Sciences, Natl. Rsch. Council of Canada, Bldg. M-50, 1200 Montreal Rd., Ottawa, Ontario K1A 0R6 Canada; [2]Institute for National Measurement Standards, Natl. Rsch. Council of Canada, 1200 Montreal Rd., Ottawa, Ontario K1A 0R6 Canada

The recent development of high quality bulk single-crystal SiGe broadened the scope for SiGe devices. Such substrates allow extended band engineering, with strain adjustment in strained-layer quantum wells (QWs) and superlattices as well as higher potential for integrated opto-electronics. We report a study of photoluminescence (PL) and optical absorption in high-quality UHV-CVD tensile-strained Si type-II multiple QWs grown on bulk crystal SiGe substrates at 525°C. Detailed PL experiments as a function of excitation density together with applied uniaxial stress were performed to study the band alignment and to help elucidate the origin of the observed PL peaks. Spatially direct and indirect transitions of the Si QWs and an intense broad sub-gap PL were observed. The broad PL band is quite efficient luminescence and persists at extremely low excitation densities. With increasing excitation power, the PL lines of Si QWs shift to lower energies, whereas the sub-gap PL shifts to higher energy. The PL lines from the SiGe substrate show no such shifts. Both the Si QWs PL and the sub-gap PL show much weaker excitation power dependences than the substrate PL. The applied (110) compressive stress results in a red shift of the substrate PL lines, as expected, but a blue shift of the Si QWs PL lines due to the built-in tensile strain being compensated by the applied stress. The sub-gap PL was verified not to be correlated with the SiGe substrate since it was essentially unchanged, but the substrate PL decreased more than 70% in intensity, when the excitation wavelength was changed from 514 nm to 458 nm. This was further confirmed by the observation that it shifted in the opposite direction under the applied stress. Nevertheless, the sub-gap PL is probably not related to the spatially indirect transitions in the type-II Si QWs, either as it peaks at energy of ~200 meV lower and no phonon replica was observed. Its no-phonon nature was also supported by the infrared (IR) data - strong absorption was observed in this near-IR region. The absorption coefficient α near the absorption edge Eg was found to follow the square law: $(\alpha h\upsilon)^2 \propto (h\upsilon\text{-}Eg)$ better than the square root law: $(\alpha h\upsilon)^{1/2} \propto (h\upsilon\text{-}Eg)$. The Eg value deduced according to the square law is in good agreement with the peak energy of the sub-gap PL with quantum confinement, excitonic binding energy and exciton localization energy considered. However, the Eg value deduced according to the square root law is unreasonably small. These results suggest that the Si QWs samples on bulk crystal SiGe might partially have become pseudo-direct gap materials. Details of this work along with the implication of the strong near-IR PL and absorption observed in Si/SiGe type-II QWs on SiGe will be presented.

Session GG: AlGaN/GaN HEMTs: RF Dispersion, Processing Effects and Novel Gate Oxides

Friday AM Room: Saltair
June 27, 2003 Location: Olpin Union Building

Session Chair: Michael Manfra, Lucent Technologies, Bell Labs., Murray Hill, NJ 07974 USA

8:20 AM

GG1, Influence of Dual Frequency PECVD Si3N4 Passivation on the Electrical Characteristics of AlGaN/GaN Heterostructure Field Effect Transistors: Wei Sin Tan[1]; *Peter A. Houston*[1]; Geoff Hill[1]; Charlie M.W. Low[1]; Robert J. Airey[1]; Peter J. Parbrook[1]; [1]University of Sheffield, Dept. of Elect. & Electl. Engrg., Mappin St., Sheffield S17 4PP UK

Silicon nitride (Si3N4) passivation is commonly used to reduce the effects of current collapse (reduced rf current compared to dc current) in AlGaN/GaN heterostructure field effect transisitors (HFETs) and can also increase the maximum dc drain current. The reasons behind these observed changes remains unclear and the purpose of this paper is to try to shed some light on the mechanisms responsible. The structures used here were grown by metal organic vapour phase epitaxy on sapphire substrates with a 3 µm GaN buffer layer grown at 1030°C. The modulation-doped AlGaN layer consisted of a 15 nm unintentionally doped AlGaN spacer and a 15 nm Si doped (nominally ~1x1018 cm-3) AlGaN donor layer. The HFET devices were fabricated using a conventional mesa isolation, with Schottky gates approximately 1.5 µm long by 140 µm wide and the source-gate and gate-drain spacings of 3 µm. Measured room temperature sheet carrier concentration and Hall mobility for the unpassivated devices were (1.1-1.6) x 1013 cm-2 and 900-1100 cm2V-1s-1 respectively. The dielectric passivation was deposited by PECVD after formation of the contacts. From the literature, an RF excitation frequency of 13.56 MHz for the PECVD deposition process is in widespread use, resulting in a deposited film which is under tensile stress. However, by intermixing low (below 1 MHz) and high frequency RF excitation components, the film stress can be changed from tensile to compressive. We observed a striking linear dependence of the change in maximum drain current in the HFET devices on the amount of stress in the deposited dielectric. The maximum drain current increased by up to 20% for tensile stressed dielectric layers and reduced by as much as 30% for compressive layers compared to unpassivated devices. Similar trends were also observed in the changes to the sheet carrier concentration based on 77K Hall measurements. A variation in the knee voltage and the slope of the pre-saturation region of the I-V curves with dielectric stress suggested that the dielectric layer significantly affects the device channel conductivity. Gated transmission line measurements revealed that only the source-gate and gate-drain gap resistances of the device were altered upon passivation, with no significant change to the channel and contact resistances. In addition, the mitigation of current collapse observed after Si3N4 surface passivation was not dependent on the stress of the latter. These observations provide new insight into the effects and mechanisms related to surface passivation of HFETS.

8:40 AM

GG2, RF Dispersion in Unpassivated AlGaN/GaN HEMTs Grown by MBE: *Oleg Mitrofanov*[1]; Michael Manfra[1]; Nils Weimann[1]; [1]Bell Laboratories, Lucent Technologies, 600 Mountain Ave., Murray Hill, NJ 07974 USA

Recent advances in the development of AlGaN/GaN high electron mobility transistors (HEMTs) has led to the demonstration of power densities exceeding 10W/mm at 8GHz for small periphery devices. Nevertheless, significant RF dispersion is still observed in many devices and represents a significant challenge to future progress. RF dispersion is characterized by an increase of the knee voltage and a drop in the maximum channel current at microwave frequencies. Several groups have shown that the effects of dispersion can be mitigated by passivating the device surface with SiN. This result strongly suggests that surface state traps are responsible for dispersion, however the exact physical mechanism is not well understood. We have recently demonstrated unpassivated AlGaN/GaN HEMTs grown by plasma-assisted MBE on 6H-SiC with power densities exceeding 8W/mm at 2GHz. In this talk, we present the results of a detailed study of dispersion in our MBE grown layers. We have probed dispersion in these devices using a variety of pulsed gate techniques. Transient behavior of the drain current under different gate voltage conditions and as a function of temperature can help characterize the active states responsible for trapping. For our best devices, dispersion effects are not significant. We find that the full channel is restored within 1ms after the gate is pulsed from pinch-off to 0 volts. The measurement is limited by the instrument temporal resolution. In order to better understand trapping behavior in these MBE grown layers, we currently exploring dispersion in our poorer performing devices. Measurements are performed on devices in which the drain current reaches only ~70% of the dc value within 1 ms after switching the gate voltage from pinch-off to 0 V. The drain current transients depend on a number of factors. Firstly, gate lag response depends on the off-state gate voltage. The transient is slower if the gate is biased at voltage lower than the pinch-off voltage, suggesting that states within the channel or buffer may play a role. The transient time also depends on the gate-drain separation, implying that the gate lag is also related to the surface states between the gate and drain contacts. These devices also exhibit slow drain current slump under applied gate voltage. The current slump is measured by turning on the device with short low duty cycle gate pulses and sampling the source-drain current during each pulse. The drain current drops by ~2% during first few hours, after which the current stabilizes. We are currently studying the current dynamics as a function of temperature. Temperature studies may elucidate the energy scale of the traps contributing to dispersion. Finally, we will correlate the measured dispersion with structure design and MBE growth conditions.

9:00 AM

GG3, Reduction of Surface-Induced Current Collapse in AlGaN/GaN HFETs on Free-Standing GaN Substrates: *Yoshihiro Irokawa*[1]; B. Luo[2]; F. Ren[2]; B. P. Gila[3]; C. R. Abernathy[3]; S. J. Pearton[3]; C.-C. Pan[4]; G.-T. Chen[4]; J.-I. Chyi[4]; S. S. Park[5]; Y. J. Park[5]; [1]Toyota Central R&D Labs., Inc., Nagakute, Aichi 480-1192 Japan; [2]University of Florida, Dept. of Chem. Engrg., Gainesville, FL 32611 USA; [3]University of Florida, Dept. of Matls. Sci. & Engrg., Gainesville, FL 32611 USA; [4]National Central University, Dept. of Electl. Engrg., Chung-Li 32054 Taiwan; [5]Samsung Advanced Institute of Technology, Suwon 440-600 S. Korea

AlGaN/GaN heterostructure field effect transistors have demonstrated excellent potential for microwave power transistor applications such as in next generation wireless base stations, phased array radar and satellites. There are several remaining hurdles to commercialization of these devices, including the high gate leakage of metal gate structures at elevated temperatures and the reduced drain current and increased knee voltage under high drain-source voltage conditions. The latter phenomenon is often referred to as current collapse. It is generally accepted that the presence of traps on the surface between the gate and drain or in the GaN buffer layer is the cause of this effect, though creation of a second parasitic virtual gate that can reduce the channel current. Numerous authors have shown that deposition of thin dielectric or oxide layers, including SiNx, MgO and Sc_2O_3, can provide effective surface passivation on HFET structures grown epitaxially on lattice-mismatched substrates such as Al_2O_3 or SiC. Little is known about the current collapse effect in AlGaN/GaN HFETs on free-standing GaN substrates. In this study, we made a comparison of the dc and pulsed characteristics of AlGaN/GaN HFETs on both GaN and Al_2O_3 substrates before and after Sc_2O_3 passivation. The FET structure included a 3 $_{\mu}$m thick undoped GaN buffer and 40 nm unintentionally doped $Al_{0.3}Ga_{0.7}N$ layer. This structure was grown simultaneously on both c-plane Al_2O_3 and free-standing (200 $_{\mu}$m thick), n-type GaN substrate. The HFET process sequence included Cl_2/Ar dry etch mesa isolation, lift-off of e-beam deposited Ti/Al/Pt/Au Ohmic contacts, annealing of these contacts at 850°C for 45 s under a flowing N_2 and lift-off of e-beam deposited Pt/Au Schottky contacts. In the drain-source current versus drain-source voltage characteristics from both types of devices before and after passivation, the homoepitaxial HFETs had a higher output resistance and lower knee voltage because of the higher electron mobility. Both types of devices showed higher drain-source current after Sc_2O_3 passivation due to a

reduction of electron accumulation into surface traps associated with dislocations and other defects. In the transfer characteristics, the transconductance is higher for the homoepitaxial HFETs. In the gate lag measurements, the HFETs on Al_2O_3 showed a large difference between the dc and pulsed drain current in unpassivated devices. On the other hand, the Sc_2O_3 passivation mitigated most of this current degradation, as reported previously. By contrast, the HFETs on GaN showed a much lower initial amount of gate current lag and therefore a smaller improvement upon passivation. This suggests that a significant portion of the degraded output power under large signal conditions is due to surface states associated with dislocations.

9:20 AM Student

GG4, The Effect of Processing Induced Stress on AlGaN/GaN HFET Characteristics: *Adam M. Conway*[1]; Peter M. Asbeck[1]; Jeong S. Moon[2]; [1]University of California, San Diego, ECE Dept., 9500 Gilman Dr., MS 0407, San Diego, CA 92093 USA; [2]HRL Laboratories LLC, 3011 Malibu Canyon Rd., Malibu, CA 92065 USA

This paper demonstrates for the first time that the electrical characteristics of $Al_xGa_{1-x}N$/GaN HFETs can be significantly affected by stress effects resulting from Si_3N_4 passivation layers and from recess etching. GaN-based transistors are being very actively developed for microwave power applications. Piezoelectric and spontaneous polarization induce sheet charges of $1x10^{13}$q/cm^2. During device processing, additional stress can be unintentionally introduced by means of alloyed ohmic contacts, stressed Schottky metal, gate recess etching or dielectric overlayers. A Si_3N_4 passivation layer is normally deposited to minimize the effects of surface states, which hamper device performance in the form of gate or drain lag, and current slump. Depending on the deposition technique and growth conditions, the film can be under tensile or compressive stress as high as $8x10^9$ dynes/cm^2. The stress distribution in the underlying semiconductor is much lower than this on average, but is sharply peaked at openings in the Si_3N_4 film, next to the gate metal. Similarly, for a gate recess etch, the stress distribution is concentrated at the edges of the recess well. We have analyzed the stress distribution for these configurations, assuming elastically isotropic media.[1] The large resultant stress in turn creates piezoelectric polarization, the divergence of which induces bound charge. The bound charges can be donor- or acceptor-like, depending on the sign of the stress and position. The effect of this added charge on HFET threshold voltage, breakdown voltage and gate leakage current are discussed in this work. A commercially available two-dimensional simulator was used to model the transistor in the presence of the piezoelectric polarization. For the Si_3N_4 case, the added stress-induced charge is concentrated at the edge of the gate, either compensating or adding charge to the channel underneath the gate. Thus, the voltage required to pinch off the channel is modified from the non-stressed case. The magnitude of the threshold voltage change depends on the Si_3N_4 film stress, thickness and gate length. For 1000A of Si_3N_4 under tensile stress of $5x10^9$ dynes/cm^2 on a 0.15μm gate, the threshold voltage shifts by 1.25V. The added bound charge also provides an additional electric field that can enhance or decrease the electric field from gate to drain or from gate to channel, causing a change in gate leakage current and breakdown voltage. Experimental results are presented which show that the threshold voltage changes during application of Si_3N_4 as expected from the simulations. Measurements with $Al_xGa_{1-x}N$ /GaN HFETs show that threshold voltage shifts which have the correct sign and magnitude for a Si_3N_4 film in tensile stress are obtained. [1]P.A. Kirkby et al., J. of Appl. Phys, vol.50, no.7, pp.4567-4578, July 1979.

9:40 AM

GG5, Characterization of Processing Effects on Defects in AlGaN/GaN HEMT's and Correlation with Device Performance: Gregg H. Jessen[1]; G. David Via[1]; James K. Gillespie[1]; *Robert C. Fitch*[1]; Brad D. White[2]; Shawn T. Bradley[2]; Dennis E. Walker[2]; Leonard J. Brillson[2]; [1]Air Force Research Laboratory, Sensors Direct., Bldg. 620, 2241 Avionics Cir., Wright Patterson AFB, OH 45433-7322 USA; [2]Ohio State University, Dept. of Electl, Engrg., 205 Dreese Lab., 2015 Neil Ave., Columbus, OH 43210 USA

The quest for making AlGaN/GaN high performance microwave devices into a commercially viable product is hindered by material quality uniformity and the ability to control material defects. Attempts to characterize HEMT structures prior to fabrication by monitoring key material and electrical parameters have been met with mixed success in predicting future device performance. In this work, we characterize AlGaN/GaN HEMT's at the gate by using micro-cathodoluminescence spectroscopy (μCLS) to detect spectral features associated with specific point defects related to gallium vacancies and p-type substitutional impurities. We use these spectral features as figures of merit to monitor processing effects and relative defect concentrations at individual device locations and correlate the optical signatures with DC and RF device performance. The HEMT's in this work were grown by MOCVD on sapphire and silicon carbide substrates with Al mole fraction from 0.24-0.30. We observe point defect reduction due to thermal processing steps involved with the ohmic contact anneal. We also observe the decline in AlGaN surface material quality as a result of RIE surface damage, which has implications for gate recess processing. We find that sheet resistance can be predicted accurately by observing characteristic AlGaN band edge emission prior to fabrication while contact resistance correlates with measurements performed after processing. In this sample set with relatively low defect densities, no particular defect is found to directly correlate with contact resistance. However, the ratio of the observed defects tracks well with contact resistance. The depth dependent capabilities of the μCLS technique also allow us to estimate the observed defects to be localized near the GaN side of the AlGaN/GaN interface. These observations provide physical insight to the nature of the interaction of these defects and their effects on ohmic contact resistance. We propose a model to explain our findings in terms of a lateral contact resistance related to a scattering barrier arising from point defect segregation around threading dislocations and the unfavorable energy conditions for gallium vacancies to form in these regions. For a HEMT to perform well, all of the device parameters must meet minimally acceptable criteria. However, we have shown in this work that some variables such as sheet resistance can be predicted prior to fabrication while others such as contact resistance are detectable after fabrication is complete. In this sample set, variations in contact resistance appear to have the largest effect on frequency response in spite of variations seen in terms of capacitance changes from variations in the 2-DEG or nominal AlGaN layer thickness. These results show that optical spectral characterization can be used to understand AlGaN/GaN device and material properties and optimize their processing and growth.

10:00 AM Break

10:20 AM Student

GG6, Trap States Induced Frequency Dispersion of AlGaN/GaN Heterostructure Field Effect Transistors: *R. M. Chu*[1]; Y. G. Zhou[1]; K. J. Chen[1]; K. M. Lau[1]; [1]Hong Kong University of Science & Technology, Dept. of Electl. & Elect. Engrg., Clear Water Bay, Kowloon Hong Kong

The power handling capability of AlGaN/GaN heterostructure field effect transistors was found to degrade severely with increasing operation frequency. Several assumptions have been put forward to explain this DC to RF dispersion, such as surface trapping in the access region between the gate and drain, traps in the GaN buffer layer, or dielectric loss in the AlGaN barrier layer. In this investigation, we present a model which includes a previously overlooked trapping and de-trapping process at the Schottky metal-semiconductor interface. Effect of this interfacial trapping process was examined through frequency-dependent impedance measurement of AlGaN/GaN Schottky diodes. Our model follows the widely recognized Cowley-Sze Schottky theory which assumed a practically existing interfacial layer between metal and semiconductor.[1] Under gate voltage modulation, presence of the interfacial layer leads to an "unpinning" of the Fermi level at semiconductor surface, leading to a change of the surface state occupation. This trapping and de-trapping process can be equivalently modeled as a resistor and a capacitor (both are frequency-dependent) in serial connection between the gate metal and the semiconductor. Theoretical calculation reveals that the interfacial trapping can drastically suppress the gate-to-channel modulation efficiency at high frequency, strongly depending on the interfacial layer thickness. To examine the theoretically predicted frequency dispersion, impedance (i.e., serial resistance and capacitance) of an AlGaN/GaN Schottky diode was measured using HP4284 and HP4291 systems, with measurement frequency ranging from 20 Hz to 1.8 GHz. Results show that the capacitance component exhibits an evident decrease when the measurement frequency becomes larger than 10 MHz. At zero DC bias, high-density electrons accumulate closely beneath the AlGaN barrier layer, therefore the contribution of traps in the GaN buffer layer and AlGaN/GaN interface can be excluded. The experimentally observed frequency dispersion of impedance is consistent with that predicted by the metal-semiconductor interfacial trapping model. In addition to sur-

face traps, AlGaN/GaN interface states may also contribute to the dispersion of transistor performance between DC and RF. Frequency-dependent capacitance of the AlGaN/GaN Shcottky diode was measured at different gate biases. Dispersion of the capacitance-voltage curves was observed in the vicinity of threshold voltage at low frequencies, indicating the existence of AlGaN/GaN interface trap states. Adopting an analytical method similar to that developed for trap states in metal-oxide-semiconductor capacitors, we extracted the interface trap density and the corresponding time constant at several bias points, yielding values in the order of $10^{13}cm^{-2}eV^{-1}$ and 1 µs. Reference: [1]H. Rohdin, N. Moll, A. M. Bratkovsky, and C. Y. Su, Phys. Rev. B 59, 13102 (1999).

10:40 AM Student

GG7, AlGaN/GaN Metal Oxide Semiconductor Field Effect Transistors using Titanium Dioxide: *Peter J. Hansen*[1]; S. Heikman[2]; S. P. DenBaars[1]; R. A. York[2]; U. K. Mishra[2]; J. S. Speck[1]; V. Vaithyanathan[3]; D. G. Schlom[3]; [1]University of California, Matls., Santa Barbara, CA 93106 USA; [2]University of California, ECE, Santa Barbara, CA 93106 USA ; [3]The Pennsylvania State University, Matls. Sci. & Engrg., University Park, PA 16802 USA

Minimizing gate leakage in field effect transistors used in microwave power electronics is desirable both for low noise and reliability. An SiO_2 layer under the gate has been shown to reduce gate leakage current by six orders of magnitude compared to that of a conventional HFET.[1,2] Ideally the gate leakage current should be suppressed without affecting the transconductance or threshold voltage of the device. A high K dielectric should allow for a thin equivalent oxide thickness while reducing gate leakage. Titanium dioxide (TiO_2, with the rutile structure) was grown epitaxially on AlGaN/GaN HFET structures by molecular beam epitaxy (MBE). Growth was first performed on GaN templates to establish epitaxial growth conditions. X-ray diffraction showed [001] TiO_2 ‖ [10-10] GaN and (100) TiO_2 ‖ (0001) GaN. The full width at half max (FWHM) of the TiO_2 (200) peak was 0.31° in the theta -2 theta scan and the 2 omega FWHM was 0.86°. Growth conditions established for the oxide on GaN were then used to grow TiO_2 on AlGaN/GaN structures. Metal Oxide HFETs were processed with TiO_2 under the gate in the following manner. HFETs were partially processed prior to TiO_2 deposition. First, source and drain ohmic contacts were defined and deposited. The devices were then isolated using a reactive ion etch. Gate metals were deposited on some of the die on the wafer and the devices in these die were measured as standards. 30 nm of TiO_2 was then blanket deposited over the wafer. Gate metals were deposited on the remaining die. The gate leakage current of this structure is approximately four orders of magnitude lower than that of a conventional HFET, at ~4*10-6 mA/mm at 50V. A maximum device current of approximately 1A/mm was measured at a positive gate bias of +1V, with a pinch off voltage of approximately -7.5V. The transconductance was 140 mS/mm, approximately 20% less than for devices with no dielecric. The dielectric constant of the TiO_2 was ~43. These results indicate that TiO_2 is an excellent candidate as a gate dielectric on AlGaN/GaN HFETs. The high dielectric constant of the oxide allows for a low impact on the transconductance and threshold voltage of the device while reducing gate leakage. Further investigation of growth and processing conditions is required for device optimization. [1]M. A. Khan, X. Hu, G. Sumin, A. Lunev, J. Yang, R. Gaska, and M. S. Shur, IEEE Trans. Electron. Dev. Lett., 21, 63 (2000). [2]M. A. Khan, X. Hu, A. Tarkji, G. Simin, J. Yang, R. Gaska, and M. S. Shur, Appl. Phys. Lett., 77, 1341, (2000).

11:00 AM Student

GG8, AlGaN/GaN MOSHEMT Using Sc_2O_3 as the Gate Oxide: *Rishabh Mehandru*[1]; Ben Luo[1]; Jihyun Kim[1]; Fan Ren[1]; Brent P. Gila[2]; Andrea H. Onstine[2]; Cammy R. Abernathy[2]; Stephen J. Pearton[2]; D. Gotthold[3]; R. Birkhahn[3]; B. Peres[3]; R. Fitch[3]; J. Gillespie[4]; T. Jenkins[4]; J. Sewell[4]; D. Via[4]; A. Crespo[4]; [1]University of Florida, Chem. Engrg., C/O Rm. 227, Bldg. #723, Gainesville, FL 32611 USA; [2]University of Florida, Matls. Sci. & Engrg., Gainesville, FL 32611 USA; [3]EMCORE, Somerset, NJ 08873 USA; [4]Air Force Research Laboratory, Sensors Direct., Wright-Patterson AFB, OH 45433-7322 USA

There is great interest in the development of AlGaN/GaN based high electron mobility transistors (HEMTs) for high power and high frequency applications. In order to reduce the gate leakage current, metal oxide semiconductor (MOS) based HEMT technology was developed using dielectrics of SiN_x and SiO_2 with different deposition techniques. An additional problem with HFET is that without some form of surface passivation they exhibit so-called current collapse at rf conditions. We have previously shown that both Sc_2O_3 and MgO deposited by O_2 rf plasma assisted Molecular Beam Epitaxy (MBE) provide low interface state densities on GaN and also effective suppression of the effects of surface states on rf output power. In particular Sc_2O_3 is a very promising candidate as a gate dielectric and surface passivant because it is more stable on GaN than MgO. Sc_2O_3 has a bixbyite crystal structure, large bandgap (6.3 eV) and high dielectric constant. In this work, Sc_2O_3 was used as the gate oxide to reduce the gate current and as passivation layer to suppress the drain current collapse. The AlGaN/GaN HEMT structures were grown with a Metal Organic Chemical Vapor Deposition (MOCVD) on c-plane Al_2O_3 substitutes. A Cl_2/Ar based discharge in an Inductively Coupled Plasma (ICP) system was used to define the mesa. Ohmic metallization and ohmic anneal preceded the gate dielectric growth. Then the wafer was divided in two pieces and 400 Å of Sc_2O_3 was grown on one piece by rf plasma-accelerated MBE at 300°C using elemental Sc and O_2 derived from a 13.56 MHz plasma source. Gate metal was deposited on both the wafers. The ICP system was employed to open the Sc_2O_3 window for final metal deposition. The HEMT and MOSHEMT characteristics were measured in both dc mode and pulsed mode using an Agilent 4156°C parameter analyzer for dc mode and a pulse generator, dc power supply and oscilloscope for the pulsed measurements. The maximum drain source current, IDS reaches a value of over 0.8 A/mm and is ~40% higher on Sc_2O_3 /AlGaN/GaN transistors relative to conventional HEMTs fabricated on the same wafer. The MOS-HEMTs can be modulated to +6 V of gate voltage. Gate lag measurements further corroborate the effectiveness of Sc_2O_3 in reducing the surface state density at the interface. Threshold voltage of the MOSHEMT is in good agreement with the theoretical value, indicating the Sc_2O_3 retains a low surface state density on the AlGaN/GaN structures and effectively eliminates the collapse in drain current seen in unpassivated devices.

11:20 AM Student

GG9, Highly Selective, Smooth PEC Undercut Etching of Heterostructures: *Yan Gao*[1]; Andreas R. Stonas[2]; Ilan Ben-Yaacov[2]; Umesh K. Mishra[2]; Steve P. DenBaars[1]; Evelyn L. Hu[1]; [1]University of California, Santa Barbara, Matls. Dept., Santa Barbara, CA 93106 USA; [2]University of California, Santa Barbara, Electl. & Compu. Engrg. Dept., Santa Barbara, CA 93106 USA

Photoelectrochemical (PEC) wet etching has been found to be very promising as a low-damage means of fabricating GaN-based devices. The doping- and bandgap-dependence of PEC etching can be applied to form three dimensional device structures by selective etching of a particular thin layer in the heterostructure. We have employed this selective, lateral PEC wet etching in the formation of a novel GaN electronic device, a Current Aperture Vertical Electron Transistor (CAVET).[1] The direction of current flow in CAVETs is perpendicular to the surface, promising high breakdown voltage and low dispersion; an etched aperture constrains the current flow. Our previous work formed the aperture by selectively etching a thin, unintentionally-doped In0.03Ga0.97N sacrificial layer. This work examines the optimization of the doping of the sacrificial layer, to improve device performance, and the concomitant changes in PEC etch conditions to maximize etch selectivity, uniformity and smoothness. Selectivity was found to be affected by the nature of the doping of the sacrificial layer, and by the concentration and composition of the etchant. We will compare results using both KOH and HCL. I-V characteristics of the initial CAVET devices will be presented also. [1]Y. Gao, A. R. Stonas, I. Ben-Yaacov, U. K. Mishra, S. P. DenBaars, E. L. Hu, AlGaN/GaN Current Aperture Vertical Electron Transistors (CAVET) fabricated by Photoelectrochemical wet etching, accepted by Electronics Letters (2003).

Session HH: Narrow Bandgap Nitrides and Arsenides

Friday AM Room: Auditorium
June 27, 2003 Location: Olpin Union Building

Session Chairs: Charles Tu, University of California, Dept. of Electl. & Compu. Engrg., La Jolla, CA 92093-0407 USA; Dan Friedman, National Renewable Energy Laboratory, Golden, CO 80401-3305 USA

8:20 AM

HH1, Identification of Defects in GaNP by Optically Detected Magnetic Resonance: *Weimin M. Chen*[1]; N. Q. Thinh[1]; I. A. Buyanova[1]; C. W. Tu[2]; [1]Linkoping University, Dept. of Physics & Measurement Tech., Linkoping 581 83 Sweden; [2]University of California, Dept. of Electl. & Compu. Engrg., La Jolla, CA 92093-0407 USA

Anion-mixed III-N-V semiconductors such as Ga(In)NAs and GaNP represent a new class of highly mismatched electronic materials, and have recently received great attention due to their fascinating physical properties and potential applications. Because of the large mismatch in size and electronegativity between N and other group-V atoms it replaces, the anion-mixed III-N-V materials exhibit a number of attractive properties among which the predominant signature is the giant bowing of the bandgap energy. Due to the same mismatch, the preparation of the materials remains a great challenge and should resort to non-equilibrium growth conditions. As a result, an increasing content of N in III-N-V alloys is expected to facilitate formation of various extended and point defects, affecting alloy quality. In this work we address this important defect issue by using optically detected magnetic resonance (ODMR) measurements. We reveal the first experimental signatures of intrinsic defects in GaNP. One of the defects has been identified as a P(Ga)-N complex, exhibiting a central hyperfine structure due to interactions with a nuclear spin I=1/2 (most likely P(Ga) antisite) and also a nuclear spin I=1 due to one N atom. The corresponding ODMR spectrum was found to be isotropic, suggesting an A1 symmetry of the defect state. Stronger localization of the electron wave function at the defect as compared to the isolated P(Ga) antisite in its parent binary compound GaP suggests an important role of the N atom as an electron trap in the material. We have also demonstrated that defect formation is facilitated by increasing N composition in the alloys.

8:40 AM

HH2, Signature of the Defect Limiting the Minority-Carrier Lifetime in GaInNAs: *Aaron J. Ptak*[1]; Steve W. Johnston[1]; Sarah Kurtz[1]; [1]National Renewable Energy Laboratory, Natl. Ctr. for Photovoltaics, MS3212, 1617 Cole Blvd., Golden, CO 80401 USA

GaInNAs material quality is approaching necessary levels for long-wavelength lasers, but much work is necessary before the material is useful in next-generation, multijunction solar cells. The quality of grown layers, including the photoluminescence intensity, mobility, and especially the minority-carrier lifetime, is significantly reduced with the introduction of nitrogen into GaAs. Experimental studies of defects in GaInNAs typically show a great assortment of levels in the bandgap, making it difficult to ascertain which defect or defects are having a profound influence on material quality. Here, we present deep-level transient spectroscopy (DLTS) measurements of our GaInNAs material showing only two traps, a deep hole trap and a relatively shallow electron trap, allowing us to simplify the picture. The hole trap appears with an activation energy between 0.5 eV for low-bandgap samples (Eg~1.0 eV) and 0.8 eV for high-bandgap samples (Eg~1.3 eV), with respect to the valence band maximum (VBM). Additionally, an electron trap appears almost fixed in the bandgap with changing nitrogen concentration at an energy ~0.9 eV above the VBM. The activation energy of the electron trap has a much smaller dependence on the bandgap than does the hole trap. This bandgap dependence makes the energy level of the electron trap quickly approach the conduction band minimum (CBM) as the bandgap decreases, while the hole trap continues to appear near the center of the gap. Forward-bias DLTS measurements show an additional deep electron trap. It is probable that this electron trap is the same defect as the deep hole trap, observed under conditions of electron and hole emission, respectively. Because the same defect traps both electrons and holes, the result is a midgap state acting as a very efficient channel for recombination. The Shockley-Read-Hall treatment of trapping centers indicates it is far more probable that a mid-gap state will drastically affect minority-carrier lifetimes than a relatively shallow level, supporting the idea that the mid-gap state is the defect limiting the minority-carrier lifetime.

9:00 AM

HH3, Trap-Dominated Minority-Carrier Recombination in GaInNAs pn Junctions: *Daniel J. Friedman*[1]; John F. Geisz[1]; [1]National Renewable Energy Laboratory, 1617 Cole Blvd., Golden, CO 80401 USA

GaInNAs with a few % [N] is of great fundamental as well as practical interest for application in long-wavelength LEDs and solar cells. Intriguingly, minority-carrier recombination in GaInNAs is invariably found to be significantly faster than in GaAs. In GaInNAs pn junctions, the high recombination rate leads to large junction dark currents, a serious problem for any devices which require low dark current. Photoluminescence decay and DLTS studies of this material indicate the presence of lifetime-reducing defect levels in the gap, but do not directly quantify the effects of the levels on the dark current to identify which level is responsible for the high recombination rates. Here, we quantitatively study the magnitude and characteristic n>1 ideality factor of the dark current, using it as a direct probe of the recombination mechanism limiting device performance. We grew a variety of GaInNAs pn junctions with bandgaps ranging from ~0.95 to 1.1 eV by MOVPE, and characterized them with CV, spectral quantum efficiency, and temperature-dependent dark-JV measurements. Consistent with previous reports, the dark currents are not well described by the n=1 diffusion dark current mechanism which does so well in describing dark currents in high-quality GaAs junctions. The dark current-voltage (JV) curves show a wide range of magnitudes and shapes; the ideality factor for these devices is typically in the range of n=1.2 to 1.5, not n=1. Furthermore, computing the diffusion dark current for these GaInNAs junctions, we find that diffusion recombination is a negligible contribution to the total dark current for these junctions. The extensive body of literature on defect states in GaInNAs suggests recombination through recombination/generation (RG) centers in the bandgap is likely to be significant. To evaluate quantitatively the contribution of the RG dark current, we use the classic theory of Sah, Noyce and Shockley to compute the RG dark current as a function of voltage and temperature. Fitting to the measured JV curves gives RG-center activation energies and carrier capture lifetimes. With suitable choices of these parameters, remarkably good agreement with the magnitude and functional form of the measured voltage- and temperature-dependent dark currents is found, constituting strong evidence that the observed dark currents are dominated by recombination at RG centers. The RG-center energy is found to be constant at ~0.3 eV below the conduction band or above the valence band as the bands move closer with increasing [N] (the two possiblities cannot be distinguished with this approach), reasonably consistent with a previous report by Kaplar (JAP v90 p3405). The corresponding limiting capture lifetimes are in the range of ~0.01-1 ns, tending to decrease with decreasing bandgap (increasing [N]), implying RG center density increases with [N].

9:20 AM Student

HH4, Strong Photoluminescence Enhancement of 1.3 µm GaInNAs Active Layers by Introduction of Antimony: *Seth Robert Bank*[1]; Homan Bernard Yuen[1]; Wonill Ha[1]; Vincent Froedrick Gambin[1]; Mark Allen Wistey[1]; James S. Harris[1]; [1]Stanford University, Electl. Engrg., 126X CIS-X, Via Ortega, Stanford, CA 94305 USA

The desire to bring fiber to the home has motivated the need for inexpensive, yet high-performance, directly modulated vertical-cavity surface-emitting lasers (VCSELs) emitting near 1.3 µm for coarse wavelength division multiplexing (CWDM) networks. Seven years ago, Kondow et al. proposed that the introduction of dilute amounts of nitrogen into InGaAs could yield GaAs-based materials with the appropriate bandgap (~0.9 - 1.0 eV). This has spurred significant research on GaInNAs active layers which have enabled the fabrication of long-wavelength GaAs-based VCSELs. Such devices make use of the many advantages of GaAs over InP - chief among them being high reflectivity AlAs/GaAs distributed Bragg reflector mirrors. Wang and coworkers first demon-

strated improvements in material quality using antimony as a surfactant during GaInNAs growth. Workers at Furukawa Electric also showed that antimony incorporation could be used to extend the wavelength of their material from 1.20 to 1.26 μm. More recently, Harris and coworkers used the same principle to grow the first GaAs-based quantum wells (QWs) with peak luminescence out to 1.6 μm without serious degradation of material quality. We present a direct comparison of GaInNAs/Ga(N)As (QW/barrier) and GaInNAsSb/GaNAsSb active layers analyzed by photoluminescence (PL), high-resolution X-ray diffraction (HRXRD), and secondary ion mass spectrometry (SIMS). The samples analyzed in this experiment were grown in a modular Varian Gen II molecular beam epitaxy machine with nitrogen supplied by an inductively coupled rf plasma source. Samples were ex-situ annealed by rapid thermal annealing in a nitrogen ambient. Composition was determined by previous growths measured with HRXRD, SIMS, Rutherford backscattering spectrometry (RBS), and nuclear reaction analysis (NRA). The GaInNAs sample used in this study was the best 1.3 μm PL sample produced by this group and contains three 70 Å $Ga_{0.70}In_{0.30}N_{0.016}As_{0.984}$ QWs surrounded by 200 Å GaNAs barriers. The antimony-containing sample was a single 70 Å $Ga_{0.68}In_{0.32}N_{0.012}As_{0.64}Sb_{0.024}$ QW with 200 Å GaNAsSb barriers grown under similar conditions. Under optimal annealing conditions, (760C for 1 min. and 720C for 1 min.) the GaInNAs and GaInNAsSb samples showed PL peaks at 1.310 and 1.326 μm, respectively. The peak luminescence intensity was >40% larger for the GaInNAsSb sample. It has been observed that peak and integrated luminescence scale linearly with the number of QWs for similar GaInNAs(Sb) samples. Thus, the luminescence intensity enhancement was a factor of 4.2. Additionally, the integrated intensity per quantum well was found to be a factor of 8.0 times larger. The full width at half maximum (FWHM) was slightly larger, however, for the antimony sample 59.6 meV, compared to 58.32 meV. This is likely due to non-optimal growth conditions for the antimonide sample and further improvements are expected. Qualitative improvements in ω-2θ (HRXRD) scans are also seen with the introduction of antimony.

9:40 AM

HH5, Effects of MOCVD Growth Conditions on Properties of GaInNAs/GaAs Quantum Wells: Noppadon Nuntawong[1]; Hongjun Cao[1]; *Abdel-Rahman A. El-Emawy*[1]; Marek Osinski[1]; [1]University of New Mexico, Ctr. for High Tech. Matls., 1313 Goddard SE, Albuquerque, NM 87106 USA

Effects of MOCVD growth parameters on structural and optical properties of double-quantum-well structures containing uncoupled GaInNAs/GaAs and InGaAs/GaAs quantum wells have been investigated. By varying growth temperature, growth rate, V/III ratio, and DMHz flow rates; we have achieved a longer-wavelength emission from a GaInNAs well than from an InGaAs well grown in the same structure. GaInNAs/GaAs multiple-quantum-well structures grown under optimum conditions emitted at 1.25 μm. All samples were grown on (100) semi-insulating GaAs substrates in MOCVD reactor using arsine, TMG, TMI and DMHz. A 3000 Å GaAs buffer layer was grown at 680°C, and then the temperature was lowered for the active region growth. Two types of samples were grown in order to assess the effects of possible interaction between nitrogen and indium. First, a DQW structure with InGaAs wells and GaAs barriers was grown to serve as a reference. Then, a combination of InGaAs and GaInNAs quantum wells separated by a wide GaAs spacer was grown. Our goal was to achieve emission from GaInNAs at a wavelength longer than the corresponding InGaAs QW grown under the same conditions, except for the obvious difference in the nitrogen source flow. Figure 1 shows room-temperature photoluminescence (PL) spectra from a set of samples grown under different DMHz flow conditions. These samples were grown at 570°C with 1 Å/s growth rate. The well thickness was 8 nm and the GaAs barrier was 200 nm. Curve (a) shows the PL spectrum from an InGaAs/GaAs double-quantum-well (DQW) sample and is used as a reference. The emission from the InGaAs/GaAs DQW exhibits only one strong peak at 1100 nm. Curve (b) shows the PL emission from two uncoupled QWs, InGaAs/GaAs and GaInNAs/GaAs, grown at the DMHz flow rate of 300 sccm. The PL spectrum from this sample has two peaks - one peak at 1100 nm related to the InGaAs/GaAs well, and another longer-wavelength peak at 1115 nm related to the GaInNAs/GaAs well. Further increase in the nitrogen flow to 600 sccm (curve (c)) produces a red shift in PL, while the GaInNAs-related peak is observed at 1130 nm. The data presented in Figure 1 show strong evidence that nitrogen was indeed incorporated in the QW, but in the same instance the PL intensity decreases with increasing nitrogen content. This may be due to some nitrogen-related defects such as increased group-V vacancies or misplacement of In atoms due to lower surface mobility. Figure 2 shows the PL spectra of samples grown at various temperatures. The samples were grown in a temperature range of 530-570°C. The DMHy flow rate was kept constant at 300 sccm. Within this temperature range, the nitrogen incorporation increases with decreasing temperature. At 570°C, the peak wavelength of GaInNAs/GaAs QW was 1185 nm with a full width at half maximum (FWHM) of 33.27 meV. At 550°C, the peak was 1225 nm with FWHM of 30.617 meV. At 530°C, the peak was 1245 nm with FWHM of 35.233 meV. Outside this range, the PL intensity dropped rapidly. At lower temperatures, the incorporation of nitrogen was limited by the dissociation efficiency of DMHy and surface mobility of In atoms was very low. At higher temperatures, nitrogen incorporation decreased, probably due to decreasing sticking coefficient. Figure 2 also shows the PL spectrum for sample DE1012 that was grown under similar growth conditions as DE1014, except that DMHy was turned off. As can be seen, sample DE1012 has a weak and broad PL spectrum with two peaks at 1165 nm and 1213 nm. This sample shows poor quality material as investigated by x-ray measurements. From the PL spectra of DE1012 and DE1014 it can be concluded that incorporation of nitrogen in InGaAs material not only produces a red shift in the PL, but also reduces the strain between the active region and the GaAs substrate. Therefore, the upper limit of In composition can be increased.

10:00 AM Break

10:20 AM Student

HH6, An Investigation of GaNAs(Sb) for Strain Compensated Active Regions at 1.3 and 1.55 μm: *Homan Bernard Yuen*[1]; Seth Robert Bank[1]; Mark Allen Wistey[1]; Akihiro Moto[2]; James S. Harris[1]; [1]Stanford University, Electl. Engrg., 126X CIS-X, Via Ortega, Stanford, CA 94305 USA; [2]Innovation Core SEI Inc., 3235 Kifer Rd., Ste. 150, Santa Clara, CA 95051 USA

The dilute nitride GaInNAs has been found to optically emit at wavelengths longer than previously thought possible for materials grown coherently on GaAs. Kondow et al. discovered the addition of nitrogen to GaAs decreases both the overall lattice parameter and the bandgap. It is only possible to obtain wavelengths out to 1.2 μm with InGaAs on GaAs before relaxation occurs due to the large lattice mismatch. The addition of nitrogen enabled the development of optoelectronic devices, such as vertical-cavity surface-emitting lasers (VCSELs) and edge emitting lasers at the important telecom wavelength of 1.3 μm. However, attempts to push out to 1.55 μm have not been successful with GaInNAs. Addition of further indium or nitrogen results in severely degraded material quality due to phase segregation, 3-dimensional growth, or relaxation. In an effort to improve material quality, Wang and coworkers discovered that antimony could be used as a surfactant in GaInNAs growth. However, it was discovered that antimony acted as both a surfactant and constituent when used in GaInNAs, forming GaInNAsSb. Until now, devices utilizing GaInNAsSb as the quantum well (QW) material used GaNAsSb as the barrier material. Antimony was used for the barriers because it was also thought it could improve the quality of GaNAs and the QW/barrier interfaces. Although much focus has been placed on the quantum well material GaInNAsSb, there has not been much study of GaNAsSb. In this talk, an analysis of GaNAsSb will be presented. The samples analyzed in these experiments were grown in a modular Varian Gen II molecular beam epitaxy machine with nitrogen supplied by a rf plasma source. Incorporation of nitrogen is linearly dependent upon the inverse of the group-III growth rate. The barrier compositions are thus determined uniquely by the QW growth conditions. Work has shown that GaNAs/GaAs is weakly type I or II, depending on the nitrogen mole fraction. The addition of antimony to semiconductors shifts the band alignment to type II, such as GaAsSb/GaAs. Consequently, it has been suggested that GaNAsSb could be type-II compared to GaAs. An examination of the lattice parameter and strain of GaNAsSb on GaAs also is presented. Under growth conditions needed for QWs emitting at 1.3 and 1.55 μm, GaNAsSb barriers are virtually lattice matched to GaAs, erasing any strain compensation found when using GaNAs barriers.

10:40 AM

HH7, Growth of Metastable GaAsBi Alloy by Molecular Beam Epitaxy: *Masahiro Yoshimoto*[1]; Satoshi Murata[1]; Akiyoshi Chayahara[2]; Junji Saraie[1]; Kunishige Oe[1]; [1]Kyoto Institute of Technology, Dept. Elect. &

Info. Sci., Matsugasaki, Sakyo, Kyoto 606-8585 Japan; [2]AIST Kansai, 1-8-31, Midorigaoka, Ikeda, Osaka 563-8577 Japan

$GaAs_{1-x}Bi_x$ alloy with the GaBi mole fraction of 4.5% has been grown by molecular beam epitaxy (MBE). MBE method was proven to be more suitable for the growth of the metastable alloy than metalorganic vapor phase epitaxy (MOVPE). This is the first successful growth of the $GaAs_{1-x}Bi_x$ alloy by MBE. III-V semiconductor alloys consisting of semiconductor and semimetal components have been proposed to obtain materials with temperature-insensitive bandgaps. In our previous study, the bandgap of $GaAs_{1-x}Bi_x$ grown by MOVPE showed a weak temperature dependence. However, the maximum GaBi mole fraction was limited to 2.6 % in MOVPE. Non-equilibrium processes in MBE are expected to enhance the incorporation of Bi into $GaAs_{1-x}Bi_x$. $GaAs_{1-x}Bi_x$ was grown on (001)-oriented GaAs substrate in MBE with solid sources of Ga, As and Bi. Before growth of $GaAs_{1-x}Bi_x$, 500-nm thick GaAs was grown on the GaAs at a substrate temperature (T_{sub}) of 500°C. $GaAs_{1-x}Bi_x$ with thickness of 300-700 nm was grown on the homoepitaxial GaAs grown layer at T_{sub} between 365 and 395°C. In θ-2θ scan of X-ray diffraction (XRD) measurements, the diffraction peak of the heteroepitaxial layer was observed at a lower value of 2θ than that of (004)-diffraction of GaAs. By increasing Bi flux with constant fluxes of Ga and As at T_{sub} of 395°C, the GaBi mole fraction increased from 0.6 to 1.7% based on results of Rutherford back scattering (RBS) measurements. According to the increase in the GaBi mole fraction, the lattice constant of the epilayer estimated from XRD increased from 0.5660 to 0.5672 nm. Assuming that Vegard's law holds over the entire range of the GaBi mole fraction of $GaAs_{1-x}Bi_x$, the lattice constant of hypothetical zincblende GaBi was calculated to be 0.6225 nm by extrapolating the relation between the GaBi mole fraction and the lattice constant. The GaBi mole fraction increased from 0.6% to 4.5% with decreasing T_{sub} from 395 to 365 °C with constant fluxes of Ga, As and Bi. Desorption of Bi from the growing surface is suppressed at the low T_{sub} of 365 °C, resulting in the high GaBi mole fraction. MBE method is expected to be suitable to obtain materials, such as $In_{1-x}Ga_xAs_{1-y}Bi_y$, with a temperature-insensitive bandgap in the wavelength region of optical fiber communication. In MOVPE, $In_{1-x}Ga_xAs_{1-y}Bi_y$ could not be grown due to insufficient decomposition of metalorganic sources at the growth temperature. Source supply without a decomposition process in MBE is expected to realize $In_{1-x}Ga_xAs_{1-y}Bi_y$ alloy. This alloy will lead up to laser diodes with an emission of temperature-insensitive wavelength, which eliminates the use of massive temperature-control equipment in wavelength-division-multiplexing (WDM) fiber communication systems.

11:00 AM Student

HH8, Infra-Red Properties of Mn Doped InAs and (In,Mn)As Epitaxial Films: *Philip T. Chiu*[1]; Aaron J. Blattner[1]; Bruce W. Wessels[1]; [1]Northwestern University, Matls. Sci. & Engrg., 2220 N. Campus Dr., Cook Hall, Evanston, IL 60208 USA

The optical properties of Mn-doped InAs and (In,Mn)As alloy semiconductor thin films grown by MOVPE on GaAs substrates were measured with fourier transform infra-red (FTIR) spectroscopy. These alloys are potentially of interest for tunable infrared detectors. Alloy films with Mn concentrations of up to 20 percent as determined by energy dispersive x-ray spectroscopy (EDS) were examined. Mn in InAs behaves as a shallow acceptor in the dilute limit. The (In,Mn)As alloy thin films examined were ferromagnetic at room temperature, with Curie temperatures of 330 K. FTIR spectroscopy was used to observe the effect of Mn not only as a p-type dopant, but also as a ferromagnetic ion, on the fundamental absorption characteristics. The absorption spectra were measured at room temperature for both Mn doped InAs and (In,Mn)As, with carrier concentrations ranging from $7x10^{17}$ to $8.6x10^{18}$ cm^{-3}. The band edge absorption was nearly independent of carrier concentration, with all thin films measured having an energy gap of approximately 0.35 eV, comparable to that of bulk InAs. The measured spectral dependence of absorption differed from that of pure InAs in that the band edge absorption was significantly broadened. Furthermore a sharp minimum in the above gap absorption spectra was also observed at 0.58 eV for (In,Mn)As alloy thin films. Since both doped and undoped films exhibited the same anamolous spectral feature, the effect is presumed not the result of any Zeeman splitting of the valence bands due to the presence of ferromagnetic ions. Rather, the above band gap absorption minimum is tentatively attributed to a strain induced splitting of the valence band resulting from the large lattice mismatch between the InMnAs film and GaAs substrate of 7.4%. The mismatch strain causes significant changes in the energy band structure, and hence the optical properties of the heteroepitaxial thin films. The hydrostatic and shear components of strain split the normally degenerate heavy and light hole bands of the valence bands. A splitting of 0.23 eV between the heavy and light hole bands would account for the difference in energy between the energy gap and the above gap minimum.

Index

N

O

P

Q

R

S

T

U

V

W

X

Y

Z