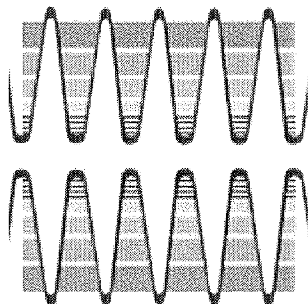

June 23-25, 2004
46TH ELECTRONIC MATERIALS CONFERENCE
Notre Dame University, Notre Dame, Indiana

Intended Audience

The 46th Annual Electronic Materials Conference (EMC) of the EMPMD Electronic Materials Committee of TMS (The Minerals, Metals, & Materials Society) provides a forum for topics of current interest and significance in the areas of preparation and characterization of electronic materials. Individuals actively engaged or interested in electronic materials research and development are encouraged to attend this meeting. Attendees include students, professors, scientists, engineers, researchers, technicians, R&D managers, and product managers.

The conference has become international with approximately 80%national (USA) attendees and 20% international attendees. Each year, over 500 people in the electronic materials industry attend the conference.

The Exhibition

The 2004 EMC will host an exhibition of electronic materials technology and related services. Exhibitors are invited to display equipment, instrumentation, products, software, publications and services relating to electronic materials science, industry and research.

The Exhibition will provide an ideal opportunity for EMC attendees to meet suppliers of related products and technology, and for attendees to acquaint themselves with new technologies and products. Technical session participants are encouraged to visit the exhibition. The exhibition features:

- Show hours scheduled to complement the technical program schedule
- Conference coffee break conducted in the exhibition area.
- A Welcoming cocktail reception held in the exhibit area on the opening day of the meeting.
- Booth area conveniently located near the technical session rooms.

EXHIBIT DATES AND HOURS

Wednesday, June 23, 2004.............9:20 am-4:00 pm and 6:00 pm-8:00 pm
Thursday, June 24, 2004 ....10:00 am-4:00 pm

EXHIBITOR PRODUCTS AND SERVICES AT A GLANCE

- Advanced thin-film characterization
- Chemical Vapor Deposition (CVD)
- Compound semiconductor materials
- Failure analysis
- GaAs and InP based epitaxial wafers;

- High performance purification
- High purity metalorganics
- III-V materials
- Materials characterization
    - MOCVD
    - Optoelectronics
    - Sapphire substrates
- Scanning probe &electron microscopes
- Silicon heterostructures
- Ultra high purity (UHP)metals,
- gas &chemical delivery systems
- Wafer processing equipment
- Wide bandgap semiconductors

Social Events

WELCOMING RECEPTION

All attendees are invited to attend a Welcoming Reception on Wednesday, June 23 from 6:00 pm-8:00 pm at the University of Notre Dame in De Bartolo Hall.

GREAT HALL OF THE CENTURY CENTER

On Thursday evening, June 24, conference attendees and their guests will have the opportunity to enjoy an evening by the St. Joseph River. Enjoy Century Center's location on a riverfront park in downtown South Bend. Its unique feature is the three-story Great Hall window. Century Center includes an art museum. The College Football Hall of Fame, one of the world's major sports shrines, connects to the Center by a dramatic concourse filled with the spirit of the sport. A catered dinner will take place in the Great Hall. After dinner, participants have the option of visiting the neighboring College Football Hall of Fame and/or the South Bend Regional Museum of Art.

INFORMAL COFFEE BREAKS

During the intermission of morning and afternoon sessions (at approximately 10:00 am-10:40 am and 3:00 pm-3:40 pm) coffee, tea, and sodas will be served in De Bartolo Hall, the same location as the exhibits.

Related TMS Publications

TMS BOOKS

Proceedings are available from additional TMS conferences related to electronic materials, including those listed below. For more details on these titles, including on-line tables of contents and ordering information, visit the TMS Document Center at:
http://doc.tms.org.

ADVANCED MATERIALS FOR
ENERGY CONVERSION II
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CALPHAD and Alloy Thermodynamics
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SURFACES AND INTERFACES IN NANOSTRUCTURED MATERIALS AND TRENDS IN LIGA, MINIATURIZATION, AND NANOSCALE MATERIALS, 5th MPMD Global Innovations Symposium
Sharmila M. Mukhopadhyay, John Smugeresky, Sudipta Seal, Narendra B. Dahotre, and Arvind Agarwal, editors
Approx.720 pp.,illus.,softcover
Order No.04-5662 *Weight 4 lbs
M $118 S $93 L $168

SPECIAL ISSUES OF THE *JOURNAL OF ELECTRONIC MATERIALS*
Each year, the *Journal of Electronic Materials* (*JEM*) publishes several special issues that comprise conference and symposium proceedings and related papers. Limited numbers of these archival-quality issues are available for individual purchase. Issues
from prior volume years are also available.

PLANNED SPECIAL ISSUES AND SPECIAL ISSUES FROM 2004

III-Nitrides and Related Materials (May)
Order No.JEM-0405
2003 U.S.Workshop on the Physics and Chemistry of II-VI Materials (July)
Order No.JEM-0407
Advanced Thin Films (September)
Order No.JEM-0409
Phase Stability,Phase Transformations, and Reactive Phase Formation in Electronic Materials III (October)
Order No.JEM-0410

SPECIAL ISSUES FROM 2003
III-V Nitrides and Silicon Carbide (May)
Order No.JEM-0305
2002 U.S.Workshop on the Physics and Chemistry of II-VI Materials (July)
Order No.JEM-0307
3rd International Conference on Alternative Substrate Technology (August)
Order No.JEM-0308
Materials and Processes for Submicron Technologies III (October)
Order No.JEM-0310
Phase Stability, Phase Transformations, and Reactive Chemistry of II-VI Materials (November)
Order No.JEM-0311
Lead-Free Solders and Processing Issues Relevant to Microelectronics (December)
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ADVANCE REGISTRATION FORM

46th TMS Electronic Materials Conference (EMC)
June 23–25, 2004 • University of Notre Dame, Notre Dame, Indiana

WEB Take advantage of the convenience of on-line pre-registration via the TMS website: http://www.tms.org
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FAX Fax this form to TMS Meeting Services
724-776-3770
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MAIL **Return this form with payment to** **TMS** Meeting Services 184 Thorn Hill Road Warrendale, PA 15086

Advance Registration Deadline: June 2, 2004

Payment must accompany form. Forms received after June 2nd will be processed at the next higher fee.

Please print or type

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GUESTS DO NOT RECEIVE ADMISSION TO TECHNICAL SESSIONS OR THURSDAY DINNER

Please check the appropriate category and enter the totals where indicated.

Registration Fees (includes a one-year subscription to *Journal of Electronic Materials*)		**Fees to June 2, 2004**	**Fees after June 2, 2004**
❍ Full Conference Member		$387	$462
❍ Full Conference USA Nonmember		$563	$638
❍ Full Conference NON-USA Nonmember		$584	$659
❍ One Day Member	Day Attending: ________	$332	$387
❍ One Day USA Nonmember	Day Attending: ________	$508	$563
❍ One Day NON-USA Nonmember	Day Attending: ________	$529	$584
❍ Air Mail Delivery of *Journal of Electronic Materials* (Outside United States of America)		$20	$20

Registration Fees (without a one year subscription to *Journal of Electronic Materials*)		**Fees to June 2, 2004**	**Fees after June 2, 2004**
❍ Full Conference		$355	$430
❍ One Day	Day Attending: ________	$300	$355
❍ Student (Copy of student school identification card must accompany form.)		$150	$200

Social Function Tickets (Thursday Dinner Event included in full conference and student registration fees.)

❍ Adult One Day Attendee or Guest .... Number:________ @ $60/ea. =________

❍ Child (12 years and younger) .... Number:________ @ $25/ea. =________

❍ Check if you require transportation to the Thursday Dinner Event. .... Number:________

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Payment should be made in US dollars drawn on a US bank.

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REFUND POLICY: Written requests must arrive at TMS no later than June 2, 2004. No refunds will be issued after June 2, 2004. A $50 processing fee will be charged for all cancellations.

2004 CAMPUS ACCOMMODATIONS AND MEAL PLAN REQUEST FORM

EMC University of Notre Dame
Center for Continuing Education

Deadline: May 19, 2004

Send this form to:
Center for Continuing Education
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115 McKenna Hall
Notre Dame, IN 46556

Questions?
Call (574) 631-6691
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Options:

☐ **Plan C $330 (for those attending both DRC and EMC – includes dinner on arrival day)** __________
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2004 Electronics Materials Conference Grid

REGISTRATION

3:00PM–5:00PM, Tuesday, June 22, 2004, McKenna Hall
7:30AM–5:00PM, Wednesday, June 23, 2004, McKenna Hall
7:30AM–4:00PM, Thursday, June 24, 2004, McKenna Hall
7:30AM–10:00AM, Friday, June 25, 2004, McKenna Hall

EXHIBITS

9:20AM–4:00PM & 600PM–8:00PM, Wednesday, June 23, 2004, DeBartolo Hall
10:00AM–4:00PM, Thursday, June 24, 2004, DeBartolo Hall

Room	WEDNESDAY, JUNE 23RD AM	WEDNESDAY, JUNE 23RD PM	THURSDAY, JUNE 24TH AM	THURSDAY, JUNE 24TH PM	FRIDAY, JUNE 25TH AM
101	EMC Plenary Lecture/Student Awards Joint DRC/EMC Invited Session: Molecular Electronics & Carbon Nanotubes	Joint DRC/EMC Session: Materials and Circuits for Flexible Electronics	Session V: Surface Engineering and Thin-Film Transistor Performance	Session CC: Transport in Organic Semiconductor Device	Session JJ: Contacts to Nanotubes, Nanowires, and Organic Films
102	Session A: High-K Dielectric Stacks	Session H: High-K Dielectrics and Metal Gates	Session Q: High-K Oxides	Session X: Spin Injection, Spin Transport, and Magnetic Anisotropy	Session EE: Epitaxy for Devices
126	Session F: Materials and Structures for Chemical and Biological Sensors				
129	Session G: Nanocharacterization I (Advanced Electron Microscopy)	Session P: Nanocharacterization I (Including Spintronic Materials)	Session W: Mismatched Materials: Metamorphic and Growth on Templates	Session DD: Narrow Bandgap Devices and Materials	
136	Session C: Materials Integration: Wafer Bonding and Alternative Substrates	Session K: Quantum Dots in III-V and Group IV Compounds	Session S: Physics and Devices in Low Dimensional Structures	Session Z: Semiconductor Nanostrucures: Materials to Devices	Session GG: Semiconductors: Processing and Oxidation
140	Session D: SiC: Growth and Device Processing	Session L: Contacts to Silicon Carbide Session M: Non-Destructive Testing and In-Situ Monitoring-Control	Session T: Molecular Electronics I	Session AA: Dilute Nitrides	Session HH: Molecular Electronics I
141	Session B: Magnetic Semiconductors: Growth and Characterization	Session I: Point Defects, Extended Defects and Doping in Wide Band Gap Materials Session J: Si-Based Heterojunctions and Strained Si: Growth, Characterization and Applications	Session R: Nanotubes and Nanowires I	Session Y: Nanotubes and Nanowires II	Session FF: Defects in SiC
155	Session E: Nitride HEMTs: Transport and Devices	Session N: Nitride HEMTs: RF Dispersion and Passivation Session O: Wide Bandgap Light Emitting Diodes	Session U: III-Nitride Growth	Session BB: Contacts to Wide Bandgap Semiconductors	Session II: Characterization of Nitride Semiconductors

2004 EMC At-A-Glance

Wednesday Morning, June 23, 2004

8:20 AM	EMC PLENARY LECTURE/STUDENT AWARDS
Room:	101
Plenary Speaker:	Federico Capasso Harvard University, Cambridge, MA 02138 USA
Topic:	"Quantum Cascade Lasers: From Bandstructure Engineering to Commercialization"
Break:	9:20 AM–10:00 AM

Time	**Jt. DRC/EMC Invited Session: Molecular Electronics and Carbon Nanotubes** **Room: 101**	Time	**Session A: High-K Dielectric Stacks** **Room: 102**	Time	**Session B: Magnetic Semiconductors: Growth and Characterization** **Room: 141**
10:00 AM	(Invited), Characterization of Silicon-Based Molecular Resonant Tunneling Diodes with Scanning Tunneling Microscopy ……………….…….M. C. Hersam	10:00 AM	A1, (Invited), New Metal Gate/High-K Dielectric Stacks for Continual Electrical T_{ox} Scaling and High-Performance CMOS Applications ……………..……..Robert Chau	10:00 AM	B1, Point Contact Andreev Reflection Spin Polarization Measurements in InMnSb Epilayers ……………………B. Nadgorny
				10:20 AM	B2, (Student), Structural and Magnetic Properties of Cr-Doped InN Films Grown by Plasma-Assisted MBE ……………..……..Rekha Rajaram
10:40 AM	(Invited), IR Emission from Schottky Barrier Carbon Nanotube FETs ……………..…………R. Martel	10:40 AM	A2, (Student), Electron Spin Resonance Study of Atomic Layer Deposited HfO_2 on (111) Silicon …………………. J. P. Campbell	10:40 AM	B3, (Student), Single Crystals of $Zn_{1-x}Mn_xO$ and $Zn_{1-x}Co_xO$ for Spintronic Applications …………….....Matthew H. Kane
		11:00 AM	A3, Origin of a Residual Charge and Effects of Nitridation of High-k Oxides in MOSFETS: Density Functional Studies …………………Jacob Gavartin	11:00 AM	B4, (Student), Local Structure about Mn Ions in III-Mn-V Ferromagnetic Semiconductor Alloys ………………..Aaron M. Stuckey
11:20 AM	(Invited), Measurement of Electron Transport and Mechanical Properties of Single Molecules ……………………Nongjian Tao	11:20 AM	A4, (Student), Negative Bias-Temperature Instabilities in Metal-Oxide-Silicon Devices with SiO2 and SiOxNy/HfO2 Gate Dielectrics …………………….Xing J. Zhou	11:20 AM	B5, Strong Ferromagnetism in GaMnN Alloys Grown by MBE ……....Joseph E. Van Nostrand
		11:40 AM	A5, Si and SiGe Vertical MOSFETs with CVD-HfO_2 Gate Dielectric …....Sankaran K. Jayanarayanan	11:40 AM	B6, Late News

2004 EMC At-A-Glance

Wednesday Morning, June 23, 2004

Session C: Materials Integration: Wafer Bonding and Alternative Substrates Room: 136		Session D: SiC Growth and Device Processing Room: 140		Session E: Nitride HEMTs: Transport and Devices Room: 155	
10:00 AM	C1, UHV-Wafer Bonding of Heterostructure Semiconductor Materials Using Low Energy Hydrogen Ion Beam Surface Cleaning ………...………Razek Nasser	10:00 AM	D1, Drift Free, 10 kV, 20A, 4H-SiC PiN Diodes ……………..Mrinal Kanti Das	10:00 AM	E1, A Study of AlGaN/GaN Heterostructures on Silicon ………………………..S. Elhamri
10:20 AM	C2, (Student), Changes in Interfacial Bonding Energies in the Chemical Activation of GaAs Surfaces …………...…………Ning Liu	10:20 AM	D2, (Student), Influence of Low Field Mobility Related Issues on SiC MESFET Performance ……………….Ho-Young Cha	10:20 AM	E2, Quantum Transport in a Tunable AlGaN/GaN Two-Dimensional Electron Gas …………Michael James Manfra
10:40 AM	C3, (Student), InGaAs Quantum Wells Grown by MOCVD on InP/GaAs Composite Substrates …..……Sumiko Lynn Hayashi	10:40 AM	D3, 2.5 kV, 17 mOhms-cm^2 4H-SiC JFETs ………………Sei-Hyung Ryu	10:40 AM	E3, Use of Modulation Doped Superlattice AlGaN Barrier in GaN/AlGaN HFETs ……………….Uttiya Chowdhury
11:00 AM	C4, Combined Use of Neon Ion Implantation and Hydrogen Plasma Implantation in Ion-Cutting ……………………Peng Chen	11:00 AM	D4, (Student), Characteristics of Trench-Refilled 4H-SiC P-N Junction Diodes Fabricated by Selective Epitaxial Growth …………………….Canhua Li	11:00 AM	E4, (Student), SiC Substrate Inclusions and Their Impact on AlGaN/GaN HEMT Performance ………………….Benjamin Poust
11:20 AM	C5, (Student), High Resolution X-Ray Diffraction Characterization of the Depth Dependent Structural Transformations in HE-Implanted PZN-PT …..………Natee Tangtrakarn	11:20 AM	D5, Modifications of 4H-SiC and 6H-SiC(0001) Surfaces by Atomic Hydrogen and Nitrogen for the Epitaxial Growth of GaN ………………..Maria Losurdo	11:20 AM	E5, Suppression of Gate Current Leakage in AlGaN/GaN MIS-HFETs with Ultrathin Al_2O_3/Si_3N_4 Bilayer Insulator ……………………….C. X. Wang
11:40 AM	C6, Late News	11:40 AM	D6, Development of High Growth Rate (20µm/h) SiC Epitaxy in a Horizontal Hot-Wall CVD Reactor ……………………..Jie Zhang	11:40 AM	E6, Late News

2004 EMC At-A-Glance

Wednesday Morning, June 23, 2004

Wednesday Afternoon Begins…

Session F: Materials and Structures for Chemical and Biological Sensors — Room: 126		Session G: Nanocharacterization I (Advanced Electron Microscopy) — Room: 129		Joint DRC/EMC Session: Materials and Circuits for Flexible Electronics — Room: 101	
10:00 AM	F1, Fabrication of a Solid-State Single Nanopore for DNA Characterization ……………………..Hung Chang	10:00 AM	G1, (Invited), Nanoscale Control of Epitaxial Quantum Dot Assembly in Ge(Si)/Si Heteroepitaxy ……………………...Robert Hull	1:30 PM	(Invited), Nanowire Thin-Films: A New Electronic Materials Technology for Thin-Film Devices and High-Performance Large-Area Electronics ……………...Stephan Empedocles
10:20 AM	F2, Chemical Sensing Properties of Modified Silicon Surfaces ……………………Brian J. Eves				
10:40 AM	F3, Applications of Dielectrophoretic "Tweezers" in Determining the Biological Receptor-Ligand Interaction Forces and Selectively Removing Different Species in Biochips …………………………Haibo Li	10:40 AM	G2, (Invited), Direct Observation of Charge Transfer at a MgO(111) Surface ………………Laurence Marks	2:10 PM	(Invited), Printing of Polymer Field-Effect Transistors ………………………H. Sirringhaus
				2:50 PM	Digital Lithography for Thin-film Transistor Fabrication ……………………William S. Wong
11:00 AM	F4, (Student), Self-Assembled Protein Nanopatterns …………………………..Bo Gao			3:10 PM	Break
11:20 AM	F5, (Student), Electrical Detection of DNA Hybridization Using Nano-Gap Gold Break-Junctions …………………Samir M. Iqbal	11:20 AM	G3, (Invited), Nanoscale Characterization of Epitaxial Cu_2O Films Made by Electrodeposition ……………………..Frank Ernst	3:30 PM	(Invited), Pentacene Based Transponder Tags with Multiple-Bit Circuitry …………………………Paul Baude
11:40 AM	F6, (Student), High Temperature Hydrogen Sensors on GaN and AlGaN/GaN Heterostructures with Different Catalytic Metals …………………...Junghui Song			4:10 PM	Hole Mobility in Organic Single Crystal Field Effect Transistors ………………….David J. Gundlach
				4:30 PM	An 8V Organic Complementary Logic Process for Flexible Polymeric Substrates ………………………...Hagen Klauk

2004 EMC At-A-Glance

Wednesday Afternoon, June 23, 2004

Session H: High-K Dielectrics and Metal Gates Room: 102		Session I: Point Defects, Extended Defects, and Doping in Wide Band Gap Materials Room: 141		Session J: Si-Based Heterojunctions and Strained Si: Growth, Characterization and Applications Room: 141	
1:30 PM	H1, (Invited), Dual Metal Gate CMOS Using CVD Metal Gate Electrodes ……………...Vijay Narayanan	1:30 PM	I1, (Student), Investigation of Carbon-Related Defect States in MBE-Grown GaN Co-Doped with Carbon and Silicon ……….Andrew M. Armstrong	1:30 PM	
		1:50 PM	I2, (Student), Beryllium Doped GaN Grown by RF-Plasma Molecular Beam Epitaxy ………………Kyoungnae Lee	1:50 PM	
2:10 PM	H2, (Student), Comparative Study of Trapping Characteristics of HfSiON Dielectric in nMOSFETs with Poly-Si or TiN as Gate Electrode ……………………..D. C. Guo	2:10 PM	I3, Remote Hydrogen Plasma Doping of Single Crystal ZnO ……….Yuri M. Strzhemechny	2:10 PM	
2:30 PM	H3, (Student), Characterization of Ultra-Thin Hf-Based Alternative Dielectric Layers for Si CMOS by Z-Contrast Imaging and Electron Energy-Loss Spectroscopy in STEM ……..Melody Pacifico Agustin	2:30 PM	I4, Microstructure and Nucleation Behavior of Heteroepitaxial GaN Films Grown on Mesa-Patterned 4H-SiC Substrates ………………Nabil D. Bassim	2:30 PM	
2:50 PM	H4, (Student), Nucleation Density Study of MOCVD Grown Ru and RuO_2 Films for Gate Electrode Applications …………..Filippos Papadatos	2:50 PM	I5, (Student), Drift Dominated AlGaAs Solar Cells for High Temperature Application ………………….Yanning Sun	2:50 PM	
3:10 PM	Break	3:10 PM	Break	3:10 PM	
3:30 PM	H5, Electrical Characteristics of Single Crystal Silicon and Germanium Layers Grown on $(La_xY_{1-x})_2O_3$ / Si (111) ………………..….E. J. Preisler	3:30 PM		3:30 PM	J1, High Electron Mobility Transistor Structures on Sapphire Substrates Using CMOS Compatible Processing Techniques …………………..Carl H. Mueller
3:50 PM	H6, (Student), Atomic-Scale Structure of Alkaline-Earth Metal on Si(001) Surface Reconstructions …………..Duane M. Goodner	3:50 PM		3:50 PM	J2, (Student), Temperature Sensitivity of DC Operation of Sub-Micron Strained-Si MOSFETs ………………….Valerio Gaspari
4:10 PM	H7, (Student), Optical Properties of Prospective High-k Dielectrics …………………..E. Cicerrella	4:10 PM		4:10 PM	J3, (Student), MOS Capacitors on Epitaxial $Ge/Si_{1-x}Ge_x$ with High-k Dielectrics ………………….Sachin V. Joshi
4:30 PM	H8, Pr-Silicate Ultrathin Films for High-k Gate Dielectrics Prepared by Metal-Organic Chemical Vapor Deposition …………Yoshishige Tsuchiya	4:30 PM		4:30 PM	J4, (Student), Uniaxially-Tensile Strained Ultra-Thin Silicon-On-Insulator with Up to 1.0% Strain ……………………R. L. Peterson

2004 EMC At-A-Glance

Wednesday Afternoon, June 23, 2004

Session K: Quantum Dots in III-V and Group IV Compounds Room: 136		Session L: Contacts to Silicon Carbide Room: 140		Session M: Non-Destructive Testing and In-Situ Monitoring-Control Room: 140	
1:30 PM	K1, Thermal Processing of InAs and InGaAs Quantum Dots for Device Integration …………………Jeff Cederberg	1:30 PM	L1, (Student), Electronic Defect States at Annealed Metal/4H-SiC Interfaces ……………Sergey Tumakha	1:30 PM	
1:50 PM	K2, Thermal Effect on the Luminescence Properties of InP Quantum Dots Coupled with an InGaP Quantum Well Through a Thin InAlGaP Barrier ……………………X. B. Zhang	1:50 PM	L2, (Student), Schottky Diodes on n-Type 4H-SiC Grown by Sublimation Epitaxy and Chemical Vapor Deposition: The Effect of Deep Level Defects ………………Daniel J. Ewing	1:50 PM	
2:10 PM	K3, InAs and InGaAs Quantum Dot Growth by MOCVD ………………Theodore Chung	2:10 PM	L3, (Student), Mechanism of Ohmic Behavior of Al/Ti Contacts to P-Type 4H-SiC After Annealing ……………..Brian J. Johnson	2:10 PM	
2:30 PM	K4, (Student), The Effect of Two-Temperature Capping on Germanium/Silicon Quantum Dots and 3D Tomographic Analysis of Superlattices So Composed ………Thomas E. Vandervelde	2:30 PM	L4, (Student), In-Situ Characterization of Ohmic Contacts to N-Type SiC Under High Temperature and Current ……………..David DeAngelis	2:30 PM	
2:50 PM	K5, (Student), Photo-luminescence Study of Ge/Si Quantum Dots Grown with Single and Double Si Caps …………………………Kai Sun	2:50 PM	L5, (Student), Ta-Ru-N Diffusion Barriers for High-Temperature Metallizations to SiC ………………...C. M. Eichfeld	2:50 PM	
3:10 PM		3:10 PM	Break	3:10 PM	
3:30 PM		3:30 PM		3:30 PM	M1, (Student), Interpretation of Prism-Coupled Optical Reflectivity Measurements from He-Implanted Single Crystal PZN-PT Waveguides ………………………Aijie Chen
3:50 PM		3:50 PM		3:50 PM	M2, (Student), Investigation of Longitudinal Optical Phonon Plasmon Coupled Modes in SiC Epitaxial Film Using FTIR ………Swapna Geetha Sunkari
4:10 PM		4:10 PM		4:10 PM	M3, Spectroscopic Ellipsometry Analysis of the Critical Point Structure of InAs/GaSb Strain-Layer Superlattices ………………………K. G. Eyink
4:30 PM		4:30 PM		4:30 PM	M4, A Fast, Direct and Fully Automated Measurement of Layer Relaxation Using X-Ray Diffraction ……………...Paul Anthony Ryan

2004 EMC At-A-Glance

Wednesday Afternoon, June 23, 2004

Session N: Nitride HEMTs: RF Dispersion and Passivation Room: 155		Session O: Wide Bandgap Light Emitting Diodes Room: 155		Session P: Nanocharacterization II (Including Spintronic Materials) Room: 129	
1:30 PM	N1, Characterization of Trapping Centers in the Structure of AlGaN/GaN HEMTs ………………..Oleg Mitrofanov	1:30 PM		1:30 PM	P1, (Student), Spatially Resolved Electroluminescence from Operating Organic Light-Emitting Diodes Using Conductive Atomic Force Microscopy ……………...Liam S.C. Pingree
1:50 PM	N2, (Student), Reduction of Current Collapse in an Un-Passivated AlGaN-GaN Double-Channel HEMT …………………Rongming Chu	1:50 PM		1:50 PM	P2, (Student), Experimental Study of Masking Scheme Effects on the Nanoscale Sidewall Roughness of Deep Etched InP/InGaAsP Heterostructures for Optical Waveguides …………………….Weifeng Zhao
2:10 PM	N3, (Student), Effect of Different SiN_x Passivation and Their Strain on the Reliability of GaN-Based HEMT Structures …………………..Zhihong Feng	2:10 PM		2:10 PM	P3, (Student), Multi-Step Feedback Controlled Lithography: A Processing Technique for Fabricating Atomically Registered Organosilicon Heterostructures Using Room Temperature Ultra-High Vacuum Scanning Tunneling Microscopy ……………………..……Rajiv Basu
2:30 PM	N4, Passivation of GaN and AlGaN Using Ex-Situ UV-Ozone and MBE Grown Oxides…………Brent P. Gila	2:30 PM		2:30 PM	P4, Correlating Atomic-Scale Materials Morphology with Optical Properties of Mid-IR W-Laser Structures …………..……..Georo I. Boishin
2:50 PM	N5, (Student), Successful Passivation of GaN/AlGaN HFET by Use of Spin-Deposited Polyimide ……………...Uttiya Chowdhury	2:50 PM		2:50 PM	P5, Late News
3:10 PM	Break	3:10 PM		3:10 PM	Break
3:30 PM		3:30 PM	O1, (Student), Enhancement of Blue-Light Extraction Efficiency by Surface Texturing …………….Shao-Hua Huang	3:30 PM	P6, (Student), Characterization and Spintronic Applications of ErAs Interlayers in Ferromagnetic Metal/GaAs Heterostructures ……………………..B. D. Schultz
3:50 PM		3:50 PM	O2, Improving the Wavelength-Power Performance in Green GaInN/GaN Light Emitting Diodes ………………Christian Wetzel	3:50 PM	P7, Advanced Microstructure Characterization of Epitaxial Semimetallic ErAs Particles in an $In_{0.53}Ga_{0.47}As$ Matrix …………………Dmitri O. Klenov
4:10 PM		4:10 PM	O3, Electrical and Optical Properties of AlGaInN Based Deep Ultraviolet Light Emitting Diodes Grown on (0001) Sapphire …………...Sergey A. Nikishin	4:10 PM	P8, (Student), Reaction Kinetics, Thermodynamics, and Growth Characteristics of Ultra-Thin Mn Films on GaAs(001) ………………………..J. L. Hilton
4:30 PM		4:30 PM	O4, High Performance AlInGaN Ultraviolet Light-Emitting Diode at 340 nm …………………….S.-R. Jeon	4:30 PM	P9, (Student), Nanometer-Scale Studies of Point Defect Distributions in GaMnAs Films …………………….J. N. Gleason
4:50 PM		4:50 PM	O5, Late News	4:50 PM	P10, (Student), Mn-Doped InAs Self-Organized Quantum Dots with Curie Temperatures Above 300 K ………………………….M. Holub

2004 EMC At-A-Glance

Thursday Morning, June 24, 2004

	Session Q: High-K Oxides Room: 102		Session R: Nanotubes and Nanowires I Room: 141		Session S: Physics and Devices in Low Dimensional Structures Room: 136
8:20 AM	Q1, (Student), Novel Ultra-Thin $TiAlO_x$ Alloy Oxide for New Generation of Gate Dielectric …………………………Wei Fan	8:20 AM	R1, Growth of InMnAs Nanowires for Low-Dimensional Spintronic Applications …………….Lincoln J. Lauhon	8:20 AM	Invited S1, Polarization Measurements of a Single Charge-Tunable Quantum Dot ………………………..Eric Stinaff
8:40 AM	Q2, (Student), Room Temperature Fabrication of Al_2O_3/ TiO_2/Al_2O_3 Nanolaminates for High-k Gate Dielectrics Structure ……………Wei Fan	8:40 AM	R2, Effects of Surface Oxide Properties on the Electrical Characteristics of Ge Nanowires …………… Ying-Lan Chang		
9:00 AM	Q3, Relative Stability and Electronic Properties of Zirconium and Hafnium Nitrides and Oxynitrides. First Principles DFT Study …………………..Anatoli Korkin	9:00 AM	R3, (Student), MOCVD Growth and Characterization of GaN Nanowires ………………………….Jie Su	9:00 AM	S2, (Student), Spatial Ordering of InAs Quantum Dots in a Microdisk Cavity to Achieve Large Spontaneous Emission Enhancement……Zhigang Xie
9:20 AM	Q4, (Student), High Deposition Rate Atomic Layer Deposition Process …………………………..Gi Kim	9:20 AM	R4, (Student), Effect of Growth Conditions on the Composition and Structure of SiGe Alloy and SiGe/Si Heterostructure Nanowires ………………Kok-Keong Lew	9:20 AM	S3, Multicolor Quantum Dot Infrared Photodetectors (QDIPs) ………………...Seongsin M. Kim
9:40 AM	Q5, Late News	9:40 AM	R5, (Student), Four-Point Resistivity and Gate-Dependent Conductance of p- and n-Type Silicon Nanowires ………………..Yanfeng Wang	9:40 AM	S4, Characteristics of Low Threshold Quantum Dot Lasers Operating at 1.31µm and a Study of Their Carrier Recombination Processes …………Kristian Michael Groom
10:00 AM	Break	10:00 AM	Break	10:00 AM	Break
10:20 AM	Q6, Characteristics of WN_x and ZrN_x as Gate Electrodes: The Effect of Nitrogen Concentration ………………Pei-Chuen Jiang	10:20 AM	R6, Properties of Gallium Nitride Particles Prepared by Ammonolysis from Different Starting Materials ……………..Birgit Schwenzer	10:20 AM	S5, Carrier Recombination Lifetime in Compressively Strained InGaAs Quantum Well Lasers Grown on GaAs Substrates ………………….Wataru Susaki
10:40 AM	Q7, (Student), The Study of Electrical Characteristics of Different HfO_2-Al_2O_3 Stack Layer Grown by Atomic Layer Deposition ………………..Yong-Seok Kim	10:40 AM	R7, (Student), Growth Control of Carbon Nanotube by Applied Electric Field ……………Masatoshi Maeda	10:40 AM	S6, Optimizing the Growth of 1300 nm InAs/GaAs Quantum Dots with InGaAs and InAlAs Layers: Achievement of High-Performance Lasers….H. Y. Liu
11:00 AM	Q8, Nanoscale Characterizations of Ferroelectric BT-Based Films for High-Density FeRAMs ………………………B. L. Yang	11:00 AM	R8, (Student), Growth of Arrays of mm Long, Straight Single-Walled Carbon Nanotubes ……………………….Zhen Yu	11:00 AM	S7, (Student), Sub-Picosecond Photocarrier-Lifetimes at 1.55 µm in GaSb/ErSb Nano-Particle Superlattices ……………..Micah Paul Hanson
11:20 AM	Q9, (Student), Characterization of Cerium Oxide (CeO_2) and Hafnium Oxide (HfO_2) Thin Films on Si (100) as Alternative High-k Gate Oxide Deposited by Pulsed Laser Ablation ………..………….K. Karakaya	11:20 AM	R9, Growth and Characterization of Single-Walled Carbon Nanotubes by Microwave Plasma-Enhanced Chemical Vapor Deposition ………Matthew Maschmann	11:20 AM	S8, (Student), GaAs BDD Quantum Node Switches Fabricated on Selectively MBE Grown Quantum Wire Networks ………………..Takahiro Tamura
11:40 AM		11:40 AM	R10, (Cancelled), Synthesis, Electron Microscopy and Applications of Inorganic Nanotubes…..Maja Remskar	11:40 AM	S9, Growth of PbTe-Based Superlattice Structures for High-Temperature Thermoelectric Applications……….Chris Caylor

2004 EMC At-A-Glance

Thursday Morning, June 24, 2004

	Session T: Molecular Electronics I Room: 140		Session U: III-Nitride Growth Room: 155		Session V: Surface Engineering and Thin-Film Transistor Performance Room: 101
8:20 AM	T1, (Invited), Abstract not available	8:20 AM	U1, (Student), The Compositional Dependence of Phase Separation in InGaN Alloys ……………………Manu Rao	8:20 AM	V1, (Invited), Pentacene Thin Film Transistors and Integrated Circuits: Performance, Stability, and Operating Voltage ……………………..Hagen Klauk
		8:40 AM	U2, Crystal Quality of InN Thin Films Grown on ZnO Substrate by RF-MBE ………………..Satoru Ohuchi		
9:00 AM	T2, (Student), Metal-Molecule-Semiconductor Heterostructure Devices on GaAs and Si ………………...Saurabh Lodha	9:00 AM	U3, (Student), Microstructure and Enhanced Morphology of Planar Nonpolar m-Plane GaN Grown by Hydride Vapor Phase Epitaxy ………………Benjamin Allen	9:00 AM	V2, (Student), Pentacene OTFT with Parylene Active Layer Patterning and Passivation ……………………...Lisong Zhou
9:20 AM	T3, (Student), Hybrid-Basis Modeling of Transport Through Silicon-Based Molecular Devices ………………Gengchiau Liang	9:20 AM	U4, Fabrication of GaN Quantum Dots on AlGaN Template by Liquid Droplet Epitaxy …………Maria Gherasimova	9:20 AM	V3, Gate Dielectric Surface Modification for Controlling the Threshold Voltage and Sub-threshold Characteristics of OTFTs ………………David J. Gundlach
9:40 AM	T4, Electrical Properties of Organic/Silicon Junctions …………...Gregory P. Lopinski	9:40 AM	U5, (Student), Analysis of GaN on Highly-Compliant Nanoscale Silicon Pillar Arrays ……………………..Xinyu Sun	9:40 AM	V4, Organic Field-Effect Transistors Prepared by Ink-Jet-Printing and Spin-Coating from Different Solutions of Poly-3-Octylthiophene ………………..Matthias Ploetner
10:00 AM	Break	10:00 AM	Break	10:00 AM	Break
10:20 AM	T5, (Student), A Self-Consistent Transport Model for Molecular Conductors with Few Applications to Real Systems …………………Ferdows Zahid	10:20 AM	U6, Growth and Characterization of Single Crystal GaN by the Ammonothermal Method …………Michael J. Callahan	10:20 AM	V5, (Student), Low Temperature a-Si:H TFT on Polymer Substrates with Improved Stability ……………………...Lisong Zhou
10:40 AM	T6, (Student), Inelastic Electron Tunneling Spectro-scopy of Self-Assembled Alkanedithiol Monolayers ………………..Wenyong Wang	10:40 AM	U7, (Student), Bulk GaN Growth by Sublimation …………………Huaqiang Wu	10:40 AM	V6, (Student), Improved Solution-Deposited OTFT Performance by Dielectrics and Electrode Surface Treatments ………………..Chung-Chen Kuo
11:00 AM	T7, (Student), In-Situ Analysis of In-Wire Molecular Junctions Using Inelastic Tunneling Spectroscopy ……………...Marco A. Cabassi	11:00 AM	U8, Characterization of AlInGaN Based Heterostruc-tures Grown by Migration Enhanced Metalorganic Chemical Vapor Deposition ………………..Qhalid Fareed	11:00 AM	V7, Control of Transport by Self-Assembled-Monolayers in Organic Field-Effect Transistors …………..Shin-ichiro Kobayashi
11:20 AM	T8, (Cancelled), Charge Transport and Scaling in Molecular Wires ……..Amy Szuchmacher Blum	11:20 AM	U9, Using Optical Reflec-tance to Quantify GaN Evolution on Sapphire …………………D. D. Koleske	11:20 AM	V8, Microcantilever Arrays as Biological and Chemical Sensors …………………..Steven L. Tripp
11:40 AM		11:40 AM		11:40 AM	V9, (Student), Controlling Kinesin-Microtubule Biomolecular Nanomotors ………………..Ying-Ming Huang

2004 EMC At-A-Glance

Thursday Afternoon, June 24, 2004

Thursday Morning Continued…

	Session W: Mismatched Materials: Metamorphic and Growth on Templates — Room: 129		Session X: Spin Injection, Spin Transport and Magnetic Anisotropy — Room: 102		Session Y: Nanotubes & Nanowires II — Room: 141
8:20 AM	W1, (Student), Extended Defect Microstructure of Metamorphic Buffer Layers Based on AlGaSb and InAsP ……………G. Suryanarayanan	1:30 PM	X1, Spin Injection from Fe_3Si into GaAs ……..Atsushi Kawaharazuka	1:30 PM	Y1, (Student), P Type Semiconductive Carbon Nanotube for Quantum Wire …………….Takafumi Kamimura
8:40 AM	W2, Comparison of Mixed Anion, InAsP and Mixed Cation, InAlAs Metamorphic Buffers Grown by MBE on InP Substrates and Device Implications ………………..Mantu K. Hudait	1:50 PM	X2, Fabrication and Characterization of an InGaAs Channel Spin Transistor with Fe Electrodes as Spin Injector/Detector ....…...Kanji Yoh	1:50 PM	Y2, (Student), Transient Photobleaching in Isolated Single-Walled Carbon Nanotubes ………………..Michael S. Arnold
9:00 AM	W3, (Student), Doping Studies in Metamorphic AlSb and InAlSb Films …………………….Peter O. Hill	2:10 PM	X3, Point Contact Spin Spectroscopy of Ferro-magnetic MnAs and GaMnAs Epitaxial Films …………………..B. Nadgorny	2:10 PM	Y3, (Student), Control of Electrical Property of Carbon Nanotube by Oxygen Ion Implantation with Ultra-Low Energy of 25eV ……………Kazuhiko Matsumoto
9:20 AM	W4, Surface Reconstruction Domains During the Growth and Annealing of InGaAs Alloys …………………...Alex Riposan	2:30 PM	X4, Magnetic Properties of MnAs/GaAs(001) at the Structural Phase Transition …………………………A. Ney	2:30 PM	Y4, (Cancelled), Simultations of Electronic Transport in Single-Wall and Multi-Wall Carbon Nanotubes …………..……Alexandre Mayer
9:40 AM	W5, (Student), Development of Metamorphic Buffers on InP for 6.00Å Narrow Bandgap Heterojunction Bipolar Transistors …………………Randy Sandhu	2:50 PM	X5, Ferromagnet/DMS Hybrid Structures: Low-Dimensional Magnetic Traps …………………...P. Redlinski	2:50 PM	Y5, Late News
10:00 AM	Break	3:10 PM	Break	3:10 PM	Break
10:20 AM	W6, Strain Relief of $In_xGa_{1-x}As$ Selectively Grown on Nanoscale SiO_2-Patterned GaAs(001) by Molecular Beam Epitaxy ………………………..S. C. Lee	3:30 PM	X6, Spin-Polarized Ballistic Transport in InSb/InAlSb Heterostructures ……………………Hong Chen	3:30 PM	Y6, Quantum Confinement Observed in Ultrafine ZnO and ZnO/ZnMgO Coaxial Nanorod Heterostructures ………………………Won Il Park
10:40 AM	W7, Epitaxial Lateral Overgrowth of InAs on W Masks ……..Lars-Erik M. Wernersson	3:50 PM	X7, (Student), Magneto-transport Studies of Magnetic Anisotropy in Strain-Engineered InMnAs Ferromagnetic Layers ……………………...W. L. Lim	3:50 PM	Y7, Rational Growth of Branched and Hyper-Branched Nanowire Structures ………………………..Deli Wang
11:00 AM	W8, (Student), Origin of Multiply-Tilted Grains in Conventional and Lateral Epitaxial Overgrowth of InAs Thin Films on (100) GaAs by MOCVD ……………….A. A. Khandekar	4:10 PM	X8, Magneto-Optical Studies of the Magnetic Anisotropy in III-Mn-As Ferromagnetic Semiconductors ………………….M. Kutrowski	4:10 PM	Y8, (Student), Heteroepitaxial Fabrication and Structural Characterizations of Ultrafine GaN/ZnO Coaxial Nanorod Heterostructures ………………………Sung Jin An
11:20 AM	W9, (Student), Lateral Growth Behavior of GaSb by Metal Organic Vapor Phase Epitaxy ………………Brian E. Hawkins	4:30 PM	X9, (Student), Magneto-Optical Activity of InMnAs Epitaxial Films at Room Temperature ……………..………Philip T. Chiu	4:30 PM	Y9, Ultrathin Epitaxial Metal Nanowires on Silicon (001) and (111) …………………….Herbert Pfnür
11:40 AM	W10, Room-Temperature Yellow-Amber Emission from InGaP Quantum Wells Grown on an InGaP Metamorphic Buffer Layer on GaP(100) Substrates ……..Vladimir A. Odnoblyudov	4:50 PM	X10, (Student), Magnetic Circular Dichroism in GaMnAs/ ZnSe Hybrid Structures with Be Co-Doping …………….Raja Chakarvorty	4:50 PM	Y10, (Student), Fabrications and Characterizations of Electroluminescent Devices Using n-ZnO Nanorod Arrays Vertically Grown on p-GaN Epilayers ………………………Won Il Park

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Thursday Afternoon, June 24, 2004

	Session Z: Semiconductor Nanostructures: Materials to Devices Room: 136		Session AA: Dilute Nitrides Room: 140		Session BB: Contacts to Wide Bandgap Semiconductors Room: 155
1:30 PM	Z1, (Invited), Near-Infrared in Vivo Imaging Using Quantum Dots ……………………Sungjee Kim	1:30 PM	AA1, (Student), Near-Field Scanning Optical Microscopy of Compositional Fluctuations in Dilute Nitride Alloys ………………………..Kai Sun	1:30 PM	BB1, (Student), Low Resistance Ohmic Contacts to Si Implanted GaN and Application in AlGaN/GaN HEMTs ……………………….Haijiang Yu
		1:50 PM	AA2, Identification of Nonradiative Recombination Centers in Ga(As,N) by Raman Spectroscopy ……….Manfred E. Ramsteiner	1:50 PM	BB2, (Student), Non-Polar GaN: p-Type Doping and Ohmic Contact Technology ……………………….John Simon
2:10 PM	Z2, (Student), Solution Phase Synthesis of Straight and Branched CdSe Nanowires ………Katherine Leigh Richter	2:10 PM	AA3, Thermal Annealing Effects and Local Atomic Configurations in GaInNAs Thin Films by Fluorescence X-Ray Absorption Fine Structure Spectroscopy …………………....Kazuyuki Uno	2:10 PM	BB3, Ir-Based Low Resistance Ohmic Contacts on p-GaN …………………………J. W. Bae
2:30 PM	Z3, Metal-Semiconductor Transition in Armchair Nanotubes: Possibilities for Metallic FET …………………Slava V. Rotkin	2:30 PM	AA4, (Student), Transmission Electron Microscopy (TEM) Structural Characterization of GaInNAs and GaInNAsSb Quantum Wells Grown by Molecular Beam Epitaxy (MBE) ……Tihomir Lubenov Gugov	2:30 PM	BB4, (Student), Effects of Reactive Ion Plasma Treatment on Ohmic Contacts to n-GaN and n-$Al_{0.55}Ga_{0.45}N$ ……………..Fitih M. Mohammed
2:50 PM	Z4, Size and Position-Controlled Zinc Oxide Nanodot Arrays with Focused Ion Beam Nanopatterning of Substrates ……………………Shizuo Fujita	2:50 PM	AA5, (Student), Electroabsorption and Band Edge Optical Properties of GaInNAsSb Quantum Wells Around 1550nm …………………Vincenzo Lordi	2:50 PM	BB5, The Effect of Substrate Bias During Plasma Etching on Metal Contact Performance for High % Al n-AlGaN Thin Films and LEDs………K. H.A. Bogart
3:10 PM	Break	3:10 PM	Break	3:10 PM	Break
3:30 PM	Z5, (Student), Defect-Free 50-Layer Strain-Balanced InAs Quantum Dots Grown on AlGaInAs/InP for Infrared Photodetector Applications ………………..Zhenhua Zhang	3:30 PM	AA6, Effects of Arsenic Species and Si-Doping on Nitrogen Incorporation in GaAsN Films …………………..H. A. McKay	3:30 PM	BB6, (Student), Formation of Low Resistance Contacts to Digital Alloys of n-$Al_{0.7}Ga_{0.3}N$ ……………………..Jonshin Yun
3:50 PM	Z6, Modification of Band Structures in Stacked InAs/GaAs Quantum Dot Systems by the Control of Mismatch Strain ……………………...Woong Lee	3:50 PM	AA7, (Student), Temperature Dependent Behavior of GaInNAs(Sb) Alloys Grown on GaAs …………………Seth R. Bank	3:50 PM	BB7, (Student), Fabrication of Light Emitting Diodes Using Low Resistance and Highly Transparent Ni-La Solid Solution Ohmic Contacts to p-Type GaN ………………...Tae-Yeon Seong
4:10 PM	Z7, (Student), Selectivity Between Quantum Dots and Dashes on InP and GaAs Based on Lattice Mismatch and Surface Migration ………………..G. Balakrishnan	4:10 PM	AA8, (Student), Ion Damage in Dilute Nitride Growth: Effect of Deflector Plate Voltage ………………Michael M. Oye	4:10 PM	BB8, (Student), Low Resistance and Highly Reflective MIO/Ag-Based Ohmic Contacts to p-Type GaN for Flip-Chip Light Emitting Diodes……………..June-O Song
4:30 PM	Z8, Red Light Emission by Electroluminescence from InP Quantum Dots on GaP(100) ……………………….F. Hatami	4:30 PM	AA9, Improving Optical Properties of 1550-nm GaInNAs/ GaAs Multiple Quantum Wells by GaInNAs Quaternary Barrier and Space Layer …………………..……..H. Y. Liu	4:30 PM	BB9, (Student), Ohmic and Blocking Contacts to n-Type ZnO (0001) Epitaxial and Bulk Material ………………Timothy E. Murphy
4:50 PM	Z9, Late News	4:50 PM		4:50 PM	BB10, (Student), Ohmic Contact on Nitrogen-Doped UNCD Films and Observation of Conduction Band Offset Between UNCD and Si ..……………………Ningyue Jiang

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Thursday Afternoon, June 24, 2004

Session CC: Transport in Organic Semiconductor Device — Room: 101		Session DD: Narrow Bandgap Devices and Materials — Room: 129		NOTES
1:30 PM	CC1, (Invited), Intrinsic Charge Carrier Transport on the Surface of Organic Semiconductors …………………..V. Podzorov	1:30 PM	DD1, High Quality InSb Photodiodes Structures Grown by MOVPE ……………………..Ariel Sher	
		1:50 PM	DD2, MBE Growth of 6.2 Å InAsSb High Electron Mobility Transistors ……………..Brad P. Tinkham	
2:10 PM	CC2, Fabrication and Characterization of Single-Crystal Organic Field Effect Transistors …….Christopher R. Newman	2:10 PM	DD3, Effects of Buffer Layers on the Structural and Electronic Properties of InSb Films …………………Xiaojun Weng	
2:30 PM	CC3, Intrinsic Hole Mobility and Temperature-Dependent Trapping in a Regio-Regular Poly(Thiophene) ………………...Alberto Salleo	2:30 PM	DD4, (Student), Zn Doping of p-Type GaAsSb from Spin-On Glass Dopant Sources …………………….Shishir Rai	
2:50 PM	CC4, Field Effect in Pentacene Single-Crystal/Sio_2/ Doped-Si Structures ………………………J. Takeya	2:50 PM	DD5, Low Resistance Ohmic Contacts on p-GaAsSb ……………………..J. H. Jang	
3:10 PM	Break	3:10 PM	Break	
3:30 PM	CC5, (Student), A New Model for an Organic Field-Effect Transistor ………………….Tae-Ho Jung	3:30 PM	DD6, (Student), Interwell Excitonic Effect in GaNAs/ GaAsSb Type-II Active Regions for Long Wavelength Operation ………………..Hyunsoo Yang	
3:50 PM	CC6, (Student), Alq and TPD Static Induction Transistor with Organic Semiconductors …………………..Serkan Zorba	3:50 PM	DD7, (Student), Measurements of Recombination Rates in Low-Doped Epitaxial GaInAsSb Lattice-Matched to GaSb by Frequency Response of Photoluminescence …………………..D. Donetsky	
4:10 PM	CC7, (Student), Contact Resistance in Pentacene Organic Thin-Film Transistors …………….Paul V. Pesavento	4:10 PM	DD8, Auger and Radiative Recombination Parameters in 0.55 eV InGaAsSb ………………...Ravi J. Kumar	
4:30 PM	CC8, Fa Electron Currents in Submicron Pentacene Transistors ……………………………..J. Jo	4:30 PM		

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Friday Morning, June 25, 2004

Session EE: Epitaxy for Devices Room: 102		Session FF: Defects in SiC Room: 141		Session GG: Semconductors: Processing and Oxidation Room: 136	
8:20 AM	EE1, (Student), Recombination Lifetime and Internal Quantum Efficiency in Gallium Arsenide Doped Beyond $N_A=1x10^{19}$ ……………..Thomas D. Boone	8:20 AM	FF1, Stacking Fault Growth in A-Face SiC PiN Diodes ………………R. E. Stahlbush	8:20 AM	GG1, Electrical and Optical Properties of Anodic LaAl ……………………….Tito Busani
8:40 AM	EE2, Photoluminescence Due to Be-As_{Ga} Complex in Low-Temperature MBE-Grown Be-doped GaAs ………………...Hiroyuki Bando	8:40 AM	FF2, Stacking Fault Nucleation in 4H-SiC PiN Diodes ………..Mark Erickson Twigg	8:40 AM	GG2, Improvement in the Insulating Properties of Thermal Oxide on InAlP …...Anthony John SpringThorpe
9:00 AM	EE3, Gallium-Arsenide Deep-Level Materials for THz and 1.5um Fiber-Optic Applications ……………………Janet L. Pan	9:00 AM	FF3, Cross-Polarization Imaging and Micro-Raman Detection of Defects in the Epitaxy of 4H-SiC …………..Orest J. Glembocki	9:00 AM	GG3, (Student), Electrical Properties and Microstructure of InAlP Native Oxides for MOS Applications ………………………….Ying Cao
9:20 AM	EE4, (Student), Compensation of Interfacial Charges at the Regrowth Interface Between InP Layers …………………...Yingda Dong	9:20 AM	FF4, A New Approach to Investigate Superscrew Dislocations in Silicon Carbide …………………...Xianyun Ma	9:20 AM	GG4, (Student), InAlP Native Oxide/GaAs MOS Heterostructure Interface State Density Measured by Impedance Spectroscopy ……………………..……Xiang Li
9:40 AM	EE5, Intersubband Emission from MBE-Grown InGaAs-AlAsSb Quantum Cascade Structures Spanning the λ~3-5μm Atmospheric Window ………………Matthew J. Steer	9:40 AM	FF5, Identification of Dislocations in Diffused 4H-SiC PIN Diodes Using EBIC ………...Stanislav I. Soloviev	9:40 AM	GG5, (Student), Lateral Wet Oxidation of AlAsSb Lattice Matched to GaSb ……………………Kevin Meneou
10:00 AM	Break	10:00 AM	Break	10:00 AM	Break
10:20 AM	EE6, (Student), The Sequential LPE and MBE of InAs on GaP - A Hybrid Form of MBE ………………………...An Chen	10:20 AM	FF6, High Temperature Operation of SiC Electronics and Sensors ………………Ruby N. Ghosh	10:20 AM	GG6, (Student), Characterization of Sulfur Passivated Group III Antimonide Semiconductors ……………..Joshua A. Robinson
10:40 AM	EE7, Growth of CaF_2/Si/CaF_2 Resonant-Tunneling Structures by B and Sb Surfactant-Enhanced Epitaxy ……………….Karl R. Hofmann	10:40 AM	FF7, Thermally Stimulated Current Spectroscopy of High-Purity Semi-Insulating 4H-SiC Substrates ……………..Zhaoqiang Fang	10:40 AM	GG7, (Student), Modifications of GaSb Surface Electronic Structure by the Chalcogen Atoms: S, Se and Te ………………………Zhiyan Liu
11:00 AM	EE8, Molecular Beam Epitaxial Growth of Cd-Based II-VI Wide-Band-Gap Compounds on Si …………………Gregory N. Brill	11:00 AM	FF8, (Student), First Observation of Current Induced Deep-Level Defects in 4H SiC PiN Diodes with Magnetic Resonance …………….……S. K. Yerkes	11:00 AM	GG8, (Student), Sputtered Titanium Oxide Barrier Layers for PZT MEMS …………..Steven Joseph Gross
11:20 AM	EE9, (Student), Epitaxial Growth of $FeSi_{2-x}Ge_x$: Towards a Tunable Silicon Based Electro-Optic Material ………………….Ryan J. Cottier	11:20 AM	FF9, (Student), Spin Dependent Recombination Observation of Hyperfine and Super-hyperfine Interactions of Interface Trap Defects at the 6H Silicon Carbide/Silicon Dioxide Boundary ………...………D. J. Meyer	11:20 AM	GG9, Novel Selective Dry Etch Process for Ultra Thin Pt Salicide Formation ………………………….Jihun Oh
11:40 AM		11:40 AM	FF10, (Student), Comparison of 4H-SiC PiN Diodes Fabricated with Different Starting Substrates …………………...P. A. Losee	11:40 AM	

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Friday Morning, June 25, 2004

Time	Session HH: Molecular Electronics II Room: 140	Time	Session II: Characterization of Nitride Semiconductors Room: 155	Time	Session JJ: Contacts to Nanotubes, Nanowires and Organic Films Room: 101
8:20 AM	HH1, (Student), Measuring Conduction Through Molecules Using Step Junction ……………..….Jaewon Choi	8:20 AM	II1, (Student), Demonstration of Non-Degenerate Electron Conduction in InN Grown by Molecular Beam Epitaxy …………..Craig Hartley Swartz	8:20 AM	JJ1, (Invited), Contacts to Carbon Nanotubes for Electronic and Spin-Electronic Devices ……….Bruce William Alphenaar
8:40 AM	HH2, Experimental Current-Voltage Characteristics of DNA and Modified DNA Molecules …………....V. Soghomonian	8:40 AM	II2, A Study of the Interfaces of GaN and AlN Nucleation Layers During GaN Growth on 4H- and 6H- SiC(0001) …………………...Tong-Ho Kim		
9:00 AM	HH3, (Student), Binary Molecular Materials for Storage, Transport, and Processing of Digital Information ………………………..Yuhui Lu	9:00 AM	II3, (Student), Capacitance-Voltage and Scanning Probe Studies of InGaN/GaN Quantum-Well Structures …………………………X. Zhou	9:00 AM	JJ2, Measuring the Specific Contact Resistance of Contacts to Semiconductor Nanowires …………….Suzanne E. Mohney
9:20 AM	HH4, (Student), Self-Assembled Monolayer Resist for Electron/Neutral Atom Beam Lithography ……….Siyuranga O. Koswatta	9:20 AM	II4, Quantitative Stress Characterization in GaN Films Grown on Patterned Si(111) by Micro-Raman Spectroscopy ………………………...D. Wang	9:20 AM	JJ3, (Student), Contact Resistance in Nanowire Characterization ………………...Ryan A. Munden
9:40 AM		9:40 AM	II5, (Student), Transmission Electron Microscopy and Photoluminescence Study of GaN Epilayers Grown by MOCVD ………………….Xiaolong Fang	9:40 AM	JJ4, (Student), Studies on Metal Contacts to InP Nanowires ……………………..…..S. S. Lau
10:00 AM		10:00 AM	Break	10:00 AM	Break
10:20 AM		10:20 AM	II6, (Student), Intra d-Shell Photoluminescence Transitions of Mn^{4+} Ions in GaN:Mn Codoped with Mg Acceptors ………………………..Bing Han	10:20 AM	JJ5, (Invited), Making Electrical Contacts to Organic Materials by Soft Lithography …………………...Julia W.P. Hsu
10:40 AM		10:40 AM	II7, (Student), The N-Face GaN Etch Property by Photo-Electro-Chemical (PEC) Wet Etching and its Application for High Efficiency GaN LEDs ………………………..Yan Gao		
11:00 AM		11:00 AM	II8, (Student), Optical Modes in Mushroom-Shaped GaN/ InGaN Microdisk Resonators Fabricated Using Photoelectrochemical Etching ……………..Elaine D. Haberer	11:00 AM	JJ6, Current Injection Mechanism in Metal/Molecular-Organic-Semiconductor/Metal Sructures …………………Subhasis Ghosh

2004 Electronic Materials Conference
TECHNICAL PROGRAM

Wednesday, June 23, 2004

EMC PLENARY LECTURE/STUDENT AWARDS

Ceremony: 8:20 AM

Room: 101

Plenary Speaker: Federico Capasso, Harvard University, Div. of Engrg. & Applied Scis., Cambridge, MA 02138 USA

Topic: Quantum Cascade Lasers: From Bandstructure Engineering to Commercialization

Break: 9:20 AM - 10:00 AM

Joint DRC/EMC Invited Session: Molecular Electronics and Carbon Nanotubes

Wednesday AM Room: 101
June 23, 2004 Location: DeBartolo Hall

Session Chair: Theresa S. Mayer, Pennsylvania State University, University Park, PA 16802-2705 USA

10:00 AM Invited

Characterization of Silicon-Based Molecular Resonant Tunneling Diodes with Scanning Tunneling Microscopy: N. P. Guisinger[1]; R. Basu[1]; M. E. Greene[1]; A. S. Baluch[1]; *M. C. Hersam*[1]; [1]Northwestern University, Dept. of Matls. Sci. & Engrg., 2220 Campus Dr., Evanston, IL 60208-3108 USA

In recent years, substantial progress has been made in the emerging field of molecular electronics. In particular, metal-molecule-metal junctions have been widely studied. In this paper, charge transport through molecule-semiconductor junctions is considered. The presence of the energy band gap in semiconductors provides opportunities for resonant tunneling through individual molecules, leading to interesting effects such as negative differential resistance (NDR). Furthermore, by doping the substrate, the majority charge carrier can be tailored, thus allowing asymmetry to be intentionally designed into the current-voltage characteristic. Through judicious choice of the molecular species, the bias voltage of the NDR can also be controlled. By demonstrating these effects on the Si(100) surface, semiconductor-based molecular electronic devices have the potential of being directly interfaced to conventional silicon integrated circuit technology. As an introduction, this paper will summarize recent theoretical[1] and experimental[2] work on silicon-based molecular resonant tunneling diodes. In particular, the ultra-high vacuum scanning tunneling microscope (STM) has allowed individual molecules to be imaged, addressed, and manipulated on the Si(100)-2×1 surface with atomic resolution at room temperature. While previous work has focused on the characterization of individual styrene and 2,2,6,6-tetramethyl-1-piperidinyloxy (TEMPO) molecules, this paper will also detail previously unpublished results for isolated cyclopentene molecules and full monolayers of TEMPO and cyclopentene. In all cases, STM current-voltage characteristics on individual molecules mounted on degenerately n-type Si(100) show multiple NDR events at negative sample bias. On the other hand, at positive sample bias, the current-voltage characteristics do not show NDR, although discontinuities in the differential conductance are observed. When the Si(100) substrate is changed to degenerate p-type doping, multiple NDR events are observed at positive sample bias while the discontinuities in the differential conductance occur at negative sample bias. These empirical observations can be qualitatively explained by considering the energy band diagram for a semiconductor-molecule-metal junction. For full organic monolayers on degenerately doped Si(100), similar behavior is observed except that the degree of NDR is significantly attenuated compared to charge transport measurements on isolated molecules. Possible explanations for this behavior include broadening of molecular energy levels through intermolecular interactions or concurrent tunneling paths through multiple molecules. This paper will conclude by describing recent efforts to quantify and understand the critical parameters that dictate charge transport through individual molecules and organic monolayers on Si(100) surfaces.[1]T. Rakshit, G.-C. Liang, A. W. Ghosh, and S. Datta, arXiv:Cond-Mat, 0305695v1 (2003). [2]N. P. Guisinger, M. E. Greene, R. Basu, A. S. Baluch, and M. C. Hersam, Nano Letters, 4, 55 (2004).

10:40 AM Invited

IR Emission from Schottky Barrier Carbon Nanotube FETs: *R. Martel*[1]; J. Misewich[2]; J. C. Tsang[3]; Ph. Avouris[1]; [1]Université de Montréal, CP 6128, Succursale Centre-Ville, Montréal H3C-3J7 Canada; [2]Brookhaven National Laboratory, Matls. Sci. Dept., Upton, NY 11973 USA; [3]IBM T. J. Watson Research Center, Kitchewan Rd., Yorktown Heights, NY 10598 USA

Single-walled carbon nanotubes (SWNTs) are tubular 1D nanostructures made of p conjugated C-C bonds. The SWNTs are exceptional 1D electrical conductor with a band structure forming unique sets of 1D subbands. These subbands form sharp singularities (van Hove) in the density of state, which lead to strong optical interband transitions. Here, we explore the optical properties of SWNT devices. We present recent advances on a novel electroluminescence device based on an ambipolar carbon nanotube FET. The device enables efficient charge injection across the metal-nanotube contact barrier and the band gap recombination of carriers in the nanotube with an emission in the near IR. The emitted light is linearly polarized along the nanotube axis and clearly originates from the nanotube channel. The emission wavelength is at around 1.7 mm and its intensity peaks at Vd=2 Vg. To our knowledge this nanotube device represents the smallest electrically pumped optical emission source. It also opens up new possibilities for studying fundamental electron-hole interactions in 1D and for exploring further electronic and optoelectronic applications with SWNTs.

11:20 AM Invited

Measurement of Electron Transport and Mechanical Properties of Single Molecules: *Nongjian Tao*[1]; Bingqian Xu[1]; Xiaoying Xiao[1]; [1]Arizona State University, Dept. of Elect. Engrg. & Ctr. for Solid State Elect. Rsch., Tempe, AZ 85287 USA

The ability to measure the conductance of a single molecule not only promises a better understanding of electron transfer in molecules, but also is a necessary step towards the goal of building a functional device using single molecules. Rapid progress has been made in recent years, but such measurements are still a difficult task. In order to reliably measure single molecule conductance, one must provide a reproducible and efficient electronic coupling between the molecule and the probing electrodes. Due to the apparent difficulty of forming microscopically identical molecule-electrode contacts, a statistical analysis over a large number of electrode/molecule/electrode junctions is necessary for a complete picture. One must also find a signature to identify that the measured conductance is due to not only the sample molecules but also a single sample molecule. We have developed a method to determine the conductance of single molecules covalently bonded to gold electrodes by repeatedly forming a large number of molecular junctions. We create each molecular junction by separating two Au electrodes from contact in a solution containing the sample molecules. During the separation, we

simultaneously measure the conductance and the force between the two electrodes. The conductance decreases in discrete steps, corresponding to the breakdown of individual molecules covalently bonded to the electrodes. Each discrete drop in the conductance is accompanied by a discrete drop in the force, which allows us to determine the bonding strength of the molecule to the electrodes. We have also determined the effective spring constant of a single molecule and the dependence of the conductance on the applied force. Using the method, we have studied both electron transport and mechanical properties of a number of different molecules, ranging from simple alkanedithiols to oligopeptides, covalently bonded to two Au electrodes via S-Au bonds. Our method has the following distinctive features: First, pronounced peaks in the conductance histogram constructed from thousands of individual measurements can be used to identify with the conductance of a single molecule. Second, since each molecular junction is formed by mechanically separating two electrodes, only the molecules bonded to the electrodes contribute to the measured conductance. In fact, the mechanical force provides direct information on the bonding nature of the molecules to the gold electrodes. Third, statistical analysis reduces mistaking signals from impurities for those from the sample. Finally, our method works in aqueous solution, which opens the door to the study of biological molecules under physiological conditions. Acknowledgement: We thank Stuart Lindsay, Larry Nagahara, Devens Gust, Thomas Moore, Anna Moore and Otto Sankey for their contributions, and DOE(DE-FG03-01ER45943) and NSF(CHE-0243423) for financial support.

Session A: High-K Dielectric Stacks

Wednesday AM Room: 102
June 23, 2004 Location: DeBartolo Hall

Session Chairs: Susanne Stemmer, University of California, Matls. Dept., Santa Barbara, CA 93106-5050 USA; Vijay Narayanan, IBM SRDC, T. J. Watson Rsch. Ctr., Yorktown Heights, NY 10598 USA

10:00 AM Invited

A1, New Metal Gate/High-K Dielectric Stacks for Continual Electrical T_{ox} Scaling and High-Performance CMOS Applications: *Robert Chau*[1]; Suman Datta[1]; Mark Doczy[1]; Jack Kavalieros[1]; Matthew Metz[1]; [1]Intel Corporation, Components Rsch., Logic Tech. Dvlp., 5200 N.E. Elam Young Pkwy., MS RA3-252, Hillsboro, OR 97124 USA

For more than 15 years the physical thickness of SiO2 has been aggressively scaled for low-power, high-performance CMOS applications. Recently SiO2 with physical thickness of only 1.2nm has been successfully implemented in Intel's 90nm logic node which is currently in production. In addition, SiO2 with physical thickness of 0.8nm (less than three atoms thick) has been demonstrated in our research laboratory and integrated into extremely scaled CMOS transistors with sub-30nm physical gate lengths. Continual gate oxide scaling, however, will require the use of dielectric materials with higher dielectric constant (K) since i) the gate oxide leakage current is increasing with decreasing SiO2 thickness, and ii) SiO2 is running out of atoms for further scaling. So far the most common high-K dielectric materials investigated by both academia and industry are Hf-based and Zr-based. There are two typical problems in replacing conventional polySi/SiO2 with the polySi/high-K dielectric stack for high-performance CMOS applications. First, high-K dielectrics and polySi electrode are incompatible due to the Fermi level pinning at the polySi/high-K interface, which causes high threshold voltages in MOSFET transistors. The Fermi level pinning is most likely caused by defect formation at the polySi/high-K dielectric interface which is very fundamental and difficult to fix. Second, polySi/high-K transistors exhibit severely degraded channel mobility due to the coupling of low energy surface optical (SO) phonon modes arising from the polarization of the high-K dielectric to the inversion channel charge carriers. The only way to alleviate the above problems is to use a composite gate dielectric stack with the high-K dielectric "sandwiched" between two SiO2 layers. However such approach increases the electrical thickness (Tox) significantly and reduces the overall drive current of the n- and p-channel transistors. It does not have sufficiently scalability required for high-performance CMOS applications. Computer simulations and physical modeling have shown that metal gate electrodes may be more effective than polySi in screening the high-K SO phonons from coupling to the channel under inversion conditions, resulting in improved channel mobility. However, the use of high-K/metal-gate require an n-type metal and a p-type metal with the right work functions on the high-K dielectric for high-performance CMOS logic applications on bulk Si. So far, all the metal gate electrodes reported in literature have work functions that are mid-gap or close to mid -gap on high-K dielectrics, and the resulting CMOS transistors have high threshold voltages and hence poor drive performance. We have successfully engineered n-type and p-type metal electrodes that have the correct work functions on the high-K for high-performance CMOS. The resulting metal gate/high-K dielectric stacks have equivalent oxide thickness (EOT) of 1.0nm and electrical Tox of 1.45nm with negligible gate oxide leakage, and p- and n-channel mobilities that are close to that of poly/SiO2. 80nm physical-gate-length CMOS transis tors with the new metal gate/high-K dielectric stacks have been fabricated to produce the expected high performance (due to reduction in electrical Tox in inversion and increase in inversion charge). At Vd = 1.3V, the NMOS transistor achieves record-setting Ion = 1.66mA/um with Ioff = 37nA/um, while the PMOS transistor achieves record-setting Ion = 0.70mA/um with Ioff = 25nA/um. Both the n-ch and pchannel transistors exhibit negligible gate oxide leakage currents. Intel Corporation is on track to implement this new metal gate/high-K dielectric technology in its 45nm logic technology node to be in production in 2007.

10:40 AM Student

A2, Electron Spin Resonance Study of Atomic Layer Deposited HfO_2 on (111) Silicon: *J. P. Campbell*[1]; P. M. Lenahan[1]; R. Puthenkovilakam[2]; J. P. Chang[2]; [1]Pennsylvania State University, Dept. of Engrg. Sci. & Mechanics, 212 Earth & Engrg. Sci. Bldg., Univ. Park, PA 16802 USA; [2]University of California, Dept. of Chem. Engrg., Boelter Hall Rm. 5531, Los Angeles, CA 90095 USA

The processing chemistry and defect structure of HfO_2/silicon systems is of considerable current interest as these systems appear to be leading candidates to replace the silicon dioxide based gate dielectrics of metal-oxide-silicon technology. In this study, we investigate the defect structure of unannealed 40Å thick atomic layer deposited (ALD) HfO_2 on (111) silicon with electron spin resonance. The strongest defect signature corresponds to an interfacial dangling bond defect with $g_{||} = 2.0091$ and $g_{perp} = 2.0016$. This tensor is essentially identical to that of the interfacial defect reported earlier in HfO_2/Si structures by Kang et al.[1] The tensor is similar to, but not identical to, the tensor observed for the P_b silicon "dangling bond" center found in conventional Si/SiO_2 interfaces. Several other groups have also recently reported P_b-like interface defects in high-k/Si systems.[2-3] In addition, we observe lower densities of several other defect centers; to the best of our knowledge, observation of these paramagnetic defects has not yet been reported in the literature. One has a very nearly isotropic g = 2.0022. Another low density defect has a nearly isotropic g = 2.0067. Upon 30 minutes of vacuum ultraviolet irradiation ($hc/\lambda \leq 10.2$eV) a fourth defect signature was observed. This defect spectrum is rather narrow with a zero crossing g = 2.0006 and might be an E' like SiO_2 dangling bond defect that is found in conventional SiO_2-based systems. The observation of the g = 2.0067 and g = 2.0006 spectra suggest the presence of high defect density silicon and a high intrinsic defect density dielectric. Future work will involve a study of defect type and density as the film thickness is increased from 40 to 400 Å and a comparison of the unannealed HfO_2/Si system discussed above and a forming gas annealed HfO_2/Si system. [1]A.Y. Kang, P.M. Lenahan, J.F. Conley, Jr., and R. Solanki, Appl. Phys. Lett. 81(6), 1128 (2002). [2]A. Stesmans and V.V. Afanas'ev, Appl. Phys. Lett. 82(23), 4074 (2003). [3]S. Baldovino, S. Nokhrin, G. Scarel, M. Fanciulli, T. Graf, and M.S. Brandt, J. Non-Cryst. Sol., 322, 168 (2003).

11:00 AM

A3, Origin of a Residual Charge and Effects of Nitridation of High-k Oxides in MOSFETS: Density Functional Studies: *Jacob Gavartin*[1]; Adam S. Foster[2]; Alexander L. Shluger[1]; Gennadi Bersuker[3]; [1]University College London, Dept. of Physics & Astron., Gower St., London WC1E

6BT UK; [2]Helsinki University of Technology, Lab. of Physics, PO Box 1100, Helsinki FIN-02015 Finland; [3]International Sematech, Austin, TX 78741 USA

Introduction of the oxides with a high dielectric constant as gate materials would allow for further miniaturization of field effect transistors. However, performance of high-k MOSFET prototypes generally suffers from the flat band potential instability associated with charged defects in the oxide. Post deposition annealing (PDA) of the oxide films in nitrogen contained ambient is considered to be the way of reducing this effect. However, there is little understanding of the role of nitrogen in relevant oxides, and the experimental data on nitridation are often conflicting. Following our previous density functional simulations of the oxygen vacancies and interstitials in the monoclinic Hafnia and Zirconia,[1-4] we study hydrogen contained defects as a suggested source of a positive built up charge in these materials.[5] In particular, we consider, protons, hydrogen atoms, hydroxide ions and water molecules in various polymorphs of Zirconia and Hafnia. We discuss the stability, reactivity and diffusivity of the above defects, and their effects on mechanical and electrical degradation. The calculations suggest a mechanism for the tetragonal-to-monoclinic phase transformation and the role of proton diffusion on the relative stability of these phases. We also discuss the conditions under which various charge states of hydrogen are realised and how they affect the dielectric response. Having established the role of the intrinsic defects and hydrogen, we then consider nitrogen contained species in the monoclinic hafnia and discuss their influence on electric properties of the oxide. Assuming various nitrogen PDA sources used experimentally, we study interaction of atomic and molecular nitrogen, ammonia and nitric oxide molecules with the host lattice. We further consider migration and various dissociation reactions with and without presence of anion vacancies and interstitial defects. Calculations suggest that nitrogen anneal of the oxides may lead to an effective immobilisation of native defects. However, nitrogen in molecular form is unlikely to significantly reduce a residual charge in the bulk film. In contrast, an atomic nitrogen, having larger solubility, may lead to a formation of oxynitride films with larger thermal and chemical stability. [1]A S Foster, A L Shluger, and R M Nieminen, Phys. Rev. Lett. 89, 225901 (2002). [2]A S Foster, F L Gejo, A L Shluger, and R M Nieminen, Phys. Rev. B 65, 174117 (2002). [3]A S Foster, V B Sulimov, F L Gejo, A L Shluger, and R M Nieminen, Phys. Rev. B 64, 224108 (2001). [4]A L Shluger, A S Foster, J L Gavartin, and P V Sushko, In Nano and Giga Challenges in Microelectronics. Ed. J. Greer, A. Korkin, and J. Labanowski (Elsevier, 2003, 151-222). [5]V V Afanas'ev, A Stesmans, Microelectronics Engeneering, 2004, in print.

11:20 AM Student

A4, Negative Bias-Temperature Instabilities in Metal-Oxide-Silicon Devices with SiO2 and SiOxNy/HfO2 Gate Dielectrics: *Xing J. Zhou*[1]; Sergery N. Rashkeev[2]; Leonidas Tsetseris[2]; Daniel M. Fleetwood[1]; Ronald D. Schrimpf[1]; Sokrates T. Pantelides[2]; Felix A. James[3]; Evgeni P. Gusev[4]; C. D'Emic[4]; [1]Vanderbilt University, Elect. Engrg. Computer Sci., VU Sta. B 351825, Nashville, TN 37235-1683 USA; [2]Vanderbilt University, Physics & Astron., Dept. of Physics & Astron., Nashville, TN 37235 USA; [3]Sandia National Laboratories, PO Box 5800, Albuquerque, NM 87185-1083 USA; [4]IBM Semiconductor Research and Development Center, IBM Thomas J.Watson Rsch. Ctr., Yorktown Heighs, NY 10598 USA

Negative bias-temperature instabilities (NBTI) are an important reliability problem affecting metal-oxide-semiconductor (MOS) devices.[1] NBTI are associated with the generation of oxide and interface trap charge at the Si/dielectric interface, when negative bias is applied to the gate for long times and/or elevated temperatures.[2]Hydrogen related species are associated with NBTI and many other defect formation processes in MOS gate dielectrics.[3] We have compared NBTI in two types of capacitors: one has thermal SiO_2 gate oxide; the other has a HfO_2 gate dielectric with a thin oxynitride at the Si interface. The changes in interface trap N_{it} and oxide trap N_{ot} charge densities with bias-temperature stress were determined by the midgap charge separation method. Activation energies for NBTI for the SiO_2 capacitors for N_{ot} is 0.27±0.03 eV, and for N_{it} is 0.31±0.04 eV; for SiO_xN_y /HfO_2 devices, Ea for N_{ot} is 0.35±0.04 eV, and for N_{it} is 0.22±0.03 eV. These activation energies are closest to the lateral motion of H^+ at the Si/SiO_2 interface. H^+ is very stable state at interface.[4] Under negative bias, a hydrogen atom in a bridging site in the near-interfacial Si will tend to (1) be charged positively, owing to the "negative U" properties of hydrogen in Si, and (2) be attracted to the interface. Once the H^+ is at the interface, it faces a small barrier (~ 0.3 eV) against lateral motion. During the lateral diffusion along the Si/SiO_2 interface, the H^+ may react with a Si-H bond to form an interface trap; or "hop" into the oxide in the presence of sub-oxide bonds (i.e., O vacancies that are very near the Si/SiO_2 interface) and trapped positive charge in SiO_2 to form positive oxide-trap charge, since there is large barrier for the diffusing H^+ to move into the oxide at a perfect /SiO_2 interface.[4] The differences in defect formation between the SiO_2 and SiO_xN_y /HfO_2 devices may then be explained by different amounts of hydrogen in the two types of devices, as well as the differences in O vacancy densities in the near-interfacial SiO_2. These results are consistent with the key roles played by hydrogen in MOS defect formation in MOS radiation response and long-term reliability, and suggest that minimizing the excess hydrogen in device processing may help to reduce NBTI. [1]Dieter K. Schroder and Jeff A. Babcock, J. Appl. Phys. 93, 1 (2003). [2]S. Ogawa, M. Shimaya, and N. Shiono, J. Appl. Phys. 77, 1137 (1995). [3]D. M. Fleetwood, Microelectron. Reliab. 42, 523 (2002). [4]S. T. Pantelides, S. N. Rashkeev, R. Buczko, D. M. Fleetwood, and R. D. Schrimpf, IEEE Trans. Nucl. Sci. 47, 2262 (2000).

11:40 AM

A5, Si and SiGe Vertical MOSFETs with CVD-HfO_2 Gate Dielectric: *Sankaran Kartik Jayanarayanan*[1]; Weiping Bai[1]; Dim-Lee Kwong[1]; Sanjay Kumar Banerjee[1]; [1]University of Texas, Elect. & Computer Engrg., 10100 Burnet Rd., Bldg. 160, Austin, TX 78758 USA

As CMOS devices are scaled into the sub-0.1 µm regime, conventional silicon dioxide-based gate dielectrics will face limitations and reliability problems due to unacceptable direct tunneling, high leakage current and breakdown. High-K materials are being explored to replace SiO_2 as the gate dielectric. Among all high-K gate dielectric materials, hafnium oxide (HfO_2) is being extensively investigated as one of the most promising candidate materials. High channel mobility materials such as SiGe and non-bulk planar CMOS structures such as vertical MOSFETs are also being investigated as ways to improve MOSFET performance. Since high quality SiO_2 cannot be thermally grown on SiGe, deposited high-K dielectrics on SiGe are an attractive option. We have fabricated the first Si as well as SiGe vertical MOSFETs with HfO_2 gate dielectric deposited by Rapid Thermal Chemical Vapor Deposition (RTCVD). After a standard pre-gate cleaning, the samples were pre-annealed in the presence of NH_3 at 700°C for 10 s to prevent oxide growth on the interface during the following HfO_2 deposition. 9 nm of CVD-HfO_2 was then deposited at 500°C. An in situ N_2 post-anneal at 700°C for 30 s was performed to improve the quality of the HfO_2 layer. A TEM cross-section of the device showed the physical thickness of the HfO_2 layer to be 9 nm, and conformal and uniform throughout the device. A polysilicon-gate electrode was deposited, implanted, and annealed at 900°C for 1 minute. X-ray diffraction (XRD) rocking curves of the Si (004) plane demonstrate that the SiGe layers do result in compressive strain. The Ge profile, with a mole-fraction of about 15%, is uniform over the entire device, as measured by Secondary Ion Mass Spectroscopy (SIMS). The 90 nm p-channel MOSFETs show excellent subthreshold and output characteristics. The drive current for the vertical SiGe PMOSFET was found to be enhanced by as much as 40% as compared with the silicon control device, in both the forward and reverse modes of operation. The drain induced barrier lowering (DIBL) for the SiGe device was observed to be higher than the Si device, since SiGe has a lower bandgap than Si. The gate leakage currents for the Si and SiGe devices with HfO_2 gate are comparable, and about 1000x lower than the gate leakage current for a Si PMOSFET with a 2 nm SiO_2 gate dielectric.

Session B:
Magnetic Semiconductors: Growth and Characterization

Wednesday AM	Room: 141
June 23, 2004	Location: DeBartolo Hall

Session Chairs: Nitin Samarth, Pennsylvania State University, Physics Dept., University Park, PA 16802 USA; Margaret Dobrowolska, University of Notre Dame, Dept. of Physics, Notre Dame, IN 46556 USA

10:00 AM

B1, Point Contact Andreev Reflection Spin Polarization Measurements in InMnSb Epilayers: *B. Nadgorny*[1]; R. P. Panguluri[1]; T. Wojtowicz[2]; W. L. Lim[2]; X. Liu[2]; J. K. Furdyna[2]; [1]Wayne State University, Physics, 666 W. Hancock, Detroit, MI 48201 USA; [2]University of Notre Dame, Physics, Notre Dame, IN 45556 USA

Narrow-gap ferromagnetic In1-xMnxSb alloy, which has a small effective hole mass, and thus a higher hole mobility, has the potential for applications in infrared spin-photonics[1] and in spin-transport devices. We have done Point Contact Andreev Reflection (PCAR)[2] measurements on epitaxially-grown ferromagnetic epilayers of In1-xMnxSb with x~0.03, which have a Curie temperature of ~9K. We demonstrate the feasibility of the PCAR spectroscopy in In1-xMnxSb by first studying Andreev reflection in its non-magnetic analog, In1-yBeySb, with y~0.05, chosen in such way that its free hole concentration (p=1.5×1020 cm-3) was close to the one in In1-xMnxSb. We analyzed dI/dV characteristics of In1-yBeySb/Sn junctions at different temperatures, and found them to be consistent with conventional Andreev reflection in a non-magnetic material, with the possible presence of proximity-induced superconductivity effects at the lowest temperatures. These measurements provided control data for comparison with subsequent PCAR measurements on ferromagnetic In1-xMnxSb. High transparency contacts were found for both magnetic and non-magnetic semiconductors. In contrast to our work on GaMnAs,[3] where we have observed some thermal spectra broadening, point contacts in In1-xMnxSb/Sn are well described by the conventional theory, with the characteristic suppression below the superconducting gap due to the spin polarization of In1-xMnxSb, which was found to be 52 ± 3%. [1]T. Wojtowicz et al., Appl. Phys. Lett. 82,4310 (2003). [2]R.J. Soulen et a.l, Science, 282, 85 (1998); S.K. Upadhyay, et al., Phys. Rev. Lett. 81, 3247 (1998). [3]R.P. Panguluri et al., submitted to Phys. Rev. Lett.

10:20 AM Student

B2, Structural and Magnetic Properties of Cr-Doped InN Films Grown by Plasma-Assisted MBE: *Rekha Rajaram*[1]; Glenn Solomon[2]; R. F.C. Farrow[3]; J. S. Harris[4]; S. S.P. Parkin[3]; [1]Stanford University, Matls. Sci., Ctr. for Integrated Sys., CISX 126X, Via Ortega, Stanford, CA 94305 USA; [2]CBL Technologies Inc., 2682 Middlefield Rd., Ste. I, Redwood City, CA USA; [3]IBM Almaden Research Center, San Jose, CA 95120 USA; [4]Stanford University, Solid State and Photonics Lab, Stanford, CA 94305 USA

Diluted magnetic semiconductors (DMS) based on III-V Nitrides have attracted much interest as they are expected to have long diffusion lengths and spin lifetimes due to reduced spin-orbit coupling. Also, the predicted Curie temperatures for these p-doped materials exceed room temperature. While several groups have studied the doping of GaN with magnetic ions, there have been no reports yet of diluted magnetic InN alloys. The growth of epitaxial InN is very difficult because of a lack of lattice-matched substrate with a similar thermal expansion coefficient. Also, the optimum growth temperature for InN is low compared to that of GaN because of its high dissociation pressure. Hence it is difficult to grow InN by CVD, which requires high temperatures for the decomposition of ammonia. However, InN has several interesting electrical properties, including a high electron drift velocity, which suggest many potential applications. Hence we have studied a DMS system based on Cr-doped InN. The Nitride films were grown by Plasma-Assisted MBE on c-plane Sapphire substrates. Thin GaN buffer layers grown by CVD were used to accommodate the high lattice mismatch between InN and Sapphire. In-situ RHEED was used to analyze the effect of growth temperature and plasma power on the crystalline quality of the films. X-ray diffraction (XRD) confirmed crystalline films with InN (0001) oriented parallel to Al_2O_3(0001). The FWHM of InN (0002) X-Ray rocking curve was about 0.1°. The GaN layers were strained while the InN was almost fully relaxed. Room temperature PL measurements of InN films yield a bandgap of around 0.8eV, which is typical of single crystal films. Cr-doped InN films (with up to about 1% Cr, determined by RBS) were grown at 350°C. XRD of the In(Cr)N films did not show any peaks corresponding to any other phases. Ferromagnetism was observed at low temperatures using a SQUID magnetometer, with a Curie temperature of about 50K. Hall measurements showed a high n-type carrier concentration of about $1*10^{20}cm^{-3}$. This is an interesting result since most of the other III-V based DMS materials exhibit p-type conductivity.

10:40 AM Student

B3, Single Crystals of $Zn_{1-x}Mn_xO$ and $Zn_{1-x}Co_xO$ for Spintronic Applications: *Matthew H. Kane*[1]; Varatharajan Rengarajan[2]; Christy Vestal[3]; Kandoor Shalini[1]; John Zhang[3]; Jeffrey Nause[2]; Christopher Summers[1]; Ian T. Ferguson[4]; [1]Georgia Institute of Technology, Sch. of Matls. Sci. & Engrg., Atlanta, GA 30332-0245 USA; [2]Cermet Inc., 1019 Collier Rd., Ste. C, Atlanta, GA 30318 USA; [3]Georgia Institute of Technology, Sch. of Chmst. & Biochmst., Atlanta, GA 30332-0400 USA; [4]Georgia Institute of Technology, Sch. of Elect. & Computer Engrg., Atlanta, GA 30332-0250 USA

Dilute magnetic semiconductors make ideal candidates for spintronic applications due to the ability to integrate them into existing semiconductor technologies. Recent research in the field of ferromagnetic semiconductors has suggested that the II-VI oxide based ferromagnetic semiconductors $Zn_{1-x}Mn_xO$ and $Zn_{1-x}Co_xO$ may be suitable for room temperature spintronic applications, as they both have a Curie temperature greater than 300 K. The exact nature of the ferromagnetism as well as the processing conditions required to reliably achieve and optimize the performance of these materials is still under investigation. Both non-equilibrium thin film growth techniques as well as solid state reaction have both been used to produce ferromagnetic II-VI compounds. This is in stark contrast to the traditional III-V compounds such as $Ga_{1-x}Mn_xAs$ which are generally produced using far-from-equilibrium techniques. This work discusses single crystals of $Zn_{1-x}Mn_xO$ and $Zn_{1-x}Co_xO$ which may show future use as substrates for next generation spintronic devices. Single crystals of $Zn_{1-x}Mn_xO$ and $Zn_{1-x}Co_xO$ have been grown by a patented technique. X-ray diffraction measurements show that transition metals can be incorporated on Zn sites and that an increase in the lattice parameter is apparent with increasing alloying content. No macroscopic second phases could be identified via x-ray diffraction, though peak asymmetries in the high resolution XRD scans suggest non-uniform alloy composition in the more heavily alloyed samples. UV-visible transmission measurements show absorption bands in the visible regime that are distinctive to interatomic transitions in the individual divalent transition metal substituents. Magnetization measurements using SQUID magnetometry on these samples show varying magnetic behavior depending on the alloy concentration and processing conditions. Photoluminescence measurements performed show green band emission related to intrinsic defects, and electrical property measurements indicate background n-type conductivity typical of ZnO. Further work is needed to optimize the material processing in this system for reproducible and significantly robust ferromagnetism in these materials. However, this work demonstrates that ZnO may provide also a suitable platform for the incorporation of transition metal elements into single crystals for next-generation spintronic devices.

11:00 AM Student

B4, Local Structure about Mn Ions in III-Mn-V Ferromagnetic Semiconductor Alloys: *Aaron M. Stuckey*[1]; Igor de Vasconcelos[1]; Tomasz Wojtowicz[1]; Xinyu Liu[1]; Jacek K. Furdyna[1]; B. A. Bunker[1]; [1]University of Notre Dame, 341 Nieuwland Sci. Hall, Notre Dame, IN 46556 USA

"Spintronic" semiconductors show great promise for many magnetoelectronic and magneto-optical applications. One such material which has garnered a great deal of attention has been $Ga_{1-x}Mn_xAs$, in which the magnetic spins are believed to be aligned through spin interactions carried via the holes. A number of attempts have been made to increase the Curie temperature (T_c) of random alloys of $Ga_{1-x}Mn_xAs$.

This study examines local structure in two methods, one which increased the number of magnetic ions taking part in the ferromagnetic interaction, the other which attempted to increase the number of holes available to mediate the ferromagnetic interaction (via heavy Be co-doping leading to the formation of quaternary $Ga_{1-x-y}Mn_xBe_yAs$ alloy). The increase in the number of magnetic Mn ions participating in ferromagnetism caused by low-temperature annealing of the $Ga_{1-x}Mn_xAs$ random alloys after growth has now been established[1,2] and linked to the change in the Mn site occupation.[2] A theoretical model[3] has indicated that at very large hole concentration (caused by doping with either Mn or Be acceptors, or both) it is energetically favorable for an increasing fraction of Mn ions to occupy interstitial or other sites rather than substitutional sites. Channeling Rutherford back scattering (c-RBS) and channeling particle induced x-ray emission (c-PIXE) studies have already verified the change in Mn site occupation, both with annealing[2] and acceptor doping,[2,4] but additional experimental techniques can shed light on the problem. Here, we report on XAFS (X-ray Absorption Fine-structure Spectroscopy) measurements of the local structure about the Mn site in both $Ga_{1-x}Mn_xAs$ and $Ga_{1-x-y}Mn_xBe_yAs$ random alloys. Results will be presented on the site occupation of Mn in different substitutional and interstitial sites as well as possible nanoprecipitates. Recent XAFS results concerning Mn location in new members of III-Mn-V family of ferromagnetic semiconductors: $In_{1-x}Mn_xSb$ and $In_{1-x-y}Mn_xBe_ySb$ alloys will also be presented. [1]S. J. Potashnik, K.C. Ku, S.H. Chun, J.J. Berry, N. Samarth, and P. Schiffer, Appl. Phys. Lett. 79, 1495 (2001). [2]K. M. Yu, W. Walukiewicz, T. Wojtowicz, I. Kuryliszyn, X. Liu, Y. Sasaki, and J. K. Furdyna, Phys. Rev. B 65, 201303-1(R) (2002). [3]W. Walukiewicz, Appl. Phys. Lett. 54, 2094 (1989). [4]K.M. Yu, W. Walukiewicz, T. Wojtowicz, W.L. Lim, X. Liu, Y. Sasaki, M. Dobrowolska, and J.K. Furdyna, Phys Rev B 68, 041308-1(R) (2003).

11:20 AM

B5, Strong Ferromagnetism in GaMnN Alloys Grown by MBE: *Joseph E. Van Nostrand*[1]; John D. Albrecht[2]; [1]Air Force Research Lab, Matls. & Mfg. Direct., B620, 2241 Avionics Cir., Ste. 21, WPAFB, OH 45433-7322 USA; [2]Air Force Research Lab, Sensors Direct., 2241 Avionics Cir., B620, WBAFB, OH 45433 USA

Magnetic semiconductors have attracted a great deal of interest not only for their potential use in spintronics, but also because of the fundamental question of how does ferromagnetism arise from a dilute alloy of a paramagnetic semi-insulator. In this presentation, we report on progress on the growth and characterization of GaMnN alloys with the range 5-15% Mn incorporation grown by low-temperature MBE. Magnetization and transport data indicates that high-quality alloys of GaMnN have been grown and ferromagnetic transitions at approximately 150 K are observed. The Hall and low-temperature magnetoresistance transport data, combined with X-ray diffraction measurements, give a strong indication that the alloy is uniform and that we do not observe phase segregation. In addition to the presentation of experimental data on our samples, we will comment on explanations for the origin of magnetic ordering in these films. The final analysis argues that the accepted model of carrier-mediated exchange does not give rise to ferromagnetic ordering in these n-type GaMnN alloys.

11:40 AM B6, Late News

Session C: Materials Integration: Wafer Bonding and Alternative Substrates

Wednesday AM June 23, 2004 — Room: 136 Location: DeBartolo Hall

Session Chairs: Karl D. Hobart, Naval Research Laboratory, Washington, DC 20375 USA; Peter D. Moran, Michigan Technological University, Dept. of Chem. Engrg., Houghton, MI 49931 USA

10:00 AM

C1, UHV-Wafer Bonding of Heterostructure Semiconductor Materials Using Low Energy Hydrogen Ion Beam Surface Cleaning: *Razek Nasser*[1]; Volker Gottschalch[2]; Axel Schindler[1]; Bernd Rauschenbach[1]; [1]Leibniz-Institute for Surface Modification, Dept. of Ion Beam Tech., Permoserstr. 15, Leipzig D-04303 Germany; [2]University of Leipzig, Inst. of Anorganic Chmst., Linnéstr. 3, Leipzig D-04103 Germany

A room temperature direct wafer bonding process under UHV conditions without applying external pressure based on low energy hydrogen ion beam surface cleaning has been studied for GaAs and other III-V-semiconductors. Successful bonding has also been performed between III-V-wafers and Si or Ge, respectively. XPS, Atomic force microscope measurements, ultrasonic microscopy, HR-TEM cross section, photoluminescence, electrical characterization and the measurement of the bond strength together with post-processing thermal treatment steps were performed to characterize the ion beam treated surfaces and the bonded interfaces formed. The developmental work focuses on later optoelectronic applications. Therefore we concentrate on the bonding of GaAs with GaAs hetero-epitaxial multilayer-systems and of GaAs with Ge. The bonding technique comprises three steps which are performed one after the other under UHV conditions in a multi chamber UHV system. The first step is a newly developed cleaning technology for semiconductor surfaces to remove oxide layers and carbon contamination from the surfaces of the two wafers to be bonded. The cleaning is performed at surface temperatures of 150°C, 7 min for GaAs and of 350°C, 25 min for Ge, respectively using low energy bombardment of mass separated hydrogen (H2+) ion beam of 300 eV ion energy and of 4.5 µA/cm2 ion current density from a 4 cm diameter broad beam hot filament ion source. In comparison to conventional cleaning, this technique leads to surfaces which are free of contamination and which do not show any deterioration in roughness. The second step is the bonding at room temperature without using any mechanical force from outside. The last step is a post-bonding thermal treatment of up to 350°C for 60 min maximum. The TEM measurements show for GaAs on GaAs a slight interface of about 3 nm thickness whereas for GaAs on Ge no such interface layer has been detected. Both, the bonding of p-GaAs on n-GaAs and p-Ge on n-GaAs without detailed processing optimization so far show reasonable diode like I-U-characteristics.

10:20 AM Student

C2, Changes in Interfacial Bonding Energies in the Chemical Activation of GaAs Surfaces: *Ning Liu*[1]; Thomas F. Kuech[2]; [1]University of Wisconsin, Matls. Sci. Prog., 1415 Engrg. Dr., Madison, WI 53706 USA; [2]University of Wisconsin, Dept. of Chem. & Bio. Engrg., 1415 Engrg. Dr., Madison, WI 53706 USA

The integration of III-V materials, through wafer bonding, has been pursued using semi-insulating GaAs as an integration platform. In these applications, an increase in initial bonding strength allows for more aggressive post-bonding processing. Many efforts have directed to increasing the bonding strength and improve the bonding quality by activating the surfaces during wafer bonding processes. Plasma or ozone-based treatments are commonly used to remove hydrocarbon contaminants which are one of the main sources for the bubble nucleation and to activate the surface. In this study, GaAs(100)-GaAs(100) bonded pairs were prepared using $HCl:H_2O(1:1)$ wet chemical treatments combined with plasma or ozone pre-bonding treatments. The affect of the addi-

tional use of a HCl:H_2O treatment after these dry processing steps was determined. The bond strength was quantitatively determined using the crack-opening method. Bonded surfaces were characterized using IR transmission imaging combined with FTIR measurements. With the single plasma treatment, the bonding energy was ~48 mJ/m^2. However, the bonding energies were increased to ~179 mJ/m^2 and ~497 mJ/m^2, respectively, by combining the supplementary HCl:H_2O(1:1) treatment with plasma and ozone treatments. The increase of the bonding energy in these experiments is described in terms of the intermediates on the surfaces during the pre-treatments. For GaAs-GaAs bonding, previous studies have shown that the room temperature bond is formed by hydrogen-bonded H_2O/OH groups. The areal concentration of these groups is directly correlated to the bonding strength. The surface of GaAs wafers is initially covered by the native oxide, consisting of a complex mixture of Ga and As oxides as well as suboxides and potentially some free As. The HCl:H_2O rinsing removes the native oxide and then forms Ga-OH groups on the surface. Our results indicated that on GaAs surfaces the high concentration of hydroxyl groups, due to the HCl:H_2O(1:1) final treatment, increased the extent of the hydrogen bonding, which contributed to the overall increase in the bonding strength. Based on these observations, the development of alternative techniques to increase the areal concentration of hydroxyl groups would lead to a significantly increased bonding energy. We compare the use of basic solutions, such as those based on NH_4OH, with these conventional solutions in the quantitative determination of the bond energy.

10:40 AM Student

C3, InGaAs Quantum Wells Grown by MOCVD on InP/GaAs Composite Substrates: *Sumiko Lynn Hayashi*[1]; David Bruno[1]; Rajinder Singh Sandhu[2]; Mike Wojtowicz[2]; Gangyi Chen[3]; Robert F. Hicks[3]; Mark S. Goorsky[1]; [1]University of California, Dept. MSE, BH 2517, Los Angeles, CA 90095 USA; [2]Northrop Grumman Space Technology, 1 Space Park Dr., Redondo Beach, CA 90278 USA; [3]University of California, Dept. Chem. Engrg., Los Angeles, CA 90095 USA

InP on GaAs wafer bonded substrates were employed for the epitaxial deposition of InGaAs/InAlAs quantum wells. InP template layers are bonded and transferred to GaAs handle wafers to create a III-V semiconductor on insulator structure using silicon nitride intermediate layers. A psuedomorphic In0.6Ga0.4As/InAlAs single quantum well structure was grown by MOCVD on 1) an epi-ready InP substrate, 2) an InP substrate that was subject to our chemical-mechancial polishing (CMP) process, and 3) a hydrogen split and CMP InP template layer on GaAs. This provides a comparison between the template structure and a standard wafer, and also separately investigates the effectiveness of our CMP step independently of the bonded structure. To fabricate the composite InP/GaAs "substrate", an InP wafer is implanted with a high dose of hydrogen (5.0x1016 H2+/cm2) to a depth that corresponds to the desired InP layer thickness (150 keV ~ 0.6 μm). The wafers are bonded and annealed at a low temperature (150ºC) to strengthen the bond, subsequently the InP layer is exfoliated at 300 ºC along the projected range of the implant. The splitting process generally leaves a rough surface, therefore, a chemical mechanical polishing step using sodium hypochlorite and citric acid "slurry" has been developed to produce low roughness, damage free surfaces with very low material removal rates such that the final InP layer thickness is ~ 0.3 μm. MOCVD growth was carried out in a Veeco D125 Turbo-disk MOCVD system, using TMIn, TMGa, TMAl, and TBAs precursors at a total pressure of 60 Torr. High resolution x-ray diffraction (HRXRD), double crystal x-ray topography, transmission electron microscopy and atomic force microscopy were employed to investigate the structural defects in these structures and how they affect the subsequent electronic properties. The transferred layer exhibits mosaic tilt that is non-uniformly distributed throughout the layer (TAD FWHM 40-100 arc sec), most likely due to voids trapped in the bonded interface. Ion implantation damage may also contribute to this width, which remains through annealing at 800°C. This increase in mosaicity is mimicked in the quantum well structure grown upon the transferred layers. Quantum well structures grown on the epi-ready InP substrate and the CMP substrate exhibit similar crystalline quality (TAD FWHM 10 arcsec). All three specimens exhibit identical composition profiles from the HRXRD patterns, however, the layers grown on the CMP surfaces (template layer and the separately polished substrate) are more specular and exhibited lower surface roughness than on the epi-ready InP substrate. The electronic properties of the quantum well structures were also investigated with photoluminescence and room temperature Hall measurements.

11:00 AM

C4, Combined Use of Neon Ion Implantation and Hydrogen Plasma Implantation in Ion-Cutting: *Peng Chen*[1]; Paul K. Chu[1]; Bo Chen[2]; Alexander Usenko[2]; William Carr[2]; [1]City University of Hong Kong, Dept. of Physics & Matls. Sci., Tat Chee Ave., Kowloon Hong Kong; [2]New Jersey Institute of Technology, Newark, NJ 07102 USA

Among the many techniques to fabricate silicon-on-insulator (SOI) wafers, the ion-cut process is developing very quickly and in fact commercially employed by SOITEC in their "Smart-Cut" technology as well as Silicon Genesis. In the ion-cut process, an oxidized silicon or receptor wafer is bonded to another silicon or donor wafer implanted with a high enough dose of hydrogen (normally around 5•1016 cm-2). By means of annealing and/or mechanical techniques, layer splitting occurs parallel to the bonded interface around the H-implanted region in the hydrogen-implanted wafer and thus a thin Si layer can be transferred from the donor wafer to the receptor wafer. One of the important issues is the non-uniform thickness of the transferred layer and this can lead to yield degradation especially for ultra-thin (less than 100 nm) SOI wafers when low implantation energy is required. Some co-implantation methods have been proposed to overcome these hurdles and they include co-implantation of boron and hydrogen or helium and hydrogen. In the work presented here, a new method is used to improve the quality of layer transfer using neon pre-implantation followed by hydrogen plasma immersion ion implantation (PIII). Neon implantation introduces a trapping layer in the Si substrate for hydrogen. Neon has advantages in trapping hydrogen over boron and helium due to its relatively big atom size and chemical inertness. The hydrogen PIII technology has advantages over traditional beam-line ion implantation with respect to high efficiency, small instrument footprint, and low cost. In our process, a buried trapping layer is first formed in <100> p-silicon substrate by 5´1015~1´1016 cm-2 Ne+ implantation at 170 kV. After a pre-annealing step at 600°C, 3-5´1016 cm-2 of hydrogen was plasma implanted into these samples between 20 kV to 25 kV. The control samples were prepared by hydrogen PIII only without Ne pre-implantation. Following PIII, the samples were annealed at 600°C to form surface blistering for initial monitoring or bonded to other silicon wafers to conduct layer transfer. Surface blistering was studied using scanning electron microscope (SEM), Fourier transform infrared (FTIR) spectroscopy was utilized to examine the chemical bond, and atomic force microscopy (AFM) was employed to measure the surface morphology and thickness of the transferred layer. Our SEM data indicate that after annealing at 600°C, the Ne/H co-implanted samples form surface blistering with a much higher intensity than the hydrogen-implanted samples. Besides, the former samples exhibit much better uniformity in the bubble size from the center to the edge of the wafers. AFM measurements show that the layers transferred from the co-implanted samples have better thickness uniformity. These results suggest an alternative method to yield higher quality and lower cost using the ion-cut process.

11:20 AM Student

C5, High Resolution X-Ray Diffraction Characterization of the Depth Dependent Structural Transformations in HE-Implanted PZN-PT: *Natee Tangtrakarn*[1]; M. Levy[1]; P. D. Moran[1]; [1]Michigan Technological University, Matls. Sci. & Engrg., 1400 Townsend Dr., Houghton, MI 49931 USA

High energy He+ implantation of PZN-PT is used to integrate the material with alternative substrates by enabling the slicing off of single crystal thin films from bulk substrates through subsequent selective etching or thermal annealing. The manner in which He ion implantation impacts the ability to slice off single crystal thin films depends on the poorly understood structural changes induced by the implantation process. This work is a high-resolution x-ray diffraction (HRXRD) of the structural transformations in single crystal PZN-PT due to high energy He+ ion implantation. In particular, 002 HRXD measurements are performed on 001-oriented 4.5%PZN-PT samples implanted with 1.0 MeV He ions for doses varying from 0.75x 1015 up to 100 x 1015 He ions/cm2 and for 3.8 MeV He ions for doses varying from 10x1015 up to 100x1015 He ions/cm2. These data are interpreted in terms of the formation of at least two distinct structural regions in the sample: a through-implanted region (film 1) for which the impact on the structure

is only due to the "electronic stopping" of the implanted ions by PZN-PT, and a highly damaged sub-surface layer (film 2) that occurs roughly at the depth corresponding to the peak concentration of implanted ions where lattice damage is due to the nuclear stopping of the implanted He ions. An unusually large change in the perpendicular lattice constant is observed to occur both in film 1 (e > 2.0%), and in film 2 (e > 3.5%). The dependence upon He ion dose of these perpendicular strains are measured and reported. The breadth of the 002 HRXD peak from film 1 is only slightly dependent on dose, where as that from film 2 broadens significantly and is greatly reduced in intensity as the ion dose increases. The data from film 1 are consistent with the film remaining single crystal but possessing an increasingly non-uniform depth-dependent strain distribution as the ion dose is increased, whereas the data from film 2 is interpreted as evidence that increased ion dose results in increasingly large densities of extended crystalline defects in this region that eventually results in the onset of amorphization.

11:40 AM C6, Late News

Session D: SiC Growth and Device Processing

Wednesday AM Room: 140
June 23, 2004 Location: DeBartolo Hall

Session Chairs: Robert E. Stahlbush, Naval Research Laboratory, Washington, DC 20375 USA; Michael A. Capano, Purdue University, Sch. of Elect. & Computer Engrg., W. Lafayette, IN 47907-1285 USA

10:00 AM

D1, Drift Free, 10 kV, 20A, 4H-SiC PiN Diodes: *Mrinal Kanti Das*[1]; [1]Cree, Inc., Power R&D Advd. Devices, 4600 Silicon Dr., Durham, NC 27703 USA

4H-SiC material technology has advanced to allow the demonstration of high power PiN diodes up to the 20 kV range.[1] However, the 4H-SiC PiN diodes suffer from forward voltage instability, where the VF may increase by several volts during operation.[2] Detailed study[3] of this phenomenon have provided the following picture: 1.) under forward bias, bipolar current flow in the ¡§i¡¨ layer causes electron-hole recombination; 2.) the recombination provides energy to the lattice allowing basal plane screw dislocations (BPD) to generate stacking faults; 3.) the stacking fault becomes negatively charged by trapping electrons; 4.) electron injection is attenuated at the cathode with a corresponding reduction of hole injection at the anode; 5.) the area under the fault becomes devoid of plasma thereby reducing the effective current handling area; 6.) a larger amount of forward bias is now needed to maintain the same forward current level. Hence, the key to producing drift-free PiN structures is the reduction of BPDs. Typically, the areal density of BPDs in the substrate is ~2000 cm-2 of which 90% can be turned into relatively benign threading edge dislocations in epitaxy. Recent innovations have reduced the epilayer BPD density below 10 cm-2.[3] This contribution reports the first high power (10 kV, 20 A) 4H-SiC PiN diodes fabricated using this low BPD process. A 400 ?Ým wide JTE implant is formed around the device periphery. The implants are activated with a 1600°C anneal in Ar. Sintered Ni contacts are made to the anode and cathode before depositing a thick Au overlayer. Full 10 kV blocking capability is achieved with an extremely low forward drop of 4.2 V \@ 20 A (100 A/cm2). The excellent forward conduction is due to the improved injection efficiency obtained by reducing defects at the metallurgical junction via continuous epitaxial growth of the n- drift and p+ injection layers and sufficiently high carrier lifetime (~1 ?Ýsec) allowing the low-doped drift layer to be well conductivity modulated under forward bias. Long term forward voltage stability measurements (constant current density of 100 A/cm2) made on conventionally grown devices show 20% of the diodes remained stable after 50 hr testing. Based on analysis of the long term VF stability data, we have developed an effective short term (30 min constant current stress at 50 A/cm2), on-wafer screening technique that is predictive of long term VF stability. Using this on-wafer screening technique, we find that 86% of the 20 A diodes drifted less than a mere 100 mV using the low BPD process! This is a major step toward commercialization of high power SiC PiN diodes. [1]M.K. Das, ISDRS 2003, Dec 2003, Washington, DC. [2]H. Lendenmann, et al., Mat. Sci. Forum 433-436 (2003) 901. [3]J. Sumakeris, et al., ICSCRM 2003, Oct 2003, Lyon, France.

10:20 AM Student

D2, Influence of Low Field Mobility Related Issues on SiC MESFET Performance: *Ho-Young Cha*[1]; Y. Choi[1]; L. F. Eastman[1]; M. G. Spencer[1]; L. Ardaravicius[2]; A. Matulionis[2]; O. Kiprijanovic[2]; [1]Cornell University, Elect. & Computer Engrg., 401 Phillips Hall, Ithaca, NY 14853 USA; [2]Semiconductor Physics Institute, Vilnius Lithuania

SiC has received tremendous attention due to distinctive material properties. The high saturation velocity, coupled with high breakdown field and high thermal conductivity, amplifies an interest of high power, high frequency applications. SiC metal-semiconductor field-effect transistors (MESFETs), one of promising device types for high frequency applications, have been rapidly developed for a decade, and significant improvements have been accomplished in the development of growth and fabrication technology. To date the highest cut-off frequency achieved in SiC MESFETs is 22 GHz with a gate length of 0.45 µm.[1] However, the saturation velocity derived from the cut-off frequency of fabricated MESFETs is still far lower than predicted values (~ $2x10^7$ cm/s). One of reasons for the degradation of the cut-off frequency could be the self-heating effects resulting from high voltage operating conditions. However, self-heating effects alone cannot account for such an enormous difference. In this work, we investigated the important effects of low field parasitic regions and proposed a modified model to characterize fabricated SiC MESFETs. Tsap et al.[2] and Murray et al.[3] proposed analytical models for SiC MESFETs using a field dependent mobility that plays an important role in both current and frequency characteristics. Nevertheless, these models would lead to inaccurate estimation because they considered only the intrinsic device region. In fact, the parasitic source and drain regions do not have significant effects on current characteristics of GaAs FETs because the drift velocity of GaAs in the low field regions is comparable to its saturation velocity. This results from the velocity overshooting behavior. On the other hand, the velocity-field characteristics of SiC does not have the overshooting behavior, and thus the current density of SiC MESFETs is restricted fundamentally by the low drift velocity in the low field parasitic region between source and gate. The extension of the depletion region toward the drain side, which actually expands the effective channel region, is considerable in high voltage operating FETs. In addition, the unsaturated channel region increases the electron transit time further. Both the extended depletion region toward the drain side and the unsaturated channel region under the gate play an important role in the degradation of cut-off frequency in comparison with the predicted value based on intrinsic models. The proposed 2-dimensional model was verified by comparing simulated results to the measured data of fabricated SiC MESFETs. Both simulated current and frequency characteristics were in good agreement with measured data. [1]S. T. Allen, et al., IEEE MTT-S Digest, 57, (1997). [2]B. Tsap, et al., Solid-State Electron., vol. 38, 1215-1219, (1995). [3]S. P. Murray and K. P. Roenker, Solid-State Electron., vol. 46, 1495, (2002).

10:40 AM

D3, 2.5 kV, 17 mOhms-cm² 4H-SiC JFETs: *Sei-Hyung Ryu*[1]; Sumi Krishnaswami[1]; James Richmond[1]; James Scofield[2]; Anant Agarwal[1]; John Palmour[1]; [1]Cree, Inc, Silicon Carbide Power Devices, 4600 Silicon Dr., Durham, NC 27703 USA; [2]Air Force Research Laboratory, PRPE, 1950 Fifth St., Wright-Patterson AFB, OH 45433-7251 USA

Introduction: Vertical power JFETs in 4H-SiC are very attractive for high power, high temperature switching applications because of their low specific on-resistances, fast switching characteristics, and lack of gate oxide related problems. Several groups have demonstrated normally-off hybrid[1] or monolithic[2,3] switches based on 4H-SiC JFETs. 4H-SiC JFETs are also useful as fault current limiters in a normally-on configuration.[4] In this paper, we present our latest result in normally-on, 2.5 kV 4H-SiC JFET development. The device showed a specific on-resistance of 17 mOhms-cm², which is approximately 117 times lower than the theoretical value for a silicon device. Experimental: A 15 um thick, 4 x 10^{15} cm^{-3} doped n-type epilayer was grown on an n^+, 4H-SiC substrate as the drift layer for the device. P-wells and the floating guard rings were

formed by aluminum implantation, and n^+ source regions were then formed by heavy-dose nitrogen implantations. The implants were activated at 1600°C in silicon overpressure. Then, an undoped epilayer was grown as the lateral channel layer. The channel epilayer was then implanted with nitrogen. A 3000 A thick p^+ epilayer was grown as the top gate. The nitrogen implants were annealed during the epi regrowth. The p^+ and n-channel epilayers were then patterned using a dry etching technique down to n^+ source and p-well implants. A 1.5 um thick PECVD oxide layer was then deposited and densified in dry O_2 as field passivation. After opening the vias, Al/Ni ohmic contacts[5] were formed on the n^+ source, the p-wells, and the p^+ gates regions, while Ni was used to form backside contact. Finally, a 2 um thick Ti/Pt/Au layer was evaporated and lifted-off to form overlayer and probing pads. A pinch-off voltage of -3 V was measured, which indicates approximately 90% activation of the nitrogen implants in the lateral channel regions. The device showed a specific on-resistance of 17 mOhms-cm^2 with a gate bias of 2 V, which was dominated by the lateral JFET resistance. Static and dynamic characteristics of the devices at elevated temperatures will be presented at the conference. This work is supported by AFRL contract # F33615-01-C-2188, monitored by Dr. J. Scofield. [1]P. Friedrichs et al.,: Materials Science Forum Vols. 389-393 (2002), pp. 1185 - 1190. [2]K. Asano et al.,: Proceedings of 13th ISPSD, IEEE, 2001, pp. 23 - 26. [3]J. H. Zhao et al.,: ICSCRM'03, Lyon, France, Oct 5-10, 2003. [4]D. Tournier et al.,: Materials Science Forum Vols. 389-393 (2002), pp. 1243 - 1246. [5]B.-H. Tsao et al.,: ICSCRM'03, Lyon, France, Oct 5-10, 2003.

11:00 AM Student

D4, Characteristics of Trench-Refilled 4H-SiC P-N Junction Diodes Fabricated by Selective Epitaxial Growth: *Canhua Li*[1]; Joseph Seiler[1]; Pete A. Losee[1]; Ishwara B. Bhat[1]; T. Paul Chow[1]; [1]Rensselaer Polytechnic Institute, ECSE Dept. & Ctr. for Integrated Elect., 110 8th St., Troy, NY 12180 USA

There has been significant progress in recent years in the epitaxial growth and device processing of 4H-SiC for use in high power and high temperature electronics. However, there still exist several processing issues to be solved. For example, ion implantation has been used as the only viable means for selective area doping in SiC, as dopant diffusion is extremely slow even at high temperature and fabrication of junctions using epitaxial technology compromises surface planarity. However, the damages introduced by ion implantation and anisotropic diffusion during the annealing are inevitable problems that need to be solved. We have recently reported a new method to realize selective doping of SiC by selective epitaxial growth using a novel high temperature mask. Selective growth and lateral overgrowth techniques have been used successfully in GaN epitaxy, but similar work has not been reported in SiC epitaxy due to the high growth temperature involved. In this work, we have used selective epitaxial growth technique to refill trenches etched on substrates, and to fabricate pn junction diodes. Epitaxial growth of SiC was carried out in a conventional, horizontal cold wall reactor at temperatures in the range 1500-1600°C. Silane and propane are used as the as the precursors with hydrogen as the carrier gas. The wafer used was 12um p-epi/p+-substrate purchased from Cree. The high temperature mask was deposited and pattered using standard photolithography and etched by reactive ion etching (RIE). The etched trench depth was about 1.5µm. The RIE-etched trenches were filled by nitrogen doped n-type epitaxial films grown by selective epitaxy. The nominal planar doping was about 5e16cm3. Each wafer consisted of several diodes with variable perimeter/area ratio (P/A). This will help to evaluate the leakage currents across the bottom surface as well as the vertical side surface. P/A was varied by changing the trench width to masked width ratio and also by changing the overall diode area. Cross sectional scanning electron microscopy (SEM) shows that all trenches were refilled and refilled SiC shows facets that depend on the orientation of trenches. However, when the trench direction is along <1100> direction, refilled SiC surface is even with the original masked surface without edge overgrowth. The extent of selectivity also depended on the C/Si ratio during growth. Forward and reverse current-voltage (IV) measurements were carried out with epitaxial refilled 4H SiC p-n junction diodes. Reverse current density at ?100V is ~10-5A/cm2. Forward and reverse IV is compared to classical planar diodes. In general, carrier recombination takes place in the depletion layer (bulk recombination) as well as on the surface or perimeter of a device. Forward analysis by plotting J0rec of the diodes with different perimeter-area (P/A) ratios, distinguishes the contribution of bulk and surface recombination. Detailed analysis of the diode data is being carried out and will be compared to the conventional diodes. 1. Bhat et al, presented at the ICSCRM2003, Lyon, France, October 5-10, 2003. This work was supported by DARPA Contract #DAAD19-02-1-0246.

11:20 AM

D5, Modifications of 4H-SiC and 6H-SiC(0001) Surfaces by Atomic Hydrogen and Nitrogen for the Epitaxial Growth of GaN: *Maria Losurdo*[1]; Maria M. Giangregorio[1]; Pio Capezzuto[1]; Giovanni Bruno[1]; April S. Brown[2]; Tong-Ho Kim[2]; Changhyun Yi[2]; [1]IMIP-CNR, Plasma Chmst. Lab., Via orabona, 4, Bari 70126 Italy; [2]Duke University, Dept. of Elect. & Computer Engrg., 128 Hudson Hall, Durham, NC 27709 USA

A critical issue in the heteroepitaxy of GaN on SiC substrates is the preparation of SiC surfaces. In this contribution, we present an alternative low-temperature route to prepare clean and ordered 4H- and 6H-SiC(0001)Si surfaces, based on the replacement of RCA+HF with HCl/HF wet etching followed by an in situ exposure to atomic hydrogen at the low temperature of 200°C. As a first step, we compared the conventional preliminary RCA-HF wet etching with a HCl-HF wet etching. By using HCl to change the acidity of the buffered HF etching solution yields more effective oxide removal and hydrogen passivation of the SiC surfaces. This is explained in terms of the polarization of the Si-C bonds, which creates a potential along the [0001] direction that is cancelled to stabilize the crystal by adsorption of negatively charged ions such as OH- and F- present in the buffered HF diluted solutions, while the concentration of this ions is suppressed in HCl acid solutions. Following this preliminary ex-situ wet etch, various in situ cleaning procedures such as Ga flash and anneal at 800°C, and the exposure to atomic hy drogen from a remote r.f. H2 plasma source at various temperatures. It is found that the interaction of SiC surfaces with atomic hydrogen at 200°C is suitable for producing clean, smooth and terraced surfaces with a reconstruction, ideal for GaN heteroepitaxy. The suitability of the 200°C process is explained in terms of the different coverage/sticking coefficient of the atomic hydrogen onto the SiC surfaces depending on temperature. The study of the interaction of the SiC surfaces with atomic nitrogen is interesting since depending on the Si-N bonds configuration at the SiC/GaN or SiC/AlN interfaces a charged layer forms that impacts the structural quality and dislocation density of the GaN layer. Therefore, we have studied the impact of exposing the SiC surfaces to an atomic nitrogen flux during the initial stage of the GaN or AlN growth. The SiC surface charge induced by the hydrogen and nitrogen plasmas affects the structural properties and chemical composition of the SiC/GaN interface. The interplay among the cleaning procedure, the subsequent interaction with atomic nitrogen, the resulting surface charge and GaN nucleation will be discussed and aimed at the optimization of the SiC/GaN interface. We characterized the morphological and chemical modifications of SiC surfaces during exposure to atomic hydrogen and nitrogen in the early stage of GaN growth by various corroborating techniques including spectroscopic ellipsometry, XPS, RHEED, AFM and Kelvin probe microscopy for surface potential. Spectroscopic ellipsometry is used for real timing monitoring of the interaction of SiC with atomic hydrogen and nitrogen, and understanding different surface kinetic processes characterizing the 4H- and 6H-SiC (0001)Si surfaces.

11:40 AM

D6, Development of High Growth Rate (20µm/h) SiC Epitaxy in a Horizontal Hot-Wall CVD Reactor: *Jie Zhang*[1]; Janice P. Mazzola[1]; Jeff Wyatt[2]; Mike S. Mazzola[2]; Jeff Casady[1]; [1]SemiSouth Laboratories, Inc., One Rsch. Blvd., Ste. 201B, Starkville, MI 39759 USA; [2]Mississippi State University, Dept. of Elect. & Computer Engrg., Box 9571, Starkville, MI 39759 USA

SiC possesses enormous potential for applications in high power and high frequency electronics. Especially for megawatt power switching applications, thick (> 50um) and high quality SiC epitaxial layers are required. Although tremendous progress has been made in SiC epitaxy during the past years, growth of thick SiC epilayers remains to be a challenging technology. In this paper we present our efforts on the development of thick SiC epilayers with high growth rate in a horizontal hot-wall CVD reactor. Epilayers grown at 10 - 20 um/h with specular morphology have been obtained. The process developed in the research CVD reactor is scaleable to a larger reactor of the same configuration with 2 ? 3? wafer capacity. Epitaxial growth was performed in a horizon-

tal hot-wall reactor at 400 torr using the H2-SiH4-C3H8 chemical system. Pd-membrane purified H2 carrier flow of 8 to 13 slm was used. The SiH4 flow was in the range of 1.8 sccm to 6 sccm giving a C/Si ratio of 1.5 to 5. A quarter piece cut from a 2? 4H-SiC, 8° off-axis, Si-face substrate was placed in a SiC-coated graphite susceptor. The process developed in a small reactor will be transferred to an up-scaled horizontal hot-wall reactor with 2- 3? wafer capacity. The epilayer thickness was measured by FTIR, and the net carrier concentration was obtained by mercury C-V measurements. The surface morphology was examined in an optical microscope with Nomarski contrast. The growth rate dependencies on the H2 carrier flow rate, the SiH4 flow rate and the growth temperature were investigated. Our initial experiments show that a slight increase of H2 carrier flow from 11.4 slm to 12 slm pushes the growth rate at the upstream region from 7 um/h to 10.5 um/h, while the downstream growth rate has increased from 3.2 um/h to 5 um/h. Increasing SiH4 flow rate is also very efficient in increasing the growth rate. An increase of SiH4 flow by 10% raises the growth rate by almost 50% (from 14 um/h to 20 um/h) for the upstream region of the substrate, while the downstream growth rate does not increase with the SiH4 flow rate. The above preliminary experimental results have shown the feasibility of reaching high growth rates of 10 ? 20 um/h in a horizontal hot-wall system. The background doping is n-type in the high 1014 to low 1015 cm-3 range, and the morphology is smooth even at these high growth rates. The growth rate uniformity can be greatly improved by careful adjustment of growth p arameters. Significant improvement in growth rate uniformity is also expected in the up-scaled CVD system currently under construction. The results from the up-scaled system will be added to the full paper.

Session E: Nitride HEMTs: Transport and Devices

Wednesday AM Room: 155
June 23, 2004 Location: DeBartolo Hall

Session Chairs: James S. Speck, University of California, Dept. of Matls., Santa Barbara, CA 93106 USA; Michael Manfra, Lucent Technologies, Bell Labs., Murray Hill, NJ 07974 USA

10:00 AM

E1, A Study of AlGaN/GaN Heterostructures on Silicon: *S. Elhamri*[1]; R. Berney[1]; M. Ahoujja[1]; W. C. Mitchel[2]; W. D. Mitchell[2]; J. C. Roberts[3]; P. Rajagopal[3]; T. Gehrke[3]; E. L. Piner[3]; K. J. Linthicum[3]; [1]University of Dayton, Dept. of Physics, 300 College Park, Dayton, OH 45469 USA; [2]Air Force Research Laboratory, Matls. & Mfg. Direct., Wright-Patterson AFB, OH 45433-7707 USA; [3]Nitronex Corporation, 628 Hutton St., Ste. 106, Raleigh, NC 27606 USA

Due to their superior electrical and optical properties, AlGaN/GaN heterostructures are being actively studied by many semiconductor research groups. Sapphire and silicon carbide are the two most commonly used substrates for the growth of this heterostructure. However, silicon is being sought as an alternative substrate for the nitrides. Silicon offers some important advantages; namely, high quality, large size wafers and very low cost. The ability to successfully deposit device quality AlGaN/GaN on a silicon substrate would be a major achievement and holds much promise for electronic device development. We report on a study of magnetotransport properties of high quality AlGaN/GaN heterostructures grown on silicon substrates. To characterize these structures, we performed three different types of measurements. First, variable temperature Hall effect measurements revealed that the temperature dependence of the mobility is characteristic of a two dimensional electron gas. Carrier Hall mobilities in excess of 1500 cm^2/Vs and carrier densities larger than 1 x 10^{13} cm^{-2} were measured at room temperature. Second, variable field Hall measurements at low temperatures showed conduction dominated by a single carrier type. Third, Shubnikov-de Haas (SdH) measurements were performed in fields up to 8 T and in temperatrues as low as 1.2 K. These measurements revealed the existence of well-defined Shubnikov-de Haas oscillations, which is further evidence of the presence of a high quality two dimensional electron gas in these structures. These oscillations became visible only after the samples were exposed to radiation from an ultraviolet light emitting diode (LED) (395 nm). Radiation from a blue LED (470 nm) also resulted in a persistent photocurrent at low temperature, but did not lead to the observation of SdH oscillations. This behavior was also observed in some AlGaN/GaN samples grown on sapphire and on silicon carbide. The observed persistent photocurrent in these heterostructures on silicon allowed us to study the dependence of the mobility on the carrier density and the dependence of the ratio between the classical and quantum scattering times to investigate the dominant scattering mechanisms in these structures. Our results suggest that small angle scattering is the main scattering mechanism suppressing the SdH oscillations prior to UV illumination. Further details of our study will be presented.

10:20 AM

E2, Quantum Transport in a Tunable AlGaN/GaN Two-Dimensional Electron Gas: *Michael James Manfra*[1]; Kirk Baldwin[1]; A. M. Sergent[1]; R. J. Molnar[2]; [1]Bell Laboratories, Semiconductor Physics Rsch., 700 Mountain Ave., 1D-368, Murray Hill, NJ 07974 USA; [2]MIT Lincoln Laboratory, Lexington, MA USA

We report on the transport properties of a tunable two-dimensional electron gas (2DEG) confined at the lower interface of a GaN/$Al_{0.06}Ga_{0.94}N$/GaN heterostructure grown by molecular beam epitaxy on semi-insulating GaN templates prepared by hydride vapor phase epitaxy. Using an insulated gate Hall bar structure, the electron density is continuously tuned from ~ 2x$10^{12}$$cm^{-2}$ down to 1.5x$10^{11}$$cm^{-2}$, thereby reducing the measurable 2DEG density by a factor of 10 over previously reported results. At T=300mK, the 2DEG displays a maximum mobility of 80,000cm^2/Vs at a sheet density of 1.75x$10^{12}$$cm^{-2}$. At lower densities, the mobility exhibits a power law dependence on density- ~ n_e^{α}, with α~ 1.0, over the range of 2x$10^{11}$$cm^{-2}$ to 1x$10^{12}$$cm^{-2}$. In this density regime, the mobility is no longer limited by alloy and interface roughness scattering. Long-range Coulomb scattering from charged dislocations dominates. The 2DEG remains metallic at a density of 1.5x$10^{11}$$cm^{-2}$ at T=300mK. We also compare the density dependence of the transport lifetime (τ_t) obtained from low field Hall measurements and the quantum lifetime (τ_q) derived from analysis of the amplitude of Shubnikov-de Haas oscillations in the density range of 2x$10^{11}$$cm^{-2}$ to 1.75x$10^{12}$$cm^{-2}$. The transport lifetime τ_t is a strong function of electron density, increasing from ~2.7ps at n_e=2x$10^{11}$$cm^{-2}$ to ~11ps at n_e=1.75x$10^{12}$$cm^{-2}$. Conversely, we find that the quantum scattering time τ_q is relatively insensitive to changes in electron density over this range. The ratio τ_t / τ_q displays a much weaker dependence on density than is expected for scattering produced by remote ionized impurities. The functional dependence of τ_t / τ_q is consistent with a recently proposed model of scattering produced by charged dislocations.[1] Finally we discuss our study of weak localization and antilocalization corrections to the classical conductivity at very low magnetic fields. It has recently been proposed that GaN is a candidate system for spintronic applications. In order to evaluate this claim, we use weak localization measurements to extract the relevant scattering times as a function of 2DEG density. We report on our measurements of the dephasing time τ_ϕ and the spin-orbit scattering time τ_{so} as a function of 2DEG density. [1]D. Jena et al. Phys. Rev. B 66, 241307 (2002).

10:40 AM

E3, Use of Modulation Doped Superlattice AlGaN Barrier in GaN/AlGaN HFETs: *Uttiya Chowdhury*[1]; Raymond Kirk Price[2]; Michael M. Wong[3]; Dongwon Yoo[1]; Xuebing Zhang[1]; Milton Feng[2]; Russell D. Dupuis[1]; [1]Georgia Institute of Technology, Sch. of Elect. & Computer Engrg., 778 Atlantic Dr., Atlanta, GA 30332-0250 USA; [2]University of Illinois, Micro & Nanotech. Lab., 208 N. Wright, Urbana, IL 61801 USA; [3]University of Texas, Microelect. Rsch. Ctr., 10100 Burnet Rd., Austin, TX 78758 USA

Of the III-nitride based electronic devices, heterostructure FETs are probably the closest to commercial realization because of industrial interest in the device and advanced stage of the technology. One of the key areas of improvement in the technology is the heterojunction forming the electron barrier, which has to be designed based on trade-offs between lattice mismatch, 2-DEG concentration and alloy scattering. In this work, we report on the first use of a superlattice structure for improvement of barrier properties in a GaN/AlGaN HFET. We have studied

the use of a superlattice based electron barrier which effectively increases the energy barrier while reducing the lattice mismatch and alloy scattering. The device structure was grown by low-pressure MOCVD using a high-temperature AlN nucleation layer on a 6H conducting n-type SiC substrate. The precursors used for the growth were trimethylgallium (TMG), trimethylaluminum (TMA), ammonia (NH_3) and silane (SiH_4). A growth pressure of 200 Torr and temperature of ~1050C was used to grow the GaN layer while the AlN nucleation layer and the AlGaN superlattice was grown at a reduced pressure of 50 Torr and a temperature of ~1070C. After the growth of a thick undoped GaN layer, a 5 period superlattice consisting of 2 nm $Al_{0.3}Ga_{0.7}N$ barrier and 2 nm $Al_{0.2}Ga_{0.8}N$ well was grown. The second and third periods of the superlattice are Si-doped to give the effect of modulation doping. Room temperature Hall-effect measurement on the structure yielded a high sheet concentration of 2.46 x 10^{13} /cm^3 and a mobility of 10^{18} cm^2 /V-sec. In order to determine depletion properties and profile the 2DEG, capacitance-voltage(C-V) measurement using a mercury point C-V system was performed. Low frequency capacitance-voltage (C-V) measurement on five different points on the wafer showed a uniform threshold voltage of ~4V and very good pinch-off characteristics. The 2DEG was determined to be at the GaN-superlattice interface. Transmission line measurement (TLM) was used to determine the contact resistance of the structure. The results showed a very low contact resistivity of 0.088 Ω-mm. The sheet resistivity measured by the same technique was ~222 Ω /square which is consistent with contactless resistivity map data obtained from similar structures grown on 4H insulating SiC substrate. Standard processing techniques were used to fabricate HFET devices from the epitaxial wafers. Under DC measurement conditions, these devices exhibit a high Gm of ~212 and a relatively high $I_{ds\ max}$ of 0.83 A/mm. In addition, the devices show a significant reduction in knee voltage (knee voltage ~ 4V) in the family of curves. To our knowledge, this is the first investigation of the use of superlattice structure for improvement of barrier properties in an HFET.

11:00 AM Student

E4, SiC Substrate Inclusions and Their Impact on AlGaN/GaN HEMT Performance: *Benjamin Poust*[1]; Rajinder S. Sandhu[1]; Benjamin Heying[2]; Ioulia Smorchkova[2]; Randy Hsing[2]; Michael Wojtowicz[1]; Mark S. Goorsky[1]; [1]University of California, Matls. Sci. & Engrg., 6531 Boelter Hall, 405 Hilgard Ave., Los Angeles, CA 90095-1595 USA; [2]Northrop Grumman Space Technology, Space & Elect. Grp., Redondo Beach, CA 90278 USA

Large inclusions in semi-insulating SiC substrates are shown to impact the performance of AlGaN/GaN HEMT devices, and the nature of the impact depends upon the structure of the inclusion. AlGaN/GaN HEMT structures were deposited by MBE using low temperature AlN nucleation layers on 3" SiC substrates with large (~1 cm^2) foreign polytype inclusions. Prior to HEMT deposition, the inclusions were visible to the unaided eye, appearing less transparent than the surrounding SiC material. Optical birefringence imaging (OBI) using polarizers, high resolution x-ray diffraction, and double crystal x-ray diffraction imaging (DCDI) show the substrate inclusions to consist of heavily distorted material, some polycrystalline, oriented away from the nominally [0001] surface by several degrees. Strain in the SiC adjacent to the inclusions is observed with both the OBI and DCDI techniques. The inclusions appeared less transparent following HEMT deposition, indicating enhanced visible absorption in the layers attributed to the presence of mid-gap states. Diffraction from the GaN over the inclusions is not typically observed in x-ray diffraction images showing strong diffraction from the surrounding GaN, suggesting heavy distortion or misorientation of the material deposited on an inclusion. Large increases in 2DEG sheet resistance over the inclusions were observed in both non-contact resistivity measurements and four point probe measurements taken over a large distribution of patterned test structures. Substantial drops in unity gain cut-off frequencies were observed in HEMT devices patterned over the inclusions, whereas high frequencies were measured over the wafer that did not contain inclusions. Despite the use of a low temperature AlN nucleation layer which might be expected to mask defects in the underlying substrate, it appears that inclusions in SiC promotes growth of highly defective HEMT structures with introduced mid-gap states and a large decrease in carrier mobility. One particularly large inclusion was observed to grow much less transparent upon deposition of the HEMT structure, such that the inclusion had become visible to the unaided eye. DCDI showed the SiC inclusion to be distorted, but largely crystalline. A network of cracks and dislocations with nearly equilateral triangular symmetry was observed under diffuse light and with IR transmission imaging following HEMT deposition. X-ray diffraction measurements and DCDI show the GaN, like the inclusion above which it was grown, to be oriented at least several degrees away from the remainder of the wafer. Non-contact resistivity maps show large increases in sheet resistance along the inclusion border correlating well with strain in the SiC and hexagonal GaN adjacent to the inclusion. Above the center of the inclusion, however, the sheet resistance measured was significantly lower than that of the hexagonal material located far from the inclusion.

11:20 AM

E5, Suppression of Gate Current Leakage in AlGaN/GaN MIS-HFETs with Ultrathin Al_2O_3/Si_3N_4 Bilayer Insulator: *C. X. Wang*[1]; N. Maeda[1]; M. Hiroki[1]; T. Tawara[2]; T. Saitoh[2]; T. Makimoto[2]; T. Kobayashi[1]; T. Enoki[1]; [1]NTT Incorporation, NTT Photonics Lab., 3-1, Morinosato, Wakamiya, Atsugi, Kanagawa 243-0198 Japan; [2]NTT Incorporation, NTT Basic Rsch. Lab., 3-1, Morinosato, Wakamiya, Atsugi, Kanagawa 243-0198 Japan

Nitrides-based heterostructure field effect transistors (HFETs) have been studied extensively because of their importance for high-power high-frequency applications in recent years. Metal-insulator-semiconductor (MIS) structures, using relatively thick SiO_2, Si_3N_4 or TiO_2 insulator, have been developed to significantly reduce the gate current leakage and suppress the current collapse in nitrides-based HFETs at the expense of the reduction in transconductance for which ultrathin insulator is desirable. We have proposed a novel MIS structure using bilayer Al_2O_3/Si_3N_4 insulator previously[1]. In this work, MIS-HFET with ultrathin Al_2O_3/Si_3N_4 insulator has been developed and investigated in detail. AlGaN/GaN-based device structure was grown on sapphire (0001) substrates with GaN buffer layer using low pressure metal-organic vapor phase epitaxy (MOVPE) system. The $Al_{0.3}Ga_{0.7}N$ barrier consisted of 3nm undoped space layer, 11nm Si-doped layer (4x$10^{18}$$cm^{-3}$) and 4nm undoped layer for Schottky contact. Devices had the gate configuration of 1.5µmx20µm and drain-source spacing of 5µm. Insulators were deposited at room temperature using ECR-plasma system prior to the gate fabrication. Two Al_2O_3/Si_3N_4 bilayer insulators were used in this study, composed of Si_3N_4 as interlayer with fixed thickness of 0.5nm and Al_2O_3 layer with different thickness of 2.5nm or 8nm. Conventional HFET without insulator and MIS-HFET with 10nm of widely used Si_3N_4 insulator were also studied for comparison. The gate leakage current in Al_2O_3/Si_3N_4 MIS-HFET was found lower than that of the conventional HFET by approximately four orders of magnitude, with 2.5x10^{-10}A/mm at -30V, even using ultrathin Al_2O_3/Si_3N_4 (2.5nm/0.5nm) bilayer. No apparent current collapse was observed in two Al_2O_3/Si_3N_4 MIS-HFET samples in the small frequency (120Hz) sinusoidal wave superimposed DC measurements, demonstrating the good passivation effect of Al_2O_3/Si_3N_4 insulators. Under the condition of low current leakage less than 1x10^{-6}A/mm at V_{DS}=0V, gate voltage in MIS-HFET can be applied up to 2.5V by using ultrathin Al_2O_3/Si_3N_4 (2.5nm/0.5nm) bilayer, higher than 1.5V in the conventional HFET, because of high quality of Si_3N_4AlGaN interface and the large bandgap offset between Al_2O_3 and nitrides. This voltage increased to 3.5V by using thicker Al_2O_3/Si_3N_4 (8nm/0.5nm) bilayer, higher than 3.0V in MIS-HFET with 10nm of Si_3N_4 insulator. Maximum drain current in Al_2O_3/Si_3N_4 MIS-HFETs was up to 40% higher than the conventional HFET. Maximum transconductance of 140mS/mm was achieved in Al_2O_3/Si_3N_4 MIS-HFETs. This work indicates that ultrathin Al_2O_3/Si_3N_4 bilayer insulator is a superior candidate for gate leakage and current collapse suppression in AlGaN/GaN MIS-HFET. [1]N. Maeda, T. Tawara, T. Saitoh, K. Tsubaki and N. Kobayashi Phys. Stat. Sol.(a) 200(2003)168.

11:40 AM E6, Late News

Session F: Materials and Structures for Chemical and Biological Sensors

Wednesday AM Room: 126
June 23, 2004 Location: DeBartolo Hall

Session Chairs: Thomas F. Kuech, University of Wisconsin, Dept. of Chem. Engrg., Madison, WI 53706 USA; Laura Rea, US Air Force Research Laboratory, Wright Patterson AFB, OH 45433-7707 USA

10:00 AM

F1, Fabrication of a Solid-State Single Nanopore for DNA Characterization: *Hung Chang*[1]; [1]Purdue University, Sch. of Elect. Engrg., 465 Northwestern Ave., PO 103, W. Lafayette, IN 47907-1285 USA

Characterizations of biological entities by a single pore have been of interest in recent years. Alpha-hemolysin, a protein-based channel, has been used to electrophoretically transport single strands of DNA, and offers the potential to perform direct sequencing.[1,2] A solid-state micropore has been utilized to characterize bacteria.[3] However, pores in scale of a few nanometers have to be realized to address the characterizations of DNA and the related nucleic acids.[4,5] We have performed the fabrication of silicon-based nanopores made on an SOI wafer using processes of e-beam lithography and TEM, as also described in [5]. In this paper, we will report the fabrication processes, the analysis of the fabrication parameters and the preliminary results of DNA measurements. We will also present an update on future work on integration of novel sensors for DNA sequencing. The fabrication started with a double-sided polished SOI wafer with 140nm SOI and 400nm buried oxide. The wafer was etched through from the back side, and the etch process stopped on the buried oxide layer. There thus remained a thin diaphragm form by the SOI and buried oxide layers. E-beam lithography was then performed on the thin diaphragm to open etch windows of 100 nm in diameter. An anisotropic wet etch of silicon was used to form a pyramid-shaped cavity in the SOI layer, and to open a pore, few tens of nanometers wide, on the buried oxide layer. After the buried oxide layer was removed, thermal oxide was grown to shrink the pore below 50 nm. The final step was to make the nanopore by shrinking the 50 nm pore in TEM, while the pore was being inspected. Pore size could be controlled as accurately as one nanometer with an in-situ TEM observation. The nanopores could be thus precisely fabricated between 3 to 5 nm so far in our case. We will present experiment results of the fabrication and the initial measurements of translocations of dsDNA through a single nanopore. Our future goal is to develop an integrated micro-machined system with a nanopore and fluidic channels to directly and electrically characterize DNA. [1]J. J. Kasianowicz et al., Proc. Natl. Acad., Vol. 93, November 1996, pp. 13770-13773. [2]A. Meller et al., Electrophoresis, Vol.23, pp. 2583-2591. [3]H.Chang et al., Journal of Vacuum Science & Technology B. Vol. 20, September/October 2002, pp. 2058-2064. [4]J. Li et. al., Nature, Vol. 412, July 2001, pp.166-169. [5]A. J. Storm et al, Nature Materials, Vol. 2, August 2003, pp. 537-540.

10:20 AM

F2, Chemical Sensing Properties of Modified Silicon Surfaces: *Brian J. Eves*[1]; Tim R. Ward[1]; Steve A. Mitchell[1]; Gregory P. Lopinski[1]; [1]National Research Council, Steacie Inst. for Molecular Scis., 100 Sussex Dr., Ottawa, Ontario K1A 0R6 Canada

We are exploring the use of chemically modified silicon for electrical monitoring of adsorption and surface reactions. Adsorption of charged species or changes in charge state of surface bound species induce band bending, resulting in changes in surface conductivity. Atomically flat hydrogen terminated Si(111) are used as the starting point for producing surfaces terminated with halogens as well as with a wide range of organic functional groups (methyl, acid, ester, amino, hydrazide, etc.). The structure and chemical composition of these surfaces have been characterized by a number of surface science techiques (STM, HREELS, XPS). Electronic properties are studied via surface photovoltage, surface conductivity and non-linear optical measurements. Stable monolayers with a low density of electrically active defects (<10^11 cm^-2) can be prepared. Surfaces modified with tert-butylhydrazide show a large reversible increase in surface photovoltage upon exposure to oxygen or iodine. These changes are attributed to spontaneous and photoinduced ionization of species trapped in the film which results in substantial band bending in the silicon substrate. This band-bending effect is sufficient to result in a substantial second harmonic response and a change in surface conductivity. In contrast to the hydrazide monolayers, the halogen (Cl, Br) termination of low doped Si(111) n-type surfaces creates an inversion layer at the surface which is confirmed by Hall effect measurements. In-situ monitoring of the halogenation reaction has led to the identification of optimal conditions for preparing high-quality halogen terminated surfaces. Exposure to various molecules (nitrogen, water, methanol, pyridine, and triethylamine) induce significant reversible changes in conductivity indicating that physisorbed species can strongly modulate the conductance of this inversion layer.

10:40 AM

F3, Applications of Dielectrophoretic "Tweezers" in Determining the Biological Receptor-Ligand Interaction Forces and Selectively Removing Different Species in Biochips: *Haibo Li*[1]; Rashid Bashir[2]; [1]Purdue University, Elect. & Computer Engrg., 1285 EE Bldg., Mailbox 358, W. Lafayette, IN 47907 USA; [2]Purdue University, Sch. of Elect. & Computer Engrg., Dept. of Biomed. Engrg., 465 Northwestern Ave., EE322B, W. Lafayette, IN 47907 USA

The importance of specific receptor-ligand interaction forces in biology has been recognized for many years but only in the past decade have these kinds of forces been studied at the level of a few macromolecules with atomic force microscopy (AFM), which still requires sophisticated instrumentation and delicate treatment. It is well-known that biological particles can experience dielectrophoretic force when placed in a non-uniform electrical field. In this study, we use dielectrophoresis (DEP) as novel "tweezers" to simply determine the interaction forces between various receptor/ligands, such as poly-L-lysine/carboxyl, poly-L-lysine/dimethylamine, and antigen/antibody interactions. The DEP tweezers can also be used to remove different particle species from the binding sites according to the different binding strengths in the biochips. A micro-device was fabricated in silicon substrate with interdigitated electrode array. The electrodes were covered with PECVD silicon dioxide as the insulating layer to minimize electro-hydrodynamic effects. Detailed characterization of the DEP forces on the particles was performed by finite element modeling and confirmed with experiments. The surface of the device was treated and specific molecules were immobilized to bind the interacting partners, which were either coated on polystyrene beads, or present on bacterial surfaces (antigens). An experimental protocol was then used, which involved choosing a proper AC signal frequency and the measurement of the voltage necessary to unbind the particles from the binding sites. The total unbinding forces were calculated and the density of the binding sites on the beads or bacteria was assumed to obtain the single-event receptor-ligand interaction force. Experimentally determined levitating voltages of different beads (functionalized with charge molecules) on uncoated device surfaces are close to the simulated values. However, when charged beads are used with charged surfaces, the results are very different. Carboxyl group provides a negative charge on the surface of the bead and hence gets electrostatically attached to the positively charged poly-L-Lysine surface of the chip, as evident by the fact that a large number of beads are still not removed, even at very high voltages. Dimethylamine groups provide a positive charge on the beads and thus it is possible to remove all the beads from the positively charged surfaces. This technique of DEP "tweezers" can also be used to selectively remove different particle species from specifically functionalized regions in the biochips according to their different binding strengths, hence very useful in removal of non-specifically bound entities within a biochip.

11:00 AM Student

F4, Self-Assembled Protein Nanopatterns: *Bo Gao*[1]; Wenchuang Hu[2]; Gary H. Bernstein[2]; Marya Lieberman[1]; [1]University of Notre Dame, Dept. of Chmst. & Biochmst., Notre Dame, IN 46556 USA; [2]University of Notre Dame, Dept. of Elect. Engrg., Notre Dame, IN 46556 USA

The spatially controlled immobilization of proteins onto surfaces with well-defined feature size, shape, and spacing has attracted much attention recently. Such protein nanoarrays are important for the funda-

mental study of the interactions between protein and surfaces and have potential applications in the design of protein-based sensors and biomaterials. We propose to make protein nanopatterns on silicon substrates by molecular lift off. The lift off technique has been adapted for deposition of monolayer films of molecules. Our method involves the fabrication of nanopatterns of a self-assembled monolayer (SAM). Patterns on silicon substrates are defined by e-beam lithography in PMMA resist. The SAM displays chemical functionalities which act as adhesion providers for the desired protein. After liftoff of the PMMA and passivation of the unpatterned region, proteins are selectively adsorbed on to the chemically functionalized areas. A cold cathode field emission EBL system and the use of a cold development technique enable us to define patterns with sub-10 nm feature size and therefore enable us to pattern single nanoparticles or protein molecules. Surface characterization results of such protein nanostructures will be reported from AFM, ellipsometry, XPS and reflective IR measurements.

11:20 AM Student

F5, Electrical Detection of DNA Hybridization Using Nano-Gap Gold Break-Junctions: *Samir M. Iqbal*[1]; Ganesan Balasundaram[2]; Subhasis Ghosh[3]; Donald E. Bergstrom[2]; Rashid Bashir[1]; [1]Purdue University, Sch. of Elect. & Computer Engrg., 465 Northwestern Ave., W. Lafayette, IN 47907-1285 USA; [2]Purdue University, Dept. of Medicinal Chmst. & Molecular Pharmacology, Arthur E. Hansen Bldg., W. Lafayette, IN 47907 USA; [3]Jawaharlal Nehru University, Sch. of Physical Scis., New Delhi 110067 India

There have been numerous publications in recent years aiming towards single-molecule manipulation with the potential of characterization of biological processes at the molecular scale. Most of the current techniques are based on microscopic methods requiring sophisticated equipment and usually handle only one molecule at a time. We have used a simple approach of electromigrated break junctions to achieve parallel manipulation of DNA molecules. The IV characteristics of DNA molecules have been studied. The molecule lengths were in the nanometer range, attached to electromigrated Au break junctions via thiol groups. The aim of the study was to characterize the electrical behavior of the hybridization and denaturing of double strand DNA (ds-DNA). The ds-DNA denatures at a certain melting temperature (Tm) resulting in two single strand DNA (ss-DNA) and potentially reduced conduction. In organic molecules, increasing temperature increases the current through molecule, whereas due to denaturing phenomenon increasing the temperature to Tm and beyond should decrease the current through the DNA molecule. The break junctions were made on 200Å Au patterned film evaporated on a 25Å Ti adhesion layer on SiO_2/Si substrate. Nanoscale breaks in the thin Au film were made with electromigration upon a voltage stress of up to 10 volts at room temperature in air. The Au strips had narrow central regions of 3-4 micron width, to ensure break occurred in the center. Au pads were evaporated at the edges of the strips for probing. Thin films of Au are reported to have peculiar properties under various conditions e.g. the electromigration under electrical stress, temperature, humidity and ambient effects. It has been observed that all these conditions need to be optimized to achieve break-junctions at nanoscale and for proper DNA docking. After electromigration, the chips were incubated in 6µM concentration of DNA strands (upto 18 mer long) in 600µL buffer volume. The incubation was done for 72 hours in Nitrogen ambient. The chips were rinsed in buffer solution, dried and conduction through the electrode-DNA-electrode complex was measured at increasing temperatures. Post-incubation temperature measurements were carried out in vacuum. Control strands at same concentration were used which did not have thiol groups at the ends. The control chips underwent the same processing as described. Initial results show that a decrease in current was observed at temperatures above Tm, indicating some level of denaturing of the DNA bases. Subsequent incubation of the chip with denatured ss-DNA in buffer solution showed re-naturing of the ss-DNA. Further process details and experimental results will be presented in the presentation.

11:40 AM Student

F6, High Temperature Hydrogen Sensors on GaN and AlGaN/GaN Heterostructures with Different Catalytic Metals: *Junghui Song*[1]; Jeffrey S. Flynn[2]; George R. Brandes[2]; Wu Lu[1]; [1]Ohio State University, Dept. of Elect. Engrg., 205 Dreese Labs., 2015 Neil Ave., Columbus, OH 43210 USA; [2]ATMI, Danbury, CT 06810 USA

Since the first semiconductor gas sensor was developed, growing demands have fueled the research and development of advanced gas sensors in harsh environments. Devices based on group III-nitride semiconductors are one of leading candidates for high temperature applications due to the large band gap. Moreover, since the Fermi level is not pinned in III-nitride films, devices based on these materials are ideal for gas sensing applications. Especially, the two-dimensional electron gas (2DEG) at AlGaN/GaN interface can be modulated by the change of surface states[1]. Therefore, devices fabricated on AlGaN/GaN heterostructures have great potentials for gas sensing at high temperatures. In this paper, we report results of Schottky diodes and field effect transistors (FETs) on GaN and AlGaN/GaN heterostructures for hydrogen sensing at high temperatures. Shottky diodes and FETs with different catalytic metals on GaN and AlGaN/GaN heterosturctures were fabricated. To minimize the degradation of ohmic contac ts due to oxidation, Si_3N_4 thin film was deposited and vias were used for wire-bonding and gas sensing. The devices were post-annealed in a furnace to suppress the gate leakage current[2]. Samples were wire-bonded and mounted on a ceramic plate for gas sensing measurements at high temperatures. Gas sensing tests were performed over a wide range of temperatures from room temperature to 800°C in 5% H2/95% Ar. For Pt/AlGaN/GaN Shottky diodes, the results show that these devices can be operated over a large temperature range from 100°C to 800°C. At a forward bias of 1.5 V, the sensitivity increases significantly as the temperatures increases from 0.37 at 100°C to 12.09 at 400°C. The sensitivity decreases to 0.5 at 600°C under the same bias. However, these devices showed great sensitivities at high biases, e.g. at 600°C the current increases from 24.9 mA in Ar to 31.6 mA in 5% H2/95% Ar at a bias of 15 V. The comparative studies of Schottky diode s and FETs on GaN and on AlGaN/GaN heterostructures with different catalytic metals including Pt, PdAg, and IrPt will also be presented. The sensing mechanism and device degradation issues at high temperatures will be discussed. This work is supported by National Science Foundation. [1]Z. Lin, W. Lu, J. Lee, D. Liu, J. S. Flynn, and G. R. Brandes, ¨Barrier heights of Schottky contacts on strained AlGaN/GaN heterostructures: determination and effect of metal work functions¨, Appl. Phys. Lett., vol. 82, pp. 4364 ¨C 4366, 2003. [2]Z. Lin, H. Kim, J. Lee, and W. Lu, ¨Thermal Stability of Schottky Contacts on Strained AlGaN/GaN Heterostructures¨, Appl. Phys. Lett., vol. 84, Feb. 2004 (in press).

Session G: Nanocharacterization I (Advanced Electron Microscopy)

Wednesday AM June 23, 2004 | Room: 129 Location: DeBartolo Hall

Session Chairs: Rachel S. Goldman, University of Michigan, Dept. of MSE, Ann Arbor, MI 48109-2136 USA; Julia W.P. Hsu, Sandia National Laboratories, Albuquerque, NM 87112-1415 USA

10:00 AM Invited

G1, Nanoscale Control of Epitaxial Quantum Dot Assembly in Ge(Si)/Si Heteroepitaxy: Surajit Atha[1]; Jennifer Gray[1]; Martin Kammler[1]; Alan Kubis[1]; Alain Portavoce[1]; Tom Vandervelde[2]; John C. Bean[2]; *Robert Hull*[1]; Frances Ross[3]; Jerry Floro[4]; [1]University of Virginia, Matls. Sci., 116 Engineers Way, Charlottesville, VA 22904 USA; [2]University of Virginia, Dept. of Elect. & Computer Engrg., Thornton Hall, Charlottesville, VA 22904 USA; [3]IBM Yorktown Heights Research Center, Yorktown Heights, NY USA; [4]Sandia National Laboratories, Albuquerque, NM USA

Heteroepitaxial growth of quantum dot (QD) clusters has been an active area of recent research. Significant progress has been made in the fundamental understanding of heteronucleation phenomena, and in the organization of QDs into single spatial frequency ordered arrays via strain field interactions. However, application of semiconductor QDs to many potential nanoelectronic architectures, for example quantum cellular automata (QCAs), requires organization of QDs into non-periodic

patterns. We report on successful applications of methods for pre-programming of Si(100) substrates for subsequent epitaxial growth of Ge(Si) QDs in patterns of arbitrary complexity Application of advanced nanoscale characterization techniques provides critical insight into these "programmed assembly" phenomena. First, we report upon three-dimensional tomographic techniques using focused ion beam (FIB) reconstruction methods to track the three-dimensional assembly of QD arrays in the Ge(Si)/Si system. Following the breakthroughs of Tersoff, Lagally, Bean and co-workers, it is known that the interaction of strain fields can drive single spatial frequency ordering of QD arrays in the growth of layered QD superlattices. In this work, we present new techniques enabling FIB tomographic reconstructions of the 3D distributions of such QD arrays, providing substantial new insight into this strain-mediated ordering phenomenon. We also describe new techniques for the aperiodic ordering of epitaxial QDs upon nano-patterned substrates. In the first approach, a Ga+ focused ion beam is used to pre-determine Ge nucleation sites upon a Si(100) substrate using a unique transmission electron microscope (TEM) that is equipped with ultra high vacuum chemical vapor deposition capabilities and an integrated FIB source. We show that ultra-low dose (<10e14 cm-2), high frequency (10e4 features/s) Ga+ implants into clean Si(100) surfaces, followed by annealing, allow nanoscale control of the nucleation of Ge epitaxial quantum dots into arbitrarily complex patterns. This localization phenomenon involves modification of surface energetics and localized strain/damage centers arising from the Ga+ implant. In a separate approach, we describe the self-assembly of "quantum dot molecules" (QDMs) in the Ge(x)Si(1-x)/Si(100) system. These QDMs have been observed by us in a relatively limited range of kinetically-limited growth conditions, and comprise QD quadruplets forming on the edges of {511}-faceted pits that form spontaneously during epitaxial growth of the Ge(x)Si(1-x) film to reduce lattice-mismatch strain energy. These QDM structures form randomly on unpatterned surfaces, but can be forced into controlled patterns by creating FIB topography of appropriate dimensions and symmetries to match the QDM dimensions. This work was supported at UVa by the NSF-MRSEC on "Nanoscopic Materials Design" and an NSF-FRG DMR-0075116. This work was partially supported by the DOE Office of Basic Energy Sciences. Sandia is a multiprogram laboratory of the United States Department of Energy operated by Sandia Corporation, a Lockheed Martin Company, under contract DE-AC04-94AL85000.

10:40 AM Invited

G2, Direct Observation of Charge Transfer at a MgO(111) Surface: Arun Subramanian[1]; *Laurence Marks*[1]; Oliver Warschkow[2]; Don Ellis[2]; Peter Blaha[3]; [1]Northwestern University, Matls. Sci., 2225 N. Campus Dr., Evanston, IL 60201 USA; [2]Northwestern University, Dept. of Physics & Astron., Evanston, IL 60201 USA; [3]TU Vienna, Inst. f. Matls. Chmst., A-1060 Vienna Austria

Transmission Electron Diffraction (TED) combined with Direct Methods have been used to study the √3x√3R30 reconstruction on the polar (111) surface of MgO and refine the valence charge distribution. The surface is non-stoichiometric and is terminated by a single magnesium atom. A charge-compensating electron hole is localized in the next oxygen layer and there is a nominal charge transfer from the oxygen atoms to the top magnesium atom. The partial charges that we obtain for the surface atoms are in reasonable agreement with empirical bond-valence estimations. More accurate all-electron LAPW calculations confirm the experimental results, and indicate additional near-surface polarization of density around some of the oxygen atoms. Similar phenomena may well occur at bulk interfaces with oxides.

11:20 AM Invited

G3, Nanoscale Characterization of Epitaxial Cu_2O Films Made by Electrodeposition: Fumiyasu Oba[1]; Run Liu[2]; Yeonseop Yu[1]; Eric Bohannan[2]; *Frank Ernst*[1]; Jay Switzer[2]; [1]CASE, Matls. Sci. & Engrg., 10900 Euclid Ave., Cleveland, OH 44106-7204 USA; [2]University of Missouri, Dept. of Chmst. & Grad. Ctr. for Matls. Rsch., 103 Matls. Rsch. Ctr., Rolla, MO 65409-1170 USA

By electrochemical deposition from aqueous solutions at room temperature, single-crystalline, epitaxial films of Cu2O (cuprite) were fabricated on (001) single-crystal substrates of Si, Au, and InP. Integrating Cu2O films with elemental semiconductors is of technological interest e. g. for gate dielectric materials in metal-oxide/semi-conductor field-effect transistors. In order to study the structure and growth mechanisms of these films at the nanometer length scale, we have employed advanced methods of TEM (transmission electron microscopy). Conventional TEM and electron diffraction have revealed unique orientation relationships between the Cu2O and the substrate in each one of the three systems. For Cu2O/Si and Cu2O/InP, the orientation relationship can be described as a 45° [001] rotation around the [001] substrate normal. For Cu2O/Au, in contrast, we observe two different orientation relationships: "cube-on-cube" (lattices parallel to each other) and 90° <110>. The observed orientation relationships agree with the predictions of a recently proposed crystallographic model considering the proximity of reciprocal lattice points of the film and the substrate. Specifically, this model replaces each reciprocal lattice point of each crystal by a sphere of radius r*. Preferred orientation relationships are then predicted under the assumption that they maximize the total overlap volume of the spheres attached to the reciprocal lattice points. In apparent contradiction to the unique orientation relationships, HRTEM (high-resolution TEM) studies of the Cu2O/Si and the Cu2O/InP interfaces revealed that in both systems the epitaxial layer and the substrate are separated by an amorphous interlayer, which has a thickness of a few 4 nm. In the Cu2O/Si system, the interlayer mainly consists of SiO2, as determined by elemental mapping using ESI (electron spectroscopic imaging), Z-contrast imaging using STEM (scanning TEM) with a HAADF (high-angle angular dark-field detector), and composition profiles obtained by XEDS (X-ray energy-dispersive spectrometry). In the Cu2O/InP system, the same nanoscale characterization methods have indicated the formation of Cu3P and InPO4 at the layer/substrate interface. It has been speculated that the epitaxial orienation relationship between the film and the substrate is established through pinholes in the amorphous interlayer, and there is experimental evidence in support of this hypothesis. However, recent HRTEM studies on Cu2O grown on InP under slightly different conditions revealed nanoscopic islands of Cu2O with the same special orienation relationship but no direct contact to the InP substrate. Potential micromechanisms for the evolution of the Cu2O films during early stages of electrodeposition will be discussed.

Joint DRC/EMC Session: Materials and Circuits for Flexible Electronics

Wednesday PM Room: 101
June 23, 2004 Location: DeBartolo Hall

Session Chairs: Vitaly Podzorov, Rutgers University, Piscataway, NJ 08854 USA; Alberto Salleo, Palo Alto Research Center, Palo Alto, CA 94306 USA

1:30 PM Invited

Nanowire Thin-Films: A New Electronic Materials Technology for Thin-Film Devices and High-Performance Large-Area Electronics: *Stephan Empedocles*[1]; [1]Nanosys, Inc., 2625 Hanover St., Palo Alto, CA 94304 USA

Nanosys, Inc is a technology company focused on the development of nanotechnology-enabled systems in a range of different industries. Nanosys's platform technology is based on a unique class of inorganic semiconductor nanomaterials and methods for their integration into higher-order structures that enables the creation of unique applications based on materials in which the performance characteristics of traditional inorganic semiconductors are combined with the processability of plastics. One area of particular focus at Nanosys is the development of a new nanomaterial-based high-performance thin-film technologyX Duan, C Niu, V Sahi, J Chen, JW Parce, S Empedocles, J Goldman; Nature 425, 274-278 (18 Sep 2003) that can be deposited and processed over large areas, but has the potential to provide performance approaching that of single-crystal silicon. The technology is based on the formation of dense, uniform and aligned thin-films of single-crystal silicon nanowires, which, when processed to form TFTs create hundreds to thousands of parallel high-performance single-crystal silicon connections across the TFT channel. The superior performance of this TFT technology derives from the fact that the silicon nanowires, including an integrated gate-dielectric shell, are fabricated off-line using standard high-temperature CMOS processing before being coated onto the TFT substrate. Once deposited, the nanowire thin-film can be processed with manufacturing infrastructure used for traditional a-Si or p-Si TFTs, but requires none of the common high-temperature processing steps for semiconductor deposition, annealing and dielectric deposition. In addition, this technology has the potential to be combined with many advanced printing technologies, enabling the development of high-performance printed electronics. The technology is compatible with CMOS electronics, and can be deposited on glass, plastic and even flexible substrates, enabling the fabrication of high-performance large-area electronics in a variety of applications ranging from display-backplanes to low-cost RFID to planar phased-array antennas. This overview presentation will cover the fundamental elements of Nanosys's electronic nanomaterials and platform technology, and its application to this unique new technology for large-area electronics.

2:10 PM Invited

Printing of Polymer Field-Effect Transistors: *H. Sirringhaus*[1]; [1]University of Cambridge, Cavendish Lab., Madingley Rd., Cambridge CB3 OHE UK

Polymer transistors offer new opportunities for the controlled manufacturing of active electronic circuits by a combination of solution processing and direct printing. Control over the morphology of the polymer semiconductor is obtained by making use of self-organisation mechanisms, such as liquid-crystalline phase behaviour. Accurate definition of the transistor channel and other circuit components can be achieved by high resolution printing techniques such as surface energy-assisted inkjet printing. In this presentation we will discuss recent progress towards new architectures for both planar-channel and vertical-channel polymer transistors with submicrometer channel length, the use of thin, self-assembled polymer dielectrics as well as current understanding of charge transport and charge injection in polymer field-effect devices. Submicrometer FETs can be fabricated by dewetting conducting polymer ink droplets off narrow hydrophobic lines on top of a hydrophilic substrates to yield TFTs with channel length of 250-500 nm. This requires detailed understanding of the fluid dynamic conditions for dewetting. We will also discuss self-aligned printing approaches capable of achieving even smaller feature size of less than 100 nm. Thin dielectrics with thickness less than 100 nm are required for correct device scaling of TFTs with submicrometer channel length. We have developed an approach for self-assembled bilayers of polymer semiconductors and polymer dielectrics based on vertical phase separation of ternary blend solutions comprising both the semiconductive and the dielectric polymer material. These bilayers exhibit very high thermodynamic stability, that allows fabrication of TFTs with sub-50 nm thick polymer dielectrics. Finally, we will also give an overview over applications of printed transistor circuits, such as active matrix displays.

2:50 PM

Digital Lithography for Thin-film Transistor Fabrication: *William S. Wong*[1]; Rene Lujan[1]; Steven E. Ready[1]; Michael L. Chabinyc[1]; Ana Claudia Arias[1]; Robert A. Street[1]; [1]Palo Alto Research Center, 3333 Coyote Hill Rd., Palo Alto, CA 94304 USA

Conventional methods for materials processing, such as thin-film deposition and photolithographic patterning provide the foundation for device fabrication in the microelectronics industry. Although these methods are scaleable and cost-effective, as demonstrated in silicon integrated circuits, they are not always the most appropriate methods for applications where further miniaturization is not an advantage, such as in large-area electronics. For example, the fabrication of flat-panel displays and image sensors, with a typical feature size of approx. 50 microns, is relatively expensive and complex using a conventional photolithographic process. Similarly, the processing of large-area platforms is also complicated and costly with conventional vacuum deposition methods. Developing an alternative inexpensive and simplified deposition process in conjunction with an alternative patterning method would enable low-cost, large-area electronics for displays, sensors, and evolving technologies such as electric paper. The spatial resolution and small drop volume of jet-printing methods present opportunities to simplify and reduce the cost for conventional large-area electronic device fabrication. In this talk, I will describe how jet printing can be used as a viable alternative to conventional photolithographic and thin-film deposition processes. A novel digital-lithographic method, in which an electronically generated and digitally aligned etch mask is jet-printed onto a process surface, was used to fabricate hydrogenated amorphous silicon thin-film transistor (TFT) arrays. The digital lithographically fabricated arrays had features as small as 40 microns with 5 micron layer-to-layer registration and pixel resolution of 75 dpi over a four-inch diameter wafer. The resulting TFTs, with on/off ratios of 10^8 and threshold voltages of 2-3 V were then integrated with a-Si sensor media for an image sensor. Operation of the image sensor as an x-ray detector will be shown. To further demonstrate the efficacy of the digital lithographic process, results from multi-layer patterning on flexible substrates for sensor and display applications will also be presented. Additionally, the same digital-lithographic process has been implemented in fabricating solution-based organic semiconductor TFT arrays in which the semiconductor is deposited and patterned simultaneously using jet printing. Device characteristics for both the organic and inorganic TFTs fabricated by digital lithography will be presented and compared to devices created by conventional methods.

3:10 PM Break

3:30 PM Invited

Pentacene Based Transponder Tags with Multiple-Bit Circuitry: *Paul Baude*[1]; David Ender[1]; Michael Haase[1]; Tommie Kelley[1]; Dawn Muyres[1]; Steven Theiss[1]; [1]3M, CRML, 201-1N-35, St. Paul, MN 55144 USA

We present pentacene based RFID transponder tags with 8 bit, write-once, circuitry. Integrated circuits using pentacene thin film transistors are shown to provide sufficient amplitude modulation at rf carrier frequencies of 125kHz and above to communicate with an external reader. The transponder circuitry operates using direct ac powering of the logic and output modulator circuitry.[1] The circuitry was patterned entirely using laser ablated polymeric shadow masks. These shadow masks yield transistors with gate lengths of 20 μm with a 30 μm design rule. We demonstrate improved pentacene transistor performance with the use of a polymeric dielectric surface treatment, resulting in mobilities of over 3 cm2/V-sec. This surface treatment is compatible with an electron-beam evaporated aluminum oxide, or a sputtered silicon dioxide gate dielec-

tric. The transponder data is realized using a write-once scheme that involves breaking, or leaving in place, various output nodes connected to circuit ground. The state of each of the 8 writeable bits is revealed in the reader's demodulated data stream. The internal clock signal is generated using a 27 stage ring-oscillator resulting in a data rate of about 1 kbit/second. [1]P. F. Baude, D. A. Ender, M. A. Haase, T. W. Kelley, D. V. Muyres, S. D. Theiss, Appl. Phys. Lett., 82, 3964 (2003).

4:10 PM

Hole Mobility in Organic Single Crystal Field Effect Transistors: Claudia Goldmann[1]; Cornelius Krellner[1]; Kurt P. Pernstich[1]; Simon Haas[1]; *David J. Gundlach*[1]; Bertram Batlogg[1]; [1]Laboratory for Solid State Physics, ETH Zurich, HPF-F9, Zurich 8093 Switzerland

Transport in organic molecular crystals (OMCs) is a topic of intense fundamental study. In OMCs the intrinsic transport properties are easily masked by chemical and structural defects that trap charge carriers. To access the transport properties of OMCs we make use of a field-effect device structure to accumulate a large sheet carrier density of holes at the crystal surface and fill trap states.[1] Thin lamellar OMCs (<5 micron thick) are grown using a physical vapor transport technique.[2] Single crystal organic FETs are fabricated on heavily-doped and thermally oxidized silicon wafers with patterned source/drain electrodes. Self-assembled monolayers are used to modify the interface properties of the source/drain contacts and the gate insulator. The devices are completed by placing an OMC on top of the patterned substrate. Using this method in either a 2 or 4 terminal configuration hole mobility greater than 10 cm^2/Vs for rubrene and 1 cm^2/Vs for tetracene and pentacene has been measured. These values compare favorably to those reported recently.[1,3] The 4 terminal measurement allows the contact effects to be separated from the channel properties. We will present the temperature dependence of the electrical characteristics and discuss the transport of the field-accumulated charge near the surface. Additionally, we will report on complementary space-charge-limited-current measurements that reflect the bulk properties of the OMCs. [1]J. Takeya et.al., J. Appl. Phys. 94, 5800 (2003). [2]A. Laudise, et. al., J. Cryst. Growth 187, 449 (1998). [3]V. Podzorov et.al., Appl. Phys. Lett. 83, 3504 (2003); V. Butko et.al., Appl. Phys. Lett. 83, 4773 (2003); R. de Boer et.al., Appl. Phys. Lett 83, 4345 (2003).

4:30 PM

An 8V Organic Complementary Logic Process for Flexible Polymeric Substrates: *Hagen Klauk*[1]; Marcus Halik[1]; Ute Zschieschang[1]; Florian Eder[1]; Günter Schmid[1]; Christine Dehm[1]; [1]Infineon Technologies, New Memory Platforms, Matls. & Tech., Erlangen 91052 Germany

We have designed and fabricated the first organic complementary integrated circuits on a flexible substrate. Pentacene and hexadecafluorocopperphthalocyanine (F16CuPc) were used as the p-type and n-type organic semiconductors, and solution-processed polyvinylphenol was used as the gate dielectric. In principle, complementary circuits have several advantages over circuits based on a single carrier type, including lower power dissipation, greater speed, and better noise margins. The problem with organic complementary circuits is the small electron mobility of even the best air-stable organic semiconductors. The Philips group has reported ambipolar TFTs and inverters based on narrow-bandgap polymers and interpenetrating networks of p-type and n-type materials, but the electron mobilities in these materials are below 10-4 cm2/Vs.[1] Crone and coworkers have demonstrated organic TFTs based on sexithiophene and F16CuPc and reported complementary circuits with a signal propagation delay of 10 µsec per stage. These circuits were fabricated on silicon wafers with inorganic gate dielectrics and were operated in ambient air with a supply voltage of 100 V.[2] For our complementary circuits we build on a manufacturing process we have recently developed for organic TFTs on flexible polymeric substrates, using a solution-processed polyvinylphenol gate dielectric layer.[3] TFTs and circuits were fabricated on 125 µm thick, flexible polyethylene naphthalate (Teonex® Q65 PEN, provided by DuPont Teijin Films, Wilton, U.K.), with an Al gate electrode, a 50 nm thick PVP gate dielectric, Au source/drain contacts, and evaporated organic active layers. Pentacene TFTs have a hole mobility of 0.1 cm2/Vs and a subthreshold swing of 0.6 V/decade. F16CuPc TFTs have an electron mobility of 0.002 cm2/Vs and a subthreshold swing of 1.4 V/decade. Although the mobility of these F16CuPc TFTs is smaller than the mobility of most p-channel organic TFTs, it is to our knowledge the best performance reported for an n-channel organic TFT on a flexible substrate. All electrical measurements were performed in air under ambient conditions. For the complementary circuits, the pentacene active layer was deposited and patterned using a water-soluble photoresist and a brief O2 plasma etch,[4] followed by the deposition of the F16CuPc active layer. By adjusting the W/L ratios of the p-channel and n-channel TFTs to account for the difference in mobility, complementary inverters with a gain of about 6 were obtained. To evaluate the dynamic performance of the circuits we have designed and fabricated 5-stage complementary ring oscillators. These ring oscillators operate with a supply voltage as low as 8 V and with a signal delay as low as 8 µsec per stage (using a design rule of 2 µm and a supply voltage of 40 V). To our knowledge, these are the fastest organic complementary circuits reported to date, and the first on a flexible substrate. [1]E. J. Meijer et al., Nature Materials, vol. 2, p. 678 (2003). [2]B. Crone et al., Nature, vol. 403, p. 521 (2000); J. Appl. Phys. vol. 89, p. 5125 (2001). [3] H. Klauk et al., Appl. Phys. Lett., vol. 82, p. 4175 (2003). [4]C. D. Sheraw et al., Appl. Phys. Lett., vol. 80, p. 1088 (2002).

Session H: High-K Dielectrics and Metal Gates

Wednesday PM   Room: 102
June 23, 2004   Location: DeBartolo Hall

Session Chairs: Pat M. Lenahan, Pennsylvania State University, University Park, PA 16802 USA; Robert Chau, Intel Corporation, Hillsboro, OR 97124 USA

1:30 PM Invited

H1, Dual Metal Gate CMOS Using CVD Metal Gate Electrodes: *Vijay Narayanan*[1]; Cyril Cabral[1]; Fenton R. McFeely[1]; Alessandro C. Callegari[1]; Sufi Zafar[1]; Paul C. Jamison[2]; An L. Steegen[2]; Michael Gribelyuk[2]; Eduard Cartier[1]; Victor Ku[2]; Phung Nguyen[2]; Alex Vayshenker[2]; Ying Li[2]; Byoung H. Lee[2]; Supratik Guha[1]; Evgeni Gousev[1]; Matt Copel[1]; Deborah Neumayer[1]; Rajarao Jammy[1]; Meikei Ieong[1]; Wilfried Haensch[1]; Ghavam Shahidi[1]; [1]IBM, SRDC/Rsch., IBM T. J. Watson Rsch. Ctr., 1101 Kitchawan Rd., Rt. 134, Yorktown Heights, NY 10598 USA; [2]IBM, SRDC/Microelect. Div., IBM Microelect., Hopewell Junction, NY 12533 USA

To meet the requirements for scaling high performance logic, it is becoming very apparent that metal gates need to replace doped polysilicon gates to achieve EOTs < 1 nm. However, there are a number of material and integration challenges associated with the introduction of metal gates, including the availability of suitable nFET and pFET workfunction metal electrodes and choice of integration scheme (gate last, conventional or silicide gate). In this presentation, metal electrodes will be reviewed in terms of both their structural and electrical properties on SiON and Hf-based dielectrics. We have concentrated our efforts on developing CVD approaches for metal gate deposition to obviate the well known problems of process damage & conformality (for replacement gate) associated with PVD processes. Focusing on CVD W as a prototypical metal, we have examined the stability of W/SiON and W/HfO2 stacks in capacitor and FET structures. The effect of post metal anneals on W gated HfO2 stacks with different interface layers will be examined and correlated with the thermal stability of the gate stack, flatband shifts, changes in EOT and charge trapping. It will also be shown that CVD W gated SiON and HfO2 stacks show electrical reliability as good - and in some cases better - than poly-Si/SiON gate stacks. We have also demonstrated dual metal gate functionality using novel CVD processes for TaSiN (workfunction = 4.4 eV, nFET electrode) and Re (workfunction = 4.8-5eV, pFET electrode). All three gate materials will be compared on Hf based dielectrics and it will be shown that all three gate electrodes are high temperature stable, though the structural and electrical properties of the gate stack are strongly dependent on specific electrode and interface layer combinations and post deposition processing. Finally, issues associated with CMOS integration of dual metal gates will be discussed.

2:10 PM Student

H2, Comparative Study of Trapping Characteristics of HfSiON Dielectric in nMOSFETs with Poly-Si or TiN as Gate Electrode: *D. C. Guo*[1]; L. Y. Song[1]; X. W. Wang[1]; T. P. Ma[1]; B. H. Lee[2]; S. Gopalan[2]; R.

Choi[2]; [1]Yale University, Dept. of Elect. Engrg., 15 Prospect St., New Haven, CT 06520 USA; [2]International Sematech, Austin, TX 78741 USA

In this study, we compare charge trapping characteristics of poly-Si gated with that of TiN gated nMOSFETs. In both cases, HfSiON is used as the gate dielectric. Our results show that nMOSFETs with TiN metal gate exhibit superior stability over those with poly-Si gates under identical positive bias stress conditions. NMOSFETs with 4nm HfSiON as the gate dielectric were fabricated at SEMATECH Inc. Some of the transistors have n+ poly-Si as the gate electrode and others have TiN metal electrodes. Constant voltage stress (CVS) is used to study/compare the threshold voltage instability, degradation of transconductance as well as interface trap generation in devices with the two different gate materials. Stress voltages used in this study correspond to electric fields ranging from 5MV/cm to 10MV/cm. Fig.1 shows threshold voltage shift (ΔVth) as a function of stress time under various stress conditions for poly-Si gated (open symbols) and TiN gated (solid symbols) nMOSFETs, respectively. While ΔVth in both sets of data increases with time logarithmically, it is evident that n+-poly gated nFETs exhibit more severe threshold voltage shifts than TiN gated nFETs under otherwise identical stress conditions. Fig.2 (a) shows that severe degradation in peak Gm is observed in n+-poly gated nFETs. For example, 187 second stress at 9MV/cm resulted in 17% degradation in peak Gm. In contrast, Fig.2 (b) shows almost no change in peak Gm in TiN gated nFETs. To separate possible contribution of stress induced interface trap generation to the ΔVth from that of charge trapping in the HfSiON bulk, we measured the subthreshold swing (SS) on both types of transistors during the entire course of stress. We observed (data not shown here) that at high stress condition (Eox > 9MV/cm) the SS values increase with stress time monotonically for poly gated nFETs, while there is no apparent change for the TiN gated nFETs even under higher stress field, indicating the lack of interface trap generation in TiN gated MOSFETs. Base on the above, we speculate that at low and moderate stress fields (e.g. Eox <8MV/cm) electron trapping in the bulk HfSiON is a dominant trapping mechanism for both electrodes. However, electron trapping probability is significantly higher in poly-gated MOSFETs than in TiN gated ones. At high stress conditions (e.g. Eox >9MV) holes generated by hot-electrons arriving at the poly-Si/HfSiON interface may migrate to the HfSiON/Si-substrate interface, where they either get trapped there or recombine with trapped electrons, leading to generation of new interface traps. In contrast, the lack of hole source at the TiN/HfSiON interface may account for the non-discernible change in the Subthreshold Swing as well as in the transconductance degradation.

2:30 PM Student

H3, Characterization of Ultra-Thin Hf-Based Alternative Dielectric Layers for Si CMOS by Z-Contrast Imaging and Electron Energy-Loss Spectroscopy in STEM: *Melody Pacifico Agustin*[1]; Brendan Foran[2]; Gennadi Bersuker[2]; Joel Barnett[2]; Susanne Stemmer[1]; [1]University of California, Matls. Dept., Santa Barbara, CA 93106-5050 USA; [2]International Sematech, 2706 Montopolis Dr., Austin, TX 78741-6499 USA

Alternative gate dielectrics are currently being investigated for Si based complementary metal-oxide-semiconductor (CMOS) devices. Concurrently, new metal gates are being investigated. The properties of these novel gate stacks are dependent on the often complex structure and chemistry of interfaces between the layers. We investigated two types of gate stacks consisting of hafnium oxide and hafnium silicate gate dielectrics, respectively, with poly-Si and titanium nitride/poly-Si electrodes, respectively. The Hf-silicate gate stacks incorporated Hf-Si-O films capped with TiN/poly-Si electrodes. Substrates were processed in either HF or anhydrous-HF, which were followed by exposure to NH_3 for 15 s at 700°C, and HF that was not exposed to NH_3. After high-k deposition, an anneal was performed for the films on the nitrided substrates in NH_3 for 60 s at 700°C. High-resolution TEM and Z-contrast imaging showed the presence of an interfacial SiO_{2-x} layer between the Si and the high-k in all three gate stacks with varying thickness. Compositional profiles were obtained by electron energy-loss spectroscopy (EELS) and energy dispersive x-ray spectroscopy (EDS). These profiles showed that nitrogen is present at the lower interface for stacks that were exposed to the NH_3 anneals. An unexpected oxygen-rich layer was detected at the interface between TiN and poly-Si. Low-loss EELS and the fine structures of core loss EELS of oxygen K-edge and nitrogen K-edge indicated that the layer is an oxynitride. Significant roughness of the Hf-Si-O/TiN interface caused an apparent overlap of Hf, Si, O, Ti and N. Core loss EELS of Ti $L_{2,3}$ edge indicated that the Ti signal is due to interfacial roughness and that TiN had not reacted with the high-k layer. For the Hf-oxide gate stacks, HfO_2 was grown by atomic layer deposition directly on Si and on SiO_2 that was thermally-grown on Si, respectively. For the HfO_2 on Si, the growth of a SiO_2 interfacial layer during ALD growth of the HfO_2 was observed. The oxygen K-edges for both thermally-grown and process-grown SiO_2 are compared with thermally-grown SiO_2 not exposed to high-k (HfO_2) deposition. The gate stack with the thermally-grown SiO_2 underlayer also shows an interfacial SiO_{2-x} layer between HfO_2 and poly-Si. In addition, we have performed simulations of the EELS fine structures of oxygen K-edges of Hf-oxide and Hf-silicate by an ab initio self-consistent real-space multiple-scattering calculation using FEFF 8.20. The purpose of the simulations was to investigate whether EELS can be used to detect silicate-type bonding in these ultra-thin SiO2-like interfacial layers. For crystalline $HfSiO_4$, the simulations of oxygen K edges show that at least a 30 atom cluster is needed before bulk-like fine structure is observed. This corresponds to about 8 Å in diameter around the absorbing atom. Similar results are seen for monoclinic HfO_2.

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H4, Nucleation Density Study of MOCVD Grown Ru and RuO_2 Films for Gate Electrode Applications: *Filippos Papadatos*[1]; Steve Consiglio[1]; Spyridon Skordas[1]; Sebastian Naczas[1]; Eric T. Eisenbraun[1]; Alain E. Kaloyeros[1]; [1]SUNY, Sch. of Nanoscis. & Nanoengrg., 251 Fuller Rd., CESTM B110, Albany, NY 12203 USA

Owing to issues related to dopant supersaturation and stability, metal gate electrodes are predicted to replace traditional polysilicon-based electrodes as soon as the 65-nm technology node. In particular, metal organic chemical vapor deposition (MOVCD)-grown ruthenium-based electrodes are under consideration for use as PMOS electrodes, as a result of the low resistivity, excellent stability, and appropriate work function afforded by these materials. Moreover, as the microstructure and chemical stability of the dielectric/electrode interface is paramount to the functionality of such structures, the utilization of high k dielectric materials such as HfSiON requires that the nucleation phenomena of Ru electrodes on such dielectric materials be well understood and controlled. It has been reported that ruthenium and ruthenium oxide films deposited on SiO_2/Si substrates using ruthenocene-based precursors yielded films with poor nucleation density. Therefore, this study intends to investigate mechanism s to enhance the initial nucleation of the thin ruthenium/ruthenium oxide films deposited on high-k materials such as $HfSi_xO_y$. In this study, thin metallic ruthenium and ruthenium oxide films (≤30nm) were deposited by MOCVD on SiO_2/Si and $HfSi_xO_y$ substrates. Diethylruthenocene [$(EtCp)_2Ru$] and oxygen were employed to deposit both metallic ruthenium and oxide phase films. The $HfSi_xO_y$ films were also deposited by MOCVD using dialkylamido precursors and oxygen as co-reactants. The depositions were performed in a 200 mm cluster tool with in-situ plasma capability. The cluster tool featured a load lock with a robotic arm which eliminated sample air exposure between deposition steps. Nucleation on SiO_2/Si substrates served as a reference to evaluate the effect of using different types of substrates. The effect of surface cleaning and plasma treatment on the nucleation of the metallic films was also investigated via four experiments. In the first experiment, the metallic films were deposited on untreated SiO_2/Si and $HfSi_xO_y$ substrates. The second experiment included a standard RCA cleaning step on the substrates prior the metal deposition. For the third experiment, the substrates were plasma treated prior to metal electrode deposition, while for the fourth the substrates were treated both by RCA cleaning and plasma. The RCA cleaning was performed in a class 100 cleanroom while the plasma treatment was performed in the gate electrode chamber, without air exposure prior to electrode fabrication. All samples were handled in a cleanroom environment to avoid particle contamination. Scanning electron microscopy (SEM) and atomic force microscopy (AFM) were employed to examine the resulting surface morphology, nucleation density and roughness of the electrode films. Transmission electron microscopy (TEM) was also utilized to examine the effects of the plasma treatment step on the metal/dielectric interface.

3:10 PM Break

3:30 PM

H5, Electrical Characteristics of Single Crystal Silicon and Germanium Layers Grown on $(La_xY_{1-x})_2O_3$ / Si (111): *E. J. Preisler*[1]; N. A.

Bojarczuk[1]; S. Guha[1]; [1]IBM T. J. Watson Research Laboratory, 1101 Kitchawan Rd., Yorktown Hts., NY 10598 USA

Silicon-on-insulator (SOI) technology is rapidly emerging at the forefront of the development of high speed and low power silicon device technology. Further, it has been shown that ultra-thin SOI (< 50 nm) has the potential to enable even greater improvements in device characteristics as compared to bulk silicon. We present the results of electrical testing on ultra-thin silicon and germanium layers grown directly by molecular beam epitaxy (MBE) on a lattice matched oxide grown on a silicon substrate. Back gated pseudo-MOSFET?s are demonstrated on fully depleted films. It is shown that both the silicon and germanium films exhibit excellent device characteristics. The intrinsically p-type Ge films exhibit hole mobilities of as high as 500 cm2 V-1 s-1 from Hall measurements and field effect mobilities of as high as 400 cm2 V-1 s-1 extracted from drain characteristics of the back-gated transistor structures.

3:50 PM Student

H6, Atomic-Scale Structure of Alkaline-Earth Metal on Si(001) Surface Reconstructions: *Duane M. Goodner*[1]; David L. Marasco[1]; Anthony A. Escuadro[1]; Michael J. Bedzyk[1]; [1]Northwestern University, Matls. Sci. & Engrg., 2220 N. Campus Dr., Evanston, IL 60208 USA

X-ray standing waves (XSW) have been used to investigate the atomic-scale structure of sub-monolayer Ba/Si(001) and Sr/Si(001) surface phases that play an important role in the growth of SrTiO3 on Si(001). The position of ordered alkaline-earth metal atoms relative to the underlying Si substrate has been studied for a (2x3) Sr/Si(001) phase and (2x1) phases of both Sr/Si(001) and Ba/Si(001). XSW analysis shows that Sr adatoms in the (2x3) phase must occupy cave or bridge sites. Our results also suggest that when prepared at a sufficiently low temperature, the (2x3) phase is accompanied by secondary Sr located at valley-bridge sites. The (2x1) phases of both Sr/Si(001) and Ba/Si(001) were also found to consist of alkaline-earth metal atoms occupying cave or bridge sites. These phases were accompanied by significant amounts of disordered Sr and Ba, but no specific site was found to be preferentially occupied by these randomly distributed adatoms. The atomic-scale structural parameters obtained from these results are important for investigations of the SrTiO3/Si(001) interface. Our findings support surface reconstruction models different from other recently proposed models[1-4] that were based on density functional theory calculations and consisted of alkaline-earth metal atoms occupying valley-bridge sites. [1]C.J. Forst, C.R. Ashman, K. Schwarz, P.E. Blochl, Nature 427, 53 (2004). [2]X. Zhang, A.A. Demkov, H. Li, X. Hu, Y. Wei, J. Kulik, Phys Rev B 68(2003). [3]C.R. Ashman, C.J. Forst, K. Schwarz, P.E. Blochl, Phys. Rev. B 69(2004). [4]R. Droopad et al., Journal of Crystal Growth 251, 638 (2003).

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H7, Optical Properties of Prospective High-k Dielectrics: *E. Cicerrella*[1]; J. L. Freeouf[1]; L. F. Edge[2]; J. H. Haeni[2]; D. G. Schlom[2]; R. Uecker[3]; P. Reiche[3]; T. Heeg[4]; J. Schubert[4]; G. Lucovsky[5]; [1]Oregon Health & Sciences University, Dept. of Elect. & Computer Engrg., Beaverton, OR 97006 USA; [2]Pennsylvania State University, Dept. of Matls. Sci. & Engrg., Univ. Park, PA 16802-5005 USA; [3]Institute of Crystal Growth, Berlin D-12489 Germany; [4]Insitut für Schichten und Grenszflächen, Jülich 52425 Germany; [5]North Carolina State University, Dept. of Physics, Raleigh, NC USA

With devices shrinking in size, the current gate dielectrics in silicon MOSFETs are unable to prevent excessive gate leakage. This has created a need to find a replacement material. Many ternary oxides are possible candidates. Optimum materials must have a high dielectric constant and a large bandgap as well as thermodynamic stability with silicon. We believe that some rare earth perovskites will be thermodynamically stable with silicon, and therefore are possible gate dielectrics. There is little known about the dielectric constants and bandgaps of these materials, but to determine if a material will be a suitable gate dielectric this information is essential. Thus, we have begun to study these properties. Here we discuss results obtained both from bulk single crystals and from thin films. The single crystals were grown using the Czochralski technique; the thin films were grown by molecular beam deposition and pulsed laser deposition. The bulk samples were then cut from the single crystal along the [100], [010], and [001] direction and given an optical polish. At room temperature both $DyScO_3$ and $GdScO_3$ are orthorhombic and therefore their dielectric tensor contains three independent coefficients. Indeed, other measurements have observed substantial anisotropy. We are now using a far UV spectroscopic ellipsometer to investigate the ellipsometric spectral response of $DyScO_3$ and of $GdScO_3$. We have observed substantial optical anisotropy for bulk single crystal $DyScO_3$ as measured by Far UV spectroscopic ellipsometry (5 eV < hí < 9 eV), but this anisotropy was not evident in band gap determinations from optical transmission studies. We have determined the optical bandgaps for bulk single crystals to be about 6 eV for $GdScO_3$ and over 5 eV for $DyScO_3$ using transmission measurements and ellipsometry. We shall report precise bandgaps and the full Far UV spectroscopic ellipsometry-determined optical dielectric spectra for both materials for these orientations.

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H8, Pr-Silicate Ultrathin Films for High-k Gate Dielectrics Prepared by Metal-Organic Chemical Vapor Deposition: *Yoshishige Tsuchiya*[1]; Hirotsugu Fujita[2]; Hiroshi Mizuta[3]; Hiroshi Nohira[2]; Takeo Hattori[2]; Shunri Oda[1]; [1]Tokyo Institute of Technology, Rsch. Ctr. for Quantum Effect Elect., 2-12-1, O-Okayama, Meguro-ku, Tokyo 152-8552 Japan; [2]Musashi Institute of Technology, Dept. of Elect. & Elect. Engrg., 1-28-1, Tamazutsumi, Setagaya-ku, Tokyo 158-8557 Japan; [3]Tokyo Institute of Technology, Dept. of Phys. Elect., 2-12-1,O-okayama, Meguro-ku, Tokyo 152-8552 Japan

Technological need of overcoming an issue of the leakage current with ultrathin gate oxide films has driven the research on alternative high-k materials. Exploring new gate insulator materials with a higher dielectric constant is exceedingly important for further scaling down of device dimensions. Lanthanide oxides are attractive candidates for the post HfO_2 era. In Ref. [1], a high dielectric constant of ~31 was reported for the Pr_2O_3 film grown on the Si substrate by electron-beam evaporation. Their results showed Pr-based composites are potentially useful, but, for the practical purpose, the chemical vapor deposition (CVD) technique is more important, and there are few reports on the Pr-base composites grown by the CVD. In this paper, we report on material and electrical properties of Pr-silicate ultrathin films grown by using the metal-organic chemical vapor deposition (MOCVD) technique. A p-type Si (100) wafer was used as substrates and placed on a susceptor in a lateral flow-type deposition chamber. $Pr(DPM)_3$ was adopted as a source for praseodymium and introduced into the chamber by the Ar carrier gas. Since oxygen atoms are contained in the precursor, we did not use any oxidizing agent, and the source was continuously supplied to the chamber. Total pressure in the reaction chamber was maintained at 1.5 Torr during deposition. Films were grown at various substrate temperatures of 460, 600, and 770°C. Al Kα excited O 1s photoelectron spectra of the film grown at 770°C showed that a Pr-silicate thin layer was formed inside the film. The band gap, the conduction and valence band offsets at the interface were estimated as 6.3 eV, 3.2 eV and 2.0 eV, respectively, from the measurement of O 1s and angle-resolved valence band spectra. These values are larger than those reported for Pr_2O_3[2]. With decreasing a growth temperature, both the band gap and the band offsets decreased. This result suggests that the Pr/Si ratio in the Pr-silicate varies with deposition temperature. Even in the film deposited at lowest temperature, 460°C, both conduction and valence band offsets are larger than 1 eV, which is a general criterion to judge if the material is appropriate for reducing the leakage current when it is used as a gate dielectric. The capacitance equivalent thickness (CET) and the leakage current density (J_g) were estimated from the C-V and J-V measurements for the Au/Pr-silicate/Si MIS diode structure. The chemical oxide prepared on the Si substrates prior to the deposition improved electrical properties. The CET of 1.5 nm and J_g of 9.6×10^{-6} A/cm^2 at V_{fb}-1 V were obtained for the film deposited at 770°C. [1]H. J. Osten et al., IEDM Tech. Dig., 653 (2000). [2]H. J. Osten et al., Appl. Phys. Lett. 80, 297 (2002).

Session I: Point Defects, Extended Defects, and Doping in Wide Band Gap Materials

Wednesday PM Room: 141
June 23, 2004 Location: DeBartolo Hall

Session Chairs: Joan M. Redwing, Pennsylvania State University, University Park, PA 16802-5006 USA; Thomas H. Myers, West Virginia University, Morgantown, WV 26506 USA

1:30 PM Student

I1, Investigation of Carbon-Related Defect States in MBE-Grown GaN Co-Doped with Carbon and Silicon: *Andrew M. Armstrong*[1]; Aaron R. Arehart[1]; Daniel S. Green[2]; Umesh K. Mishra[2]; James S. Speck[2]; Steven P. DenBaars[2]; Steven A. Ringel[1]; [1]Ohio State University, Elect. Engrg., 205 Dreese Lab., 2015 Neil Ave., Columbus, OH 43210 USA; [2]University of California, Matls. & Elect. & Computer Engrg., Santa Barbara, CA 93016 USA

Carbon doping of GaN is important for device technologies such as forming highly resistive buffer layers for nitride-based HEMTs. Carbon incorporation renders otherwise n-type unintentionally doped GaN semi-insulating, likely via the substitutional deep acceptor C_N. However, carbon's amphoteric nature suggests that other defects such as a substitutional donor, interstitial, or auto-compensating pairs may also form, depending on the position of the Fermi level during growth. Despite progress in assessing the impact of carbon on the electrical properties of GaN, the identification of specific carbon-related states in semi-insulating GaN remains a fertile area of study. Here, we employed DLOS (deep level optical spectroscopy) to investigate the role of carbon in MBE-grown GaN:C:Si and present for the first time a systematic study of the evolution of the defect spectra as a function of carbon incorporation. We compare our findings with MOCVD-grown GaN:C:Si. The MBE-grown samples have a silicon background of 10^{18} cm^{-3} and were co-doped with carbon tetrabromide (CBr_4) to achieve carbon concentrations of $5x10^{17}$, $1x10^{18}$ or $5x10^{18}$ cm^{-3}, yielding lightly compensated, heavily compensated, or semi-insulating layers, respectively. Because the dominant acceptor states prove to be very deep and have concentrations comparable to or greater than the donor concentration, typical defect spectroscopy methods relying on the thermal activation of dilute deep levels are not applicable. Thus DLOS and C-V defect profiling were utilized. The unique ability of DLOS to identify activation energies of very deep states in semi-insulating GaN enables C-V profiling to determine their concentrations. Levels observed at Ec-Et = 1.35, 2.56 and 3.28 eV are compared between MBE- and MOCVD-grown GaN, and a new level is reported in MBE-grown GaN at Ec-1.94 eV. The Ec-1.94 and 3.28 eV levels demonstrate a strong dependence on carbon incorporation as their concentrations increase more than threefold with increasing carbon doping. The latter is attributed to C_N, while the former may be due to interstitial carbon. The commonly observed level at Ec-1.35 eV does not exhibit a clear trend among the samples, however evidence suggests a possible relation to carbon. The behavior of the Ec-1.35 and 1.94 eV levels suggests that carbon may incorporate differently in MBE- and MOCVD-grown GaN. The origin of the Ec-2.56 eV level is under current investigation via positron annihilation spectroscopy. The possibility of a V_{Ga}- or carbon-related source is discussed in regard to the position of the Fermi level, since this state has been correlated with V_{Ga} for n-type GaN without the presence of excess C in earlier studies. The lack of p-type behavior when [C] > [Si] suggests that the carbon auto-compensates via substitutional donor-acceptor pair formation and pins the Fermi level.

1:50 PM Student

I2, Beryllium Doped GaN Grown by RF-Plasma Molecular Beam Epitaxy: *Kyoungnae Lee*[1]; Brenda VanMil[1]; Thomas H. Myers[1]; Lijun Wang[1]; Nancy C. Giles[1]; [1]West Virginia University, Physics, PO Box 6315, Morgantown, WV 26506 USA

Beryllium doping has been investigated for GaN grown by rf-plasma molecular beam epitaxy on Ga-polar MOCVD GaN templates. Samples were grown under various conditions: standard; with the addition of atomic hydrogen; using indium as a potential "co-dopant"; and with electron-beam irradiation. Theoretical predictions claim each of the latter three conditions should suppress defect formation, primarily suppressing the interstitial formation thought to be the primary compensating defect in Be-doping of GaN. As-grown and high-temperature annealed electrical and optical properties of these layers will be reported for Be concentrations ranging between $5x10^{17}$ to 10^{20} cm^{-3}. Since structural degradation due to polarity reversal typically accompanies heavy Be-doping, step-doped samples were grown under the varied growth conditions with nominal dopant steps of 10^{18} and 10^{19} and 10^{20} cm^{-3} and subjected to a polarity revealing etch to determine at which dopant concentration the polarity reversed from Ga-polar to N-polar. Nitrogen-polar GaN doped with Be exhibits a significant photo-luminescence (PL) signature typically interpreted as donor-acceptor pair (DAP) PL, leading to claims of a lower electrical activation energy that that observed for Mg-doping. This DAP PL is absent from Ga-polar GaN with similar Be concentrations, indicating the Be is incorporating at microscopically different sites, or possibly is forming different compensating complexes. Highly Be-doped Ga-polar GaN apparently forms isolated polarity-inverted regions which then incorporate Be via the N-polar mechanism resulting in the DAP PL being observed. Ga-polar samples not exhibiting the PL were then annealed after growth at atmospheric pressure in either under a nitrogen/hydrogen "activating" anneal or under pure nitrogen. The annealing process activated the DAP PL for samples grown under standard conditions, but samples remained semi-insulating. Results will be presented for the other growth conditions. Microscopic models suggesting that the DAP PL may be due to defect complex formation will be discussed. This work was supported at WVU by ONR Grants N00014-02-1-0974 and N00014-01-1-0571 and was monitored by Colin E. C. Wood.

2:10 PM

I3, Remote Hydrogen Plasma Doping of Single Crystal ZnO: *Yuri M. Strzhemechny*[1]; David C. Look[2]; Donald C. Reynolds[3]; Cole W. Litton[3]; Nelson Y. Garces[4]; Nancy C. Giles[4]; Larry E. Halliburton[4]; Shigeru Niki[5]; Leonard J. Brillson[1]; [1]Ohio State University, Ctr. for Matls. Rsch., 205 Dreese Lab., 2015 Neil Ave., Columbus, OH 43210-1272 USA; [2]Wright State University, Semiconductor Rsch. Ctr., 3640 Col. Glenn Hwy., Dayton, OH 45435 USA; [3]Wright-Patterson AFB, AFRL/MLPS, Bldg. 620, 2241 Avionics Cir., Wright-Patterson AFB, OH 45433 USA; [4]West Virginia University, Dept. of Physics, PO Box 6315, Morgantown, WV 26506 USA; [5]National Institute of Advanced Industrial Science and Technology, Thin Film Solar Cells Grp., 1-1-1 Umezono, Tsukuba, Ibaraki 305-8568 Japan

ZnO is a promising material for important optoelectronic applications, yet fundamental questions on the nature of its conductivity remain that impact the ability to control both n- and p-type doping. Thus, high-quality p-type ZnO with reproducible properties remains a contested goal. Similarly, theory[1] suggests that hydrogen is a shallow donor impurity rather than a compensating center, a prediction supported by a number of spectroscopic studies. Some electrical measurements are also consistent with H donor character, although the polycrystalline samples, direct plasma exposure, or the ion implantation involved likely introduce additional complications. Here we present clear transport and spectroscopic evidence in favor of the hypothesis of hydrogen as a shallow donor rather than a compensating center. We employ a remote hydrogen plasma treatment at the surface of high quality, single crystal ZnO that provides independent control of temperature and pressure. We investigated the effects of this tre atment on Hall concentration and mobility as well as on the bound exciton photoluminescence for a variety of representative ZnO single crystals - bulk air-annealed, Li-doped, and epitaxially grown on sapphire. These measurements show that remote H-plasma processing introduces changes in both the electrical and optical properties of ZnO that are consistent with the introduction of new shallow donors. Specifically, we showed that H-plasma-induced increases in I_4 exciton luminescence (photon energy ~3.363 eV at 4 K) correlates with increases in free carrier concentrations and mobilities determined from our Hall effect measurements. Single crystals grown by chemical vapor

transport, then air-annealed at different temperatures transform the bound exciton emission. Specifically, the I_4 intensity decreases significantly as annealing temperature increases. Conversely, this I_4 emission increases dramatically with hydrogenation, regaining almost all the intensity lost due to anneali ng. To detect Hall variations, given the small - tens of nanometers - SIMS-measured penetration depth of the H-plasma ions, we employed two approaches: (1) reducing the initial bulk carrier concentration by compensating via Li in-diffusion, (2) using an epitaxial thin film of ZnO on sapphire to minimize the thickness of the conductive layer relative to the diffusion depth of hydrogen species. Li doping removed the I_4 line and subsequent hydrogenation reintroduced broader emission in the I_4 region. Li doping removed the initial $>10^{17}$ cm^{-3} carrier concentration whereas hydrogenation restored detection of the conductivity and Hall coefficient. For a hydrogenated thin film grown on sapphire by molecular beam epitaxy, we observed an order of magnitude increase from ~ $2x10^{17}$ to $2x10^{18}$ cm^{-3} in the number of donors created by hydrogenation. Thus remote hydrogen plasma treatment can control ZnO transport and excitonic properties. Fu rthermore, it identifies the shallow donor with a hydrogen-related impurity.1. C.G. Van de Walle, Phys. Rev. Lett. v. 85, 1012 (2000).

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I4, Microstructure and Nucleation Behavior of Heteroepitaxial GaN Films Grown on Mesa-Patterned 4H-SiC Substrates: *Nabil D. Bassim*[1]; J. A. Powell[4]; Mark E. Twigg[1]; Charles R. Eddy[1]; Richard L. Henry[1]; Ronald T. Holm[1]; James C. Culbertson[1]; Philip G. Neudeck[2]; A. J. Trunek[3]; [1]Naval Research Laboratory, Elect. Sci. & Tech., Code 6812, 4555 Overlook Ave. SW, Washington, DC 20375 USA; [2]NASA Glenn Research Center, Cleveland, OH USA; [3]OAI, Cleveland, OH USA; [4]Sest, Inc., Cleveland, OH USA

Thin heteroeptiaxial GaN films grown on (0001) 4H-SiC mesa surfaces with and without atomic scale steps were studied by transmission electron microscopy, atomic force microscopy, and polarized light microscopy. Analysis of a mesa that was completely free of atomic-scale surface steps prior to III-N film deposition showed that these GaN layers (grown with a HT AlN nucleation layer) had a wide variation in island height (1 µm to 3 µm) and included the presence of pit-like defects on the film surface. This sample had a low dislocation density (5 x 108/cm2) as compared to conventionally-grown samples on unpatterned (0001) on-axis 4H-SiC (2 x 109/cm2), coupled with a 3-5 times increase in grain size. Comparison of GaN films grown simultaneously on step-free and stepped 4H-SiC mesa regions showed that the presence of surface steps reduced the overall grain size of the film from 7-10 µm to a grain size of about 2 to 3 µm. Because GaN films grow via a Volmer-Weber mechanism, a decrease in the number of substrate steps acting as heterogeneous nucleation sites may allow the growth of large GaN islands before coalescence, thus reducing the number of threading dislocations. An analysis of the effects of cleaning of the 4H-SiC wafers prior to growth on the nucleation behavior of the AlN film, as well as the effect of growth interrupts during deposition will be discussed. The development of a technique to grow large-grained films with fewer extended defects is promising for the microstructural design of unique GaN device structures grown on 4H-SiC substrates.

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I5, Drift Dominated AlGaAs Solar Cells for High Temperature Application: *Yanning Sun*[1]; Aristo Yulius[1]; Michael P. Young[1]; Eric S. Harmon[2]; Jerry M. Woodall[1]; [1]Yale University, Elect. Engrg., PO Box 208284, New Haven, CT 06520 USA; [2]LightSpin Technologies, Inc., 314 Main St., Norfolk, MA 02056 USA

We investigate an AlGaAs (Eg = 1.7 eV) solar cell grown on GaAs substrate for high temperature applications by applying a drift dominated design. This unique design can build an internal electric field throughout the active region by varying the doping concentration, which allows us to collect photo-generated carriers by drift due to this electrical field instead of diffusion associated with conventional p-n junction devices. Since MBE grown AlGaAs is known to have non-radiative traps, this drift dominated device design is expected to be more efficient in transporting minority carriers. We have already demonstrated this concept on highly defected cells by the quantum efficiency measurement on drift dominated InP photodiodes grown on GaP substrate. The results show that even with 8% lattice mismatch, we've still achieved excellent spectral response especially in the UV-visible region where we have higher than 75% internal quantum efficiency and only about 10% degradation from InP on InP substrate devices. The structure of our drift dominated AlGaAs solar cell can be described as follows: we vary the beryllium doping concentration from $10^{15}cm^{-3}$ at the junction to $10^{20}cm^{-3}$ at the surface to achieve drift fields of 5000-10000 volts/cm in the 500 nm p-type top layer. After that we have 500nm intrinsic AlGaAs layer which is fully depleted and provide another larger than 10^4 volts/cm drift field. Electrons generated in these two top layers will transport with their saturation drift velocity (~10^7 cm/s) and can get through these layers in less than picoseconds. The 200nm n-type AlGaAs region is right under the intrinsic region and the doping concentration is also graded from $10^{16}cm^{-3}$ at the junction to $5*10^{18}cm^{-3}$. Therefore all together we have drift fields in the top 1200nm region as the active region of the device. We also have 5nm heavily p-doped GaAs layer on the top for good ohmic contact. AlGaAs characterization structures and cells have been fabricated and tested. We used electrochemical C-V profiler (ECV) to profile the carrier concentration as a function of sample depth. The profile confirms that the carrier concentration has been graded as expected. The dark current-voltage characteristics have been measured. The idea factor extracted from the J-V curve in the forward direction is about 1.78, and reverse saturation current is very low, about $0.2nA/cm^2$. The spectral response on the AlGaAs drift cell shows 40-45% internal quantum efficiency at green and orange and 20-35% at longer wavelengths. However, the response at blue-UV range is very low, which we currently think is due to the carriers generated by UV-blue photon absorption recombining via interstitial Be traps in the heavily p-doped ($10^{20}cm^{-3}$) region near the AlGaAs surface. Details of the high-energy-photon loss mechanism will be presented at the conference.

3:10 PM Break

Session J: Si-Based Heterojunctions and Strained Si: Growth, Characterization and Applications

Wednesday PM Room: 141
June 23, 2004 Location: DeBartolo Hall

Session Chairs: Sarah H. Olsen, University of Newcastle-upon-Tyne, Newcastle NE1 7RU UK; Doug Webb, ATMI, Meza, AZ 85210 USA

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J1, High Electron Mobility Transistor Structures on Sapphire Substrates Using CMOS Compatible Processing Techniques: *Carl H. Mueller*[1]; Samuel A. Alterovitz[2]; Edward T. Croke[3]; George E. Ponchak[4]; [1]Analex Corporation, 21000 Brookpark Rd., MS 7-1, Brookpark, OH 44135 USA; [2]NASA Glenn Research Center, 21000 Brookpark Rd., MS 54-5, Cleveland, OH 44135 USA; [3]HRL Laboratories, 3011 Malibu Canyon Rd., RL63, Malibu, CA 90265 USA; [4]NASA Glenn Research Center, 21000 Brookpark Rd., MS 54-5, Cleveland, OH 44135 USA

System-on-a-chip (SOC) processes are under intense development for high-speed, high frequency transceiver circuitry. As frequencies, data rates, and circuit complexity increases, the need for substrates that enable high-speed analog operation, low-power digital circuitry, and excellent isolation between devices becomes increasingly critical. SiGe/Si modulation doped field effect transistors (MODFETs) with high carrier mobilities are currently under development to meet the active RF device needs. However, as the substrate normally used is Si, the low-to-modest substrate resistivity causes large losses in the passive elements required for a complete high frequency circuits. These losses are projected to become increasingly troublesome as device frequencies progress to the Ku-band (12 - 18 GHz) and beyond. Relative to Si, the high electrical resistivity of sapphire enables superior performance in passive device such as inductors, and less cross-talk between devices. Sapphire is an excellent substrate for high frequency SOC designs because it supports excellent both active and passive RF device performance, as well as

low-power digital operations. We are developing high electron mobility SiGe/Si transistor structures on r-plane sapphire, using either in-situ grown n-MODFET structures or ion-implanted high electron mobility transistor (HEMT) structures. Advantages of the MODFET structures include high electron mobilities at all temperatures (relative to ion-implanted HEMT structures), with mobility continuously improving to cryogenic temperatures. We have measured electron mobilities over 1,200 and 13,000 cm^2/V-sec at room temperature and 0.25 K, respectively in MODFET structures. The electron carrier densities were 1.6 and $1.33x10^{12}$ cm^{-2} at room and liquid helium temperature, respectively, denoting excellent carrier confinement. Shubnikov de-Haas oscillations were observed, thus confirming the 2D nature of the carriers. Conversely, HEMT structures using ion-implanted processing are appealing because they are compatible with existing CMOS processing, and thus would be attractive for complex, highly integrated circuitry. Using this technique, we have observed electron mobilities as high as 900 cm^2/V-sec at room temperature at a carrier density of $1.3x10^{12}$ cm^{-2}. The temperature dependence of mobility for both the MODFET and HEMT structures provides insights into the mechanisms that allow for enhanced electron mobility as well as the processes that limit mobility, and will be presented. Using the MBE Sb doped structures, transistors with varying source-to-drain distances and gate lengths (1 - 5 µm) were fabricated. Although the design is not optimized, the initial results are promising. The I-V behavior indicated the saturated drain current region extended over a wide drain voltage range, with knee voltages of approximately and 0.5 V and increased leakage starting at voltages slightly higher than 4 V. The saturation drain currents were lower than expected, and reasons for this are under investigation.

3:50 PM Student

J2, Temperature Sensitivity of DC Operation of Sub-Micron Strained-Si MOSFETs: *Valerio Gaspari*[1]; *Kristel Fobelets*[1]; Sarah H. Olsen[2]; Jesus Enrique Velazquez-Perez[3]; Anthony G. O'Neill[2]; Jing Zhang[4]; [1]Imperial College London, Elect. & Elect. Engrg., MailStop EEE-OSD, Exhibition Rd., London, England SW7 2BT UK; [2]University of Newcastle upon Tyne, Elect. Engrg., Newcastle NE1 7RU UK; [3]Universidad de Salamanca, Dept. de Física Aplicada, Edificio Trilingue, P.za de la Merced s/n, Salamanca E-37008 Spain; [4]Imperial College London, Physics, Exhibition Rd., London SW7 2AZ UK

The DC performance of sub-micrometer Strained-Si n-type surface channel MOSFETs has been investigated for operating temperatures ranging from 10 K to 300 K. The strained-Si layer that constitutes the active region of the devices was grown on strain-relaxed constant-composition SiGe buffer layer, preceded by a linearly graded SiGe virtual substrate. The final Ge concentration in the devices presented in this study ranges from 10% to 30%. Si control devices were produced as performance references. Devices were fabricated using industry-standard CMOS processing techniques, with a reduced thermal budget to preserve the integrity of the layer structure. The low-field maximum transconductance of strained-Si devices is found to be higher that that of the corresponding Si control device for all temperatures and all virtual substrate Ge concentrations greater than 10%, indicating an increased value of mobility in the strained Si layer. The largest relative performance gain (with respect to the Si control) is observed in the device with a 20% Ge virtual substrate. The relative transconductance increase in strained-Si devices decreases with decreasing temperature down to approximately T = 100 K, below which it remains constant. This seems to indicate that the importance for performance increase of reduced inter-valley phonon scattering in strained Si decreases as the relative importance of phonon scattering processes as a mobility-limiting factor decreases. The remaining amount of performance gain below T = 100 K is attributed to reduced in-plane effective mass and Coulomb scattering in strained Si in comparison with the Si control device. The sub-threshold slope of strained-Si devices is found to be approximately insensitive to virtual substrate Ge concentration, up to a Ge content of 20%. Higher concentrations of Ge in the virtual substrate were observed to result in an increase in the minimum sub-threshold slope over the entire temperature range. The sub-threshold slope in high-Ge-content devices was limited by relatively large off-state currents, which we attribute to the presence of leakage paths through the virtual substrate.

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J3, MOS Capacitors on Epitaxial Ge/$Si_{1-x}Ge_x$ with High-k Dielectrics: *Sachin V. Joshi*[1]; Xiao Chen[1]; David Q. Kelly[1]; Tat Ngai[1]; James Chen[1]; Sanjay K. Banerjee[1]; [1]University of Texas, Microelect. Rsch. Ctr., Bldg. 160, 10100 Burnet Rd., Austin, TX 78758 USA

High K dielectrics on Ge can reduce gate leakage while taking advantage of the high mobility of Ge. However Ge substrates have poor mechanical and thermal properties, high cost, and process complexity. Epitaxial Ge layers, of about inversion layer thickness could confine electrons or holes under a gate bias enabling high mobility MOSFETs. Ge/$Si_{1-x}Ge_x$ MOS capacitors were fabricated on p-type silicon substrates. ≈60A° Ge or $Si_{1-x}Ge_x$ (x=0.9) epitaxial layers were deposited by remote plasma-assisted chemical vapor deposition (RPCVD) at ≈300°C. ≈50A° RPCVD HfO_2 was then deposited in another chamber without breaking the vacuum, at ≈250°C using hafnium t-butoxide precursor. Subsequently post-deposition annealing, TaN sputtering, capacitor patterning and etch, backside metallization and sintering were done, at or below 400°C. MOS capacitors directly on Si were fabricated using the same procedure. Physical and electrical characteristics were investigated. Using X Ray Diffraction (XRD) and XRD simulation we confirmed that ≈50A° Ge epitaxial layer with over 90% compressive strain on Si substrate is grown. Owing to the low temperature meta-stable RPCVD growth, ≈65A° epitaxial Ge layer is achieved, well beyond the equilibrium Critical Layer Thickness (CLT (<10A°)) as seen from cross-sectional High Resolution Transmission Electron Microscopy (HRTEM). The RMS roughness for Ge and $Si_{1-x}Ge_x$ epitaxial layers is ≈1.5A°, indicating a smooth surface for HfO_2 growth. The interfacial layer is ≈ 10A° on Si, but less than 5 A° on Ge layer probably because Ge oxides are volatile at high temperature and high vacuum. Low-frequency curves were simulated using the NCSU CVC program from the measured high-frequency capacitance with QM correction. EOT of HfO_2 on Ge is determined to be 9.7A°, half of that on Si (20A°), due to the lower interfacial thickness between HfO_2 and Ge. The interface state density (D_{it}) in HfO_2 /Si stack is ≈10^{11}/cm^2/eV. The $D_{it's}$ in HfO_2 /Ge/Si and HfO_2 / Si_{1-x} Ge $_x$ /Si stacks are of the order of 10^{12}/cm^2/eV, probably due to the less stable interface between HfO_2 and Ge/Si_{1-x} Ge_x. Leakage currents densities of these HfO_2 films at -1V are ≈10^{-2} A/cm^2 with reasonably well behaved J-V characteristics. These values are comparable with recent values with similar EOTs for gate stacks of HfO_2 on Si, and are 3 orders of magnitude lower than those reported for HfO_2 on Ge for similar EOTs. We attribute this leakage reduction to the epitaxial Ge layer and high-k dielectric layer being grown without breaking the vacuum, thus avoiding interfacial contamination. Thus, low temperature MOS capacitor stacks with strained epitaxial Ge or Si_{1-x} Ge_x (x=0.9) layer directly on Si substrates, and with HfO_2 (EOT=9.7A°) as dielectric, both using RPCVD is demonstrated. Well behaved MOS capacitors show that RPCVD process is a promising technique for low thermal budget, high performance applications.

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J4, Uniaxially-Tensile Strained Ultra-Thin Silicon-On-Insulator with Up to 1.0% Strain: *R. L. Peterson*[1]; H. Yin[1]; K. D. Hobart[2]; T. S. Duffy[3]; J. C. Sturm[1]; [1]Princeton University, Dept. of Elect. Engrg., E-Quad, Olden St., Princeton, NJ 08544 USA; [2]Naval Research Laboratory, Washington, DC 20375 USA; [3]Princeton University, Dept. of Geoscis., Guyot Hall, Princeton, NJ 08544 USA

Low uniaxial tensile strain of <0.04% has been recently reported to increase both PMOS and NMOS silicon-on-insulator (SOI) effective mobilities by ~15%,[1] much more than that expected by comparable biaxial strain.[2] We have demonstrated uniaxial tensile strain in SOI of 0.6% using stress balance of a SiGe/Si bi-layer structure.[3] In this study, record uniaxial strain of 1.0% has been achieved by thinning the Si film in the bi-layer. This increased strain level should allow for even greater device performance enhancement. SiGe and Si films are transferred to a BPSG (borophosphorosilicate glass)-coated Si wafer by a wafer bonding and Smart-Cut™ layer transfer process described previously,[4] forming 30nm $Si_{0.7}Ge_{0.3}$ / 10-25nm Si / BPSG. After transfer, the Si film remains relaxed and SiGe commensurately compressively strained. The SiGe/Si layers are patterned into islands with <100> edges. Upon high-temperature annealing BPSG viscosity decreases substantially and the SiGe expands laterally to relax its compressive strain, stretching the underlying Si film to create tensile strain. The bi-layer structure thus reaches an equilibrium state of stress balance.[5] Strain is measured by micro-Raman spectroscopy at 488 or 514nm.[6] For islands of edge length L, lateral relaxation occurs according to the time constant, $\tau \propto L^2$.[4] Small square islands result in biaxially-symmetric strain, while rectangular islands maintain their initial strain in the long dimension (here, 150µm) but

quickly expand in the short dimension (≤ 20μm), yielding uniaxial tensile Si strain. The net strain change is identical for the Si and SiGe films because of their coherent interface.[5] That the two layers move together is clearly demonstrated for 20μmx150μm islands of 30nm SiGe/25nm Si/200nm BPSG, before and after 30min at 800°C in nitrogen: $\Delta\varepsilon_{Si} \approx \Delta\varepsilon_{SiGe}$ = 0.75%. To obtain larger uniaxial Si strain we use a thinner layer of Si: 30nm SiGe/10nm Si/5.5nm SiN_x / 1μm BPSG. SiN_x is added to suppress dopant out-diffusion from BPSG.[5] After 15min at 750°C, SiGe strain in the short-dimension direction changes from 1.2% to 0.2% (i.e., from full compressive strain to almost complete relaxation) in agreement with predicted SiGe strain of 0.2% based on stress balance. The resulting uniaxial tensile strain in the underlying 10nm Si layer is directly measured to be 1.0%, again confirming a coherent SiGe/Si interface. For stress balance of the same bi-layer, uniaxial Si strain is greater than biaxial Si strain (~0.7%) due to the long island dimension constraint, which causes all the expansion to take place in the short dimension. [1]B.M. Haugerud, et. al., Journal of Applied Physics, 94, 4102 (2003) [2]S. Takagi, et. al., IEDM Digest, Washington, DC (2003), pp.57-60 [3]H. Yin, et. al., MRS Fall Meeting, Boston, MA (2003) [4]H. Yin, et. al., Journal of Applied Physics, 91, 9716 (2002) [5]H. Yin, et. al., IEDM Digest, Washington, DC (2003) [6]S.C. Jain, et. al., Physical Review B, 52, 6247 (1995).

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J5, Influence of the Si-Ge Interdiffusion in $NiSi_{1-u}Ge_u$ on Morphological Stability: *Johan Seger*[1]; Tobias Jarmar[2]; Fredric Ericson[2]; Ulf Smith[2]; Shi-Li Zhang[1]; [1]KTH, Dept. of Microelect. & Info. Tech., PO Box E229, Kista SE-164 40 Sweden; [2]Uppsala University, The Ångström Lab., Matl. Sci., PO Box 534, Uppsala SE-751 21 Sweden

In order to meet the requirements specified in the International Technology Roadmap for Semiconductors (ITRS), for realization of the aggressive downscaling, new materials need to be introduced. The regions of interest here are the source/drain (S/D) where shallow junctions need to be combined with low sheet resistance and low resistivity contacts, and the channel where high mobility is essential for high performance nano-MOSFETs. This so-called "material scaling" leads to a requirement for the integration of new materials in standard Si processing technology. One of the most promising candidates for the "material scaling" approach is $Si_{1-x}Ge_x$. The incorporation of compressively strained $Si_{1-x}Ge_x$ in a MOSFET, i.e. in the channel region or in S/D, has made the study of phase and morphology stabilities in $NiSi_{1-u}Ge_u$ on $Si_{1-x}Ge_x$ particularly interesting. The poor morphological stability of $NiSi_{1-u}Ge_u$ formed on $Si_{1-x}Ge_x$ is of a serious concern when forming contacts based on self-aligned silicide (salicide) technology. Our recent studies show that the agglomeration of $NiSi_{1-u}Ge_u$ begins already around 550 °C and is independent of the crystallinity of the underlying $Si_{1-x}Ge_x$ film, polycrystalline or single-crystal. We have identified that interdiffusion of Si and Ge inside the germanosilicide grains is a major cause for agglomeration. In the present work, we study the Si-Ge interdiffusion in $NiSi_{1-u}Ge_u$ using various single-crystal $Si_{1-x}Ge_x$ films of different compositions and different thickness combinations.Compressively-strained $Si_{1-x}Ge_x$ layers were grown epitaxially on Si(100) with chemical vapor deposition. Nickel films were deposited by means of electron-beam evaporation. The samples were annealed rapid thermally. A four-point probe was used to measure the sheet resistance in order to monitor the solid-state interaction as well as to correlate the resistance variation to the evolution of the surface morphology. Phase identification was carried out using X-ray diffraction. Scanning transmission electron microscopy in combination with energy dispersive spectroscopy was used to detail the morphology of the interface region. Our results show that a substantial interdiffusion of Si and Ge inside the $NiSi_{1-u}Ge_u$ grains already occurs at 600 °C. The atomic movement of the least mobile species at such low temperatures results in a rapid composition homogenization of a $NiSi_{0.78}Ge_{0.22}$/NiSi bilayer structure and a hindrance of the undesired $NiSi_2$-formation. It also leads to an improved morphological stability of the $NiSi_{0.78}Ge_{0.22}$/NiSi structure on Si, compared to the stability of $NiSi_{0.78}Ge_{0.22}$ on $Si_{0.78}Ge_{0.22}$. Our investigation als o shows that the film texture of $NiSi_{1-u}Ge_u$ is strongly affected by the characteristics of the $Si_{1-x}Ge_x$ layer and it is found that the layer sequence of the various $Si_{1-x}Ge_x$ layers influences the film texture. Ni interaction with the $Si_{0.78}Ge_{0.22}$/Si structure leads to a preferentially orientated textured $NiSi_{1-u}Ge_u$ film whereas $NiSi_{1-u}Ge_u$ formed on the $Si/Si_{0.78}Ge_{0.22}$ system gives a randomly orientated silicide film.

Session K: Quantum Dots in III-V and Group IV Compounds

Wednesday PM Room: 136
June 23, 2004 Location: DeBartolo Hall

Session Chair: Ben Shanabrook, Naval Research Laboratories, Nanostructures Section, Washington, DC 20375-5000 USA

1:30 PM

K1, Thermal Processing of InAs and InGaAs Quantum Dots for Device Integration: Forrest Kaatz[1]; *Jeff Cederberg*[1]; [1]Sandia National Laboratories, PO Box 5800, Albuquerque, NM 87185 USA

Semiconductor quantum dots are being investigated to take advantage of the effects of three-dimensional quantum confinement for optoelectronic devices. We are investigating InAs and InGaAs quantum dots formed by metal-organic chemical vapor deposition. The incorporation of quantum dots into integrated devices requires evaluation of their optical properties after thermal treatments used to modify the ground state energy. The InAs quantum dots investigated have a ground state at 1130 meV (1100 nm) when grown directly on GaAs layers. Investigations looked at a matrix of thermal treatments ranging from 600 to 900 C and times from 15 seconds to 1 hour. For samples annealed in contact with a GaAs wafer (proximity capping), we have observed a blue shift in the peak energy of 40 meV at 600 C for treatment times of 10 minutes. Extending this treatment out to 1 hour produces a 112 meV shift in the ground state. The emission intensity is retained for temperatures up to 650 C for the times investigated, but higher temperatures res ulted in significant intensity degradation, possibly due to non-radiative recombination at point defects formed during treatment. Quantum dot emission is not observed when the sample is annealed at 900 C for any length of time, setting a maximum processing temperature. Samples capped with PECVD SiO2 and annealed have similar annealing characteristics, however, the magnitude of the blue shift is reduced compared to the proximity capped samples. The origin of this effect is not clear, since SiO2 capping is known to enhance the disordering of quantum well structures. In0.40Ga0.60As quantum dots emitting at 1050 nm, treated using similar conditions, will be compared to the InAs structures to evaluate their thermal stability. Our results will be contrasted with results from the literature. Support from the Division of Materials Science and Engineering, Office of Science, U.S. Department of Energy, is gratefully acknowl edged. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under contract DE-AC04-94AL85000.

1:50 PM

K2, Thermal Effect on the Luminescence Properties of InP Quantum Dots Coupled with an InGaP Quantum Well Through a Thin InAlGaP Barrier: *X. B. Zhang*[1]; J. H. Ryou[1]; G. Walter[2]; N. Holonyak[2]; R. D. Dupuis[1]; [1]Georgia Institute of Technology, Sch. of Electric & Computer Engrg., Atlanta, GA 30332 USA; [2]University of Illinois, Micro & Nanotech. Lab., Urbana, IL 61801 USA

InP self-assembled quantum dots (SAQDs or simply QDs) on InGaP matrices have been studied by several research groups and on InGaAlP and InAlP matrices by the present authors. Lasers emitting in the red spectral region operating CW at 300K were realized by using In0.5(Al0.6Ga0.4)0.5P as the confining layer. We have demonstrated that by using an auxiliary InGaP quantum well (QW) coupled to InP QDs through a thin InAlGaP barrier layer (QW+QD structure), the carrier collection efficiency and the operation of QD lasers can be markedly improved. The QW with a thin barrier used here not only helps the thermalization of injected hot carriers in QW before they tunnel into the QDs but also helps the carrier injection in QDs. Furthermore, the thin barrier between the QW and QD layers can be used to adjust the uniformity and the density of QDs. This improved laser operation was also realized in the InAs QW+QD system. On the other hand, by directly

growing InAs QDs in InGaAs quantum wells (dot in the well or simply DWELL structure), laser diodes with fairly low threshold current density were obtained. This was attributed to the improved QD density and the better capture of carriers into QDs with a surrounding QW. Here, we will show a comparison study of the thermal effect on the luminescence properties of QW+QD and DWELL structures. We show that the InP QW+QD structures are superior to the DWELL in that the luminescence peak of InP QW+QD is much less sensitive to temperature than that of the DWELL. The temperature dependent cathodoluminescence (CL) properties of (1) InP/InAlGaP QDs coupled with an InGaP QW through a thin InAlGaP barrier, (2) the InP QDs directly in the InAlGaP well, and (3) a reference sample InP/InAlGaP QDs were studied in our SEM fitted with an Oxford MonoCL system. With an increase in temperature, we found that the CL peak of the reference sample shows a large red shift as compared with the bandgap of InP bulk material. This large red shift is due to (1) the easier thermal activation of carriers out of smaller QDs and (2) the transfer of thermally activated carriers from small QDs to large ones. Within the temperature range studied, this red shift is much larger in DWELL but is much smaller, and in some temperature range, the energy of CL peak is independent on temperature in QW+QD. The larger red shift observed in DWELL is due to the fact that the QW surrounding the QDs helps the transfer of thermally activated carrier from small QDs to large ones. The temperature insensiti ve emission energy observed in QW+QD is caused by (1) thermalization of hot carriers in QW and (2) nonuniform tensile strain in QW created by the QDs on top of the QW.

2:10 PM

K3, InAs and InGaAs Quantum Dot Growth by MOCVD: *Theodore Chung*[1]; Gabriel Walter[2]; Nick Holonyak[2]; Russell D. Dupuis[1]; [1]Georgia Institute of Technology, Elect. & Computer Engrg., 777 Atlantic Dr., Atlanta, GA 30332-0250 USA; [2]University of Illinois, Micro & Nanotech. Lab., 208 N. Wright St., Urbana, IL 38018 USA

The deposition of InAs and InGaAs quantum dots (QDs) by metalorganic chemical vapor deposition (MOCVD) is studied. First, atomic force microscope (AFM) images of the samples deposited under various growth conditions are presented, and a physical model on the epitaxial growth front describing the nature of three-dimensional island formation is described. The model will explain the reason why a low effective V/III ratio at the GaAs surface is the most important factor in the formation of coherent InAs islands, second only to growth temperature. In addition, it illustrates the interdependent relationship between various growth conditions (growth temperature, arsine flow rate, switching time, and hydrogen shroud flow) on the deposition of InAs QDs (size and shape) as well as the trade-off in the material and optical properties. Experimental results presented show that the hydrogen shroud flow and gas switching are the most critical growth parameters due to the large dynamic range and ease of control. The second part of the study involves the growth of InGaAs QDs on GaAs substrates using cycled sub-monolayer deposition technique, which has so far only been demonstrated successfully in molecular beam epitaxy (MBE) in pushing the QD ground-state emission to 1.3 um. Tertiarybutylarsine (TBA) instead of arsine is adopted as the arsenic source for the deposition in order to achieve low V/III ratio with consistency. When deposited under the new deposition technique, InGaAs QDs imbedded in GaAs waveguide show discrete energy peaks at 980 nm, 1045 nm, 1154 nm and a ground-state wavelength as far as 1.214 um. The photoluminescence (PL) data show the evolution from two-dimensional quantum well (QW) to three-dimensional QDs with increasing number of deposition cycles. In addition, the number of discrete states increases with the deposition cycles until a maximum of three or four energy levels is reached. However, a further increase in deposition cycles reduces the number of transition states and shifts the lowest transition state toward shorter wavelength. The further results from the capping layer growth and annealing study on InGaAs QDs demonstrate a blue-shift in photoluminescence wavelength as a function of annealing. The data show that the growth of high-quality upper cladding layer is the key in obtaining near QD laser near 1.3 um wavelength in MOCVD. Furthermore, it explains why the threshold current density of InAs or InGaAs QD lasers grown by MOCVD has remained consistently higher than that of MBE grown diodes and the lasing wavelength of MOCVD grown InAs or InGaAs quantum dot lasers has been limited to less than 1.17-1.18 um.

2:30 PM Student

K4, The Effect of Two-Temperature Capping on Germanium/Silicon Quantum Dots and 3D Tomographic Analysis of Superlattices So Composed: *Thomas E. Vandervelde*[1]; Alan Kubis[2]; Kai Sun[3]; Timothy L. Pernell[4]; James L. Merz[3]; Robert Hull[2]; John C. Bean[4]; [1]University of Virginia, Dept. of Physics, Charlottesville, VA 22904 USA; [2]University of Virginia, Dept. of Matls. Sci. & Engrg., Charlottesville, VA 22904 USA; [3]Univeristy of Notre Dame, Dept. of Physics, Notre Dame, IN 46556 USA; [4]University of Virginia, Dept. of Elect. & Computer Engrg., Charlottesville, VA 22904 USA

It is well documented that quantum dots (QDs), grown and subsequently buried under silicon at temperatures greater than 400°C, flatten during capping. Although QD arrays in Si superlattices have been studied for more than a decade, the process of flattening is not well understood. Here, we examine the process by which flattening occurs, using a two-temperature capping technique. Briefly, a 300ºC cold cap layer is deposited, conformally coating the dot, followed by deposition of hot Si at 750ºC. Through this process, full or partial shape retention of the buried QDs can be selectively maintained. Interestingly, we found that dots grown with this technique do not flatten in the traditional way: In fact, the dot truncates without any associated base spreading. The material from this truncation fills in the topologically lower regions, thereby flattening the surface of the sample. We analyzed this truncation by growing a series of samples under conditions of varied cold cap thicknesses and base growth temperatures. In addition, we determined that an anneal at or above 650°C was sufficient to induce this truncation, while adatom flux was not required for truncation to occur. We subsequently examined the samples using cross-sectional TEM to determine the degree of shape retention and location of the truncated material. This technique also provided the optimal growth conditions for two additional studies: A photoluminescence (PL) study, which is used to determine how shape retention affects recombination efficiency, and a 3D tomographic reconstruction of a superlattice. We grew Ge QD supperlattice samples with 20 layers of buried dots that maintained either their full or partially truncated shape. These samples were then analyzed using TEM to look for presence of dislocations, degree of shape retention, and alignment/self-segregation of upper layers, compared to lower layers. The size-retention of these dots allowed for focused ion beam-based tomographic reconstruction. This technique requires the serial sectioning of a structure in 20nm slices, so if the dots were thinner than 20nm they would not be resolved. The data from this sectioning was then reconstructed and a 3D model detailing the alignment of the dots throughout the volume was created. The findings from all of the above techniques help to elucidate the properties of QDs in complicated structures and imply possible techniques to refine current technological practices. This work was funded by the National Science Foundations Materials Research Science and Engineering Center (MRSEC) on Nanoscopic Materials Design at the University of Virginia.

2:50 PM Student

K5, Photoluminescence Study of Ge/Si Quantum Dots Grown with Single and Double Si Caps: *Kai Sun*[1]; Thomas E. Vandervelde[2]; Alan Kubis[3]; Timothy L. Pernell[4]; Robert Hull[3]; John C. Bean[4]; James L. Merz[1]; [1]University of Notre Dame, Dept. of Elect. Engrg., 275 Fitzpatrick Hall, Notre Dame, IN 46556 USA; [2]University of Virginia, Dept. of Physics, Charlottesville, VA 22904 USA; [3]University of Virginia, Dept. of Matls. Sci. & Engrg., Charlottesville, VA 22904 USA; [4]University of Virginia, Dept. of Elect. & Computer Engrg., Charlottesville, VA 22904 USA

Photoluminescence (PL), Transmission Electron Microscopy (TEM), and Atomic Force Microscope (AFM) measurements have been made on Si/Ge quantum dot (QD) samples, which were grown by molecular beam epitaxy under a variety of conditions in order to optimize the radiative recombination from the QDs. A 1.4 nm layer of Ge was deposited on a Si(100) wafer in the Stranski-Krastanov growth mode at either 650ºC or 750ºC, and subsequently capped with a Si layer ranging in thickness from 1 to 20 nm, grown at ~300ºC (referred to as a "cold cap"). In most cases, the cold cap was followed by the growth of a thicker Si capping layer grown at the same temperature used for the QD growth ("hot cap"). The cold cap is used to preserve the shape of the QD, while the hot cap improves the luminescent efficiency. A third variant of capping was also explored where the cap was continuously grown from "cold" to "hot", in order to eliminate the growth interruption between cold and hot caps. The following results were observed by PL. (1) For the cold-capped

QDs, annealing at 650ºC for 20 min. improves their luminescence slightly. (2) For the samples having both cold and hot caps, the QD-related PL signals are much stronger than the samples having only a cold cap, and there is usually a slight improvement of luminescence intensity with decreasing thickness of the cold cap. (3) When the hot cap is grown continuously from low to high temperature, a new emission band appears in the PL spectra. A bimodal distribution of dot sizes is generally observed in the AFM images, and differences have been noted between dot growth at 650ºC and 750ºC. For the samples grown at 750ºC, the QD-related PL signals shift to higher energy, suggesting that either the Ge QDs grown at 750ºC are smaller in size, or that they contain a higher concentration of Si through intermixing of Si with the Ge dots.[1] The latter result is supported by both the AFM and TEM images. For growth of multiple Ge layers at 750ºC, there is a dramatic increase in luminescence intensity and shift of the emission to higher energy. This work was funded by the National Science Foundation's Materials Research Science and Engineering Center (MRSEC) on "Nanoscopic Materials Design" at the University of Virginia. [1]M. Stoffel, U. Denker, G.S. Kar, H. Sigg, and O.G. Schmidt, Appl. Phys. Lett. 83, 2910 (2003).

Session L: Contacts to Silicon Carbide

Wednesday PM   Room: 140
June 23, 2004   Location: DeBartolo Hall

Session Chair: Lisa M. Porter, Carnegie Mellon University, Dept. of MSE, Pittsburgh, PA 15213-3890 USA

1:30 PM Student

L1, Electronic Defect States at Annealed Metal/4H-SiC Interfaces: *Sergey Tumakha*[1]; Leonard J. Brillson[1]; Robert S. Okojie[2]; [1]Ohio State University, Elect. Engrg., 2015 Neil Ave., 205 Dreese Lab., Columbus, OH 43210 USA; [2]NASA-Glenn Research Center, 21000 Brookpark Rd., M/S 77-1, Cleveland, OH 44135 USA

Depth-resolved electron-excited luminescence studies of SiC surfaces and interfaces provide evidence for localized states that can influence charge transfer at metal-SiC junctions. Until recently, such states have only been inferred, based on the variations in Fermi level position with metal work function, rather than measured directly. Schottky barrier studies of 4H-SiC with a wide range of metals show no strong Fermi level "pinning" in a narrow range of energies,[1] suggesting only a moderate influence of localized states. Previously, we reported 1.9 eV process-dependent interface state emission at Pt/Ti/4H-SiC interfaces. Furthermore, high temperature annealing can produce stacking faults and effective gap states in highly-doped n-type 4H-SiC.[2] At issue is whether these and other interface states due to chemical bonding and/or diffusion are present at metal-SiC interfaces and play a role in barrier formation. Here we present low energy, electron-excited nanoluminescence (LEEN) spectroscopy measurements of both free and metallized 4H-SiC Si-face surfaces at room and elevated temperatures. For bare surfaces annealed in ultrahigh vacuum (UHV), we observe the emergence of a 2.47 eV midgap emission due to stacking faults at T= 1150°C after 2 hours. Additional 2 hour, 1150°C anneals increase this emission along with a 2.2 eV shoulder and a broad 1.7-1.9 eV shoulder previously attributed to bounding partial and misfit dislocations. For Au deposited at bare SiC in UHV, similar new 1.9 eV and 2.3 eV emission appears at room temperature under the metal. Depth-resolved spectra with increasing incident beam energy EB (0.5 - 3 keV) and excitation depth show that the 1.9 eV emission is localized within the first 50 nm. Similarly, the ~ 2.3 eV emission appears only for EB of 0.5 keV, corresponding to ~ 5 nm localization or less, considering the 3 nm average Au overlayer thickness. A 1 hour, 800°C anneal removes this 1.9 eV feature, along with some 2.3 eV emission. Conversely, 1 hour, 900 °C annealing adds new emission at 2.5 and ~ 2.8 eV. For Ag, another unreactive metal, deposited on bare SiC in UHV at room temperature, the induced 1.9 eV feature does not change with annealing but extends ~200 nm into the SiC. In contrast, for Ni, a more reactive metal, there are no significant changes with metal deposition and annealing. For Ti, even more reactive, only 2.8 eV peak luminescence increases. The pervasive appearance of 1.9 eV emission and the absence of new gap states due to chemical reaction indicates that native defects rather than extrinsic metal-induced states dominate interface state behavior. [1]A. Itoh and H. Matsunami, Phys. Stat. Sol. (a) 162, 389 (1997); [2]L.J. Brillson, S. Tumakha, G.H. Jessen, R.S. Okojie, M. Zhang, and P. Pirouz, Appl. Phys. Lett. 81, 2785 (2002).

1:50 PM Student

L2, Schottky Diodes on n-Type 4H-SiC Grown by Sublimation Epitaxy and Chemical Vapor Deposition: The Effect of Deep Level Defects: *Daniel J. Ewing*[1]; Rafal R. Ciechonski[2]; Mikael Syväjärvi[2]; Rositza Yakimova[2]; Lisa M. Porter[1]; [1]Carnegie Mellon University, Matls. Sci. & Engrg., 5000 Forbes Ave., Pittsburgh, PA 15213 USA; [2]Linköping University, Dept. of Physics & Measurement Tech., SE-581 83, Linköping Sweden

In this study the influence of deep levels on the current-voltage (I-V) and capacitance-voltage (C-V) properties of Ni Schottky contacts on n-type 4H-SiC samples grown by either sublimation epitaxy (SE) or chemical vapor deposition (CVD) were investigated. Currently epitaxial layers of 4H-SiC are commercially produced by CVD. This technique uses high purity gases (silane and propane) carried in a high flow of hydrogen and yields epitaxial layers of high purity. The main drawback of the method is the low growth rate, typically ~5μm/hr. Significantly higher growth rates, which are needed for fabricating the thick layers required in power devices, can be achieved by the novel SE technique applied here. The SE growth process is based on the sublimation of a SiC source in vacuum in which collision-free transport is utilized to raise the growth rate up to 50 μm/hr while maintaining device-quality surface morphology and n-type doping in the range of low 10^{15}-10^{16} cm^{-3}. The contacts studied in this work were deposited on SiC epilayers fabricated by both techniques in order to provide a larger data set for the analysis and conclusions. The I-V and C-V data showed that near-ideal diodes could be fabricated on both types of samples. Measurements of the deep level concentrations using deep level transient spectroscopy (DLTS) indicated the presence of primarily Z_1/Z_2 defects with concentrations ranging from 1.68-7.00 x 10^{13} cm^{-3} and 1.05-2.00 x 10^{13} cm^{-3} for the sublimation epitaxy and CVD samples, respectively. Data from I-V measurements of numerous Schottky diodes on both types of samples showed that the ideality factors and reverse leakage currents had direct correlations with the deep level concentrations, whereas the barrier heights and the doping concentrations showed inverse correlations with the deep level concentrations. The variations in the barrier heights (and ideality factors) were ϕ_B = 0.88-1.26 eV (n = 1.16-2.65) and ϕ_B = 0.94-1.38 eV (n = 1.04-1.33) for the SE and CVD samples, respectively. Extrapolation of t he barrier heights calculated from I-V measurements to n = 1.0 yield values that approach the average barrier heights calculated from C-V measurements (1.4 eV). These trends, along with additional details about the growth methods, the specific defects, and their implications on electrical properties, will be presented.

2:10 PM Student

L3, Mechanism of Ohmic Behavior of Al/Ti Contacts to P-Type 4H-SiC After Annealing: *Brian J. Johnson*[1]; Michael A. Capano[1]; [1]Purdue University, Elect. & Computer Engrg., 465 Northwestern Ave., W. Lafayette, IN 47907 USA

A great deal of research has been focused on aluminum-titanium contacts to p-type silicon carbide, but there is still no consensus on the mechanism of ohmic behavior in this contact system. Proposed mechanisms have generally involved heavy doping of the semiconductor surface by diffused aluminum, and electric field enhancement by surface morphology modification. In this talk, we will show that these mechanisms actually contribute little or nothing to the ohmic behavior of Al-Ti contacts to SiC. Instead, we find that the ohmic behavior is due primarily to the reactive formation of interfacial alloys such as Ti3SiC2 and Al4C3. In our experiments, aluminum and layered Al-Ti contacts of varying composition were deposited by electron-beam evaporation, vacuum-annealed for two minutes at 1000°C, and capped with gold. Electrical measurements were then taken, resulting in specific contact resistances of 2.5 - 4.2 x 10-4 ohm-cm2. The contacts were then etched off with acids and the resulting surfaces examined by atomic-force microscopy (AFM) to determine pitting depth and density. Next, the contacts were re-capped with gold and electrical tests were repeated. The aluminum contacts were non-ohmic and the Al-Ti contacts ranged 3.6 - 5.9 x 10-3 ohm-cm2, an

approximately one order of magintude increase in resistivity. This rules out the heavy-doping theory because, if heavy doping of surface SiC were responsible for ohmic behavior, then the contacts should not have been made worse by the liquid etch; indeed, they should have been improved, because gold has a lower Schottky barrier to p-type SiC than does either aluminum or titanium. Finally, the gold was etched away in acid and the contacts were argon-ion-milled to a depth of approximately 165 nm. The contacts were inspected by AFM to ensure that surface morphology had not significantly changed, gold caps were re-deposited, and electrical tests were performed. None of the contacts was found to be ohmic after the argon etch. This rules out the field-enhancement theory of ohmic behavior, leaving only alloy-assisted transport as a possible mechanism of ohmic behavior. X-ray diffraction studies, as well as transmission electron microscopy by other researchers, point to the identities of these alloys being Ti3SiC2 and Al4C3, depending on the aluminum-titanium ratio. The precise mechanisms by which these alloys cause ohmic conduction will be presented and discussed.

2:30 PM Student

L4, In-Situ Characterization of Ohmic Contacts to N-Type SiC Under High Temperature and Current: *David DeAngelis*[1]; Robert S. Okojie[2]; [1]Carnegie Mellon University, Elect. & Computer Engrg., 5000 Forbes Ave., Pittsburgh, PA 15213 USA; [2]NASA Glenn Research Center, Sensors & Elect. Tech. Branch, 21000 Brookpark Rd., MS 77-1, Cleveland, OH USA

We report the results of the in-situ characterization of Ti/TaSi$_2$Pt ohmic contacts to 6H-SiC during high temperature and current accelerated stressing. Several 6H-SiC four-point probe test structures are exposed to a constant current of 1 mA and temperature up to 600°C in air ambient at intervals of 100 hrs up to 400 hrs. The insertion of SiC devices into the critical sections of the propulsion systems and on-board electronics and sensors for planetary missions to harsh planets (i.e., Venus) and other cosmic bodies will require that these devices survive and operate reliabily during the entire mission. The temperature in these environments is sometimes greater than 500°C and with high radiation values. Thus, the goal of this work is to evaluate the long term stability and reliability of Ti/TaSi$_2$Pt ohmic contact metallization to 6H-SiC under simulated constant operating conditions at high temperature. The current-voltage (I-V) characteristics, the series resistance, and the specific contact resistance (SCR) of the test structures are measured in-situ under the above environmental conditions. After every 100 hrs of heating at 600°C in air and at 1 mA, the samples are cooled and similar measurements are repeated. The results are then compared to determine deviations from the initial values. Unstable voltage offsets that precede the eventual failure of SiC devices have been largely attributed to the electrical instability at the semiconductor metallurgical junction. Another marker of premature failure is associated with the irreversible drift of the device reading during operation. One source of drift is likely due to microstructural changes in the material after extended current stressing. Before the contact resistance is measured, the ohmic behavior of the test structure is verified. The device is heated in the atmosphere from room temperature to 600°C. The temperature effect on the resistance shows a non-linear behavior, starting with a high resistance at room temperature and gradually decreasing. From about 250°C, the resistance begins an upward swing and continues to 600°C. This behavior is explained by the dominance of impurity and phonon scattering mechanisms on current transport at temperature below 250°C and above, respectively. The plots of the resistance versus temperature during the various 100 hr cyclic soaking period do not track perfectly as is expected under ideal conditions, thus suggesting that microstructural changes are occurring either within the metal contact (e.g., phase transformation), at the metallurgical junction (e.g., chemical reaction), or within the crystal. With regard to the SCR, it is initially measured to be 4 x 10^{-4} cm^2 and remains constant over the temperature range after the first 100 hrs. However, a factor of two increase is observed after 400 hrs of soak at 600°C in air, even as the SCR remain relatively constant at the new values. At the talk, transmission electron microscopy and scanning electron microscopy analyses will be used in conjunction with the I-V characteristics to discuss the failure mechanisms.

2:50 PM Student

L5, Ta-Ru-N Diffusion Barriers for High-Temperature Metallizations to SiC: *C. M. Eichfeld*[1]; M. A. Horsey[1]; S. E. Mohney[1]; A. V. Adedeji[2]; J. R. Williams[2]; [1]Pennsylvania State University, Matls. Sci. & Engrg., Univ. Park, PA 16802 USA; [2]Auburn University, Physics Dept., AL 36849 USA

There is a need for diffusion barriers for contacts to SiC for devices that must operate at high temperature in air. In this study, Ru was selected as one component of ternary Ta-Ru-N barrier layers, since RuO_2 is a metallic conductor, and it was speculated that the barriers might remain electrically conductive even after they begin to oxidize. The elements Ta and N were selected because of their utility in other diffusion barriers. The Ta-Ru-N barriers were deposited by reactive sputtering in Ar-N_2 gas and were tested on ohmic contacts to heavily doped p-type 4H SiC. Barriers with varying Ta, Ru and N concentrations were compared on both Ni and Al/Ni ohmic contacts. Processing conditions were chosen to optimize the adhesion of the barrier layers to the ohmic contacts and to minimize specific contact resistances. Annealing the barrier along with the ohmic contacts was required for good adhesion to the Ni contacts. These samples were annealed at 950°C for 60 s. On the other hand, adhesion of the barriers to the Al/Ni contacts was good even if the barrier was deposited after the contact was annealed, in this case at 850°C for 60 s. Furthermore, the resistance of the Al/Ni contacts was lower when the barriers were deposited after the contacts were annealed. Finally, top layers of Pt, Sn, and Au were added to all samples prior to long-term aging at 350°C in air, as these layers are often needed for packaging. Upon aging in air at 350°C, all ohmic contacts showed an initial change in specific contact resistance after 25 h but stabilized by 100 h. The Ni and Al/Ni ohmic contacts beneath a barrier of roughly equal concentrations of Ru and Ta exhibited average specific contact resistances of 4 x 10^{-4} Ohm cm^2 and 7 x 10^{-5} Ohm cm^2 after 100 h in air at 350°C. After 1500 h, the specific contact resistance did not change further. With a more Ru-rich barrier, Ni and Al/Ni ohmic contacts exhibited average specific contact resistances of 3 x 10^{-5} Ohm cm^2 and 4 x 10^{-5} Ohm cm^2, respectively, after 100 h. They changed very little to 4 x 10^{-5} Ohm cm^2 and 4 x 10^{-5} Ohm cm^2 after 1500 h. X-ray diffraction of the barrier layers prepared without the other metallization layers was performed for samples aged in air and evacuated quartz tubes. All barriers remained amorphous after at least 250 h (the longest time tested), with the exception of the Ru-rich barrier aged in air, which showed initial signs of crystallization between 100 and 250 h.

3:10 PM Break

Session M: Non-Destructive Testing and In-Situ Monitoring-Control

Wednesday PM Room: 140
June 23, 2004 Location: DeBartolo Hall

Session Chairs: Kurt G. Eyink, Air Force Research Laboratory, Wright Patterson AFB, OH 45433-7707 USA; Mark S. Goorsky, University of California, Dept. of MSE, Los Angeles, CA 90095-1595 USA

3:30 PM Student

M1, Interpretation of Prism-Coupled Optical Reflectivity Measurements from He-Implanted Single Crystal PZN-PT Waveguides: *Aijie Chen*[1]; M. Levy[1]; P. D. Moran[1]; [1]Michigan Technological University, Matls. Sci. & Engrg., 1400 Townsend Dr., Houghton, MI 49931 USA

This work reports on the realization of optical waveguides in PZN-PT. Single crystal bulk PZN-PT is a relaxor ferroelectric with unusually large electro-optic and piezoelectric coefficients. The goal of this work is to develop a deeper understanding of how He ion implantation can be used to engineer the depth-dependent change in refractive index of PZN-PT for fabricating optical waveguide devices. A methodology for extracting the depth dependence of the refractive index from prism-coupled optical reflectivity data is applied to study of the manner in which high energy He+ ion implantation impacts the refractive index in single crystal PZN-PT waveguide structures. Prism coupled reflectivity measurements from 001-oriented 4.5%PZN-PT samples implanted with

1.0 MeV He ions for doses varying from 0.75x 1015 up to 100 x 1015 He ions /cm2 and for 3.8 MeV He ions for doses varying from 10x1015 up to 100x1015 He ions /cm2 are collected . A method for interpreting prism coupled waveguide data from structures with an arbitrary smoothly varying depth-dependent refractive index profile based on the Chandler-Lama reflectivity matrix formalism is then described. This method is implemented to extract from the prism coupling data the shape of the refractive index depth profile in implanted PZN-PT as a function of implant dose and energy. These results are interpreted in terms of the physical processes resulting in the refractive index modulation and the manner in which He ion implantation can be used to fabricate single-mode optical waveguides in PZN-PT.

3:50 PM Student
M2, Investigation of Longitudinal Optical Phonon Plasmon Coupled Modes in SiC Epitaxial Film Using FTIR: *Swapna Geetha Sunkari*[1]; Michael S. Mazzola[1]; Janice P. Mazzola[2]; Jeffery L. Wyatt[1]; [1]Mississippi State University, Elect. Computer Engrg., 216 Simrall Engrg. Bldg., Hardy Rd., Starkville, MS 39759 USA; [2]SemiSouth Laboratories Inc., One Rsch. Blvd., Ste.201B, Starkville, MS 39759 USA

Room Temperature Fourier Transform Infrared Spectroscopy (FTIR) was performed on heavily doped and lightly doped 4H-SiC epitaxial layers grown by Chemical Vapor Deposition on both conducting and semi-insulating substrates. Free carrier concentration and film thickness have been measured. A model based curve fit of the experimentally observed reflectance spectra from these samples is performed using a dielectric function that accounts for the phonon-photon coupling and plasmon-photon coupling. Different portions of the infrared spectrum yield information about the thickness and free carrier concentration. From the reflectance data experiments we find that the interference shape of the resulting infrared spectrum between 1000 cm-1 and 6000 cm-1 is mostly sensitive to the thickness of the film stack, and between 600 cm-1 and 1200 cm-1 is mostly sensitive to the free carrier concentration. The experimentally observed shift in the longitudinal optical phonon (ùLO) frequency with respect to carrier concentration was previously reported.[1] It has been observed that the interface between lightly and heavily doped epitaxial layers can be easily resolved because of the appreciable difference in the index of refraction introduced by the large difference in the free carrier concentrations, however the interface between two lightly doped epitaxial layers is more difficult to resolve. Better resolution may be possible by taking into account the phonon plasmon coupling. In this work, the complex dielectric functions of the films were obtained by fitting the measured reflectance spectra with separately measured dielectric functions of the bare substrates. The shift in the longitudinal optical phonon frequency with respect to carrier concentration is observed and has been explained by the phonon plasmon coupling. The free carrier concentration is derived from the dielectric function taking into account the plasmon photon coupling and also by considering the small perturbations caused by phonon plasmon coupling. The shift in the ùLO peak towards higher wave numbers is observed which is consistent with results reported from Raman spectroscopy.[2] The measurements were taken at various points across the wafer and the spatial mapping of carrier concentrations is presented. The thickness and carrier concentrations of the epi layers on both semi-insulating and conducting substrates are presented. [1]SiC Epitaxial Film Characterization using FTIR and improve parameter estimation M.S.Mazzola, J.P.Mazzola, S.Sunkari, and Y.Koshka, Presented at the EMC, L1, 3.30pm on June 26th, UTAH. [2]Raman Scattering from anisotropic LO-phonon-plasmon-coupled mode in n-type 4H- and 6H-SiC, H.Harima, S.Nakashima and T.Umera, J.Appl Phys., 78, 1996 (1995).

4:10 PM
M3, Spectroscopic Ellipsometry Analysis of the Critical Point Structure of InAs/GaSb Strain-Layer Superlattices: *K. G. Eyink*[1]; H. J. Haugan[1]; G. J. Brown[1]; D. H. Tomich[1]; L. Grazulis[1]; F. Szmulowicz[1]; [1]Air Force Research Laboratory, AFRL/MLPS, 3005 Hobson Way, Wright-Patterson AFB, OH 45433 USA

We have used spectroscopic ellipsometry to investigate the InAs/GaSb short period superlattices (SPSs), grown by molecular beam epitaxy, with InSb or uncontrolled interfaces. These SPSs have been receiving considerable attention due to the ability to tune the absorption edge from ~2ìm to at least 24ìm by changing the in SPSL component layer thickness. In this study, we have examined the optical properties of SPSs grown with a band gap in the range of 3-5ìm. All layers were analyzed using spectroscopic ellipsometry in the range 2-4eV. Room temperature measurements showed the critical point structure for the E1 and E1 + D associated with the GaSb and InAs. The E1 critical point associated with the GaSb was observed to shift higher energies as either the thickness of the GaSb or the InAs layers increased. The potential of using the critical point energies for thickness determination will be discussed.

4:30 PM
M4, A Fast, Direct and Fully Automated Measurement of Layer Relaxation Using X-Ray Diffraction: *Paul Anthony Ryan*[1]; Kevin M. Matney[2]; Petra Feichtinger[2]; [1]Bede Scientific Instruments Ltd., Belmont Business Park, Belmont, Durham, Co Durham DH1 1TW UK; [2]Bede Inc., 14 Inverness Dr. E., Ste. H-100, Englewood, CO 80112 USA

We have developed a method for measuring relaxation of epi-layers which requires no a-priori knowledge of the composition or relaxation and can be automatically performed in minutes. Unlike traditional methods, the resulting data requires no complex analysis or user intervention. The relaxation and composition values provide information about the in-plane lattice parameter of the layer, which may be of interest for the growth properties of subsequent layers. The technique can be applied to patterned production wafers, making monitoring layer relaxation possible in a production environment. Traditional methods for measuring relaxation typically require either a priori knowledge of the relaxation and composition, or multiple asymmetric scans taking many hours. The analysis of such methods is complicated and requires manual processing. The method presented here only requires 2 experimental scans, with no assumptions made about the relaxation or composition. The new method presented here involves scanning along the in-plane lattice parameter of the layer, measuring at every value of relaxation for a given composition. Because of this approach, a profile of the relaxation distribution is created, rather than in the traditional method where an average relaxation value for the whole illuminated area is obtained. This can indicate whether a layer is the onset of relaxation or whether there are regions of relaxed material amongst a fully strained layer (for example, edge effects during selected area growth on patterned wafers). This information about the device structure on product wafers can prove invaluable. Examples from fully strained (used in SiGe HBT - type structures) and fully relaxed SiGe layers on Si (used in strained-Si layers) are presented to illustrate the technique and information available.

Session N: Nitride HEMTs: RF Dispersion and Passivation

Wednesday PM Room: 155
June 23, 2004 Location: DeBartolo Hall

Session Chairs: Michael Manfra, Lucent Technologies, Bell Labs., Murray Hill, NJ 07974 USA; Christian Wetzel, Uniroyal Optoelectronics, Tampa, FL 33619 USA

1:30 PM
N1, Characterization of Trapping Centers in the Structure of AlGaN/GaN HEMTs: *Oleg Mitrofanov*[1]; *Michael Manfra*[1]; [1]Lucent Technologies, Bell Labs., 600 Mountain Ave., Murray Hill, NJ 07974 USA

RF dispersion, caused by the presence of charge trapping centers within the device structure, continues to limit the performance of AlGaN/GaN high electron mobility transistors (HEMTs). Identification of the trapping centers in the actual devices and estimation of their densities and location is essential for finding correlations between the epitaxial growth conditions and the presence of the trapping effects. Our AlGaN/GaN HEMTs grown by MBE typically show small RF dispersion and gate lag. For certain growth conditions, these trapping effects are negligible. Using transient current spectroscopy with tunable trap filling conditions, several trapping centers can be identified within the structure of our devices. In this study we present a detailed characterization of one of the trapping centers present in GaN/AlGaN/GaN HEMTs. The trap characteristics are obtained from an analysis of the electron capture and emis-

sion processes. Electron capture occurs in the vicinity of the gate contact via tunneling through the Schottky contact. The electrons trapped in the barrier of the transistor partially deplete the two-dimensional electron gas and limit the maximum drain current. Due to the presence of strong electric fields, the field-assisted effects must be taken into account when characterizing the trapping centers in the barrier. We demonstrate that the leading mechanism of electron emission from the traps at room temperature is the field-assisted Poole-Frenkel (PF) emission. According to the PF model the emission rate increases exponentially with the applied field. This functional dependence is clearly observed in our samples. In addition, the apparent activation energy of the trap extracted from the temperature dependence of the emission rate decreases with the applied field and confirms the physical mechanism of emission. By fitting the expression for the PF emission rate to the experimental data obtained at various temperatures and fields, we estimate the characteristics of the observed trapping center. We show that the energy level of the traps lies ~0.5 eV below the conduction band minimum. The level is located much deeper inside the bandgap than expected from the standard activation energy measurements, which typically give the values of 0.1-0.2 eV. The functional dependence of the emission rate on the electric field suggests that the trapping center is described by the long-range Coulomb attractive potential. We also estimate that the strength of the electric field acting on the trapped electron is ~1-3 MV/cm. Such strong fields exist only in one area of the device: in the barrier under the gate contact. The study provides insight into the physics of the trapping effects in AlGaN/GaN HEMTs.

1:50 PM Student

N2, Reduction of Current Collapse in an Un-Passivated AlGaN-GaN Double-Channel HEMT: *Rongming Chu*[1]; Yugang Zhou[1]; Jie Liu[1]; Kevin J. Chen[1]; Kei May Lau[1]; [1]Hong Kong University of Science & Technology, Dept. of Elect. & Elect. Engrg., Clear Water Bay, Kowloon, Hong Kong

HEMTs made of wide-bandgap AlGaN/GaN heterostructures features high current density and breakdown field, but are usually plagued with current collapse problem. Under high-frequency large-signal drive, the output current swing usually shows severe collapse, resulting in reduced efficiency and output power density. Incorporation of surface passivation layer such as Si3N4 sometimes alleviates the current collapse, but is not always effective. In this study, we characterize and analyze the current collapse phenomenon in an un-passivated AlGaN/GaN/AlGaN/GaN double-channel HEMT. The AlGaN/GaN/AlGaN/GaN double-channel HEMT was grown on a sapphire substrate by MOCVD method. Polarization effect induces two 2DEG channels at the upper and lower AlGaN/GaN interfaces respectively. The lower AlGaN barrier layer was designed to have low Al composition and small thickness to allow low source/drain access resistance to the lower channel and hard pinch-off. DC-IV measurement of the double-channel HEMT reveals a distinct double-hump structure in the transconductance characteristics, corresponding to the effective gate modulation to the upper and lower 2DEG channel respectively. The unique double-channel behavior manifests itself at microwave frequencies. Dynamic IV measurement was carried out to simulate RF large-signal behaviors of the AlGaN-GaN double-channel HEMT. Drain current value at each bias point of the I-V plane are obtained by pulsing the gate and drain bias synchronously from a quiescent point to the bias point under testing. Similar to what observed in AlGaN/GaN single-channel HEMTs, the AlGaN-GaN double-channel shows collapse of drain current when the drain bias is pulsed toward a lower value and/or the gate bias is pulsed toward a less negative value. i.e., During RF large-signal operation, upside waveform of the output signal more likely suffers from current collapse, while the downside waveform of the output signal remains un-collapsed. This observation is consistent with the model which attributes current collapse to trapping/de-trapping at the surface of the gate-to-drain region. Plotting measured dynamic IV characteristics in the transfer curve fashion, we clearly observed that current collapse only happened for the upper channel with a drastic reduction of transconductance, while the lower channel is collapse-free. This novel feature further supports the surface trapping model. In the gate-to-drain spacing region, the upper channel has a large number of mobile carriers and effectively screens the lower channel from voltage fluctuations on the surface. As a result, surface trapping/de-trapping has little chance to reduce the current or delay the frequency response of the lower channel. From this point of view, current collapse has a chance to be reduced on a reproducible basis through the structure optimization of double- or multiple- channel HEMTs with properly managed carrier density in each channel. RF power and linearity characterization of the double-channel HEMT confirmed conclusions drawn from the dynamic IV measurement.

2:10 PM Student

N3, Effect of Different SiN_x Passivation and Their Strain on the Reliability of GaN-Based HEMT Structures: *Zhihong Feng*[1]; Yugang Zhou[1]; Shujun Cai[1]; Kei May Lau[1]; [1]Hong Kong University of Science and Technology, Dept. of Elect. & Elect. Engrg., Clear Water Bay, Kowloon, Hong Kong

AlGaN/GaN high electron mobility transistors (HEMTs) have shown great potential for high voltage, high temperature and high power operation at microwave frequencies.[1] However, the study on the reliability of GaN-based devices is still at the initial stages. Several mechanisms have been identified, as the causes, including the presence of surface states that presumably deplete channel charges during large signal operation. Several studies have shown that the use of a proper passivation material such as SiNx can minimize or prevent current collapse.[2,3] SiNx prepared in different ways may lead to different passivation performance. In this work, 50 nm thick SiNx layers were deposited using plasma-enhanced chemical vapor deposition (PECVD) under two different frequencies (13.56 MHz for HF-SiNx and 380 KHz for LF-SiNx). After annealing at 500°C in N2 ambient for up to 170 hours, the passivation effect of the SiNx layers on the GaN/AlxGa1-xN/GaN high electron mobility transistor (HEMT) structures were evaluated. AlGaN/GaN heterostructures were grown by metalorganic vapor phase epitaxy (MOVPE) on 2'' epi-ready sapphire substrates. A GaN cap layer of 2 nm was grown to intentionally reduce the surface states and the oxidation of the surface of AlGaN. The Al mole fraction determined by X-ray diffraction was around 30%. The mobility and sheet charges of the 2DEG of the structure were measured and monitored by standard Hall-measurements. Without any passivation, an irreversible (µ-Ns) degradation of the HEMT structure was observed after 30 hours of annealing. The high frequency HF-SiNx provided superior long-term stability to the HEMT structure, with no change in 2DEG behavior (µ-Ns) after 170 hours of aging. However, significant degradation was found for samples passivated by low frequency LF-SiNx before annealing. After annealing, a partial recovery of the 2DEG behavior was observed for these LF-SiNx passivated samples. A stress state change from compressive stress to tensile stress for LF-SiNx and the tensile stress enhancement for HF-SiNx on 4'' Si-wafer were observed due to the SiNx layer densification after the annealing. Based on the comparison of the initial annealing behavior of HF/LF SiNx and the stress of HF/LF SiNx on 4'' Si-wafer, the long-time reliability could be explained as a consequence of piezoelectric effects enhancement by a denser SiNx passivation solidification. [1]S. C. Binari, J. M. Redwing, G, Kelner, and W. Kruppa, Electron. Lett. 33, 242 (1997). [2]G. Simin, A. Koudymov, H. Fatima, J. Zhang, et al. IEEE Electron Device Lett. 23, 458 (2002). [3]M. Ochiai, M. Akita, Y. Ohno, et al. Jpn. J. Appl. Phys. 42, 2278 (2003).

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N4, Passivation of GaN and AlGaN Using Ex-Situ UV-Ozone and MBE Grown Oxides: *Brent P. Gila*[1]; A. H. Onstine[1]; M. Hlad[1]; R. Frazier[1]; G. T. Thaler[1]; A. Herrero[1]; R. Mehandru[2]; J. LaRoche[2]; S. Kim[2]; E. Lambers[1]; C. R. Abernathy[1]; F. Ren[2]; S. J. Pearton[1]; N. Moser[3]; R. Fitch[3]; [1]University of Florida, Matls. Sci. & Engrg., PO Box 116400, Gainesville, FL 32611-6400 USA; [2]University of Florida, Chem. Engrg., PO Box 116005, Gainesville, FL 32611-6005 USA; [3]Air Force Research Laboratory, Electron Devices Branch, Wright-Patterson AFB, OH 45433 USA

Gallium Nitride (GaN) field effect transistors (FETs) have attracted considerable interest as high power electronics for use in the electric utility industry, defense and space applications, and hybrid vehicles. GaN based HEMT devices are more highly developed and are now being fabricated into preliminary MMIC prototypes. However, one major concern with the GaN HEMT device is the reduction of drain current under high source-drain voltage applications. This phenomenon, known as current collapse, is believed to be due to traps at both the exposed surface and in the underlying GaN buffer. Currently, this problem is greatly reduced by the addition of a dielectric on the top surface of the fabricated HEMT, which acts as a passivation layer to reduce the surface electrical traps. Another point of interest concerning the passivation is its influence on the device isolation current. This talk will discuss the effects of substrate surface preparation of GaN and AlGaN, both in-situ and ex-situ

and the subsequent gas-source MBE growth of Sc_2O_3. Surface preparation techniques have been explored on the GaN using RHEED, AES, SIMS and C-V measurements. A similar study of the as-fabricated HEMT surface was carried out to create a cleaning procedure prior to dielectric passivation. Post-deposition materials characterization included AES, AFM and XPS, as well as gate pulse and isolation current measurements for the passivated HEMT devices. All oxide growth was carried out in a Riber 2300 MBE using MOCVD grown n-GaN/sapphire or processed AlGaN/GaN HEMT substrates. Surface preparation of the as-received n-GaN substrates and the AlGaN/GaN HEMTs will be discussed. Substrate growth temperature was 100°C and scandium oxide film thickness was 10nm. A corresponding interface state density of 7E11 $cm^{-2}eV^{-1}$ was calculated for the oxide/GaN test diode using the AC conductance method. The recipe for the Sc_2O_3 was then employed on the AlGaN HEMTs for passivation and device isolation. The resulting process has led to the near elimination of the current collapse phenomenon on MOVCD grown HEMTs. Additionally the passivation also provides for low leakage current, nA range, for device to device isolation. Without this passivation technique, the isolation current rises into the µA range. This rise in isolation current is also seen when SiO_2 and SiN_X are employed as passivation. Recently, it has been shown that the GaN terminated HEMT structure is more readily passivated than the AlGaN terminated HEMT structure. On average, GaN terminated HEMTs show a 10% higher passivation (90% dc current) than AlGaN terminated HEMTs (80% dc current). This is also seen in the XPS results from the surface analysis. The UV-ozone produced oxide shows a 5.0 eV shift in XPS spectra verses a 0.7 eV shift fro the AlGaN surface. This indicates that the GaN ozone oxide is more insulating than the AlGaN ozone oxide.

2:50 PM Student

N5, Successful Passivation of GaN/AlGaN HFET by Use of Spin-Deposited Polyimide: Mark D. Hampson[1]; *Uttiya Chowdhury*[2]; Michael M. Wong[3]; Dongwon Yoo[2]; Xuebing Zhang[2]; Milton Feng[1]; Russell D. Dupuis[2]; [1]University of Illinois, Micro & Nanotech. Lab., 208 N. Wright, Urbana, IL 61801 USA; [2]Georgia Institute of Technology, Sch. of Elect. & Computer Engrg., 778 Atlantic Dr., Atlanta, GA 30332-0250 USA; [3]University of Texas, Microelect. Rsch Ctr., 10100 Burnet Rd., Austin, TX 78758 USA

Nitride based HFETs are of key technological interest due to their potential to deliver high-power, high-frequency operation. In the present state of the technology, probably the biggest challenge facing further performance improvement is deterioration of RF performance resulting from carrier trapping from surface traps. It is well acknowledged that a suitable surface passivation technique needs to be in place in order to obtain good RF performance. We report on the successful use of spin-deposited polyimide for the passivation of III-nitride HFETs. The device structure studied was fabricated from an AlGaN/GaN heterostructure grown by low-pressure metalorganic chemical vapor deposition (MOCVD). The substrate used was 4H semi-insulating SiC. Growth was initiated with high-temperature grown AlN nucleation layer on which a thick GaN:ud layer was grown. After the GaN layer, a thin AlN spacer layer is grown followed by a 30 nm $Al_{0.2}Ga_{0.8}N$ layer. The AlGaN layer consists of a Si delta-doping spike at a distance of 5 nm from the AlN-AlGaN interface in order to provide higher sheet concentration in the 2DEG. Room-temperature Hall-effect measurements for a wafer with the same layer structure grown on a 6H-SiC substrate yielded a mobility of 1052 cm^2/V-s with a sheet concentration of 2.431013 cm^{-2}. Contact-less resistivity measurement shows a sheet resistivity of ~400 Ω /square. Low-frequency C-V measurements shows a sharp depletion at a pinch-off voltage of ~6.6 V. The position of the 2DEG calculated from the C-V data also matches with the expected value. X-ray dynamic diffraction simulation shows a close match between the measured and simulated diffractogram. The as-grown epitaxial layers were processed into devices with a two-finger geometry with 2 x 75 µm total gate-width and 0.23 µm gate length. Chlorine-based dry etching process using an ICP-RIE was used to obtain device isolation. Ohmic metal used for source and drain contacts consisted of a four-layer metal stack of Ti/Al/Ni/Au. The gate pattern was created using e-beam lithography with a Ni/Au Schottky metallization scheme. To obtain passivation, a 4:1 polyimide to thinner mixture was spun on the devices, which was subsequently cured at 300 C to ensure a low-stress film for surface passivation. The processed devices were tested for RF performance under both unpassivated condition and after passivation using spin-deposited polyimide. RF measurement was performed at a frequency of 18GHz. The passivation scheme yielded an improvement of power density from 2.14 W/mm to 4.02 W/mm and improvement of power-added-efficiency from 12.5% to 24.47%. Additionally, the passivated devices demonstrated a peak RF power density of 7.65 W/mm with a peak power-added-efficiency (PAE) of 22.58%. This high power density and PAE demonstrates the promise of this technology.

3:10 PM Break

Session O: Wide Bandgap Light Emitting Diodes

Wednesday PM Room: 155
June 23, 2004 Location: DeBartolo Hall

Session Chairs: Russell D. Dupuis, Georgia Institute of Technology, Sch. of Elect. & Computer Engrg., Atlanta, GA 30332-0250 USA; Andrew A. Allerman, Sandia National Laboratories, Albuquerque, NM 87185 USA

3:30 PM Student

O1, Enhancement of Blue-Light Extraction Efficiency by Surface Texturing: *Shao-Hua Huang*[1]; *Dong-Sing Wuu*[1]; *Ray-Hua Horng*[2]; Tsung-Yu Chen[3]; [1]National Chung-Hsing University, Dept. of Matls. Engrg., 250, Kuo Kuang Rd., Taichung 402 Taiwan; [2]National Chung-Hsing University, Inst. of Precision Engrg., 250, Kuo Kuang Rd., Taichung 402 Taiwan; [3]Advanced Epitaxy Technology Inc., R&D, 119,Kuangfu N. Rd, Hsinchu Industrial Park, Hsinchu 303 Taiwan

GaN related alloy semiconductors with wide band gap ranging from 3.4 to 6.2 eV at room temperature are the focus of current research because of the promise for the use as UV or blue emitters and detectors. For the applications of the next generation lighting, it is necessary to develop the high power and high light excitation blue light-emitting diodes (LEDs) for large-area chips. However, the performance of large-area GaN LEDs is poor if the LEDs were fabricated on the sapphire substrate due to the poor thermal conductivity. To solve this problem, the GaN epilayers with LED structure can be transferred to the other substrate with good thermal conductivity such as Si or metallic material by wafer bonding technology. Moreover, textured lighting-surface of LED could enhance the light extraction efficiency for the large-area LED application. For the highly efficient red/amber LEDs, the textured surfaces were directively obtained by plasma etching on the top epilayer. However, the thickness of top layer p-GaN cladding is thin about 0.4 mm. It is not desirable to directively etching the p-caldding GaN layer due to increasing the resistance of p-GaN after surface textured process, and such treatment might cause electrical deterioration. In previous study, we reported a highly efficient AlGaInP LEDs with mirror substrate (MS). Now, we try to use this technology with the surface roughening to make the high performance blue LEDs. In this study, we used the laser lift-off (LLO) process to separate the GaN film and sapphire substrate after bonded onto the Si substrate. The bonded adhesive layer is used Pd-Au in wafer-bonding process. The surface roughening n-GaN is used the KOH dissolved in ethylene glycol at 120 ~160°C to etch the n-GaN surface. Individual, 1000´1000 mm2, LEDs with a backside contact through the n+-Si substrate were then fabricated. After the processing, with the mirror substrate GaN LED has more 2 times intensity than the original GaN LEDs. With the surface roughening GaN LED can promote more than quadruple light intensity. In the output power, the package surface-textured GaN LEDs with Si substrates can be injected high current up to 1 A due to the Si substrate being good heat sink. Details of processes and data will be described in the full paper.

3:50 PM

O2, Improving the Wavelength-Power Performance in Green GaInN/GaN Light Emitting Diodes: *Christian Wetzel*[1]; Theeradetch Detchprohm[1]; Peng Li[1]; Jeffrey S. Nelson[1]; [1]Uniroyal Optoelectronics, 3401 Cragmont Dr., Tampa, FL 33619 USA

Progress of light emission efficiency in the green and deep green spectral range is crucial for the success of all solid state lighting. High

performance GaInN/GaN quantum well (QW) based light emitting diodes (LEDs) have led to a wide range of commercial applications. Yet, power performance in the green and deep green spectral range is still lagging far behind the development of red and blue. Among the key problems is the observation of a steep roll-off in emission power efficiency when the wavelength is increased from 460 nm in the blue to 525 nm and 545 nm in the green and deep green. The physical reason behind this behavior needs to be identified to overcome such limitations. Many studies in this direction have been hampered by a limited set of available sample data. A meaningful study requires a large base of sample data to meliorate the effects of sample variations across the epitaxial wafer and from growth run to growth run. We analyzed the data of hundreds of growth runs for several distinct epi development stages. In particular, when comparing data for different epi optimization concepts we find a strong variation of their respective roll-off slopes in the green while in the blue performance results are identical. These findings show that the roll-off slopes are not universal and can be controlled at a high performance level by advanced epi optimization. We will discuss the epi optimization processes that lead to either behavior and present performance results of the newly optimized green LED dies (2.4 mW at 20 mA, unpackaged, 527 nm dominant). In particular we find a clear correlation with the morphology of the active region and the role of threading dislocations as will be discussed. We have been able to reduce the surface roughness of the active region from 15.4 nm root mean square, over 0.96 nm to values as low as 0.14 nm. Our results open pathways for new strategies on how to further extend power performance of green and deep green LEDs.

4:10 PM

O3, Electrical and Optical Properties of AlGaInN Based Deep Ultraviolet Light Emitting Diodes Grown on (0001) Sapphire: Boris A. Borisov[1]; Vladimir V. Kuryatkov[1]; Jayant Saxena[1]; Gela Kipshidze[1]; K. A. Bulashevich[2]; I. A. Zhmakin[2]; Sergey Yu. Karpov[2]; Yuri N. Makarov[2]; Mark Holtz[3]; Yuriy Kudryavtsev[4]; Rene Asomoza[4]; *Sergey A. Nikishin*[1]; Henryk Temkin[1]; [1]Texas Tech University, Nano Tech Ctr./Elect. & Computer Engrg., Box 43102, MS-3102, Lubbock, TX 79409 USA; [2]STR Inc., PO Box 70604, Richmond, VA 23255-0604 USA; [3]Texas Tech University, Nano Tech Ctr./Physics, Lubbock, TX 79409 USA; [4]CINVESTAV, SIMS Lab. of SEES/ Elect. Engrg., Mexico D.F. 07300 Mexico

We compare two types of deep ultraviolet (UV) light emitting diodes (LEDs) operating at near 280 nm. LEDs based on digital alloys of AlN/$Al_{0.08}Ga_{0.92}N$ and random alloys of AlGaN were grown by gas source molecular beam epitaxy with ammonia.[1] The digital alloys consist of pairs of 1.00-1.25 nm thick AlN barriers and 0.50-0.75 nm wells of $Al_{0.08}Ga_{0.92}N$. LEDs consist of 50 nm thick AlN nucleation/buffer layers, followed by a ~ 1 µm thick n-type cladding layer with a bandgap of 5 eV, an active layer designed for near 280 nm emission, and a p-type cladding layer with a bandgap of 5 eV, and a contact layer. The cladding layers were constructed either of digital alloys of AlN/$Al_{0.08}Ga_{0.92}N$ or random alloys with an equivalent average AlN content. The n-type cladding layers are transparent at wavelengths longer than 250 nm allowing for emission through the substrate. For n- type digital alloys with the effective bandgap of ~5 eV we obtain electron concentration as high as 2 x 10^{19} cm^{-3} with the mobility of 10 cm^2/Vs. In equivalent random alloys electron concentrations of $1x10^{18}$ cm^{-3} and mobility of 25 cm^2/Vs is reached. In p-type digital alloys hole concentrations of $1x10^{18}$ cm^{-3}, with mobility of 4 cm^2/Vs are measured by Hall experiments. Hole concentrations cannot be measured directly in random alloys with the AlN content of 0.7. Under a constant Mg flux we observe a decrease in hole concentration, from ~10^{18} cm^{-3} to ~10^{15} cm^{-3} as the AlN content is increased from 0 (pure GaN) to 0.4. To assure sufficient conductivity through the structure, devices based on random alloys were terminated with a GaN contact layer. Our experimental results, supported by detailed numerical simulations, show that the main obstacle to high power operation of these devices is the combination of high series resistance and poor carrier confinement. We obtain the lowest series resistance, 60 Ω for a 0.5 mm diameter mesa device based on digital alloy in the p-type cladding layer. Poor carrier confinement can be alleviated only by improved design of the active region. Preliminary experiments show that the addition of undoped, 10 nm thick, AlN barriers on each side of the active layer, results in significant improvement (by at least a factor of 2.5) in the emission efficiency without any change in the electrical characteristics. The introduction of AlN barriers also results in the elimination of the parasitic emission at 320 nm, even under very low excitation current density of 40 A/cm^2. This work is supported by DARPA, NSF (ECS-00700240, 0321186, 0304224), NATO SfP 974505, SBCCOM, and the J. F Maddox Foundation. [1]G. Kipshidze et al, Phys. Stat. Sol. (a), 192, 286 (2002).

4:30 PM

O4, High Performance AlInGaN Ultraviolet Light-Emitting Diode at 340 nm: *S.-R. Jeon*[1]; M. Gherasimova[1]; Z. Ren[1]; J. Su[1]; G. Cui[1]; J. Han[1]; H. Peng[2]; E. Makarona[2]; Y. He[2]; Y.-K. Song[2]; A. V. Nurmikko[2]; L. Zhou[3]; W. Goetz[3]; M. Krames[3]; [1]Yale University, Dept. of Elect. Engrg., New Haven, CT 06520 USA; [2]Brown University, Div. of Engrg., Providence, RI 02912 USA; [3]Lumileds Lighting, LLC, San Jose, CA 95131 USA

The intense pursuit in research toward UV LEDs with emission wavelength below 360nm is fuelled by potential applications such as chemical/biochemical analysis, solid-state lighting, high-density optical storage, and covert communication. Outstanding issues include the enhancement of radiative recombination, the increase of electrical conductivity in p-AlGaN, and further reduction of the dislocation densities. In this work, we report on the performance of AlInGaN UV LEDs at the 340nm wavelength range. The quaternary AlInGaN multiple quantum well active regions are embedded into AlGaN p-n diodes, which are grown on AlN buffer layer on c-axis sapphire substrate using low-pressure metalorganic chemical vapor deposition. Structural characterizations performed using AFM, XRD, and TEM underline the importance of AlN buffer layers. Time resolved photoluminescence (PL) from cryogenic to room temperature (RT) is employed to probe the recombination mechanisms and efficiency of quantum wells. The electrical characteristics of UV LEDs were measured under pulsed current and direct current (DC) operation at RT. An increase of PL decay lifetime during initial temperature rise implies a substantial fraction of radiative recombination; subsequent reduction of the lifetime toward RT is relatively small and a lifetime on the order of 450 psec is typically observed at RT. Circular shape devices with diameters of 100 µm and below have been evaluated with a bottom-emitting scheme through sapphire. Light output power densities exceeding 250mW/mm^2 and an external quantum efficiency of 0.5% at 1.5 kA/cm^2 current density in device with 50µm - diameter have been measured under DC operation using silicon photodiodes directly off a planar device chip (bare-chip). The internal quantum efficiency is estimated to be 10%. The performance of fully packaged, large area LEDs, as well as the effect on the optimization of p-type AlGaN electron blocking layer will also be presented. This research was supported by DARPA SUVOS program under SPAWAR Systems Center Contact No.N66001-02-C-8017.

4:50 PM O5, Late News

Session P: Nanocharacterization II (Including Spintronic Materials)

Wednesday PM Room: 129
June 23, 2004 Location: DeBartolo Hall

Session Chairs: Julia W.P. Hsu, Sandia National Laboratories, Albuquerque, NM 87112-1415 USA; Jacek K. Furdyna, University of Notre Dame, Notre Dame, IN 46556 USA

1:30 PM Student

P1, Spatially Resolved Electroluminescence from Operating Organic Light-Emitting Diodes Using Conductive Atomic Force Microscopy: *Liam S.C. Pingree*[1]; Mathew M. Kern[2]; Brian J. Scott[2]; Tobin J. Marks[2]; Mark C. Hersam[1]; [1]Northwestern University, Matl. Sci. & Engrg., 2220 Campus Dr., Evanston, IL 60208 USA; [2]Northwestern University, Chmst. & Matls. Rsch. Ctr., Evanston, IL 60208 USA

The advancement of materials characterization tools enables detailed studies of complex organic/inorganic systems at the nanoscale. The re-

sults of these studies subsequently allow improved materials development and process optimization. In this paper, organic light-emitting diodes (OLEDs) serve as a testbed to demonstrate the utility and the necessity of this strategy. The miniaturization of OLEDs, with potential applications in ultrahigh density displays and other novel optoelectronic devices, has placed an emphasis on the need to limit the effects of dark spots or non-emissive regions in the material. The effects of small non-emissive regions become enhanced as these devices decrease in size and can lead to significant device-to-device non-uniformities. To study this phenomenon and develop a strategy to limit its effects, we have developed an experimental approach for spatially mapping and correlating, with nanometer scale resolution, topology, current, quantum efficiency, and electroluminescence characteristics of operating OLEDs. Previous attempts to study light emission from these materials include the use of electroluminescence microscopy, near-field scanning optical microscopy, conductive atomic force microscopy (cAFM), and scanning tunneling microscopy. However, none of these techniques have previously been able to simultaneously probe topology, current-voltage response, and electroluminescence-voltage response of a functioning OLED device at the nanometer scale. By combining cAFM with light collection optics and a photomultiplier tube, our newly developed cAFM electroluminescence technique achieves this goal. Both spectroscopic and spatial mapping data have been collected by our technique on 8 micron by 8 micron OLED pixel arrays. The spectroscopic data demonstrates the expected OLED behavior, with a turn on voltage of 7.5 V, initial detectable light emission at 9.5 V, and external quantum efficiency of 0.3%, which agrees with comparable millimeter scale OLED devices. In spatial mapping mode, simultaneous topography, current, and light emission images are acquired on the OLED pixel array at a fixed applied bias. These images illustrate clear spatial variations in the electroluminescence. Although the OLED pixels were fabricated simultaneously and nominally have the same structure, the magnitude of the current and the photon emission differs by up to 60% for neighboring OLEDs in a single array. One possible interpretation of these data is that dark spots have formed on the sub-10 micron length scale. Since the pixels with attenuated photon emission also show reduced current flow, the reduced photon emission cannot be solely attributed to a local reduction in external quantum efficiency, but rather to variations in growth conditions. Besides device-to-device non-uniformities, clear response variations are observed within a given OLED, demonstrating enhanced performance characteristics upon the initial turn-on of the device. In this manner, our cAFM electroluminescence technique not only provides spatially dependent information but also time-dependent device behavior.

1:50 PM Student

P2, Experimental Study of Masking Scheme Effects on the Nanoscale Sidewall Roughness of Deep Etched InP/InGaAsP Heterostructures for Optical Waveguides: *Weifeng Zhao*[1]; Jeong-Oun Bae[1]; Jae-Hyung Jang[1]; Ilesanmi Adesida[1]; M. Kwakernaak[2]; A. Lepore[2]; J. H. Abeles[2]; [1]University of Illinois, Micro & Nanotech. Lab. & Dept. of Elect. & Computer Engrg., Urbana, IL 61801 USA; [2]Sarnoff Corporation, Princeton, NJ 08543 USA

Dry etching of III-V semiconductors is one of the key processing steps in the fabrication of photonic devices based on optical waveguides such as edge-emitting lasers, modulators and add/drop filters. In these device applications, the etched sidewall of waveguides should be very smooth to minimize light scattering loss due to imperfect sidewall profiles. Masking strategy is one of the critical factors that contribute to sidewall roughness (SWR) of waveguides during etching. Our previous study shows the SWR of the InP/InGaAsP optical waveguide becomes larger as the etch depth increases. In this study, the effect of the thickness of the NiCr mask on the sidewall profiles of optical waveguides was experimentally investigated by comparing the SWRs of waveguides etched using several different thicknesses of NiCr layer. The etched waveguide height was kept constant to determine the optimum thickness of the NiCr layer. The fabrication processes used in our work were as follows: a 500 nm-thick SiO_2 was de posited on I nP/InGaAsP heterostructures and specially designed line patterns were written by electron beam lithography. NiCr metal mask patterns were fabricated on the SiO_2 layer using lift-off technique. The resulting composite etch mask consisted of NiCr/SiO_2. Inductively-coupled-plasma reactive ion etching (ICP-RIE) was then utilized to etch high mesa waveguides into the InP/InGaAsP heterostructures. The etched waveguide patterns were cleaved to permit the AFM loaded with a carbon nanotube tip to directly access the sidewall vertically. The selection of the carbon nanotube as the AFM tip was crucial to the success achieved in imaging the whole sidewall areas of the waveguides. The high aspect ratio and the stiffness of the waveguide structures made the measurement processes critical. Our study shows that the SWR in the x direction, i.e., light propagation direction, increased from 2.2 nm to 4.0 nm, and the SWR in the y direction, i.e., the vertical direction, decreased from 19.5 nm to 2.8 nm , as the NiCr layer thic kness increased from 10 nm to 150 nm. The measured power spectra of the sidewall profiles as well as their impact on optical scattering loss will also be discussed.

2:10 PM Student

P3, Multi-Step Feedback Controlled Lithography: A Processing Technique for Fabricating Atomically Registered Organosilicon Heterostructures Using Room Temperature Ultra-High Vacuum Scanning Tunneling Microscopy: *Rajiv Basu*[1]; Nathan P. Guisinger[1]; Mark E. Greene[1]; Mark C. Hersam[1]; [1]Northwestern University, Matls. Sci. & Engrg., Cook Hall - Rm. #2036, 2220 Campus Dr., Evanston, IL 60208 USA

This study demonstrates a fabrication scheme to build molecular nanostructures consisting of distinct chemical species with atomic precision at room temperature. Using the technique of feedback controlled lithography (FCL), the tip of an ultra-high vacuum scanning tunneling microscope is used to desorb individual hydrogen atoms from a hydrogen passivated Si(100)-2×1 surface. Following FCL, organic molecules that are delivered to the surface in the gas phase selectively react with the patterned dangling bonds. Subsequent FCL patterning and gas phase deposition allow distinct molecular species to be bound to the surface in atomic registry with the original pattern. The present study combines this multi-step FCL approach with suitable self-directed growth chemistry to fabricate heteromolecular nanostructures with atomic precision. Specifically, styrene molecules that are known to experience self-directed growth along dimer rows of the Si(100)- 2×1:H surface have been constrained to grow between a pair of individual barrier molecules that have been chemisorbed along the same dimer row using FCL. The molecule chosen to serve as a barrier to chain growth is the free radical TEMPO (2,2,6,6 tetramethyl piperidinyloxy), which requires only a single dangling bond to attach to the silicon surface. Following TEMPO deposition, an individual dangling bond is patterned between the two TEMPO molecules on the same dimer row and styrene chain growth is initiated. The presence of the TEMPO molecules physically restricts the growth of the styrene chain, thus the patterned position of the TEMPO molecules determines the length of the styrene chain. These data not only represent unprecedented control over the fabrication of organosilicon molecular chains but also present new opportunities for studying the properties of hetermolecular nanostructures on silicon surfaces.

2:30 PM

P4, Correlating Atomic-Scale Materials Morphology with Optical Properties of Mid-IR W-Laser Structures: *Georo I. Boishin*[1]; Chadwick L. Canedy[1]; Chul Soo Kim[1]; Igor Vurgaftman[1]; William W. Bewley[1]; Jerry R. Meyer[1]; Lloyd J. Whitman[1]; [1]Naval Research Laboratory, 4555 Overlook Ave. SW, Washington, DC 20375 USA

The active region of mid-IR type-II W-lasers contains three distinct materials, AlAsSb, GaInSb, and InAs, with ideal MBE growth temperatures that differ by more than 100°C. We have found that our devices have optimal photoluminescence (PL) only when grown in a temperature window of 480°C to 510°C. In the literature, similar devices with binary AlSb barriers have had optimal PL intensities when grown at a temperature about 70 °C lower than our samples. We have used cross-sectional scanning tunneling microscopy (XSTM) to characterize the atomic-scale structure of our devices vs. growth temperature. We find that the growth temperature strongly influences the morphology of the AlAsSb and GaInSb layers in ways that can be correlated with the observed variations in the PL. Below the optimal temperature range, 3D clusters of AlAs are observed within the AlAsSb barriers (where the As is deposited as digital monolayers of AlAs). Such degradation in the barriers is consistent with the decrease in PL intensity. Increasing the growth temperature smoothes the AlSb growth front and leads to greater uniformity of the 2D AlAs digital layers. However, a structure grown at 526°C shows evidence of InSb clustering in the GaInSb layers, which could account for the observed rapid drop in PL at temperatures above the optimal range. *Supported by the Office of Naval Research.

2:50 PM P5, Late News

3:10 PM Break

3:30 PM Student

P6, Characterization and Spintronic Applications of ErAs Interlayers in Ferromagnetic Metal/GaAs Heterostructures: *B. D. Schultz*[1]; J. L. Hilton[1]; J. Strand[2]; C. Adelmann[1]; P. A. Crowell[2]; C. J. Palmstrøm[1]; [1]University of Minnesota, Dept. of Chem. Engrg. & Matls. Sci., Minneapolis, MN 55455 USA; [2]University of Minnesota, Sch. of Physics & Astron., Minneapolis, MN 55455 USA

Rare-earth pnictides, such as ErAs, are of interest as diffusion barriers in spintronic devices due to their thermodynamic stability and epitaxial compatibility with a number of compound semiconductors. In-situ XPS studies show that significant interfacial reactions occur when $Fe_{1-x}Co_x$ films are grown by MBE on GaAs surfaces at temperatures above 100°C. Epitaxial $Fe_{1-x}Co_x$ films grown on 5 monolayer (ML) thick ErAs interlayers showed no indication of interfacial reactions at growth temperatures up to 225°C; however, partial monolayer coverages of both Ga and As were observed segregating to the surface during growth. In-situ STM images show that the growth of ErAs films by molecular beam epitaxy (MBE) at 535°C on GaAs(100) surfaces proceeds by the embedded growth mode. The growth begins with island nucleation within the substrate surface where it is energetically favorable for Er to displace Ga from its surface lattice sites. The excess As used during growth results in the displaced Ga forming GaAs on regions of the surface unoccupied by ErAs. Once the ErAs islands reach 3-4 ML in height they begin to grow laterally, which results in additional displacement of GaAs surface layers. After 3-4 ML of growth the ErAs islands coalesce and form a uniform film; however, a portion of the displaced GaAs is trapped on the surface of the uniform ErAs film. The embedded growth mode is observed for ErAs (compressive strain), ScAs (tensile strain), and $Sc_{0.3}Er_{0.7}As$ (lattice-matched) growth on GaAs, with only the lateral size of the nucleated islands being influenced by the strain in the epitaxial layer. The size of the nucleated islands is also observed to be a function of the substrate temperature during growth. The surfaces of the coalesced $Sc_{1-y}Er_yAs$ films were found to contain significant concentrations of both Ga and As, which remained constant with additional $Sc_{1-y}Er_yAs$ growth. The growth of elemental Er on As-rich GaAs (2×4)/c(2×8) surfaces at 450°C initially resulted in the formation of embedded ErAs islands along with a transformation of the surface reconstruction to a Ga-rich (4×2)/c(8×2). This paper reports on the details of the embedded growth mode and the surface composition of $Sc_{1-y}Er_yAs$ films grown by MBE on $Al_{1-x}Ga_xAs$(100) surfaces as characterized in-situ by RHEED, LEED, XPS, and STM. This paper also reports on the subsequent use of these ErAs interlayers as diffusion barriers in $Fe_{1-x}Co_x$/GaAs based spin-LED structures and their effect on spin-polarized transport across the $Fe_{1-x}Co_x/Al_{1-x}Ga_xAs$ interface. This work was supported in part by ONR N/N00014-1-0233 and N00014-02-1-1021, DARPA N/N00014-99-1-1005 and N/N00014-01-1-0830, NSF/DMR-9819659, and AFOSR AF/F49620-98-1-0341.

3:50 PM

P7, Advanced Microstructure Characterization of Epitaxial Semimetallic ErAs Particles in an $In_{0.53}Ga_{0.47}As$ Matrix: *Dmitri O. Klenov*[1]; Daniel C. Driscoll[1]; Arthur C. Gossard[1]; Susanne Stemmer[1]; [1]University of California, Matls. Dept., Santa Barbara, CA 93106-5050 USA

Conventional high-resolution transmission electron microscopy (HRTEM) and high angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) were used to characterize epitaxial metal/semiconductor composites of semimetallic ErAs particles embedded in an $In_{0.53}Ga_{0.47}As$ matrix. These structures were grown by molecular beam epitaxy on semi-insulating (001) InP substrates. HAADF-STEM provides directly interpretable, atomic number sensitive, atomic-resolution images free of strain and interference contrast (caused by the overlap of the particle with the $In_{0.53}Ga_{0.47}As$ matrix along the electron beam direction) typically observed in HRTEM. One deposited monolayer of ErAs formed periodic islands with heights ranging between 4 and 6 unit-cells on the surface of InGaAs. HAADF showed no residual Er on the InGaAs surface outside of the islands. HAADF was also used to determine the crystal structure of the ErAs particles as a function of particle size. The particle shape varied from round to rod-shaped along [1-10] and particles were uniformly distributed. A very low density of planar defects (stacking faults) was observed in the matrix. The ErAs deposition caused an InGaAs surface instability with perturbations of the surface parallel to [1-10]. Additional $In_{0.53}Ga_{0.47}As$/ErAs overgrowth resulted in an unusual microstructure with surface perturbations of subsequent layers shifted parallel to [110] by half a wavelength relative to the underlying layer. The InGaAs layer showed a strong faceting parallel to {113}. Growth of 2.5 nm thick $In_{0.52}Al_{0.48}As$ layers on the ErAs prevented surface roughening, as reported previously.[1] Possible reasons of the surface instability are discussed. [1]D.C. Driscoll, M. P. Hanson, E. Mueller, A. C. Gossard, J. Cryst. Growth 251, 243 (2003).

4:10 PM Student

P8, Reaction Kinetics, Thermodynamics, and Growth Characteristics of Ultra-Thin Mn Films on GaAs(001): *J. L. Hilton*[1]; B. D. Schultz[1]; C. J. Palmstrøm[1]; [1]University of Minnesota, Dept. of Chem. Engrg. & Matls. Sci., Minneapolis, MN 55455 USA

A number of ferromagnetic Mn-based compounds have been grown epitaxially on GaAs, including ferromagnetic metals, diluted magnetic semiconductors, and digital alloys. However, elemental Mn is not thermodynamically stable in contact with GaAs. RBS, XRD, and TEM showed that for 2000Å Mn films deposited in-situ on MBE-grown GaAs(001) epilayers, significant interfacial reactions occurred for post-growth anneals above 200°C. These reactions initially resulted in the formation of a two-phase region of tetragonal Mn_2As and tetragonal MnGa, with an average composition of $Mn_{0.6}Ga_{0.2}As_{0.2}$, and were found to be limited by the rate of Mn diffusion through the reacted region. The two phases formed a mixed-phase epitaxial layer on the GaAs substrate with Mn_2As(001)<100> and MnGa(001)<100> || GaAs(001)<110>. Additional annealing resulted in the dissociation of the $Mn_{0.6}Ga_{0.2}As_{0.2}$ region into a MnGa-like region near the sample surface and a Mn_2As-like region near the GaAs substrate. In order to understand the implications of these reactions for the growth of Mn-based materials on GaAs, the growth characteristics of ultra-thin Mn films were investigated at the atomic scale using in-situ XPS and STM. Atomic layer-by-layer calculations of XPS intensities show that Mn grown on GaAs at 95°C and 250°C forms reacted regions of $Mn_{0.6}Ga_{0.2}As_{0.2}$ with thicknesses of ~10 ML and ~70 ML, respectively. For Mn depositions on the GaAs c(4×4) surface at 95° C, STM studies show the random formation of monolayer-high clusters that coalesce into a uniform film following 1 ML of coverage. On the (2×4)/c(2×8) surface the growth of Mn results in the formation of clusters on the arsenic dimer rows of the GaAs reconstruction that grow in size with increasing coverage. Results from RBS, XRD, and TEM of Mn/GaAs heterostructures will be combined with results from in-situ XPS and STM of 0-50 monolayer Mn coverages to determine the nature and behavior of the reactions between Mn, Ga, and As at the metal-semiconductor interface. This research was supported in part by ONR N/N00014-1-0233 and N00014-02-1-1021, DARPA N/N00014-99-1-1005 and N/N00014-01-1-0830, NSF/DMR-9819659, and AFOSR AF/F49620-98-1-0341.

4:30 PM Student

P9, Nanometer-Scale Studies of Point Defect Distributions in GaMnAs Films: *J. N. Gleason*[1]; M. E. Hjelmstad[1]; V. D. Dasika[2]; R. S. Goldman[1]; S. Fathpour[2]; S. Chakrabarti[2]; P. K. Bhattacharya[2]; [1]University of Michigan, Dept. of Matls. Sci. & Engrg., Ann Arbor, MI 48109 USA; [2]University of Michigan, Elect. Engrg. & Computer Sci., Ann Arbor, MI 48109 USA

GaMnAs and related alloys are promising candidates for spintronic applications compatible with conventional GaAs technologies. The relative arrangements of Mn and other point defects in GaMnAs are expected to significantly impact its electronic and magnetic properties.[1,2] At present, the nanometer-scale details of point defect distributions in GaMnAs are not well understood. Therefore, we have investigated the arrangement of point defects in GaMnAs films grown by low temperature molecular beam epitaxy, using ultra high vacuum cross-sectional scanning tunneling microscopy (XSTM). The heterostructures consist of 10-period superlattices of alternating GaMnAs (0.5, 2.5, and 5.0% Mn) and AlGaAs layers, sandwiched between thick p+ GaAs layers. High resolution constant-current XSTM reveals three types of defects, "M", "A", and "V", associated with substitutional manganese, arsenic antisites, and arsenic vacancies, respectively. "A" and "V" defects are present in all low temperature grown layers, while "M" defects are predominately located within the GaMnAs films. In the low temperature grown GaAs and GaMnAs layers, the concentration of "A" defects is ~1-2x10^{20} cm^{-3}, consistent with typical values reported in the literature.[3] In the GaMnAs layers, the concentration of "V" defects apparently increases with "M" defect concentration, consistent with a Fermi-level dependent vacancy

formation energy.[4] Furthermore, the concentration of "M" defects is typically 3-4 times that of "A" defects, suggesting the possibility of significant compensation of the free carriers associated with substitutional manganese by arsenic antisites. Quantitative A-A, M-M, and A-M pair correlations reveal random distributions for > 2nd nearest-neighbors (NN), suggesting significant repulsion of 1st NN defect pairs. A-V and M-V pair correlations will also be discussed. [1]M. Berciu and R.N Bhatt, Phys. Rev. Lett. 87, 107203 (2001). [2]S. Sanvito and N. Hill, J. Magn. Magn. Mater. 242, 441 (2002). [3]A. Suda and N. Otsuka, Surf. Sci. 458, 162 (2000). [4]W. Walukiewicz, Appl. Phys. Lett. 54, 2094 (1989).

4:50 PM Student

P10, Mn-Doped InAs Self-Organized Quantum Dots with Curie Temperatures Above 300 K: *M. Holub*[1]; S. Chakrabarti[1]; S. Fathpour[1]; P. K. Bhattacharya[1]; Y. Lei[2]; T. D. Mishima[3]; M. B. Santos[3]; M. B. Johnson[3]; D. A. Blom[4]; [1]University of Michigan, Dept. of Elect. Engrg. & Computer Sci., Solid State Elect. Lab., Ann Arbor, MI 48109-2122 USA; [2]Argonne National Laboratory, Matl. Sci. Div., Electron Microscopy Ctr., Argonne, IL 60439 USA; [3]University of Oklahoma, Dept. of Physics & Astron., Ctr. for Semiconductor Physics in Nanostruct., Norman, OK 73019 USA; [4]Oak Ridge National Laboratory, Metals & Ceram. Div., Oak Ridge, TN 37831 USA

Among III-V diluted magnetic semiconductors, (Ga,Mn)As and its heterostructures ($T_C \leq 160K$) have elicited the greatest amount of interest for their potential application in semiconductor spintronic devices. It is clearly desirable to achieve spin injection and device operation at room temperature, rendering (Ga,Mn)As unsuitable for such applications at the present time. We report here the successful low-temperature molecular beam epitaxy (LT-MBE) of Mn-doped InAs self-organized quantum dots (QDs) exhibiting room-temperature ferromagnetism and discuss their structural and magnetic properties. TEM bright field imaging and diffraction analysis show that the InAs:Mn multilayer structures are fully pseudomorphic with respect to the GaAs substrate, but some dislocations, stacking faults, and point defects are generated during low-temperature epitaxy. No evidence of hexagonal, NiAs-type MnAs clusters was observed by TEM imaging nor was a second lattice structure detected by diffraction analysis. A high-resolution, cross-sectional TEM image of a single dot shows that InAs:Mn QDs grown by LT-MBE maintain a zinc-blende crystal structure and are near-pyramidal in shape, having a height and base width of 12nm and 21nm, respectively. Nanoscale variation of the Mn composition within a single QD layer is resolved by EELS analysis using an in-plane Mn L-edge profile. We find that the majority of the Mn dopants are contained within the dot as indicated by an increase in the Mn L-edge peak intensity when the EELS probe scanned over an InAs:Mn dot. XEDS spectra taken from an InAs:Mn QD layer and GaAs cap confirm that Mn resides preferentially inside the InAs:Mn QDs. Furthermore, positional disorder of Mn atoms is evident from comparison of the Mn L-edge profile peak intensities obtained from multiple EELS scans within a single InAs:Mn QD layer. Field-dependent SQUID magnetometry performed at various temperatures reveals a clear hysteresis loop, indicating ferromagnetic order in the InAs:Mn QD multilayer samples. Hysteresis is observed when the field is applied either parallel or perpendicular to the sample surface, but is less pronounced for the case of a perpendicularly applied field. This result suggests that magnetic anisotropy favors in-plane magnetization as expected for compressively strained InAs:Mn QDs grown atop a LT-GaAs buffer layer. We measure T_C=350K in a sample grown using a Mn/In flux ratio of 0.15. The reported Curie temperatures of MnAs and MnGa clusters in Ga(Mn)As are 318K and above 400K, respectively. Thus, an observed Curie temperature of 350K suggests a magnetic response that is either unique to InAs:Mn QDs or As-rich MnGaAs clusters, though significant clustering is not indicated by our material characterization as discussed above. This work is supported by ONR and ARO (MURI program).

Notes

Session Q: High-K Oxides

Thursday AM — Room: 102
June 24, 2004 — Location: DeBartolo Hall

Session Chairs: Evgeni P. Gusev, IBM Corporation, T. J. Watson Rsch. Ctr. USA; T. P. Ma, Yale University, Dept. of Elect. Engrg., New Haven, CT 06520-8284 USA

8:20 AM Student

Q1, Novel Ultra-Thin TiAlO$_x$ Alloy Oxide for New Generation of Gate Dielectric: *Wei Fan*[1]; Bernd C. Kabius[1]; Sanjib Saha[1]; John A. Carlisle[1]; Orlando Auciello[1]; R. P.H. Chang[2]; Ciro Lopez[3]; Eugen Irene[3]; [1]Argonne National Laboratory, Matls. Sci. Div., Argonne, IL 60439 USA; [2]Northwestern University, Dept. of Matls. Sci. & Engrg., Evanston, IL 60208 USA; [3]University of North Carolina, Chmst. Dept., Chapel Hill, NC 27599 USA

According to the technology roadmap for the semiconductor industry, alternative gate oxides with equivalent oxide thickness (EOT) of less than 1.5 nm are critical to satisfy the requirements of sub-100 nm MOSFET devices. Among high-k metal oxides, TiO_2 has been investigated because of its high dielectric constant (>50). However, the use of TiO_2 thin films as gate dielectric was hampered primarily due to its low barrier height with respect to Si. On the other hand, intensive studies have been carried out on Al_2O_3, due to its large band gap (8.8 eV) and thermodynamic compatibility of the interface with Si. The drawback of Al_2O_3 is its relatively low dielectric constant compared with other current leading high-k gate oxides. Therefore, we determined that a hybrid structure including Al_2O_3 and TiO_2 might create a novel material with high dielectric constant and low tunneling current for the next generation MOSFET devices (US patent pending). Ultra-thin TiAl layer with specific composition were grown on Si (100) by sputter deposition. In situ oxidation was then performed by using both molecular oxygen (O_2) (P=1.0x10^{-3} Torr) or atomic oxygen (O) sources (P=1.0x10^{-4} Torr). In situ XPS study showed that a full oxidation of TiAl can be achieved at 500 ^oC using both oxygen sources. However, the TiAlO$_x$ layer formed through atomic oxygen annealing presented a capacitance density 60% higher with a magnitude-lower dielectric leakage than the one via molecular oxygen oxidation. Furthermore, various studies, including in situ XPS, NEXAFS, HR-TEM, showed that a full transition of TiAl to TiAlO$_x$ could be accomplished at even room temperature by exposure to atomic oxygen. Since both Ti and Al have less oxide formation energies than Si and amorphous TiAlO$_x$ exhibits excellent diffusion resistance to oxygen, the presence of Ti and Al at the interface with Si is expected to significantly reduce the formation of interfacial SiO$_x$. Comparing with the high temperature oxidation process which produced a SiO$_x$ interface layer ~1 nm thick, the SiO$_x$ layer formation at room temperature was practically eliminated and an atomic sharp oxide/Si boundary was therefore obtained, as revealed by XPS and TEM. The amorphous TiAlO$_x$ layer with equivalent oxide thickness (EOT) of 1.7 nm and negligible hysteresis was obtained via atomic oxygen oxidation at 500 ^oC, exhibiting a high permittivity (k=30) and low leakage current density (5.4x10^{-5} A/cm^2). As a result of the room temperature oxidation process with the assistance of atomic oxygen which effectively reduced the interfacial layer thickness, stoichiometric TiAlO$_x$ layers with EOT of 0.4-0.5 nm were produced on n$^-$, p$^-$, and n$^+$ Si and a dielectric leakage about 10$^{4-5}$ times lower than that for SiO_2 was also achieved. (This work was supported by the U.S. Department of Energy, BES-Materials Sciences, under Contract W-31-109-ENG-38.)

8:40 AM Student

Q2, Room Temperature Fabrication of $Al_2O_3/TiO_2/Al_2O_3$ Nanolaminates for High-k Gate Dielectrics Structure: *Wei Fan*[1]; Sanjib Saha[1]; Bernd C. Kabius[1]; John A. Carlisle[1]; Orlando Auciello[1]; R. P.H. Chang[2]; [1]Argonne National Laboratory, Matls. Sci. Div., Argonne, IL 60439 USA; [2]Northwestern University, Dept. of Matls. Sci. & Engrg., Evanston, IL 60208 USA

To take advantages of the combination of Al_2O_3 and TiO_2, which exhibits high bandgap and high permittivity, respectively, $Al_2O_3/TiO_2/Al_2O_3$ nanonaminates were developed in our study for a gate dielectric structure with high capacitance density, low leakage and good thermal stability with Si. We report our recent work on in situ chemical and structural characterization of the proposed high-k dielectric stacks with growth, which provided critical information on developing the proper process strategies. Al_2O_3(1 nm)/TiO_2(1 nm)/ Al_2O_3(1 nm) nanolaminates were fabricated by in situ oxidation of Al/Ti/Al multilayers sputtered within an integrated cycle. An atomic oxygen beam, which has high oxidation power and brings no damage to sample surface compared with molecular oxygen or oxygen plasma, was used to oxidize the metal thin layers. Direct oxidation of the Al/Ti /Al stack at low temperature produced Ti suboxides within the interlayer, which induced large dielectric leakage due to the creation of oxygen vacancies. The diffusion resistance of the top Al_2O_3 layer and the relatively higher oxide formation energy of TiO_2 with respect to Al_2O_3 and Ti suboxides suppressed the oxidation of the Ti center layer. Stoichiometric $Al_2O_3/TiO_2/Al_2O_3$ multilayers were produced by the high temperature oxidation process at 500 ^oC. However, the formation of the interfacial SiO$_x$ layer between the dielectric stack and Si substrate was inevitable at high temperature, because of the enhanced mobility of oxygen atoms across the dielectric layer toward the Si substrate. A 2-step oxidation process, involving oxidation of the Ti/Al structure followed by deposition and oxidation of the top Al layer at room temperature, was therefore developed to overcome the partially oxidation problem of the TiO_2 interlayer and to prevent the formation of SiO$_x$ interfacial layer. As a result, a fully oxidized $Al_2O_3/TiO_2/Al_2O_3$ gate dielectric stack with an EOT of 1.0 nm was grown on Si at room temperature. The conduction mechanism across the dielectric stack was also investigated based on the leakage temperature dependence. The analysis revealed that both Schottky emission and tunneling contribute to the electron conduction. The leakage current under the gate injection was dominated by Schottky emission, which exhibited much stronger temperature dependence than the one under substrate injection due to the relatively larger barrier heights on gate side. (Work supported by the U.S. Department of Energy, BES-Materials Sciences, under Contract W-31-109-ENG-38.)

9:00 AM

Q3, Relative Stability and Electronic Properties of Zirconium and Hafnium Nitrides and Oxynitrides. First Principles DFT Study: *Anatoli Korkin*[1]; Dmitry Bazhanov[2]; Andrey Knizhnik[2]; Andrey Safonov[2]; Matt Stoker[3]; Alexander Bagaturyants[2]; [1]Nano & Giga Solutions, 1683 E. Spur St., Gilbert, AZ 85296 USA; [2]Kintech, Moscow Russia; [3]Motorola, Tempe, AZ USA

Zirconium and hafnium nitrides and stable in metallic, MN, and in the (narrow band) dielectric, M3N4, forms proving an opportunity to design a metal/insulator interface from two different phases of the same material. In this paper we present the periodic DFT plane waves and localized orbital study of the atomic structure, stability and electronic properties of the various phases of zirconium and hafnium nitrides, MN and M3N4, and oxynitrides, M2N2O. Among three structures studied for M3N4 stochiometry, the orthorhombic Pnam and spinel structures are dielectric, while the rock salt structure (MN structure with M vacancies) is metallic, the former (experimentally known structure) being the most and the latter the least stable forms for both Zr and Hf materials. The energy of the nitrogen vacancy formation is 1 eV higher in Hf3N4 than in its Zr analogue revealing the known trend of increasing stability of the highest (+4) oxidation state for the heavier transition elements. Among two structures studied for MN2 O, the experimentally known cubic Bixbyite-type crystal structure in the Ibca space group is more stable than the hexagonal La2O3-type structure in the P3-m space group by 0.6 eV for Zr and 0.9 eV for Hf oxynitride. Both phases are dielectric. The stochiometric MN2O compound can be prepared from the 1:1 mixture of MO2 and M3N4. Our calculations show that this reaction is only slightly (0.01 eV) exothermic for both Zr and Hf, while oxidation of the nitrides is highly exothermic. The analysis of the density of states reveals that the band gap is higher in the dielectric phases of Hf than in Zr nitrides.

9:20 AM Student

Q4, High Deposition Rate Atomic Layer Deposition Process: *Gi Kim*[1]; Anu Srivinastava[1]; Ana Londergan[1]; Sasangan Ramanathan[1]; Tom Seidel[1]; [1]Genus Inc., Sunnyvale, CA 94087 USA

Atomic Layer Deposition (ALD) has received increasing interest in the last several years, especially with respect to integration of ultra thin (~ few tens of A) dielectrics in advanced DRAM capacitors and gate applications.[1, 2] Outstanding conformality and compositional control are obtained with ALD. Yet, the deposition rates are commercially unsatisfactory for applications using films >100A. The novel operation of the ALD process in the kinetic regime, with short exposure times - less than that required for saturation can markedly improve the deposition rate of the film relative to standard ALD processes operated into saturation. The short exposure time process results in film deposition rates up to ~200A/min (up to 10x standard ALD processes). This result is obtained in spite of the fact that the intrinsic ALD deposition rate (A/cycle) is reduced relative to saturated ALD operation. A case study is reported for TMA/H2O chemistry. The deposition rate is found to increase monotonically from 175 to 350°C, indicative of a fundamentally different thermally activated reaction chemistry process as compared with longer saturated reaction processes. The latter exhibits a maximum at ~200°C. The purge characteristics, indicating the onset of the admixture of CVD with ALD, are studied for the limit of very small purge times. The "starved reaction" mode, STAR-ALD provides useful conformality, stoichiomentry, electrical properties, etc. Nominally 100% conformality has been demonstrated for aspect ratios > 10:1. The composition is nominally Al2O3 (RBS, X-ray Ellipsometry). The electrical properties show dielectric breakdown fields >8MV/cm for as-deposited films and low leakages are obtained, useful for device applications. Trace carbon (TMA source) is found to be negligible and comparable to the trace levels found using saturated ALD chemistries. The film uniformity has been achieved at the ~ 1% level for 100A deposition and this is pressure and mass transport sensitive. The film deposition rate (A/unit time) as a function of exposure times of the reactants exhibits a maximum. This corresponds to the crossover of the increasing function of the ALD deposition rate (A/cycle) and the decreasing cycle time function of the exposure time(s) for the reactants. A phenomenological model is also described that is characterized by a maximum in the film deposition rate at a time related to the saturating half-reaction time constants of the ALD process. [1]H. Seidl, et.al, "A Fully IntegratedAl2O3 Trench Capacitor DRAM for Sub-100nm Technology," IEDM Tech Dig., paper 33.2, 2002. [2]J.H.Lee, et.al, PolySi Gate CMOSFETSD with HfO2-Al2O3 Laminate Gate Dielectric for Low Power Applications, VLSI Symposium, Hawaii June 2002.

9:40 AM Q5, Late News

10:00 AM Break

10:20 AM

Q6, Characteristics of WN_x and ZrN_x as Gate Electrodes: The Effect of Nitrogen Concentration: *Pei-Chuen Jiang*[1]; S. H. Wang[1]; Yi-Sheng Lai[1]; J. S. Chen[1]; [1]National Cheng Kung University, Dept. of Matls. Sci. & Engrg., No.1, Ta-Hsueh Rd., Tainan 701 Taiwan

The selection of materials for gate electrodes has been a critical issue as the dimension of CMOS devices continuous to scale down. To see the potential of metal nitrides as gate electrodes, we investigate the properties of the WN_x and ZrN_x films of various nitrogen contents, using $WN_x/SiO_2/Si$ and $ZrN_x/SiO_2/Si$ structures. The SiO_2film was grown by thermal oxidation at 900°C and WN_x or ZrN_x films were deposited by sputtering. The work function (ϕ_m) of metal nitrides were extracted from the C-V measurement of MOS structures with different oxide thickness. By increasing the N_2/Ar gas flow ratio during sputtering deposition, we obtained a series of WN_x films of different phases, which are $W+W_2N$, W_2N and W_2N+WN. On the contrary, ZrN_x films exhibit only the ZrN phase, regardless of the N_2/Ar flow ratio. The nitrogen concentration in both nitrides increases continuously with increasing N_2/Ar flow ratio. The different nitrogen contents in WN_x and ZrN_x films result in dissimilar chemical bonding states between the metal atom (W or Zr) and N, which causes a diverse values of ϕ_m. As gate electrodes, the metal nitrides are expected to possess low resistivity and good thermal stability. The resistivity of WN_x and ZrN_x films can vary from tens to thousands of $\mu\Omega$cm, depending on the nitrogen concentration in the films. Overstoichiometric nitrogen in the nitride films will generally increase the electron scattering probability and thus increase the film resistivity. Regarding the thermal stability, the WN_x film remains intact after annealing at 400-500°C in N_2+H_2. However, it partly transforms to WO_3 after annealing at 600°C owing to the loss of nitrogen. The partial oxidation of WN_x induces a significant increase of resistivity, and leads to the change of bonding states in WN_x. The connection between the chemical/material characteristics of metal nitrides upon heat treatments and their electrical properties will also be discussed.

10:40 AM Student

Q7, The Study of Electrical Characteristics of Different HfO_2-Al_2O_3 Stack Layer Grown by Atomic Layer Deposition: *Yong-Seok Kim*[1]; Dongwon Lee[1]; Dongchan Suh[1]; Dae-Hong Ko[1]; Ja-Hum Ku[2]; [1]Yonsei University, Dept. of Ceram. Engrg., 134, Shinchon-Dong, Seodaemun-Gu, Seoul, 120-749 Korea; [2]Samsung Electronics Company, Ltd., R&D, San #24, Nongseo-Ri, Kiheung-Eup, Yongin, Kyungki-Do 449-900 Korea

For scaling complementary metal-oxide-semiconductor (CMOS) technology beyond the 50 nm, high-k gate dielectric will be necessary in order to maintain low leakage current density. Various high-k gate dielectrics (HfO_2, ZrO_2, Al_2O_3, La_2O_3 etc.) have been investigated as a possible replacement for SiO_2 to suppress the leakage current. However, gate dielectric must have very low leakage current, minimal low-k interfacial layer, large bandgap, low interface trapped charge density and low dopant penetration. Among these oxides, HfO_2 is one of the most promising materials because of its large dielectric constant (k>25) and large band gap (E_g>5.5eV). However, annealing in oxygen ambient will lead to fast diffusion of oxygen through the HfO_2 film, causing the growth of uncontrolled low-k interfacial layer. Al_2O_3 have excellent leakage current characteristics, low oxygen diffusion coefficient, low interface state density (D_{it}), and good thermal stability when directly in contact with Si. In this study, to compare electrical characteristics of different types of HfO_2-Al_2O_3 stack layer, HfO_2(3nm)/Al_2O_3(2nm), Al_2O_3(2nm)/HfO_2(3nm) and Al_2O_3(1nm)/HfO_2(3nm)/Al_2O_3 (1nm) films were deposited on p-type Si wafer by atomic layer deposition at 350• with $HfCl_4$, TMA and H_2O as precursor. And Pt was deposited by sputtering as a gate electrode. Capacitance-voltage (C-V) measurements were used to obtain capacitance equivalent thickness (CET), interface trapped density, threshold voltage and flatband voltage of high-k gate stack. And current-voltage (I-V) characteristics were taken to measure leakage current properties. The thickness of interfacial oxide layer between gate stack and Si substrate was increased upon annealing in N_2 ambient, which is due to diffusion of oxidizing species from N_2 ambient. After annealing at 700• in each sample, CET increases ~3Å by slight interfacial layer growth while leakage current reduces to ~10^{-3}X. However, $Al_2O_3/HfO_2/Al_2O_3$ films after annealing at 900•, interlayer thickness increase drastically to CET of ~50Å. In comparison to $Al_2O_3/HfO_2/Al_2O_3$ films, the CET of HfO_2/Al_2O_3 and Al_2O_3/HfO_2 films increase to ~41Å. Electrical characteristics were supplemented by high resolution transmission electron microscopy (HR-TEM) and synchrotron radiation x-ray photoelectron spectroscopy (XPS). By HR-TEM and XPS analyses, we observed the properties of HfO_2-Al_2O_3 gate stacks and interfacial layer between gate stack and Si substrate upon different annealing temperature. At high temperature annealing, hafnium aluminate was formed in boundary of HfO_2 and Al_2O_3 due to interdiffusion of HfO_2 and Al_2O_3, and HfO_2 layer was crystallized to monoclinic and tetragonal phases.

11:00 AM

Q8, Nanoscale Characterizations of Ferroelectric BT-Based Films for High-Density FeRAMs: M. J. Jin[1]; W. I. Kweon[1]; N. J. Park[1]; S. J. Kim[1]; *B. L. Yang*[1]; S. K. Hong[2]; S. S. Lee[2]; Y. J. Park[2]; [1]Kumoh National Institute of Technology, Dept. of Matls. Sci. & Engrg., 188 Shinpyung-Dong, Gumi-si, Gyeongbuk 730-701 Korea; [2]Hynix Semiconductor Inc., Memory R&D Div., New Device Team, Icheon-si, Kyoungki-Do 467-701 Korea

Importance of ferroelectric high-density memories (>64Mb) using the integrated cells of size less than 0.1um2 will be more increased in upcoming ubiquitous era. Thus nanoscale control of microstructures of ferroelectric films with large switching polarization has been one of the issues to obtain the uniform electrical properties for realization of high-density memories. In this study the grain orientation and size distribution of BT-based films by spin-on coatings were examined by FEG-SEM/EBSD and XRD. Ferroelectric domain characteristics by PFM were also performed to study the dependency of reliabilities on grain orientation and distribution. Film process effects such as RTA and furnace annealing on grain orientation and uniformity will be discussed aiming at understandings of the nucleation and growth of the a or b-axis oriented films during the processes.

11:20 AM Student
Q9, Characterization of Cerium Oxide (CeO_2) and Hafnium Oxide (HfO_2) Thin Films on Si (100) as Alternative High-k Gate Oxide Deposited by Pulsed Laser Ablation: *K. Karakaya*[1]; J. H.M. Snijders[2]; P. Graat[2]; T. Dao[2]; A. J.H. M. Rijnders[1]; Z. M. Rittersma[3]; D. H.A. Blank[1]; [1]University of Twente, Faculty of Sci. & Tech., PO Box 217, Enschede 7500AE The Netherlands; [2]Philips, Ctr. for Indust. Tech., Prof. Holstlaan 4, Eindhoven 5656AA The Netherlands; [3]Philips Research Leuven, Kapeldreef 75, Leuven 3001 Belgium

Cerium oxide and hafnium oxide are candidates for novel high-k gate dielectric applications due to their electrical and chemical properties. Electrical and morphological properties of cerium oxide, hafnium oxide films and laminated stacks of those oxides are investigated in this work. Films are deposited on HF cleaned silicon (100) substrates by pulsed laser deposition technique, from high-density cerium oxide and hafnium oxide targets at various pressures and temperatures in an UHV-PLD system equipped with in situ RHEED. Properties of both pure oxides and laminated cerium-hafnium oxides, which are deposited in identical conditions, are compared. High purity argon, oxygen and high vacuum ($<10^{-7}$ mbar) environments are used as deposition atmosphere and depositions are done at temperatures varies from room temperature up to 850°C. Rutherford Backscattering for interface oxide thickness and chemical composition, XPS for chemical state of compounds, XRD and XRR for morphological characterization and AFM for surface quality, are used for to investigate film properties. After depositing top electrode by shadow mask deposition in a sputter system, electrical characterizations of the films are also performed by capacitance-voltage measurements at various frequencies and current-voltage measurements for leakage current determination.

Session R: Nanotubes and Nanowires I

Thursday AM   Room: 141
June 24, 2004   Location: DeBartolo Hall

Session Chairs: Hou T. Ng, NASA Ames Research Center, Moffett Field, CA 94043 USA; Ray Tsui, Motorola Laboratories, Phys. Scis. Rsch. Labs., Tempe, AZ 85284 USA

8:20 AM
R1, Growth of InMnAs Nanowires for Low-Dimensional Spintronic Applications: Steven J. May[1]; Jian-Guo Zheng[1]; Bruce W. Wessels[1]; *Lincoln J. Lauhon*[1]; [1]Northwestern University, Matls. Sci. & Engrg. & Matls. Rsch. Ctr., 2220 Campus Dr., Evanston, IL 60208 USA

Ferromagnetic semiconductors are promising materials for the realization of spintronic devices, and semiconductor nanostructures (dots, rods, wires) provide a means to explore and exploit the effects of reduced dimensionality on electronic, optical, and magnetic properties of semiconductors. If the synthesis methods used to produce ferromagnetic semiconductor thin films prove compatible with the synthesis of semiconductor nanowires, one might be able to make magnetic semiconducting nanowires, and thereby open up a range of interesting fundamental studies and new nanoscale spintronic devices. Towards this goal, we have synthesized InAs and InMnAs nanowires with diameters of 20 nm and lengths of several microns by atmospheric pressure metal-organic vapor phase epitaxy (MOVPE). Gold catalyst nanoparticles on Si(100) and GaAs(111) wafers were used to initiate wire growth via a vapor-liquid-solid (VLS) mechanism in the presence of the reactants trimethylindium (TMIn), arsine (AsH3), and tricarbonyl(methycyclopentadienyl)manganese (TCM). Thin film growth was also monitored to enable comparisons of growth rate and stoichiometry between the thin films (thermally activated growth) and nanowires (metal catalyzed growth). Oriented, epitaxial growth of Au-catalyzed InAs nanowires on GaAs(111) substrates was observed for substrate temperatures of 400-480°C. High resolution transmission electron microscopy (TEM) imaging of individual nanowires verified that the nanowires were single crystals (zincblende) with [111] being the preferred growth direction. Scanning electron microscopy (SEM) and TEM studies of nanowire morphology showed a slight taper in the nanowire diameters consistent with a small amount of radial overgrowth via vapor-solid deposition on the wire surface. The radial growth rates were consistent with thin films growth rates synthesized under the same conditions. InMnAs nanowires were synthesized by introducing the manganese precursor (TCM) into the TMIn/AsH3 reactant stream under conditions favorable to InAs nanowire growth. The Mn precursor notably affected nanowire composition and morphology. At substrate temperatures of 440°C and above, using precursor flow rates suited to single phase InMnAs thin film growth, TCM inhibited nanowire growth. At 400°C, and with reduced TCM flows relative to thin film growth conditions, InMnAs nanowires were successfully synthesized. Mn incorporation was verified for individual nanowires by energy dispersive x-ray spectroscopy (EDS) measurements in a TEM. Magnetic force microscopy was used to study ferromagnetic domain formation. Excess flowrates of the manganese precursor were associated with a significant change in wire morphology, specifically, copious side branching. EDS measurements revealed compositional segregation associated with this growth mode, with the side branches being primarily InAs and the tips of the branches being primarily MnAs. In addition, Au clusters were not observed at the tips of InMnAs nanowires. Ongoing scanning-TEM and EDS studies seek to clarify the influence of TCM flow on the morphology and Mn content of VLS-grown nanowires.

8:40 AM
R2, Effects of Surface Oxide Properties on the Electrical Characteristics of Ge Nanowires: Dunwei Wang[1]; *Ying-Lan Chang*[2]; Hongjie Dai[1]; [1]Stanford University, Dept. of Chmst., Stanford, CA 94305 USA; [2]Agilent Technologies Inc., Agilent Labs., 3500 Deer Creek Rd., Palo Alto, CA 94304 USA

Recently, chemically derived nanotube and nanowire materials have attracted much attention as candidates for future electronics components including field effect transistors. Chemical routes to electronic devices may offer an advantage of material dimension control without relying on lithography, the potential of device fabrication on a wide range of substrates, the possibility of high device performance brought about by the advanced intrinsic properties of novel materials or high degree of perfection in the material structures, and new processing and integration strategies. Currently, for further device scaling and miniaturization, germanium is of renewed interest as an electronic material to potentially compliment silicon due to its higher carrier mobility and the trend in gate dielectrics evolution. Single crystalline Ge nanowires with p and n-type doping are readily obtained at synthesis temperatures below 300°C via a chemical vapor deposition method. X-ray photomission spectroscopy (XPS) study shows that Ge oxides are present on nanowires surface. As a result of the surface states due to the presence of Ge oxides, band bending is observed on both p and n-type Ge nanowires. Bending direction is opposite for p and n-type nanowires. Moreover, it is found that the degree of band bending also depends on the oxidation level-the more oxides on the surface, the more band bending is observed. After annealing treatment in ultra high vacuum, the ratio of Ge 3d electron binding energy peak intensity due to Ge oxide vs. Ge bulk is greatly reduced, suggesting surface oxides are effectively removed. This annealing treatment is also found to reduce the band bending significantly. We also studied oxidation kinetics of clean Ge nanowire surfaces. After air exposure, GeO is found to form first on p-type GeNWs, and it is converted to GeO2 as Ge nanowires are exposed to ambient air longer. A distinct phenomenon is found on n-type nanowires, where GeO2 is found to form directly and instantly and keeps growing as exposure time to ambient air is increased. This finding correlates well with electrical measurements.

9:00 AM Student
R3, MOCVD Growth and Characterization of GaN Nanowires: *Jie Su*[1]; George Cui[1]; Maria Gherasimova[1]; Seong-Ran Jeon[1]; Jung Han[1]; Dragos Ciuparu[2]; Lisa Pfefferle[2]; Yiping He[3]; Arto V. Nurmikko[3]; [1]Yale University, Elect. Engrg., New Haven, CT 06520 USA; [2]Yale University, Chem. Engrg., New Haven, CT 06520 USA; [3]Brown University, Engrg., Providence, RI 02912 USA

In the past five years there has been an increasing effort, pioneered largely by the community of inorganic synthesis, in preparing semiconductor-based nanowires using catalyst-mediated growth process. While the proof-of-concept work of synthesizing nanostructures by vapor-

liquid-solid (VLS) growth mechanism had been unambiguously established in semiconductors such as Si, Ge, GaAs, GaP, and GaN, the majority of the published work employed inorganic synthesis techniques such as flow-tube-based vapor transport and laser ablation that offer only limited flexibility and control. The synthesis of nanostructures by modern epitaxial process such as MOCVD or MBE would have clear advantages including a better controlled process environment (in terms of temperature, reactant flows, source purity) that will enable microscopic understanding of synthesis mechanisms and the possibility of modulating the chemical composition along the wire direction on the atomic scale, thus enabling the realization of novel quantum structures and metastable configurations. Additionally, due to the daunting challenges in directed manipulation and assembly of individual nanowires into complicated circuits there is a pressing need to enhance the single-wire functionality in-situ through heteroepitaxy. The employment of atomistic epitaxial tools such as MOCVD will inject exciting degrees of freedom into nanowire device synthesis. We report here the catalyst-mediated MOCVD growth of GaN nanowires using a commercial horizontal cold wall reactor. Trimethylgallium and ammonia were used as Ga and N precursors. Anchoring of the catalyst was achieved using either a metal (Ni, Fe, Co) impregnated mesoporous silica templates (MCM-41) or generic substrates with catalyst solution dispersed on the surface. The nanowires are single crystals with a diameter ranging between 20 and 40 nm and length up to 10 um, with a surface distribution density of 1-5e9cm-2. SEM images give clear evidence of the presence of metallic droplets at the tip of nanowires that is consistent with the VLS growth mode. Selective area electron diffraction (SAED) identifies <1120> as the predominant axis directions. The diffraction fringes along the nanowire axis are consistent with the spacing of a-plane GaN. Parameters such as catalyst preparation, reactant supersaturation, N/Ga ratio, and growth temperature will be presented. While still at an early stage of this research, we have already ventured beyond GaN synthesis into InGaN/GaN heterostructures and nanostructures. The authors acknowledge the support of DOE NETL and NSF.

9:20 AM Student

R4, Effect of Growth Conditions on the Composition and Structure of SiGe Alloy and SiGe/Si Heterostructure Nanowires: *Kok-Keong Lew*[1]; Ling Pan[2]; Timothy E. Bogart[1]; Elizabeth C. Dickey[2]; Joan M. Redwing[1]; [1]Pennsylvania State University, Dept. of Matls. Sci. & Engrg., Univ. Park, PA 16802 USA; [2]Pennsylvania State University, Matls. Rsch. Inst., Univ. Park, PA 16802 USA

The synthesis of multi-layered $Si_xGe_{(1-x)}$/Si nanowires in which the composition is controlled along the axial or radial direction of the wire is of interest for fundamental studies of carrier confinement in nanoscale geometries as well as nanoscale device fabrication. Vapor-liquid-solid (VLS) growth is commonly used for the synthesis of Si and Ge nanowires. In the VLS process, a metal (gold) is used to catalyze the decomposition of a source gas (SiH_4 and GeH_4) resulting in the formation of a nanowire via precipitation from the Au-Si or Au-Ge liquid eutectic phase. The synthesis of $Si_xGe_{(1-x)}$ alloy nanowires using this approach is challenging due to the lower decomposition temperature of GeH_4 compared to SiH_4 which results in Ge deposition on the outer surface of the nanowire during growth. In this study, the effect of VLS growth conditions on the composition and structure of $Si_xGe_{(1-x)}$ nanowires was initially investigated in order to identify conditions that yield nanowires with well-controlled and homogeneous alloy composition. Anodized alumina membranes with a nominal pore diameter of 200 nm were used as templates for electrodeposition of Au metal catalyst plugs and subsequent VLS growth. VLS growth was carried out in an isothermal quartz tube reactor using SiH_4 (10% in H_2) and GeH_4 (2% in H_2) as source gases. The inlet $GeH_4/(SiH_4+GeH_4)$ gas ratio was varied from 0.01 to 0.14. The reactor pressure was held constant at 12 Torr and the growth temperature was varied from 350 to 500°C. $Si_xGe_{(1-x)}$/Si heterostructure nanowires were fabricated by switching on and off the GeH_4 while maintaining a constant SiH_4 flow at 500°C. Scanning transmission electron microscopy (STEM) imaging and quantitative energy dispersive x-ray spectroscopy (EDS) were used to confirm the presence of Si and Ge in the nanowires and to profile the elemental composition throughout the wire. The Ge fraction in the nanowires increased linearly from 12.4 to 40.0 atomic % as the inlet gas ratio was raised from 0.01 to 0.074 at a growth temperature of 425°C. Tapered nanowires consisting of a $Si_xGe_{(1-x)}$ core and a Ge outer shell were obtained when the growth temperature was increased above 425°C or the inlet gas ratio was increased to 0.14. The Ge coating was reduced when the temperature was lowered to 375°C at a constant inlet gas ratio of 0.14. The results indicate that reduced growth temperatures are essential for the fabrication of homogeneous $Si_xGe_{(1-x)}$ alloy nanowires with high Ge content. $Si_xGe_{(1-x)}$/Si multi-layered nanowires were also fabricated and compositional modulation along the axis of the nanowire was confirmed by EDS analysis.

9:40 AM Student

R5, Four-Point Resistivity and Gate-Dependent Conductance of p- and n-Type Silicon Nanowires: *Yanfeng Wang*[1]; Kok-Keong Lew[2]; Marco A. Cabassi[1]; Tsung-Ta Ho[1]; Joan M. Redwing[2]; Theresa S. Mayer[1]; [1]Pennsylvania State University, Dept. of Elect. Engrg., Univ. Park, PA 16802 USA; [2]Pennsylvania State University, Dept. of Matls. Sci. & Engrg., Univ. Park, PA 16802 USA

There has been considerable interest in bottom-up integration of semiconductor nanowires for their application in future logic, optoelectronic, and sensing circuits. To achieve these goals, robust synthetic approaches must be developed for incorporating p- and n-type dopants into the nanowires. In this talk, we present the results of four-point resistivity and gated-dependent conductance measurements on silicon nanowires (SiNWs) that were intentionally doped with boron or phosphorous during growth. The SiNWs used in these studies were synthesized by template-directed vapor-liquid-solid (VLS) growth where Au plugs are deposited within 80-nm diameter pores of alumina membranes to catalyze SiNW growth at temperatures near 500°C. The doping concentration was varied by changing the ratio of trimethylboron (TMB) or phosphine (PH_3) to silane (SiH_4) from 0 to 210^{-2} while maintaining a constant total flow rate of gas in the reactor. Following synthesis, SiNWs were removed from the membrane and integrated onto a back-gated testbed for electrical measurements. This was accomplished by electrofludically aligning individual SiNWs between pairs of large area electrodes and then using e-beam lithography followed by metal liftoff of Ti (20 nm)/Au (80 nm) to define the source/drain (S/D) electrodes and two additional voltage leads. Nanowire resistivity was calculated from measured values of four-point resistance, which was determined by forcing a constant current between the S/D electrodes and measuring the voltage developed across the two voltage leads. The gate dependent properties of unintentionally-doped SiNWs show a large decrease in the drain-to-source current, IDS, as the gate bias, VGS, is made more positive, which is consistent with depletion mode operation of a SiNW device with a p-type background. Increasing the $TMB:SiH_4$ ratio from 0 to 210^{-2} resulted in a reduction in the gate modulation and a corresponding decrease in SiNW resistivity from 7 to 0.5 Ω-cm suggesting that the B-concentration is increasing with higher TMB flow rate. Low ratios of $PH_3:SiH_4$ (210^{-5}) still resulted in SiNWs with p-type behavior. However, at higher ratios of $PH_3:SiH_4$ (210^{-3}) IDS decreased as VGS became more negative and the resistivity dropped to 0.3 Ω-cm, which is consistent with n-type behavior. These results demonstrate that p- and n-type dopants can be effectively incorporated from TMB and PH_3 gas sources during SiNW synthesis.

10:00 AM Break

10:20 AM

R6, Properties of Gallium Nitride Particles Prepared by Ammonolysis from Different Starting Materials: *Birgit Schwenzer*[1]; Jerry Hu[2]; Stacia Keller[1]; Frederick F. Lange[2]; Steven P. DenBaars[2]; Umesh K. Mishra[1]; [1]University of California, ECE Dept., Santa Barbara, CA 93106-9560 USA; [2]University of California, Matls. Dept., Santa Barbara, CA 93106 USA

Despite the increasing interest in semiconducting nanostructures still relatively little work has been reported for group-III nitride compounds compared to research on II-VI semiconducting nanoparticles. For our study on gallium nitride (GaN) nanostructures the particles were prepared by different methods of ammonolysis. With recent reports for the synthesis of indium nitride nanostructures, using only indium oxide as the starting material we investigated a similar approach for the preparation of GaN particles and compared the results with GaN particles prepared by the well-known approach of using a mixture of gallium oxide (Ga2O3) and metallic Ga. Thirdly we looked at the reaction of metallic Ga with ammonia, which also yields nano- and micrometer size GaN particles. The choice of the starting material for the preparation of GaN in our experiments had a significant influence on the optical properties of the final material. While GaN nanostructures prepared from only

Ga2O3 showed no luminescence when excited by a He-Cd laser (325 nm, 300K), the GaN samples prepared from a Ga2O3/Ga mixture and pure Ga showed bright emission around 370 nm. For GaN prepared from a Ga2O3/Ga mixture the luminescence intensity decreased with increasing ammonia flow during the synthesis. Also, non-luminescing GaN prepared Ga2O3 from could be converted into luminescing GaN by annealing under N2 at elevated temperatures. According to powder XRD all three approaches yielded highly crystalline wurtzite GaN particles. However, for the particles prepared from metallic Ga a second XRD pattern was detected, indicating the presence of an additional hexagonal GaN phase. 71Ga-NMR of the differently prepared GaN samples illuminated the differences of the materials further. For GaN particles prepared from Ga2O3 one sharp signal was detected at 327 ppm for the Ga atoms in the material. The sharpness of the peak indicated highly symmetric surroundings of the Ga atoms within the crystal, the shift of the detected signal was in agreement with the signal reported for GaN. The GaN prepared from a Ga2O3/Ga mixture showed a broad peak, centered around 372 ppm in addition to the sharp one at 327 ppm. The broadening of the signal indicates a non-symmetric environment for the Ga atoms (inhomogeneity broadening). Apparently also in this material two phases exist, which coincide in the XRD data. For the sample prepared from metallic Ga in addition to the two previously observed signals another broad peak centered around 422 ppm corresponding to a third phase was observed in the 71Ga-NMR spectra. Thereby the decrease in symmetry can be attributed to a non-stochiometric Ga:N ratio. Mechanisms explaining the experimental observations will be discussed.

10:40 AM Student

R7, Growth Control of Carbon Nanotube by Applied Electric Field: *Masatoshi Maeda*[1]; Takafumi Kamimura[2]; Chan-Kyeong Hyon[3]; Atsuhiko Kojima[3]; Kousuke Kurachi[4]; Takushi Kawai[4]; Masashi Torigoe[4]; Kazuhiko Matsumoto[2]; [1]University of Tsukuba, Pure & Applied Scis., 1-1-1, Tennoudai, Tsukuba, Ibaraki 305-8577 Japan; [2]Osaka University, Grad. Sch. of Engrg. Sci., 8-1, Mihogaoka, Ibaraki, Osaka 565-0871 Japan; [3]CREST/JST, 4-1-8, Motomachi, Kawaguchi, Saitama 332-0012 Japan; [4]Meiji University, Dept. of Elect. & Communications, 1-1-1, Higasimita, Tama, Kawasaki 214-8571 Japan

We have investigated the effects of the electric field for the control of the growth of the carbon nanotube (CNT) between electrodes. CNT is the useful element for the nanodevices. However the control of the position and the direction is difficult. Therefore, it is indispensable to control the growth of CNT. An n-type silicon wafer with a thermally grown oxide (200 nm) was used as the substrate. The layered electrodes of Mo/Si (30/150 nm) and catalyst of Fe (5 nm) were patterned on the substrate using the conventional photo-lithography process. The CNTs were grown between two electrodes by the thermal chemical vapor deposition using bubbeled ethanol and hydrogen. During the growth of CNT, the DC bias was applied between two electrodes. First the effect of the shape of the electrode was examined. Two types of shape were adopted. One is the sharp triangular structure in order to concentrate the electric field between the sharp tips of the electrodes. The other is the conventional rectangular structure. The electric field between them is expected to be perpendicular to the electrode and to be parallel each other. Second, the effect of the applied bias with two types was examined. One is the constant applied voltage during the growth period. The other is the ramp DC voltage, which decreases, e. q., from 10 V to 0 V at constant rate for 20 minutes, during the growth period. The sample was observed using Scanning Electron Microscope. The difference of the shape of CNTs by the difference of the electrode structure, and of the type of the applied bias, was examined. In the cases of the sharp triangular structure, only few CNT grew straightforward to the opposite electrode only near the sharp tip of the electrode, and almost CNT shows the curved structure and starts to grow from the side of the triangular electrode. In the case of the rectangular electrode structure, all CNT grew straightforward to the opposite electrode. From these results, CNT was found to grow along the electric field between two electrodes. The effect of the applied bias with two types was examined using the rectangular electrode. In the cases of the constant DC voltage between two electrodes, CNT starts to grow from positive biased electrode, and it is hard to reach the negative biased electrode. Just before the negative biased electrode CNT stop to grow. The reason was explained by the etching effect of the positive ionized hydrogen which attacks the carbon atom near negative biased electrode and stop to grow the CNT. In the cases of the ramp DC voltage which decrease from 10 V to 0 V for 20 minutes, length of CNT increased and CNT can bridge between two electrodes. This is because the etching effect of carbon by the positive ionized hydrogen may be decreased by the decreased applied bias. The effects of the applied bias for the control of the growth of the carbon nanotube was examined. Using the combination of the rectangular electrode and the ramp DC bias, we have succeeded in bridging the strait CNT between electrodes.

11:00 AM Student

R8, Growth of Arrays of mm Long, Straight Single-Walled Carbon Nanotubes: *Zhen Yu*[1]; Shengdong Li[1]; Lifeng Zheng[1]; Peter Burke[1]; [1]University of California, EECS MS 2625, Irvine, CA USA

In this work, we demonstrate the growth of arrays of 1.5 mm long, straight single walled nanotubes fabricated using a single furnace with methane and H2 as the feedstock. Recently Huang et al[1] have fabricated 3.7 mm long single walled carbon nanotubes using a two-furnace, dual temperature growth system with CO and H2 as the feedstock. Our work shows arrays of long, straight nanotubes can be grown in a single furnace system. Using a home-built CVD system based on a 3 inch Lindberg furnace, we have synthesized long, straight nanotubes using CVD. The catalysts were prepared as follows: First, a lithographically patterned Ti(50 nm)/Au(200 nm) metallization layer is deposited and patterned using e-beam evaporation onto a Si wafer. Next, an aqueous solution containing nanoparticle catalyst is deposited and lifted off onto only the patterned Au. The nanoparticle catalyst solution was prepared by adding 0.3g of alumina nanoparticles (Degussa), 0.05 mmol of Fe(NO3)3•9H2O (Aldrich), and 0.015 mmol of MoO2(acac)2 (Aldrich) to 3 l DI water (18 M?Ç.cm). The growth procedure was as follows: First, the sample was heated to 900 C in Ar. Next, H2 was flowed for 10 minutes. Next, methane/H2 mixture was flowed for 15 minutes to activate the growth. The sample was then allowed to slowly cool in Ar. Post-growth characterization was carried out with SEM. AFM growth from nanotubes grown under similar conditions in our lab yielded diameters of 1.5 nm, indicating that our nanotubes are single walled. The growth results indicate an aligned array of nanotubes (6) with pitch of 50 microns and length of at least 200 microns. 3 of the 6 nanotubes were 1.5 mm in length. The growth of the longer nanotubes was terminated only by the presence of a neighboring catalyst site. With properly designed catalyst geometries with room to grow, cm long single walled nanotube growth should be possible. We believe the ability to grow these ultra-long, straight nanotubes is due to two key factors: First, we have designed a special gas injector to efficiently mix the gases before flow and minimize the turbulence. This allows the nanotubes to grow long distances in a single direction parallel to the gas flow. Second, the Au underlayer supports the nanoparticle catalysts above the substrate, allowing the nanotubes to grow without interference from the substrate over long distances. The second step is unique to our growth procedure. In the future it should be possible to grow 2d arrays by rotating the wafer and carrying out a second growth run. By engineering the nanotube pitch, ultra-dense electrical circuitry could be fabricated. [1]S. Huang, B. Maynor, X. Cai, J. Liu, "Ultralong Well-Aligned Single-Walled Carbon Nanotube Architectures on Surfaces", Advanced Materials, vol. 15, pp. 1651-1655, 2003.

11:20 AM

R9, Growth and Characterization of Single-Walled Carbon Nanotubes by Microwave Plasma-Enhanced Chemical Vapor Deposition: *Matthew Maschmann*[1]; A. Goyal[2]; Zafar Iqbal[2]; Timothy S. Fisher[1]; Roy Gat[3]; [1]Purdue University, Mech. Engrg., 585 Purdue Mall, W. Lafayette, IN 47907-2088 USA; [2]New Jersey Institute of Technology, Dept. of Chmst., NJ USA; [3]Seocal, Inc.

Two very recent papers by Kato et al.[1] and Li et al.[2] have reported growth of single-walled carbon nanotubes by RF plasma-enhanced chemical vapor deposition (PECVD). As demonstrated in a variety of film growth processes, PECVD can enable growth at lower operating temperatures than other vapor deposition techniques and is thus attractive in processing of integrated devices that include materials that are unstable at high temperatures. Importantly, the Li et al. paper reported strongly preferential growth of semiconducting nanotubes of the type that would be useful in next-generation integrated circuits. The present work reports the synthesis of single-walled nanotubes by microwave (2.5 GHz) plasma-enhanced chemical vapor deposition. The nanotubes were catalyzed with Mo:Co particles on MgO supports. The catalyst was prepared in powder form, suspended in acetone, and dispersed over a Si wafer with a native oxide. The nanotubes were grown at a substrate temperature of 800C

under a spherical hydrogen-methane plasma with 200W of input microwave power, and the volumetric flow rate ratio of hydrogen to methane was 50:3. The resulting nanotube array was analyzed by Raman spectroscopy, which revealed radial breathing mode shifts in the range of 185 to 236 cm-1, indicative of single-walled nanotubes with diameters ranging from 1.0 to 1.3 nanometers. The presentation will include STM and AFM analyses of the resulting nanotubes. Further, results of variations in microwave power, substrate temperature, and feedstock gas ratios (from lean to rich) will be presented. [1]Toshiaki Kato, Goo-Hwan Jeong, Takamichi Hirata, Rikizo Hatakeyama, Kazuyuki Tohji, Kenichi Motomiya, "Single-walled carbon nanotubes produced by plasma-enhanced chemical vapor deposition," Chemical Physics Letters, 381, 422-426 (2003). [2]Yiming Li, David Mann, Marco Rolandi, Woong Kim, Ant Ural, Steven Hung, Ali Javey, Jien Cao, Dunwei Wang, Erhan Yenilmez, Qian Wang, James F. Gibbons, Yoshio Nishi, and Hongjie Dai, "Preferential Growth of Semiconducting Single-Walled Carbon Nanotubes by a Plasma Enhanced CVD Method," Nano Letters, to appear (2004).

11:40 AM Cancelled

R10, Synthesis, Electron Microscopy and Applications of Inorganic Nanotubes: *Maja Remskar*[1]; Ales Mrzel[1]; Janez Kovac[1]; Rosendo Sanjines[2]; [1]Jozef Stefan Institute, Jamova 39, Ljubljana SI-1000 Slovenia; [2]Ecole Polytechnique Federale de Lausanne, Inst. de Physique de la Matiere Complexe, EPFL-Ecublens, Lausanne 1015 Switzerland

Soon after the first report on the synthesis of MoS2 and WS2 nanotubes by sulphurization of transition metal oxides in 1992,[1] it was found that the nanotubes of the same kind can grown also by the chemical transport reaction. The advantage of lasting transport reaction is in the fact that the so-grown nanotubes contain extremely low density of structural defects.[2] The tubes grow up to several millimetre lengths with diameters ranging from several micrometers to less than ten nanometers. The MoS2 and WS2 nanotubes have been successfully alloyed with gold, silver[3] and copper. The chirality, otherwise typical for the pure MoS2 and WS2 nanotubes, was partially or completely removed in the alloyed nanotubes. The existence of noble metal-MoS2 ternary compounds gives evidence that the cylindrical geometry of crystals can stabilise new compounds otherwise unknown in a plane geometry. The sub-nanometer MoS2-xIy nanotubes have been synthesised using C60 as a growth promoter.[4] The nanotubes group to the first case of molecular crystals composed of inorganic nanotubes. Scanning tunnelling microscopy investigations of individual nanotubes and nanotube bundles will be presented. Due to the metallic behaviour these smallest known inorganic nanotubes belong to the family of promising molecular wires.[5] The conditions of synthesis will be explained and recent results of structural determination with foreseen applications will be discussed. Electron microscopy, scanning tunneling microscopy and photoelectron spectroscopy will be presented. The potential applications of inorganic nanotubes range from high porous catalytic and ultralight anticorrosive materials, non-toxic strengthening fibers to cantilevers in atomic force microscopy or tips in scanning tunneling microscopy. The bundles of sub-nanometer diameter nanotubes can be reversibly doped with lithium and have been shown to be a very promising electrode material for Li-batteries.[6] Their small diameter and metallic behaviour makes them promising also for field emission devices.[7] [1]R. Tenne et al, Nature 1992, 360, 444; [2]M. Remskar et al, Appl. Phys. Lett. 1996, 69, 351; [3]M. Remskar et al, Adv. Mater. 12 (2000) 814; [4]M. Remskar et al., Science 292 (2001) 479; [5]M. Remskar et al., Adv.Mater. 15 (2003) 237; [6]R. Dominko et al, Adv.Mater. 14 (2002) 1531; [7]V. Nemanic et al., Appl.Phys.Lett. 82 (2003), 4573.

Session S: Physics and Devices in Low Dimensional Structures

Thursday AM Room: 136
June 24, 2004 Location: DeBartolo Hall

Session Chairs: James L. Merz, University of Notre Dame, Notre Dame, IN 46556-5602 USA; Glenn Solomon, Stanford University, Stanford, CA 94305-4075 USA

8:20 AM Invited

S1, Polarization Measurements of a Single Charge-Tunable Quantum Dot: *Eric Stinaff*[1]; Allan Bracker[1]; Daniel Gammon[1]; Morgan Ware[1]; Andrew Shabaev[1]; Alexander Efros[1]; Vladimir Korenev[2]; [1]Naval Research Laboratory, Washington, DC USA; [2]A. F. Ioffe Institute, St. Petersburg Russia

The ability to observe and control the spin degree of freedom of charge carriers in quantum dots is a necessary requirement for many quantum computation proposals. We will present observations of the polarization effects arising from the spin polarization of individual charge carriers in quantum dots under various experimental conditions. Studies, performed at the Naval Research Lab, of luminescence from an individual QD as the charge state is varied from positive to neutral to negative reveals unique polarization signatures associated with each of these charge states. Single dot spatial resolution was achieved by the use of submicron apertures in a shadow mask deposited on the sample surface. The charge state was controlled by embedding the dots within a diode structure. Changes in both the sign and degree of polarization will be presented in the context of a model developed to account for the various dependencies. Among these effects are evidence of optical pumping of the isolated electron in the dot as a function of increasing power, distinct population effects as a function of applied bias, and the ability to depolarize charge carriers in an applied magnetic field. Spin lifetimes are deduced from changes in the observed photoluminescence polarization as a function of transverse magnetic field (Hanle effect). Each charge state is found to have a characteristic Hanle linewidth revealing lifetimes consistent with the model for formation put forward. The insight gained into the formation and control of the spin degree of freedom within individual quantum dots should prove valuable to their potential use in quantum information processing and spintronics. Work supported in part by ONR, NSA/ARDA, and DARPA/SPINS. ES is an NRC/NRL Postdoctoral Research Associate.

9:00 AM Student

S2, Spatial Ordering of InAs Quantum Dots in a Microdisk Cavity to Achieve Large Spontaneous Emission Enhancement: *Zhigang Xie*[1]; Glenn Solomon[1]; [1]Stanford University, Solid State Photonics Lab., CISX B113, Stanford, CA 94305 USA

Recently self-assembled quantum dots (QD) have been intensively investigated for the purpose of a single photon emitter. Due to the Purcell effect, the spontaneous emission (SE) can be greatly enhanced (on resonance) or suppressed (off resonance) by a small optical cavity. Hence a single QD on resonance with a microcavity mode will make this approach even promising. Because of its small mode volume and high quality factor, a microdisk cavity can strongly enhance the SE rate and coupling efficiency of QDs. InAs quantum dots (QDs) made by self-assembled growth naturally have a very random spatial and spectral distribution. While the spatial and spectral profile of an optical cavity mode are highly predictable. According to our FDTD calculation, the mode profile of a microdisk cavity is centered at about 150 nm to the edge. To achieve the maximum interaction of single QD SE with a cavity mode, QDs should ideally be spatially located in the cavity mode, but well isolated from nearby nonradiative surface recombination. Obviously, the traditional self-assembling growth cannot provide such spatial control. So in most cases, we either see an ensemble of QDs interaction with a cavity mode, or see an individual single QD interaction with a cavity mode, but the SE rate enhancement is not as high as expected. To

circumvent this obstacle, we have developed a patterned regrowth technique to place QDs at the antinode of a whispering gallery mode. We show that the regrowth process does not affect the QDs optical properties while maintaining reasonable cavity quality factors. In our research, we see strong evidence of sizing effect, which provide additional method to control the QD density besides traditional control, such as material deposition and growth temperature. The entire sizing effects can be explain by the limited diffusion length of In ad-atom and quantitatively agrees with our model. AFM and SEM results are shown to support our conclusion. The PL signature of our QDs is discussed, as well as the path of optically generated carriers (generation-diffusion-recombination). The QD density can be adjusted to produce low numbers of QDs (1~3 dots) per disk, so the optimal coupling of a single QD with a single cavity mode is quite plausible.

9:20 AM

S3, Multicolor Quantum Dot Infrared Photodetectors (QDIPs): *Seongsin M. Kim*[1]; [1]Stanford University, Elect. Engrg. Dept., Stanford, CA USA

Nanostructure quantum dots have been the subject of major ongoing research efforts, owing to their potential broad applications in the revolution of nanophotonics. The creation of nanostructures by selfassembly has become very important part towards the development of the new nano-scale devices such as quantum dot laser and Quantum Dot Infrared Photodetector (QDIP). Self-assembled quantum dots (SAQD) are grown by MOCVD or MBE based on Stranski-Krastanow growth mode. SAQDs appeal by the lack of non-radiative recombination due to epitaxial interfaces, typical dimensions in the 10nm to a few 10nm region providing for strong quantum confinement, as well as the compatibility with monolithic device integration. One of the emerging nano-devices, QDIPs are an important device application for the detection of mid- (MIR) and far-infrared (FIR) radiation utilizing optical inter-subband transitions. Specially QDIPs can have better performances compared to other detection technologies such as sensitivity to normal incident infrared light, larger electron-phonon (LO) scattering times which lead to longer excited state lifetime and relaxation times, and potentially high temperature operation. In addition, it is expected in better performance of multi-color detections due to narrow distribution of the discrete energy states and narrow spectrum at a detective wavelength.[1] In this work, InGaAs SAQDs were grown on InGaP or InGaAs matrices by MOCVD and fabricated as intersubband photoconductive structures. We observed bias controlled two-color photoconductive responses at mid- IR - l= 5.5mm and far-IR- l= 9.2mm at 77K. The photoresponses were sensitive to both temperature and applied bias. In our model, the origin of two-color photoresponse comes from different sub-levels, not from the size distribution of quantum dots.[2] The detailed characteristics and model will be presented. [1]Z. Ye, J. Campbell, Z. Chen, E. Kim, and A. Madhukar J. Appl. Phys. v 92, 4141, (2002). [2]S. M. Kim et al, "Characteristics of Multicolor Quantum Dot Infrared Photodetectors." (submitted, 2004).

9:40 AM

S4, Characteristics of Low Threshold Quantum Dot Lasers Operating at 1.31µm and a Study of Their Carrier Recombination Processes: *Kristian Michael Groom*[1]; Hui-Yun Liu[1]; Ian R. Sellers[2]; Tom J. Badcock[2]; Marina Gutiérrez[1]; Sumon K. Ray[1]; Jo Shien Ng[1]; Mark Hopkinson[1]; Richard A. Hogg[1]; John P.R. David[1]; David J. Mowbray[2]; Maurice S. Skolnick[2]; [1]University of Sheffield, Elect. & Elect. Engrg., Sir Frederick Mappin Bldg., Mappin St., Sheffield, S. Yorkshire S1 3JD UK; [2]University of Sheffield, Physics & Astron., Hicks Bldg., Hounsfield Rd., Sheffield, S. Yorkshire S3 7RH UK

The incorporation of self-assembled In(Ga)As quantum dots (QDs) within an InGaAs/GaAs matrix (DWELL structure) has allowed the possibility of low threshold GaAs-based lasers operating at the important telecommunications wavelength of 1.31µm. Here, we shall demonstrate how we have achieved such performance, and discuss the form of the temperature dependence of these devices. Initially, methods to overcome the problem of performance limiting gain saturation resulting from a low dot density, and a temperature stability deviating from that predicted for an ideal QD system are discussed. Such methods include the optimisation of the QD density via studies of the In composition in the $In_xGa_{1-x}As$ layers, the use of two separate In sources for growth of InAs and InGaAs layers, and the possibility of incorporating InAlAs/InGaAs barriers to increase the separation between the QD ground state transition and the barrier. Furthermore, by introducing an in-situ QD annealing step we demonstrate a significant improvement in the structural quality of the QD layers through TEM data, which corroborate with a reduction in the diode leakage current observed through electrical measurements. The removal of this leakage path has resulted in the demonstration of room temperature threshold current density (J_{th}) of 32.5Acm^{-2} at 1.31µm, with lasing via the ground state up to 100°C. Room temperature QD lasers with J_{th} as low as 32.5Acm^{-2} and 19Acm^{-2} have previously been reported.[1,2] However, with the former operating at 1.25µm, and the latter utilising high reflectivity coated facets, our result represents the lowest J_{th} for as-cleaved QD lasers operating above 1.3µm. Through optimisation of device fabrication, we demonstrate how performance can be improved further. Additionally, a study of a QD laser in which the QDs exhibit a bimodal size distribution has enabled an observation of the thermally activated spectral redistribution of carriers between different subsets of dots and a comparison with the temperature dependence of J_{th}. Below 200K, the observed negative?T_0 regime is demonstrated to result from a transition from a Fermi carrier distribution, to one in which only a limited subset of dots are populated. Above 200K, the rapid rise in J_{th} is consistent with the observation of a reduction in the integrated QD emission, indicating that carriers excited out of the dots recombine non-radiatively. A less rapid fall in integrated intensity for higher injection currents suggests that the nature of this recombination is not predominantly Auger recombination. We acknowledge the contribution of Bookham Technology, Caswell, UK. This work is supported by the UK Engineering and Physical Sciences Research Council (EPSRC) and the European Commission growth programme NANOMAT project, Contract No. G5RD-CT-2001-00545. [1]X Huang et al. IEEE Phot. Tech. Letts. 12, 227 (2000). [2]G Park et al. IEE Phot. Tech. Letts. 13, 230 (2000).

10:00 AM Break

10:20 AM

S5, Carrier Recombination Lifetime in Compressively Strained InGaAs Quantum Well Lasers Grown on GaAs Substrates: *Wataru Susaki*[1]; Tomoyoshi Ohhashi[1]; [1]Osaka Electro-Communication University, 18-8 Hatsu-Cho, Neyagawa 572-8530 Japan

Compressive strain quantum well (QW) has been introduced in lasers to realize excellent characteristics, for example, such as temperature insensitive low threshold current and high efficiency in InGaAs lasers.[1] We show the spontaneous carrier recombination life time in compressively strained InxGa1-xAs QW lasers grown on GaAs substrates increases with the compressive strain or In content x. It will be explained that introducing the compressive strain substantially eliminates the electron transition probability not responsible to the lasing. The layer structure of lasers studied is the separate-confinement-heterostructure strain - compensated single QW (SQW) InxGa1-xAs (x=0.20, 0.25, 0.30) with GaAsP barriers and InGaP waveguides,[1] and triple QW (TQW) InxGa1-xAs (x=0.14, 0.18) with GaAs wave-guides,[2] both are grown by MOVPE. The QW and wave-guide layers are not intentionally doped. The lasers are ridge stripe type with stripe width of around 2•m and the cavity length of 500•m. The threshold currents of SQW lasers are 11mA (x=0.20), 18mA (x=0.25), and 14mA (x=0.30), and, those of TQW are 31mA(x=0.14), and 29mA (0.18). The spontaneous recombination lifetime has been determined from the rate equation analysis using lasing delay time to rectangular current pulse with bias current below threshold. The delay time might include the charging time for the junction capacitance. Based on the analysis of the effect of the junction capacitance to the delay, the delay time is measured under the conditions for the bias current near threshold and pulse height less than threshold current. The carrier life times increase with x, and are 3+0.5ns, 3.5+0.5ns, 4.0+0.5ns, 5+0.5ns, and 6+0.5ns, for x=0.14, 0.18, 0.20, and 0.25, respectively. On the other hand, the lifetime of unstrained AlGaAs TQW laser (QW width: 8nm) emitting at 780 nm is 2.5ns and that of GaAs double heterostructure laser with the active layer thickness of 0.1•m is 1.9ns. Radiative carrier recombination occurs between sublevels in conduction band and sublevels in valence band in QW laser. In the lasers with 8nm QW thickness, the lasing electron transition occurs between the first electron subband (e1) and the first heavy hole subband (hh1). For carrier recombination between e1 and the first light hole subband (lh1) and, between the second electron subband (e2) and the second hole subband (hh2) is possible in unstrained AlGaAs 8nm-QW lasers for carrier injection levels at threshold from the analysis. Contribution of these non-lasing transitions results in ordinary radiative shorter lifetime. Introducing the compressive strain by adding In in the QW, energy separation between hh1-hh2, hh1-lh1

increases, and holes injection rate into the hh1 subband increases, which results in longer carrier recombination lifetime. [1]H. Asano et al., Dig. ISLC'98, 47(1998). [2]TQW lasers studied are supplied from Mitsubishi Electric Corp.

10:40 AM

S6, Optimizing the Growth of 1300 nm InAs/GaAs Quantum Dots with InGaAs and InAlAs Layers: Achievement of High-Performance Lasers: *H. Y. Liu*[1]; I. R. Sellers[2]; K. M. Groom[1]; M. Hopkinson[1]; T. J. Badcock[2]; D. J. Mowbray[2]; M. S. Skolnick[2]; [1]University of Sheffield, EPSRC Natl. Ctr. for III-V Tech., Dept. of Elect. & Elect. Engrg., Sheffield S1 3JD UK; [2]University of Sheffield, Dept. of Physics & Astron., Sheffield S3 7RH UK

Recently, the development of 1300-nm InAs/GaAs QD lasers has progressed rapidly. However, the performance of these lasers appears to be limited by gain saturation and poor temperature stability around room temperature (RT), due to a low dot density and a small energy separation between the QD ground and first-excited states. In order to improve device performance, we have increased both the QD density and energy separation by the incorporation of InGaAs and InAlAs layers. Initially, the structural and optical properties of GaAs-based 1300-nm InAs/InGaAs dots-in-a-well (DWELL) structures have been optimized by using different In compositions, x, for the InGaAs well. The QD density has been increased from $1.26x10^{10}cm^{-2}$ at x=0% to $3.6x10^{10}$ cm^{-2} at x=20%. However PL measurements reveal that the room temperature integrated intensity is sharply degraded when the In composition is increased from 15 to 20%. These results suggest that the optimum In composition is 15%. Based on these results, optimised devices exhibit excellent characteristics with a room temperature Jth of $33Acm^{-2}$ at 1307nm, with lasing via the ground state up to 100°C and negligible variation of the external slope efficiency across this temperature range. To the best of our knowledge this represents the best reported Jth for a >1300nm QD laser with uncoated facets. The use of InGaAs potential barriers in the InAs/InGaAs DWELL structures results in a reduction of the energy separation between the discrete QD energy levels. To increase this separation, a combined InAlAs-GaAs strained buffer layer (SBL) and combined InAlAs-InGaAs strain-reducing layer (SRL) were introduced into the structure. This modification results in an increase of the QD density from $1.6x10^{10}$ to $2.8x10^{10}$ cm^{-2} and an increase of the energy separation from 84 to 93 meV for optimum thickness of GaAs in the InAlAs-GaAs SBL, due to the increased confinement potential of the Al containing ternary. We have also investigated the effect on luminescence efficiency of surrounding the QDs with these thin InAlAs layers. No degradation of the low temperature or room temperature photoluminescence intensity is found as the thickness of the InAlAs layer in the InAlAs-InGaAs composite cap layer is increased. Based on these results, 1300 nm InAs/GaAs QD lasers containing InAlAs cap layers have been successfully operated at room temperature and show promise for improved high temperature operation. In conclusion, the QD density, PL intensity, and energy level separation has been modified by using an InGaAs and InAlAs-GaAs SBL and an InAlAs-InGaAs SRL. The results show some of the best performance values to date for GaAs-based 1300-nm InAs QD lasers.

11:00 AM Student

S7, Sub-Picosecond Photocarrier-Lifetimes at 1.55 µm in GaSb/ErSb Nano-Particle Superlattices: *Micah Paul Hanson*[1]; Daniel C. Driscoll[1]; Jeramy Zimmerman[1]; Elliott R. Brown[2]; Arthur C. Gossard[1]; [1]University of California, Matls. Dept., Santa Barbara, CA 93106-5050 USA; [2]University of California, ECE Dept., Santa Barbara, CA 93106 USA

Materials with short sub-picosecond photocarrier lifetimes are important for high-speed photodetectors and photomixers. Low temperature grown GaAs and more recently GaAs:ErAs have been used successfully for devices operating at 980nm. It has proved to be more difficult to produce a similar material capable of absorbing at the longer wavelength of 1.55 µm. In this paper we present carrier lifetime measurements of a series of samples grown by molecular beam epitaxy consisting of layers of semimetallic ErSb nanometer-sized particles within a GaSb matrix. We show that by adjusting the amount of ErSb, and the spacing between the layers, photocarrier lifetimes can be tuned down to less than 300 fs. ErSb grows on GaSb in an island growth mode. By depositing ErSb in amounts less than that required for the islands to coalesce into a complete film, a layer of isolated particles can be formed. This layer of ErSb particles can be epitaxially overgrown with GaSb and the process can be repeated to form a superlattice. Atomic force microscopy images of uncovered islands indicate that these particles range from about 7 Å high and 70 nm² in area for a 0.3 Å deposition to about 15 Å high and 1300 nm² in area for a 7.6 Å deposition. These particles have previously been shown to reduce the unintentional hole concentration in GaSb. In this work we find that they also act as fast non-radiative carrier recombination centers. Pump-probe lifetime measurements were made using a femtosecond Er-doped-fiber-amplified mode-locked laser and fiber-optic components in a transmission geometry. The rise time of the leading edge of the cross-correlation signal is ~300 fs, which is the temporal limit of the experiment. A series of superlattices consisting of layers of ErSb particles separated by GaSb spacer layers were grown. All superlattices were 620nm thick and grown on relaxed 500 nm AlSb buffer layers nucleated on GaAs substrates. Two sample sets were examined. In one set the period between the ErSb layers was held constant at 20nm and the amount of ErSb was varied from 0.3 Å to 6.1 Å. Larger depositions produce larger particles and result in shorter lifetimes ranging from 1.1 ps for the smallest 0.3 Å deposition to the experimental temporal resolution limit of 300 fs for the 6.1 Å deposition. A second sample set maintained a fixed 0.3 Å deposition of ErSb while the distance between the layers of particles was varied from 5nm to 40nm. As the layers of ErSb particles were brought closer together, increasing the three-dimensional density, the photocarrier lifetime was reduced down to 580 fs for the 5 nm period sample. The ability to change the photocarrier lifetime by changing layer thickness and depositions alone make this material promising for high-speed photoconducting devices.

11:20 AM Student

S8, GaAs BDD Quantum Node Switches Fabricated on Selectively MBE Grown Quantum Wire Networks: *Takahiro Tamura*[1]; Miki Yumoto[1]; Taketomo Sato[1]; Hideki Hasegawa[1]; [1]Hokkaido University, Rsch. Ctr. for Integrated Quantum Elect. & Grad. Sch. of Elect. & Info. Engrg., North 13, West 8, Kita-ku, Sapporo, Hokkaido 0608628 Japan

In spite of their large potentials for high-density, high-speed and ultra low-power LSIs, quantum devices are difficult to integrate. This is due to their low current drive and to poor threshold voltage control resulting from their high structure- and charge- sensitivity, making them unsuitable for the conventional logic gate architecture. To solve this problem, we have recently proposed a novel hexagonal binary decision diagram (BDD) quantum circuit approach[1] where logic functions are realized by nm-scale Schottky gate control of electron paths on a hexagonal quantum wire (QWR) network. Using QWRs formed by EB lithography and wet chemical etching, we have already demonstrated a 2-bit quantum adder circuit.[2] However, for higher density of integration and higher temperature operation, circuits should be fabricated on denser networks of narrower QWRs. The purpose of this paper is to report on BDD quantum node switches fabricated on hexagonal networks of embedded AlGaAs/GaAs QWRs formed by selective MBE growth. For QWR growth, hexagonal patterns of <-110>- and <510>-oriented mesas were formed on GaAs (001) substrate by EB-lithography and chemical etching. Then, GaAs buffer ridge template was grown, and finally supply of AlGaAs/GaAs/AlGaAs led to selective wire growth. The wire cross-sections were defined by high index crystalline facets whose temporal evolution was governed by facet boundary planes. Through understanding of growth mechanism, the wire width could be reduced down to a few nm, and a hexagon density of 5 x $10^{8}cm^{-2}$ has been achieved. Y-branch BDD node devices for path-switching of a single or few electrons were fabricated using wires with effective widths of several ten nm. Each of the exit branches of the device was controlled by a nm-scale Schottky wrap gate. Each branch showed clear conductance quantization at low temperatures with the first step visible up to 80K. Injecting electrons from the entry-branch and applying complementary voltage signals on gates, clear path switching between 0-th and 1-st conductance steps was observed at low temperatures. Low-power path switching was possible even at room temperature. The slope of conductance vs. gate voltage was found to be inversely proportional to temperature as expected from theory. A large slope indicated tight potential control. QWR line charge densities determined by gate-dependent SdH measurements gave gate capacitances of a few fF, indicating capability of GHz clock operation as confirmed for etched QWRs by direct microwave measurements.[3] The work reported here is supported by 21C COE Project on “Meme-Media Technology Approach to the R&D of Next-Generation Information Technologies” from MEXT, Japan. [1]S. Kasai and H. Hasegawa, IEEE, Electron Dev. Lett.23,446(2002). [2]S. Kasai, M. Yumoto and H. Hasegawa: Solid State

THURSDAY AM

Electron., vol. 47: 199-204 (2003). [3]M.Yumoto, S.Kasai and H.Hasegawa presented at 2003 EMC June, 2003.

11:40 AM

S9, Growth of PbTe-Based Superlattice Structures for High-Temperature Thermoelectric Applications: *Chris Caylor*[1]; Paul Crocco[1]; Tom Colpitts[1]; John Posthill[1]; Rama Venkatasubramanian[1]; [1]Research Triangle Institute, International, Ctr. for Thermoelect. Rsch., 3040 Cornwallis Rd., PO Box 12194, Research Triangle Park, NC 27709-2194 USA

PbTe-based materials have the potential to be used as a mid-temperature stage of a cascade thermoelectric module in combination with a low-temperature Bi_2Te_3 / Sb_2Te_3 superlattice stage. To this end, we have begun to explore low-dimensional superlattices and related structures in the PbTe-PbSe system. It is hoped to find a thermoelectric performance enhancement similar to RTI's work in the Bi_2Te_3 / Sb_2Te_3 superlattice system as well as complementing the work of Harman on PbSe quantum-dots in a PbTe matrix. An efficient PbTe-based mid-temperature stage would offer significant advantages at system level, in addition to adding several efficiency points. Hence it is critical to develop high-performance, thin-film (~10 micron) PbTe-based devices and hence high-quality materials in this superlattice system. Preliminary work using thermal evaporation produced PbTe, PbSe, and PbTe / PbSe multilayer films that were intrinsically n-type with thermal conductivities ranging from 4 W/mK for PbSe films to 2 W/mK for PbTe films. Thermal conductivity of PbTe / PbSe multilayer films have exhibited a minimum at a period of ~6nm. The lowest thermal conductivity recorded for these multilayer films was 1.1 W/mK, showing potential for TE enhancement by thermal conductivity reduction compared to pure PbTe and PbSe films. This work was conducted on 2°-off axis (100) GaAs with a substrate temperature of 350°C, which produced polycrystalline films. Further work produced PbTe, PbSe and PbTeSe films with that were extrinsically doped n- and p-type with Bi and Na respectively. These experiments were conducted on BaF_2 substrates which produced single crystal films with growth temperatures of 370°C, while mobilities and TE power factors of the individual films approach the values of bulk material. These films, on BaF_2, show a marked increase in the electrical power factor ($\alpha^2\sigma$) over the intrinsic samples, grown on GaAs. Our early results on single-layer PbTe films are significantly better than those of previously-reported MBE films; the results will be discussed from a phenomenological point of materials deposition. The use of BaF_2 as a substrate, combined with improvements to the evaporation system, enabled the growth of superlattice films of $PbTe/PbTe_{0.75}Se_{0.25}$ as demonstrated by X-ray diffraction studies. The characterization of these films will be discussed with an emphasis on the potential thermal conductivity enhancement above and beyond the previous polycrystalline multilayer films and its physical cause. The impact of this materials development will be reported with power generation device results.

Session T: Molecular Electronics I

Thursday AM June 24, 2004 — Room: 140 — Location: DeBartolo Hall

Session Chairs: Avik W. Ghosh, Purdue University, W. Lafayette, IN 47907 USA; Theresa S. Mayer, Pennsylvania State University, University Park, PA 16802-2705 USA

8:20 AM Invited

T1, Abstract not available.

9:00 AM Student

T2, Metal-Molecule-Semiconductor Heterostructure Devices on GaAs and Si: *Saurabh Lodha*[1]; Adina Scott[1]; David B. Janes[1]; [1]Purdue University, Elect. & Computer Engrg., 465 Northwestern Ave., W. Lafayette, IN 47907 USA

A key challenge for molecular devices is the nature of the electrical contacts to the molecules. While the majority of devices reported to date employ metal contacts, semiconductor contacts could allow more stable (covalent) chemical bonds as well as improved electrical properties. The energy bands of the semiconducting contact give an extra degree of freedom for enhanced device functionality. Several groups have reported metal/molecule/semiconductor (MMS) device structures on either Si or GaAs substrates. Devices reported to date have generally employed n-type semiconductor layers and have observed significant decreases in current density for MMS devices (w.r.t. comparable MS devices). The present work focuses on MMS devices employing self-assembled monolayers (SAMs) of organic monolayers within lithographically defined structures on doped semiconductor layers. The first class of devices involve SAMs of alkane-monothiols, alkane-dithiols, and aromatic-dithiols which were self-assembled on p+-GaAs following an oxide etch. IR absorption spectra and ellipsometry indicate the formation of uniform and crystalline monolayers. The Au top contacts to these devices were evaporated using a low energy, indirect path technique in order to avoid damage or penetration of the SAM. The room temperature conductance of the Au-molecule-GaAs devices is significantly higher than that of Au-GaAs control samples, and the I-V curves are much more symmetric. The low-bias currents observed in these devices also exhibit greatly reduced dependences on temperature. These observations can be explained, at least qualitatively, in terms of the electrostatic properties and density of states of the molecular layers. The presence of the molecular layer lowers the effective barrier height due to the relatively low dielectric constant of the molecules (approx. 2.2) and, in some cases, the net dipole moment of the molecules. The observed effects are consistent with previous studies of nanocontacts[1] and unpinned Schottky barriers on n-GaAs.[2] Since the barrier for carriers into the semiconductor is small, the observed current is believed to be associated with the molecular states. High current densities (>10^5 A/cm^2 at 1 V, in Au-1-octadecanethiol-GaAs devices) indicate that the molecular layers have relatively high densities of states near the metal Fermi level and that strong coupling has been achieved between the contacts and the molecules. Comparable devices are also being developed on Si (111) surfaces, using SAMs formed by reduction of diazonium salts. These SAMs are bound to the surface by a C-Si bond, which should be very stable both mechanically and electrically. [1]T. Lee et al. Ohmic nanocontacts to GaAs using undoped and p-doped layers of low-temperature-grown GaAs. Applied Physics Letters, 212, 76:2000. [2]S. Lodha et al. Fermi level unpinning in ex-situ Schottky contacts on n-GaAs capped with low-temperature-grown GaAs. Applied Physics Letters, 4452, 80:2002.

9:20 AM Student

T3, Hybrid-Basis Modeling of Transport Through Silicon-Based Molecular Devices: *Gengchiau Liang*[1]; Avik W. Ghosh[1]; Titash Rakshit[1]; Supriyo Datta[1]; [1]Purdue University, Sch. of Elect. & Computer Engrg., W. Lafayette, IN 47906 USA

Molecular electronics promises to be the basis for the next generation of electrical devices, following considerable progress in experimental techniques and theoretical studies in the area. There have been many theoretical simulations of conducting properties of molecular devices using both first-principles and semi-empirical methods. Most of the first-principles calculations give accurate results for isolated molecules; however, transport properties of molecules require an accurate description of the molecule and its interface with the contact under non-equilibrium conditions. Usually the localized basis-sets that describe molecules very well are not efficient in characterizing bulk properties of the contact, although the latter are quite important for determining the functionality of a device. Semi-empirical calculations like Extended Huckel Theory (EHT) or effective mass method are typically better equipped to modeling both the bulk and the surface physics of contacts. In this work, we discuss a formalism to couple two different basis function descriptions in order to accurately model the molecules and the contacts. As an example, we use EHT with optimized tight-binding parameters to describe bulk silicon, and couple it with an ab-initio basis, 6-31g(d), to simulate the contact surface atoms and the molecules grown on silicon. Such a coupling is achieved by matching the surface green's function in real space in both basis sets. We will use this hybrid-basis formalism to describe STM measurements on molecules like styrene (C8H8) grown on silicon. Our simulations predict a prominent negative-differential resistance (NDR) in such molecular I-Vs due to the interaction between the molecular levels and the silicon band-edge. According to this mechanism, NDR is expected to occur only for negative sample bias on n-type Si(100) and for positive sample bias on p-type Si(100). Experimental observations of

this bias dependent NDR for differently doped substrates support our theoretical predictions.

9:40 AM

T4, Electrical Properties of Organic/Silicon Junctions: *Gregory P. Lopinski*[1]; Thomas J. Hammond[1]; Bruno Fabre[1]; Danial D.M. Wayner[1]; [1]National Research Council, Steacie Inst. for Molecular Scis., 100 Sussex Dr., Ottawa, Ontario K1A 0R6 Canada

Covalent attachment of organic molecules to silicon surfaces offers the promise of constructing hybrid organic/silicon molecular devices that may be useful for memory, logic and/or sensor applications. Silicon surfaces modified with alkyl chains are prepared via photochemical and thermal reactions with atomically flat H-terminated Si(111) surfaces and were characterized by STM, HREELS and Kelvin probe measurements. Various methods of forming electrical contact to these monolayers have been explored including use of liquid metal drops, metal evaporation and electrochemical growth of conducting polythiophene. The use of conducting polymer for the top contact is found to be particularly useful, avoiding potential damage to and/or penetration of the organic layer that may result from metal deposition. This method also results in a device structure with covalent contacts at both electrodes yielding improved stability and electronic coupling. Electron transport in the resulting structures follows that expected for MIS (metal-insulator-semiconductor) diodes, controlled by a combination of electron tunneling through the organic layer and thermionic emission over a Schottky barrier at the silicon/molecule junction. Temperature dependent measurements have been used to separate these contributions and extract barrier heights and voltage dependent tunneling probabilities. Low voltage tunneling probabilities extracted from polythiophene/decyl/Si(111) structures(~ 0.5-2x10^-6) are reasonably consistent with previous measurements on various self-assembled monolayer systems on metal surfaces. Photo and current-induced charge trapping is observed to alter the I/V characteristic of these diodes, indicating that surface states play an important role in determining the transport properties of these silicon/organic junctions. Processing strategies for minimizing these surface state densities will also be discussed.

10:00 AM Break

10:20 AM Student

T5, A Self-Consistent Transport Model for Molecular Conductors with Few Applications to Real Systems: *Ferdows Zahid*[1]; Magnus Paulsson[2]; Eric Polizzi[1]; Avik W. Ghosh[1]; Supriyo Datta[1]; [1]Purdue University, Elect. & Computer Engrg., EE Bldg., 465 Northwestern Ave., W. Lafayette, IN 47907-2035 USA; [2]Danish Technical University, Physics, Sorgenfrivej 3, Lyngby 2800 Denmark

We develop a self-consistent transport model for molecular conductors by coupling Extended Huckel Theory (EHT) with Non-equilibrium Green's Function (NEGF) formalism. The electrostatic potential of the molecule is calculated self-consistently by a combination of CNDO (complete neglect of differential overlap) method and finite element method (FEM). Our self-consistent electrostatic potential incorporates both the charging and screening effects inside the molecule under applied bias. The electrostatic potential is a functional of density matrix and we have divided it into three separate parts: (i) the Poisson part which incorporates the charging and screening effects and it is calculated self-consistently using CNDO approximation, (ii) the Laplace part which is just the solution of Laplace equation in free space and it is calculated using FEM with proper boundary conditions, (iii) the image correction term which incorporates the effect of electrodes around the molecular device and it is calculated self-consistently using FEM. As this model is based on a semi-empirical method it is computationally inexpensive compare to other ab-initio models yet at the same time it is able to preserve the complete accuracy in terms of physical characteristics. We believe our transport model can be very useful in describing many physical characteristics of molecular conductors which have been experimentally observed. We apply this model to investigate the origin of asymmetry in various measured current-voltage (I-V) characteristics of molecules with no inherent spatial asymmetry with particular focus on a recent break junction measurement and achieve an excellent match between theoretical and experimental I-V characteristics, both in shape as well as overall magnitude. We argue that such asymmetry arises due to unequal coupling with the contacts and a consequent difference in charging effects, which can only be captured in a self-consistent model for molecular conduction. The direction of the asymmetry depends on the sign of the majority carriers in the molecule. For conduction through highest occupied molecular orbitals (i.e. HOMO or p-type conduction), the current is smaller for positive voltage on the stronger contact, while for conduction through lowest unoccupied molecular orbitals (i.e. LUMO or n-type conduction), the sense of the asymmetry is reversed. We are also investigating few other physical characteristics of molecular conductors: (i) changes in potential profile and I-V characteristics of the molecular device under the influence of gate voltage, (ii) characterization of the contact region of the molecule and the electrodes and its effects on the I-V characteristics, (iii) explaining the I-V characteristics of different conjugated aromatic thiols experimentally observed in STM measurements and (iv) effect of different substrate materials (e.g. Silicon) on the I-V of the molecular devices.

10:40 AM Student

T6, Inelastic Electron Tunneling Spectroscopy of Self-Assembled Alkanedithiol Monolayers: *Wenyong Wang*[1]; Takhee Lee[1]; Ilona Kretzschmar[1]; Mark A. Reed[1]; [1]Yale University, Elect. Engrg., Applied Physics, & Physics, PO Box 208284, New Haven, CT 06520 USA

In the past several years tremendous progress has been made in the electronic transport characterization of self-assembled monolayers (SAMs). Alkanethiol (CH3(CH2)n-1SH) is one of the molecular systems that has been studied extensively due to its ability to form a robust SAM on gold surfaces. Recently tunneling has been identified as the main conduction mechanism for alkanethiol SAM, as expected since the Fermi levels of contacts lie within a large HOMO-LUMO gap of a short length molecule. In this study, electronic tunneling behavior through alkanethiol SAMs is further investigated with the technique of inelastic electron tunneling spectroscopy (IETS). Electronic transport measurements on octanedithiol SAMs are performed with a nanoscale test structure. Temperature-variable current-voltage (I(V)) measurements are carried out between 300 and 4.2 K. No significant temperature dependence of the I(V) characteristics is observed, confirming that tunneling is the transport mechanism for octanedithiol SAM. IETS spectra are obtained via the lock-in second harmonic (proportional to dG/dV) measurement technique. The IETS spectra of the octanedithiol device clearly show vibrational signatures of an octanedithiolate bonded to gold electrodes. The pronounced IETS peaks at 4.2 K correspond to vibrational modes perpendicular to the junction interface, which include the stretching modes of Au-S (at 33 mV) and C-C (at 133 mV), and wagging mode of CH2 (at 158 mV), identified from comparison with previously reported infrared, Raman, and high resolution electron energy loss spectra of SAM covered gold surfaces. Peaks at 80, 107, and 186 mV are also reproducibly observed but are less pronounced, and they correspond to CH2 scissoring, rocking, and stretching modes, respectively, which are parallel to the interface. This observation of the orientation-dependent peak intensities is in agreement with IETS theoretical predictions. IETS peak width broadening effect is examined as a function of AC modulation voltage and temperature. IETS is performed with different modulations at a fixed temperature of 4.2 K. The observed full width at half maximum (FWHM) of the peak (C-C stretching) agrees with theoretical calculation considering thermal (~ 5.4 kT) and modulation (~ 1.7 V_rms) broadening effects with a saturation of the linewidth at low modulation. An intrinsic linewidth of 3.73 +/- 0.98 mV is determined from this modulation broadening effect. The thermal broadening of the peak width is also studied with a fixed modulation at temperatures from 4.2 to 80 K, and experimental FWHMs are in excellent agreement with calculations considering thermal broadening, modulation broadening, and the intrinsic linewidth determined above.

11:00 AM Student

T7, In-Situ Analysis of In-Wire Molecular Junctions Using Inelastic Tunneling Spectroscopy: *Marco A. Cabassi*[1]; Lintao Cai[1]; Yoram Selzer[2]; David L. Allara[2]; Thomas E. Mallouk[2]; Theresa S. Mayer[1]; [1]Pennsylvania State University, Elect. Engrg., 121 Elect. Engrg. E., Univ. Park, PA 16802 USA; [2]Pennsylvania State University, Chmst., 152 Davey, Univ. Park, PA 16802 USA

Inelastic electron tunneling spectroscopy (IETS) is an in-situ analysis technique that has recently been applied to determine the vibrational spectra of several nanoscale molecular junctions. Because the peaks in the spectra can be related to specific infrared (IR) and raman active vibrational modes of the molecule, the technique can yield strong evidence that the measured transport properties are due to the intended

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molecules rather than an artifact introduced during junction fabrication. In this talk, we will present the current-voltage characteristics and IETS spectra measured using sub 40-nm diameter in-wire metal-molecule-metal junctions containing oligo-(phenylene ethynylene) (OPE) molecular wires and their ¡VNO2 derivatives (NOPE). The in-wire junctions are synthesized by replicating the pores of polycarbonate mesoporous membranes using sequential electrodeposition and molecule self assembly steps. Following synthesis, the 5 ?Ým long nanowires are released from the membrane and electrofluidically aligned between pairs of lithographically defined large area electrodes. Room temperature electrical measurements on junctions containing these and other molecular wires such as oligo-(phenylene vinylene) (OPV) show differences in conductance that are expected based on their differing molecular structure.[1] IET spectra were obtained by cooling these junctions to 10 K and collecting the second harmonic of the current as a function of bias using a digital lock-in amplifier with a 6 mV rms, 500 Hz excitation voltage. Two predominant peaks at 180 and 284 mV were observed in the IETS spectra of the NOPE junctions, which can be tentatively assigned to the vibration of the ¡VNO2 moiety and the alkyne stretch of this molecule. This will be compared to IET spectra obtained for OPE molecular wires. These results indicate that our in-wire junctions are free of process induced artifacts and can be confidently used to study transport mechanisms in metal-molecule junctions. [1]Cai, L. T.; Skulason, H.; Mattzela, J. B.; Kushmerick, J. G.; Pollack, S. K.; Naciri, J.; Shashidhar, R.; Allara, D. A., Mallouk, T. E.; Mayer, T. S. J. Phys. Chem. B (2004) in press. The authors would like to acknowledge the Tour group (Rice University) for providing the molecules used in this study.

11:20 AM Cancelled

T8, Charge Transport and Scaling in Molecular Wires: *Amy Szuchmacher Blum*[1]; James G. Kushmerick[1]; Steven K. Pollack[1]; Martin H. Moore[1]; Jawad Naciri[1]; Raganathan Shashidhar[2]; B. R. Ratna[1]; [1]Naval Research Laboratory, Ctr. for Bio/Molecular Engrg., Code 6930, 4555 Overlook Ave. SW, Washington, DC 20375 USA; [2]Geo-Centers, Inc., Maritime Plaza One, Ste. 050, 1201 M St. SE, Washington, DC 20003 USA

Despite a large degree of interest in understanding charge transport through individual molecules, measurements conducted on different metal-molecule-metal systems using different techniques often yield dramatically different results. Thus, the scaling rules for transport through collections of molecules remain of great interest. Here, we present conductivity measurements for three different classes of molecular wire compounds as measured via scanning tunneling microscopy (STM) and a crossed-wire tunnel junction, allowing us to investigate conductance on two size scales. We show that STM measurements on single molecules correlate well with crossed-wire measurements of ~10^3 molecules. Our data implies that the conductance through a group of parallel molecules is a linear superposition of the individual molecular conductance. These results also indicate that intermolecular charge hopping does not strongly contribute to charge transport in a self-assembled monolayer, an important factor for the design of future molecular-based devices.

Session U: III-Nitride Growth

Thursday AM June 24, 2004 — Room: 155 — Location: DeBartolo Hall

Session Chairs: Russell D. Dupuis, Georgia Institute of Technology, Atlanta, GA 30332-0250 USA; Andrew A. Allerman, Sandia National Laboratories, Albuquerque, NM 87185 USA

8:20 AM Student

U1, The Compositional Dependence of Phase Separation in InGaN Alloys: *Manu Rao*[1]; Subhash Mahajan[1]; [1]Arizona State University, Chem. & Matls. Engrg., PO Box 876006, Tempe, AZ 85287-6006 USA

Phase separation is predicted to occur in InGaN alloys and has been observed in several experimental studies. Theoretical calculations have shown that the equilibrium solubility of InN in bulk GaN is approximately 6% at typical MOCVD growth temperatures. The situation in epitaxially deposited thin films is significantly different. Strain in the epilayer due to mismatch with the underlying substrate has an energy associated with it and this leads to a shift in the critical temperature for phase separation. The situation is complicated by the fact that In incorporation may itself be a function of the level of strain, which in turn varies with the layer thickness. Using a metal-organic chemical vapor deposition (MOCVD) system, thick GaN buffer layers were deposited on (0001) sapphire substrates. The buffer layers were thick enough to be relaxed and therefore form a "virtual substrate" for growth of InGaN. InGaN was then deposited covering a range of compositions. TEM was performed on [10-10] cross-sections and [0001] plan-view samples. Calculations were also performed to evaluate the influence of coherency strain on the equilibrium phase diagram. At very low InN contents (~3%), plan-view TEM images show a homogenous microstructure and selected area diffraction (SAD) patterns show no evidence of phase separation. With higher InN contents (~11%), a speckled contrast is observed in the images. Closely spaced satellites are present around fundamental reflections in SAD patterns. These are indicative of composition modulations. Samples containing InN contents of between 22 and 28% have microstructures exhibiting much stronger local contrast. This may occur as a result of strain associated with phase separation. SAD patterns also exhibit satellite spots, which are further spaced from the fundamental reflections, implying shorter modulation wavelength. Cross-sectional TEM images from the samples exhibiting phase separation show a lack of contrast in the epilayer for 25-50 nm from the GaN/InGaN interface. The thickness to which this occurs depends on the overall layer composition. It appears that coherency strain due to growth on the GaN buffer layer suppresses phase separation, a result which is consistent with theoretical calculations. However, relaxation begins to occur during the early stages of InGaN growth and therefore coherency strain alone cannot account for the lack of phase separation observed within 25-50nm. Preliminary evidence suggests that In is initially rejected from the InGaN layer. This occurs since lower In incorporation lessens the mismatch and strain energy associated with epitaxial deposition on the GaN buffer. Therefore, the In content of the alloy in the vicinity of the interface is low enough that phase separation does not occur in this region. As the layer progressively relaxes, In incorporation increases and consequently phase separation occurs. Further experimentation will clarify whether this is indeed the case. The support of this work by NSF is gratefully acknowledged.

8:40 AM

U2, Crystal Quality of InN Thin Films Grown on ZnO Substrate by RF-MBE: *Satoru Ohuchi*[1]; Toshiyuki Takizawa[1]; [1]Matsushita Electric Industrial, Semiconductor Device Rsch. Ctr., 1-1, Saiwai-chou, Takatsuki, Osaka 569-1193 Japan

Recently InN has been emerged as a candidate for the application to high-speed electric devices. Sapphire has been usually used as a substrate for InN growth, therefore, its large lattice-mismatching to InN (more than 25%) generates a lot of dislocations and consequently degrades the crystal quality. Y. Nanishi et al have demonstrated InN growth on GaN free-standing substrate which has small lattice-mismatching (11%) and successfully obtained high quality InN thin film on only N-face substrate.[1] Wurtzite ZnO has a lattice constant close to InN (the lattice-mismatching of around 9%) and can be a candidate as a substrate. However, the properties of InN grown on ZnO substrate has never been reported yet. In this study we have demonstrated InN thin films grown by RF-plasma molecular-beam epitaxy (RF-MBE) on ZnO substrate and have successfully obtained high quality InN thin films. We employed both Zn- and O-face c-axis ZnO substrates to study the surface effects of the substrate. First the thermal cleaning was executed on the ZnO substrate at the temperature of 720°C for 30 min, then InN thin film was directly grown at the growth temperature of 550°C for 1 h. The crystal quality of InN thin films grown was estimated by X-ray diffraction (XRD) and transmission electron microscopy (TEM). We successfully obtained black and mirror-like InN thin films grown on both Zn- and O-face ZnO substrate, whereas the difficulty of InN growth on Ga-face GaN substrate has been reported. The growth rate of InN thin films grown on each substrate was around 0.2 µm/h, and the bandgap was estimated to be 0.8 eV by photoluminescence study. According to the

cross-sectional TEM study of InN thin films obtained, the InN layer around the top was orderly grown, although a transition InN layer induced by lattice-mismatching was found above the interface (the thickness of around 10 nm). The defect density was estimated around $5x10^{10}$ cm^{-2} from TEM study. Especially, the full width at half maximum (FWHM) of XRD rocking curve of InN (0002) has been recorded to be 150 arcsec, which value is very small compared with previously reported. In addition no Zn diffusion into InN film was detected by secondary ion mass spectroscopy (SIMS). In conclusion, wurtzite ZnO substrate has a potential to realize high quality InN film. [1]F. Matsuda, Y. Saito, T. Muramatsu, T. Yamaguchi, Y. Matsuo, A. Koukitu, T. Araki and Y. Nanishi, ICNS-5 (2003), Tu-P2.099.

9:00 AM Student

U3, Microstructure and Enhanced Morphology of Planar Nonpolar m-Plane GaN Grown by Hydride Vapor Phase Epitaxy: *Benjamin Allen Haskell*[1]; Feng Wu[1]; Hideo Sasano[1]; Paul T. Fini[1]; Steven P. DenBaars[1]; James S. Speck[1]; Shuji Nakamura[1]; [1]University of California, Engrg. Matls. Dept., Santa Barbara, CA 93106-5050 USA

Nonpolar (1-100) m-plane gallium nitride has been found to grow heteroepitaxially on (100) γ-$LiAlO_2$ by several groups. Previous attempts to grow m-plane GaN by hydride vapor phase epitaxy (HVPE) yielded films unsuitable for subsequent device regrowth due to the high densities of faceted voids intersecting the films' free surfaces. We report here on the growth of planar m-plane GaN films on (100) γ-$LiAlO_2$ and elimination of such bulk and surface defects. The surface morphology achieved is now smooth enough to allow for the fabrication of m-plane GaN templates and free-standing substrates for subsequent nonpolar device regrowth. GaN films were grown in a conventional three-zone horizontal HVPE reactor at substrate temperatures of 860-890°C. Typical growth rates ranged from 30 to 240 µm/hour, yielding free-standing films of up to 90 µm thickness. The m-plane GaN films were optically transparent and mirror-like, with gentle undulations 50-200 nm peak-to-valley over millimeter length scales. Atomic force microscopy revealed a finely striated surface morphology, similar to that observed in m-plane GaN films grown by molecular beam epitaxy. Local RMS roughness was 0.89 nm over 25 μm^2 areas, comparable to planar nonpolar a-plane GaN films. Plan-view and cross-sectional transmission electron microscopy were performed on the m-plane GaN films to quantify microstructural defect densities. Basal plane stacking faults were found with a density of 1×10^5 cm^{-1}, while threading dislocations could be observed in the g = 0002 diffraction condition with a density of 4×10^9 cm^{-2}.

9:20 AM

U4, Fabrication of GaN Quantum Dots on AlGaN Template by Liquid Droplet Epitaxy: *Maria Gherasimova*[1]; S.-R. Jeon[1]; G. Cui[1]; J. Su[1]; Z. Ren[1]; J. Han[1]; Y. He[2]; Y.-K. Song[2]; A. V. Nurmikko[2]; [1]Yale University, Dept. of Elect. Engrg., PO Box 208284, New Haven, CT 06520 USA; [2]Brown University, Div. of Engrg., 182 Hope St., Providence, RI 02912 USA

Compound semiconductor quantum dots (QDs) are of interest as a potential active medium component in optoelectronic devices, as well as an object of study of physical phenomena related to zero-dimensional carrier confinement. Formation of GaN islands on AlN templates due to the mismatch-induced compressive strain has been reported.[1] However, the use of AlN as a template presents a major hindrance to the incorporation of GaN dots into electrically injected structures due to its limited conductivity. Alternative approaches to GaN island formation include the use of silicon as anti-surfactant on AlGaN templates[2] and nitridation of Ga droplets on SiC by nitrogen-seeded gas source in vacuum.[3] In the present work, GaN QDs on conductive AlGaN templates were synthesized by metalorganic chemical vapor deposition (MOCVD) using nanoscale gallium droplets as an intermediate phase, a procedure referred to as liquid droplet epitaxy (LDE). The nucleation of Ga droplets and their subsequent conversion to GaN islands in the presence of ammonia (NH3) were investigated by atomic force microscopy (AFM), scanning electron microscopy (SEM) and photoluminescence (PL). We will report on the observations related to the Ga droplets morphology as a function of MOCVD growth conditions and correlate them with the model of heterogeneous nucleation. The discrete nature of nano-droplets is preserved upon conversion with NH3 exposure, even though hexagonal facets emerge due to the transformation into crystalline phase. QDs ranging between 10 and 100 nm in lateral size and between 2 and 50 nm in height were observed by AFM and SEM, with the typical densities on the order of 10^10 cm-2. PL spectra obtained with the 266 nm excitation at room temperature exhibit distinct peaks at approximately 340 nm for samples even without any capping of AlGaN, suggesting high optical functionality in the QDs prepared by LDE. The authors acknowledge the support of DOE NETL. [1]M. Miyamura, K. Tachibana, Y. Arakawa, Appl. Phys. Lett. 80 3937 (2002). [2]J.-S. Lee, S. Tanaka, P. Ramvall, H. Okagawa, MRS Symposium, Fall 2003 meeting. [3]C.-W. Hu, A. Bell, F. A. Ponce, D. J. Smith, I. S. T. Tsong, Appl. Phys. Lett. 81 3236 (2002).

9:40 AM Student

U5, Analysis of GaN on Highly-Compliant Nanoscale Silicon Pillar Arrays: *Xinyu Sun*[1]; Jianyu Liang[2]; Jimmy Xu[2]; Steve Hersee[1]; [1]University of New Mexico, Ctr. for High Tech. Matls., 1313 Goddard SE, Albuquerque, NM 87106 USA; [2]Brown University, Div. of Engrg., Box D, Providence, RI 02912 USA

Theory and experiment indicate that the strain due to lattice mismatch can be accommodated by connecting a substrate and an epilayer using compliant nanoscale bridges. This paper describes the TEM (transmission electron microscopy) analysis of GaN grown on dense Si nanopillar arrays that were fabricated using an anodic-aluminum-oxide membrane. The nanopillar diameter in these novel substrates was approximately 40 nm with some pillars as small as 20 nm in diameter. Electron microscopy analysis of the GaN reveals several novel defect reduction mechanisms that reflect the high compliance of this novel form of substrate. Stacking faults (SFs) were the dominant defect type and these were generally found within ~100nm of the epi/substrate interface. In about ~10% of the coalescence regions grain boundary defects occurred indicating tilting between adjacent nuclei. Importantly, high-resolution TEM shows that these grain boundary defects can "heal" and they are then followed by high quality GaN. This unusual "healing" mechanism is in some cases accompanied by the generation of a SF and appears to be related to the extreme compliance of the nanopillar substrate. Voids were present at the GaN/Si interface on approximately half of the nanopillars. The void structure appears to be further strain reduction mechanism, that is analogous to a Stranski-Krastanov growth mode. These results will be compared to previous examples of nanoscale heteroepitaxy. The TD (threading dislocation) density is greatly reduced in these samples and based on examination of many TEM images we estimate that at a distance of 0.3 mm from the heterointerface the TD density is < 108 cm-2. This analysis reveals that the silicon nanopilllar array is a highly compliant substrate for GaN growth and this paper will discuss the latest measurements on these samples.

10:00 AM Break

10:20 AM

U6, Growth and Characterization of Single Crystal GaN by the Ammonothermal Method: *Michael J. Callahan*[1]; Kelly Rakes[1]; David F. Bliss[1]; Lionel O. Bouthillette[1]; Buguo Wang[2]; Sheng-Qi Wang[2]; Robert Lancto[2]; [1]Air Force Research Laboratory, Sensors Direct., AFRL/SNHC, 80 Scott Dr., Hanscom AFB, MA 01731 USA; [2]Solid State Scientific Corporation, 27-2 Wright Rd., Holis, NH 03049 USA

Commercially available low dislocation GaN substrates would allow enhancement of nitride device reliability and performance. Ammonothermal growth is a promising cost effective technique for growing GaN ingots for use as high quality substrates because of its similarity to large-scale industrial quartz growth. Several crystals of GaN were grown simultaneously on C-plane HVPE seeds with surface areas approaching $1cm^2$ in an autoclave under mild conditions (< 550°C and 3 kpsi) using potassium amide as a mineralizer. Hundreds of microns of single crystal GaN verified by high resolution x-ray diffraction was grown ammonothermally on the gallium and nitrogen faces of the HVPE seeds. Process conditions and characterization of the ammonothermal GaN by AFM, SEM, Pl, SIMS and high-resolution x-ray diffraction will be presented. Finally initial plans to scale up and optimize the ammonothermal system to obtain 25 mm diameter crystals with thicknesses of several millimeters will be discussed.

10:40 AM Student

U7, Bulk GaN Growth by Sublimation: Phanikumar Konkapaka[1]; *Huaqiang Wu*[1]; Yuri N. Makarov[2]; Michael G. Spencer[1]; [1]Cornell University, Elect. & Computer Engrg., 401 Phillips Hall, Ithaca, NY 14853 USA; [2]Semiconductor Technology Research, Inc., Richmond, VA 23255 USA

GaN is one of the most interesting wide band gap semiconductor materials that is useful for fabrication of laser diodes [LD], light emitting diodes [LED] and high power, high frequency electronic devices. But, due to the severe shortage of GaN substrates, these devices are fabricated on foreign substrates such as SiC, Sapphire, $LiGaO_2$ or $LiGaO_3$. Hence, they are suffering from high dislocation density [10^7-$10^{11}cm^{-2}$] and bending caused by lattice mismatch and thermal expansion coefficient mismatch respectively between GaN epi layer and substrate. Homoepitaxy of GaN by developing GaN substrates is the only way to address this problem. In the present work, bulk GaN is grown by transporting Ga vapor that is obtained from decomposing GaN powder. Ammonia was used as the source of Nitrogen. A novel growth cell design was used to grow bulk GaN layers. Bulk GaN single crystal layers of 8.5 mm x 8.5 mm size were grown on GaN epi on Sapphire substrates at growth rates > 200 microns per hour at 1155°C at a total pressure of 600 Torr. Double crystal X-ray rocking curve yielded a lower FWHM for the grown GaN layer compared to that of the substrate indicating a higher quality of grown GaN layers. SEM and AFM characterization showed the growth mode to be dislocation mediated spiral growth. Electrical properties were characterized by Hall Effect measurement. The grown bulk GaN crystals have a mobility of 550 cm^2/Vs and a carrier concentration of 6.67 x 10^{18} cm^{-3}.

11:00 AM

U8, Characterization of AlInGaN Based Heterostructures Grown by Migration Enhanced Metalorganic Chemical Vapor Deposition: *Qhalid Fareed*[1]; Jianping Zhang[1]; Remis Gaska[1]; Ibrahim Yilmaz[2]; Gintautas Tamulaitis[2]; Michael S. Shur[2]; M. Asif Khan[3]; [1]Sensor Electronic Technology Inc., 1195 Atlas Rd., Columbia, SC 29209 USA; [2]Renssaeler Polytechnic Institute, Troy, NY 12180 USA; [3]University of South Carolina, Dept. of Elect. Engrg., Columbia, SC 29208 USA

We present our data on Migration Enhanced Metal Organic Chemical Vapor Deposition (MEMOCVD™) epitaxial technique for growth of AlN/GaN/InN films and heterostructure layers on SiC and sapphire substrates. Using this new technique, we achieved a better mobility of precursor species on the surface and, thus, better atomic incorporation and improved surface coverage, which yield improved surface morphology, reduced density of growth defects and increased carrier lifetime in the materials. X-ray diffraction and photoluminescence studies show improvement in the quality of layers. Non destructive light induced transient grating measurements of GaN layers show carrier lifetime more than 400ps for GaN layers with MEMOCVD™ buffer layers which is more than 4 times higher compared to the layers on conventional MOCVD buffers. Atomic force microscopic studies shows fine step growth morphology with root mean square roughness below 2Å which is about 3 times improvement over conventional MOCVD deposition. We used the advantages of MEMOCVD™ for fabrication of Deep UV LEDs with peak emission wavelengths in 250 nm - 365 nm range, low-temperature (comparable to MBE) growth of high quality InN-on-GaN heterostructures, and high-temperature growth of uniform Heterostructure Field Effect Transistor epitaxial wafers.

11:20 AM

U9, Using Optical Reflectance to Quantify GaN Evolution on Sapphire: *D. D. Koleske*[1]; M. E. Coltrin[1]; K. C. Cross[1]; M. J. Russell[1]; A. A. Allerman[1]; [1]Sandia National Laboratories, Albuquerque, NM USA

In this presentation we will show how physical models can be applied and fit to the optical reflectance waveform yielding kinetic and roughness information at all stages of MOCVD GaN growth. Three stages of the growth are of particular interest, namely the initial GaN nucleation layer (NL) deposition, the NL evolution as it is annealed before high temperature growth, and the transition from island growth to 2D coalescence. The NL thickness can be monitored and controlled using optical reflectance. In one set of samples the reflectance signal was used to control the NL thickness to within 0.1 nm. after growth, the NL was heated in H_2 and NK_3 to temperatures > 1000°C. During this annealing reflectance signal started to decrease. As the temperature was increased further, the decomposition accelerated and GaN nuclei formed from the gas phase desorbed GA atoms, causing eh NL to roughen. This was shown in AFM images of NLs that were interrupted along the annealing schedule and by attenuation of the optical reflectance signal. Taking into account the NL decomposition kinetics we show how NL roughness can be calculated independent of the reflectance waveform. We will show several examples where different NLs were annealed to their maximum roughness and how the roughness calculated from the AFM images agreed with the roughness calculated from the reflectance waveform. Finally, the transition from island growth to 2D coalescence can be monitored and intentionally delayed.[2] The reflectance waveform can be analyzed during this transition to obtain the GaN roughness and the waveform can be modeled using an analytical grain growth model. Implication of the fits to the reflectance waveform will be discussed in relationship to growth reproducibility and changes to the growth kinetics. [1]D. D. Koleske, et al., Appl. Phys. Lett 82, 1770 (2003). [2]D. D. Koleske, et al., Appl. Phys. Lett 81, 1940 (2002).

Session V: Surface Engineering and Thin-Film Transistor Performance

Thursday AM — Room: 101
June 24, 2004 — Location: DeBartolo Hall

Session Chairs: William S. Wong, Xerox Corporation, Palo Alto Rsch. Ctr., Palo Alto, CA 94304 USA; C. Dan Frisbie, University of Minnesota, MN USA

8:20 AM Invited

V1, Pentacene Thin Film Transistors and Integrated Circuits: Performance, Stability, and Operating Voltage: *Hagen Klauk*[1]; Marcus Halik[1]; Ute Zschieschang[1]; Günter Schmid[1]; Christine Dehm[1]; [1]Infineon Technologies, New Memory Platforms, Matls. & Tech., Paul-Gossen-Str. 100, Erlangen 91052 Germany

We have used the small-molecule aromatic hydrocarbon pentacene to fabricate organic thin film transistors and integrated circuits on glass and on flexible polymeric substrates, using solution-processed polyvinylphenol as the gate dielectric and photolithographically patterned gold source/drain contacts. Transistors on glass substrates typically have carrier mobilities near 0.5cm^2/Vs, and ring oscillators operate with signal propagation delays near 20µsec per stage. To evaluate the operational and environmental stability, we have processed 32 nominally identical glass substrates and measured TFT and ring oscillator performance before and after exposing the substrates to elevated temperatures, increased humidity, repeated thermal cycling, and electrical stress. In most cases the observed changes in TFT and circuit performance are reasonably small. For example, after cycling two substrates with six ring oscillators 300 times between 20 and 80°C, the signal delay changed from initially (17±5)µsec to (21±5)µsec per stage. At room temperature and in ambient humidity, TFTs can be operated continuously for several days without degradation in performance. Ring oscillators operate continuously for several hours and in that time perform more than 10^7 switching cycles. When stored under ambient conditions, the performance of TFTs and ring oscillators remains virtually unchanged for more than 12 months. The polymer gate dielectric pentacene TFTs and circuits described above typically operate with supply voltages between 20 and 40V. To reduce the operating voltage and make organic electronics suitable for low power applications we have developed pentacene TFTs with an ultra-thin molecular self-assembled monolayer gate dielectric. With a gate dielectric thickness of 2.5nm these TFTs can be operated with supply voltages as low as about 2V while offering small threshold voltage (near 1V), excellent subthreshold swing (between 100 and 200mV/decade), large on/off current ratio (greater than 10^4), large carrier mobility (as high as 1cm^2/Vs), and low gate leakage (usually less than 100pA). These self-assembled monolayer dielectrics are sufficiently robust to permit the use of standard photolithographic and wet chemical etching techniques, allowing TFTs with channel lengths of a few microns and large transconductance to be fabricated.

9:00 AM Student

V2, Pentacene OTFT with Parylene Active Layer Patterning and Passivation: *Lisong Zhou*[1]; Thomas N. Jackson[1]; [1]Pennsylvania State University, Elect. Engrg., 121 Elect. Engrg. E., Univ. Park, PA 16802 USA

Organic thin film transistors (OTFTs) are of interest for flat panel displays and other large-area electronic applications. Recently, and active matrix polymer dispersed liquid crystal display was demonstrated using pentacene OTFTs, with photosensitized polyvinyl alcohol (PVA) used to pattern the pentacene active layer.[1] However, PVA is permeable to moisture which may be a problem for OTFT stability or for applications where OTFTs are combined with devices that are degraded by water, for example organic light emitting diodes. As an alternative to photosensitized PVA, we have used parylene C as a barrier layer to allow pentacene patterning with conventional photolithography. In this approach, the parylene C is used to isolate the pentacene layer from the photolithography chemicals that would otherwise degrade the organic semiconductor film.[2] To demonstrate the utility of parylene passivation and photo-patterning, we have fabricated patterned-active-layer pentacene OTFTs. Heavily doped thermally oxidized silicon was used as the substrate, gate electrode, and gate dielectric for these devices. Platinum source and drain contacts were deposited by ion beam sputtering and photo-lithographically defined using a lift-off process. A pentacene active layer with 50 nm average thickness was deposited by thermal evaporation after vapor treatment of the SiO2 surface with octadecyltrichlorosilane. An ~1mm thick parylene C layer was vapor deposited at near room temperature onto the pentacene active layer a passivation layer. Conventional solvent-based photolithography was used to form photoresist structures on top of the device active areas and the unwanted regions of the pentacene active layer were removed by oxygen plasma etching. Parylene and photoresist have similar etch rates and etching was continued until the photoresist was entirely removed. Devices were tested prior to deposition of the parylene film and after active layer patterning. Typical mobility was 0.5 - 1.0 cm2/V-s for these devices before patterning. After patterning the device threshold voltage was unchanged, but mobility decreased by about 40%. Off current was in the pA range and the substhreshold slope was improved compared to devices patterned using photosensitive PVA. [1]C. D. Sheraw, L. Zhou, J. R. Huang, D. J. Gundlach, T. N. Jackson, M. G. Kane, I. G. Hill, M. S. Hammond, J. Campi, B. K. Greening, J. Francl and J. West, "Organic Thin-Film Transistor-Driven Polymer-Dispersed Liquid Crystal Displays on Flexible Polymeric Substrates," Applied Physics Letters, vol. 80, n. 6, February 2002. [2]D. J. Gundlach, T. N. Jackson, D. G. Schlom, and S. F. Nelson, Appl. Phys. Lett., vol. 74, p. 3302 (1999).

9:20 AM

V3, Gate Dielectric Surface Modification for Controlling the Threshold Voltage and Subthreshold Characteristics of OTFTs: Kurt P. Perstich[1]; Daniel Oberhoff[1]; *David J. Gundlach*[1]; Bertram Batlogg[1]; [1]Laboratory for Solid State Physics, ETH Zurich, HPF-F9, Zurich 8093 Switzerland

Over the past decade the electrical performance of Organic Thin Film Transistors (OTFTs) has improved significantly. Efforts have mainly concentrated on increasing the charge carrier field-effect mobility and various organosilanes that form Self Assembled Monolayers (SAMs) have been used to advantageously modify the gate dielectric surface properties to increase the field-effect mobility. We report on the use of organosilanes with various dipole moments to modify the gate dielectric surface for controlling the threshold voltage and subthreshold characteristics of OTFTs. In this study we fabricated top contact pentacene TFTs on heavily doped and thermally oxidized silicon wafers. Prior to the pentacene film deposition the silicon dioxide surface was treated with solutions containing various organosilanes that form SAMs and characterized by static contact angle measurements. Depending on the organosilane the field-effect mobility ranged from 0.1 to 1.0 cm^2/Vs. More significant was the variation in the threshold voltage (V_T = 26 to -13 V), the subthreshold slope (S = 4.9 to 0.9 V/decade), and the switch-on voltage (V_{SO} = 49 to -1.9 V) which showed a clear dependence on the dipole orientation of the various organosilane molecules. The molecules of the SAMs can be simplistically viewed as increasing or decreasing the density of mobile carriers in the region between the SiO_2 surface and the first few molecular layers of pentacene by shifting the surface potential. Because the subthreshold characteristics are strongly dependent on the film microstructure (structural and chemical defects) and the resulting electronic structure we also investigated films deposited on treated substrates held at various temperatures. With increasing substrate temperature the molecular order as characterized by XRD, and correspondingly the mobility, was improved for pentacene films on most SAMs, but almost no change in threshold voltage was observed. In our experiments the SAMs are not affected by the substrate heating so we find their effect on the subthreshold characteristics and threshold voltage to be substrate temperature independent. Our use of organosilanes provides a unique method to further optimize OTFT performance and demonstrates that controlling the interface properties is of critical importance.

9:40 AM

V4, Organic Field-Effect Transistors Prepared by Ink-Jet-Printing and Spin-Coating from Different Solutions of Poly-3-Octylthiophene: *Matthias Ploetner*[1]; Thomas Wegener[2]; Stefan Richter[1]; Steffen Howitz[2]; Wolf-Joachim Fischer[1]; [1]Dresden University of Technology, IHM, Dresden D-01062 Germany; [2]GeSiM, Rossendorf, Großerkmannsdorf D-01454 Germany

We investigated organic field-effect transistors using commercially available poly-3-octylthiophene as semiconductor. In order to compare different deposition technologies with different solutants we made use of simple uniform test devices in bottom-contact design. They have been prepared on thermally oxidized doped Silicon as gate dielectrics/gate electrodes with lift-off patterned source/drain-contacts of Au on top. The semiconductor has been deposited as a final step without additional intermediate films. Ink-jet printing has been performed using a piezoelectric actuated microfluidic pipette developed by GeSiM. It enables droplets with a volume in the order of 380 pl to be dosed in a drop-on-demand sequence. This allowed us to adjust jetting parameters to the needs of droplet formation for a certain ink. One key parameter for ink-jet printing is the choice of the solutant. Using the most common chloroforme we did not succeed in printing. Trichlorethylene worked better yielding single dots, but lines were obtained with stacked dots only and, as a result, the transistor behaviour remained poor. Best results have been obtained using chlorobencene or xylole as solvent. Using these inks lines of about 180 µm in width have been printed on top of S-channel-D-structures with channels of 15 .. 50 µm in width and 1 .. 3 mm in length. Although ink-jet printing led to thick edge bulges at the side walls of the lines, this did not act to the smaller channels within. In between the bulges of jetted lines we obtained films with comparatively uniform thicknesses of about 8 .. 15 nm depending on concentration. In order to estimate the influence of the deposition technology and the rather uncommon solutants we additionally prepared oFETs by spinning the organic semiconductor on the same test vehicles. Both oFET transfer and output characteristics have been measured. Simple calculations with those data yielded field-effect hole mobilities of up to 1.10-3 cm^2/Vs and threshold voltages of about +5 .. 10 V. The limitation to these moderate values may be attributed to the preparation under normal humid atmosphere and application of chemicals as delivered. The experiments pointed out that i - transistor properties of oFETs with ink-jetted channels were not significantly diminished compared to ones with films spin-coated under the same conditions, ii - problems with gate leakage and/or gate charging observed at blanket films from spin-coating disappeared with patternd features from ink-jetted semiconductors. As a result of this we conclude that ink-jet printing does not only offer a very versatile technology for deposition and patterning of organic field-effect transistors for low cost electronics, but a useful tool to investigate different oFET materials without the problems accompanied by blanket deposition.

10:00 AM Break

10:20 AM Student

V5, Low Temperature a-Si:H TFT on Polymer Substrates with Improved Stability: *Lisong Zhou*[1]; Thomas N. Jackson[1]; [1]Pennsylvania State University, Elect. Engrg., 121 Electl. Engrg. E., Univ. Park, PA 16802 USA

a-Si:H TFTs fabricated are of interest for applications in light weight, rugged, and flexible electronics. To accommodate low-cost commercially available polymeric substrates, fabrication temperatures less than about 150°C are required, significantly lower than is typically used for fabrication on glass substrates (>250°C). Several groups have demonstrated a-Si:H TFTs fabricated on polymeric substrates at or below 150°C[1,2] however, most had poor device electrical stability or did not report stability at all. Using hydrogen dilution for both a-Si:H and silicon nitride deposition, we have fabricated trilayer TFTs on glass (Corning 7059) and 50 mm thick Kapton® polyimide substrates at 150°C with performance and stability similar to devices fabricated at 250°C. To maintain substrate flatness and provide improved thermal transfer, we

used a pressure-sensitive silicone gel adhesive layer[3] to mount polymeric substrates onto glass carriers. 50 nm thick chromium gate electrodes were deposited by thermal evaporation and patterned by wet etching. A tri-layer stack of SiNx gate dielectric (350 nm)/active layer a-Si:H (50 nm)/passivation SiNx (300 nm) was then deposited using a three chamber load-lock plasma-enhanced chemical vapor deposition (PECVD) system with a maximum temperature of 150°C. The SiNx was deposited with a gas mixture of SiH_4:NH_3:H_2 = 1:10:45 at 0.5 torr and the a-Si:H with SiH_4:H_2 = 1:10 at 0.5 torr. After a-Si:H active layer and passivation SiNx layer patterning a 50 nm n-type microcrystalline silicon (n+ μC-Si) contact layer and 200 nm thick molybdenum (Mo) source and drain contact electrodes were deposited by PECVD at 150°C and DC sputtering, respectively. The Mo contacts were then patterned by CF_4 reactive ion etching (RIE) and wet etching, and the n+ μC-Si by chlorine-based RIE. Finally, the sample was annealed for 30 minutes at 150°C. The characteristics for devices fabricated on Kapton® and glass substrates are very similar with linear region and saturation region mobility of 0.8 cm^2 /V-s and 1.0 cm^2 /V-s, respectively, low sub-threshold slope (0.3 - 0.5 V/ decade), and low threshold voltage (2 - 4 V). TFT stability was characterized by bias stressing at VG = VD = 20V for 600 seconds. Devices on either Kapton® or glass show threshold voltage shift less than 1.3 V, which is comparable to TFTs fabricated at 250°C and significantly better than for devices fabricated at low temperature with a standard silicon nitride deposition process. [1]H. Gleskova, S. Wagner, V. Gasparík and P. Kováè, J. Electrochem. Soc., 148, G370-G374 (2001). [2]C.S. Yang, L.L.Smith, C.B.Arthur, G. N. Parsons, J. Vac. Sci. Technol. B, 18, page 683-689 (2000). [3]J.R. Huang, Y. Lee, C.M.C. Toporow, G.J. Vendura, Jr., T.N. Jackson and C.R. Wronski, 26th IEEE Photovoltaic Specialists Conference, page 699-702 (1997).

10:40 AM Student

V6, Improved Solution-Deposited OTFT Performance by Dielectrics and Electrode Surface Treatments: *Chung-Chen Kuo*[1]; Sungkyu Park[1]; E. Bullock[2]; John E. Anthony[2]; Thomas N. Jackson[1]; [1]Pennsylvania State University, Dept. of Elect. Engrg., 121 Elect. Engrg. E. Bldg., Univ. Park, PA 16802 USA; [2]University of Kentucky, Dept. of Chmst., Lexington, KY 40506 USA

We previously demonstrated solution-deposited organic thin film transistors (OTFTs) based on triisopropylsilylethynyl pentacene (TIPS-pentacene), a soluble small molecule organic semiconductor, with mobility > 0.1 cm^2/V-s.[1] These first devices had poor contact characteristics, which limited their performance. To improve carrier injection, four thiolates contact treatments were tested: pentafluorobenzenethiol, 3,4-dichlorobenzenethiol, 4-nitrobenzenethiol, and 2-mercaptobenzimidazole. In addition, to improve the growth of the TIPS-pentacene layer on the gate dielectric we used a polymer brush treatment. For this treatment a layer of polystyrene-c-methyl-methacrylate (PS-c-MMA) dissolved in toluene is spun on the SiO_2 dielectric sample. After drying the sample is heated to 160ºC for several hours. Excess PS-c-MMA is then removed with toluene, leaving a 10nm thick polymer brush on the SiO_2 surface. After brush deposition, contacts are deposited, patterned, and thiol treated, if desired. OTFTs are then completed by depositing TIPS-pentacene from chlorobenzene or toluene. OTFT field-effect mobility for brush and thiol treated devices typically ranged from 0.05 to 0.22 cm^2/V-s. [1]K. Shankar and et al, the 61st Device Research Conference, (2003).

11:00 AM

V7, Control of Transport by Self-Assembled-Monolayers in Organic Field-Effect Transistors: *Shin-ichiro Kobayashi*[1]; [1]Tohoku University, Inst. for Matls. Rsch., Iwasa Lab., Katahira, Aoba-ku, Sendai City, Miyagi prefecture 2-1-1 Japan

In the case of MOSFET, the channel carrier density without application of gate voltage is controlled by ion implantation techniques. In organic field-effect transistors (TFT), similar doping techniques, hopefully without disturbing the stacking of organic molecules are highly demanded. To achieve the control of channel conductance or carrier density without gate voltage, we paid attention to the organic self-assembled-monolayers (SAMs), which have often been used to improve the field-effect mobility in various organic TFTs. In this study, we demonstrate that, by changing the molecules for the SAMs on SiO2 substrates, the channel carrier density is controlled in the organic TFTs. We have grown three kinds of organic SAMs using silane compounds F-, Me-, and NH2-SAMs by the CVD process. Here, F-, Me-, and NH2-SAMs correspond to (CF3)(CF2)7(CH2)2Si(OC2H5)3, (CH3)(CH2)7Si(OC2H5)3, and (NH2)(CH2)3Si(OC2H5)3 molecules, respectively. Thin films of C60 and pentacene were fabricated on top of this monolayer by a molecular beam deposition. We showed the relation between SAMs observed threshold voltage (Vth) and determined from square root of drain current-gate voltage ((ID)1/2-VG) curves for pentacene and C60 TFTs. The effect of end groups of SAMs molecules on the threshold voltage is consistent between C60 and pentacene TFTs. The F-SAMs and NH2-SAMs shift Vth values to positive and negative sides, respectively, while the effect of Me-SAMs is in between the two. An interpretation of Vth is that, below this particular voltage, charge carriers are localized due to the surface traps. When the carrier density produced by gate voltage exceeds the number of traps, the drain current takes off, and this onset is observed as Vth. Thus Vth value is determined by the density of traps and the carrier density at gate VG=0V. In conclusion, we have presented a novel method of controlling the surface charge density in the organic TFTs using SAMs sandwiched by gate insulators and active organic films. This simple technique provides a simple way of controlling interface charge, which should be quite useful for fabricating organic TFTs with desired performance.

11:20 AM

V8, Microcantilever Arrays as Biological and Chemical Sensors: *Steven L. Tripp*[1]; Babita Dhayal[1]; Ronald Reifenberger[1]; [1]Purdue University, Dept. of Physics & Ctr. for Sensing Sci. & Tech., 525 Northwestern Ave., W. Lafayette, IN 47907 USA

Chemical and biological sensors have a wide range of applications from environmental and medical monitoring to testing for biological and chemical warfare agents.[1,2,3] While the primary effort has been to create highly selective and sensitive sensors with quick response times and a long operating lifetime, the scalability of the sensors to smaller dimensions is also of critical interest. Specificity is also a major concern in the design of sensors. However, since high specificity inevitably translates into a binding chemistry that produces strong (irreversible) binding events, highly selective sensors usually implies a limited lifetime. A new type of sensor uses microcantilevers as a nanomechanical sensing platform.[4] Microcantilevers offer two forms of detection: the first being a change in resonance frequency due to mass uptake and the second being a static deflection due to relative changes in surface stress. Both methods have high sensitivity and quick response times, with specificity dependent on the surface functionalization. The use of parallel microcantilever arrays has been proposed for the detection of multiple analytes simultaneously.[5] Our research focuses on the general use of microcantilever arrays for parallel detection of multiple analytes in both gaseous and liquid environments. Our system employs an array of eight microcantilevers and has the capability of measuring cantilever deflection or frequency change in both gaseous and liquid environments. Unoptimized performance in liquid phase yields sensitivities of ~2 ppm, with a response time of ~30 sec. Noise in the cantilever deflection signal in gas phase is < 0.5 nm. Temperature-induced deflections on the order of 1 nm/ °C were observed, requiring the construction of a temperature-controlled, light-tight box. Slight pressure changes in gas and liquid delivery systems give a false transient signal, requiring the design of a flow system to maintain constant pressures (ΔP ~ 0.4 mPa). We are currently designing techniques for the simultaneous, unique functionalization of all eight cantilevers to accommodate a wide range of chemical coatings including self-assembled monolayers (SAMs), polymers, and biological molecules. Results of sensing experiments we have already conducted will also be described. [1]K. J. Albert, N. S. Lewis, C. L. Schauer, G. A. Sotzing, S. E. Stitzel, T. P. Vaid, and D. R. Walt, Chem. Rev. 100, 2595 (2000). [2]A. J. Ricco, R. M. Crooks, and G. C. Osbourn, Acc. Chem. Res. 31, 289 (1998). [3]M. G. Nikolaides, S. Rauschenbach, S. Luber, K. Buchholz, M. Tornow, G. Abstreiter, and A. R. Bausch, ChemPhysChem 4, 1104 (2003). [4]T. Thundat and L. Maya, Surf. Sci. 430, L546 (1999). [5]F. M. Battiston, J.-P. Ramseyer, H. P. Lang, M. K. Baller, Ch. Gerber, J. K. Gimzewski, E. Meyer, and H.-J. Güntherodt, Sens. and Actuat. B77, 122 (2001).

11:40 AM Student

V9, Controlling Kinesin-Microtubule Biomolecular Nanomotors: *Ying-Ming Huang*[1]; Maruti Uppalapati[2]; Thomas N. Jackson[1]; William O. Hancock[2]; [1]Pennsylvania State University, Dept. of Elect. Engrg., 121 Elect. Engrg. E., Univ. Park, PA 16802 USA; [2]Pennsylvania State Uni-

versity, Dept. of Bioengrg., 218 Hallowell Bldg., Univ. Park, PA 16802 USA

Kinesins are molecular motors that move along microtubules, providing a model system for force generation that can be exploited for developing kinesin-powered nano- and micro-machines.[1] Microtubules are ~25 nm diameter cylindrical polymers of the protein tubulin and can be many microns long. Kinesins bind to microtubules and use the energy of ATP hydrolysis to walk unidirectionally along these tracks at speeds of ~1um/s. A key requirement for extracting useful work from this system is to attain directional movement from microtubules moving over kinesin coated surfaces. Hiratsuka, et al, used microfabricated walls of patterned SAL601 photoresist[2] and Moorjani, et al, used the epoxy-based photoresist SU-8 to pattern 1.5 um deep microchannels on glass substrates to localize motility and direct microtubule movements.[3] Jia, et al, also showed the microtubules could be sorted by using electrophoresis and dielectrophoresis.[4] Here we report the chemical properties of the surface can affect the interaction of motors with the surface and thus determine the activity of the motors. We observe that motors are partially inactive on low energy, hydrophobic surfaces (for example, octadecyltrichlorosilane treated surfaces), causing the microtubules to bind to surface without moving. However on a range of high energy, hydrophilic surfaces (for example, oxygen plasma treated surfaces) the motors are active and can move microtubules long distances. We find that surface topography can have a strong effect, for example microtubule motility tests on kinesin-functionalized replica gratings show motion primarily along grating ledges with motion across grating step inhibited. These results demonstrate that both physical and chemical properties can be used to confine and direct biomolecular nanomotors. [1]J. Howard, the Movement of Kinesin along Microtubules, Annu. Rev. Physiol. 58, pp. 703-729 (1996). [2]Y. Hiratsuka, T. Tada, K. Oiwa, T. Kanayama and T. Q. P. Uyeda, Controlling the Direction of Kinesin-Driven Microtubule Movements along Microlithographic Tracks, Biophys. J., 81, pp.1555-1561 (2001). [3]S. G. Moorjani, L. Jia, T. N. Jackson, and W. O. Hancock, Lithographically Patterned Channels Spatially Segregate Kinesin Motor Activity and Effectively Guide Microtubule Movements, Nano lett., Vol.3 No. 5, pp. 633-637 (2003). [4]L. Jia, S. G. Moorjani, T. N. Jackson, and W. O. Hancock, Microscale Transport and Sorting by Kinesin Molecular Motors, Biomedical Microdevices, 6:1, pp 67-74 (2004).

Session W: Mismatched Materials: Metamorphic and Growth on Templates

Thursday AM — Room: 129
June 24, 2004 — Location: DeBartolo Hall

Session Chairs: David Wilt, NASA, Glenn Rsch. Ctr., Cleveland, OH 44135-3127 USA; Ralph Dawson, University of New Mexico, Albuquerque, NM 87106 USA

8:20 AM Student

W1, Extended Defect Microstructure of Metamorphic Buffer Layers Based on AlGaSb and InAsP: *G. Suryanarayanan*[1]; A. A. Khandekar[2]; T. F. Kuech[3]; S. E. Babcock[4]; P. W. Deelman[5]; R. D. Rajavel[5]; K. Elliott[5]; D. H. Chow[5]; [1]University of Wisconsin, Matls. Sci. Prog., 1509 Univ. Ave., #201A MSE Bldg., Madison, WI 53706 USA; [2]University of Wisconsin, Dept. of Chem. Engrg., 1415 Engrg. Dr., Madison, WI 53706 USA; [3]University of Wisconsin, Dept. of Chem. Engrg. & Matls. Sci. Prog., 1415 Engrg. Dr., Madison, WI 53706 USA; [4]University of Wisconsin, Dept. of Matls. Sci. & Engrg. & Matls. Sci. Prog., 1509 Univ. Ave., Madison, WI 53706 USA; [5]HRL Laboratories, RL61B, 3011 Malibu Canyon Rd., Malibu, CA 90265 USA

InAs-based high-speed electronics suffer from the lack of suitable lattice-matched semi-insulating substrates. As a result, GaAs and InP have been used as substrates in conjunction with a metamorphic buffer. Transistor device structures based on such compositionally-graded metamorphic buffer layers have shown excellent device performance despite the potential for a large number of extended defects. The specific nature of the extended defect structure of these metamorphic buffer layers has not been presented in detail. In this paper we will compare and contrast the extended defect structure of metamorphic buffer layers based on AlGaSb or InAsP on (100) GaAs and InP substrates respectively using cross-sectional transmission electron microscopy (TEM). Plan-view TEM was also used to study defect microstructure of the InAs-based device layers on top of these buffer layers. The nature of the extended defect structure as well as the dislocation density was measured as a function of distance from the substrate. There is a clear reduction of defect density with distance from the substrate. Significant defect reduction occurs at two locations in the film, just above the substrate, where a dense defect structure appears in the first few tens of nanometers of the substrate, and at the interface to the active device layers. The drop in dislocation density from near substrate to near surface is ~5x. Mismatch dislocations are visible at the substrate/film interface region in a network of approximately uniformly spaced dislocations running along <110> directions. The estimated spacing between these mismatch dislocations is ~5nm and their contrast is consistent with either 60º or 90º dislocations. The threading dislocations that characterize the regions above the mismatch dislocations and in the metamorphic buffer layers are entangled. In addition to threading dislocations, stacking faults are also observed extending across the device layers. The dislocation densities were ~10^9 cm^{-2} close to the active device layers. The defect density reduction with film thickness was more rapid using the thinner 300 nm InAsP buffer than with the 1.7 μm AlSb/AlGaSb buffer layer. Many of the dislocations that thread through the InAsP buffer from the substrate bend parallel to the substrate near the device layers which was not observed with the AlGaSb buffer layer. The determination of the extended defect structure and its interaction with the specific physical and chemical nature of the metamorphic buffer layers can be used to design improved buffer layers to enhance the defect density reduction leading to better improved performance and possibly reliability in high-speed electronic devices.

8:40 AM

W2, Comparison of Mixed Anion, InAsP and Mixed Cation, InAlAs Metamorphic Buffers Grown by MBE on InP Substrates and Device Implications: *Mantu K. Hudait*[1]; Yong Lin[1]; Steven A. Ringel[1]; [1]Ohio State University, Elect. Engrg., 205 Dreese Lab., 2015 Neil Ave., Columbus, OH 43210 USA

A wide range of new device opportunities exist for III-V InGaAsP semiconductors with lattice constants greater than that of InP due to the reduction in electron effective mass and the narrowing of the direct bandgap. Hence, compositionally step-graded buffers (SGBs) on InP are receiving recent and substantial interest, since such buffers may generate a virtual substrate so that lattice-matched, metamorphic device structures with large lattice constants can be grown. The III-V semiconductors offer several pathways to achieve optimum metamorphic structures between the lattice constant of InP and InAs, by grading either on the anion (group-V) or cation (group-III) sublattice. The purpose of this paper is to compare both $In_xAl_{1-x}As$ cation SGBs with $InAs_yP_{1-y}$ anion SGBs from the viewpoints of growth advantages, strain relaxation efficiency, dislocation density and surface morphology, using solid source MBE. For the purpose of this study, both $InAs_yP_{1-y}$ and $In_xAl_{1-x}As$ compositionally SGB layers were grown on InP so that each type of buffer spans the identical range of lattice constants and misfit strain with respect to InP. A total, nominal misfit from substrate to final layer of 1.2% was chosen, requiring the $InAs_yP_{1-y}$ composition to span from y=0 to y=0.40, and the $In_xAl_{1-x}As$ composition to span from x=0.52 to x=0.70. For optimized growth, RHEED investigations indicated that even though the initial (2x4) symmetry of the InP surface was maintained for both InAsP and InAlAs GB growths, the RHEED patterns were far sharper for the mixed anion buffers. This in-situ observation was found to be consistent with ex-situ AFM studies for which the well-developed crosshatch patterns observed for each type of buffer, displayed a distinct roughness in the field for the InAlAs that was not present for the InAsP. The RMS roughness of ~7nm for the InAlAs was approximately 4 times greater than that of the InAsP GB. In spite of the differences in surface morphology, triple axis x-ray diffraction revealed that both mixed anion and cation buffers symmetrically relaxed the 1.2% misfit strain to similar levels of ~90%, with negligible tilt (~20-200 arcsec) with nearly equal numbers of α([1-10]) and β([110]) dislocations during the relaxation process, indicating an insensitivity to asymmetric dislocation kinetics. However, TEM analysis indi-

cates the presence of phase decomposition for the InAlAs graded layers, with no such degradation in the InAsP layers, consistent with the improved surface for the InAsP graded buffer. The impact of these structural differences on electronic quality of the relaxed buffers will be presented in the context of thermophotovoltaic device performance. Finally, the additional degree of freedom in MBE growth control that is allowed by grading on the anion sublattice during MBE growth of metamorphic buffers will be discussed.

9:00 AM Student

W3, Doping Studies in Metamorphic AlSb and InAlSb Films: *Peter O. Hill*[1]; Sanjay Krishna[1]; L. R. Dawson[1]; Philip Dowd[1]; [1]University of New Mexico, Ctr. for High Tech. Matls., 1313 Goddard SE, Albuquerque, NM 87106 USA

In recent years, there has been considerable interest in the development of mid-wave infrared emitters operating in the range of 2-5 micron for applications such as remote sensing, LADAR, surveillance and reconnaissance, missile tracking, and infrared countermeasures. Advances in epitaxial growth have allowed the development of “Arsenic-free” optically pumped lasers on GaSb substrates, using relaxed graded-composition InAlSb layers grown using a digital alloying technique. Previous work with these structures displayed significantly higher characteristic temperature values than comparable wavelength GaSb lattice-matched lasers or mixed group V lasers due to improved confinement for both electrons and holes. In order to realize electrically pumped structures, doping effects in the Antimonide layers need to be better understood. To date, relatively little work has been carried out on these materials with regard to doping studies and characterization. Typically, Antimonide materials are not as easily doped as Arsenides and this appears especially true when doping n-type. Silicon, a common donor in GaAs, is amphoteric in GaSb and a good acceptor in AlSb. The group II acceptor activation in antimonide material systems, namely Beryllium, is comparable to arsenide materials yielding carrier densities of >10^18cm-3. Therefore the donor elements from group VI need to be investigated for AlSb and InAlSb films, namely Tellurium. Hence the majority of this study was performed on n-type materials, which initially have exhibited lower conductivity than arsenides. In this abstract, we report studies of n (and p) doped AlSb and InAlSb grown by solid-source molecular beam epitaxy on semi-insulating GaAs substrates. Thick (3-5 micron), relaxed layers of either AlSb or nominally 30% In-content InAlSb were deposited at growth rates between 0.7 and 1.0 micron/hr. The GaTe donor source shutter was opened after the characteristic 1X3 RHEED pattern was observed. Samples were grown between 500C and 515C, and the temperature of the GaTe source was fixed at 475C which provided carrier densities from mid-10^17cm-3 to 10^19cm-3. The range in carrier concentration is an artifact of relative dopant cell position, growth temperature, and growth rate. Samples were then metallized with indium dots and the contacts were annealed at 150C for 5 minutes. Ionized carrier densities were measured using the Van der Paaw/Hall technique over a 70° temperature range. The data was plotted on semi-log scales (ln N vs. 1/kT), and the ionization energy of the Tellurium donors was extracted from the characterstic slope. Preliminary results indicate that Tellurium in AlSb forms a donor level 36meV below the conduction band (CB) edge whereas the donor level for Tellurium in InAlSb is between 58meV and 100meV below the CB edge, and appears to be dependent on the In content. Further experimental details and results will be presented at the conference. Work supported by MDA/AFOSR Grant F49620-03-1-0437.

9:20 AM

W4, Surface Reconstruction Domains During the Growth and Annealing of InGaAs Alloys: *Alex Riposan*[1]; Brad G. Orr[2]; Chris Pearson[3]; [1]University of Michigan, Matls. Sci. & Engrg., 2200 H.H. Dow Bldg., Ann Arbor, MI 48109 USA; [2]University of Michigan, Applied Physics, 1115 Aberdeen Dr., Ann Arbor, MI 48103 USA; [3]University of Michigan, CSESP, 303 E. Kearsley St., Flint, MI 48502 USA

The surface reconstructions of InGaAs compound semiconductor alloys were investigated at different stages during growth and during annealing. Films of different compositions were grown by Molecular Beam Epitaxy (MBE) under various growth conditions and analyzed in-situ by Scanning Tunneling Microscopy (STM). The composition of the surfaces was measured ex-situ by X-ray photoelectron spectroscopy (XPS). It was found that the atomic structure of these surfaces depends on film composition and misfit strain and changes during film growth and annealing. We examined the atomic surface structure of In0.27Ga0.73As/GaAs(001) and In0.81Ga0.19As/InP(001) ternary alloys. Both these compositions possess the same amount of misfit strain (1.9% in compression) with respect to the substrate. The surface reconstruction of these layers is generally more disordered than those of their binary counterparts, and consists of different reconstruction domains. In particular, both surfaces show domains of a mixed-terminated (4x3) reconstruction, which is better ordered for the high In composition. Domains with a regular x3 but an irregular 4x periodicity, (nx3), are also observed, especially at low In compositions. In addition, there are pockets of α2(2x4) in the case of In0.27Ga0.73As/GaAs, and β2(2x4) in the case of In0.81Ga0.19As/InP. The coverage of both (2x4) reconstructions decreases during annealing, concomitant with a decrease in In surface concentration due to In desorption. This suggests that the (2x4) reconstructions are enriched in In compared to the (4x3)/(nx3). The coverage of different reconstructions also changes with film thickness, following changing surface composition and increasing strain energy. In the case of the In0.27Ga0.73As films, the In composition at the surface increases with film thickness and reaches a saturation level, in agreement with previous reports. The coverage of the (4x3) reconstruction reaches a saturation level at the same time, suggesting that a high and stable In concentration at the surface and/or a high strain energy favor a better ordered (4x3). The coverage of the α2(2x4) reconstruction increases initially with film thickness, then it decreases as the strain energy continues to increase, despite the fact that the surface reaches a stable composition. These results point out the importance of considering the effects of strain energy and inhomogeneous composition in the understanding of alloys surface structure.

9:40 AM Student

W5, Development of Metamorphic Buffers on InP for 6.00Å Narrow Bandgap Heterojunction Bipolar Transistors: *Randy Sandhu*[1]; A. Cavus[1]; C. Monier[1]; M. Lange[1]; A. Noori[2]; S. L. Hayashi[2]; M. Wojtowicz[1]; T. Block[1]; M. S. Goorsky[2]; A. Gutierrez-Aitken[1]; [1]Northrop Grumman Space Technology, Semiconductor Matls., R6/2134D, One Space Park, Redondo Beach, CA 90278 USA; [2]University of California, Matl. Sci. & Engrg., Los Angeles, CA 90095 USA

6.00Å based InAlAs/InGaAs heterojunction bipolar transistors (HBTs) offer several performance advantages over lattice-matched compound semiconductor HBTs grown on InP (5.88Å). They include higher electron mobilities, higher peak electron velocities, and narrow energy band gap, to be beneficial for achieving high frequency performance at lower power dissipation. Among the challenges associated with narrow-bandgap materials with high indium content is the absence of suitable semi-insulating substrates. This paper will discuss development of metamorphic buffers as a platform for innovative HBT band gap engineering with a lattice parameter towards that of InAs. In this presentation, we compare device performance and defects in HBTs grown on compositionally graded buffer layers and constant composition buffer layers. Molecular beam epitaxy (MBE) was employed to achieve fully relaxed metamorphic InAlAs buffers on SI InP substrates to serve as templates for 6.00Å-based lattice parameter In0.86Al0.14As/In0.86Ga0.14As double heterojunction bipolar transistors (DHBTs). Two different types of buffer approaches were investigated in this study in order to achieve the optimal template for 6.00Å-based DHBT device performance. In the first approach, a 0.9-um thick graded buffer layer (GBL) was used in which the InxA1-xlAs buffer indium mole fraction was graded from lattice-matched (xIn = 0.52) to 6.00Å (xIn = 0.86). The graded buffer growth parameters were optimized to achieve complete strain relaxation during growth while minimizing dislocation interactions. In the second approach, In0.86Al0.14As constant composition buffer layers (CCBL) of total thickness ranging from 0.9, 2, and 5 m in thickness were grown directly on InP. 6.00 Å narrow band gap In0.86Al0.14As/In0.86Ga0.14As DHBT structures were grown directly on top of the different metamorphic buffer layers. Representative 80x80-mm2 AFM area images from the DHBT surfaces grown on the different buffer layers show that the GBL exhibits a crosshatch pattern whereas the CCBLs show no evidence of a crosshatch pattern. The GBL structures possess low threading dislocation densities (~106 cm-2) and a lack of dislocation pile-ups. The CCBL structures tend to have higher threading density (as high as 109 cm-2). Large-area devices with 30x30 mm2 emitter active area were fabricated to evaluate the impact of the buffer design on transistor elec-

trical characteristics. In the case of the DHBTs grown on CCBLs, a DC gain around 20 is obtained with the use of the 0.9 m thin buffer. Slight improvement is achieved by increasing the buffer thickness with b up to 35 using a 5 m buffer. However, the increase in CCBL thickness severely impacts the device thermal response as observed by the thermal slump in the DC IVs. On the other hand, devices grown using only 0.9-um graded buffer exhibit the highest b of 80. The base-collector junction diode characteristics 4, show similar trend of improvement with GBL versus CCBL approach by 2 orders of magnitude. The difference of density of dislocations correlates well with the improved device performance of the structures. Initial results from material and device characterization indicate that metamorphic graded buffer layers with optimised growth conditions offer a suitable platform for developing narrow bandgap HBT technology for low-power applications.

10:00 AM Break

10:20 AM
W6, Strain Relief of $In_xGa_{1-x}As$ Selectively Grown on Nanoscale SiO_2-Patterned GaAs(001) by Molecular Beam Epitaxy: *S. C. Lee*[1]; L. R. Dawson[1]; B. Pattada[1]; S. R.J. Brueck[1]; [1]University of New Mexico, Ctr. for High Tech. Matls. & Dept. of Elect. & Computer Engrg., 1313 Goddard, SE, Albuquerque, NM 87106 USA

Epitaxial growth of a strain-relieved $In_xGa_{1-x}As$ layer, free from misfit dislocations, on a nanoscale SiO_2-patterned substrate GaAs(001) is reported. A 40-nm thick SiO_2 mask layer is patterned with a 355-nm period 2-D array of circular holes using large-area interferometric lithography and dry etching. On this SiO_2-patterned substrate, a 50-nm thick GaAs buffer and a 200-nm thick $In_{0.06}Ga_{0.94}As$ layer were grown by molecular beam epitaxy (MBE) at 595°C, which is within the range of typical MBE growth temperatures for GaAs but is above the desorption temperature of In atoms from a GaAs surface. At this temperature, selective growth mode was achieved with a Ga flux of 1.4×10^{13} atoms/cm^{2}s and an In flux having a low, but finite, incorporation rate of about 0.2% leading to a $In_{0.06}Ga_{0.94}As$ layer. Deposition of $In_xGa_{1-x}As$ on SiO_2-patterned GaAs(001) selectively begins within each GaAs open circular area and laterally proceeds over the SiO_2 mask resulting in coalescence between $In_xGa_{1-x}As$ regions originating from adjacent nucleation sites. After overall coalescence, the $In_xGa_{1-x}As$ surface becomes smooth and flat. Cross section TEM of the as-grown sample confirms epitaxial growth of the $In_{0.06}Ga_{0.94}As$ layer over the SiO_2 mask. The boundary between the amorphous SiO_2 mask and the single crystal $In_{0.06}Ga_{0.94}As$ was clearly revealed. Crystalline defects were not found near the coalescence regions. In both cross section and plan-view TEM, no misfit dislocations were observed. In spite of high growth temperature and spatially nonuniform substrate, the TEM results suggest that the crystallinity of the $In_{0.06}Ga_{0.94}As$ layer is not severely degraded. Double crystal x-ray diffractometry, provides additional information on the crystalline structure. From the analysis of peak separation results, the $In_{0.06}Ga_{0.94}As$ layer was almost fully relaxed. The ratio of the difference between the in-plane lattice constant of the $In_{0.06}Ga_{0.94}As$ ($a_{\|, InGaAs}$) and the lattice constant of GaAs substrate (a_{GaAs}) to the difference between the lattice constant of an unstrained $In_{0.06}Ga_{0.94}As$ (a_{InGaAs}) and a_{GaAs} is 0.90. This means that $a_{\|, InGaAs}$ is very close to a_{InGaAs} and that the $In_{0.06}Ga_{0.94}As$ layer selectively grown on the nanoscale SiO_2-patterned GaAs(001) is almost completely relaxed. The strain relaxation of the $In_{0.06}Ga_{0.94}As$ is very different from a conventional relaxation process, typically associated with the generation of misfit dislocations. Luryi and Suhir proposed a model for strain relief of an epilayer deposited on a lattice-mismatched, nanoscale-patterned substrate with a sample structure similar to ours [Appl. Phys. Lett. 49, 140 (1986)]. Comparison of the experimental results with their model will be presented.

10:40 AM
W7, Epitaxial Lateral Overgrowth of InAs on W Masks: *Lars-Erik M. Wernersson*[1]; Jonas Lembke[1]; Bo Martinsson[1]; Erik Lind[1]; Werner Seifert[1]; [1]Lund University, Solid State Physics, Box 118, Lund S-22100 Sweden

Embedded metal in InAs may be used to reduce the resistance of buried layers, such as the extrinsic base in heterostructure bipolar transistors. We have studied the conditions for epitaxial overgrowth of W patterns in InAs using low pressure MOVPE with trimethylindium and arsine as source materials on InAs (100) wafers. At a growth temperature of 500°C we observed polycrystalline deposition on all W patterns, while at 550°C epitaxial InAs was deposited on small (< 1 µm) patterns and polycrystalline InAs on wider patterns. At 600°C epitaxial lateral overgrowth of InAs was observed on all patterns and the selective growth was studied as a function of the V/III ratio on W ring test structures and wires oriented in different directions. 100 nm wide wires oriented in the [110]-direction was found to effectively block the lateral overgrowth by the formation of mesa ridges limited by {110}B and {111}B planes for V/III ratios between 14 to 56. Wires, oriented in 30° off from the [110]-direction, were completely covered without any void formation and the surface was planarized after 300 nm InAs deposition at the lower V/III ratio. A reduced lateral growth without overgrowth was observed on wires oriented in 45°, 60° and 90° off from the [110]-direction in agreement with the ring structures, where the highest lateral coverage was found in the 30°-direction. This orientation dependence is in agreement with the overgrowth of InP,[1] while the lateral growth of InAs on GaAs substrates has shown the opposite directional dependence.[2] Studies of the overgrowth of W in GaAs have however shown that the lateral growth rate strongly depends on the epitaxial growth conditions.[3] Finally, electrical characterization of overgrown contacts showed no degradation of the specific contact resistance related to the overgrowth procedure. It was estimated to be below 5x10-5 •cm2. A precise evaluation could however not be performed due to the conducting although undoped substrate. The combination of the observed orientation dependence of the formation of mesa structures and the electrical properties of the contacts may be used to design selectively grown InAs emitters placed on W masks on thin base layers. [1]Wernersson, L.-E.; Jarlskog, L.; Lofgren, A.; Nilsson, N.; Samuelson, L.; Seifert, W.; Suhara, M.; Contacting of buried InP-based layers by epitaxial overgrowth over patterned tungsten features Indium Phosphide and Related Materials, 1999. IPRM. 1999 Eleventh International Conference on , 16-20 May 1999, Page(s): 353-356. [2]Suryanarayanan Y., Khandekar A., Keuch T., and Babcock S.; Micorstructure of lateral epitaxial overgrown InAs on (100) GaAs substrates Appl. Phys. Lett. 83, 1977 (2003). [3]L.-E. Wernersson, M. Borgström, B. Gustafson, A. Gustafsson, L. Jarlskog, J.-O. Malm, A. Litwin, L. Samuelson and W. Seifert MOVPE overgrowth of metallic features for realisation of 3D metal-semiconductor quantum devices J. Crystal Growth 221, 704 (2000).

11:00 AM Student
W8, Origin of Multiply-Tilted Grains in Conventional and Lateral Epitaxial Overgrowth of InAs Thin Films on (100) GaAs by MOCVD: *A. A. Khandekar*[1]; G. Suryanarayanan[2]; S. E. Babcock[3]; T. F. Kuech[4]; [1]University of Wisconsin, Dept. of Chem. & Bio. Engrg., 1415 Engrg. Dr., Madison, WI 53706 USA; [2]University of Wisconsin, Matls. Sci. Prog., 1509 Univ. Ave., Madison, WI 53706 USA; [3]University of Wisconsin, Dept. of Matls. Sci. & Engrg. & Matls. Sci. Prog., 1509 Univ. Ave., Madison, WI 53726 USA; [4]University of Wisconsin, Dept. of Chem. & Bio. Engrg. & Matls. Sci. Prog., 1415 Engrg. Dr., Madison, WI 53726 USA

The performance of many InAs-based electronic devices is improved by the use of a semi-insulating (SI) substrate. SI GaAs, having a 7% lattice mismatch is often used for InAs device formation. The strain relaxation and dislocation structure in the initial 3D growth islands determine the overall utility of the InAs films. Lateral epitaxial overgrowth (LEO) has been shown to substantially reduce the dislocation density in InAs films. The effect of growth chemistry and temperature on the defect microstructure in InAs, grown on both planar and LEO GaAs substrates was studied. InAs islands and thin films were deposited via MOCVD using trimethyl indium and arsine. LEO substrates consisted of 0.6, 2, and 5 µm wide, stripe-shaped window openings in the SiO_2 mask, at a 10 µm pitch. The stripes were parallel to the GaAs [01-1] crystallographic direction. The growth temperature and V/III ratio were varied from 500 - 700°C, and 2 - 80, respectively for the planar growth. The LEO was carried out at 700° C and a V/III ratio of 80 to minimize the nucleation on the mask. For the planar growth at high temperature and high V/III ratio, multiple x-ray diffraction peaks separated by 4-7° were observed, indicating presence of misoriented InAs grains, which were confirmed in cross-sectional TEM micrographs. Single, substrate-aligned peaks existed for the films grown at low temperatures or at low V/III ratios. Individual islands grown at high temperature and high V/III ratio were divided into multiply-tilted regions, with 3-7° misorientations with respect to each other and the GaAs, as indicated by the backscattered electron Kikuchi pattern (BEKP) maps. For the LEO InAs films on 2 and 5 µm window opening substrates, multiple peaks, separated by ~2° existed in the rocking curve scans with x-ray beam along [011]. Single

substrate-aligned peak was observed for the orthogonal scan geometry. For the 0.6-µm opening sample, single peaks existed for both the scan geometries. InAs nucleation occurred preferentially, along the mask edges for the 2 and 5 µm windows-openings. InAs islands initially coalesced along the mask edges and then across the entire window opening. Three distinct regions of coalesced islands, along the two mask edges and at the center, were tilted by 1-3° with respect to each other for 2 and 5 µm window openings. For the 0.6 µm window, evenly distributed, small-sized islands coalesce at an early stage to yield singular orientation. Tilt formation in InAs islands was strongly dependent on the island size. Early coalescence of small-sized islands and the modification of the strain relaxation by the growth chemistry were the important factors governing the microstructure and orientation in the LEO InAs films and in achieving defect reduction.

11:20 AM Student

W9, Lateral Growth Behavior of GaSb by Metal Organic Vapor Phase Epitaxy: *Brian E. Hawkins*[1]; Thomas F. Kuech[1]; [1]University of Wisconsin, Dept. of Chem. & Bio. Engrg., 1415 Engineering Dr., Madison, WI 53706 USA

Metal Organic Vapor Phase Epitaxy (MOVPE) GaSb films on semi-insulating GaAs substrates are used in high-speed electronic and long-wavelength optical devices. In the case of large area growth, defects caused by the lattice mismatch (7.8%) degrade the electronic properties of GaSb films. Lateral epitaxial overgrowth techniques can be used to overcome the problem of lattice mismatch leading to a greatly reduced defect density in coalesced films. A fundamental understanding of the lateral growth behavior of GaSb is essential for improving these lateral epitaxial overgrowth techniques. The crystallographically dependent growth rates were determined by measuring the lateral growth rates of the GaSb on the mesas. GaSb substrates were patterned to form mesa structures using standard photolithographic procedures and an HF/Tartaric acid/H2O2/H2O etchant to create circular mesas nominally 100, 75, 50, and 10 µm in diameter with heights of ~ 400 nanometers. GaSb was then grown on the mesa-patterned substrates in a horizontal MOVPE reactor operating at 78 Torr using trimethyl antimony and either trimethyl or triethyl gallium over a range of typically employed growth temperatures and gas phase compositions. Optical microscopy was used to characterize the change in the size and shape of the various mesas. The vertical and lateral growth rates when using trimethyl gallium are characterized by a kinetically limited regime from temperatures of 500-600°C and a mass transport limited regime from temperatures of 600-650°C. At temperatures higher than 600°, the lateral growth rates decrease with increasing temperature. In the mass-transport limited regime, the vertical growth rate was observed to have a linear dependence on the trimethyl gallium partial pressure and a weak dependence on the trimethyl antimony partial pressure. The lateral growth rates in this regime were found to decrease at the extremes of the investigated range of V/III ratios, at V/III > 1.8 or V/III< 1.2. For triethyl gallium grown GaSb, vertical growth rate data exhibited mass-transport limited behavior over the temperature range of 500°C-650°C. The lateral growth rates, however, displayed a single temperature regime over which the lateral growth rates decreased with increasing temperature. Both the lateral and the vertical growth rates increased with a non-linear dependence on both the triethyl gallium and trimethyl antimony partial pressures. For both tiethyl and trimethyl gallium precursors, the lateral growth rate in the [01-1] direction was greater than that in the [0-1-1] direction at lower growth temperatures. A model of the growth behavior is developed combining these surface lateral and vertical growth rates with the specific fluxes of reactants based on the combined gas phase and surface chemistry within a model of the thermal-fluid environment of the reactor. This model is used to describe the LEO growth behavior.

11:40 AM

W10, Room-Temperature Yellow-Amber Emission from InGaP Quantum Wells Grown on an InGaP Metamorphic Buffer Layer on GaP(100) Substrates: *Vladimir A. Odnoblyudov*[1]; Charles W. Tu[1]; [1]University of California, Elect. & Computer Engrg., 9500 Gilman Dr., La Jolla, CA 92093-0407 USA

Solid-state lightning recently has become one of the most exciting subjects of research in the semiconductor technology area. In particular, white light from light-emitting diodes (LEDs) would offer many advantages for general lighting: reduced electrical energy consumption, reduced carbon-related pollution, increased lifetime, and improved human visual experience. Indeed, solid-state lighting through LEDs is considered a disruptive technology,[1] which eventually would replace present incandescent and fluorescent technologies, much like transistors replacing vacuum tubes. The three wavelengths best for tri-color mixing to produce white light are 460, 540, and 610 nm. The first two are produced from AlGaInN LEDs, and the last, 610 nm, from AlGaInP LEDs grown on GaAs substrates. There are several problems with currently used yellow-amber AlGaInP based LED's. The first problem is low quantum efficiency or luminous efficacy in the yellow-amber range due to poor electron confinement. The second problem is complicated and high-cost procedure of removing the light-absorbing GaAs substrate and wafer-bonding a transparent GaP substrate.[2] The third problem is low optical gain due to the use of bulk layers in the active region of LEDs. We propose using a metamorphic InxGa1-xP buffer layer grown directly on GaP(100) substrates. The purpose of a fully relaxed metamorphic buffer layer is to change the lattice constant from that of GaP(100) to a larger lattice constant of InxGa1-xP and use this template as the new substrate for pseudomorphic growth of the desired LED structure. This approach would provide great design flexibility to optimize device performance. Using the proposed approach we have grown samples in order to obtain light emission. The 0.5-micron-thick In0.2GaP metamorphic buffer layer was deposited at substrate temperature of 4000C. On top of the buffer layer an optical structure was grown at 5000C. It consists of a 0.2-micron-thick In0.2Ga0.8P bottom waveguide layer, an 8-nm-thick In0.38Ga0.62P single quantum well, and a 0.2-micron-thick In0.2GaP top waveguide layer. Amber emission with peak wavelength at 610 nm was detected by an electrically cooled Ge photodetector. Thus, a new approach to obtain yellow-amber light emission was successfully realized in this work. Further characterization and investigation to optimize light output are underway. [1]The Promise of Solid State Lighting for General Illumination: Light Emitting Diodes (LEDs) and Organic Light Emitting Diodes (OLEDs) Update 2002, Department of Energy (BTS) and the Optoelectronics Industry Development Association. [2]F.A.Kish et al., Appl. Phys. Lett. 64, 2839(1994).

Session X: Spin Injection, Spin Transport and Magnetic Anisotropy

Thursday PM Room: 102
June 24, 2004 Location: DeBartolo Hall

Session Chairs: Chris J. Palmstrøm, University of Minnesota, Minneapolis, MN 55455 USA; Tomasz Wojtowicz, University of Notre Dame, Notre Dame, IN 46556 USA

1:30 PM

X1, Spin Injection from Fe_3Si into GaAs: *Atsushi Kawaharazuka*[1]; Manfred Ramsteiner[1]; Jens Herfort[1]; Hans-Peter Schönherr[1]; Helmar Kostial[1]; Klaus H. Ploog[1]; [1]Paul-Drude-Institut für Festkörperelektronik, Hausvogteiplatz 5-7, Berlin 10117 Germany

Hybrid structures consisting of a ferromagnetic metal layer on a semiconductor (FM/SC) have been demonstrated to be suitable for room-temperature spin injection. For spin-electronic device applications, it is desirable to establish a FM/SC hybrid system, which exhibits a high thermal stability. In this respect, Fe_3Si, which is ferromagnetic up to 840 K and almost lattice matched to GaAs, is a promising material for spin injection. We report on the electrical spin injection from Fe_3Si into GaAs at room temperature. The light-emitting diode (LED) device with the Fe_3Si injection layer is grown by molecular-beam epitaxy (MBE). After growing the n-i-p $In_{0.1}Ga_{0.9}As$/GaAs structure, the substrate is transferred into the As-free metal deposition chamber through UHV, and then the 35-nm-thick Fe_3Si layer is grown on the n-GaAs layer at the substrate temperature T_G of 200°C. The structural properties of the Fe_3Si layer are characterized by double crystal X-ray diffraction (XRD) measurements. A very narrow XRD peak width and the appearance of distinct interference fringes reveal a high structural perfection as well as abrupt inter-

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faces. Spin injection is investigated in the temperature range between 25 and 295 K by analyzing the magnetic-field dependence of the circular polarization degree of the EL intensity. To eliminate the polarization induced by Zeeman splitting and carrier thermalization, we subtract the polarization obtained from the reference sample without a ferromagnetic injection layer from the one with the Fe_3Si injection layer. The resulting net polarization follows the magnetization curve of Fe_3Si, which is independently obtained by using superconducting-quantum-interference-device (SQUID) magnetometry. These results provide evidence for the successful spin injection from the ferromagnetic metal Fe_3Si into the semiconductor GaAs up to room temperature. The net polarization in the saturation region at 25 K is about 3%, which is comparable to the values previously reported for the injection from Fe and MnAs into similar semiconductor LED structures. However, the saturation value decreases with increasing temperature and reaches about 1% at room temperature. At the same time, the polarization induced by the Zeeman effect shows a remarkable temperature dependence with a minimum contribution around 150 K. Note that the observed temperature dependence of the EL polarization cannot be explained by artifacts due to the magnetic circular dichroism (MCD). Such an MCD effect would indeed be proportional to the magnetization of the ferromagnetic layer. However, the magnetic properties of the Fe_3Si injection layer do not change below room temperature, since the Curie temperature of Fe_3Si is much higher. Instead, we show that the complete temperature dependence can be consistently explained by taking into account the carrier lifetime of the recombining electrons and the spin-relaxation time in the (In,Ga)As quantum well.

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X2, Fabrication and Characterization of an InGaAs Channel Spin Transistor with Fe Electrodes as Spin Injector/Detector: *Kanji Yoh*[1]; Zatur Mufida[1]; Marhoun Ferhat[2]; Alexandru Riposan[3]; Joanna Mirecki Millunchick[3]; [1]Hokkaido University, RCIQE, N13,W8, Kita-ku, Sapporo 060-8628 Japan; [2]Japan Science Technology Agency Japan; [3]University of Michigan, Matls. Sci. & Engrg., Ann Arbor, MI 48109 USA

Spin-injection from ferromagnetic metals into semiconductors is one of the key technologies to achieve spintronics[1] in the future. In spite of its potential importance, there have been keen discussions on whether or not an efficient spin injection into semiconductor is possible at all.[2] We have been demonstrating that high efficiency spin injection is possible without tunneling barriers between ferromagnetic metal electrode and InAs.[3,4,5] The spin transistor structure consists of AlInAs/InGaAs modulation-doped structure grown on InP and strained In0.81Ga0.19As channel layer inserted in InGaAs sub-channel. We have observed current modulation presumably due to spin-orbit interaction in the channel for the first time. The heterostructure was grown by MBE. It consists of AlGaAs In order to make non-alloyed Ohmic contact with Fe, the growth of relatively thick In0.81Ga0.19As channel layer of 80Å was preferred to fabricate the transistor structure together with precise etching control. This was made possible by increasing critical thickness of strained In0.81Ga0.19As channel layer by appropriate growth condition.[6] The crystal quality bcc Fe thin film[7] was grown on In0.81Ga0.19As channel layer in a ultra-high-vacuum with e-beam evaporator. The growth rate of Fe film was set to approximately 1 mono-layer per minute and the growth temperature was 23°C to minimize inter-diffusion between Fe and InGaAs. No temperature treatment was done to cure the materials. By doing so, fairly high spin injection efficiency is expected to be achieved based on polarization properties of electro-luminescence measurements.[3,4,5] The non-ferromanetic metals were deposited on top of Fe and lifted-off. The gate metal was deposited after gate recess etching. Decent Ohmic and pinch-off characteristics were obtained in the FET performance. The overall performance was 60mS/mm in 2µm gate device. When the Fe electrodes were magnetized in parallel to the current, peculiar current voltage characteristics were obtained. The current was seen to oscillate as a function of gate voltage. The oscillation amplitude in general was approximately 1% in magnitude, but in certain conditions of gate and drain voltage, the modulation increased up to 10% to 30%. We believe that this is the first demonstration of spin transistor operation with the gate voltage control of spin-orbit interaction of electrons in the channel. [1]S.Datta and B.Das; Appl.Phys.Lett. 56 (1990) 665. [2]G.Schmidt et al, Phys.Rev.B 62, R4790 (2000). [3]H.Ohno, Kanji Yoh et al, Jpn.J.Appl.Phys. Express Lett. Vol.42 pp.L1-L3 (2003). [4]Kanji Yoh et al, J.Crystal Growth 251, pp.337-341 (2003). [5]Kanji Yoh et al, Semi.Sci.Technol. in Press (2004). [6]J.M.Millunchick, personal correspondence. [7]H.Ohno et al, J.Vac.Sci.& Technol.B 19 (2000) 2280.

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X3, Point Contact Spin Spectroscopy of Ferromagnetic MnAs and GaMnAs Epitaxial Films: *B. Nadgorny*[1]; R. P. Panguluri[1]; K. C. Ku[2]; S. H. Chun[2]; N. Samarth[2]; I. I. Mazin[3]; [1]Wayne State University, Physics, 666 W. Hancock, Detroit, MI 48201 USA; [2]Pennsylvania State University, Physics & Matls. Rsch. Inst., Univ. Park, PA 16802 USA; [3]Naval Research Laboratory, Ctr. for Computational Matls. Sci., Washington, DC USA

We have used point contact Andreev reflection spin spectroscopy[1] to directly measure the spin polarization in the MBE-grown epilayers of ferromagnetic semiconductor MnAs and dilute ferromagnetic semiconductor (Ga,Mn)As. A ballistic transport spin polarization of approximately 49% and 44% is obtained for the type A and type B orientations of MnAs, respectively.[2] These measurements are consistent with our density functional calculations in MnAs, and with recent observations of a large tunnel magnetoresistance in MnAs/AlAs/(Ga,Mn)As tunnel junctions.[3] We have also explored the feasibility of using Andreev Reflection Spin Spectroscopy in the point contact geometry to determine the spin polarization in dilute magnetic semiconductor, (Ga,Mn)As with the Curie temperature ~ 140 K. The applicability of the PCAR technique to a dilute magnetic semiconductor, such as (GaMn)As is justified by our recent study of its non-magnetic analog, highly-doped (p=8x1020) GaBeAs,[4] in which we found that conductance spectra of Sn/GaBeAs contacts are consistent with the conventional theoretical description of Andreev reflection in metals and that the Schottky barriers at the interface with the semiconductors are negligible.[4] In (GaMn)As, on the other hand, a reduction of the superconducting gap, accompanied by thermal broadening of the spectra was observed, possibly due to magnetic disorder at the interface. After taking these unconventional effects into account in the data analysis, we found (GaMn)As to be highly spin polarized, with the spin polarization in the range of 75-95%. [1]R.J. Soulen, et al., Science 282, 85 (1998); S.K. Upadhyay, et al., Phys. Rev. Lett. 81, 3247 (1998). [2]R. P. Panguluri, et al, Phys. Rev. B 68, 201307(R) (2003). [3]S. H. Chun, et al, Phys. Rev. B 66, 100408 (2002). [4]R.P. Panguluri et al, submitted to Phys. Rev. Lett.

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X4, Magnetic Properties of MnAs/GaAs(001) at the Structural Phase Transition: *A. Ney*[1]; T. Hesjedal[2]; C. Pampuch[2]; A. K. Das[2]; L. Daweritz[2]; T. Tolinski[3]; J. Lindner[3]; K. Lenz[3]; K. Baberschke[3]; R. Koch[2]; K. H. Ploog[2]; [1]Stanford University, Solid State & Photonics Lab., CIS-X 310, Stanford, CA 94305 USA; [2]Paul-Drude-Institute for Solid State Electronics, Hausvogteiplatz 5-7, Berlin D-10117 Germany; [3]Freie Universitat Berlin, Inst. fur Experimentalphysik, Arnimallee 14, Berlin D-14195 Germany

MnAs is one of the promising ferromagnetic metals for which spin injection into semiconductors had been demonstrated.[1] It can be grown on the two leading semiconductor substrates Si and GaAs forming high quality interfaces. The major drawback concerning applications is the coupled structural and magnetic phase transition at about 40°C. In the bulk, the ferromagnetic, hexagonal α-MnAs abruptly transforms into the paramagnetic, orthorhombic β-MnAs. In heteroepitaxially constrained MnAs/GaAs(001) films, the two phases coexist from 10 to 40°C and the magnetization steadily decreases with temperature. We present detailed magnetic measurements on MnAs/GaAs(001) in the phase transition region covering the α-, the β-phase and the α+β coexistence region. The coexistence of two magnetically distinguishable types of α-MnAs around the onset of the coexistence region at 10°C, the occurrence of metastable magnetic properties, and the absence of a Curie-Weiss peak in the susceptibility indicates that the magnetic phase transition in thin films is of first order as well. The two types of α-MnAs are characterized by different coercivity and magnetic anisotropy, the latter due to a change in shape anisotropy of the striped phase. The broad coexistence region is explained by a continuosly varying strain state of the MnAs film. Furthermore, the previously measured change in stress[2] can be calibrated to absolute values via the onset of the phase transformation. The fact, that the phase transition is of first order, suggests the possibility to shift the loss of ferromagnetic order towards higher temperatures, e. g., by changing the epitaxial constraints of the film. Indeed, recent experiments on MnAs/GaAs(111) show that the ferromagnetic order is maintained even above 60°C.[3] [1]M. Ramsteiner et al., Phys. Rev. B 66, 081304(R) (2002).

[2]A. K. Das et al., Phys. Rev. Lett. 91, 087203(2003). [3]B. Jenichen et al., Phys. Rev. B 68, 132301 (2003).

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X5, Ferromagnet/DMS Hybrid Structures: Low-Dimensional Magnetic Traps: *P. Redlinski*[1]; T. Wojtowicz[1]; T. Rappoport[1]; A. Libal[1]; J. K. Furdyna[1]; B. Janko[1]; [1]University of Notre Dame, Physics, 225 Nieuwland Sci. Hall, Notre Dame, IN 46556 USA

Recently there is an increasing interest in using spin of particles, instead of their charge, as a basis for the operation of a new type of electronic devices. In this work we perform detailed theoretical calculations to show that the spin degrees of freedom can be utilized for achieving a strong spatial localization - of interest for "spintronic applications" - for both charged quasiparticles (electrons, trions) as well as of neutral complexes (excitons). We show that in each of these cases the localization leads to a sizable quantization of electronic states. In particular, we show, that a strong force, as high as 10^9 meV/m can be exerted on an exciton by the magnetic field of a nanomagnet placed 10 nm above diluted magnetic semiconductor (DMS) quantum well (QW). We argue that such strong localization is made possible by the giant effective magnetic moment of the exciton in such a material, which, in turn is related to the gigantic effective g-factor of band electrons in DMSs. We have considered CdMnTe/CdMgTe QW buried at nanometers distances below two relevant nanomagnetic Fe islands: of either rectangular[1] or cylindrical[2] geometry. Magnetic field profiles were calculated by solving magnetostatic equations with magnetization distribution determined from micromagnetic theoretical simulations. The energy spectra in the conduction band as well as in the valence band were calculated by approximating the Schrodinger differential equation with a finite difference algebraic eigen-equation. The valence band electrons were modeled by Luttinger Hamiltonian leading to inclusion of mixing between heavy- and light-holes which cause anisotropic spin-splitting of valence energy levels in DMS QW in the presence of an external magnetic field. In the case of rectangular nanomagnet the combination of confinement due to the QW barriers and due to local field in x- and y-directions produce spin-polarized one dimensional structures with the confinement energy of the order of few meV at sub Kelvin temperatures. For nanodisks, where vortex states of magnetization are formed,[2] quasi zero dimensional spin-polarized structures are formed with confinement energy as high as tens of meV. In addition to confinement energies we have also calculated the probabilities of interband optical transitions for both types of nanomagnets. [1]J. Kossut, et. al, Appl. Phys. Lett., 79, 1789, 2001. [2]M. Berciu, B. Janko; Phys. Rev. Lett., 90, 246804, 2003.

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X6, Spin-Polarized Ballistic Transport in InSb/InAlSb Heterostructures: *Hong Chen*[1]; J. A. Peters[1]; J. J. Heremans[1]; N. Goel[2]; S. J. Chung[2]; M. B. Santos[2]; [1]Ohio University, Dept. of Physics & Astron., & The Nanoscale & Quantum Phenomena Inst., Clippinger Labs., Athens, OH 45701 USA; [2]University of Oklahoma, Dept. of Physics & Astron., & Ctr. for Semiconductor Physics in Nanostruct., Norman, OK 73019 USA

Much of the effort in semiconductor spin-electronics is motivated by the promise of new devices that exploit spin-polarized currents, such as the spin transistor. Interesting electron properties (small mass, strong spin-orbit coupling) make InSb quantum wells attractive for transport-based spintronic devices. We describe and experimentally demonstrate a method to create spin-polarized ballistic electrons through spin-orbit coupling in a two-dimensional electron system in an InSb/InAlSb heterostructure. Reflection of a spin-unpolarized injected beam from a lithographic barrier creates two fully spin-polarized side beams, in addition to an unpolarized specularly reflected beam because the strong spin-orbit coupling in InSb quantum wells leads to different reflection angles for different spin polarizations. We present experimental results verifying the realization of the method. To further demonstrate ballistic electron transport in InSb/InAlSb heterostructure mesoscopic devices, we fabricated anti-dot lattices and measured their magnetotransport properties. Strong features characteristic of ballistic transport were observed at temperatures up to 50 K, beyond which the strictly two-dimensional character of the electron system faded. The temperature dependencies of the magnetoresistance peaks reveal a scattering time particular to anti-dot lattices, with a linear dependence on temperature in the range 0.4 K to 50 K. The small effective mass in the InSb quantum well, however, allows observation of ballistic transport features up to high temperatures. Typically, metals deposited directly on the narrow gap InSb/InAlSb heterostructures do not lead to reliable Schottky barriers, leading to large gate leakage currents. We successfully used an organic dielectric layer between the heterostructure and the Al front gate. The front gate was used to vary the density in the quantum well. Mobility and density were measured on Hall bars from room temperature to 0.4 K (zero gate voltage room temperature mobility and density were found to be 4.8x10^4 cm^2/Vs and 3.1x10^11 cm^-2 respectively, while at T = 1.5 K the values are 1.5x10^5 cm^2/Vs and 2.4x10^11 cm^-2). From the data, we characterize the scattering mechanisms over temperature. The range over which the density could be varied by means of a front gate was experimentally observed to be limited in the as-grown heterostructures. Our Poisson-Schroedinger simulations show that a saturation in electron density occurs due to charge accumulation in the heterostructure, and concomitant screening of the gate electric field. Elucidation of the saturation points to growth sequences to alleviate the density limitation, yielding higher carrier densities in the well. In conclusion, we will present a set of measurements on InSb/InAlSb heterostructures, illustrating this material's usefulness in spintronics. We present ballistic spin-polarized transport due to large spin-orbit coupling in InSb quantum wells, demonstrate ballistic transport up to high temperatures in anti-dot lattices, and analyze the effect of a front gate on the transport properties (supported by NSF-DMR).

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X7, Magnetotransport Studies of Magnetic Anisotropy in Strain-Engineered InMnAs Ferromagnetic Layers: *W. L. Lim*[1]; X. Liu[1]; Z. Ge[1]; S. Shen[1]; T. Wojtowicz[2]; J. K. Furdyna[1]; M. Dobrowolska[1]; [1]University of Notre Dame, Dept. of Physics, 225 Nieuwland Sci. Hall, Notre Dame, IN 46556 USA; [2]Polish Academy of Sciences, Inst. of Physics, 02-668 Warsaw Poland

Ferromagnetic $In_{1-x}Mn_xAs$ semiconductor alloys (x < 0.08) with thickness of 20 nm were fabricated by low-temperature molecular beam epitaxy either on $In_{1-y}Al_yAs$ or on (Ga,Al)Sb buffers grown on (001)- oriented GaAs substrates. The ferromagnetic order in InMnAs with T_C up to 50K is clearly demonstrated by the SQUID and magnetotransport measurements. In particular, strain engineering in InMnAs (i.e., build-in compressive strain from InAlAs buffer, or tensile strain from (Ga,Al)Sb buffer) leads to the observation of an in-plane easy axis of magnetization for InMnAs/InAlAs (along the [110] direction), and of out-of-plane easy axis (along the [001] direction) for InMnAs/(Ga,Al)Sb - as revealed by square hysteresis loops observed via SQUID when applied magnetic field is along the easy direction. Magnetotransport measurements show negative magnetoresistance and strong anormalous Hall effect (AHE) in both types of samples. Square hysteresis loops in AHE were observed in InMnAs/(Ga,Al)Sb samples but not in InMnAs/InAlAs samples. This confirms the SQUID results indicating that the easy axis of magnetization for InMnAs/(Ga,Al)Sb is out of the layer plane while the easy axis of magnetization in InMnAs/InAlAs is in the layer plane. Transport studies in the presence of an in-plane magnetic field of the Planar Hall Effect (PHE) were carried out on the InMnAs/InAlAs samples with the Hall bar patterns fabricated along three orientations [110], [1-10] and [100]. Various widths of the Hall bar patterns were also fabricated. The Planar Hall effect in InMnAs/InAlAs samples is observed to be smaller than that observed in GaMnAs films with similar physical dimensions. Furthermore, for InMnAs samples with millimeters sizes we have not observed any clear features related to the domain switching, suggesting that the sizes of the domains are smaller in InMnAs/InAlAs than in the GaMnAs. In addition, PHE measurements carried out on the InMnAs/InAlAs system show the existence of a uniaxial anisotropy in the layer plane similar to that observed in GaMnAs system, suggesting that the difference between [110] and [1-10] directions is universal in III-Mn-As system. It is interesting that in the InMnAs system we observe a cubic anisotropy that is different than in GaMnAs - the easy axis in InMnAs films is in the [110] direction, instead of the [100] direction observed in the GaMnAs layers. With successful strain engineering described above, InMnAs has become a viable candidate for implementing giant-PHE and nano-constricted giant magnetoresistance devices. This work is supported by grants from DARPA SPINS program.

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X8, Magneto-Optical Studies of the Magnetic Anisotropy in III-Mn-As Ferromagnetic Semiconductors: *M. Kutrowski*[1]; L. Titova[1]; K. J. Yee[1]; W. L. Lim[1]; X. Liu[1]; T. Wojtowicz[1]; J. K. Furdyna[1]; M. Dobrowolska[1]; [1]University of Notre Dame, Physics, 225 Nieuwland Sci. Hall, Notre Dame, IN 46556 USA

Magneto-optical Kerr effect (MOKE) and magnetic circular dichroism (MCD) are used to investigate the temperature induced changes in magnetic anisotropy in ferromagnetic GaMnAs and InMnAs layers grown by MBE. Temperature-reorientation of the easy axis of magnetization (EAM) from out-of-plane to in-plane has been reported by others for GaMnAs layers under compressive strain,[1,2] while the tensile strain case was not investigated. To examine the latter, the 150nm $Ga_{1-x}Mn_xAs$ layers (0.02 < x < 0.07) has been deposited on ZnSe buffers grown on GaAs [001] substrates, which results in either tensile (for x < 0.04) or compressive (for x > 0.04) strain due to the lattice mismatch between GaMnAs and ZnSe. At low x (x ~ 0.02) the EAM is found to point along the [001] (out of plane) direction up to T_C, as manifested by a square hysteresis observed by MOKE. However, when GaAs substrate is removed by etching, both MOKE and MCD show strongly tilted low temperature (T) hysteresis curves, indicating a large in-plane component of the EAM, which we ascribe to partial strain release by substrate removal. As the T is increased, the square shape of the hysteresis curve is gradually restored. At higher x (x ~ 0.07), when GaMnAs layers are strained compressively, no EAM changes are observed with increasing T. $In_{1-x}Mn_xAs$ layers also exhibit unusual behavior of the EAM. We examined two groups of InMnAs samples, one with x ~ 0.05 and one with x ~ 0.07, thus expected to have different concentration of defects and holes. This has led to strikingly different behaviors. The first group reveals a predominantly in-plane EAM at low T, and fast EAM re-orientation to the out-of-plane direction with increasing T. In the second group we observe an out-of-plane orientation of the EAM, which does not change with T. Possible causes of the observed behavior in both materials are discussed in terms of competition between the uniaxial and cubic anisotropy which have different temperature and carrier concentration dependences. [1]M. Sawicki et al., J. of Supercon. 16, 7 (2003). [2]H. Ohno, J. Crystal Growth 251, 285 (2003).

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X9, Magneto-Optical Activity of InMnAs Epitaxial Films at Room Temperature: *Philip T. Chiu*[1]; *Steven J. May*[1]; Bruce W. Wessels[1]; [1]Northwestern University, Matls. Sci. & Engrg., 2220 Campus Dr., Cook Hall, Evanston, IL 60208 USA

InMnAs is a ferromagnetic semiconductor that shows considerable promise for spintronic applications. Recently our group has shown that this semiconductor when prepared by MOVPE has a Curie temperature of 330 K. Preliminary magnetic measurements have been performed on single-phase films that support this finding. For spintronic applications including spin injectors and tunnel junctions, a better understanding of its magnetic properties and specifically the in-plane anisotropy of InMnAs is required. To this end, the magneto-optic Kerr effect (MOKE) for heteroepitaxial InMnAs on GaAs and InAs substrates was investigated. MOKE magnetometry measurements were taken in the longitudinal configuration and yielded square hysteresis loops at room temperature for all films studied. The magnitude of the coercive field ranged from 340 to 470 Gauss. The saturation Kerr rotation varied linearly from 0.29 to 1.1 mdeg with respect to the manganese concentration, in good agreement with the previously measured dependence of SQUID magnetization on concentration. The shape of the MOKE hysteresis loops was invariant with respect to the in-plane direction of the applied magnetic field for heteroepitaxial InMnAs grown on GaAs substrates. However, InMnAs films grown on InAs exhibit a two-fold in-plane magnetic anisotropy, with the easy axis of magnetization along the [1 1 0] direction. The observed magnetic anisotropy is attributed to coherency strains. This work provides the first evidence of room temperature magneto-optical activity due to ferromagnetism in a ferromagnetic compound semiconductor.

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X10, Magnetic Circular Dichroism in GaMnAs/ZnSe Hybrid Structures with Be Co-Doping: *Raja Chakarvorty*[1]; K. J. Yee[1]; X. Liu[1]; P. Redlinski[1]; Z. Ge[1]; S. Shen[1]; M. Kutrowski[2]; L. Titova[1]; T. Wojtowicz[2]; J. K. Furdyna[1]; B. Janko[1]; M. Dobrowolska[1]; [1]University of Notre Dame, Notre Dame, IN USA; [2]University of Notre Dame, Notre Dame, IN, USA & Polish Academy of Sciences, Inst. of Physics, Warsaw Poland

Magnetic circular dichroism (MCD) in ferromagnetic semiconductors - through its dependence on exchange interaction between carrier spins and magnetic moments within the medium - holds promise of providing important physical insights into spin-based processes that are responsible for the unique properties of ferromagnetic semiconductors generally. In this study we investigate MCD in a series of magnetic epitaxial $Ga_{0.98}Mn_{0.02}As$:Be layers grown on hybrid ZnSe/GaAs substrates, with various Be co-doping. The growth of GaMnAs:Be on ZnSe buffers circumvents the difficulty commonly encountered in optical studies of GaMnAs layers grown directly on GaAs, since ZnSe is an excellent etch-stop, thus allows removal of the GaAs layer for transmission experiments. In addition, by controlling the temperature of Be cell, one can change the hole concentration, which plays a very important role in ferromagnetism in GaMnAs. We performed systematic optical absorption measurements on our samples in the range from 450 to 1100nm as a function of temperature (from 1.5 to 300K) in magnetic fields up to 6 Tesla. We used circular polarization combined with photo-modulation to demonstrate the presence of clear MCD response in a series of GaMnAs:Be samples. The magnitude and the spectral form of the MCD showed a progressive change as the hole concentration increases. Moreover, the study on GaMnAs with Si co-doping is also carried out to investigate the effect of the reduction of hole concentration. The observed magnetic field and temperature dependence of the MCD data cannot be fully explained by the model proposed by Szczytko et al.,[1] which includes the effects of the disorder and Moss-Burstein shift. To interpret our data, it was further necessary to modify this model by introducing the k-dependence of the exchange integral β. Our results clearly point towards the presence of intricate spin and exchange correlations in the valence band, as reflected by the complex structure of the exchange interaction. This work is supported by grants from DARPA SPINS program. [1]J. Szczytko et al., Phys. Rev. B 64, 75306 (2001).

Session Y: Nanotubes & Nanowires II

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June 24, 2004 Location: DeBartolo Hall

Session Chairs: Zhou Chongwu, University of Southern California, Dept. of Electophysics, Los Angeles, CA USA; Kazuhiko Matsumoto, Osaka University, Inst. of Scientific & Industrial Rsch., Ibaraki, Osaka 565-0871 Japan

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Y1, P Type Semiconductive Carbon Nanotube for Quantum Wire: *Takafumi Kamimura*[1]; Chan-Kyeong Hyon[2]; Atsuhiko Kojima[2]; Masatoshi Maeda[3]; Kazuhiko Matsumoto[1]; [1]Osaka University, Grad. Sch. of Engrg. Sci., 8-1, Mihogaoka, Ibaraki-shi, Osaka 567-0047 Japan; [2]CREST/JST, 1-1-1, Umezono, Tsukuba, Ibaraki 305-8568 Japan; [3]University of Tsukuba, Grad. Sch. of Pure & Applied Scis., 1-1-1, Tennoudai, Tsukuba, Ibaraki 305-8571 Japan

We here succeeded in observing the coexistence of the Coulomb charging effect and the resonant tunneling ballistic transport of the holes in the CNT of the length of 4.5μm at 8.6K. The sample was prepared as follows. A p-type silicon wafer with a thermally grown oxide (200nm) is used as a substrate. The layered catalysts of Fe/Mo/Si (3/10/10nm) are patterned on the substrate using the conventional photo-lithography process. The distance between two catalysts for the source and drain was 4.5μm. Single-walled CNT is grown between two catalysts by chemical vapor deposition using mixed gas with ethanol, hydrogen and argon. Finally, Pt/Au electrodes are deposited on the patterned catalysts for the source and drain and the back side of Si substrate for the gate. Thus, back gate type CNT field effect transistor was fabricated. In the drain current-gate bias characteristics at 8.6K, the periodic current peaks are observed, suggesting the Coulomb oscillation peaks. The period of the Coulomb oscillation peaks is 150mV, from which the gate capacitance is estimated

to be 10.7aF. The origin of the Coulomb charging effect is considered to be the carrier confinement in a single island because of the high periodicity of the Coulomb oscillation peaks. The heights of Coulomb oscillation peaks decrease with increase of the gate voltage, indicating that the measured CNT has the p type semiconductive property. Hence the Coulomb charging effect occurs by the holes confinement in the CNT. In the drain current-drain bias characteristics at 8.6K, a Coulomb gap of 7.0mV is ovserved around zero bias voltage. The total device capacitance and the Coulomb charging energy are estimated to be 25.8 aF and 3.1meV, respectively. From the Coulomb charging energy, the length of the island Lisland is estimated to be 4.0µm, which is in good agreement with the length of the CNT at the channel. Hence the Coulomb charging effects are occurred by the hole confinement in the whole channel of the CNT. The outside of the Coulomb gap for higher drain voltages, the current increases with steps. The width of the drain current step ΔV_D is 0.4meV. The spacing of the discrete quantum energy levels ΔE_Q in the CNT with the length of 4.5µm is estimated to be 0.37meV, which is in good agreement with ΔV_D. Therefore, the step like drain current is attributed to the resonant tunneling of hole through the quantum confinement discrete energy levels of CNT. Surprisingly, quantum confinement discrete energy levels for hole was formed through such a long distance of 4.5µm in p type semiconductive CNT. This fact suggests the existence of the ballistic transport of the holes in the semiconductive CNT, and its phase coherent length extends over a distance of at least 4.5µm. We first succeeded in observing coexistence of the Coulomb charging effect and the ballistic transport of the holes in semiconductive CNT.

1:50 PM Student

Y2, Transient Photobleaching in Isolated Single-Walled Carbon Nanotubes: *Michael S. Arnold*[1]; Song Lan[2]; Jay E. Sharping[2]; Samuel I. Stupp[1]; Prem Kumar[2]; Mark C. Hersam[1]; [1]Northwestern University, Matls. Sci. & Engrg., 2220 Campus Dr., Evanston, IL 60208-3108 USA; [2]Northwestern University, Elect. & Computer Engrg., 2145 Sheridan Rd., Evanston, IL 60208-3118 USA

Transient photobleaching at the band gap of semiconducting, isolated single-walled carbon nanotubes (SWNTs) has been observed in response to optical excitation at the second van Hove optical transition. The photobleaching is characterized by a non-degenerate pump-probe technique, and the dependence of the photobleaching intensity on pump and probe intensity, wavelength, and relative polarization is studied. Spectrally, the photobleaching is maximized for pump wavelengths at the second van Hove transition and for probe wavelengths slightly red-shifted (6 meV) from absorption at the first van Hove transition. For pump intensities greater than 1 kW cm-2, a saturation of the measured integrated photobleaching intensity is observed suggesting increased multi-particle non-radiative recombination for large excited particle densities or a saturation of a finite number of states. For probe intensities greater than 500 W cm-2, a saturation of the measured integrated photobleaching intensity is observed and fit to a simple probe saturation model. The photobleaching intensity is roughly twice as large for co-polarized compared with cross-polarized pump and probe beams. Larger extinction is not observed for the cross-polarized case due to either non-straight nanotubes or because of non-zero optical absorption and emission for polarizations orthogonal to the nanotube axis. In additional experimentation, the temporal decay of the optically excited state is probed using a time-resolved, degenerate pump-probe technique. It is observed that both fast (~1 ps) and slow (~100 ps) processes are important. Lastly, since the dielectric constant of the environment external to a SWNT is expected to affect electron-electron and electron-hole interactions and the optical properties of SWNTs, data is presented for both surfactant-isolated and DNA-wrapped SWNTs in both methanol and heavy water. Increasing red-shift of both absorption and photobleaching is observed for increasing external static dielectric constant, thus suggesting a method for tuning the spectral characteristics of future carbon nanotube based electro-optical devices.

2:10 PM Student

Y3, Control of Electrical Property of Carbon Nanotube by Oxygen Ion Implantation with Ultra-Low Energy of 25eV: Takushi Kawai[1]; Kazuhiro Yamamoto[2]; Takafumi Kamimura[3]; Chan-Kyeong Hyon[4]; Atsuhiko Kojima[4]; Kousuke Kurachi[5]; Masatoshi Maeda[6]; Masashi Torigoe[1]; Toshio Nemoto[7]; *Kazuhiko Matsumoto*[8]; [1]Meiji University, Sch. of Sci. & Tech., 1-1-1 Higashimita, Tama, Kawasaki, Kanagawa 214-8571 Japan; [2]National Institute of Advanced Industrial Science and Technology, Rsch. Ctr. for Advd. Carbon Matls., 1-1-1, Umezono, Tsukuba, Ibaraki 305-8568 Japan; [3]Osaka University, Grad. Sch. of Engrg. Sci., 8-1, Mihogaoka, Ibaraki, Osaka 567-0047 Japan; [4]CREST/JST; [5]Meiji University, Grad. Sch. of Sci. & Tech., 1-1-1 Higashimia, Tama, Kawasaki, Kanagawa 214-8571 Japan; [6]University of Tsukuba, Grad. Sch. of Pure & Applied Sci., 1-1-1, Tennnoudai, Tsukuba, Ibaraki 305-8577 Japan; [7]Meiji University, 1-1-1 Higashimita, Tama, Kawasaki, Kanagawa 214-8571 Japan; [8]Osaka University, ISIR, 8-1, Mihogaoka, Ibaraki, Osaka 567-0047 Japan

We have succeeded in converting the electrical property of carbon nanotube (CNT) from p-type to n-type by the Oxygen ion (O^+) implantation with ultra-low energy of 25eV. Conventional CNTs shows the unipolar p-type characteristics. Experiments so far have shown that p-type to n-type conversion of the carbon nanotube can be made by doping the surface of the tube by evaporating alkali metals. We approached the p-type to n- type conversion by O^+ ion implantation. For the high acceleration energy, it only induced defects and couldn't acquire the doping characteristic. In this experiment, we used the ultra low ion implantation system, which only has acceleration energy of 25eV. The sample was prepared as follows. A p-type silicon wafer with a thermally grown oxide (100 nm) was used as a substrate. The layered catalysts of Si/Mo/Fe (10/10/3 nm) were patterned on the substrate using the conventional photo-lithography process. The distance between catalysts for the drain and source was 4µm, where single-walled CNT was grown by thermal chemical vapor deposition (CVD) using Ar-bubbled alcohol gas. After the growth of CNT, Pt/Au (30/200 nm) electrodes were deposited on the patterned catalysts and on the back side of the Si substrate. Thus, a back gate type CNT-FET structure was fabricated. The fabricated sample was then implanted by the O^+ ion at room temperature with the acceleration energy of 25eV, and the amount of doses are 1.75×10^{11} ions/cm^2, 1.36×10^{12} ions/cm^2, 2.49×10^{12} ions/cm^2, 8.18×10^{12} ions/cm^2, respectively. The drain current-gate bias characteristic was measured in vacuum at room temperature before and after the implantation. Before O^+ implantation, the drain current decreases monotonically by the increase of the gate bias from -20V to 0V and shows the lowest value at aroud 0V. This is the well-known p-type characteristics of the CNT. Therefore, the carrier is hole. At the positive gate bias for electron conduction, the drain current increases slightly, but the amount of the current is two to four orders of magnitudes lower than that of at negative bias. After the O^+ ion implantation, as the dose amount increases, the drain current at positive gate bias region for electron conduction increased drastically more than one order of magnitude while at negative gate bias region for hole conduction decreased. Furthermore, the threshold voltage of the electron conduction had shifted to the negative bias direction. These experimental results indicate the increase of the electron transport and the decrease of the hole transport in the CNT by the O^+ ion implantation. Therefore, the electrical property of the CNT started to convert from p-type to n-type by the O^+ ion implantation. The possibility considerable for this change may be that the irradiated O^+ ions displaced with the carbon atoms in the CNT as a dopant, lead the CNT convert p-type to n-type. We have succeeded in converting the electrical property of CNT from p-type to n-type by the O^+ ion implantation with ultra-low energy of 25eV.

2:30 PM Cancelled

Y4, Simulations of Electronic Transport in Single-Wall and Multi-Wall Carbon Nanotubes: *Alexandre Mayer*[1]; [1]Facultés Universitaires Notre-Dame de la Paix, Lab. de Physique du Solide, Rue de Bruxelles, 61, Namur 5000 Belgium

We present simulations of electronic transport in single-wall and multi-wall carbon nanotubes, which are placed between two metallic contacts. We consider situations where the electrons first encounter a singe-wall nanotube (corresponding to either the inner or the outer shell of the (10,10)\@(15,15)\@(20,20) and (10,10)\@(20,10)\@(20,20) nanotubes), before encountering the multi-wall structures. The role of this two-step procedure is to enforce the electrons to enter a single shell of the multi-wall nanotubes, and we study how from that point they get redistributed amongst the other tubes. Because of reflections at the metallic contacts, the conductance of finite armchair nanotubes is found to depend on the length of the tubes, with values that alternate between three separate functions. Regarding the transport in multi-wall nanotubes, it is found that the electrons keep essentially propagating in the shell in which they are initially injected, with transfers to the other tubes hardly exceeding

one percent of the whole current even when micron-long distances are considered. In the case where the three tubes are conducting, these transfers are already completed after four nanometers. The conductance and repartition of the current present then oscillations, which are traced to the band structure of the nanotube. The transfers between the layers and the amplitude of these oscillations are significantly reduced when the intermediate tube is semiconducting.

2:50 PM Y5, Late News

3:10 PM Break

3:30 PM Student

Y6, Quantum Confinement Observed in Ultrafine ZnO and ZnO/ZnMgO Coaxial Nanorod Heterostructures: *Won Il Park*[1]; Gyu-Chul Yi[1]; Miyoung Kim[2]; [1]Pohang University of Science and Technology (POSTECH), Dept. of Matls. Sci. & Engrg., San 31, Hyoja-dong, Namgu, Pohang, Kyungbuk 790-784 Korea; [2]Samsung Advanced Institute of Technology (SAIT), PO Box 111, Suwon 440-600 Korea

One-dimensional semiconductor nanorod heterostructures are potentially ideal functional components for nanometer-scale electronics and optoelectronics, due to their high aspect ratio offering easy manipulation for nanodevice fabrications. Heteroepitaxial nanorod quantum structures greatly increase the versatility and power of these building blocks. We already reported fabrication of ZnO/ZnMgO nanorod quantum well structures with composition modulation along the axial direction. These axial nanorod quantum structures exhibited a blue-shift in the bandedge photoluminescence (PL) peak due to a quantum confinement effect in ultrathin ZnO well layers between ZnMgO barrier layers. The quantum confinement effect along the radial direction was negligible in these nanorod heterostructures, because of the thick diameter (35 nm) of ZnO nanorods. Despite significant progress in nanorod quantum structures, meanwhile, coaxial nanorod quantum structures have rarely been reported. As for oxide nanorods, in particular, no quantum confinement effect in the radial direction was observed due to nanorod diameters thicker than 20 nm and heavy effective masses of electrons and holes. Hence, ultrafine ZnO nanorods with diameters less than 10 nm must be employed as a core material in their coaxial nanorod heterostructures. Here, we report on synthesis of ultrafine ZnO nanorods and $Zn_{0.8}Mg_{0.2}O$ coaxial nanorod heterostructures that exhibit quantum confinement effect. Employing catalyst-free metalorganic vapor-phase epitaxy, ultrafine ZnO nanorods with very thin diameter below 10 nm were prepared and subsequently coaxial nanorod heterostructures were fabricated by epitaxial growth of $Zn_{0.8}Mg_{0.2}O$ layers on the whole surfaces of the ZnO nanorods. From PL spectra of ultrafine ZnO nanorods, a systematic blue-shift in their PL peak position with decreasing their diameter was observed, which is mainly due to the quantum confinement effect along the radial direction in ZnO nanorods. Furthermore, the $Zn_{0.8}Mg_{0.2}O$ coaxial nanorod heterostructures exhibited significantly increased PL intensity and much reduced thermal quenching. Our controlled growth of ultrafine ZnO and $ZnO/Zn_{1-x}Mg_xO$ coaxial nanorod heterostructures opens up significant opportunities for fabrication of oxide-based quantum device structures with radial composition modulation.

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Y7, Rational Growth of Branched and Hyper-Branched Nanowire Structures: *Deli Wang*[1]; Fang Qian[1]; Chen Yang[1]; Zhaohui Zhong[1]; Charles M. Lieber[1]; [1]Harvard University, Chmst. & Chem. Bio. Dept., 12 Oxford St., Cambridge, MA 02138 USA

Branched and hyper-branched nanowire structures were synthesized via a multi-step nanocluster-catalyzed vapor-liquid-solid approach. Scanning electron microscopy studies of silicon nanowire structures prepared in this way confirmed the formation of branched nanostructures, and showed that branch density could be controlled by the nanocluster catalyst concentration. This same approach was also used to grow branched gallium nitride nanowires. High-resolution transmission electron microscopy studies of the branched silicon nanowire structures revealed that the branches grew epitaxially as single-crystal nanowires from the silicon nanowire backbone. In addition, hyper-branched silicon nanowire structures were prepared in a controlled manner by repeating the catalyst deposition and nanowire growth steps. The ability to prepare rationally branched and hyper-branched nanowires should open up new opportunities for both fundamental research and applications, including three dimensional nanoelectronics.

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Y8, Heteroepitaxial Fabrication and Structural Characterizations of Ultrafine GaN/ZnO Coaxial Nanorod Heterostructures: *Sung Jin An*[1]; Won Il Park[1]; Gyu-Chul Yi[1]; Miyoung Kim[2]; [1]Pohang University of Science and Technology (POSTECH), Dept. of Matls. Sci. & Engrg., San 31, Hyoja-dong, Nam-gu, Pohang, Kyungbuk 790-784 Korea; [2]Samsung Advanced Institute of Technology (SAIT), PO Box 111, Suwon 440-600 Korea

Composition-modulated semiconductor nanorod heterostructures greatly increase the versatility and power of these building blocks for nanometer-scale electronics and optoelectronics. In particular, recent fabrication of semiconductor coaxial nanorod heterostructures showing a composition modulation along a nanorod radial direction is of high interest. Although the coaxial structures exhibiting a thick diameter of 20-100 nm have previously been applied for high electron mobility nanotransistors, the device performance may be enhanced by using ultrafine coaxial heterostructures. The ultrafine coaxial heterostructure exhibits one-dimensional quantum effects by carriers confined one-dimensionally in a core nanorod. Additionally, a well-defined, clean interface in the heterostructures is very important for excellent device performance and reliability since defects at the interface deteriorate device characteristics. For one-dimensional (1-D) coaxial heterostructures, especially, the effect of the interfacial defects on material properties becomes more significant due to their high interface to volume ratio. Nevertheless, interfacial defects in 1-D nanorod heterostructures have rarely been investigated yet. Here we report on synthesis of ultrafine GaN/ZnO coaxial nanorod heterostructures by heteroepitaxy and their structural defect characterizations. Initially, ultrafine ZnO nanorods with diameter less than 10 nm were grown on Si and sapphire substrates using catalyst-free metal-organic chemical vapor deposition (MOCVD). After the ultrafine ZnO nanorod preparation, GaN/ZnO coaxial nanorod heterostructures has been fabricated by epitaxial growth of a GaN layer on the nanorods. The epitaxial growth and precise control of GaN overlayer thickness were obtained by low pressure MOCVD. Both synchrotron-radiation x-ray diffraction and transmission electron microscopy (TEM) were employed for the structural characterizations of GaN/ZnO coaxial nanorod heterostructures. Furthermore, defects near the interface between ZnO and GaN layers were investigated using high-resolution TEM. Despite the observation of clean interfaces, close examination of the GaN and ZnO lattice images reveals the presence of edge dislocations.

4:30 PM

Y9, Ultrathin Epitaxial Metal Nanowires on Silicon (001) and (111): Tammo Block[1]; Svend Vagt[1]; Volkmar Zielasek[1]; *Herbert Pfnür*[1]; [1]University of Hannover, Inst. of Solid State Physics, Surface Sci. Sect., Appelstr. 2, D-30419 Hannover Germany

We combine electron beam lithography in ultra-high vacuum with epitaxy of silver on silicon (001) and (111) surfaces in order to generate crystalline metal nanostructures of arbitrary lateral shape with dimensions down to 10 nm on an insulating support. Our experiments are performed in a combined SEM-STM system (JEOL) for confocal and simultaneous operation of both microscopes at variable sample temperatures in the range 80-900 K. While the electron gun (1-25 keV) provides an SEM resolution of 4 nm a tiltable sample stage allows us to vary the angle of incidence between 30 and 0° so that also µRHEED images can be obtained. Employing a nanolithography technique pioneered by Ichikawa and coworkers[1] we generate clean Si(001) or (111) windows, resp., within a thin thermal surface oxide layer of 0.3-0.7 nm thickness by means of electron-beam stimulated thermal desorption: After irradiation of selected areas on the substrate surface by the electron beam (25 keV, doses in the range 100 C/sqcm) in order to stimulate oxygen desorption the substrate is heated to 1050 K. Thermal desorption of SiO from the pre-irradiated areas leads to the formation of windows within the oxide mask, baring clean, flat Si(001) (or (111)) terraces as demonstrated by STM and µRHEED. After silver deposition at a sample temperature of 130 K we observe the nucleation of small Ag islands in the windows as well as on the oxide areas. Subsequent annealing to room temperature or above leads to the formation of continuous flat epitaxial Ag islands constricted to the window areas with lateral sizes in the unconstricted direction in the range of some 100 nm while spherical non-percolated Ag clusters with diameters of several nanometers form on the oxide areas. So far we have demonstrated the generation of 2D Ag nanowires with a width of 20 nm and a total length of some micrometer.

In order to determine the influence of single structural defects like grain boundaries, lateral constrictions, or atomic steps on electrical transport we generate the nanowires between TiSi contact pads that are produced on the substrate ex-situ via standard e-beam lithography. First measurements of electrical conductance of single crystalline Ag nanowires using the TiSi contact pads and the STM tip as probes will be presented. [1]S. Fujita, S. Maruno, H. Watanabe, M. Ichikawa, J. Vac. Sci. Technol. B 16 (1998) 2817.

4:50 PM Student

Y10, Fabrications and Characterizations of Electroluminescent Devices Using n-ZnO Nanorod Arrays Vertically Grown on p-GaN Epilayers: *Won Il Park*[1]; Gyu-Chul Yi[1]; [1]Pohang University of Science and Technology (POSTECH), Dept. of Matls. Sci. & Engrg., San 31, Hyoja-dong, Pohang, Kyungbuk 790-784 Korea

ZnO is a promising material for short wavelength photonic device applications due to its direct and wide bandgap characteristic with a large exciton binding energy of 60 meV. Recently both ZnO epitaxial films and single crystalline nanorods have shown excellent optical characteristics. Further research on ZnMgO alloys enables control of bandgap energy in ZnO-based materials and fabrication of ZnO/ZnMgO nanorod quantum structures. Despite significant progress on ZnO films and nanostructures, difficulty of p-type doping in ZnO has impeded fabrication of ZnO p-n homojunction devices. As an alternative approach to homojunction, an n-ZnO/p-GaN heterojunction has been suggested as a strong candidate for device applications since these materials have similar fundamental band gap energy and crystal structure. Here we report fabrication of n-ZnO/p-GaN nanorod electroluminescent (EL) devices and their EL characteristics. The EL devices were fabricated using vertically well-aligned n-type ZnO nanorod arrays prepared on p-GaN(0001) substrates. The ZnO nanorods were epitaxially grown on the substrates employing catalyst-free metalorganic vapor phase epitaxy. Good ohmic contacts were made simply by evaporating Pt/Au and Ti/Au bilayers on p-GaN and n-ZnO, respectively and post-thermal treatement. The EL devices with nanosized p-n junction show high current density and strong electroluminescence, presumably due to the enhanced tunneling effect on the nanojunction. The EL spectrum at an applied reverse-bias voltage of 3 V shows a broad yellow emission band centered at 2.2 eV. For reverse bias voltages above 4 V, however, the EL spectra exhibited an additional blue emission at 2.8 eV and an ultraviolet (UV) emission peak at 3.35 eV. Origins of the EL peaks will be discussed.

Session Z: Semiconductor Nanostructures: Materials to Devices

Thursday PM   Room: 136
June 24, 2004   Location: DeBartolo Hall

Session Chairs: Mark Miller, University of Utah, Salt Lake City, UT USA; James L. Merz, University of Notre Dame, Notre Dame, IN 46556-5602 USA

1:30 PM Invited

Z1, Near-Infrared in Vivo Imaging Using Quantum Dots: *Sungjee Kim*[1]; [1]California Institute of Technology, Dept. of Applied Physics, MC 128-95, Watson Bldg., 1200 E. California Blvd., Pasadena, CA 91125 USA

Near-infrared is the most viable optical probe for noninvasive in vivo biomedical imaging, and quantum dots can be ideal nano-emitters for such applications. In order to demonstrate the design flexibilities and unique capabilities of quantum dots for near-infrared in vivo imaging, we report various in vivo imaging including sentinel lymph nodes and coronary vessels. We introduce new type-II band engineering and oligomeric phophine surface coating for the quantum dot surface. The type-II engineering allows the flexibility to simultaneously optimize the quantum dot size and the emission wavelength, resulting in deep photon penetrations and maximal absorption cross sections. The oligomeric phosphine coating provides excellent colloidal aqueous stabilities while minimizing the hydrodynamic size. Using these quantum dots in small and large animal models, we show how real-time near-infrared in vivo imaging can be performed.

2:10 PM Student

Z2, Solution Phase Synthesis of Straight and Branched CdSe Nanowires: *Katherine Leigh Richter*[1]; James W. Grebinski[1]; Jing Zhang[2]; Thomas H. Kosel[2]; Masaru K. Kuno[1]; [1]University of Notre Dame, Dept. of Chmst. & Biochmst., 251 Nieuwland Sci. Hall, Notre Dame, IN 46556 USA; [2]University of Notre Dame, Dept. of Elect. Engrg., 275 Fitzpatrick Hall, Notre Dame, IN 46556 USA; [2]University of Notre Dame, Dept. of Elect. Engrg., 275 Fitzptrick Hall, Notre Dame, IN 46556 USA

For decades there has been tremendous interest in understanding and ultimately controlling crystal growth. In the realm of today's nanoscience, this interest has materialized as studies into new routes for making high quality metal and semiconductor nanoparticles or quantum dots (NPs or QDs), nanorods (NRs), nanowires (NWs), as well as other higher order nanostructures. Renewed interest in making high quality 1D semiconductor NWs has been motivated by the discovery that metal NPs have catalytic properties for promoting asymmetric crystal growth. Recent investigations in this area have led to the development of synthetic techniques that include variations of traditional vapor-liquid-solid (VLS) growth, wherein chemically synthesized or laser ablated metal NPs are used as catalyst particles. Such routes take advantage of abovementioned advances in NP syntheses to overcome intrinsic droplet size limitations, ultimately allowing one to create previously unattainable, narrow diameter NWs. Other approaches include complete solution phase analogues of VLS growth such as solution-liquid-solid (SLS) growth and supercritical-fluid-liquid-solid (SFLS) synthesis. In all cases, these synthetic methodologies have opened up new routes for preparing semiconductor NWs with tunable diameters, lengths, compositions and axial composition gradients. Here the solution phase synthesis of narrow diameter (< 10 nm) CdSe NWs is described. Crystalline NWs with lengths between 1-10 microns are obtained using a SLS approach, whereby seeded NW growth is initiated using Au/Bi core/shell NPs. A gold biphasic reduction step is initially used to obtain small 1.5 nm diameter Au NPs. This is followed by the thermolysis of trialkylbismuthines in the presence of the Au NPs to yield low melting, bimetallic, core/shell particles. The resulting Au/Bi NPs have diameters less than 5 nm and are catalytically active towards the growth of similar diameter CdSe NWs. NWs with diameters ~7 nm are obtained which may exhibit confinement effects given that the bulk exciton Bohr radius of CdSe is 5.6 nm. The choice of surfactant during the NW synthesis is observed to alter the NW growth kinetics, leading to NRs at one extreme and NWs at another. Furthermore, the presence of surface binding surfactants yields soluble NWs opening up interesting possibilities for future surface modification and/ or functionalization chemistries. Preliminary structural characterization shows NW growth along either the [111] or [0001] directions of the zinc blende (ZB) and wurtzite (W) phases respectively. High resolution TEM imaging reveals that the NWs alternate between the ZB and W structures along their length, and that the ZB sections have a very high incidence of twinning. Additional modifications to the preparation are also shown to yield higher order branched NWs. This opens up the distinct possibility of studying not only diameter dependent optical/electrical properties of NWs but also their shape and morphology dependent properties as well.

2:30 PM

Z3, Metal-Semiconductor Transition in Armchair Nanotubes: Possibilities for Metallic FET: *Slava V. Rotkin*[1]; Karl Hess[1]; [1]University of Illinois, Beckman Inst. for Advd. Sci. & Tech., 405 N. Mathews, Urbana, IL 61801 USA

Carbon nanotubes are very promising for nano- and molecular scale electronics due to the unusual dependence of the electronic properties on the tube symmetry. Semiconductor single-wall nanotubes (S-SWNTs) were already shown to have a high mobility and to work as channels of a MOS-FET and a Schottky-Barrier FET. On the other hand true metallic armchair (A-)SWNTs are ballistic. This is due to a "super"-symmetry of their band structure, which suppresses any back-scattering. We recently proposed a novel type of FET which uses a symmetry breaking mechanism and a creation of a semiconductor gap in the metallic A-SWNT. Electronic transport in a {\em metallic one dimensional FET} (METFET) may be controlled by use of an {\em inhomogeneous} electric field that is induced by a {\em highly localized} gate such as an STM tip, nanotube

THURSDAY PM

tip or nano-interconnect. The highly localized gate induces a high electric field in a narrow region. The weak screening of electric potentials in 1D channels enhances any possible field effects. We have studied two possible mechanisms for a local band gap opening: (i) The non-linear Stark effect and (ii) band-structure modulation by a very non-uniform (multipole) electric field. Tight-binding techniques were used to calculate the band structure of the A-SWNT. This approach was demonstrated to give very accurate results when the electrostatics of the problem is included in a self-consistent way. The gated region of the METFET channel (with the semiconductor band gap) represents a barrier for charge carriers. The barrier height is modulated by the gate voltage, which modulates the transmittance. An effective mass of the bulk nanotube material is small (typically about 0.06 of free electron mass) that leads us to expect a high tunneling rate for a METFET device. Indeed, for a typical nanotube of one nanometer diameter, the reflection coefficient is low. We have calculated it taking into account tunneling and thermionic emission. Low enough reflection prevents the formation of a Coulomb blockaded island in the gated region, unless the gap induced by the gate field is very large. However, for high gate voltage the reflection grows and the Coulomb blockade at the interface may add to the impedance of the channel in OFF state. We have calculated the transmittance for broad temperature range for [5,5] and [10,10] metallic (0.7 and 1.4 nm) nanotube channels for local gates resembling the geometry of a tunneling tip. The dependence of the current-voltage characteristics of these METFET's on the temperature, NT size and device geometry as well as the OFF/ON current ratio will be presented.

2:50 PM
Z4, Size and Position-Controlled Zinc Oxide Nanodot Arrays with Focused Ion Beam Nanopatterning of Substrates: *Shizuo Fujita*[1]; Sang-Woo Kim[2]; Masaya Ueda[2]; Shigeo Fujita[2]; [1]Kyoto University, Internatl. Innovation Ctr., Yoshida honmachi, Sakyo-ku, Kyoto, Kyoto 606-8501 Japan; [2]Kyoto University, Dept. Elect. Sci. & Engrg., Kyotodaigaku-katsura, Nishigyo-ku, Kyoto, Kyoto Japan

Size and position control of semiconductor nanostructures in self-assembled process is now a key issue toward actual device applications. In this paper we report the well-controlled formation of zinc oxide (ZnO) nanodot arrays, which is promising for the appearance of unique optical effects supported by enhanced confinement of excitons of large binding energy (60meV in bulk ZnO), on SiO_2/Si substrates nanopatterned by focused ion beam (FIB) technology. We have already shown that ZnO nanodot can be selectively formed on FIB-nanopatterned area by metal organic chemical vapor deposition. Following to the result above, we could achieve, by using a low magnification FIB patterning mode, periodical nanopatterning of the substrates over a large area in a short time. For example, a periodical 40,000 nanoholes array was formed over the area of 38x38μm^2 with the period of 190nm in 60min of the etching time. Then one ZnO nanodot was formed on one nanodot, resulting in a two-dimensional 40,000 nanodots array with the period of 190nm. The diameter of more than 90% of nanodots was within 45-55nm with the height of about 5nm. The minimum period achieved so far is 100nm. Cathodoluminescence from a single ZnO nanodot was obviously observed at room temperature. Blue-shift of photoluminescence peak in comparison to the bulk ZnO suggested the low dimensional confinement of excitons. Detailed structural and optical characterizations of the nanodots are now going on and are to be included in the presentation.

3:10 PM Break

3:30 PM Student
Z5, Defect-Free 50-Layer Strain-Balanced InAs Quantum Dots Grown on AlGaInAs/InP for Infrared Photodetector Applications: *Zhenhua Zhang*[1]; Chaofeng Xu[1]; Kuang-Chien Hsieh[1]; Keh-Yung Cheng[1]; [1]University of Illinois, Dept. of Elect. & Computer Engrg., 150 Micro & Nanotech. Lab., 208 N. Wright St., Urbana, IL 61801 USA

Recently, extensive research has been devoted to photodetectors in the infrared (2-20 μm) range of the optical spectrum. Current state-of-the-art detectors employ either intrinsic infrared radiation detection using very narrow bandgap semiconductors, or intersubband transitions in the quantum well infrared photodetectors (QWIPs). However, both these approaches encountered technical limitations and are extremely difficult to achieve room temperature operation. Theoretical studies indicate that photodetectors based on quantum dot (QD) nanostructures have a great potential to outperform state-of-the-art bulk and QW infrared photodetector devices. Unfortunately, current device performance lags behind the theoretical predictions, partially due to the difficulties encountered in the precise control of the self-assembled QD formation process. The resultant non-uniform QD distributions with low dot density dramatically degrade the device performance, resulting in a low responsivity and a high dark current. One of the tractable methods to improve the device performance is to employ structures with multiple, vertically stacked QD layers, which can improve the uniformity and the electronic structure of the QDs due to the vertical coupling of QDs. The multilayer structure can also effectively increase the absorption of incident photons. Nevertheless, the accumulation of the strain between the QD and barrier materials prohibits the stacking of a large number of QD layers without the generation of defects. In this study, a strain-balanced QD system is developed to achieve a defect-free multilayer QD structure using thin barrier layers to improve vertical coupling of QDs. In our design, a tensile strained GaAs layer is used to balance the compressive strain caused by the growth of InAs QDs on $Al_{0.24}Ga_{0.24}In_{0.52}As$ barrier layer on InP substrate. Fifty layers InAs QD was grown by molecular beam epitaxy with thin AlGaInAs barrier layers (150 Å) and GaAs strain-balance layers separating the QD layers. During the growth, the reflection high-energy electron diffraction pattern clearly showed a spotty to streaky transition after the deposition of the GaAs layer, indicating the 3-dimensional islands on the surface have been effectively smoothed out by the GaAs layer. High-resolution x-ray diffraction measurements show a rocking curve with satellite peaks caused by the periodic QD layers symmetrically distributed on both sides of the substrate peak, proving that the overall strain with in the QD structure is effectively balanced. The density of the defects of the structure is estimated to be much below 10^6 cm^{-2} since there are no visible defects detected by the transmission electron microscopy (TEM). TEM pictures also indicate a strong vertical alignment of QDs in the growth direction, which serves as an evidence of the increase of the uniformity of QDs by stacking multiple QD layers.

3:50 PM
Z6, Modification of Band Structures in Stacked InAs/GaAs Quantum Dot Systems by the Control of Mismatch Strain: *Woong Lee*[1]; Jae-Min Myoung[1]; [1]Yonsei University, Matls. Sci. & Engrg., 134 Shinchon-dong, Seoul 120-749 S. Korea

Numerical analysis has been carried out to seek possible routes to modify band structures for tailoring the properties of InAs/GaAs quantum dot (QD) systems by the control of lattice mismatch strains. Using a finite element method based on continuum elasticity, strain fields due to lattice mismatch between constituent materials were calculated and band edge profiles were subsequently estimated using this strain information within the framework of eight-band k·p theory. Three possible routes were included in the numerical modelling: namely, change of stacking period (inter-dot spacing), change of dot shape (dot truncation) and introduction of InxGa1-xAs strain relief-layer. Numerical analysis predicted that strains within the dot are substantially modified by the change in geometric parameters such as stacking period and dot shape (dot truncation). In this case, redistribution of strain occurred in such a way that hydrostatic strain remains constant regardless of the change in system geometry while the change in biaxial strains were significant. For a given dot shape, relaxation of the biaxial strains were predicted with smaller stacking period and for a given stacking period, strains were relaxed with dot truncation. Such change in strains resulted in the substantial change in heavy-hole edges in valence band but conduction band edges and light-hole edges were relatively insensitive to the geometry change. Lower heavy-hole edge was predicted at smaller stacking period and dot truncation lowered it further at a given stacking period. When InxGa1-xAs strain relief layer was introduced between the InAs QD and GaAs spacer, it was predicted that tensile axial strain and compressive radial strain within the dot are significantly relieved with increasing In content in the strain-relief layer. This resulted in the reduction of the magnitude of hydrostatic strain and biaxial strain, and the amount of strain relaxation was approximately proportional to the In content. Effect of strain relaxation in the dots and neighbourin g regions was well reflected in the downward shift of the conduction band edge in the dot region and flattening and upward shifts of the heavy-hole and light-hole edges in the valence band yielding narrower band gap within the dot. Significance of the numerical results herein was illuminated by comparing them with experimental results reported elsewhere. It is concluded that geometry control alone may not be sufficient to achieve QD systems

with wide range of designed properties and that control of strains in quantum dot structures via incorporation of strain-relief layer would be an effective way of band gap engineering. Further, it is proposed that if this strategy is used with geometry control, greater flexibility in the tailoring of QD properties could be achieved.

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Z7, Selectivity Between Quantum Dots and Dashes on InP and GaAs Based on Lattice Mismatch and Surface Migration: *G. Balakrishnan*[1]; Shenghong Huang[1]; L. R. Dawson[1]; H. Xu[2]; D. L. Huffaker[1]; [1]University of New Mexico, CHTM, 1313, Goddard SE, Albuquerque, NM 87106 USA; [2]University of New Mexico, Earth & Planetary Scis., Albuquerque, NM 87131 USA

We demonstrate the ability to manipulate self-assembly of quantum structures using lattice mismatch. We report the growth of quantum dots (QDs) and quantum dashes (QDashes) on GaAs and InP by molecular beam epitaxy. Furthermore, we have also shown for the first time the formation of In(0.5)Ga(0.5)Sb QDs on InGaAs/InP (001) with 3 ML coverage of dot material. Using an AlGaAsSb metamorphic buffer (MB) grown on GaAs to alter the lattice constant of the growth matrix, we are able to form QDs under highly strained conditions ($\Delta ao/a > 4\%$) and QDashes under low strain conditions ($\Delta ao/a < 4\%$). In the low strain conditions, the asymmetric surface migration inherent in the [1-10] direction in zinc blende structures dominates the QDash formation process. Using this principle we have reduced mismatch on GaAs by growing In(0.42)Ga(0.58)As ensembles, resulting in dash like structures along the [1-10] direction. Similarly we have increased the mismatch on InP by growing In(0.5)Ga(0.5)Sb resulting in QDs. These QDs are grown at 400 degrees Celsius and they nucleate with 3 ML coverage. The dots have a height of 8 nm and a diameter of 25 nm with a dot density of 4 x 10^10/cm^2. We have studied the crystal structure of both QDs and QDashes using real-space mapping and fast-fourier transform (FFT) to determine the lattice constant distribution within the quantum structure in very high-resolution transmission electron microscopy (HRTEM). Based on these studies we have concluded that the QDashes have a tensile core with compressive material forming the wetting layer and the enclosing planes. The dots have a similar structure; however the increased lattice mismatch makes them taller structures resulting in the tensile core at the center of the pyramidal structure and of lesser magnitude compared to the dashes. Studies are currently being done to establish the composition of the QDs and QDashes by z-contrast STEM imagery. This information put together with the strain information should provide us with a better insight into the mechanism of self-assembly.

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Z8, Red Light Emission by Electroluminescence from InP Quantum Dots on GaP(100): *F. Hatami*[1]; W. T. Masselink[1]; V. Lordi[2]; J. S. Harris[2]; [1]Humboldt-UniversitÄat zu Berlin, Dept. of Physics, Newtonstr. 15, 12489 Berlin Germany; [2]Stanford University, Dept. of Elect. Engrg., Stanford, CA 94305 USA

Light emitting semiconductor devices are key components for information transmission, information storage, visible displays, and lighting. Today, gallium phosphide (GaP) is usually used for emission in wavelengths consistent with human vision from red to green. GaP is an indirect bandgap semiconductor with a low luminescence efficiency and light emission is possible by doping gallium phosphide with deep levels. The quantum efficiency of such light emitting diodes is, however, very low and not sufficient for high brightness applications. The realization of direct recombination within a GaP matrix and on transparent GaP substrate is potentially of great importance because it could allow significantly higher quantum efficiencies. Furthermore, using gallium phosphide rather than gallium arsenide as substrate allows easier extraction of the emitted light for vertical structures such as super-luminescent LEDs or vertical cavity lasers. Indium phosphide (InP) quantum dots embedded in a GaP matrix and on a GaP substrate offer promising solutions to these challenges. Recently, we have demonstrated photoluminescence from type-I InP/GaP quantum dots.[1,2] In the present work the electroluminescence of self-organized InP quantum dots embedded in a GaP matrix are presented and discussed, together with their growth and fabrication. The diode structures are grown using gas-source molecular-beam epitaxy; the active range of the diodes consists of self-assembled InP quantum dots embedded in GaP matrix. The electroluminescence spectra consist of two emission lines peaked in the green and red range. The green line at about 550 nm appears to result from carrier recombination in the strained InP wetting layer and perhaps in the surrounding GaP matrix. The red line at about 700 nm is attributed to the electron-hole recombination in the quantum dots. For the currents lower than 100 mA the electroluminescence spectra are dominated by the electroluminescence due quantum dots. The electroluminescence from quantum dots is observed up to room temperature. [1]F. Hatami, L. Schrottke, and W.T. Masselink, Appl. Phys. Lett. 78, 2163 (2001). [2]F. Hatami, W.T. Masselink, L. Schrottke, J.W. Tomm, V. Talalaev, C. Kristukat, and A.R. Gõni, Phys. Rev. B 67, 85306 (2003).

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Session AA: Dilute Nitrides

Thursday PM June 24, 2004 — Room: 140 — Location: DeBartolo Hall

Session Chairs: Charles W. Tu, University of California, La Jolla, CA 92093-0407 USA; Luke Mawst, University of Wisconsin, Madison, WI 53706 USA

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AA1, Near-Field Scanning Optical Microscopy of Compositional Fluctuations in Dilute Nitride Alloys: *Kai Sun*[1]; Alexander M. Mintairov[1]; Thomas H. Kosel[1]; Victor M. Ustinov[2]; Gregory M. Peake[3]; James L. Merz[1]; [1]University of Notre Dame, Dept. of Elect. Engrg., Notre Dame, IN 46556 USA; [2]Ioffe Physico-Technical Institute, 26 Polytechnicheskaya, St. Petersburg 194021 Russia; [3]Sandia National Laboratory, Albuquerque, NM 87185 USA

Dilute nitride alloys (GaAsN, InGaAsN and GaAsSbN) have recently attracted considerable attention as promising materials for laser diodes in the 1.3-1.5 micrometers range as well as for more efficient solar cells. These applications exploit their unusual electronic property - a giant bowing parameter (b ~20 eV), which arises from the large electronegativity and the small size of the nitrogen. The resulting large energy scale for statistical composition fluctuation leads to the creation of intrinsic quantum dots (QDs) in these alloys, which have been observed in near-field photoluminescence (NPL).[1] Here we present images of this QD emission in GaAsN epi-layers and a GaAsSbN quantum well (QW) using low-temperature near-field scanning optical microscopy (NSOM). We studied GaAsN epilayers (thickness 0.1-0.3 micrometers) and a 6 nm GaAsSbN QW grown on (001) semi-insulating GaAs substrates by solid source molecular beam epitaxy and by metal-organic vapor phase epitaxy, respectively. NPL spectra were taken in collection-illumination mode using uncoated fiber tips providing spatial resolution of 300 nm. The spectra were excited by 20 mW from an Ar ion laser. The NPL signal was integrated over 60 s/tip position-pixel over the whole measured spectral range (40 nm). The NPL images shown in this work were made over a range of 11x8 pixels with 200x200 nm size. We have found that monochromatic images of GaAsN epi-layers consist of a series of bright spots having spatial extent of 300-600 nm. Simultaneous analysis of these images and the near-field spectra show that the spatial resolution of these experiments is 300 nm. The larger images, and their observed elongated shapes, are due to the overlapping of different lines. Using these near-field images we observed a strong lateral inhomogeniety in GaAsN epilayers on the length scale of 1000 nm. For the GaAsSbN QW the images of the individual clusters consist of bright stripes having width 400-600 nm oriented along one of the {110} directions. The separation between the stripes is 300 nm. The length of the stripes is greater than 2000 nm. Plan-view transmission electron microscopy measurements showed the presence of composition modulation along the [110] direction having a wavelength ~100 nm. The orientation and the lateral dimensions of the composition modulation stripes observed in TEM agree well with NSOM images. However as the NSOM data are related to the emission of individual clusters, the stripe character of the images can be related to the diffusion of photo-generated carriers along the quantum-

wire-like channels created by As and Sb phase separation. The very large spatial extent of the images, exceeding a few micrometers, suggests a long life-time of photogenerated carriers, which can be attributed to II-band alignment in GaAsSb. [1]A. M. Mintairov et al, Phys. Rev. Lett. 87, 244701 (2001).

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AA2, Identification of Nonradiative Recombination Centers in Ga(As,N) by Raman Spectroscopy: *Manfred E. Ramsteiner*[1]; De-sheng Jiang[2]; Gregor Mussler[1]; James S. Harris[3]; Klaus H. Ploog[1]; [1]Paul Drude Institute for Solid State Electronics, Hausvogteiplatz 5-7, Berlin 10117 Germany; [2]NLSM, Inst. of Semiconductors, Beijing 100083 China; [3]Stanford University, Solid State & Photonics Lab., Stanford, CA 94305 USA

Despite the technological progress made in recent years, state-of-the-art Ga(As,N) and (In,Ga)(As,N) contains a considerable amount of electronic traps involved in the nonradiative recombination of electron-hole pairs. These recombination centers have to be removed by thermal annealing in order to achieve sufficient photoluminescence (PL) intensities. We studied nitrogen-related point defects and their annealing behavior in diluted Ga(As,N) by Raman spectroscopy in order to identify nonradiative recombination centers. The Ga(As,N) samples were grown by solid-source molecular beam epitaxy on GaAs(001) substrates. Raman spectra of all investigated as-grown samples reveal two peaks at 409 cm^{-1} (line X) and 427 cm^{-1} (line Y) which cannot be explained by Ga(As,N) lattice phonons. Since their integral intensity is related to the N concentration, lines X and Y are attributed to N-related defects. The origins of the two defect-related lines are different, since their relavite intensities vary from sample to sample. Their frequencies are in the range of those found for local vibrational modes (LVMs) of Si on Ga (Si_{Ga}) and As (Si_{As}) sites in GaAs. Actually, the frequencies of lines X and Y are both larger by the same factor of 1.07 than the ones of the LVMs induced by Si_{Ga} (384 cm^{-1}) and Si_{As} (398 cm^{-1}). Since N_2 molecules have the same atomic weight as Si (28 amu), it is reasonable to attribute lines X and Y to N dimers on Ga-site and As-site, respectively. Thereby, we assume that the whole molecule is vibrating as one unit like the Si impurity, but with force constants increased by about 3.5% (= sqrt{1.07} - 1). In the cases of a triple bond between the nitrogen-dimer atoms like in free N_2 molecules or a more hydrazine-like (N_2H_4) configuration, there are four valence electrons which are still available for the bonding with the Ga or As host atoms. This is a further analogy to Si on Ga or As site. The defect-induced Raman scattering efficiency is strong only for excitation at photon energies in the range between 1.8 and 2.0 eV. This resonance behavior can be attributed to the enhancement of the Raman efficiency for photon energies approaching the localized E_+ transition in Ga(As,N). The different resonance behavior observed for the two defect-induced lines provides more evidence for the assertion that they are not of the same origin. This finding is consistent with our above assignment to N dimers on different GaAs lattice sites. Rapid thermal annealing under appropriate conditions is found to be able to remove the nitrogen dimers. The required minimum annealing temperature coincides with the threshold-like onset of strong, near-bandgap photoluminescence for various growth conditions. This finding suggests that the nitrogen dimers are connected with nonradiative recombination centers.

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AA3, Thermal Annealing Effects and Local Atomic Configurations in GaInNAs Thin Films by Fluorescence X-Ray Absorption Fine Structure Spectroscopy: *Kazuyuki Uno*[1]; Masako Yamada[1]; Toshiyuki Takizawa[2]; Ichiro Tanaka[1]; Osamu Ohtsuki[1]; [1]Wakayama University, Systems Eng., Sakaedani 930, Wakayama 640-8510 Japan; [2]Matsushita Electric Ind., Saiwaicho 1-1, Takatsuki, Osaka 569-1193 Japan

Dilute nitride GaInNAs Alloys attract considerable attention due to their unique physical properties and potential application to infrared devices. Rapid Annealing or postgrowth annealing significantly improves the photoluminescence (PL) efficiency of these films and the PL peak wavelength is blue-shifted. The origin of these changes would be due to some structural changes by thermal annealing. We have studied the nearest-neighbor configuration around In atoms of GaInNAs alloys by fluorescence X-ray absorption fine structure (XAFS) spectroscopy.[1-3] In our previous XAFS measurements, we obtained some experimental results that suggested the increase in the number of In-N bonds in GaInNAs thin films after thermal annealing.[1,2] In this study, we carried out XAFS measurements at a low temperature (30K). By supressing bond vibration, we obtained distinct changes of short-range-order configuration with thermal annealing. GaInNAs samples were grown on GaAs (001) substrate by molecular beam epitaxy (MBE) with an electron cyclotron resonance plasma source. The N and In composition can be described as $Ga_{0.78}In_{0.22}N_{0.013}As_{0.987}$. Thermal annealing was carried out at 800°C for 1 min under As irradiation. Low-temperature (30K) fluorescence XAFS measurements around the In-K absorption edge were carried out at SPring-8 in Japan. Fluoresecnece XAFS measurements were successfully carried out. the radial distribution function (RDF) was calculated and peak fittings using a XAFS simuration program were carried out to examine the local atomic alignments of the samples. We investigated the following two cases: one is In-As-Ga which means As atom is the first nearest atom of In, and the other is In-N-Ga which means N atom is the first nearest. The RDF spectrum of the as-grown GaInNAs sample has two distinct peaks. These correspond to In-As-Ga configuration and the distance between In and Ga atom was expected to be 0.404nm. The RDF spectrum of the annealed GaInNAs sample has three distinct peaks. The two peaks located at the same position as those of the as-grown sample. The third peak reflects the existence of In-N-Ga configuration and the distance between In and Ga atom was expected to be 0.320nm. The above experimental results show the number of In-N bonds increases by thermal annealing. Ab initio calculations using density functional theory were carried out to examine the above considerations. A modeled super cell consists of $Ga_{31}In_1As_{31}N_1$ and its lattice constant was 0.5726nm. The distance from In to Ga in the case of In-As-Ga configuration was 0.4322nm and that in the case of In-N-Ga was 0.3465nm. The ratio of the two values is about 0.8:1.0, which is consistent with the XAFS results. [1]V.Lordi, et al., Phys.Rev.Lett.90 (2003)145505., [2]V.Gambin, et al., J.Cryst.Growth 251 (2003) 408., [3]K.Uno, et al., Jpn.J.Appl.Phys. (2004) in press.

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AA4, Transmission Electron Microscopy (TEM) Structural Characterization of GaInNAs and GaInNAsSb Quantum Wells Grown by Molecular Beam Epitaxy (MBE): *Tihomir Lubenov Gugov*[1]; Homan B. Yuen[1]; Seth R. Bank[1]; Mark A. Wistey[1]; Vincent Gambin[1]; James S. Harris[1]; [1]Stanford University, Solid State & Photonics Lab., 121 Campus Dr., Lyman Apt. 1101B, Stanford, CA 94305 USA

The quaternary GaInNAs alloy is a very promising material system for optical sources in the 1.2-1.6 micron range with application in telecommunication fiber-optic networks. Unfortunately, this is not a thermodynamically stable alloy and considerable growth challenges need to be overcome to improve the optical emission efficiency of the material. Considerable progress in dealing with these difficulties has been made for alloys containing around 30% In and 2% N which emit light around 1.3 microns. The effort to push emission out to 1.5 microns, the wavelength for long haul networks, by adding more In (up to 40%) has proven considerably more difficult. Recently, the addition of small amounts of Sb has put this alloy back on track for the 1.5 micron challenge by dramatically improving the luminescence efficiency of the material. In this work, several different TEM techniques are used for the first time as powerful tools in the structural characterization of GaInNAs(Sb) quantum well structures at the atomic level. High resolution TEM (HRTEM) is used to map out the local strain and compositional fluctuations in the quantum wells and barriers. This is correlated with Energy Filtered TEM (EFTEM) imaging as well as dark field (DF) imaging with the chemically sensitive (002) reflection. Both GaInNAs and GaInNAsSb samples were characterized with these techniques. We found that In tends to segregate for the GaInNAs samples while Sb is responsible for a much more uniform distribution of In in the GaInNAsSb samples. The results of this work bring further understanding of the performance of real devices. GaInNAs lasers are known to have broad emission spectra and high threshold currents. Researchers have speculated that this could be due to local compositional fluctuations. Our results confirm that this indeed occurs and give considerable insight into the role of Sb in improving the material quality leading to high luminescence efficiency.

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AA5, Electroabsorption and Band Edge Optical Properties of GaInNAsSb Quantum Wells Around 1550nm: *Vincenzo Lordi*[1]; Homan B. Yuen[1]; Seth R. Bank[1]; Mark A. Wistey[1]; James S. Harris[1]; [1]Stanford University, Solid State & Photonics Lab., CISX B113-17, 330 Serra Mall, Stanford, CA 94305-4075 USA

Electroabsorption modulators operating in the telecommunications wavelength range of 1300-1600 nm are important not only for optical fiber communications, but also for use in low-voltage optical interconnects to replace the electrical lines limiting the future speed of microelectronics. The novel dilute nitride III-V alloy GaInNAsSb is a promising material system for realizing quantum well (QW) devices on GaAs that operate in this wavelength range. GaInNAsSb QWs were grown by solid source molecular beam epitaxy (MBE), with atomic N supplied by a radio frequency nitrogen plasma and Sb supplied by a cracked solid source. Growth at 400-425°C was followed by rapid thermal annealing (RTA) at 760-800°C for up to 3 min. The test device consisted of a GaAs p-i-n diode with a 0.5 µm thick intrinsic region containing the QWs. Active regions consisted of up to 3 GaInNAsSb QWs 8 nm thick, with 20 nm thick GaNAs barriers. The QW composition was ~40% In, ~2.5% N, and ~2.7% Sb. The barriers contained ~2.7% N. Electroabsorption spectra of the GaInNAsSb QWs were measured by photocurrent using a monochromated white light source, at various temperatures from 25 to 300 K and with applied electric fields up to 200 kV/cm. The spectra demonstrated very nice quantum confined Stark effect (QCSE) behavior, with sharp exciton peaks having FWHM less than 25 meV at 295 K. Measurements were performed on a series of samples with increasing doses of ex situ annealing after growth. Annealing was found to increase the absorption coefficient of the material, while also blue shifting the band gap. However, the band gap ceased to blue shift after a certain thermal dose. The fully annealed sample exhibited a peak absorption coefficient on the order of 30,000 cm^{-1} at ~1540 nm wavelength. The measured electroabsorption characteristics indicate that the material is suitable for optical modulation around 1550 nm, using a few volts swing. Furthermore, electroreflectance, photoluminescence, and electroluminescence spectroscopies were used to study a series of transitions near the apparent band edge of the material that correspond to different N nearest neighbor configurations. Annealing shifts the distribution of configurations toward those with larger band gaps, which correspond to increased numbers of N-In bonds. The anneal-induced blue shift of the band gap saturates after the material has homogenized and reached the equilibrium configuration of nearest neighbor N-In bonds. This behavior is similar to what we previously observed in GaInNAs, except the energy spacing is smaller for the Sb-containing material. In addition, the exciton lineshape observed using the various measurement techniques was found to be Gaussian at 295 K, rather than Lorentzian, indicating a strong exciton-phonon interaction and/or a high density of lattice defects in the material, consistent with theoretical expectations.

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AA6, Effects of Arsenic Species and Si-Doping on Nitrogen Incorporation in GaAsN Films: M. Reason[1]; *H. A. McKay*[1]; X. Weng[1]; N. G. Rudawski[1]; W. Ye[1]; R. S. Goldman[1]; V. Rotberg[2]; [1]University of Michigan, Dept. of Matls. Sci. & Engrg., 2300 Hayward St., H. H. Dow Bldg., Ann Arbor, MI 48109-2136 USA; [2]University of Michigan, Dept. of Nucl. Engrg. & Radiological Scis., Ann Arbor, MI 48109-2136 USA

GaAsN and InGaAsN alloys with a few percent nitrogen have potential applications in infrared laser diodes, high efficiency solar cells, and other electronic devices. However, as-grown materials often exhibit poor photoluminescence efficiencies and lower than expected carrier concentrations and mobilities. In the case of dilute GaAsN alloys, conflicting results have been reported regarding nitrogen incorporation into substitutional vs. interstitial sites. To our knowledge, the effects of arsenic species and Si-doping on N incorporation in GaAsN have not yet been considered. In this work, we have investigated the effects of several growth conditions on N incorporation in GaAsN films grown by solid-source molecular beam epitaxy using a 10% N2/ 90% Ar RF plasma source. The samples consist of a 500 nm GaAs buffer layer grown at 580°C followed by a 500 nm layer of GaAsN (0.5 to 3.5% N) grown with a variety of growth temperatures (400 - 580°C), deposition rates (0.3-1µm/hr) , V/III ratios (5-30), arsenic species (As_2 or As_4), and Si-doping concentrations (undoped to $5x10^{18}$ cm^{-3}). Nuclear Reaction Analysis and Rutherford Backscattering Spectrometry in channeling and non-channeling conditions reveals significant composition-dependent non-substitutional incorporation of N, presumably as N-N or N-As split interstitials. For undoped films, the fraction of interstitial N increases linearly with increasing total N concentration and is apparently not affected by the growth temperature, V/III ratio, or arsenic species. For doped alloys, the relative concentrations of substitutional and interstitial N depends on the growth temperature, with higher substitutional and interstitial concentrations for low and high growth temperatures, respectively. It is well known that Si doping of GaAs often leads to the formation of charged Si-vacancy pairs.[1] It is possible that an electrostatic interaction between charged Si-vacancy pairs and charged N-N or N-As split interstitials drives up the concentration of N interstitials for the high temperature-grown Si-doped GaAsN films. [1]J.E. Northrop and S.B. Zhang, Phys. Rev. B 47, 6791 (1993).

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AA7, Temperature Dependent Behavior of GaInNAs(Sb) Alloys Grown on GaAs: *Seth R. Bank*[1]; Vincenzo Lordi[1]; Mark A. Wistey[1]; Homan B. Yuen[1]; James S. Harris[1]; [1]Stanford University, Solid State & Photonics Lab., 126X CIS-X, Via Ortega, Stanford, CA 94305 USA

Since the initial discovery of anomalous bowing in dilute nitride-arsenide alloys by Kondow and co-workers, intense research has led to the realization of high-performance GaAs lasers at 1.3 and 1.5 µm. GaInNAs and GaInNAsSb devices possess many potential advantages over InGaAsP/InP structures including temperature insensitive threshold current, high quantum well (QW) gain, and the availability of high index contrast AlAs/GaAs distributed Bragg reflector mirrors for monolithic vertical-cavity surface-emitting lasers. The addition of antimony into GaInNAs, along with continued improvements in growth techniques, was key to recent advances in the 1.5 µm emission regime. In this talk we investigate these materials using temperature dependent photoluminescence (PL) in the context of carrier localization to quantify local potential fluctuations. Localization at low temperature (< 150 K) has been reported in GaInNAs alloys by several groups and, in extreme cases, manifests itself as an "S-shape" in the bandgap versus temperature. Pinault and Tournie found that material quality, specifically the amount of non-radiative centers, is directly related to the severity of localization and the temperature at which it occurs. With improvements in material quality, such as those reported by Misiewicz and collaborators, the S-shape has recently been suppressed, although some degree of localization still remains at low temperatures (< 70 K). This low temperature localization was found to be directly proportional to the nitrogen mole fraction. To quantify this effect, Misiewicz and co-workers have adopted the energy separation between the Varshni fit and the measured data at 10 K (found to be 2.36 meV/%N). Using this metric, we show reductions in the localization due to improvements in growth conditions and the addition of antimony into GaInNAs. The temperature dependence of the localization energy for a single $Ga_{0.62}In_{0.38}N_{0.023}As_{0.95}Sb_{0.027}$ QW sample annealed at 740°C for one minute was found to be 2.5 meV (at a power density of ~10 W/cm^2) and is twofold lower than predicted by Misiewicz. Additionally the localization energy is found to depend on anneal; the as-grown sample showed somewhat stronger localization. The addition of antimony was found to reduce the localization energy, as expected from work on surfactant-mediated growth. Without antimony, the localization was greater than predicted by Misiewicz; with antimony, however, the localization energy was less than Misiewicz. These are the first reported measurements of reduced localization in GaInNAsSb films.

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AA8, Ion Damage in Dilute Nitride Growth: Effect of Deflector Plate Voltage: *Michael M. Oye*[1]; Jason M. Reifsnider[2]; Sridhar Govindaraju[1]; Archie L. Holmes[2]; [1]University of Texas, Microelect. Rsch. Ctr. & Texas Matls. Inst., MS R9900, Austin, TX 78712 USA; [2]University of Texas, Microelect. Rsch. Ctr. & Dept. of Elect. & Computer Engrg., Austin, TX 78712 USA

The molecular beam epitaxy growth of GaN and GaNAs material systems often utilize a nitrogen RF plasma source. In addition to neutral atomic species, ions are among the constituents produced. These ions have long been cited as the cause for crystal damage leading to the poor optical and electrical properties of MBE-grown materials. One commonly known method to remove these damaging ions is with the use of DC-biased deflector plates situated at the outlet of an RF plasma source. In practice, these deflector plates have been utilized without any consideration of additional effects that may be influencing the material quality. In this work, we present a study of the effects of the DC deflector plate voltage on the optical properties of dilute nitride materials. All growths were done in a Varian Gen-II MBE system. The active nitrogen species

were created using a VEECO-Applied EPI UniBULB™ RF plasma source. A 0.4 sccm gas flow rate was used for the 1% N in Ar gas mix at a RF power of 425 W. These RF conditions were shown to produce ion damage in our previous work. All samples were grown with a common structure at a temperature of 580°C, except for the GaInNAs quantum wells that were grown at 450°C. The triple quantum wells, each 70 angstroms thick, comprised of ~20% In and ~1% N. Equivalent structures were grown with various DC voltage settings across the deflector plates, which ranged from 0 to 2000V. We determine the extent of ion damage from the sample quality, which in turn was measured by the PL intensity improvement upon a post-growth RTA treatment at 850°C for 180 sec. The variation in PL intensity improvement for different deflector plate voltage settings suggest that additional ions are being generated within the plates. There are two observations suggesting this. The first involves an observed four-fold improvement—at an applied voltage of 800V—in the PL intensity upon a RTA treatment when compared to the improvements in the sample grown at other deflector plate voltages. A precipitous drop at higher applied voltages suggests that a Townsend (or dark) discharge develops. The second observation, at lower applied voltages, involves measured current levels across the deflector plates that were saturating at higher than expected voltages. This saturation occurred at voltage settings that correspond to ion energies which are 2-3 times higher than what is expected from our RF plasma source. As a result, we suspect that the higher than expected measured current levels are a consequence of additionally generated charged species that also contribute to the ion damage in the sam ple. Accordingly, we expect a favorable operating condition, to potentially grow higher quality nitride-based materials, within the range of approximately 800-1000V.

4:30 PM

AA9, Improving Optical Properties of 1550-nm GaInNAs/GaAs Multiple Quantum Wells by GaInNAs Quaternary Barrier and Space Layer: *H. Y. Liu*[1]; M. Hopkinson[1]; P. Navaretti[1]; M. Gutiérrez[1]; J. S. Ng[1]; J. P.R. David[1]; H. D. Sun[2]; A. H. Clark[2]; M. D. Dawson[2]; [1]University of Sheffield, EPSRC Natl. Ctr. for III-V Tech., Dept. of Elect. & Elect. Engrg., Sheffield S1 3JD UK; [2]University of Strathclyde, Inst. of Photonics, 106 Rottenrow, Glasgow G4 0NW UK

The GaInNAs (GINA) semiconductors have recently attracted considerable attention due to their unique physical properties and potential application for the long-wavelength GaAs-based laser diodes operating in the 1300-1600 nm telecommunication-wavelength range. As a low N content is preferred, the operation wavelength of most devices so far reported utilizing GaInNAs/GaAs multiple quantum well (MQW) is still limited to around 1300 nm. Here, we present the 1550-nm GaInNAs/GaAs MQW heterostructures with GaNAs or GaInNAs barrier and space layer (BSL). The stronger improvement of photoluminescence efficiency has been observed with increasing N concentration in GaNAs BSL, instead of increasing N composition in GaInNAs QWs, to achieve room-temperature emission above 1500 nm for GaInNAs/GaNAs multiple QW structure, when the nitrogen concentration in GaInNAs QW is as high as 3%. However, the strain at the QW/BSL interface is accumulated by the increasing N concentration in GaNAs layer, possibly resulting in deteriorating the structural and optical properties. Consequently, the GINA quaternary BSL is finally proposed to reduce the strain at the QW/BSL interface. RT emission at 1560 nm with linewidth of 39.7 meV (15.7 meV at 10 K) was achieved from the sample with $Ga_{0.977}In_{0.023}N_{0.01}As_{0.99}$ quaternary BSL. The remarkable improvements of GINA QW optical characteristics are also revealed by detailed spectroscopic measurements including selectively excited photoluminescence (PL), temperature dependent PL, high-resolution XRD measurements and PL excitation (PLE) spectra. These results present to us a variable approach to further developing GaAs-based light sources in the telecommunication wavelength range near 1550 mm.

Session BB: Contacts to Wide Bandgap Semiconductors

Thursday PM Room: 155
June 24, 2004 Location: DeBartolo Hall

Session Chairs: Tae-Yeon Seong, Kwangju Institute of Science & Technology, Semiconductor Thin Film Lab., Puk-gu, Kwangju 500-712 Korea; Suzanne E. Mohney, Pennsylvania State University, University Park, PA 16802 USA

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BB1, Low Resistance Ohmic Contacts to Si Implanted GaN and Application in AlGaN/GaN HEMTs: *Haijiang Yu*[1]; Lee McCarthy[2]; Huili Xing[2]; Likun Shen[2]; Stacia Keller[2]; Steven P. DenBaars[1]; James S. Speck[1]; Umesh K. Mishra[2]; [1]University of California, Matls. Dept., Santa Barbara, CA 93106 USA; [2]University of California, ECE Dept., Santa Barbara, CA 93106 USA

Ultra-high temperature annealing (up to 1500°C) may be useful for the removal of implantation defects, dopant activation, dopant diffusion and defect annihilation in III-nitride materials. We report on ultra-low resistance ohmic contacts to Si implanted GaN and the incorporation of implantation into AlGaN/GaN HEMT processing. A rapid thermal annealing (RTA) approach capable of annealing 2 inch wafers at 1500°C with 100 bar nitrogen over-pressure was used to activate implanted Si dopants, after which a contact resistance of 0.02 Ω mm was measured using Transmission Line Measurements (TLM). Prototype Si implanted AlGaN/GaN HEMTs were also fabricated, with repeatable low resistance (0.1 Ω mm) alloyed ohmic contacts. Dopant activation experiments were performed on ~2.5 µm thick semi-insulating (Fe doped) GaN films grown by MOCVD on c-plane sapphire with typical sheet resistances of $7*10^{9}$ Ω /square. Si doses from $5*10^{14}$ to $1.5*10^{16}cm^{-2}$ were implanted at 100 keV. After a 60 second activation anneal at ~1500°C, with 100 Bar nitrogen overpressure and a ~ 100nm sputtered AlN capping layer, a sheet resistance of 13.9 Ω/square was obtained for a sample with a Si implantation dose of $7*10^{15}cm^{-2}$. X-Ray reciprocal lattice mapping indicated a nearly complete recovery from implant induced lattice distortion. SIMS measurements showed dopant redistribution with a diffusivity of $~7*10^{-14}cm^{2}\cdot sec^{-1}$ under these conditions. Ohmic contacts were depositied on the implanted GaN surface using a composite layer Ti/Al/Ni/Au scheme, with TLM measurements indicating an as-deposited contact resistance of 0.07 Ω mm. After a contact anneal (30 seconds at 870°C), the contact resistance dropped to a record low 0.02 Ω mm. These techniques enabled the incorporation of ion implantation into AlGaN/GaN HEMT processing. A thick (200 nm) GaN capped HEMT structure was adopted with source and drain regions implanted with Si, which was then activated using the annealing conditions described above. After contact annealing at 870 °C, a contact resistance of 0.1 Ω mm was reproducibly achieved. This ion implanted HEMT had comparable DC and pulsed DC performance as a control sample which was fabricated without implantation. Both samples were un-passivated and showed no RF-DC dispersion in a 200 ns pulsed IV measurement. In summary, we have demonstrated low resistance ohmic contacts to GaN using Si ion implantation and an ultra-high temperature activation anneal, enabling the demonstration of the successful incorporation of ion implantation into AlGaN/GaN HEMT processing. The combination of these techniques with the optimization of implanted device design and processing will aid in the realization of manufacturable ion-implanted AlGaN/GaN HEMTs with increased process control, repeatability, and performance. The work of H.Yu was supported by the JST ERATO program at UCSB, while L. M., H. X., L. S. and S. K. were supported by the U.S. DoD through grants from the AFOSR(G.Witt) and the ONR (H. Dietrich).

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BB2, Non-Polar GaN: p-Type Doping and Ohmic Contact Technology: *John Simon*[1]; Debdeep Jena[1]; Arpan Chakraborty[2]; Huili Xing[2]; Umesh K. Mishra[2]; [1]University of Notre Dame, Dept. of Elect. Engrg.,

275 Fitzpatrick, Notre Dame, IN 46556 USA; [2]University of California, Dept. of ECE, Santa Barbara, CA 93106 USA

Growth along non-polar directions of GaN has attracted considerable interest in recent years. Especially, a-plane growth is highly desirable to cure the reduction of optical oscillator strengths due to polarization-induced quantum-confined Stark effect in nitride quantum wells. All optical devices (emitters and detectors) need a controlled and conductive acceptor doped p-layers, and good ohmic contacts to these layers are crucial. So, controlled p-doping of a-plane GaN, and the ability to form reliable ohmic contacts to the p-doped layers is of high interest for many device applications. We present characterization of conductivity and ohmic contacts over a range of typical device operating temperatures on Mg-doped a-plane GaN grown by Metal-Organic Chemical Vapor Deposition (MOCVD). Mg-doped p-type nonpolar (11-20) a-plane GaN films were grown on (11-20) a-plane 6H-SiC substrates by MOCVD by depositing a high temperature AlN buffer layer prior to the epitaxial GaN growth. Pd/Au (20/1000nm) were used to make ohmic contacts with the p-GaN layer. Hall measurements yield a room temperature mobility of ~6cm^2/Vs and a mobile hole density of ~5e17/cm^3. The conductivity was ~0.5/ohm.cm. The sample was loaded in a temperature-controlled chuck and the temperature was varied over -60C < T < 200C. The measured conductance is seen to vary exponentially with temperature. We are able to extract an activation energy of E_A=108meV for Mg acceptors in a-plane GaN from our results, which is smaller than activation energy in the polar c-plane GaN (where the accepted value is E_A=160meV). The measured resistance on patterned TLM (Transfer Length Method) mesas made out of Au:Pd/GaN ohmic contacts of varying lengths revealed a remarkably linear current voltage characteristics over the temperature range of -60C<T<200C. The specific contact resistance at room temperature extracted from the TLM measurement was found to be 0.22ohm.cm^2. The contact resistance is seen to drop exponentially with temperature, which bodes well for high-temperature electronic and optical device applications. The favorable comparison of a-plane p-type doping and ohmic contact technology to those in c-plane GaN demonstrates that non-polar GaN can be readily used for large improvements in optical device performance. Quantum-well and superlattice based structures grown along non-polar directions can take advantage of the absence of the polarization fields and the simplicity of p-type doping and ohmic contact formation demonstrated in this work. This may be easily extended to applications in heterostructure bipolar transistors, where polarization results in induced charges in graded layers.

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BB3, Ir-Based Low Resistance Ohmic Contacts on p-GaN: *J. W. Bae*[1]; T. Hossain[1]; I. Adesida[1]; K. H. Bogart[2]; A. A. Allerman[2]; D. D. Koleske[2]; [1]University of Illinois, Micro & Nanotech. Lab. & Dept. of Elect. & Computer Engrg., 208 N. Wright St., Urbana, IL 61801 USA; [2]Sandia National Laboratories, Albuquerque, NM 87185 USA

Ohmic contact formation to $Al_xGa_{1-x}N$ is a critical issue in the fabrication of high performance short wavelength light emitting diodes and laser diodes. Obtaining excellent ohmic contacts on p-type $Al_xGa_{1-x}N$ continues to be a challenge. Various metallization schemes have been investigated as p-type contacts with Ni-based metallization being the most popular. As yet, most of these metallization schemes yield specific contact resistivities in the 10^{-4}-Ωcm^2 range. It is imperative to investigate other novel metals for contact applications on p-$Al_xGa_{1-x}N$ materials. We have investigated ohmic contact formation of Ir-based metallizations on p-type GaN. Specific metallization schemes of Ir/Au, Ir/Pd/Au, and Pd/Ir/Au were investigated on Mg-doped GaN grown by metal-organic chemical vapor deposition (MOCVD) with a carrier concentration of ~ 4.5 x 10^{17} cm^{-3}. The metals were deposited by evaporation and the samples annealed in an N_2 atmosphere at various temperatures in a rapid thermal anneal system. The as-deposited samples showed non-ohmic properties with specific contact resistivity of ~10^{-3}-Ωcm^2. However, all the samples exhibited ohmic characteristics at annealing temperatures between 400°C and 500°C. The Pd/Ir/Au sample annealed at 400°C for 1 min demonstrated the lowest ohmic contact resistivity of 2.87 x 10^{-5}-Ωcm^2 while it slightly increased to 4.42 x 10^{-5}-Ωcm^2 at 500°C. Auger electron spectroscopy (AES) depth profiles of annealed Ir/Pd/Au and Pd/Ir/Au showed intensive interdiffusion trend between Pd and Au, and the weak interfacial reaction between Pd and GaN surface. The low resistance is ascribed to the reactions and the formation of Pd-Au-Ga alloy observed by X-ray diffraction (XRD).

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BB4, Effects of Reactive Ion Plasma Treatment on Ohmic Contacts to n-GaN and n-$Al_{0.55}Ga_{0.45}N$: *Fitih M. Mohammed*[1]; Deepak Selvanathan[1]; Ilesanmi Adesida[1]; K. H. Bogart[2]; A. A. Allerman[2]; [1]University of Illinois, Micro & Nanotech. Lab., Urbana, IL 61801 USA; [2]Sandia National Laboratories, Albuquerque, NM 87185 USA

The versatility in the application of GaN in high temperature, high power and high frequency electronic devices, and short wavelength optoelectronic devices such as UV detectors, light emitting diodes (LEDs) and laser diodes (LDs) has engendered a significant amount of research activities. Consequently, considerable strides have been made in improving growth of epitaxial materials and device processing techniques. Realization of these useful applications, however, necessitates advances in the development of thermally stable and low resistance ohmic contacts to the GaN-based devices. To this end, various surface treatments, wet-etching and plasma induced dry-etching, schemes have been utilized to improve ohmic contacts to such devices. It has been previously shown, by Ping et al.,[1] that $SiCl_4$ pre-metallization plasma treatment in a reactive ion etching (RIE) plasma system improved the ohmic performance of Ti/Al contacts on n-GaN. It was shown that this treatment results in the creation of nitrogen vacancies and greater electron concentration at the surface of the n-GaN epilayer giving rise to reduced contact resistance. Several other reports are present in the literature on using Cl_2, H_2 and Ar plasma treatment to improve contact resistances on n-GaN. In this work, we have carried out a systematic study to compare the effectiveness of RIE plasma treatment of different gases, such as $SiCl_4$, BCl_3 and Cl_2, on the electrical characteristics of Ti/Al/Mo/Au ohmic contacts on n-GaN and n-$Al_{0.55}Ga_{0.45}N$. The effect of variation in plasma self-bias voltage is studied, and annealing temperature of the contacts is optimized to obtain reduced contact resistance. Contact resistances have been characterized using transmission line measurements (TLM). X-ray photoelectron spectroscopy (XPS) measurements are undertaken to identify the changes occurring on the surface chemical composition and stoichiometry after plasma treatment. The mechanism of ohmic contact formation and the effect of RIE plasma treatment on n-GaN and n-$Al_xGa_{1-x}N$ will be discussed. Effects of wet chemicals on the plasma-treated surfaces will also be discussed. [1]A.T. Ping, Q. Chen, J.W. Yang, M. Asif Khan, and I. Adesida, Journal of Electronic Materials, 27, 4 (1998).

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BB5, The Effect of Substrate Bias During Plasma Etching on Metal Contact Performance for High % Al n-AlGaN Thin Films and LEDs: *K. H.A. Bogart*[1]; A. J. Fischer[1]; A. A. Allerman[1]; D. D. Koleske[1]; [1]Sandia National Laboratories, Albuquerque, NM USA

Deep UV (<300 nm) AlGaN-based LEDs have important applications as UV light sources for chemical-biological sensors, non-line-of-sight optical communications, and UV curing. Optical emission below 300 nm requires A1 stoichiometry of >0.4. The difficulty of forming high-quality ohmic contacts to n-type AlGaN materials increases with increasing percent A1 due to the difficulty in effectively doping high %A1 AlGaN. LED processing requires plasma etching to access the n-type AlGaN for metal contacts. We have found that controlling plasma processing-induced damage to the n-type AlGaN is vital for good Ohmic metal contact performance. During the plasma etch, both chemical and physical processes occur in removal of substrate material. Physical sputtering from plasma ion bombardment is critical to break AI-N and Ga-N bonds as well as assist in desorption of etch products ($GaCl_x$, $AlCl_x$, x= 1-3). The substrate bias voltage (V_{dc}) is directly proportional to the energy of ions impinging on the material surface during etching, and high voltages can lead to material damage. We have observed contacts made to plasma-etched n-Al,Gal-, N (x = 0.45-0.50) that are non-Ohmic. It is well known in the literature that plasma etching of n-GaN creates nitrogen vacancies at the surface, thus increasing n-type carriers, and improving contact performance. However, there are no reports of improved contact performance for plasma-etched high %A1 (>40%) n-AlGaN. We investigated the effect of substrate bias (V_{dc}) on n-metal contact performance for high %A1 n-AlGaN. The n-contact performance on the n-level of processed deep UV LEDs as a function of (V_{dc}) was also determined. For n-Al,Gal., N (x = 0.45-0.50) etched at -250 V, we observed both non-linear and linear I-V curves, but with specific contact resistance (pc) values >1E-3 Ωcm^2 for the n-contact. Significant improvement in pc was observed for contacts to n-$Al_{0.46}Ga_{0.54}N$ etched with lower (V_{dc}), with pc ranging from 9.85E-5 to 1.11E-4 Ωcm^2 as (V_{dc}) varied between -50 and -1 50 V. All

contacts to n-AlGaN etched in this voltage range were as good as contacts to unetched n-AlGaN (9.95 ± 6.16E-5 Ωcm²). We determined that 825°C was the optimal anneal temperature between 800°C and 850°C, with the highest temperature starting to degrade pc. The n-contact performance was measured directly on fully processed 290 nm LEDs etched at -250 and -50 V, using circular TLM structures patterned on the etched n-level of the LED. Similar to the n-AlGaN films, we observed both non-linear and linear I-V curves with high pc (~1E-3 Ωcm²) values for LEDs etched at -250 V. For LEDs etched at -50 V, we measured pc = 3-7E-5 Ωcm². The effect of pre-metallization surface treatments using wet chemical (BOE and HCl) etching as well as surface analysis by XPS, performed before and after plasma etching, will also be discussed.

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BB6, Formation of Low Resistance Contacts to Digital Alloys of n-$Al_{0.7}Ga_{0.3}N$: *Jonshin Yun*[1]; Kisik Choi[1]; Kaveri Mathur[1]; Vladimir V. Kuryatkov[1]; Boris A. Borisov[1]; Gela Kipshidze[1]; Sergey A. Nikishin[1]; Henryk Temkin[1]; [1]Texas Tech University, Nano Tech Ctr./Elect. & Computer Engrg., Box 43102, MS-3102, Lubbock, TX 79409 USA

Large bandgap alloys of AlGaN are used in light emitting diodes emitting in deep ultraviolet[1]. Formation of low resistance Ohmic contacts on such alloys is made difficult by the presence of stable Al-surface oxides and relatively low electron levels achievable. We describe low resistance contacts to short period superlattices of $AlN/Al_{0.08}Ga_{0.92}N$ (digital alloys) replacing random alloys. With the 1.25-1.5 nm thick AlN barriers and 0.5-0.75 nm wells the average Al content in the digital alloy reaches x=0.7 and Eg= 5.1 eV. Digital alloys used in this work were grown by gas source molecular beam epitaxy with ammonia on sapphire substrates. The growth consisted of a nucleation layer of AlN, undoped insulating buffer layer of random alloy of $Al_{0.7}Ga_{0.3}N$, followed by 350 nm thick digital alloy with 200 well/barrier pairs. The structure was terminated with 2 nm thick $Al_{0.08}Ga_{0.92}N$. The digital alloy was uniformly doped with Si. Hall measurements show electron concentrations up to 2 x 10^{19} cm^{-3} with mobility of 10 cm^2/Vs. The quality of surface cleaning is critical to assuring low contact resistance. We use low energy electron diffraction to systematically monitor the effectiveness of cleaning procedures and, in particular, compare surfaces etched in HCl and HF. After a 10 min etch, at room temperature, surfaces produced by both etchants showed well defined diffraction spots at voltages as low as 45 V. This indicates high degree of surface perfection and cleanliness. However, surfaces produced in HF consistently show brighter and sharper spots, as expected from surfaces largely free of oxides or physisorbed contaminants. The superiority of HF is surprising since HCl produces better surfaces in GaN and our surface layer is chemically closer to GaN than to AlN. Similar observations were made previously on the basis of Auger experiments[2]. Full surface metal layers of Ti(20nm)/Al(100nm)/Ti(40)/Au(60) were prepared by e-gun evaporation at base pressures below 2 x 10^{-7} Torr. The metal stack was lithographically patterned and etched to form circular transmission line patterns. Lift-off techniques result in surface contamination and high contact resistance and were not used. Wafers were annealed after deposition, in nitrogen, at temperatures between 550°C and 800°C. The lowest specific contact resistance of r_c~1.2 x 10^{-4} Ωcm² was obtained for 700°C anneals. The contact resistance is limited by diffusion of Al into the semiconductor, through the Ti layer, and formation of surface oxides of Ti. The annealing does not change the structure of the digital $Al_{0.7}Ga_{0.3}N$ layer. This work is supported by DARPA-SUVOS, NSF (ECS-00700240, 0321186, 0304224, and 0323640), NATO SfP 974505, SBCCOM, and the J. F Maddox Foundation. [1]V. Kuryatkov et al. Appl. Phys. Lett. 83, 1319 (2003). [2]S. W. King et al. J. Appl. Phys. 84, 5248 (1998).

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BB7, Fabrication of Light Emitting Diodes Using Low Resistance and Highly Transparent Ni-La Solid Solution Ohmic Contacts to p-Type GaN: June-O Song[1]; Dong Seok Leem[1]; *Tae-Yeon Seong*[1]; J. S. Kwak[2]; O. H. Nam[2]; Y. Park[2]; [1]Kwangju Institute of Science and Technology, Matls. Sci. & Engrg., 1 Oryongdong Pukgu, Gwangju, Gwangju 500-712 S. Korea; [2]Samsung Advanced Institute of Technology, Photonics Lab., Suwon 440-600 S. Korea

GaN-based semiconductors are of significant importance for short-wavelength optoelectronic devices such as light emitting diodes (LEDs) and laser diodes (LDs). For advance of the performance these devices, the formation of high-quality ohmic contacts satisfying both electrical and optical properties simultaneously is essential. Until now, most of ohmic schemes to p-GaN have been reported to single, bilayer, or trilayer schemes, e.g., Pt, Ni/Au, and Pt/Ni/Au. However, these schemes have high specific contact resistances, resulting in poor device reliability. In this work, we report on low resistance and highly transparent ohmic contacts to p-type GaN (n_a = 5×10^{17} cm^{-3}) using Ni-La solid solution. The ohmic properties of the Ni-La solid solution-based contacts (e.g., Ni-La/Au, Ni-La/Pt, Ni-La/Pd schemes) are compared with those of Ni/Au contacts. It is shown that the specific contact resistances of ~10^{-5} and ~10^{-4} Ωcm² are obtained for the Ni-La solid solution-based contacts and Ni/Au contacts, respectively , when the samples are annealed at 530°C for 1 min in air ambient. It is further shown that for both the annealed samples, their transmittances at a wavelength of 450 nm are similar each other. To understand detailed ohmic formation mechanisms, electronic transport mechanisms and interfacial reactions are described and discussed by means of current-capacitance, current-voltage-temperature (I-V-T), Auger electron spectroscopy, X-ray photoelectron spectroscopy, and glancing X-ray diffraction measurements. Furthermore, light emitting diodes (LEDs) are fabricated using the Ni-La dsolid solution-based and Ni/Au contact layers. The typical I-V characteristics of the LEDs with the Ni-La solid solution-based p-contact layers exhibit a forward-bias voltage of about 3.5 V at injection current of 20 mA, which is better than that of the LEDs with the Ni/Au contact layer. The output power of the LEDs is also characterised and discussed.

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BB8, Low Resistance and Highly Reflective MIO/Ag-Based Ohmic Contacts to p-Type GaN for Flip-Chip Light Emitting Diodes: *June-O Song*[1]; Dong Seok Leem[1]; Tae-Yeon Seong[1]; J. S. Kwak[2]; O. H. Nam[2]; Y. Park[2]; [1]Kwangju Institute of Science and Technology, Matls. Sci. & Engrg., 1 Oryongdong Pukgu, Gwangju, Gwangju 500-712 S. Korea; [2]Samsung Advanced Institute of Technology, Photonics Lab., Suwon 440-600 S. Korea

For high brightness GaN-based light-emitting diode (LED) applications, the achievement of the high extraction quantum efficiency of such LEDs is crucial. It was shown that the high external efficiency of GaN-based LEDs could be realized by the introduction of the flip-chip (FC) configuration where emitted light is extracted through the sapphire rather than through a current spreading layer on the top of p-GaN. For FC configuration, LEDs should be fabricated using highly reflective metallization schemes, which act as both electrical contacts to the semiconductors and as optical reflectors. Silver (Ag) was considered as a good candidate metal for the fabrication of GaN-based FCLEDs. Non-alloyed silver contacts to p-GaN give good ohmic properties with contact resistivities of 10^{-2}-10^{-3} Ωcm². However, the Ag contacts suffer from some problems, such as relatively high contact resistivity, poor adhesion to GaN, and rapid degradation due to the agglomeration during annealing in air or oxygen ambient, resulting in poor device reliability. Thus, in this work, we investigate Mg-doped In2O (3 nm)/Ag (250 nm) and Mg-doped In2O (3 nm)/Ag (250 nm)/Ni (50 nm) schemes for the formation of low resistance and highly reflective ohmic contacts for FCLEDs, whose results are compared with that of Ag contacts. It is shown that annealing the samples at temperatures in the range 330-530ºC for 1 min in air ambient for results in specific contact resistances in the range of 10^{-4}-10^{-5} Ωcm². Furthermore, blue LEDs are fabricated using the oxidized Mg-doped In2O-based contact layers and are compared with those made with Ag single contacts. The typical I-V characteristics of the LEDs with the annealed Mg-doped In2O/Ag-based p-type contact layers give a forward-bias voltage of ~3.15 V at injection current of 20 mA, which is better than that of the LEDs with the Ag(200 nm) contact layers. The output powers of these LEDs made with different schemes are also characterised. To understand the improved ohmic behaviours and performances of LEDs with the Mg-doped In2O-based contact layers, thermal stability and interfacial reactions are characterised by means of scanning electron microscopy, Auger electron spectroscopy, X-ray photoelectron spectroscopy, and glancing X-ray diffraction measurements.

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BB9, Ohmic and Blocking Contacts to n-Type ZnO (0001) Epitaxial and Bulk Material: *Timothy E. Murphy*[1]; Willie E. Bowen[1]; Joseph O. Blaszczak[1]; Jamie D. Phillips[1]; [1]University of Michigan, EECS Dept., 1301 Beal Ave., 2417D EECS Bldg., Ann Arbor, MI 48109-2122 USA

Zinc oxide (ZnO) is a wide-bandgap II-VI compound semiconductor that is of interest for optoelectronic devices operating in the ultraviolet (UV) spectral region and for electronic devices requiring transparency, radiation hardness, or high temperature operation. The success of these devices depends on the ability to fabricate and understand electrical contacts. Semiconductor lasers and light emitting diodes require low contact resistance for efficient operation and long-operating lifetime. Schottky contacts are required for some UV detectors, transistor devices, and for materials characterization techniques including capacitance-voltage and deep level transient spectroscopy. In this work, we report on the investigation of a series of metal contacts on n-type ZnO (0001) substrates and ZnO (0001) thin films deposited on c-plane sapphire substrates. Undoped n-type bulk ZnO (0001) substrates were used for this study with resistivity >500 Ωcm, with a typical electron mobility of 150 cm^2/V-s measured by Hall effect measurements. Undoped or Al-doped ZnO (0001) thin films were deposited by pulsed laser deposition with thickness near 1 μm. X-ray diffraction measurements indicate highly c-axis oriented thin films. Hall effect measurements using the Van der Pauw technique show n-type behavior, with typical values of carrier concentration in the range of 10^{17} cm^{-3} and electron mobility greater than 40 cm^2/V-s. Ohmic behavior was observed with metals including Al and In, with contact resistance measured using a circular transmission line method (c-TLM). The dependence of contact resistivity on annealing will be reported, and contact resistivity values will be compared to previous reports for n-type ZnO.[1] Previously, Schottky barriers have been reported in literature [2-4] using metals such as Au, Ag, and Pd, where Schottky barrier heights are significantly lower than expected (0.6-0.8 eV) based on the workfunctions for these metals. In our experiments, blocking behavior is observed using metals with larger workfunctions such as Pt and Au, where successful Schottky diodes were only obtained for particular chemical surface preparation prior to contact metal deposition. The characteristics of these Schottky barrier contacts will be presented and discussed. This work was supported by the Office of the Vice President for Research at the University Of Michigan. [1]H. Kim, et al, J. Appl. Phys. 94, 4225 (2003), [2]H. Sheng, et al, Appl. Phys. Lett. 80, 2132 (2002), [3]A. Y. Polyakov, et al, Appl. Phys. Lett. 83, 1575 (2003),[4]H. von Wenckstern, et al, Appl. Phys. Lett. 84, 79 (2004).

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BB10, Ohmic Contact on Nitrogen-Doped UNCD Films and Observation of Conduction Band Offset Between UNCD and Si: *Ningyue Jiang*[1]; Zhenqiang Ma[1]; [1]University of Wisconsin, Elect. & Computer Engrg. Dept., 1415 Engineering Dr., Madison, WI 53706 USA

Diamond is a very promising candidate for high-speed and high power devices due to its superior material properties. Nitrogen-doped ultrananocrystalline diamond (UNCD) films grown by microwave plasma-enhanced chemical-vapor-deposition have shown n-type high conductivity. To investigate the contact behavior of metals deposited on n-type UNCD films, transfer length method (TLM) was used to measure the contact resistance between Au and nitrogen-doped (20% N2) UNCD films. The effect of rapid thermal annealing (RTA) on the contact resistance was also studied. For the first time, the conduction band offset between UNCD and Si heterojunction was revealed using current-voltage (I-V) measurement. A 200 Å-thick Ti barrier layer and 8000 Å- thick Au metal contact were deposited on UNCD films. TLM contact metal patterns were formed using standard lithography and liftoff technique. The TLM patterns consist of Au pads with different spacings inbetween. I-V characteristics were measured between adjacent two Au contacts. Consistent with previous work, good ohmic contacts were obtained between Au and nitrogen-doped UNCD films. The total resistance between two contacts with different spacings were extracted from the slope of the I-V curves and were then plotted as a function of the pad spacing. The contact resistance between metal and nitrogen-doped UNCD, the sheet resistance of the UNCD films and the transfer length were extracted from the slope and the interception points of the plot. At room temperature, the contact resistance between a 75x50 μm2 Au pad and nitrogen-doped UNCD film is measured to be 3.13 O, corresponding to a specific contact resistivity of 3474 O μm2. Rapid thermal annealings (RTA) at 400°C in nitrogen environment were applied to the sample for different time periods in order to minimize contact resistance between metal and UNCD films. It was found that the minimum contact resistance can be obtained after improving the interface quality between Au and UNCD film using RTA. To investigate the band alignment between UNCD/Si heterojunction, 10 mm2 Ti/Au (200 Å /5000 Å) contact pads were deposited on top of the nitrogen-doped UNCD film and on the bottom of the Si substrate. I-V measurement was performed between the top contact pad and the bottom contact pad over a range of temperatures. Based on the temperature dependence of the thermionic emission current J, the activation energy at different biases V can be obtained by extracting the slope of the Arrhenius plot (ln(J/(T2(exp(qV/kBT)-1))) versus 1/T). A conduction band offset △Ec = 0.3 eV between the UNCD/Si heterojunction was measured under zero applied bias. The conduction band offset observed between UNCD and Si heterojunction holds great promise for new Si-based heterostructure devices.

Session CC: Transport in Organic Semiconductor Device

Thursday PM June 24, 2004 — Room: 101 Location: DeBartolo Hall

Session Chairs: David J. Gundlach, ETH-Zurich, Zurich Switzerland; Paul Baude, 3M Company, St. Paul, MN 55114 USA

1:30 PM Invited

CC1, Intrinsic Charge Carrier Transport on the Surface of Organic Semiconductors: *V. Podzorov*[1]; M. E. Gershenson[1]; E. Menard[2]; J. A. Rogers[2]; V. C. Sundar[3]; J. Zaumseil[3]; [1]Rutgers University, 136 Frelinghuysen Rd., Piscataway, NJ 08854 USA; [2]University of Illinois, Urbana, IL 61801 USA; [3]Lucent Technologies, Bell Labs., 700 Mountain Ave., Murray Hill, NJ 07974 USA

This talk will describe the transport properties of high-mobility organic field-effect transistors (OFETs). Development of several innovative techniques[1-3] enabled fabrication of the single-crystal OFETs with high charge carrier mobilities (up to 20 cm^2/Vs at room temperature). Intrinsic, not dominated by static disorder transport of the electric-field-induced polaronic carriers has been realized on the organic surface over a wide temperature range. Various aspects of the charge transport in these devices, including the temperature dependence of the mobility, mobility anisotropy and charge trapping will be discussed. [1]V. Podzorov et al., Appl. Phys. Lett. 82, 1739 (2003). [2]V. Podzorov et al., Appl. Phys. Lett. 83, 3504 (2003). [3]V. C. Sundar et al., Science 303, 1644 (2004).

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CC2, Fabrication and Characterization of Single-Crystal Organic Field Effect Transistors: *Christopher R. Newman*[1]; Reid J. Chesterfield[1]; Jeffrey A. Merlo[1]; C. Daniel Frisbie[1]; [1]University of Minnesota, Chem. Engrg., Matls. Sci., 421 Washington Ave. SE, 151 Amundson Hall, Minneapolis, MN 55455 USA

Molecular organic semiconductors in the oligoacene and oligothiophene families show great promise as low-cost alternatives to amorphous silicon in applications such as light-emitting diodes, flexible displays and smart cards. Although room temperature mobilities in excess of 1 cm2 V-1 s-1 have been demonstrated in thermally deposited thin films of molecules such as pentacene, transport in these films is inevitably affected (if not completely governed) by issues associated with the film microstructure. Due to the inherent difficulty of fabricating devices on fragile organic single crystals, little is known about the intrinsic charge transport mechanisms in these materials. We have successfully fabricated single-crystal organic field-effect transistors (SX-OFETs) from single crystals of molecules from both families via two techniques: 1) The application of free-standing organic crystals to prefabricated Si/SiO2 transistor structures and 2) The assembly of the transistor structure on top of the organic single crystal using CVD-deposition of the polymeric dielectric parylene. Variable-temperature measurements on these devices allow us to investigate the underlying charge transport mechanisms. We report on the observation of characteristics that in some cases deviate significantly from measurements made on polycrystalline thin films of the same materials.

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CC3, Intrinsic Hole Mobility and Temperature-Dependent Trapping in a Regio-Regular Poly(Thiophene): *Alberto Salleo*[1]; Armin R. Voelkel[1]; Tze Wee Chen[2]; Michael L. Chabinyc[1]; Robert A. Street[1]; [1]Palo Alto Research Center, 3333 Coyote Hill Rd., Palo Alto, CA 94304 USA; [2]Stanford University, Dept. of Elect. Engrg., Palo Alto, CA 94305 USA

Charge transport in organic thin-film transistors (TFTs) is limited by trapping. In addition, charge trapping that leads to bias stress (i.e. a shift of the threshold voltage of the device) has an obvious influence on the material parameters extracted from device characteristics. Device characteristics measured as a function of temperature are useful to understand charge transport and trapping mechanisms in semiconductors. We measured the temperature dependence of the mobility of a high performance regio-regular poly(thiophene). The room temperature mobility of this material is approximately 0.1 cm^2/V.s. Quasi-static measurements indicate that near 250K the mobility is non-monotonic with temperature, in contrast with conventional hopping models. Moreover, in the same temperature range quasi-static measurements are significantly different than measurements obtained with a pulsed gate signal. This anomaly can be explained by a trapping mechanism particular to polymer semiconductors. Recent studies of bias-stress effects in regio-regular poly(thiophene) TFTs indicated that hole pairs forming self-trapped bipolarons are responsible for at least one component of the bias-stress effect. In order to improve our understanding of the mechanism of hole capture, and the reverse dissociation of the bipolarons, the kinetics and temperature dependence of trapping were measured. The mobility anomaly is explained as resulting from the counteracting effects of the increasing equilibrium concentration of bipolarons, but the increasing time needed to reach equilibrium. A semi-quantitative kinetic model of bipolaron formation agrees well with the experimental results and provides an estimate of the binding energy of the bipolaron (~120 meV). Trapping at defects limits the room-temperature mobility of the regio-regular poly(thiophene). Modification of polymer processing conditions led to varying degrees of order in the polymeric film and caused the room-temperature mobility to vary over almost a factor of a hundred (0.1 cm^2/V.s to 0.004 cm^2/V.s). In an effort to determine the trap-free (=intrinsic) mobility of the regio-regular poly(thiophene), we correlated the gate dependence of the mobility with its temperature dependence for all our films. The field-effect mobility is thermally activated in all films at T<200 K and that the activation energy depends on the charge density. The experimental data agrees well with a multiple trapping and release model. The differences in room-temperature mobility are essentially due to different widths of the shallow donor distribution at the edge of the valence band due to structural disorder in the film. The intrinsic mobility of the mobile states in the ordered regions of the film is the same in all the films and is estimated to be between 1 and 10 cm^2/V.s.

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CC4, Field Effect in Pentacene Single-Crystal/Sio_2/Doped-Si Structures: *J. Takeya*[1]; C. Goldmann[2]; C. Krellner[2]; S. Haas[2]; K. P. Pernstich[2]; B. Batlogg[2]; T. Nishikawa[3]; T. Takenobu[4]; S. Kobayashi[4]; T. Shimoda[3]; T. Mitani[5]; Y. Iwasa[4]; [1]CRIEPI, 2-11-1, Iwado-kita, Komae, Tokyo 201-8511 Japan; [2]ETH, Lab. for Solid State Physics, Hoenggerberg, Zuerich CH-8093 Switzerland; [3]Seiko Epson, Co. Japan; [4]Tohoku University, IMR, Sendai Japan; [5]JAIST Japan

We report results of recently improved four-probe transconductance measurements down to ~ 100 K and the effects of self-assembled monolayers (SAMs) bonded to the SiO2 for single crystal organic field-effect transistors (OFETs). Since pentacene thin films deposited on SiO2/doped-Si substrates are the best studied OFET for practical use, the single-crystal devices of the same structure is useful as a reference, for example to extract intrinsic field-effect properties of the organic material, avoiding complications from grain boundaries and ambiguity in the extent of molecular ordering. For this purpose, we fabricated OFETs by placing thin pentacene single crystals onto SiO2/doped-Si substrates patterned with source-drain electrodes.[1] The OFETs show steep field-effect switching comparable to amorphous-Si MOS devices and mobility (~ 0.5 cm2/Vs) as large as high-quality organic thin-film transistors. At low temperatures down to 180 K, the mobility remains almost unchanged, while the hysteris observed in the drain current-gate voltage sweep is greatly suppressed. Coating the surface of SiO2 with SAMs before the deposition of organic materials is a known technique to improve the interface in the thin-film devices.[2] Recently, it turned out that even switching gate voltage can be controlled by choosing materials among various elongated silane molecules with the appropriate electron affinities.[3] In order again to avoid extrinsic influences from grain boundaries or contacts to source and drain electrodes, we have prepared pentacene single-crystal devices incorporating methyl-terminated and fluoro-terminated SAMs, and measured the transconductance by the four-terminal technique sweeping the gate voltages. The switching gate voltage reproducibly shifted by +20 V when methyl-terminated SAMs are replaced by fluoro-terminated SAMs. The result clearly demonstrates that the difference in the switching voltages comes from the pentacene crystals, indicating additional holes are induced with fluoro-terminated silanes due to the large electron affinity. [1]J. Takeya, C. Goldmann, S. Haas, K. P. Pernstich, B. Ketterer, and B. Batlogg, J. Appl. Phys., 94, 5800 (2003). [2]D. J. Gundlach, L.-L. Jia, and T. N. Jackson, IEEE Electron Device Lett. 22, 571 (2001). [3]S. Kobayashi, T. Nishikawa, T. Takenobu, S. Mori, T. Shimoda, T. Mitani, and Y. Iwasa, preprint; K. P. Pernstich, private communication.

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CC5, A New Model for an Organic Field-Effect Transistor: *Tae-Ho Jung*[1]; Ananth Dodabalapur[1]; [1]University of Texas, ECE, Microelect. Rsch. Ctr., Austin, TX 78758 USA

Organic thin film transistors are getting more attractions as new materials with higher mobility and easy process. We are developing a numerical model for simulating the response of an organic FET (OFET), to which less attention has been paid whereas analytical modeling of the materials and transistor is actively being carried out. There are many commercially available simulation tools such as MEDICI and PADRE, but they have been developed for simulating inorganic semiconductor device in which charge injection and transport are different from those in organic materials. There have been some reports on simulation characteristics of OFETs,[1-2] but the transport related issues have not been focused well in the bottom contact structure,[3-4] which is suitable for manufacturing. Our model deals with the bottom contact structure and includes physical models and application environments that are often necessary for an accurate description of OFETs. For comparison and reference purposes, we also model an OFET using MEDICI, which provides a reasonable description of the basic behavior of an OFET. In our model we implemented the multigrid finite difference method, whereas MEDICI uses the finite element method, which has advantages over the former except intensive computational complexity. However, regular rectangle representation in the finite difference method helps to easily define subregions inside a device and assign their own characteristics to model grain boundary effects and mobility variation along the channel. With the multigrid mesh structure dielectric interface region in which charges are accumulated less than one or two monolayer(s) according to the experimental results[2] can be inspected in more detail than other less important regions accelerating simulation process. In OFETs, the mobility is influenced by several factors such as parallel and perpendicular electric fields, carrier density, and grain boundary trapping. In many cases, a high contact resistance at the electrode and semiconductor interface caused by highly disordered molecules is a feature in the bottom contact structure. We assumed that the mobility in the vicinity of the electrode contact is lower than the other channel regions and this property is being modeled in the simulation tool. More complex mobility/carrier transport profiles are easily implemented with our model. [1]Y. Roichman et al., Appl. Phys. Lett. 79, 2987, 2002. [2]M. A. Alam et al., IEEE Trans. Elect. Dev. 44, 1332, 1997. [3]Deem MJ et al., IEEE Trans. Elect. Dev, 48, 1688, 2001. [4]Kanicki J et al., J. Elect. Mater. 31, 512, 2002.

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CC6, Alq and TPD Static Induction Transistor with Organic Semiconductors: *Serkan Zorba*[1]; Yongli Gao[1]; [1]University of Rochester, Physics & Astron., Rochester, NY 14627 USA

We have fabricated and studied static induction transistors (SITs) with various organic semiconductor materials, such as pentacene, perylene, tris(quinoline-8-hydroxylate)aluminum (Alq), and N,N'-di(4-methylphenyl)-N,N'-diphenylbenzidine (TPD), used as the active element. The former two resulted in unsuccessful operation due to a short caused by pinholes formed in the films. Modification of the deposition rates did not change the outcome. The latter two provided successful operation. No fatal pinholes were observed in the thin films of the latter two. In addition, Alq, normally an electron transporting material, has

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been shown to transport holes in a SIT structure. Our results indicate that if smoother and well-ordered organic thin films are fabricated, and right workfunction metals are used as the electrodes, organic SITs will be viable driving components for active matrix organic light emitting diodes (OLEDs) and other flexible opto-electronic devices.

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CC7, Contact Resistance in Pentacene Organic Thin-Film Transistors: *Paul V. Pesavento*[1]; Reid J. Chesterfield[1]; Christopher R. Newman[1]; C. Daniel Frisbie[1]; [1]University of Minnesota, Chem. Engrg. & Matls. Sci., 421 Washington Ave. SE, Amundson Hall, Minneapolis, MN 55455 USA

Contact resistances have been shown to be an important factor in organic thin-film transistor (OTFT) operation. For the researcher looking to accurately tune device properties through alterations in film processing, measured variations in device properties that are actually due to contact resistance changes could give rise to incorrect conclusions. Therefore, to better understand these effects, we describe gated four-probe measurements designed to probe contact resistance and mobilities via observed potential drops at source and drain electrodes in pentacene-based OTFTs. The devices consist of conventional top contact (inverted-staggered geometry) source and drain electrodes contacting a pentacene film deposited on a dielectric/gate electrode assembly. Two top contact, voltage sensing leads penetrate into the source-drain channel and are used to monitor potentials in the pentacene film while it is passing current during varying drain voltage (VD) or gate voltage (VG) biases. Gated four-probe measurements also allow field-effect mobilities for pentacene films to be corrected for the measured potential drops at the contacts. Specifically, we investigate contact resistance and device mobility as a function of contact metallurgy, gate bias dependence, substrate dielectric, and temperature.

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CC8, Fa Electron Currents in Submicron Pentacene Transistors: *J. Jo*[1]; J. J. Heremans[1]; F. Bradbury[1]; Hong Chen[1]; V. Soghomonian[1]; [1]Ohio University, Dept. of Physics & Astron., (on leave from Ajou University, Korea), Clippinger Labs., Athens, OH 45701 USA

Many organic semiconductors show p-type characteristics. Yet, electron transport in organic semiconductors is important for complementary circuits. The difficulties associated with electron transport result from high electron trap densities, short electron lifetimes, and high injection barriers. To observe electron transport in the organic semiconductor pentacene, we utilized submicron organic field effect transistor (OFET) structures. Short channels indeed provide stronger electric fields, aiding electron injection, and enable electrons to traverse the channel despite recombination and trapping. OFETs with 0.8 micron channel lengths were fabricated on Si/SiO2 substrates. Au contacts were used as source and drain, the p+ Si substrate as gate. Pentacene was deposited in a 10^-6 torr vacuum chamber, on an octadecyltrichlorosilane (OTS) treated surface. The asymmetric structure of our devices yields different electric field strengths at source and drain. When the contact with the higher electric field is used as a negatively biased drain electrode, we observed a drain current increase at positive gate voltages (20 V), indicating electron transport in the channel. When the contact with the weaker field is negatively biased, the devices show a current decrease at positive gate voltage, indicating p-type behavior. The results indicate that ambipolar behavior can be observed in submicron channel length OFETs. The slope of current-voltage characteristics on a log-log scale reveals that the devices operate in the space charge limited current regime. At positive gate voltages, the slope of the current increases, an indication of increased trapping of injected electrons rather than holes. These results complement observations on long-channel devices, where strong electron trapping precludes n-type behavior. The currents in our devices also demonstrate a strong dependence on oxygen doping (p-type in pentacene). After a week of exposure to air, the currents show diode-like behavior, upon varying the (drain) voltage at the high electric field contact. In this mode, a current ratio of 20:1 was observed between +20 V and -20 V drain voltage. The same experiment at the weak-field contact yields a ratio of 3. This indicates that the electron injection ability of the high-field contact was reduced by oxygen doping. As the oxygen doping increases the p-type nature of the channel, the height of electron injection barrier is concomitantly increased, and the current decreases. Our experimental results show that electron traps play an important role in realizing electron currents in pentacene OFETs. Electron traps need to be satisfied to obtain electron currents. In a long channel device, the distance precludes filling of the electron traps. In our short-channel devices, the electron traps approach saturation, and larger electron currents can be observed.

Session DD: Narrow Bandgap Devices and Materials

Thursday PM June 24, 2004 — Room: 129 — Location: DeBartolo Hall

Session Chairs: Robert M. Biefeld, Sandia National Laboratories, Albuquerque, NM 87185-0601 USA; Christine A. Wang, Massachusetts Institute of Technology, Lincoln Lab., Lexington, MA 02420-9108 USA

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DD1, High Quality InSb Photodiodes Structures Grown by MOVPE: *Ariel Sher*[1]; Yossi Paltiel[1]; Arie Raizman[1]; Sergey Shusterman[1]; Moti Katz[1]; Avigdor Zussman[1]; [1]Soreq NRC, Electro-Optics, Yavne 81800 Israel

In the recent years there is an increasing interest in InSb homo-epitaxial layer structure, growth and doping, enabling p^+-n-n^+ photodiodes to be fabricated. With this approach, the properties of each layer can be optimized separately by changing the growth parameters, yielding photodiodes with relatively low dark currents and high values of the zero biased junction area resistance (R_0A). These parameters are essential for the realization of high quality focal plan arrays (FPA) infrared (IR) detectors. Large format arrays of IR detectors with background limited performance up to 100K, based on p^+-n-n^+ MBE layer structures, were recently demonstrated[1]. Using metalorganic vapor phase epitaxy (MOVPE) as an alternative growth technique of the InSb layer structure is of great interest due to several potential production advantages. Yet, the progress towards high quality InSb photo-diodes grown by MOVPE was hampered by some inherent difficulties in the MOVPE growth of this compound. Recently we reported[2] on our results of InSb p^+-n-n^+ layer structures grown by MOVPE on InSb substrates. The photo-diodes fabricated on these structures exhibited very low dark currents and R_0A values as high as $8x10^5\Omega cm^2$ at 80K, comparable with the most recent published results for MBE grown structures. In this presentation we describe the details of the MOVPE growth procedures and show the results of the epilayers characterization. The MOVPE layer structures were grown by employing Thomas Swan vertical reactor with growth temperature of 465°C and rector pressure of 400 Torr. The conventional trimethyl reagents of indium and antimony were used . Best results, in terms of crystalline quality, were achieved by growing the structures on (100) orientated substrates with 2 degrees off towards (111). Special precautions were taken to control the actual Sb/In very close to 1, preventing either indium droplets or antimony solid precipitates. Excellent uniform crystalline quality was revealed by double crystal diffractometer (DCD) X-ray mapping.The growth rate of the whole structure was ~2µm/h. The thicknesses of the bottom layer, the active layer and the p^+ layer were 1µm, 2.5µm and 0.5µm, respectively. For p type doping of the upper layer we used zinc with diethylzinc as the metalorganic source. Sulphor hydride was the n type dopant of the bottom layer while the active layer was grown intentionally undoped. It should be noted that the evaluation of the carrier concentration in each layer is quite problematic as the substrates are fairly conductive. For the undoped active layer we used capacity-voltage (C-V) measurements of the diodes to extract carrier concentration. The p-type layer could be characterized by by Hall effect measurements, when a zinc doped layer was grown either directly on InSb substrate with a low doping level or on the unoped layer. The carrier concentration of the bottom n+ layer was derived from the Moss-Burstein shift of the PL spectra. The electrically active doping levels in the photodiode structures thus estimated as $2x10^{17}cm^{-3}$, $2x10^{15}cm^{-3}$ and $3x10^{17}cm^{-3}$ for the p^+, n and n^+, respectively. The zinc and sulphor distri-

bution in the three layer structures was confirmed by secondary ion mass spectroscopy (SIMS) measurements. Correlation of the epilayers characteristics with the photodiodes performance will be discussed. [1]Tim Ashley et al. Proc. SPIE 4820 400-405 (2002); [2]Y. Paltiel et al, submitted, (2003).

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DD2, MBE Growth of 6.2 Å InAsSb High Electron Mobility Transistors: *Brad P. Tinkham*[1]; Brian R. Bennett[1]; J. Brad Boos[1]; Richard Magno[1]; [1]Naval Research Laboratory, Elect. Tech. Div., Code 6876, 4555 Overlook Ave., Washington, DC 20375 USA

AlSb/InAs-based high electron mobility transistors (HEMTs) have been developed for use in devices demanding both low power consumption and high speed. In order to obtain even better performance, we have developed the MBE growth of high-mobility random-alloy InAsSb channels for use in place of InAs. The 6.2 Å lattice-constant $AlSb/InAs_{0.7}Sb_{0.3}$ HEMT possesses the desired type I band alignment. The existence of hole barriers on both sides of the quantum well enables the improved confinement of holes which are generated thermally or as a result of impact ionization in the channel. As a result, leakage currents are expected to be reduced compared to the AlSb/InAs system with a staggered type-II heterojunction band lineup. Our InAsSb channels were grown as random alloys (simultaneous As and Sb fluxes). This represents a change from the previous approach where the InAsSb channel was grown as a short-period superlattice [Boos et. al. Electr. Lett. 35, p. 847, 1999]. Using the random alloy, we have achieved 300K mobilities over 22,000 cm^2/Vs with a 2D sheet carrier density of $1.4 \times 10^{12} cm^{-2}$. This represents a marked improvement over the short-period-superlattice InAsSb-channel HEMT samples with mobilities of 13,000 cm^2/Vs for the same carrier density. For high-frequency performance, HEMTs need to be on a semi-insulating (SI) substrate. Since no SI substrates exist at 6.1 Å - 6.2 Å, thick buffer layers are typically grown on GaAs or InP to provide the proper lattice constant for 2D epitaxial growth. Most work on the InAs/AlSb HEMTs utilizes AlSb buffer layers and therefore the InAs quantum well is pseudomorphic with respect to relaxed AlSb (6.1355Å). It is apparent that the transport and leakage current properties of the HEMT can be affected by the magnitude and sign of the strain in the channel as well as the roughness and dislocation density at the InAsSb/AlSb interfaces. We have experimented with larger lattice constant 6.2 Å InAlSb and InAlAsSb buffer layers. To further move towards a 6.2Å structure that is stable in air, we have also grown structures that replace AlSb barrier material for the quantum wells with $In_{0.2}Al_{0.8}Sb$. The transport properties of all the variations of the InAsSb/AlSb HEMT will be discussed. All of these structures are modulation doped with Te resulting in 2D doping densities between 5×10^{11} and 5×10^{12} cm^{-2}. Variable-field Hall measurements and self-consistent bandstructure calculations have been performed to understand the effects of the Te modulation doping of AlSb on the 2DEG carrier concentration and mobility of the InAsSb channel.

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DD3, Effects of Buffer Layers on the Structural and Electronic Properties of InSb Films: *Xiaojun Weng*[1]; N. G. Rudawski[1]; D. L. Partin[2]; J. P. Heremans[2]; Rachel S. Goldman[1]; [1]University of Michigan, Matls. Sci. & Engrg., 2300 Hayward St., Ann Arbor, MI 48109-2136 USA; [2]Delphi Research and Development Center, Warren, MI 48090-9055 USA

Due to its low bandgap and high electron mobility, InSb is useful for a variety of device applications including long wavelength light sources and magnetoresistive sensors. InSb films are generally grown on GaAs substrates, with a 14.6% lattice mismatch which results in a high density of threading dislocations. In earlier work, we showed that electron scattering from the strain field associated with threading dislocations is the primary mobility-limiting mechanism in highly mismatched InSb films.[1] The electron mobility of InSb films increases with the film thickness due to the decrease of threading dislocation density. Recently, highly mismatched resistive buffers such as InAlSb showed promise for increasing the electron mobility of thin InSb films.[2,3] However, the effects of buffers on the evolution of threading dislocations and electron mobility are not well understood. Therefore, we have investigated the structural and electronic properties of n-doped InSb films grown on low-misfit GaSb, high-misfit InAlSb, and step-graded GaSb+InAlSb buffers. We find a significant decrease in room-temperature electron mobility of InSb films grown on the low-misfit buffers, and a significant increase in room-temperature electron mobility of InSb films grown on the high-misfit or step-graded buffers, in comparison with those grown directly on GaAs. Plan-view transmission electron microscopy (TEM) indicates a significant increase in threading dislocation density for InSb films grown on the low-misfit buffers, and a significant decrease in threading dislocation density for InSb films grown on the high-misfit or step-graded buffers, in comparison with those grown directly on GaAs. Cross-sectional TEM reveals the role of the film/buffer interfaces in the filtering and nucleation of threading dislocations for the high-misfit and low-misfit buffers, respectively. A quantitative analysis of electron mobility and carrier concentration dependence on threading dislocation density suggests that electron scattering from the lattice dilation associated with threading dislocations has a stronger effect on electron mobility than electron scattering from the depletion potential surrounding the dislocations. Furthermore, while lattice dilation is the predominant mobility-limiting factor in these n-doped InSb films, ionized impurity scattering associated with dopants also plays a role in limiting the electron mobility. [1]X. Weng, R.S. Goldman, D.L. Partin, and J.P. Heremans, J. Appl. Phys. 88, 6276 (2000). [2]D.L. Partin, J. Heremans, and C.M. Thrush, J. Vac. Sci. Technol. B 17, 1267 (1999). [3]R.M. Biefeld and J.D. Phillips, J. Cryst. Growth 209, 567 (2000).

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DD4, Zn Doping of p-Type GaAsSb from Spin-On Glass Dopant Sources: *Shishir Rai*[1]; P. Fay[1]; B. Han[2]; N. Pan[2]; [1]University of Notre Dame, Dept. of Elect. Engrg., 275 Fitzpatrick Hall, Notre Dame, IN 46556 USA; [2]MicroLink Devices, 6457 Howard St., Niles, IL 60714 USA

The first study of p-type doping in $GaAs_{0.51}Sb_{0.49}$ lattice-matched to InP from Zn spin-on glass sources is reported. Diffusion from spin-on sources has been shown to be considerably simpler to implement than ampoule-based approaches,[1] since the spin-on film serves both to cap the surface to prevent out-diffusion of the group-V elements as well as to supply the dopants. We have obtained shallow diffusion profiles suitable for aggressively-scaled heterojunction devices, and good electronic transport properties in the doped films have been observed. Potential applications for spin-on doping of p-type GaAsSb includes the optimization of low-resistance base contacts and extrinsic base regions in GaAsSb/InP HBTs (e.g.[2]) for ultra-high-speed applications, without the use of regrowth or other complex processing. Diffusions were carried out in a rapid thermal processor (RTP), using epitaxial heterostructures consisting of 200 nm of p-type GaAsSb grown on semi-insulating InP by MOCVD. Diffusion into epitaxial structures with carbon background doping concentrations of 1.9×10^{16} cm^{-3} and 1×10^{18} cm^{-3} (measured by Hall effect) were studied. Although the carbon doping levels in these structures are low compared to typical HBT base doping levels, these structures were intentionally selected to clearly show the effect of post-growth Zn incorporation from the spin-on diffusants. Diffusions were carried out at temperatures from 350-600 °C and durations of up to 30 minutes. SIMS depth profiling indicates that Zn starts to diffuse into GaAsSb layer at temperatures as low as 350°C, forming very shallow diffusion profiles with a measured diffusion depth of 11 nm for a 5 minute diffusion. For higher temperatures, increased diffusion depths were obtained as expected, with a depth of 50 nm obtained for a 500°C, 5 min diffusion. The Zn appears to remain largely electrically inactive for diffusions at temperatures below 500°C, as indicated by Hall-effect measurements. The threshold temperature at which Zn becomes electrically active is found to be in the range of 500-550°C. Hall effect measurements indicate that the average hole concentration increased by three orders of magnitude for the lowest-doped test structure, rising from 1.9×10^{16} cm^{-3} to 2×10^{19} cm^{-3} for a 30 min, 600°C diffusion. The measured sheet resistance decreased from 280 kΩ/sq to 910 Ω/sq., while the hole mobility was reduced from 58.6 cm^2/Vs as grown to 26.5 cm^2/Vs due to increased impurity scattering. The diffusion rate was found to increase with as-grown background doping concentration; for the lightly-doped epitaxial material, a 15 min 600°C diffusion resulted in an average hole concentration of 8.6×10^{18} cm^{-3}, while diffusion into material with a 1×10^{18} cm^{-3} background C concentration resulted in a hole concentration of 1.9×10^{19} cm^{-3} for the same diffusion conditions. [1]Y. C. Lu et al., J. Electronic Materials, vol. 19, no. 1, pp. 29-34, 1990. [2]C. R. Bolognesi et al., IEEE Trans. Electron Devices, vol. 48, no. 11, pp. 2631-2639, 2001.

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DD5, Low Resistance Ohmic Contacts on p-GaAsSb: *J. H. Jang*[1]; H. K. Cho[2]; J. W. Bae[2]; I. Adesida[2]; N. Pan[3]; [1]Kwangju Institute of Science

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and Technology, Dept. of Info. & Communications, 1 Oryong-dong Puk-ku, Kwangju 500-712 S. Korea; [2]University of Ilinois, Dept. of Elect. & Computer Engrg. & Micro & Nanotech. Lab., 208 N. Wright St., Urbana, IL 61801 USA; [3]Microlink Devices, 6457 Howard St., Niles, IL 60714 USA

Gallium arsenide antimonide (GaAsSb) is receiving much attention for applications in the area of high-speed optoelectronic devices such as double heterojunction bipolar transistors (DHBTs) and photodetectors. Compared with indium gallium arsenide lattice-matched to InP substrates which is widely used for these device applications, $GaAs_{0.5}Sb_{0.5}$ has similar bandgap energy, but it forms a type-II heterojunction with InP so that there is no potential barrier impeding carrier transport across the base-collector junction in GaAsSb/InP DHBTs employing GaAsSb as a base material. In the fabrication of DHBTs, it is cardinal to realize excellent ohmic contacts on p-GaAsSb utilized for base layer of DHBTs because parasitic resistance should be kept as low as possible. By laterally scaling base contact layer, the base-collector junction area can be scaled down to achieve very small collector and emitter junction area ratio (A_c/A_e~2). To realize super-scaled HBTs, it is imperative to find excellent base metallization schemes with short transfer length as well as low contact resistance. Carbon-doped GaAsSb ($5x10^{19}cm^{-3}$) whose thickness is 500 nm was grown utilizing metal organic chemical vapor deposition (MOCVD). Hole mobility was measured to be ~ 40 cm^2/Vs despite the high carbon doping concentration. Multilayer metallization schemes including Pd/Au, Pd/Ir/Au, Pd/Pt/Au contacts have been deposited and lifted-off to fabricate TLM (transfer length method) test patterns which was utilized to obtain electrical characteristics of ohmic contacts. Pd was selected for the bottom metallization because it reacts with semiconductors easily. Novel metals such as Pt and Ir with high work functions were utilized as the metal on the Pd layer which help to form good ohmic contact resistance under annealed conditions. The thickness of Au capping layer had effect on optimum annealing condition as well as ohmic contact properties. Two different thicknesses of Au, 15 nm and 150 nm were utilized to study the effect of the thickness of Au capping layer. To further enhance the thermal properties of these ohmic contacts, metallization schemes including Mo as a diffusion barrier were also fabricated and characterized. With the addition of Mo, thermal stability was improved. X-ray photoelectron spectroscopy study was carried out to investigate interactions between the multilayer metallizations and ternary GaAsSb compound semiconductor. The electrical characteristics of ohmic contacts were compared for the above metallization schemes under annealing temperatures ranging from 250°C to 450°C. Excellent ohmic contacts exhibiting a specific contact resistivity less than 10^{-8} Ω-cm^2} and a transfer length of less than 100 nm were achieved. These results exceed the required specifications for the base ohmic contact resistance for super-scaled DHBTs with sub-micron emitter widths.

3:10 PM Break

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DD6, Interwell Excitonic Effect in GaNAs/GaAsSb Type-II Active Regions for Long Wavelength Operation: *Hyunsoo Yang*[1]; Vincenzo Lordi[1]; James S. Harris[1]; [1]Stanford University, Solid States & Photonics Lab., CISX126, Via Ortega, Stanford, CA 94305 USA

The major limitation for rapid expansion of optical metro area networks (MANs) is availability of low cost 1.3-1.55µm devices that can operate over a significant temperature range with moderate power. Due to the well-established processing technology and a superior DBR mirror technology, there have been several types of quantum structures grown on GaAs substrate such as GaInNAs(Sb) QWs, GaAsSb QWs, and (Ga)InAs QDs. Another approach, in addition to the above type I structures, utilizes type II QWs such as GaInAs/GaAsSb. We present a new type II active region comprised of GaNAs/GaAsSb QWs. To demonstrate this new alloy, two samples were grown by molecular beam epitaxy (MBE) using a N radio frequency plasma cell on SI GaAs substrates. One sample consists of $GaAs_{0.975}N_{0.025}$ (6nm)/$GaAs_{0.9}Sb_{0.1}$ (16nm) 9QWs located in the intrinsic region of a p-i-n diode, while the other has 6QWs of $GaAs_{0.97}N_{0.03}$ (6nm)/$GaAs_{0.84}Sb_{0.16}$ (20nm). Photocurrent spectra with different bias across the p-i-n diode were taken using phase-sensitive detection. Light from a halogen lamp was passed through a monochromator and then focused on an optical window in the p-contact. Relatively small excitonic resonance and absolute absorption intensity are the result of the separation between electrons and holes in the different QW layers. Due to outdiffusion from in-situ annealing during the p-layer growth and residual N gas after closing shutter, the band diagram effectively changes, which enables the carriers to be more separated. Therefore the quantum-confined Stark effect is not clear with increased reverse bias. This interwell exciton effect can be simulated using a small exciton binding energy (<4meV), where the spectra do not have the abrupt rising characteristic similar to the indirect bandgap absorption. However, it is expected that employing 2-4nm well thicknesses would result in the enhanced electron-hole wavefunction overlaps. Some advantages of the GaNAs/GaAsSb type II configuration compared to GaInAs/GaAsSb include better carrier confinement, strain compensation, and a constant growth temperature. In general, ternary materials are expected to have better quality than quaternary materials due to reduced alloy scattering. In addition, spatial separation of In (or Sb) and N by the type II structure could improve the optical quality. In conclusion, we have developed a new material of GaNAs/GaAsSb for long wavelength optoelectronics. With the optimization of the well thickness and growth condition, higher absorption and light emission would be possible.

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DD7, Measurements of Recombination Rates in Low-Doped Epitaxial GaInAsSb Lattice-Matched to GaSb by Frequency Response of Photoluminescence: *D. Donetsky*[1]; S. Anikeev[1]; G. Belenky[1]; S. Luryi[1]; C. A. Wang[2]; D. A. Shiau[2]; M. Dashiell[3]; J. Beausang[3]; G. Nichols[3]; [1]State University of New York, Elect. & Computer Engrg., Stony Brook, NY 11794 USA; [2]Massachusetts Institute of Technology, Lincoln Lab., Lexington, MA 02420 USA; [3]Lockheed Martin Corporation, Schenectady, NY 12301 USA

Time-resolved photoluminescence (TRPL) is a standard method for minority carrier lifetime measurements in III-V compounds. Determination of electron lifetime in p-doped epitaxial GaInAsSb from PL kinetics after pulsed excitation was reported earlier. This material finds application in a variety of mid-infrared optoelectronic devices including thermophotovoltaic (TPV) energy cells. Knowledge of minority carrier lifetime is important for modeling of TPV devices. Use of TRPL method in undoped structures with background doping p ~ 10^{16} cm^{-3} is complicated due to requirement on low-injection condition ($\Delta n << p$). This work reports on utilization of PL frequency response for measurements of electron lifetime. In this case use of a narrow-band amplifier and sinusoidal modulation of the excitation source allows lifetime measurements with static injection level below 10^{15} cm^{-3}. In principle static and dynamic lifetimes can be different. Measurement under static excitation corresponds better to TPV device operating conditions. 0.54-eV GaInAsSb double heterostructures were grown by organometallic vapor phase epitaxy (OMVPE) on GaSb substrates. The confinement of excess carriers was provided with AlGaAsSb or GaSb cap layers. This paper will discuss the carrier recombination mechanisms in GaInAsSb/AlGaAsSb grown by OMVPE.

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DD8, Auger and Radiative Recombination Parameters in 0.55 eV InGaAsSb: *Ravi J. Kumar*[1]; Ronald J. Gutmann[1]; Jose M. Borrego[1]; Partha S. Dutta[1]; Christine A. Wang[2]; Gregory Nichols[3]; [1]Rensselaer Polytechnic Institute, Ctr. for Integrated Elect., CII-6015, 110 8th St., Troy, NY 12180 USA; [2]Massachusetts Institute of Technology, Lincoln Lab., Lexington, MA 02420 USA; [3]Lockheed Martin, Schenectady, NY 12301 USA

Antimonide-based materials are promising candidates for thermophotovoltaic (TPV) cells, infrared lasers and photodetectors. Minority carrier lifetime is a critical parameter which determines the performance of these devices. Radio-Frequency (RF) photoreflectance measurements and one-dimensional device simulations have been used to determine bulk and surface recombination parameters in epitaxially grown 0.50 to 0.60 eV InGaAsSb. The RF photoreflectance technique senses changes in sample conductivity as carriers recombine following excitation by a laser pulse. A one-dimensional device simulation tool is used to model the sheet conductance transient response to above-bandgap optical excitation. When sample decay times are extracted from the RF photoreflectance measurements, the recombination parameters can be obtained by matching the transient decay times from the simulations with the measured decay times. Measurements and analysis on 2 x 10^{17} cm^{-3} doped 0.55 eV p-InGaAsSb active layers with variable capping layers give SRVs of ~ 680 cm/s for 2 x 10^{17} cm^{-3} doped AlGaAsSb capping layers, ~ 1350 cm/s for 2 x 10^{18} cm^{-3} p-GaSb capping layers, and ~ 5000 cm/s for undoped GaSb capping layers. The 2 x 10^{17} cm^{-3} doped samples

have a low-level bulk lifetime of 80 to 100 ns. A higher bandgap and higher doping concentration in the capping layer are most effective in reducing SRV. Radiative and Auger coefficients compatible with the measured decay time of a sample can be obtained after removing the contribution of Shockley-Read-Hall (SRH) and surface lifetimes from the measured decay time. The experimental decay times observed with 2 x 10^{17} cm^{-3} doped samples during the low-level injection region of the decay transients are compatible with an Auger coefficient (C) ~ 1 x 10^{-28} cm^6/s and a radiative coefficient (B) ~ 3 x 10^{-11} cm^3/s. The Auger and radiative recombination coefficients obtained from high-level injection decay times show very good agreement with values obtained from low-level injection conditions. Combining the uncertainties in parameter extraction for the various samples evaluated, a radiative recombination coefficient (B) of 3 ± 1.5 x 10^{-11} cm^3/s and Auger coefficient (C) of 1 ± 0.5 x 10^{-28} cm^6/s is obtained for 0.55 eV InGaAsSb lattice matched to GaSb.

Session EE: Epitaxy for Devices

Friday AM — Room: 102
June 25, 2004 — Location: DeBartolo Hall

Session Chairs: Chuck Lutz, Kopin Corporation, Tauton, MA 02780 USA; Janet L. Pan, Yale University, New Haven, CT 06520 USA

8:20 AM Student

EE1, Recombination Lifetime and Internal Quantum Efficiency in Gallium Arsenide Doped Beyond N_A=1x10^{19}: *Thomas D. Boone*[1]; Jerry M. Woodall[1]; [1]Yale University, Elect. Engrg. & Applied Sci., PO Box 208284, New Haven, CT 06520 USA

Device performance characteristics are often limited by the minority carrier recombination lifetime (e.g., modulation bandwidth of light emitting diodes, the current gain of bipolar transistors, etc.). Previously it has been demonstrated that by increasing the semiconductor hole concentration with doping, the electron recombination lifetime is reduced [Nelson & Sobers, 1976]. Light emitting diode (LED) 3 dB modulation bandwidths greater than 1.7 GHz have been achieved in GaAs by increasing the active region doping concentration beyond N_A > 7x10^{19} [Chen, 1999]. However, compared to more moderately doped devices with smaller modulation bandwidths (< 500 MHz), the photonic output efficiency of these heavily doped devices is reduced considerably [Chen, 1999]. Typically, it has been suggested that non-radiative Auger recombination results in the inefficient luminescence observed at higher doping levels [Ahrenkiel,2000]. Here it is presented that this mechanism alone fails to accurately explain the low internal quantum efficiencies. A new model is proposed suggesting that the minimum spontaneous emission lifetime significantly influences the internal quantum efficiency in the 1x10^{19}-1x10^{20} p-type doping regime [Dumke, 1963]. A theoretical model of recombination is introduced that utilizes the maximum transition probability of the semiconductor coupled with an approximate k-space spectral distribution encountered by free carriers. The model appears to resolve the contradiction between photonic efficiency and lifetime observed at larger doping levels. The model is compared with recent experimental results, as well as several previously reported studies. Analysis suggests that higher modulation bandwidths can be achieved by LEDs with larger bandgap active regions. R.J. Nelson and R.G. Sobers, "Minority-carrier lifetime and internal quantum efficiency of surface-free GaAs" Journal-of-Applied-Physics, v.49, n.12; pp.6103-6108, Dec. 1978. C.H. Chen, M. Hargis, J.M. Woodall, and M.R. Melloch, "GHz Bandwidth GaAs Light-emitting Diodes", Applied Physics Letters, v.74, n.21, pp. 3140-3142, Mar. 1999. R. K. Ahrenkiel, R. Ellingson, and W. Metzger D. I. Lubyshev and W. K. Liu, "Auger Recombination in Heavily Carbon-doped GaAs," Applied Physics Letters, v.78, n.13, 2001. W. Dumke "Optical Transitions Involving Impurities in Semiconductors," Physical Review, v.132, n.5, p.1998, July 1963.

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EE2, Photoluminescence Due to Be-As_{Ga} Complex in Low-Temperature MBE-Grown Be-doped GaAs: Akira Higuchi[1]; *Hiroyuki Bando*[1]; Hiroshi Okamoto[1]; Tsuyoshi Okuno[2]; Yasuaki Masumoto[2]; [1]Chiba University, Dept. of Matls. Tech., 1-33 Yayoi-cho, Inage-ku, Chiba, Chiba 263-8522 Japan; [2]University of Tsukuba, Inst. of Physics, Ibaraki, Tsukuba 305-8571 Japan

Low-temperature (LT) MBE grown beryllium (Be) doped GaAs shows optical absorption saturation characteristic with subpicosecond recovery time and is very attractive to applications to all optical switches and saturable absorption mirrors.[1-4] We recently demonstrated that such ultrahigh speed dynamics was realized not only at the band edge but also at the photon energy higher than Eg by 200 meV or more.[5] This ultrahigh speed carrier dynamics is supposed due to recombination of photogenerated electrons and holes through complexes formed by Be^- acceptors and antisite arsenic donors As_{Ga} $^+$, although not confirmed experimentally up to now. Controversy arose recently from a report that electronic states due to such complexes were not observed by a scanning tunneling microscope.[6] In this report we studied photoluminescence (PL) characteristic of LT-grown Be-doped GaAs, found a broad PL peak at around 0.8eV and measured its dynamics at 77K or below. PL for a standard temperature (Tg = 560°C) grown Be-doped GaAs and LT-grown (Tg = 350, 310°C) non-doped and Be-doped (Be concentration was 2x$10^{19}$$cm^{-3}$) GaAs epiwafers (1 micrometer thick) were measured at 77K by using a photomultiplier tube with sensitivity up to 1.7 micrometers wavelength and response speed of 1ns. PL at the bandedge was not observed for any LT-grown samples, and PL centered at 1.6 micrometers with broad spectrum ($\Delta\lambda$ ~200nm) was observed only for LT-grown Be-doped samples. Its intensity decreased with decreasing the growth temperature Tg but increased by increasing Be concentration. Therefore it can be ascribed to the Be^--As_{Ga}^+ complex. This deep level PL intensity increased with lowering the temperature with an activation energy of about 0.6 eV. Temporal change of the PL was measured by exciting with optical pulses whose duration was 30ns. Signal from the photomultiplier was detected by a digital sampling oscilloscope with 4,000 times accumulation for improving the SN ratio. Response time was 120ns at 30K and it decreases as increasing the sample temperature with an activation energy of 0.6eV. The response time extrapolated to 300K was estimated to 1ps or less. These results demonstrate experimentally that the carrier recombination through the Be^--As_{Ga} $^+$ complex includes both radiative process and nonradiative one, and the effective recombination time is ultrafast at room temperature. [1]S. Gupta et al., IEEE J. Quantum Electron. 28, 2464, (1992). [2]R. Takahashi et al., Appl. Phys. Lett. 65, 1790, (1994). [3]M. Haiml et al., Appl. Phys. Lett. 74, 1269, (1999). [4]T. Okuno et al., Appl. Phys. Lett., 79, 764 (2001). [5]T. Okuno et al., Jpn. J. Appl. Phys. 41, L745, (2002). [6]B.Grandidier et al., Appl. Phys. Lett. 74, 1439, (1999).

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EE3, Gallium-Arsenide Deep-Level Materials for THz and 1.5um Fiber-Optic Applications: *Janet L. Pan*[1]; [1]Yale University, Dept. of Elect. Engrg., 15 Prospect St., Rm. 505, New Haven, CT 06511 USA

We utilize semiconductor deep-centers to make possible novel materials for THz applications and 1.5um fiber-optic emitters on GaAs. We demonstrate the first[1] GaAs light-emitting-diode (LED) emitting at 1.5um fiber-optic wavelengths from arsenic-antisite deep-levels. This is an enabling technology for 1.5um fiber-optic components lattice-matched to GaAs ICs. We demonstrate experimental results for significant internal optical power (24mW), efficiency (0.6%), and speed (THz) from GaAs deep-level optical emitters. We also demonstrate the first tunnel diodes utilizing deep-levels in low-temperature-grown (LTG) GaAs. At room temperature, our peak current density (16kA/cm2) is the largest ever in GaAs tunnel diodes. Our devices also show room-temperature peak-to-valley current ratios as high as 22. We ascertain the transport mechanisms which limit the peak and valley currents. Finally, we present the first fully-analytical eight-band model[2,3] of the deep-center wave function. (e.g., symmetry and admixture of atomic orbitals). The deep-center wave function determines the general optical properties of deep-centers (optical selection-rules and transition strengths) in terms of simple materials parameters (bandgap energy, Kane dipole, deep-level position) and angular momenta quantum numbers. This model is applicable in a wide variety of materials, and is in agreement with experiment. JLP thanks J. Woodall for his MBE, and the NSF. [1]J. L. Pan et al. Gallium-Arsenide Deep-Level Optical-Emitter for Fiber-Optics. Nature Materials, 2 (6),

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375-378, (June 2003); advance online publication, 4 May 2003 (doi:10.1038/nmat887); [2]J. L.Pan, Optical emission from bound states of semiconductor deep-centers. Opt. Exp. 9, 796-805, (2001); [3]J. L. Pan, Analytical method for finding the general optical properties of semiconductor deep centers. J. Appl. Phys. 92, 5991-6004, (2002).

9:20 AM Student

EE4, Compensation of Interfacial Charges at the Regrowth Interface Between InP Layers: *Yingda Dong*[1]; Arthur C. Gossard[1]; Mark J.W. Rodwell[1]; [1]University of California, Elect. & Computer Engrg. Dept., Santa Barbara, CA 93106 USA

In SiGe bipolar junction transistors (BJTs), selectively implanted collector (SIC) is widely used to reduce the extrinsic base-collector capacitance and limit the base width. In InP heterojunction bipolar transistors (HBTs), a similar technique can be applied with the selective implantation in an undoped collector pedestal layer followed by subsequent MBE regrowth of the HBT structure. Using this technique, the total collector depletion thickness in the HBT's extrinsic region can be much larger than that in the intrinsic region, thus significantly reducing the extrinsic base-collector capacitance. In our experiments, it has been found that the extrinsic base-collector region could not be fully depleted until a high reverse bias voltage higher (>2V) was applied across the base-collector junction. Capacitance-voltage measurements showed an n-type sheet charge accumulation on the regrowth interface between the undoped InP collector pedestal layer and the lightly Si-doped InP collector layer. To study the origin of this sheet charge accumulation at the regrowth interface, a series of samples were subjected to different processes, including UV ozone treatment, HF etch, as well as extended phosphorous annealing in the MBE chamber before the regrowth. The impurities at the regrowth interface were subsequently analyzed by secondary ion mass spectrometry (SIMS). As expected, among these samples significant but highly variable carbon and oxygen concentrations were found at the regrowth interface. For all these samples, experiencing a variety of surface treatments, the interfacial accumulation charge densities nevertheless were relatively constant, varying only between $1.6x10^{12}$ cm^{-2} and $1.9x10^{12}$ cm^{-2}. This result suggested that the absorption of impurities of carbon or oxygen was not the origin of the interfacial charge accumulation. SIMS analysis also showed that there was no Si accumulation at the regrowth interface. It is therefore believed that the n-type charge accumulation may arise from states associated with disorder at the regrowth interface. These states, as were similarly observed with InP surface states, could pin the Fermi-level close to the conduction band. Although we have been unable to eliminate the interfacial states associated with regrowth, we here report suppression of the associated charge accumulation by a compensating delta-doping. If the n-type interfacial charge accumulation is compensated by an additional p-doped layer at the regrowth interface, the net background charge concentration of the regrown layer is reduced, and full p-n junction depletion can then be obtained at a low reverse bias voltage. A thin layer of carbon-doped InGaAs was first grown on the regrowth interface prior to the growth of the n- InP collector layer. C-V measurements showed that with this p-doped compensating layer inserted, the 2000Å collector pedestal layer was fully depleted at a reverse bias less than 0.5V. Compensation with Be-doped InP layer was also investigated, but interfacial charge reduction was not consistently obtained, possibly due to the formation of Be-O complexes on the regrowth interface, which made the Be dopants electrically inactive.

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EE5, Intersubband Emission from MBE-Grown InGaAs-AlAsSb Quantum Cascade Structures Spanning the λ~3-5µm Atmospheric Window: *Matthew J. Steer*[1]; Dmitry G. Revin[2]; Luke R. Wilson[2]; Evgeny A. Zibik[2]; Richard P. Green[2]; John W. Cockburn[2]; Robert J. Airey[1]; Mark Hopkinson[1]; [1]University of Sheffield, EPSRC Natl. Ctr. for III-V Tech., Mappin Bldg., Mappin St., Sheffield, S. Yorkshire S1 3JD UK; [2]University of Sheffield, Dept. of Physics & Astron., Hounsfield Rd., Sheffield, S. Yorkshire S3 7RH UK

There is currently significant interest in the development of high-performance intersubband quantum cascade lasers (QCLs) for operation in the technologically significant λ~3-5µm atmospheric window region. The ultimate limit on short wavelength QCL operation is set by the depth of the quantum wells in the laser active region, i.e. the conduction band offset ($\triangle E_c$) of the heterostructure materials system used. Although strain-compensated InGaAs/AlInAs/InP ($\triangle E_c$ <~700meV) QCLs have been demonstrated at wavelengths down to 3.6µm, the performance of these devices is markedly inferior to that of △>5µm QCLs. Consequently, there is strong motivation to extend the QCL concept to new materials systems with the highest possible $\triangle E_c$. In this paper, we report the first successful operation of intersubband quantum cascade structures based on $In_{0.53}Ga_{0.47}As$-$AlAs_{0.56}Sb_{0.44}$. This heterostructure system, which is lattice matched to InP, is very promising for high performance QCL development, since it combines a very large conduction band discontinuity (~1.6eV) with complete compatibility with well established InP-based QCL waveguide design and fabrication technology. However, due to the very high complexity of QCL design, and the stringent demands placed on layer thickness control and uniformity, extension to new materials systems presents considerable challenges. This is especially true for InGaAs/AlAsSb where significant difficulties exist in controlling the nature of the interfaces and overcoming problems associated with the large miscibility gap of AlAsSb. We have studied a range of $In_{0.53}Ga_{0.47}As$-$AlAs_{0.56}Sb_{0.44}$ quantum cascade structures designed to produce intersubband emission between 3-5µm. Cross-sectional transmission electron microscope (TEM) images were used to assess the well and barrier thicknesses and long-range uniformity of the crystal growth. Well defined AlAsSb layers are observed even for the thinnest (6Å) barriers. All structures display clear intersubband electroluminescence peaks close to the design wavelengths, with full widths at half maximum in the range ~23-51meV. In order to verify that the emission is due to intersubband transitions we have measured the emitted power as a function of polarization angle. The signal is found to be dominantly polarized perpendicular to the plane of the quantum well layers (0º), proving conclusively the intersubband nature of the electroluminescence peaks. Of particular note is that the λ~3.1µm electroluminescence we observe is the shortest wavelength emis sion observed from any intersubband device to date. The electrical characteristics of the samples are as robust as similar InGaAs-InAlAs QC structures that we have measured. In our devices we measure a linear L-I characteristic, indicating good injection efficiency with negligible variation over the investigated current range. In addition, the optical powers measured are similar to those we have previously measured when developing GaAs- and InP based QC lasers, indicating that laser operation in the λ~3-5µm atmospheric window should be possible with the addition of established waveguide cladding layers.

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EE6, The Sequential LPE and MBE of InAs on GaP - A Hybrid Form of MBE: *An Chen*[1]; Aristo Yulius[1]; Jerry M. Woodall[1]; [1]Yale University, Elect. Engrg., 15 Prospect St., PO Box 208284, New Haven, CT 06511 USA

Device quality InAs can be grown on GaP substrates by MBE. For example, InAs/GaP Schottky diodes made by MBE exhibit nearly ideal Schottky diode characteristics.[1] Also, these diodes were found to be more stable than metal/GaP diodes at high temperature, owing to the suppression of the inter-diffusion across interfaces in large lattice-mismatched semiconductor systems.[2] Direct band gap InGaP has a better figure-of-merit than GaP for power rectifiers.[3] Therefore, we have studied the growth of InAs on InGaP lattice-matched to GaAs. Unfortunately, "normal" MBE of InAs on InGaP resulted in heterojunctions that were leaky. Therefore, we carried out experiments to address the issue of why the direct growth of InAs on InGaP resulted in leaky diodes. Our experiments showed that a critical issue was the interface formation mechanism during high temperature growth. For epilayer perfection reasons, an In-rich condition is used to grow InAs on GaP (and for InAs on InGaP). Adding excess In onto the GaP surface creates an In-Ga liquid alloy composition that is undersaturated with respect to liquid-solid phase equilibrium in the In-Ga-P phase diagram. This undersaturation is relieved at high growth temperatures by the dissolution of GaP into the liquid In until pseudo-equilibrium is reached with the GaP substrate. When an As flux is added to this liquid, growth of an InxGa1-xPyAs1-y layer graded in composition occurs at the GaP interface until the InAs composition is reached. Therefore, instead of forming an abrupt interface, a compositionally graded layer forms at the InAs/GaP interface during a high-temperature growth. We have confirmed the presence of the interface layer by HRTEM. The graded layer growth mechanism is similar to the isothermal solution mixing growth associated with the LPE of Ga1-xAlxAs.[4] The graded interface layer explains the resistive, ohmic

characteristics in the InAs/InGaP heterojunction grown at high temperature. Thus, low temperature growth can turn off the LPE components and allow normal MBE to form an abrupt interface. To test this theory, we grew InAs on InGaP in MBE at both high and low temperatures. The InAs/InGaP heterojunction grown at 250°C showed nearly ideal Schottky rectifying characteristics, but the sample grown at 500°C was ohmic-like, as expected from the theory. An ideality factor of 1.06 and a barrier height of 0.8eV were achieved in the low-temperature InAs/InGaP heterojunction rectifier. The breakdown electrical field was 0.5MV/cm without any edge-termination technique employed. The rectifier also demonstrated excellent thermal stability, similar to the InAs/GaP heterojunction. After baking in a rapid thermal annealer (RTA), the InAs/InGaP heterojunction maintains rectifying characteristics up to 700°C. [1]E.H. Chen, T.P. Chin, J.M. Woodall, and M.S. Lundstrom, J. Appl. Phys. 70, 1551 (1997). [2]J.J. Jeon, Ph.D. dissertation, Purdue University, 2001. [3]K.J. Schoen, E.S. Harmon, J.M. Woodall and T.P. Chin, J. Appl. Phys. 71, 518 (1997). [4]J.M. Woodall, J. Electrochem. Soc. 118, 150 (1971).

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EE7, Growth of CaF_2/Si/CaF_2 Resonant-Tunneling Structures by B and Sb Surfactant-Enhanced Epitaxy: Cunrang Wang[1]; Bernhard H. Mueller[1]; Markus Bierkandt[1]; Eberhard Bugiel[1]; Tobias Wietler[1]; *Karl R. Hofmann*[1]; [1]University of Hannover, Inst. for Semiconductor Devices & Elect. Matls., Appelstr. 11A, 30167 Hannover Germany

CaF_2/Si insulator-semiconductor heterostructures are highly attractive for silicon-based nanoelectronic devices such as CaF_2/Si/CaF_2 resonant-tunneling diodes. The realization of these devices requires the growth of ultra-thin (3-5 ML) CaF_2 barrier layers on Si, both on the substrate and on the Si quantum-well (QW), and of 8-12 ML Si quantum-well layers on CaF_2, which should all be atomically flat with abrupt interfaces and a minimum of defects. Growth of CaF_2 on Si (111) substrates has been extensively studied, and high-quality, atomically flat CaF_2 films on have been achieved.[1] The epitaxial growth of Si on CaF_2/Si(111) is more difficult to achieve because the smaller surface free energy of CaF_2 makes wetting of the CaF_2 surface with Si energetically very unfavorable. We have shown that by using surfactant-enhanced solid-phase epitaxy with the surfactants Sb or B continuous, smooth and epitaxial crystalline Si-QW films on CaF_2/Si(111) substrates with a clear sqrt(3) x sqrt(3) reconstruction can be obtained.[2] But a new challenge arises for the subsequent deposition of a high-quality CaF_2 barrier layer on top of such Si-QW epilayer films, because the presence of the surfactants Sb and B atoms can alter the surface properties of the Si epilayer hindering the bonding of the CaF_2 molecules to the Si surface atoms. Therefore, they may change the CaF_2 growth mechanisms as compared to the direct growth on the Si(111) substrate. We found a significant difference in the growth of CaF_2 layers on Si-QW layers that were formed by Sb and B surfactant-enhanced epitaxy. On Si epilayers produced with the surfactant Sb, a tendency towards 3D cluster formation of CaF_2 was observed. In contrast, with the surfactant B used in the Si epitaxy, relatively flat CaF_2 layers were obtained. A possible reason is that in the latter case F atoms released by the dissociation of CaF_2 form BF_x species that evaporate from the surface, resulting in a direct bond between Ca and Si atoms at the CaF_2/Si interface as in the case of CaF_2 growth on Si(111) substrates without surfactant. Thus we have utilized B surfactant-enhanced epitaxy for the fabrication of CaF_2/Si/CaF_2 double-barrier resonant-tunneling diodes. These diodes exhibited I-V characteristics with negative differential resistance which were much more stable and had 7 to 2 orders of magnitude higher peak current densities (up to ~0.5 A/cm^2) at 77 K than earlier CaF_2/Si/CaF_2 resonant-tunneling diodes.[3] [1]Thin Solid Films, 410, p. 72 (2002); [2]Appl. Surf. Sci., 211, p. 203 (2003); [3]IEEE Trans. on Nanotechnology, 2(4), (2003).

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EE8, Molecular Beam Epitaxial Growth of Cd-Based II-VI Wide-Band-Gap Compounds on Si: Yuanping Chen[1]; *Gregory N. Brill*[1]; Paul M. Amirtharaj[1]; Nibir K. Dhar[1]; [1]Army Research Laboratory, AMSRD-ARL-SE-EI, 2800 Powder Mill Rd., Adelphi, MD 20874 USA

Cd- and Zn-based II-VI wide-band-gap compound semiconductors have tremendous applications for various opto-electronic devices as well as x-ray and gamma-ray detectors. These compounds, especially Zn-based compounds were initially grown on GaAs substrates to mitigate issues related to the lattice mismatch between the epilayer and the underlying substrate. However, the most desirable situation is to grow high quality Cd- and Zn-based II-VI wide-band-gap compound semiconductors directly on Si substrates to take advantage of mature Si technology for electronic processing. Additionally, besides their applications as opto-electronic devices or x-ray/gamma-ray detectors, Cd-based binary compounds grown on Si, such as CdTe/Si, have been used as composite substrates for HgCdTe material, an infrared detecting semiconductor system. Likewise, ternary alloys, such as CdZnTe/Si and CdSeTe/Si, as well as quaternary compound, such as CdZnSeTe/Si can also be used as composite substrates that are specifically engineered to lattice match with HgCdTe material designed to detect in the long wavelength (LWIR, 8 - 12 micron) IR region. When the concentration of Zn and/or Se is carefully chosen, the composite substrate can lattice match to LWIR HgCdTe, which can minimize the dislocations generated at epilayer-composite substrate interface. Of these ternary and quaternary alloys, each has unique crystalline characteristics as result of cation mixing, anion mixing or balanced cation and anion mixing. We have carried out a detailed study on the MBE growth of Cd-based compounds on Si substrates. For the CdSeTe ternary alloy, the composition of Se was varied from 0 to 1 to study the crystalline properties. In this paper we will present our detailed study of molecular beam epitaxial growth and characteristics of CdSeTe, CdZnSeTe and CdSe on Si(211), such as crystal structure, fundamental bandgap measurements, surface morphology, defect and dislocation density. For structural characterization, we used TEM and x-ray diffraction. The alloy composition was measured by electron dispersive spectroscopy and x-ray diffraction. Photoreflectance (PR) was utilized to measure the optical response in the near bandgap (Eg) region. Cubic Cd1-xSexTe grown on Si(211) with $0 < x < 1$ has been obtained. Results show a large bowing of the bandgap as a function of composition. The large bowing suggests a breakdown of the virtual crystal approximation (VCA) and long-range non-random ordering of the crystal. For the quaternary Cd1-xZnxSeyTe1-y compound, the surface morphology of the epilayer is observed to be very sensitive to Zn concentration, with smoother surfaces obtained as Zn content is decreased. This result agrees with our previous finding that the surface morphology of CdSeTe is superior to that of CdZnTe grown on Si(211).

11:20 AM Student

EE9, Epitaxial Growth of $FeSi_{2-x}Ge_x$: Towards a Tunable Silicon Based Electro-Optic Material: *Ryan J. Cottier*[1]; Brian P. Gorman[1]; Fatima Z. Amir[1]; A. Glen Birdwell[2]; O. Wayne Holland[1]; Arup Neogi[1]; Chris L. Littler[1]; Terry D. Golding[1]; [1]University of North Texas, Physics Dept., 211 Ave. A, Denton, TX 76203 USA; [2]MEMC Electronic Materials, 6800 Hwy. 75 S., Sherman, TX 75090 USA

Iron disilicide shows great promise as a silicon based light emitter and detector operating in the 1.3 to 1.5 µm wavelength range. However, there exist a number of questions related to the exact nature of the band structure, and various optical studies have indicated both a direct and indirect bandgap. Full implementation of this material for electro-optical applications will require the ability to tailor the bandgap to permit the synthesis of heterostructure based devices. One possible approach is to alloy the material with Ge, which is expected to reduce the bandgap as well as introduce the possibility of bandgap engineering through strain and compositional effects. Previous studies have shown small amounts of Ge (2-3%) incorporated into β-$FeSi_2$ reduces the bandgap from 0.87 eV to a direct gap of 0.83 eV.[1] As part of an investigation into the optical properties of semiconducting silicides and related systems, a series of $FeSi_{2-x}Ge_x$ samples have been prepared by molecular beam epitaxy over a range of compositions (x). This is accomplished by epitaxial co-deposition of atomic Fe, Ge, and Si onto Si(100)and Si(111) wafers. In this paper we will present results of optical absorption, photoreflectance (PR), and X-ray diffraction (XRD) studies on these samples. Optical absorption and PR is used to determine both the type (direct or indirect) and energy of the alloy bandgaps, and XRD is employed to characterize phase, strain and microstructure. We will discuss our results in relation to the ability to synthesize across the alloy range and trends in the $FeSi_{2-x}Ge_x$ bandgap with x. Implications for use of the material system in next generation emitters and detectors will be discussed. This work is supported by the Advanced Technology Program of the State of Texas and the Office of Naval Research. [1]H. Chen, P. Han, X. D. Huang, L. Q. Hu, Y. Shi, and Y. D. Zheng, Appl. Phys. Lett. 69(13), 1912 (1996).

Session FF: Defects in SiC

Friday AM June 25, 2004 | Room: 141 Location: DeBartolo Hall

Session Chairs: Robert S. Okojie, NASA, Glenn Rsch. Ctr., Cleveland, OH 44136 USA; Laura Rea, US Air Force Research Laboratory, Wright Patterson AFB, OH 45433-7707 USA

8:20 AM

FF1, Stacking Fault Growth in A-Face SiC PiN Diodes: *R. E. Stahlbush*[1]; M. E. Twigg[1]; S. M. Bishop[2]; E. A. Preble[2]; R. F. Davis[2]; C. Hallin[3]; E. Janzen[3]; [1]Naval Research Laboratory, Code 6881, Washington, DC 20375 USA; [2]North Carolina State University, Raleigh, NC 27695 USA; [3]Linköping University, Linköping Sweden

While SiC has advantages for use in power devices, there are material and processing problems that must be overcome in SiC devices such as PiN diodes. A major material problems impeding PiN diode development is the formation of stacking faults (SFs) during forward-biased operation, which increases the forward voltage, Vf. Most PiN diodes have been fabricated on wafers slightly tilted from the c-face, usually by 8°. Here, we examine SF growth in a-face PiN diodes. It has been suggested that the Vf drift might be suppressed for diodes with this crystallographic orientation. While the a-face diodes failed to meet this expectation, they did provide a different and very useful perspective for examining stacking fault growth. The epitaxial growth for the diodes in this work consists of a 30 µm thick n- drift layer and a p+ anode layer. Light emission from SFs and dislocations is viewed through a contact metal grid. The imaging system incorporates a sensitive CCD making it possible to image dislocations, which dominate the emission at low currents. The diodes do exhibit a significant Vf increase. The initial Vf is ~8 V at 100 A/cm2, and within the first minute of electrical stressing at 100 A/cm2, Vf increases about one volt. The high initial voltage indicates a high density of defects suppressing carrier lifetime. To capture the growth dynamics, the stressing was performed in a series of 50 ms intervals. Two images were collected for each interval: one during the stress interval and a second low-current image at 0.1 A/cm2 after each stress interval. The first images the SFs and the second the partial dislocations bounding the stacking faults. A low-current image is also collected before stressing. Because the basal planes are perpendicular to the wafer surface the SFs appear as lines. The dislocations along the a-direction perpendicular to the face appear as points and the other two a-directions appear as short lines. Before electrical stressing there is a high density of dislocations perpendicular to the surface ranging from 104 to 105/cm2. At the start of electrical stressing many, but not all, of the dislocations split and form expanding SFs. As the SFs expand, not all of them grow at the same rate. We also plan to examine the dislocations and SFs using site-specific TEM. We will investigate differences between dislocations that do and do not form SFs and factors affecting the SF growth rate. One of the controversies concerning SF growth is whether internal stress plays a significant role. We anticipate that the combined light emission and TEM work will help resolve this question.

8:40 AM

FF2, Stacking Fault Nucleation in 4H-SiC PiN Diodes: *Mark Erickson Twigg*[1]; Robert E. Stahlbush[1]; K. G. Irvine[2]; J. J. Sumakeris[3]; T. P. Chow[3]; P. A. Losee[3]; L. Zhu[4]; Y. Tang[3]; W. Wang[3]; [1]Naval Research Laboratory, Code 6812, 4555 Overlook Ave. SW, Washington, DC 20375 USA; [2]Cree, Inc., Durham, NC 27703 USA; [3]Rensselaer Polytechnic Institute, Troy, NY 12180 USA

Using plan-view transmission electron microscopy (TEM) and light emission imaging (LEI), we have identified many of the features of stacking faults (SFs) lying the in the c-plane (0001). These SFs grow during the forward bias of 4H-SiC PiN diodes and degrade the performance of the device. Site-specific plan-view TEM has proven particularly useful in analyzing the planar defects that emerge during LEI imaging of biased diodes. Plan-view TEM affords a wide expanse of electron-transparent specimen, and allows access to the [0001] zone axis, thereby facilitating diffraction-contrast analysis of partial dislocations bounding the SF. The focus of this paper is the nucleation of SFs in 4H-SiC PiN diodes. Our TEM observations indicate that faulted threading dislocations lying in the c-plane may create SFs using a Frank-Read mechanism in which partial dislocations bow out and give rise to SFs. We have found evidence of the Frank-Read mechanism in the direct identification of stacking faults that bow out from already existing faulted dislocations. We have also found isolated SFs that appear to originate from a nearby faulted dislocation. In both cases the contrast of the SF is strongly distorted, suggested the presence of strain in generating the SF, as would be expected for the Frank-Read mechanism. It is also interesting to observe that some faulted dislocations are oriented with the fault lying in the {1-100} plane. This paper essentially addresses the conjecture that threading c-plane dislocations give rise to stacking faults in forward-biased 4H-SiC PiN diodes, thereby providing an efficient mechanism for relieving residual stresses in the 4H-SiC substrate and film.

9:00 AM

FF3, Cross-Polarization Imaging and Micro-Raman Detection of Defects in the Epitaxy of 4H-SiC: *Orest J. Glembocki*[1]; Sharka M. Prokes[1]; Robert E. Stahlbush[1]; Michael F. MacMillan[2]; [1]Naval Research Laboratory, Code 6880.1, Washington, DC 20375 USA; [2]Dow Corning Corporation, MS CO43D1, 2200 W. Salzburg Rd., Midland, MI 48686-0994 USA

The growth of 4H-SiC is often accompanied by the formation of various defects, including micropipes, low angle grain boundaries, polytype inclusions and strained regions. These defects are typically visible through cross polarized imaging, which rotates linearly polarized light allowing wafers placed between crossed polarizers to show these regions as bright areas. To date, very little work has been performed on connecting cross-polarized images to specific defects. In this paper, we have studied defects that are formed in the epitaxial growth of n^+4H-SiC using cross-polarized imaging and micro-Raman scattering. Cross-polarized images were taken with an optical scanner having a spatial resolution of 5 µm. These images were then used as a map for more detailed analysis using micro-Raman scattering that has a spatial resolution of 0.7 µm and a depth resolution of 12 µm. We find that the sample had many features such as holes of various sizes ranging from several microns to many tens of microns. Many of holes were observed at varying depths in the sample, indicating that overgrowth of existing holes from the substrate had occurred. Other holes were observed to contain material in their centers. This material was identified and spatially profiled by Micro-Raman. Our results indicate that the inclusions found within holes can be 6H, 3C or 15R polytypes of SiC. The depths of these defects depend on the size and type of hole. Interestingly some of the 3C inclusions have been found to lie above the surrounding surface (4H-SiC). Spatial profiles have also been performed in regions surrounding these features. This work was supported in part by ONR and DARPA.

9:20 AM

FF4, A New Approach to Investigate Superscrew Dislocations in Silicon Carbide: *Xianyun Ma*[1]; Tangali S. Sudarshan[1]; [1]University of South Carolina, Elect. Engrg. Dept., 301 Main St., Columbia, SC 29208 USA

Although open-core (micropipe) screw dislocations in silicon carbide (SiC) were successfully predicted by Frank's model over fifty years ago,[1] and currently closed-core and open-core dislocations in SiC can be easily delineated by synchrotron white beam X-ray topography (SWBXT)[2] and a newly developed system based on the principle of polarized light microscopy (PLM),[3] a clear understanding of the precise nature of the defect is still lacking. For example, arguments continue on whether micropipes, in nature, are mixed or pure screw dislocations.[2,4] In addition, Frank's criterion may not be accurate enough to predict whether 2c-screw dislocations in 6H are open-core or closed-core.[2, 5-6] The large scale of micropipes (with diameters of submicron or microns) makes it difficult for high-resolution transmission electron microscopy (HRTEM) to image a micropipe at an atomic level. This study will present a new approach to investigate superscrew dislocations (including elementary screw dislocations and micropipes) in a SiC single crystal at a fundamental level. The presented approach uses (a) gas phase etching to highlight the fine structure of each defect, (b) the PLM system to locate the screw dislocation or micropipe position, and (c) AFM to detect the detailed structure of each defect. This methodology can precisely determine the

magnitude and the sense of Burgers vector of each screw dislocation or micropipe. The most important is that such atomic-level investigations can be performed systematically over an entire wafer, providing a variety of detailed fundamental parameters. Initial results indicate that in commercial 6H SiC most micropipes are 4c or larger, some of the 3c dislocations are closed-core, and none of the 2c dislocations are open-core. These results differ from the "common knowledge" that the Burgers vector for closed-core screw dislocations in 6H is 1c.[2] These results also show that PLM and SWBXT defect patterns are primarily determined by the Burgers vector value. In other words, although it is a small possibility, PLM and SWBXT techniques may fail to separately identify screw dislocations that are close together (within a few microns) and are of the opposite sense. Some micropipe patterns obtained from PLM and SWBXT are actually due to the close aggregation of several elemental screw dislocations. [1]F.C. Frank, Acta Cryst., 4 (1951) 497. [2]M. Dudley, X.R. Huang, and W. Vetter, J. Phys. D: Appl. Phys. 36 (2003) A30-A36. [3] X.Y. Ma, and T.S. Sudarshan, Jpn. J. Appl. Vol. 42 (2003) L1077-L1079. [4]J. Heidl, W. Dorsch, and H.P. Strunk, Phys. Rew. Let., Vol. 80 (1998) 740-741. [5]P. Pirouz, Philo. Mag. A, Vol. 78 (1998) 727-736. [6]W. Vetter, M. Dudley, J. Mater. Res., Vol. 15 (2000) 1649-1652.

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FF5, Identification of Dislocations in Diffused 4H-SiC PIN Diodes Using EBIC: Serguei Ivanovich Maximenko[1]; *Stanislav Ivanovich Soloviev*[1]; Tangali S. Sudarshan[1]; [1]University of South Carolina, Elect. Engrg., 301S Main St., Columbia, SC 29208 USA

Significant progress in the production of low micropipe density 4H-SiC substrates resulted in an increase in the yield of large area high power devises. However, other type of extended defects such as dislocations, the density of which varies from 103 to 105 cm-2, are still an issue for substrates. Electrical activity of a dislocation depends on its nature, whether it is screw, edge or basal plane dislocation. Thus, it is important to understand the effect of a specific dislocation type on the performance of SiC power devices. In this work, we investigated the electrical behavior of dislocations in diffused SiC PIN diodes using the Electron Beam Induced Current (EBIC) mode of a Scanning Electron Microscope (SEM). The PIN diodes have been formed by selective diffusion of aluminum and boron into a 4H-SiC substrate with a 10 mm thick epilayer doped with nitrogen up to 5x1015cm-3. Diffusion was performed at a temperature of 1800-2000°C in argon ambient using a graphite mask with open windows from 70 to 1000 µm in diameter. The standard photolithography process was employed to fabricate the planar p-n diode structures. An analysis of the fabricated PIN diodes using the EBIC technique revealed three types of defects (A, B, and C), which can affect the reverse characteristics of diffused PIN diodes. "Type A" and "type B" defects exhibited bright spots in the current image contrast at zero bias, while "type C" defects exhibited dark spots. However, at the applied reverse bias, "type A" defects disappeared from the current image contrast, "type B" defects changed their contrast from bright to dark, and "type C" defects changed their contrast from dark to bright. Identification of the observed defects was performed using KOH etching after EBIC analysis. The EBIC images showed 100% correlation with etch pit maps taken at the same regions. Based on the shape of etch pits, we attributed "type A" defects to screw dislocations, "type B" defects to super-screw dislocations (SSD), and "type C" defects to threading edge dislocations converted from basal plane dislocations during epitaxial growth (this was confirmed by additional polishing followed by etching). It was found that electrical breakdown of the diodes occurs at the location of super-screw dislocations. The used EBIC technique allowed us to identify different types of dislocations and analyze their impact on diffused SiC PIN diodes. Dependence of the electrical activity of the above dislocations, on the applied reverse bias, will be discussed in this presentation.

10:00 AM Break

10:20 AM

FF6, High Temperature Operation of SiC Electronics and Sensors: *Ruby N. Ghosh*[1]; Peter Tobias[1]; [1]Michigan State University, Ctr. for Sensor Matls., 2167 BPS Bldg., E. Lansing, MI 48824-2320 USA

Field-effect devices based on SiC metal-oxide-semiconductor (MOS) structures are attractive for electronic and sensing applications above 200C, which represents the upper bound for Si based devices. We are investigating insertion opportunities in energy plants for real time monitoring and control of a coal gasifier. MOS device operation in such chemically corrosive, high temperature environments places stringent demands on the stability of the insulating dielectric and the constituent interfaces within the structure. In this paper we present our results on oxide reliability and the role of charged states at the SiO2-SiC interface from in-situ measurements up to 530C. The primary mode of oxide breakdown at high temperature is believed to be due to electron injection from the substrate. For n-type MOS capacitors we have measured the leakage current as a function of temperature. We find current densities below 1E-8 A/cm2 and 2E-9 A/cm2 at electric field strengths up to 2 MV/cm and temperatures of 330C and 180C respectively. These are promising results for high temperature operation, since the optimum bias point for SiC field-effect devices is near mid-gap, where the field across the oxide is at a minima. We will discuss our data in terms of the differences in the conduction band alignment between silicon dioxide and the various SiC polytypes. We have also investigated the effect of ambient gases on the interface state density (Dit) at the oxide-SiC interface via capacitance voltage spectroscopy at 530C, since hermetically sealed packaging technology is not available at these temperatures. Within our experimental uncertainty, Dit in a reducing environment is that of an ideal capacitor, with an approximately constant 1E11 states/cm2 eV in the energy range 0.3 eV < Ec ?E < 0.9 eV. On the other hand, in an oxidizing environment, the interface state density is a strong function of the Fermi energy (Ef) within the SiC bandgap. As Ef is varied from midgap to the conduction band edge, the magnitude of Dit increases and the time constant of the charged states also becomes longer by orders of magnitude. We show that the optimum bias voltage for SiC MOS capacitors, with respect to device stability and device-to-device repeatability is near midgap. When Ef is biased near the conduction band edge, charging and discharging from slow interface states leads to long term drift in the MOS capacitor bias. Our results are valid for SiC n-type field-effect structures in general and have observed in both the 4H and 6H polytypes. We will discuss the optimum design of robust SiC MOS devices operating in high temperature environments.

10:40 AM

FF7, Thermally Stimulated Current Spectroscopy of High-Purity Semi-Insulating 4H-SiC Substrates: *Zhaoqiang Fang*[1]; David C. Look[1]; Laura Polenta[2]; [1]Wright State University, Semiconductor Rsch. Ctr., Physics Dept., 3640 Colonel Glenn Hwy., Dayton, OH 45435 USA; [2]University of Bologna, INFM & Dept. of Physics, Bologna I-40127 Italy

Semi-insulating (SI) SiC has been widely used as a substrate material for AlGaN/GaN high electron mobility transistors, because of its fairly good lattice match with GaN and its high thermal conductivity. Instead of using vanadium (V) as a deep acceptor to compensate the shallow donors, Cree, Inc. has announced the growth of high-purity (HP) SI 4H-SiC without V-doping.[1] Similar to the case for SI-GaAs, HPSI-SiC can be directly used for the fabrication of metal-semiconductor field-effect transistors, by using the ion-implantation technique. To control the material quality, it is important to understand the nature of the deep traps. To this end, we have successfully applied thermally stimulated current spectroscopy (TSC), which is known to be a very sensitive technique for investigating point-defect and impurity related traps in various SI semiconductors, such as HPSI GaAs and InP,[2-4] and carbon doped SI-GaN.[5] In this paper, we present: i) the fundamentals of TSC spectroscopy; ii) typical TSC spectra measured on HPSI 4H-SiC materials, which were obtained from Cree (grown by physical vapor transport) and other sources (grown by high-temperature chemical vapor deposition); and iii) theoretical fitting of a dominant hole trap (peaking at 150 K) related to B. In the temperature range of 83 to 390 K, TSC features at ~150 K, ~170 K, ~215 K, ~260 K, and ~355 K can often be observed in different HPSI 4H-SiC samples. Their activation energies, calculated by using the approximate equation ET=kTm ln (Tm4/b), where Tm is the peak temperature of a given trap, b is the heating rate, and k is Boltzmann's constant, are 0.27, 0.32, 0.42, 0.53, and 0.75 eV, respectively. Based on literature data for deep centers in conductive 4H-SiC, the impurity and point-defect nature of these traps will be discussed. [1]J.R. Jenny et al., J. Electron. Mater. 31, 366 (2002). [2]Z-Q. Fang and D.C. Look, J. Appl. Phys. 69, 8177 (1991). [3]D.C. Look et al., Phys. Rev. B55, 2214 (1997). [4]Z-Q. Fang et al., J. Electron. Mater. 27, L68 (1998). [5]Z-Q. Fang et al., Mater. Res. Soc. Symp. Proc. vol 798, p. Y 5.27.1 (2004).

11:00 AM Student

FF8, First Observation of Current Induced Deep-Level Defects in 4H SiC PiN Diodes with Magnetic Resonance: *S. K. Yerkes*[1]; P. M. Lenahan[1];

R. S. Okojie[2]; [1]Pennsylvania State University, 212 Earth & Engrg. Sci. Bldg., Univ. Park, PA 16802 USA; [2]NASA Glenn Research Center, 21000 Brookpark Rd., Cleveland, OH 44135 USA

We report the first observation of high current stress induced deep-level defects in 4H SiC PiN diodes with a very sensitive electron spin resonance technique called spin-dependant recombination (SDR). Pre-stress SDR measurements yielded no SDR signal. After stressing at approximately 5.0 volts, yielding a current density of 160 A/cm^2, for 40 minutes, we observe a relatively strong SDR signal consisting of at least two peaks. The stronger peak has a g value of approximately 2.005 when the magnetic field is oriented parallel to the crystalline c-axis. The stronger signal exhibits weak g anisotropy; the weaker signal slightly stronger anisotropy. Although we have yet to develop a detailed model of the defect structure, we very tentatively link the paramagnetism to unpaired electrons primarily localized on silicon atom wave functions. The SDR amplitude is a strong function of forward bias voltage; with the signal strongly peaked at a forward bias of 2.40 volts and a current density of 7mA/cm^2. This result is consistent with, and strongly supports the idea that the observed signal is caused by deep-level defects (i.e., presumably involving stacking faults) which play dominating roles in recombination events in the depletion region of the diodes. Our results may be relevant to recent work of Lindefelt and coworkers, who conclude that a stacking fault in the 4H-SiC PiN diode acts as a one-dimensional quantum well, thus altering the physical and electronic properties of the crystal.[1] This idea is based on total energy calculations of a 4H-SiC crystal containing an intrinsic SF, where it has been found that a narrow band is split off from the bottom of the conduction band and extends about 0.2 eV into the bandgap of 4H-SiC.[2] [1]U. Lindefelt and H. Iwata, in "Recent Major Advances in SiC", Springer-Verlag, Berlin (2003). In press. [2]M. S. Miao, S. Limpijumnong, and W. R. L. Lambrecht, Appl. Phys. Lett. 79(26), p. 4360 (2001).

11:20 AM Student

FF9, Spin Dependent Recombination Observation of Hyperfine and Superhyperfine Interactions of Interface Trap Defects at the 6H Silicon Carbide/Silicon Dioxide Boundary: *D. J. Meyer*[1]; P. M. Lenahan[1]; A. J. Lelis[2]; [1]Pennsylvania State University, Engrg. Sci. & Mech., 212 EES Bldg., Univ. Park, PA 16802 USA; [2]US Army Research Laboratory, Sensors & Electron Devices Direct., 2800 Powder Mill Rd., Adelphi, MD 20783 USA

At last year's Electronic Materials Conference we reported preliminary spin dependent recombination (SDR) results on a paramagnetic deep level center at or very near the SiC/SiO_2 interface of SiC/SiO_2 metal oxide semiconductor field effect transistors (MOSFETs). SDR is a very sensitive electron spin resonance (ESR) technique that allows direct observation of deep level paramagnetic defects through measurements of currents in semiconductor devices. Our results last year indicate that the SDR response is strongly correlated to SiC/SiO_2 interface recombination currents and also that the magnitude of the SDR response is correlated with processing induced changes in interface trap density, essentially demonstrating that we are observing the dominating interface/near interface trapping defects. Since our presentation last year, we have mapped the defect g tensor and found it to be isotropic with a value of g = 2.0027; this lack of anisotropy suggests a center of high symmetry, possibly a vacancy. In addition, we have observed superhyperfine and hyperfine interactions of the defect electron with both ^{29}Si and ^{13}C nuclei. With this additional data, we can now reasonably conclude that the defect under study involves a silicon vacancy site at or very near the SiC/SiO_2 boundary. We can also draw some conclusions with regard to the wave function of the unpaired electron associated with the defect. We are presently adding conventional ESR measurements as a function of gate bias to provide a fuller description of the electronic properties of these defects. To the best of our knowledge, our work represents the first observation of SDR, in fact of any type of magnetic resonance measurement in a SiC MOSFET and arguably the first conclusive observation via magnetic resonance of a defect certain to be involved in SiC/SiO_2 interface traps.

11:40 AM Student

FF10, Comparison of 4H-SiC PiN Diodes Fabricated with Different Starting Substrates: *P. A. Losee*[1]; C. Li[1]; J. Seiler[1]; R. E. Stahlbush[2]; T. P. Chow[1]; I. B. Bhat[1]; R. J. Gutmann[1]; [1]Rensselaer Polytechnic Institute, Ctr. for Integrated Elect., 110 8th St., Troy, NY 12108 USA; [2]Naval Research Laboratory, Elect. Sci. & Tech. Div., Washington, DC 20375 USA

4H-SiC is a promising material for high power and high temperature electronics due to its wide energy band gap and large critical electric field. For high voltage applications, bipolar semiconductor devices offer the advantage of conductivity modulation of lightly doped blocking layers. In recent years, stacking fault propagation has been observed in SiC pin rectifiers.[1,2] This phenomenon can result in drifting of the diode on-state performance, rendering the devices unreliable. In this work, techniques aimed at minimizing the propagation of stacking faults as well as comparing the effects of different starting materials were explored. 4H-SiC pin diodes have been designed and fabricated using epilayers grown on substrates purchased from various vendors. A 12µm thick, lightly doped drift layer is used along with a graded doping profile between the drift region and substrate. The p-type anode is also grown epitaxially. The epi-layers on each sample were grown together as part of the same run in Rensselaer Polytechnic Institute's horizontal coldwall CVD reactor. The diodes were mesa isolated by RIE SiC etching. Gridded metal contacts to the anode were used to allow visibility during characterization. Surface morphology photographs prior to device fabrication and electroluminescence (EL) imaging during diode forward biased operation were used to characterize the samples. The images reveal a wide range in material defect density between samples, which correlate with device electrical performance such as forward-IV and reverse characteristics. Stacking fault propagation was observed on each sample included in the study, although relatively small electrical drift was observed. Samples biased (J_F=140A/cm^2) over three hours exhibited a drift in V_F (J_F=40A/cm^2) of less than 0.5V. Similar diodes with thicker (greater than 30µm) drift layers and various buffer layers are currently being fabricated and will be presented. The additional set of devices should provide a wide range of electrical results as well as evaluate the reliability of material suitable for high voltage SiC device applications. Acknowledgment: This work was supported primarily by DARPA under contract number #DAAD19-02-1-0246. [1]J. P. Bergman, H. Lendenmann, P. A. Nilsson, U. Lindefelt, P.Skytt, "Crystal defects as source of anomalous forward voltage increase of 4H-SiC diodes", Materials Science Forum, vol. 353-356, pp. 299-302, 2001. [2]R.E. Stahlbush, M. Fatemi, J. B. Fedison, S. D. Arthur, L.B. Rowland and S. Wang, "Stacking-fault formation and propagation in 4H-SiC pin diodes", Journal of Electronic Materials, vol. 31, pp. 370-375, 2002.

Session GG: Semconductors: Processing and Oxidation

Friday AM June 25, 2004

Room: 136 Location: DeBartolo Hall

Session Chairs: Doug C. Hall, University of Notre Dame, Dept. of Elect. Engrg., Notre Dame, IN 46556-5637 USA; Maria Losurdo, Institute of Inorganic Methodologies and Plasmas, Bari 70126 Italy

8:20 AM

GG1, Electrical and Optical Properties of Anodic LaAl: *Tito Busani*[1]; Roderick Devine[2]; [1]Universite' J. Fourier, CNRS-LEMD, 25, Ave. des Martyrs, Grenoble 38042 France; [2]Kirtland Air Force Base, AFRL-VSSE, Albuquerque, NM 87117 USA

Crystalline $LaAlO_3$ is an attractive replacement for SiO_2 as a gate dielectric because it has a band gap of 5.6 eV and a dielectric constant, ε, of 28. Furthermore, it is assumed to be un-reactive with Si. Previously, using reactive ion sputtering with an $LaAlO_3$ target, we obtained amorphous films of this material but with dielectric constants never exceeding 14. We concluded that the density of the films was lower than that of crystalline material. In the present we report the results of studies of anodically oxidized LaAl films. LaAl films were deposited on Si 4'' substrates at room temperature by rf sputtering in pure Ar using a stoichiometric target. The film composition was analyzed using energy dispersive x-rays. Stoichiometric anodic $LaAlO_3$ oxides were obtained

plasma assisted oxidation in a microwave frequency (2.45 GHz) reactor with typical using constant current, positive bias on the substrate/sample holder. The total current through the sample did not exceed 2.46 mA/ cm^2. The partial oxygen pressure in the chamber during the oxidation was 10 mTorr and the substrate temperature, due to the plasma discharge itself, of the order of 60°C. An oxide thickness of 100nm was achieved in less than 3 minutes as determined by a single wavelength (632.8 nm) ellipsometer. The refractive index of the oxides was 1.65 - 1.91 depending on the experimental conditions, smaller than the single crystal value (2.072) at this wavelength. Fourier transform infrared spectrometer (FTIR) revealed a main peak at 760 cm^{-1} with a FWHM of 172 cm^{-1} consistent with amorphous $LaAlO3_3$. No segregation effects were observed as confirmed by XPS measurements. The FTIR peak was shifted by 9 cm^{-1} with respect to that of sputtered $LaAlO_3$ films. C(V) and current density/ voltage (I-V) measurements were carried out to test the electrical quality of the oxide and to determine ε. Al-oxide-Al structures were prepared using different experimental conditions yielding ε values from 8.2 - 13.3. Unannealed, anodically oxidized films on Si always contained considerable fixed oxide charge, annealing at 400°C was necessary to obtain acceptable C(V) curves. Annealing also reduced the capacitance minimum which may be indicative of residual LaAl at the interface in this case. After annealing the samples had ε of 8.7-13.1. Typically, the flat band voltage moved from -12 to -2.5 V. The measured leakage current density ~ 10^{-8}-10^{-9} A/cm^2 for an electric field ~ -1 MV/cm was extremely low. Clausius-Mossotti and Lorenz-Lorenz theories will be used to explain the relation between density, ε and refractive index. From this analysis it appears that in anodic oxide the reason why is not possible to obtain an ε of 28 is both because of Si substrate-LaAl interaction and low density.

8:40 AM

GG2, Improvement in the Insulating Properties of Thermal Oxide on InAlP: M. Graham[1]; S. Moisa[1]; G. I. Sproule[1]; X. Wu[1]; J. W. Fraser[1]; P. J. Barrios[1]; *Anthony John SpringThorpe*[1]; D. Landheer[1]; [1]National Research Council of Canada, Inst. for Microstruct. Scis., Bldg. M50, Rm. #160, Ottawa, Ontario K1A 0R6 Canada

Producing chemically and electrically stable surfaces on III-V semiconductors is crucial for a number of important device applications. Passivation layers can be produced by deposition of silicon nitride or oxide or created by a variety of oxidation processes including thermal oxidation. Thermal oxidation data for AlGaAs and InAlAs in GaAs- and InP-based heterostructure devices have been reported, e.g.,[1-3] and the Al-containing oxides have often been found to possess good insulating characteristics. Recently, Al-containing thermal oxides on InAlP have been shown to be even more promising.[4-6] This paper presents data on the thermal oxidation at 500°C in moist nitrogen (95°C) of MBE-grown InAlP layers (In0.525 Al0.475 P, In0.494 Al0.506P and In0.485 Al0.515P) lattice matched to GaAs. The oxides (20 nm - 300 nm thick) have been characterized by Auger electron spectroscopy (AES), X-ray photoelectron spectroscopy (XPS), Rutherford backscattering spectroscopy (RBS), scanning electron microscopy (SEM), and transmission electron microscopy (TEM). Oxides are amorphous and appear to be a mixture of indium phosphates and aluminum oxide. The oxidation kinetics are parabolic. Of particular concern in native oxides of InAlP are the indium compounds that remain near or at the oxide/substrate interface of the oxidation front.[4-6] A brief oxidation in oxygen at 500°C following oxidation in moist nitrogen oxidizes these residual indium particles present at the interface and leads to improved electrical properties. The current density at a field of 1 MVcm-1 (8.6 V gate potential) is 1.7×10-10 Acm-2, approximat ely two orders of magnitude lower after the final treatment in dry oxygen. The breakdown voltage is increased to 44 V, corresponding to a breakdown field of 5.1 MVcm-1. Thus the films should be useful as insulators in some device applications. [1]F. A. Kish, S. J. Caracci, N. Holonyak, Jr., K. C. Hsieh, J. E. Baker, S. A. Maranowski, A. R. Sugg, J. M. Dallesasse, R. M. Fletcher, C.P. Huo, T. D. Osentowski and M. G. Crawford, J. Electron. Mat. 21, 1133 (1992). [2]U. K. Mishra, P. Parikh, P. Chavarkar, J. Yen, J. Champlain, B. Thibeault, H. Reese, S. S. Shi, E. Hu, L. Zhu and J. Speck, IEDM'97, 21.1.1. [3]R. J. Hussey, R. Driad, G. I. Sproule, S. Moisa, J. W. Fraser, Z. R. Wasilewski, J. P. McCaffrey, D. Landheer and M. J. Graham, J. Electrochem. Soc., 149, G581 (2002). [4]A.L. Holmes, Ph. D. Dissertation, The U. of Texas at Austin, December 1999. [5]P. J. Barrios, D. C. Hall, G. L. Snider, T. H. Kosel, U. Chowdhury and R. D. Dupuis, in State-of-the-Art Program on Compound Semiconductors (SOTAPOCS XXXIV), 199th Meeting of The Electrochemical Society (Washington, DC, March 25-30, 2001). [6]P. J. Barrios, D. C. Hall, U. Chowdhury, R. D. Dupuis, J. B. Jasinski, Z. Liliental-Weber, T. H. Kosel and G. L. Snider, Abstract, 43rd Electronic Materials Conference, Notre Dame, Indiana, June 27-29, 2001.

9:00 AM Student

GG3, Electrical Properties and Microstructure of InAlP Native Oxides for MOS Applications: *Ying Cao*[1]; Jing Zhang[1]; Xiang Li[1]; Thomas H. Kosel[1]; Patrick Fay[1]; Douglas C. Hall[1]; R. E. Cook[2]; Xuebing Zhang[3]; Russell D. Dupuis[3]; [1]University of Notre Dame, Dept. of Elect. Engrg., 275 Fitzpatrick Hall, Notre Dame, IN 46556 USA; [2]Argonne National Laboaratory, Electron Microscopy Ctr., Argonne, IL 60439 USA; [3]Georgia Institute of Technology, Dept. of Elect. & Computer Engrg., Atlanta, GA 30332 USA

Native oxides of $In_{0.485}Al_{0.515}P$ have excellent insulating properties and are capable of supporting inversion.[1] The leakage current density, J_L, increases by several orders of magnitude when 110 nm oxide films are thinned to ~25 nm, exposing a region with a high interfacial precipitate density.[2] Further studies are presented on the scalability of InAlP native oxides to thicknesses more suitable for MOS device applications as obtained by oxidizing thinner epilayers. Grown by MOCVD on GaAs substrates, the InAlP layers studied are 63, 31, 15, 8 and 5 nm thick. Fully wet oxidized at 500°C, the films expand ~1.7X to corresponding oxide thicknesses of 110, 53, 26, 14 and 7 nm, measured by variable-angle spectroscopic ellipsometry (VASE). MOS capacitors fabricated with as-grown (AG) oxides formed from thinner InAlP layers have notably lower J_L than 110 nm films etched back to similar thicknesses: J_L=3x10^{-11} A/cm^2 (53 nm, AG) vs. 5x10^{-10} A/cm^2 (49 nm, etched), and 1x10^{-9} A/cm^2 (26 nm, AG) vs. 1x10^{-7} A/cm^2 (24 nm, etched), all at 0.4 MV/cm. At 1.9 MV/cm, a 10^6 disparity is seen: 6x10^{-9} A/cm^2 (26 nm, AG) vs. 9x10^{-3} A/ cm^2 (24 nm, etched). Quasi-static C-V measurements show that both 53 nm and 26 nm oxides (AG) support inversion under illumination. J_L remains low for AG oxide films as thin as 14 nm (2x10^{-9} A/cm^2 at 0.4 MV/ cm). Breakdown fields for oxides 14 nm and thicker are 3-5 MV/cm. The thinnest AG InAlP oxides (7 nm) show Schottky-diode-like behavior. I-V-T measurements suggest that thermionic emission is the dominant conduction mechanism, with an electron barrier height of ~1 eV calculated using a modified Norde method. From optical constants determined by VASE measurements, the InAlP oxide bandgap is determined from a Tauc plot to be 3.52 eV. A comparison of bright-field STEM and Z-contrast images using a high-angle annular dark-field (HAADF) detector in the STEM mode for a 120 nm oxide (obtained by partially oxidizing a 1 μm thick InAlP layer) shows that precipitates are formed in the oxide with higher atomic number (Z) than the surrounding oxide, strongly suggesting that they are In-rich. We observe no such interfacial precipitates in bright-field TEM for the 26 nm thick oxide (AG), which exhibits a 10^6 times lower leakage than its etched counterpart. We hypothesize that the degree to which the heavier and more slowly outdiffusing In accumulates near the interface during oxide growth, forming In-rich precipitates responsible for increased electrical conduction, is reduced by the shorter oxidation time of thinner InAlP films. In summary, native oxides of thin InAlP epilayers show considerable promise for MOS device applications and merit further study. [1]P. J. Barrios, D. C. Hall, G. L. Snider, T. H. Kosel, U. Chowdhury and R. D. Dupuis, State-of-the-Art Program on Compound Semiconductors XXXIV, Electrochem. Soc. Proc. vol. 2001-1, pp. 258-264. [2]P. J. Barrios, D. C. Hall, U. Chowdhury, R. D. Dupuis, J. B. Jasinski, Z. Liliental-Weber, T. H. Kosel, and G. L. Snider, paper DD4, 43rd Electronic Materials Conference (Notre Dame, IN, June 27-29, 2001).

9:20 AM Student

GG4, InAlP Native Oxide/GaAs MOS Heterostructure Interface State Density Measured by Impedance Spectroscopy: *Xiang Li*[1]; Y. Cao[1]; D. C. Hall[1]; P. Fay[1]; X. Zhang[2]; R. D. Dupuis[2]; [1]University of Notre Dame, Dept. of Elect. Engrg., 275 Fitzpatrick Hall, Notre Dame, IN 46556 USA; [2]Georgia Institute of Technology, Sch. of Elect. & Computer Engrg., Atlanta, GA 30332 USA

In conventional GaAs-based MESFETs and HEMTs, use of Schottky gate contacts results in appreciable gate leakage current and limited gate voltage swing. An attractive alternative for low-leakage and high-power FETs is a metal-insulator-semiconductor (MIS) gate. However, GaAs-based MIS interfaces formed by oxidation of III-Vs have historically

suffered from a high interface trap state density, N_{it}. We report the first N_{it} measurements of native-oxide $In_{0.49}Al_{0.51}P$/GaAs MOS capacitors, using bias- and temperature-dependent variable-frequency impedance spectroscopy. Our measurements indicate that InAlP oxide has a low leakage current density and a sufficiently low N_{it} to allow inversion to be observed,[1] making it promising for devices. InAlP native oxide/GaAs MOS capacitors were fabricated on an MOCVD-grown heterostructure consisting of 63 nm of InAlP on n-type GaAs. The InAlP was oxidized at 500°C in an H_2O/N_2 ambient, resulting in a 114.6 nm thick oxide. The measured leakage current density was $8.6x10^{-10}$ A/cm^2 at 5 V bias, demonstrating the oxide's good insulating quality. An impedance spectroscopy technique has been developed to determine the properties of InAlP oxide/GaAs interface states. A new equivalent circuit model (extending the conventional model through added components that model the behavior of an interface layer and interface states) is used to aid the interpretation of the impedance measurements. Capacitor impedance (calibrated using on-wafer open/short/load compensation with a test signal level of 20 mV rms) was measured on-wafer from 40 Hz to 10 MHz as a function of applied DC bias and temperature in a dark probing chamber. The measured room-temperature impedance spectra show broad conductance peaks that shift to higher frequency as the bias is scanned from depletion through accumulation, indicating the interface states are distributed over the bandgap. Capacitors with areas from 130x130 μm^2 to 340x340 μm^2 were measured to verify scaling of the equivalent circuit. The bias-dependent equivalent circuit matches closely the measured capacitor impedances over the full range of bias and frequency, and shows the distribution of interface states with energy is approximately exponential, with a total N_{it} of $8x10^{11}$ cm^{-2} and an effective activation energy of E_a=0.34 eV. The impedance spectra of capacitors have also been measured vs. temperature from 15-90°C. For biases in accumulation, the measured conductance peak frequency increases with increasing temperature. From Arrhenius plots of the conductance peak frequency, an E_a=0.44 eV has been obtained (r=0.997), in good agreement with room-temperature bias-dependent impedance measurements. This indicates the extended circuit model with an exponential interface state distribution is consistent with both variable-bias and variable-temperature measurements. In summary, an extended impedance spectroscopy technique has been developed and applied to characterizing trap densities and distributions at InAlP native oxide/GaAs interfaces, and promises to be a useful tool in the further optimization of these MOS structures for potential device applications. This work was supported by the Air Force Office of Scientific Research grant AF-F49620-01-1-0331. [1]P. J. Barrios, D. C. Hall, G. L. Snider, T. H. Kosel, U. Chowdhury and R. D. Dupuis, Proc. of the Intl. Symp.: III-Nitride Based Semiconductor Electronics and Optical Devices and Thirty-Fourth State-Of-The-Art Program On Compound Semiconductors (SOTAPOCS XXXIV), F. Ren, D.N Buckley, S. N. G. Chu, and S. J. Pearton, eds., Pennington, N.J.: The Electrochemical Society Proceedings 258 (2001).

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GG5, Lateral Wet Oxidation of AlAsSb Lattice Matched to GaSb: *Kevin Meneou*[1]; Hung-Cheng Lin[1]; Keh-Yung Cheng[1]; Kuang-Chien Hsieh[1]; Jongjin George Kim[2]; Ramon Martinelli[2]; [1]University of Illinois, Dept. of Elect. & Computer Engrg., Micro & Nanotech. Lab., 208 N. Wright St., Urbana, IL 61801 USA; [2]Sarnoff Corporation, CN5300, Princeton, NJ 08543-5300 USA

Wet oxidation of AlGaAs alloys has emerged in the last decade as a new processing option in GaAs-based devices. In particular, lateral oxidation is used extensively in low-threshold current vertical cavity surface emitting lasers. Recently, there have been investigations into lateral, wet oxidation of other semiconductor materials, particularly AlAsSb lattice-matched to InP ($AlAs_{0.56}Sb_{0.44}$). In this work we studied lateral oxidation of AlAsSb lattice-matched to GaSb ($AlAs_{0.1}Sb_{0.9}$) and found it to be a promising technology for processing of future GaSb-based devices. We performed lateral oxidation on samples grown by molecular beam epitaxy containing a 100 nm thick layer of $AlAs_{0.1}Sb_{0.9}$ sandwiched between layers of GaSb. Oxidation temperatures used were between 300°C and 450°C. In the range of 330°C-350°C, high oxidation rates and good selectivity to GaSb were obtained. Oxidation depths as great as 130 μm at 330°C and oxidation rates up to 2.15 μm per minute at 350°C were realized. The oxidation rate is higher than can be achieved in AlGaAs at this temperature, and the high oxidation rate at such a low temperature is technologically attractive. Study of the composition of the oxide using Auger depth profiling and scanning electron microscopy (SEM) showed that the products remaining in the AlAsSb layer after oxidation are primarily AlO_x and elemental Sb, so that the composition is similar to that of oxidized $AlAs_{0.56}Sb_{0.44}$. Structurally, SEM showed that the Sb exists mostly as large grains near the center of the oxidized layer with the AlO_x at the top and bottom interfaces of the oxidized layer, contrasting with the structure reported for oxidized $AlAs_{0.56}Sb_{0.44}$.[1] Study of oxidation kinetics revealed connections between oxidation kinetics and oxidation front morphology in our material whereby the oxidation front morphology undergoes a dramatic change as the oxidation moves from reaction rate-limited oxidation into the diffusion rate-limited oxidation regime. Finally, we discovered and studied so-called "self-limiting oxidation" in this material, as has been reported once before for $AlAs_{0.56}Sb_{0.44}$.[2] When oxidation temperatures were raised to above 375°C oxidation depths remained shallow despite long oxidation times. This behavior is completely contrary to what occurs during oxidation of more familiar materials such as Si and AlGaAs, where higher oxidation temperatures result in deeper oxidation. [1]O. Blum, K. M. Geib, M. J. Hafich, J. F. Klem, and C. I. H. Ashby, Appl. Phys. Lett. 68, 3129 (1996). [2]S.K. Mathis, K.H.A. Lau, A.M. Andrews, and E.M. Hall, J. Appl. Phys. 89, 2458 (2001).

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GG6, Characterization of Sulfur Passivated Group III Antimonide Semiconductors: *Joshua A. Robinson*[1]; Sammy H. Wang[1]; Suzanne E. Mohney[1]; [1]Pennsylvania State University, Matls. Sci. & Engrg., Univ. Park, PA 16802 USA

GaSb-based semiconductors offer great potential for laser diodes with low threshold voltages, photodetectors with high quantum efficiency, and booster cells in tandem solar cell arrangements. Antimonide-based semiconductors are also of interest for high frequency, low power electronic devices. In an attempt to reduce device leakage currents and improve stability, passivation of the semiconductor surface using sulfur has gained interest in the last decade. Studies have shown that sulfur passivation decreases surface state density, increases photoluminescence, and improves the electrical performance and thermal stability of Schottky barrier contacts. Passivated GaSb surfaces have previously been examined using x-ray photoelectron spectroscopy and ellipsometry, but there has been no report of the characterization of passivated GaSb using transmission electron microscopy (TEM). In this study, we report the examination of sulfur-passivated (100) n-GaSb using TEM with energy dispersive x-ray spectroscopy. After passivation in 21% $(NH_4)_2S$, a uniform layer is formed on the semiconductor. The layer is amorphous and contains Ga and S with negligible O or Sb. It is approximately 14 nm thick when formed by a 5 min soak in 21% $(NH_4)_2S$, with shorter treatment times leading to thinner layers. The sulfide is thermally stable when annealed at 125°C for 60 min followed by 350°C for 10 min, and it prevents reaction between deposited metals and GaSb. After 20 min at 500°C, the layer becomes enriched with Ga from the GaSb, with voids and Sb precipitates forming at the sulfide/GaSb interface. It is reported that $(NH_4)_2S$ solutions etch GaSb. Using atomic force microscopy, we have also compared the etch rates reported for p-GaSb to those we have measured for p-$In_{0.75}Ga_{0.25}Sb$. For identical solution concentrations, the addition of indium to the semiconductor reduces the rate the heavily doped semiconductor is etched. Work is currently underway to produce a uniform layer of minimal thickness along with minimal etching of the semiconductor to use in processing shallow, thermally stable contacts to InGaSb.

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GG7, Modifications of GaSb Surface Electronic Structure by the Chalcogen Atoms: S, Se and Te: *Zhiyan Liu*[1]; Amit Gokhale[1]; Manos Mavrikakis[1]; Thomas F. Kuech[1]; [1]University of Wisconsin, Dept. of Chem. & Bio. Engrg., 1415 Engrg. Dr., Madison, WI 53706 USA

GaSb has important applications in high-speed and opto-electronic devices operating in the infrared and near-infrared region. However, its applications are hindered due to the chemical reactivity of GaSb surface. The GaSb oxidation chemistry produces a variety of chemically varying surface oxides as well as elemental antimony, which results in high surface states density and increased leakage current. Control over the electronic structure of the GaSb surfaces is often critical in many device applications. Chemical absorption of chalcogen atoms on III-V semiconductor surfaces have been shown to effectively alter the surface states

density, reducing the density of mid-gap states as well as the surface recombination velocity, thus enhance the optical and electrical performance of semiconductor devices. While sulfur has been used most commonly in previous passivation studies, the present study is focused on the changes in surface electronic structure and chemistry when the chalcogen is systematically changed from S to Se to Te. The surfaces of GaSb were prepared by initial surface cleaning followed by immersion in both aqueous and non-aqueous, benzene-based solutions of Na_2S, Na_2Se and Na_2Te. The use of non-aqueous passivation techniques is motivated by the desire to limit regrowth of surface oxides through contact with water. The non-aqueous solutions were prepared by the dissolution of the Na_2X compounds in benzene having an equimolar concentration of 15-crown-5 ether to facilitate solvation. Additionally, an organic oxidant, such as anthraquinone, was used to allow the electrons transfer to the solution required for the reaction of the chalcogen with the surface. The passivation efficiencies were evaluated by photoluminescence yield, and they are dependent not only on the different chalcogenides used, but also on the particular reaction media. In general non-aqueous-based treatment provided the greatest PL enhancement after treatment. An x-ray photoelectron spectroscopy (XPS) analysis of surface chemistry indicates a different chemical structure of GaSb surface after absorption of such higher order chalcogen atoms as Se and Te from that of S. A higher concentration of surface oxides but lower element antimony content was observed after Se and Te treatments. The kinetics of GaSb surface reaction with Na_2Se was studied by characterizing the evolution of Se coverage with duration of the treatment. In addition, periodic self-consistent density functional theory results on electronic states of GaSb surface before and after absorption of group VI atoms (O, S, Se, and Te) are presented in order to determine the origin of the chemical trends with coverage of these chalcogen atoms on Ga and Sb terminated (001) surfaces.

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GG8, Sputtered Titanium Oxide Barrier Layers for PZT MEMS: *Steven Joseph Gross*[1]; Raviprakash Jayaraman[1]; Srinivas Tadigadapa[1]; Susan Trolier-McKinstry[1]; Thomas N. Jackson[1]; [1]Pensylvania State University, 121 EE East, Univ. Park, PA 16802 USA

The superior piezoelectric response available from the lead zirconate lead titanate (PZT) material system compared with other materials can provide improved performance for microactuators. The cost of the higher piezoelectric constants is a greater level of process complexity. The reactivity of PZT with silicon, at temperatures below those required to obtain crystallized ferroelectric films, necessitates a chemically inert barrier layer that prevents reaction between the PZT and underlying films.[1] The Si/SiO2/Ti/Pt structure is the most common bottom electrode configuration and allows the film to be poled parallel to the thickness - the d31 mode. In cases where a large positive in-plane strain is required, the d33 mode is preferred. Sol-gel deposited ZrO2 barrier layers with interdigitated top electrodes (IDE) have successfully been employed to exploit the d33 mode.[2] Recently, we demonstrated MEMS switches and cantilever actuators based on SixNy/ZrO2/PZT stacks.[3] As with any released membrane composed of multiplayer films, the balancing of the residual stresses to achieve flat structures is of paramount importance and can be challenging. If the stress of one or more of the films is not stable, the task is even more difficult. A study of the residual stresses and stress stability of PZT/barrier multilayer films was undertaken using the wafer curvature technique. Silicon nitride and PZT were found to be stable with values of 400MPa and 120MPa respectively, while the stress of the zirconia was observed to vary (-100 to 240 MPa) when exposed to atmosphere or temperature treatments. Even after a 3 hr anneal at 700°C to reduce porosity stress stability remained poor and the data is consistent with the hydration of the zirconia.[4] This makes the curvature of the released cantilever actuators and their operation particularly sensitive to the thermal process history. To improve the stress stability titanium oxide was investigated as a barrier layer. Titania films with 50-100 nm thickness were sputtered on silicon-rich nitride coated silicon wafers and annealed at 700°C for 1-2 hrs. PZT films (300-600nm) thick were then spun on by sol-gel and crystallized at 700°C. XRD analysis shows well-crystallized PZT in the perovskite phase with randomly oriented crystallites. IDEs were deposited on the PZT by evaporating Cr/Au (5/200nm) using a bi-layer lift-off process. The PZT exhibits good hysteresis behavior with Pr = 20-32 mC/cm2, dielectric constant of 640-1060, loss of 2-3% at 1 to 10 kHz, and Ec of 50-60 kV/cm. These results suggest that sputtered titania is a viable barrier for PZT films. In addition, the low porosity of sputtered titania should result in films with improved stress stability. [1]G.R. Fox, S. Trolier-McKinstry, S.B. Krupanidhi, L.M. Casas, J. Materials Research, 10(6), 1995. [2]B.Xu, Y.Ye, L.E. Cross, J.J. Bernstein, R. Miller, Applied Physics Letters, 74(23), 1999. [3]S.J. Gross, Q.Q. Zhang, S. Tadigadapa, S. Trolier-McKinstry, T.N. Jackson, Applied Physics Letters, 83(174), 2003. [4]R. Brenier, A. Gagnaire, Thin Solid Films, 392, 2001.

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GG9, Novel Selective Dry Etch Process for Ultra Thin Pt Salicide Formation: *Jihun Oh*[1]; Jong-Heon Yang[1]; Chang-Geun Ahn[1]; Kiju Im[1]; In-Bok Baek[1]; Won-ju Cho[1]; Seongjae Lee[1]; [1]ETRI, Future Tech. Rsch. Div., 161 Gajeong-dong, Yusung, Daejon 305-350 Korea

Recently, ultra thin body Schottky barrier source/drain MOSFET (UTB SB MOSFET) has drawn attention as an alternative to the conventional MOSFET for low source/drain sheet resistance and excellent short channel immunities, even at the gate length of 20 nm. For the fabrication of the reliable UTB SB MOSFET, it is essential to form uniform silicide layer at source/drain region. However, the hot aqua regia solution, which is used to etch Pt selectively, is very corrosive even to remove PtSi unless the protecting oxide passivates PtSi surface, resulting in nonuniform PtSi formation. In this work, we propose, for the first time, the dry etch process for the formation of ultra-thin Pt salicide with high selectivity and uniformity. In this experiment, 10 nm thick Pt was deposited by RF magnetron sputtering in Ar ambient on n-type (100) Si (3~3.5 Ω cm) and SiO_2 wafers. The wafers were cleaned by the standard RCA method and dipped in 30:1 BOE for 30 sec before loaded in sputter chamber. PtSi was formed at 400°C in N_2 for an hour. Ar plasma etch was performed to remove Pt selectively in a conventional parallel plate plasma etcher at the RF power of 100 W. Then, the etching characteristics of Pt and PtSi were determined by the step profilometer, the grazing angle XRD, AES, SEM, and TEM. The sheet resistance Rs of as annealed PtSi and Pt are about 18 Ω/sqr. and 8 Ω/sqr., respectively. The Rs of Pt on oxide increases dramatically with Ar dry etch time and reaches a few hundred MΩ/sqr. after 8 min, while that of PtSi does not change significantly on Si. Rapid increase of Rs of Pt on oxide is considered to be caused by physical thinning of Pt films by Ar sputtering. In our experiment, the etch rate of Pt is about 1.5 nm/min at RF power of 100 W, however, that of PtSi cannot be determined by step profilometer. From the grazing angle XRD, no noticeable diffraction peaks are detected on oxide and the peaks of Pt (111) and Pt_2Si (211) disappear on Si substrate after 10 min of Ar sputtering. From AES spectra, it is believed that the remained Pt and Pt_2Si formed at the surface are preferentially etched away by Ar ions. Also, SEM and TEM image confirmed the successful formation of ultra-thin PtSi with uniform surface. Therefore, we suggest that selective dry etch process using inert gas is promising technique for formation of ultra-thin Pt salicide.

Session HH: Molecular Electronics II

Friday AM — Room: 140
June 25, 2004 — Location: DeBartolo Hall

Session Chairs: Avik W. Ghosh, Purdue University, W. Lafayette, IN 47907 USA; Theresa S. Mayer, Pennsylvania State University, University Park, PA 16802-2705 USA

8:20 AM Student

HH1, Measuring Conduction Through Molecules Using Step Junction: *Jaewon Choi*[1]; *Kangho Lee*[1]; Sugata Bhattacharya[1]; Saurabh Lodha[1]; David B. Janes[1]; [1]Purdue University, Sch. of Elect. & Computer Engrg., 465 Northwestern Ave., W. Lafayette, IN 47906-2035 USA

One approach for realizing contacts for molecular components is the use of pre-formed metallic contacts with appropriate gap sizes. For various classes of molecules, the required gap can range from 1 ~ 2 nm (single organic molecules) to 20 ~ 50 nm (bio-molecules such as DNA/

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RNA). We report a simple way to build electrodes with nanometer scale gaps, using step junction. The process for step junction fabrication is composed of only conventional micro-fabrication techniques - optical lithography, e-beam evaporation, and liftoff. There is no need to use e-beam lithography, electromigration, or carbon nanotubes to make nanometer scale gaps. The initiation of step junction is a positive slope on positive photoresist profile after exposure and developing. Evaporated and lifted off metal pattern on this profile has negative slope at edge and this negative slope is used as a shadow for the evaporation of subsequent layer. The subsequent layer should be thinner than the first layer to provide a gap between the layers. Because the gap is under the shadow of the thicker, first layer, it's impossible to check the gap size. To get around this problem, we have devised a way denoted as sacrificial step junction. After making the first layer using sacrificial layer and the same material for the second layer, we remove the sacrificial layer to make both electrodes the same thickness. We checked the gap size of sacrificial step junction devices under a field emission scanning electron microscope and the gap size turned out to be 10 ~ 20 nm on average. The step junction also has benefits over conventional break junction (mechanical or electrical) in that we can have different materials on each electrode and easily put thin gate electrode underneath the structure because there is no destructive method used to form the gap. In this presentation, we describe the step junction fabrication and show some illustration of measuring conduction through molecules. Generally the gap is larger than small organic molecules, so we bridge the gap with gold colloids to get conduction through molecules. Occasionally, when there is some defect on step junction, the gap size can be close to a single molecular size. We show 1, 4-benzenedimethanethiol conduction measurement data with or without using gold colloids. There is also a demonstration of gate modulation over molecular conduction with the same devices. It can also be demonstrated that an asymmetric current-voltage curve can be shown with different material electrodes because of unequal coupling of electrodes to molecules. We also discuss the application of step junctions to measure the conduction through a variety of nanoscale species, such as DNA strings, RNA strings, metal coated viruses, and doped molecules with charge transfer dopant. Applications of step junction to chemical sensor and organic transistor will also be discussed.

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HH2, Experimental Current-Voltage Characteristics of DNA and Modified DNA Molecules: *V. Soghomonian*[1]; J. J. Heremans[1]; Hong Chen[1]; B. Hartzell[1]; [1]Ohio University, Depts. of Physics & Astron., Chmst. & Biochmst., & Nanoscale & Quantum Phenomena Inst., Clippinger Labs., Athens, OH 45701 USA

Since the elucidation of its structure and function, DNA has held fascination for applications in electronics. This fascination increasingly holds, in light of the drive toward miniaturization, and integration of electronics and biological systems. The electronic properties of DNA remain controversial. A wide range of resistance values has been reported, ranging from totally insulating to superconducting. Our experimental investigation of DNA conductivity has focused on the random base-sequence lambda DNA molecule. We will show experimental results of the electronic behavior of DNA molecules both physisorbed and chemisorbed onto metal electrodes. We have fabricated Au electrodes of 8 micron separation and 180 nm separation (electron-beam lithography). DNA solutions are deposited onto the electrodes, and to ensure the alignment of the molecules within the gap, we apply an AC aligning field for 30 minutes. After alignment, the device is left in a humidity chamber to enhance the number of DNA molecules bridging the electrodes. The device is then repeatedly washed with deionized water, and blow dried under a flow of nitrogen gas. Physisorbed molecules have no termination, whereas chemisorbed molecules are terminated by disulfide groups. We discuss our results utilizing the above procedure, specifically the effects on the current-voltage (I-V) measurements, of nicks along the phosphate backbone, diverse disulfide termination, and the double helical structure. The procedure of attaching disulfide end groups to lambda DNA molecules generates two nicks in the phosphate backbone. These nicks can be repaired by the addition of a ligation enzyme. The repaired DNA double helices show a close-to-linear current-voltage characteristic, and a DC conductivity estimated at ~ 1x10^-3 S cm^-1. In contrast, the nicked DNA shows pronouncedly non-linear and rectifying behavior, with a conductivity gap of ~ 3 eV. The low-field conductivity of the nicked DNA is approximately a factor 10 lower than the repaired DNA conductivity. To assess affect of disulfide termination on charge transport, we have synthesized duplex DNA molecules labeled with disulfide end groups in two configurations: at the 3-prime ends of opposing strands, or on the 3-prime and 5-prime ends of the same strand. The I-V characteristics were not different, indicating that location of the disulfide is of secondary importance and demonstrating the importance of the double helical structure for charge transport. To further evaluate the influence of the double helix, we measured the I-V of double stranded (dsDNA) versus single-stranded (ssDNA) molecules. The results, performed by single stranding the DNA molecules by two different methods - thermal/ chemical denaturation and enzymatic digestion on the same device- show a conductivity lower by a factor 50 for ssDNA versus dsDNA (supported by NSF 0103034).

9:00 AM Student

HH3, Binary Molecular Materials for Storage, Transport, and Processing of Digital Information: *Yuhui Lu*[1]; Craig S. Lent[1]; [1]University of Notre Dame, Elect. Engrg. Dept., Notre Dame, IN 46556-5637 USA

Molecules can encode binary information directly in their molecular charge configuration, creating a new type of binary molecular material. Information storage, transport, sensor transduction, and processing are all possible at the single-molecule level. Recent experiments[1] have demonstrated field-induced binary switching of such molecules in which electrons move between redox centers composed of ferrocene and ruthenium. Appropriate molecular systems require engineering of the intervalence charge transfer, anchors for bonding to a substrate (in this case silicon), and mechanical "struts" which hold the molecules in the right orientation. More complex assemblies of four ferrocene centers in an appropriate geometry, though not surface-bound, have also been synthesized.[2] We discuss the theory of binary molecular materials and report the results of quantum-chemistry calculations which illuminate the experimental observations and show how intermolecular forces allow information transport and information processing. Both field-induced switching of the two-center molecules and molecule-molecule switching of four-center molecules are examined in detail. We discuss the relation between this type of molecular processing and the quantum-dot cellular automata[3] paradigm. [1]H. Qi, S. Sharma, Z. Li, G.L. Snider, A.O. Orlov, C.S. Lent, and T.P. Fehlner, J. Am. Chem. Soc.125, 15250-15259 (2003). [2]Jiao, J.; Long, G. J.; Grandjean, F.; Beatty, A. M.; Fehlner, T. P.; J. Am. Chem. Soc., 125(25); 7522-7523. (2003). [3]C.S. Lent, Beth Isaksen, IEEE Trans. on Electron Devices 50, 1890-1896 (2003).

9:20 AM Student

HH4, Self-Assembled Monolayer Resist for Electron/Neutral Atom Beam Lithography: *Siyuranga O. Koswatta*[1]; David B. Janes[1]; Arthur K. Mills[1]; Daniel S. Elliott[1]; [1]Purdue University, Dept. of Elect. & Computer Engrg., Box EE344, W. Lafayette, IN 47906 USA

The requirement of ultra-thin resists for high-resolution lithography is well established. Smaller size of the constituent molecules and the reduced amount of forward scattering make self-assembled monolayer (SAM) a very attractive candidate for nanolithography. Transferring of patterned SAM layers onto semiconducting substrates was previously investigated.[1] In the case of using SAM as an electron beam resist, it has been shown that it could act either as positive or negative depending upon the constituent molecules and irradiation conditions.[2,3] The use of neutral atom beams for lithography has also received a lot of attention due to its ability to do high throughput sub-wavelength lithography.[4] We have been investigating the use of SAM resists for electron and neutral atom beam lithography. Our ultimate goal is to develop and optimize processes that would allow nanoscale pattern transfer using neutral Sodium atom beams. We have already demonstrated the use of 1-decanethiol [HS $(CH_2)_9$-CH_3] and 1-octadecanethiol [HS $(CH_2)_{17}$-CH_3] SAM layers for electron beam induced pattern transfer on gold substrates. E-beam evaporated gold samples were O_2 plasma cleaned, and were immediately immersed in 5 mM solutions of the respective alkanethiols in ethanol for at least 72 h at room temperature. Afterwards, they were rinsed in ethanol and blow dried in N_2 before transferring to the SEM (JEOL JSM 6400). The electron beam patterning was performed at 2.5 keV using dosages of 50-500 $\mu C/cm^2$. The patterned samples were subsequently etched using a commercial gold etch solution. It was observed that both 1-decanethiol and 1-octadecanethiol SAM layers act as negative resists with irradiated areas having higher etch resistivity. A separate control sample without an organic monolayer was prepared under similar conditions to ensure that we were not seeing contamination based effects. We have attributed the

negative resist behavior to electron-induced crosslinking as discussed in Ref. 2,3. Crosslinkage of the irradiated SAM layer creates a carbonaceous film that is relatively more etch resistive to wet etchants compared to the non-irradiated areas. Further experiments are underway to characterize and improve the resist behavior of SAM layers. The electron beam exposure conditions (energy/dosage) on the etch selectivity of different alkanethiols will also be investigated. Ultimately, SAM resists for neutral atom lithography would be developed. [1]J. Liu, T. Lee, D. B. Janes, B. L. Walsh, M. R. Melloch, J. M. Woodall, R. Reifenberger, R. P. Andres, Appl. Phys. Lett. 77, 373 (2000). [2]K. Seshadri, K. Froyd, A. N. Parikh, D. L. Allara, M. J. Lercel, and H. G. Craighead, J. Phys. Chem. 100, 15900 (1996). [3]G. Kaltenpoth, B. Völkel, C. T. Nottbohm, A. Gölzhäuser, and M. Buck, J. Vac. Sci. Technol. B 20, 2734 (2002). [4]K. S. Johnson, K. K. Berggren, A. Black, C. T. Black, A. P. Chu, N. H. Dekker, D. C. Ralph, J. H. Thywissen, R. Younkin, M. Tinkham, M. Prentiss, and G. M. Whitesides, Appl. Phys. Lett. 69, 2773 (1996).

Session II: Characterization of Nitride Semiconductors

Friday AM Room: 155
June 25, 2004 Location: DeBartolo Hall

Session Chairs: Christian Wetzel, Uniroyal Optoelectronics, Tampa, FL 33619 USA; Leonard J. Brillson, Ohio State University, Columbus, OH 43210-1272 USA

8:20 AM Student

II1, Demonstration of Non-Degenerate Electron Conduction in InN Grown by Molecular Beam Epitaxy: *Craig Hartley Swartz*[1]; Randy P. Tomkins[1]; Thomas H. Myers[1]; David C. Look[2]; John R. Sizelove[3]; Hai Lu[4]; William J. Schaff[4]; [1]West Virginia University, Dept. of Physics, Hodges Hall, Morgantown, WV 26506 USA; [2]Wright State University, Semiconductor Rsch. Ctr., 3640 Col. Glenn Hwy., Dayton, OH 45435 USA; [3]Air Force Research Laboratory, Matls. & Mfg. Direct., Wright-Patterson AFB, Dayton, OH 45433 USA; [4]Cornell University, Dept. of Elect. & Computer Engrg., Ithaca, NY 14853 USA

Hall-effect measurements, the cornerstone technique for electrical characterization of semiconductors, can be complicated to interpret for Group III-Nitride epilayers, as conduction at the surface or substrate interface or sample inhomogeneity may dominate the transport. Multiple layer analysis of single field Hall measurements requires numerous a priori assumptions. Variable magnetic field Hall measurements can be used to determine, in principle, the influence of the various carriers and give estimates of inhomogeneities. A combination of Quantitative Mobility Spectrum Analysis (QMSA) and Multiple Carrier Fitting (MCF) is a robust approach for identifying the number and types of carriers as well as quantifying the mobilities and concentrations of multiple species. Undoped single crystal InN has always shown n-type conductivity. The source of electrons has not been determined, in part, because all single layer approximation Hall analyses are dominated by degenerate parallel conduction. We will show how a combination of QMSA and MCF techniques along with a multiple-layer approximation can be used to extract the average carrier concentration of the bulk of these thick InN layers. Removing the degenerate component has, for the first time, permitted non-degenerate donor and transport characterization. This represents an important step towards the goal of obtaining high purity and p-type InN. InN layers ranging from 60 to 7500 nm in thickness were grown by molecular beam epitaxy (MBE), and their resistivity and Hall coefficient were measured as a function of magnetic field up to 4.5 T. QMSA and MCF analyses were performed using standard techniques.[1] This approach allowed the separation of bulk and surface electrical properties. A thickness dependence was evident for the bulk electrons, with mobility increasing and carrier concentration decreasing with thickness. This phenomenon is interpreted as an increase in the layer quality with thickness. Analysis of a selection of thick InN samples will be presented. Of particular interest, the bulk electron concentration and mobility in the thickest samples demonstrate significant temperature dependence, decreasing monotonically from high to low temperature. These data have been analyzed with an accurate solution of the Boltzmann transport equation, including dislocation scattering and utilizing the latest accepted values for various fixed parameters. This constitutes the first detailed analysis of nondegenerate (or only partially degenerate) conduction in InN. [1]I. Vurgaftmann, et al., J. Appl. Phys, 84, 4966 (1998).

8:40 AM

II2, A Study of the Interfaces of GaN and AlN Nucleation Layers During GaN Growth on 4H- and 6H- SiC(0001): *Tong-Ho Kim*[1]; Changhyun Yi[2]; Soojeong Choi[1]; Mike Morse[1]; Pae Wu[1]; April S. Brown[1]; Maria Losurdo[3]; G. Bruno[3]; [1]Duke University, Elect. & Computer Engrg., 111 Hudson Hall, Durham, NC 27709 USA; [2]Georgia Institute of Technology, Sch. of Elect. & Computer Engrg., 791 Atlantic Dr., Atlanta, GA 30332 USA; [3]IMIP-CNR, Inst. of Inorganic Methodologies & of Plasmas, via Orabona, 4-70126, Bari Italy

Herein we present a study of the structural and interfacial properties of GaN and AlN nucleation layers on 4H- and 6H-SiC (0001)Si using r.f. plasma-assisted molecular beam epitaxy (MBE). X-ray diffraction, atomic force microscopy, Kelvin-probe microscopy, spectroscopic ellipsometry, and X-ray photoelectron spectroscopy are used to study the influence of AlN and GaN buffer layers on the subsequently-grown GaN, and describe the SiC/buffer and buffer/GaN epitaxial layer interfaces and their impact on the structural properties of the GaN. 4H- and 6H-SiC (0001)Si surfaces are prepared using a Ga flash technique to remove surface oxide.[1,2] Ga of 0.5, 1, and 2 ML is deposited to both SiC surfaces at 650°C and flashed off at 800°C for 1 minute during three cycles.[3] Samples are grown with 10 nm AlN or GaN buffers with each of these preparation approaches. In addition, a 500 nm GaN film is grown on samples with AlN buffer layers. Structural analysis using spectroscopic ellipsometry reveals that the SiC/GaN and SiC/AlN interfaces are characterized by a double interface: (i) a chemical interface, specifically a SiNx layer, forms by subcutaneous nitridation of the 4H-SiC and 6H-SiC substrates during the growth of the GaN and AlN buffers; and (ii) a structural interface, i.e., a pseudomorphic AlN layer and a strained/disordered GaN buffer forms on the SiC substrates before the formation of relaxed AlN and epitaxial GaN buffer layers. It has been found that the Ga surface preparation process strongly affects the surface roughness of both the GaN and AlN buffer layers, and the thickness of the SiNx interface layer. In particular, it is found as we increase the Ga supplied to the surface, the roughness of the buffer layers is decreased, and a thinner SiNx interface layer is created. This is explained through a chemical model that depicts the role of the Ga flash in the modification of the SiC stoichiometry. It has also been found that a dynamics of the SiC/GaN buffer interface exists, i.e., this interface and, hence, the thickness and composition of the SiNx interface layer changes during the growth of GaN itself. The thickness of the SiNx interface layer is greater for the GaN buffer layer than for the AlN buffer layers, and is also greater for the 4H-SiC than for the 6H-SiC substrates. The dynamics of the modification of the SiC/buffer interface has been monitored in real time by spectroscopic ellipsometry. In considering both the chemical and structural properties of the SiC/buffer interface, the optimal interface is created with 6H-SiC/AlN. We also studied the impact of the buffer layer and SiC surface preparation on GaN epitaxial films. We observe interesting correlations between the surface roughness, electric potential and edge dislocation density trend (determined by Williamson-Hall analysis) on the structural quality of GaN epitaxial layers. [1]K. Jeganathan, M. Shimuzu, H. Okumura, F. Hirose, S. Nishizawa, Surface Science 527, L197 (2003). [2]Norio Onogima, Jun Suda, Hiroyuki Matsunami, Jpn. J. Appl. Phys. Vol. 42, L445 (2003). [3]O. Brandt, R. Murralidharan, P. Waltereit, A. Thamm, A. Trampert, H. von Kiedrowski, K. H. Ploog, Appl. Phys. Lett. 75, 4019 (1999).

9:00 AM Student

II3, Capacitance-Voltage and Scanning Probe Studies of InGaN/GaN Quantum-Well Structures: *X. Zhou*[1]; E. T. Yu[1]; D. I. Florescu[2]; J. C. Ramer[2]; D. S. Lee[2]; E. A. Armour[2]; [1]University of California, Dept. of Elect. & Computer Engrg. & Matls. Sci. Prog., San Diego, CA USA; [2]Veeco TurboDisc Operations, Somerset, NJ 08873 USA

InxGa1-xN/GaN quantum-well structures are of outstanding current interest for nitride semiconductor-based visible light emitters. Because of the high densities of point and extended defects in epitaxially grown nitride semiconductor material, characterization and understanding of

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local, nanoscale structure and electronic properties in such devices is essential to achieve effective control over and optimization of device characteristics and performance. We have used scanning capacitance microscopy (SCM) and atomic force microscopy (AFM) to characterize structural and electronic properties of InxGa1-xN/GaN quantum-well structures at the nanoscale. Samples consisting of a 2-3mm n-GaN buffer layer followed by a 30Å InxGa1-xN quantum-well layer capped with 20Å GaN were grown by MOCVD on sapphire substrates. The proximity of the quantum-well layer to the sample surface allows very high spatial resolution to be attained. Macroscopic capacitance-voltage measurements combined with numerical simulations indicate that while the quantum-well layer is depleted at zero bias, either electron or hole accumulation in the quantum-well layer can be induced by application of forward or reverse bias, respectively. SCM and AFM imaging reveals localized depletion of electrons in the vicinity of threading dislocations, indicating that dislocations in these samples contain negative charge in their core. In addition, variations in local carrier density within the InxGa1-xN quantum-well layer are observed that appear to reflect the atomic step structure visible on the GaN surface. A detailed analysis of SCM and AFM image data as well as spatially resolved scanning capacitance spectra suggests that these variations may arise from monolayer fluctuations in InxGa1-xN quantum-well thickness. This observation gives rise to the very interesting possibility of imaging subsurface layer thickness variations at the monolayer level via their influence on local carrier distributions.

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II4, Quantitative Stress Characterization in GaN Films Grown on Patterned Si(111) by Micro-Raman Spectroscopy: *D. Wang*[1]; Y. Dikme[2]; J. Shuo[1]; P. van Gemmern[2]; Y. C. Lin[2]; K. J. Chen[1]; K. M. Lau[1]; M. Heuken[3]; [1]Hong Kong University of Science and Technology, Dept. of Elect. & Elect. Engrg., Clear Water Bay, Kowloon, Hong Kong; [2]RWTH Aachen, Inst. fuer Theoretische Elektrotechnik, Kopernikusstrasse 16, Aachen Germany; [3]RWTH Aachen and AIXTRON AG, Inst. für Halbleitertechnik, Templergraben 55, Kackertstr. 15-17, Aachen D-52074 Germany

Recently, great progress has been made to grow GaN-based materials on silicon substrates that offer benefits such as low-cost, large size, and high thermal conductivity.[1] The thermal mismatch between GaN and Si substrate leads to large tensile stress, and consequently, cracks in GaN films (thickness ~ 2 um) that is not suitable for device structures. Theoretically it was predicted that the maximum crack-free lateral dimension of a 0.7-um-thick GaN film on patterned Si is about 14 um.[2] However, our results and other published data show that much larger crack-free GaN films can be obtained on patterned Si substrates. It is important to quantitatively characterize the stress distribution in GaN films grown on pattered Si with different pattern sizes and different shape patterns. In this paper, we report a quantitative characterization of stress distribution on GaN films grown on patterned Si by spatially resolved micro-Raman spectroscopy which uses the 632.8 nm line of an He-Ne laser for excitation. GaN films were grown by MOCVD on patterned Si(111) substrates with arrays of rectangular stripes, squares, and hexagons with a 3.5-um etched depth and different lateral dimensions. The patterns were prepared by etching the silicon substrates using inductively coupled plasma reactive ion etching. A 32-nm-thick AlN (grown at 720°C) was used as the seed layer for growing GaN films of 1- to 2-um thick. Spatial distributions of tensile stress in the GaN films were mapped out using a Renishaw micro-Raman system in a back scattering geometry. At the center of a square GaN film, the tensile stress is at the peak value and relaxes symmetrically towards the pattern edges and corners due to the free facets and cracks around the corners. This stress relaxation mechanism by the free facets contributes to the successful growth of crack-free large area GaN films. A 10X10 um^2 square showed only a tensile stress of about 0.07 GPa and in some locations the stress becomes undetectable. The tensile stress builds up for a larger pattern unit. The tensile stress is about 0.45 GPa at the center of a crack-free 28X28 um^2 square GaN film. The largest crack-free square for 1-um-thick GaN is about 100X100 um^2, much larger than the theoretically predicted value. These results suggest that GaN on patterned silicon growth technique offers a promising approach of obtaining high-quality GaN-based films in the size of 20 ~ 100 -um wide, which is large enough for LED and HEMT fabrication. [1]Y. Dikme, G. Gerstenbrandt, A. Alam, H. Kalisch, A. Szymakowski, M. Fieger, R. H. Jansen, and M. Heuken, J. Crystal Growth, 248, 578, (2003). [2]S. Zamir, B. Meyler, and J. Salzman, Appl. Phys. Lett. 78, 288 (2001).

9:40 AM Student

II5, Transmission Electron Microscopy and Photoluminescence Study of GaN Epilayers Grown by MOCVD: *Xiaolong Fang*[1]; Subhash Mahajan[1]; [1]Arizona State University, Chem. & Matls. Engrg., Tempe, AZ 85287 USA

We have studied dislocation structures and optical properties of GaN epilayers grown by MOCVD using two different growth protocols by transmission electron microscopy and photoluminescence. GaN epilayer, grown by the conventional two-step growth technique (Sample A, 2.6μm), contains ~4×109cm-2 threading dislocations. By inserting a very thin silicon nitride interlayer on as-grown GaN nucleation layer, threading dislocation density in the GaN epilayer (Sample B, 2.4μm) was reduced to ~3×108cm-2. In Sample A, most of the dislocations emerging from the GaN/sapphire interface thread towards the surface, and no horizontal dislocations were observed in this epilayer. In sample B, almost all dislocations emerging near the GaN/sapphire interface bend to form horizontal dislocations. Most of them terminated at micro-voids near the interface which were induced by greatly enhanced vertical growth at the very beginning and followed by accelerated lateral overgrowth. By high temperature annealing of the Si3N4/GaN-NL composite, exposed areas on the amorphous silicon nitride layer could be formed due to surface roughening. This in-situ patterning induced an epitaxial lateral overgrowth (ELOG) mode for the early stage of GaN overgrowth, which was illustrated by a series of GaN overgrowths with different growth time. Full coalescence was achieved before 500nm thickness. After this thickness, no horizontal dislocations were observed and the threading dislocation density in the GaN overlayer was significantly reduced in Sample B. Room temperature photoluminescence spectra indicate that both epilayers have very good optical quality: very strong bandedge luminescence, narrow FWHMs (~40meV) for the bandedge peaks, and weak yellow luminescence. At room temperature, the bandedge peak intensity for Sample A is about 1.5 times stronger of that of Sample B. However, at low temperature (10K), Sample B shows 3 times stronger bandedge luminescence than Sample A. FWHMs of the bandedge peaks at 10K were 20.0meV and 11.9meV for Sample A and Sample B, respectively. The bandedge peak FWHM at low temperature photoluminescence of Sample B is comparable to some reported values of GaN epilayers grown by ELOG, which indicates very good crystal quality. Excitonic lines in the bandedge region were assigned to free exciton (FE, 3.4885eV for Sample A, 3.4964eV for Sample B), donor-bound exciton (D0XA or I2, 3.4808eV for Sample A, 3.4898eV for Sample B) and acceptor-bound exciton (A0XA, 3.4742eV for Sample A, 3.4840eV for Sample B) transitions. The LO replica of D0XA were also assigned. These peak positions indicated that both sample are under compressive biaxial stress. Furthermore, in both room temperature and low temperature, the yellow peak intensities of Sample B are weaker than that of Sample A. The support of this work by AFOSR is gratefully acknowledged.

10:00 AM Break

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II6, Intra d-Shell Photoluminescence Transitions of Mn^{4+} Ions in GaN:Mn Codoped with Mg Acceptors: *Bing Han*[1]; Melville P. Ulmer[2]; Bruce W. Wessels[1]; [1]Northwestern University, Dept. of Matls. Sci. & Engrg. & Matls. Rsch. Ctr., Evanston, IL 60208 USA; [2]Northwestern University, Dept. of Physics & Astron., Evanston, IL 60208 USA

Manganese doped GaN, a magnetic semiconductor, has been extensively studied since the observation of room temperature ferromagnetism. Prior calculations indicate that Mn forms multiple deep levels in the band gap of GaN, and the ferromagnetic properties of GaN:Mn strongly depend on the charge state of Mn ions. Due to the deep level nature of Mn in GaN, GaN:Mn is always highly resistive. However, the electronic states of Mn related deep levels in GaN are not well understood. To enhance the ferromagnetism and increase its conductivity, codoping GaN:Mn with shallow acceptors (Mg) is required. In this work the properties of Mn in GaN:Mn-Mg epitaxial layers are investigated using photoluminescence (PL) and photoluminescence excitation (PLE) spectroscopies. In heavily Mg codoped GaN:Mn a series of strong, sharp PL transitions at 1 eV is observed, which are attributed to the intra d-shell transition of Mn^{4+} ions. The $^4T_2(F)$-$^4T_1(F)$ transition is involved. Th e PLE spectrum of the 1eV Mn^{4+} luminescence reveals intra-center excitation

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processes via the excited states of Mn^{4+} ions. PLE peaks resolved at 1.7 and 2.3 eV are attributed to the intra d-shell $^4T_1(P)$-$^4T_1(F)$ and $^4A_2(F)$-$^4T_1(F)$ transitions of Mn^{4+}, respectively. In addition to these intra-shell excitation processes, a broad PLE band involving the $Mn^{3+/4+}$ charge transfer state is observed, which is well fitted by the Lucovsky model. The position of the $Mn^{3+/4+}$ level is 1.1 eV above the valence band as determined from the onset of this PLE band. The position of the $Mn^{3+/4+}$ level is consistent with the theory using ab initio calculations. Our work indicates Mn^{4+} is stabilized in Mn-Mg codoped GaN when the Fermi energy is lower than 1.1 eV above the valence band.

10:40 AM Student

II7, The N-Face GaN Etch Property by Photo-Electro-Chemical (PEC) Wet Etching and its Application for High Efficiency GaN LEDs: *Yan Gao*[1]; Tetsuo Fujii[2]; Rajat Sharma[1]; Kenji Fujito[2]; Mike Craven[1]; James S. Speck[1]; Steven P. DenBaars[1]; Shuji Nakamura[1]; Evelyn Hu[1]; [1]University of California, Matls. Dept., Santa Barbara, CA 93106 USA; [2]University of California, NICP/ERATO JST, Santa Barbara, CA USA

Recently, there has been much progress in understanding Photoelectrochemical (PEC) wet etching on GaN; this includes increased understanding of the effect of defects on etch rate and etch morphology, the critical issues involved in selective PEC etching, etching of crystal faces other than (0001), and their resulting etch morphologies. Initial studies of PEC etching on the LEO (Lateral Epitaxial Overgrowth) a-plane GaN/r-plane sapphire was explored to understand the effects of polarity (N-face vs. Ga-face) and dislocation dependence on the PEC etch process. The LEO a-plane GaN sample allowed us to simultaneously etch low ("wing" region) and high dislocation ("window" region) density N-face and Ga-face material under the same etch conditions. An aqueous solution of KOH was used as an etch electrolyte in this study. The dislocations appeared to substantially retard the PEC etching process: the "window" region etched much more slowly than the "wing" region. Strong dependence of etching on crystal face was also observed. The N-face exhibits crystallographic etching with {101-1-} hexagonal pyramids, even in the absence of light, while no measurable etching occurred on the Ga-face, for the conditions we employed. In addition, the (1-1-22-) plane formed an etch-stop plane, revealing an atomically smooth etched surface. This study will further seek to understand the control of etch morphology with respect to crystallographic orientation, defect density and doping of the substrate. Such studies will be critical in a number of device applications utilizing PEC etching. For example, we have already used PEC etch-roughening of N-face GaN to increase the light extraction efficiency of GaN LEDs by a factor of 2-3.

11:00 AM Student

II8, Optical Modes in Mushroom-Shaped GaN/InGaN Microdisk Resonators Fabricated Using Photoelectrochemical Etching: *Elaine D. Haberer*[1]; Rajat Sharma[1]; Cedrik Meier[1]; Andreas R. Stonas[2]; Steven P. DenBaars[1]; Shuji Nakamura[1]; Evelyn L. Hu[2]; [1]University of California, Matls. Dept., Santa Barbara, CA 93106 USA; [2]University of California, Elect. & Computer Engrg. Dept., Santa Barbara, CA 93106 USA

We have fabricated microdisks with InGaN active layers, and observed resonant modes with significant Q values. Microdisks have been used in GaAs and InP materials to form extremely high quality resonators for optical devices, ultimately resulting in low-threshold lasing. A microdisk is a thin semiconductor disk surrounded by a lower index material. Through total internal reflection, the circular geometry of the disk gives rise to low loss whispering gallery modes (WGMs) which propagate along the periphery of the disk. One of the challenges in forming a GaN microdisk is the ability to optically isolate the disk. In other material systems optical isolation of the WGMs is generally achieved by using a selective wet etch to lift-off or undercut the disk, forming a pedestal. Because GaN-based materials do not have a simple wet etch, we have chosen to use InGaN/GaN bandgap selective photoelectrochemical etching (PECE) to fabricate our microdisks. In this technique, the sample is immersed in an electrolyte solution and exposed to filtered light from a Xe lamp. The filter allows photons with energy less than the bandgap of GaN to pass, generating electrons and holes in the InGaN. The holes drift to the InGaN/electrolyte interface where they drive the photo-induced etch. We have fabricated thin GaN microdisks with a multiple QW active region, as well as AlGaN cladding layers. The 2.5 micron diameter, freestanding disks are supported in the center by a low composition InGaN/InGaN superlattice pedestal forming a mushroom-shaped structure The disk undercut was created using PECE in a dilute HCl electrolyte solution. These disks have been optically pumped using a He-Cd CW laser and a microscope objective lens in confocal geometry with a spot size of 2-5 microns in diameter. Resonant modes with Q values near 1000 were observed at pump power densities near 5 kW/cm^2. Having modeled the disk structure using a numerical FDTD software package, we believe that the observed modes are a combination of radial and whispering gallery modes. The authors would like to acknowledge the Mitsubishi Chemical Corporation for supporting this research.

Session JJ: Contacts to Nanotubes, Nanowires and Organic Films

Friday AM — Room: 101
June 25, 2004 — Location: DeBartolo Hall

Session Chairs: Suzanne E. Mohney, Pennsylvania State University, Dept. of MSE, University Park, PA 16802 USA; Lisa M. Porter, Carnegie Mellon University, Dept. of MSE, Pittsburgh, PA 15213-3890 USA

8:20 AM Invited

JJ1, Contacts to Carbon Nanotubes for Electronic and Spin-Electronic Devices: *Bruce William Alphenaar*[1]; [1]University of Louisville, Elect. & Computer Engrg., Lutz Hall Rm. 409, Louisville, KY 40292 USA

Due to their outstanding electrical and structural properties, carbon nanotubes have been considered for a variety of nanometer scale electronic and spin electronic device applications. One problem hindering nanotube device development however, is the difficulty in making reproducible low resistance electrical contacts to either single wall or multi wall carbon nanotubes. In this talk, I will describe recent experiments that reveal the influence that the contact material and contact interface conditions can have on the electrical properties of carbon nanotube devices, and provide possible methods for optimizing contacting conditions. Carbon nanotube spin electronics relies on the injection and detection of electron spin across a ferromagnetic/nanotube interface. The spin polarization can change in magnitude or direction according to the local surface potential. Since the contact area between the ferromagnet and the nanotube is so small, local fluctuations in interface conditions caused by variations in the domain configuration at the interface can also have a dramatic influence on individual device behavior. Temperature dependence measurements of the resistance switching in ferromagnetically contacted nanotubes show that the sign of the resistance switch can change from positive to negative as the temperature increases. This suggests that the sign of the injected spin polarization depends on the thickness of a non-ferromagnetic dead-layer between the contact and the nanotube. To observe larger and more reproducible spin mediated effects in carbon nanotube devices, improvements in the purity of the ferromagnetic interface layer are required. One possibility for low resistance and reproducible nanotube contacts is to incorporate metals that are liquid near room temperature, such as Ga or Hg, into the electrical contacts. We have developed a unique method to produce highly transmissive liquid metal contacts to carbon nanotubes that allows direct measurement of the influence of the contact on the nanotube conductance. Gallium is deposited onto standard gold nanotube contacts, where it gradually spreads to coat the contact region. The two-terminal multi wall nanotube conductance increases by as much as 1.4e^2/h during the transition from gold to gallium contacts, and approaches 2e^2/h at room temperature, with a current density of 2 x 10^8 A/cm^2. Surprisingly, the conductance is independent of the contact area or contact separation, leaving open the possibility that transport is ballistic in multi wall nanotubes.

9:00 AM

JJ2, Measuring the Specific Contact Resistance of Contacts to Semiconductor Nanowires: *Suzanne E. Mohney*[1]; Marco A. Cabassi[2]; Soham Dey[1]; Yanfeng Wang[2]; K. K. Lew[1]; Joan M. Redwing[1]; Theresa S. Mayer[2]; [1]Pennsylvania State University, Dept. of Matls. Sci. & Engrg. & Matls.

Rsch. Inst., Steidle Bldg., Univ. Park, PA 16802 USA; [2]Pennsylvania State University, Dept. of Elect. Engrg., Univ. Park, PA 16802 USA

Ohmic contacts to semiconductor nanowires will be an essential component of many new nanoscale electronic devices. In this presentation, we describe methods of measuring the specific contact resistance (or contact resistivity) of metal contacts to semiconductor nanowires, and we provide examples of the measurements we have made. Equations for extracting specific contact resistance from several different test structures have been developed by treating the metal/semiconductor contact as a transmission line, leading to the development of new equations analogous to those used when describing contacts to semiconductor thin films using the transmission line model (TLM). The modified or nanowire TLM equations can be applied to several different metal/semiconductor nanowire test structures, and the advantages and disadvantages of various geometries for testing the contacts is discussed. To fabricate test structures using the preferred four-terminal approach, silicon nanowires have been aligned using field-assisted assembly and contacts fabricated. Finally, the contact resistance, specific contact resistance, and semiconductor resistivity have been extracted from these measurements. A specific contact resistance of 1.8×10^{-4} Ohm-cm^2 has been measured for a p-type Si nanowire with a diameter of 136 nm and resistivity of 1.4 Ohm-cm. Other contact metallizations and contacts to nanowires of other diameters and doping densities are also under investigation.

9:20 AM Student

JJ3, Contact Resistance in Nanowire Characterization: *Ryan A. Munden*[1]; Ilona Kretzschmar[1]; Eric Stern[1]; Aric Sanders[1]; Mark A. Reed[1]; [1]Yale University, Dept. Elect. Engrg. & Applied Physics, 15 Prospect St., Rm. 509, New Haven, CT 06511 USA

Nanowires made of many different electronics materials such as metals, semiconductors, and insulators have been reported. Despite the hype about them, all of these materials require full electronic characterization before they can become truly useful in designing and implementing new devices. Until now, most measurements reported on the electrical characteristics of nanowires have been based on one, or at most a few, devices that are painstakingly contacted via e-beam lithography to a single "known" wire, or via random shadow mask or optical lithography techniques, which require subsequent inspection via high resolution microscopy. We have developed a lithographic method, which enabled us to successfully characterize the electronic properties of several different types of metal and semiconducting nanowires. 1 um sized metal contacts are fabricated via optical lithography onto pre-grown, randomly dispersed nanowires. Two-point contacts are easily obtained in large quantities, which allow us to determine characteristic current-voltage, I(V), statistics for GaN, In2O3, and other types of nanowires. We have successfully contacted very short nanowires with lengths of two or three microns. With the same method but longer nanowires, four-point contacts should be achievable, which will allow full characterization of the conductance properties of the nanowires independently of the contact resistance. From these measurements we can also obtain carrier densities in these nanowires. Our contact method has been developed to use the high throughput of optical lithography, combined with automated electrical testing to locate nanowire devices for further study. This allows us to potentially contact hundreds of individual nanowires, and rapidly obtain statistical data on I(V) characteristics circumventing tedious alignment and/or viewing procedures. From the statistical analysis of the I(V) data properties of the nanowires can be determined reliably, rather than relying on the results of a single specimen. This novel new method for contacting nanostructures allows us to obtain enough statistical data to provide feedback to the nanowire growth process in order to optimize the growth parameters. We have also been able to statistically investigate the parameters for contacting different nanowires with different types of metals, and the effects of thermal annealing and cryogenic cooling on those wires, their conductance behavior, and their contacts.

9:40 AM Student

JJ4, Studies on Metal Contacts to InP Nanowires: Jenny Hu[1]; David Aplin[1]; Clint Novotny[1]; Paul K.L. Yu[1]; Edward T. Yu[1]; Deli Wang[1]; *S. S. Lau*[1]; [1]UCSD, ECE Dept., 9500 Gilman Dr., La Jolla, CA 92093 USA

Semiconductor nanowires are very attractive building blocks for the "bottom-up" assembly of nanoelectronic and nanophotonic systems since they can function both as nanoscale devices and interconnects.[1] Materials syntheses have been well studied and the control on dimesion and electronic properties of the nanowires in a predictable manner can be achieved during growth.[2,3] A variety of nanodevices have been fabricated such as transistors,[3,4] light emitting diodes,[5] and photodetectors,[6] but less attention has been paid to in-depth study on making contacts to the semiconductor nanowires to date. In this paper, we describe studies on contact resistance to InP nanowires using a method similar to the transmission line method (TLM). InP nanowires (both p and n types) were synthesized using metal-organic chemical vapor deposition (MOCVD) via vapor-liquid-solid nanowire growth. The derived contact resistances are compared and rationalized in terms of the results reported in the literature for bulk samples. [1]Lieber, C. M., Sci. Am., 2001, 285(3), 58. [2]Cui, Y.; Lauhon, L. J.; Gudiksen, M. S.; Wang, J.; Lieber, C. M. Appl. Phys. Lett., 2001, 78, 2214; Gudiksen, M. S.; Wang, J.; Lieber, C. M. J. Am. Chem. Soc., 2000, 122, 8801. [3]Cui, Y.; Duan, X.; Hu, J.; Lieber, C. M. J. Phys. Chem. B, 2000, 104, 5213; Yu, J. Y.; Chung, S. W.; Heath, J. R. J. Phys. Chem. B, 2000, 104, 11864. [4]Cui, Y.; Lieber, C. M. Science 2001, 291, 851; Cui, Y.; Zhong, Z.; Wang, D.; Wang, W. U.; Lieber, C. M. Nano Lett., 2003, 3, 149. [5]Duan, X.; Huang, Y.; Cui, Y.; Wang, J.; Lieber, C. M. Nature, 2001, 409, 67; Zhong, Z.; Qian, F.; Wang, D.; Lieber, C. M. Nano lett., 2003, 3, 343. [6]Wang, J.; Gudiksen, M. S.; Duan, X.; Cui, Y.; Lieber, C. M. Science 2001, 293, 1455.

10:00 AM Break

10:20 AM Invited

JJ5, Making Electrical Contacts to Organic Materials by Soft Lithography: *Julia W.P. Hsu*[1]; Tae-Woo Lee[2]; Jana Zaumseil[3]; Yueh-Lin Loo[4]; Zhenan Bao[5]; John A. Rogers[6]; [1]Sandia National Laboratories, PO Box 5800, MS 1415, Albuquerque, NM 87185 USA; [2]Samsung Advanced Institute of Technology, Elect. Matls. Lab., Mt. 14-1, Nongseo-Ri, Giheung-Eup, Yongin-Si, Gyeonggi-Do 449-712 Korea; [3]Cambridge University UK; [4]University of Texas, Dept. of Chem. Engrg., Austin, TX 78712 USA; [5]Stanford University, Dept. of Chem. Engrg., Stanford, CA 94305 USA; [6]University of Illinois, Urbana, IL USA

Making electrical contacts to organic materials is a challenging roadblock to the advance of organic electronics. Traditional methods for making electrical contacts to semiconductors, which involve vapor deposition of metals followed by thermal annealing, is not applicable and can even degrade the performance of the organic materials. In this talk, I will discuss two examples of making electrical contacts to organic materials by soft lithography techniques. The first example is using nano-transfer printing (nTP) to make electrical contacts to molecular monolayers. In nTP, chemical bonding occurs between the molecules and the electrodes. To understand the nature of the electrical contact in these molecular junctions, we performed current-voltage (I-V), capacitance-voltage (C-V), and internal photoemission (IPE) experiments. We compare the transport results of the nTP diodes with those devices with evaporated top contacts. Most dramatically, the IPE energy dependence for the evaporated junctions show quadratic energy dependence characteristic of metal-semiconductor Schottky barriers, while the IPE yield of the nTP junctions depends exponentially on E, signifying electron emission from a disordered material. Thus, fundamentally different transport mechanisms are at work depending on the fabrication of the contacts. Physical soft contact lamination method was explored to fabricate organic light-emitting didoes (LEDs) in the second example. In the soft contact lamination (ScL) method, PDMS stamps coated with thin Au films of patterns defined using shadow masking, photolithography, micro contact printing, or relief molding were laminated onto MEH-PPV films on ITO substrate. In this case, only van der Waals interaction exists between the Au electrodes and the electrolumescent organic films. When compared with ITO/MEH-PPV/Au devices with evaporated electrodes, we found an order of magnitude improvement in external quantum efficiency for LEDs with laminated Au electrodes. We also fabricated high-efficiency (~ 2.5 % ph/el) soft-contact laminated LEDs with Au electrodes by employing the MEH-PPV/organic-salt blend. An added advantage of soft lithography techniques is that the techniques can be naturally extended to fabricating nanoscale devices. We will show nanometer-size emitting regions using the laminated contact approach.

11:00 AM

JJ6, Current Injection Mechanism in Metal/Molecular-Organic-Semiconductor/Metal Sructures: Ruchi Agrawal[1]; Ajit Kumar Mahapatro[1]; *Subhasis Ghosh*[1]; [1]Jawaharlal Nehru University, Sch. of Physical Scis., New Mehrauli Rd., New Delhi, Delhi 110067 India

The success of first organic electroluminescent devices based on small molecule tris-(8-hydroxyquinolate)-Al(Alq)[1] and polymer poly(p-phenylene vinylene)(PPV)[2] lead to tremendous amount of research devoted in understanding the transport properties of organic semiconductors and the operating principles of devices based on these materials. The physics of current transport processes is not understood in detail in molecular organic semiconductors(MOS), which are quite different from the crystalline inorganic semiconductors. It was early realized that charge injection in a MOS is an extremely important issue, because (i) the device characteristics of two and three terminal devices depend on the efficiency of charge injection from metal electrode to MOS in case of electrical devices, (ii) in case of optical devices, unbalanced charge injection reduces the conversion efficiency of current to light and finally (iii) the understanding of charge injection mechanism in MOS. In their simplest configuration, an organic semiconducting material is sandwiched between two metal electrodes. In this work, we present detail experimental results on current injection from different metal electrodes into hole transport MOS, like metal-phthalocyanines and electron transport MOS like metal chelates(Alq). The current-voltage(J-V) characteristics and current injected at the contact are investigated as a function of energy barrier, thickness of organic semiconductor and temperature. We have varied the work function of anode electrode and find that current is injection limited when the Schottky energy barrier is high and current is space charge limited when Schottky energy barrier is low. The contribution to injection currents from thermionic and tunneling have been varied by varying the thickness of the organic semiconductors. It has been found that the injection current in case of devices based on thick hole transport MOS, like copper-phthalocyanine layer is proportional to hole mobility and can be simulated with a modified Schottky J-V relation,[3] but the current injection in case of devices based on thick electron transport MOS, like Alq, cannot be described with this J-V relation. In case of Alq, it has been found, in spite of the presence of a large injection barrier, injection limited current exhibits weak temperature dependence. This is in contradiction with Schottky or modified Schottky J-V relation based on classical thermionic injection models. We have shown that the thermally assisted jump from the metal electrode to the hopping sites in MOS is the current injection mechanism in case of Alq. It seems the dipole moment of the molecule and the interface between MOS and metal electrode decide the current injection mechanism in metal/MOS/metal structures. [1]Appl. Phys. Lett. Vol. 51, pp 381-383 (1987). [2]Nature, Vol. 347, pp 539-341 (1990). [3]IEEE Trans. Elec. Dev. Vol 48, pp1911-1914 (2001); Appl. Phys. Lett. Vol. 80, pp 4840-4842 (2002).

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