Session DD: Oxide Semiconductor Heterojunction Diodes

Friday AM
June 25, 2010

Room: 102
Location: University of Notre Dame

Session Chairs: Deli Wang, Univ of California, San Diego; Jamie Philips, Univ of Michigan

8:20 AM

DD1, Ultraviolet Photodetectors with Novel Oxide Thin Films: *Shizuo Fujita*[1]; Takumi Ikenoue[1]; Naoki Kameyama[1]; Takayoshi Oshima[1]; [1]Kyoto University

A variety of wide band gap oxide semiconductors, which are recognized as stable and environmental-friendly materials, can meet various demands for detectable wavelength, sensitivity, cost, and endurance of ultraviolet photodetectors, in contrast to III-nitride semiconductors which always needs high-cost and dangerous sources for their growth. In this presentation, we report several oxide semiconductors we have developed as the materials for ultraviolet photodetectors. Ga_2O_3 possesses large band gap of 4.8 eV (258 nm), which is suitable for UV-C photodetectors. HIgh quality Ga_2O_3 substrates allow the Schottky-type photodetectors using high-resistive layers formed on the substrates by thermal annealing in oxygen atmosphere. The photodetector exhibited the photoresponsivity of 0.037 A/W at 250 nm with the external quantum efficiency of 18 %. The photodetector was capable of detecting solar-blind light of as weak as 1 nW/cm^2 from the flame in normal room lighting. Robust properties of Ga_2O_3 against defect generation have allowed hundred-hours operation without noticeable degradation as a power monitor for a low-pressure mercury lamp (254nm, 40 mW/cm^2). A SnO_2 semiconductor, whose band gap is about 4 eV (310 nm), is desirable for UV-B photodetectors. Molecular beam epitaxy (MBE) and thermal annealing resulted in high resistive (5×10^6 cm) SnO_2 layers on sapphire substrates. Forming interdigital Au/Ni electrodes on the SnO_2 layer, the sample operated as a UV-B photodetector with the photoresponsivity of 0.023 A/W at 290 nm with the external quantum efficiency of 10%. Oxide semiconductors can be grown by low-cost and solution-based growth techniques, which allow simple fabrication process and inexpensive devices. With the ultrasonic spray mist chemical vapor deposition where safe and inexpensive sources can be used in a simple system, Schottky-type photodetectors of PEDOT:PSS/ZnMgO were successfully fabricated on glass substrates using metal mask patterning. In spite of the low cost and low power consumption processes for the device fabrication, the photodetectors exhibited reasonably high photoresponsivity, for example, 0.074 A/W at 320 nm with the external quantuim efficiency of 36.5%. The cut-off wavelengths were tunable between 370 and 300 nm by the Mg concentrations in ZnMgO. We believe that oxide semiconductors can be key materials for the photodetectors of ultraviolet light of a variety of wavelengths and intensity.

8:40 AM Student

DD2, Polarization-Sensitive Schottky Photodiodes Based on A-Plane ZnO/ZnMgO Multiple Quantum-Wells: *Gema Tabares*[1]; Adrian Hierro[1]; Christiane Deparis[2]; Christian Morhain[2]; Jean-Michel Chauveau[2]; [1]ISOM-Dept. Ingenieria Electrica, Universidad Politecnica de Madrid, Spain; [2]CRHEA-CNRS

ZnO is attracting much attention since it is a perfect candidate for various sensors, including piezoelectric devices and UV photodetectors. Particularly, polar-ZnO shows spontaneous polarization and a piezoelectric field along the c-direction, so in order to exploit its polarization potential, nonpolar ZnO whose polar axis lies in the growth plane is a good candidate for developing polarization-sensitive photodetectors (PSPDs). We present here an analysis of the spectral response dependence on light polarization of Schottky photodiodes based on non-polar a-plane ZnO/MgZnO multiple quantum wells (MQW) grown on R-plane sapphire by molecular beam epitaxy. The structures have varying QW thickness, from 1.5 to 5.6 nm, and varying Mg contents in the barrier, from 29 to 40%, allowing the absorption edge to be tuned from 3.38 to 3.51 eV. Semitransparent Au-Schottky diodes (100 Å) with an excellent rectifying behavior have been achieved through optimization of the surface passivation with H2O2. Coplanar to the Schottky contacts, extended back ohmic contacts have been defined with a Ti/Al/Ti/Au layer. Under illumination with above quantum-well excitation energy the I-V characteristics become non-rectifying, with large saturation currents and ideality factors. The origin of this I-V degradation under illumination will be addressed through analysis of the spectral and time response of the detectors. The photodiodes present a sharp absorption edge in their responsivity characteristics. As an example, the responsivity of the ZnO/ZnMgO (MQW) photodiode shows a sharp onset at 3.38 eV, for un-polarized light illumination conditions and a UV/VIS rejection ratio of 10^4. In order to analyze the polarization sensitivity of the photodiodes, a Glan-Taylor prism was used to linearly polarize the light. The normalized spectral response of the ZnO/$Mg_{0.37}$ $Zn_{0.63}O$ MQW-photodiode for polarization angles between 90º and 0º respect to the c-axis shows absorption edges at 3.35 eV (E perpendicular to the polar axis, E-c) and 3.37 eV (E parallel to the polar axis, E||c), respectively. The responsivity shows a clear shift of the absorption edge by ~23 meV, with a maximum differential responsivity ($R\text{-}/R_{\|}$) of 0.38 at 3.37 eV. Using the un-normalized responsivities, the PSPD has ($R\text{-}/R_{\|}$)max= 5 mA/W. At 3.37 eV the polarization sensitivity contrast ($R\text{-}/R_{\|}$) reaches ~2.5. Taking into account the accumulated residual strain at the QWs, the excitonic resonances for E-c and E||c light polarization conditions may be assigned to the E_1 and E_2 transitions, respectively.

9:00 AM

DD3, A New Approach to Make ZnO-Cu_2O Heterojunctions for Solar Cells: *Aurelien Du Pasquier*[1]; Ziqing Duan[1]; Yicheng Lu[1]; [1]Rutgers State University

Recently, the ZnO-Cu_2O heterojunction based solar cells have attracted considerable research interests due to the low-cost and abundance of the materials and favorable electronic properties. Cuprous oxide (Cu_2O) is a p-type semiconductor with a direct bandgap energy of 2.1 eV. Cu_2O acts as a photovoltaic absorber that can be grown by various methods including thermal oxidation of Cu foils [1], MOCVD [2], or electrochemical deposition [3].It has been shown that Cu_2O-ZnO p–n heterojunctioncan be made by deposition of p-Cu_2O onto n-ZnO using electrochemical deposition [4] or magnetron sputtering [5]. Several Transparent Conducting Oxide/Cu_2O heterojunctions show good photovoltaic results. For example, solar power conversion efficiency of 1.2% was obtained with Al-doped ZnO-Cu_2O [6]; the highest efficiency reported to date was 2% in a sputtered MgF2/ ITO/ZnO/Cu_2O device using MgF_2 as antireflection coating [7]. We report a new approach to make ZnO-Cu_2O heterojunctions. Previously, we demonstrated a novel three-dimensinal (3-D) ZnO photoelectrode consisting of single crystalline ZnO nanotip array integrated with a Ga-doped ZnO (GZO) transparent conducting oxide (TCO) film [8,9]. In the current fabrication process, ZnO nanotips are grown by MOCVD on FTO substrates, then copper is electrochemically deposited on ZnO, and further converted to Cu_2O via a treatment in boiling copper sulfate solution. Through this process, pure Cu_2O phase is obtained, verified by the XRD measurements. Such heterojuction solar cells display a high (>80%) quantum efficiency of photocurrent, 400 mV open circuit voltage and 40 microA/cm^2 short-circuit current. The effects of deposition sequence (ZnO-Cu_2O vs. Cu2O-ZnO) and ZnO morphologies (dense films vs. nanotips) on I-V characteristics of FTO/ZnO-Cu_2O/Au devices will be presented and discussed. 1.N.A. Mohemmed Shanid, M. Abdul Khadar, Thin Solid Films 516 6245–6252 (2008). 2. G. G. Condorelli, G. Malandrino, and I. Fragala, Chem. Mater. 6, 1861 (1994). 3. Y. Tang, Z. Chen et al., Materials Letters 59 (2005). 4. D.K. Zhang, Y.C. Liu, Y.L. Liu, H. Yang, Physica B 351, 178 (2004). 5. K. Akimoto, S. Ishizuka, M. Yanagita, Y. Nawa, G.K. Paul, T. Sakurai, Sol. Energ. 80 715 (2006). 6. H. Tanaka, T. Shimakawaa, T. Miyata, Thin Solid Films 80 469-470, (2004). 7. A. Mittiga, E. Salza, F. Sarto et al., Appl. Phy. Lett. 88, 163502 (2006). 8. A.Du Pasquier, H. Chen and Y. Lu, Appl. Phy. Lett. 89 (1), 253513 (2006). 9. H. Chen, Z. Duan Y. Lu and A. Du Pasquier, J. Electronic Mat. 38, (2009).

9:20 AM Student

DD4, Double Heterojunction Metal-Semiconductor-Metal Photodetector Using ZnO/Si Structure: *Tingfang Yen*[1]; Juhyung Yun[1]; Sung Jin Kim[1]; Alexander Cartwright[1]; Wayne Anderson[1]; [1]SUNY-Buffalo

High photocurrent generation has been obtained by using a ZnO/Si double heterojunction photodetector (DHP) with metal–semiconductor-metal (MSM) structure contact. Two back to back ZnO/Si heterojunctions have been formed with two interdigitated Au/Yb contacts deposited upon ZnO with contact spacing of 2 μm. The I-V curve displayed symmetric MSM characteristics and photocurrent was one magnitude larger for n-ZnO/p-Si and two magnitudes larger for n-ZnO/n- Si than the sum of photocurrent generated from each monolayer of ZnO and Si at 20V. The high sensitivity of photocurrent has been achieved with n-ZnO/n-Si DHP showing photo to dark current ratio of 5053 and responsivity of 3.13 A/W. Two main reasons for this greatly increased photocurrent are discussed. An avalanche multiplication process occurs when applied voltage exceeds flat band voltage. Thus, under illumination, the device acts like an avalanche photodiode with internal photocurrent gain. The avalanche multiplication was obtained by gain versus bias voltage characteristic for different temperatures. Since the thickness of lightly doped ZnO is much less compared to the heavily doped n-Si, higher built-in electric field in the ZnO regions can separate electron-hole pairs and cause a tunneling current. In addition, photoluminescence result shows less defect emission with ZnO/Si structure than ZnO/SiO_2. Thus, the spectral response result was improved because of better quality of ZnO thin film with ZnO/Si structure, the ZnO acting as a passivation layer for the Si, and larger photon absorption provided by ZnO.

9:40 AM Student

DD5, A Study of Indium Doped-ZnO/p-Si(111) Diode Characteristics with Various In Mole Fraction: *Jong Hoon Lee*[1]; Hong Seung Kim[1]; Bo Ra Jang[1]; Ju Young Lee[1]; Nak Won Jang[1]; Bo Hyun Kong[2]; Hyung Koun Cho[2]; Won Jae Lee[3]; [1]Korea Maritime University; [2]Sungkyunkwan University; [3]Dong-eui University

ZnO material is attractive for using optical devices, solar cells, transparent conducting oxide electrodes, and transparent thin film transistors because of its wide band gap (3.37 eV) energy and large exciton binding energy (60 meV). Recently, although the results of p-type ZnO film have been reported, it is still difficulty to growth of reliable p-type ZnO material due to the low solubility of the dopant and the highly self-compensating process upon doing. For these reasons, the p-n junction structure have attempted with other p-type materials such as p-GaN, p-SiC and p-Si. Especially, the p-type silicon substrate has various advantages such as large area substrate, low cost and excellent Si-based technology. An un-doped ZnO material has dominant n-type conductivity at room temperature due to the native defects such as zinc interstitials (Zn_i) and oxygen vacancies (V_o), or present of hydrogen. A study of the ZnO about the carrier concentration is to obtain high carrier concentration (over 10^{20} /cm^3) for substitution of indium tin oxide. The high carrier concentration of n-type ZnO can be obtained as high doping (over 1 at. %) in the ZnO with group III donor impurities such as Ga, Al and In. As the p-n junction diode need to the properties of semi-conductor, we attempted low doping in the ZnO films with indium (0.6, 1, 5, and 10 at. %) for a stable n-type properties on diode characteristics. In this work, our aim is to investigate relationship between changed dido characteristics and effect of In-doping in the ZnO. The In-doped ZnO was deposited by using a pulsed laser deposition system with In-doped ZnO target. The structural characteristics of In-doped ZnO films were investigated by XRD and TEM. The electrical properties of In-doped ZnO films were measured by Hall measurement and the diode characteristics were investigated by current-voltage measurement. The electrical properties of In-doped ZnO films were changed to increase the carrier concentration up to 3.0×10^{19} and to decrease resistivity up to the 1.5×10^{-2} -cm. Also, the diode characteristics were considerably change by the effect of In-doping. Especially, In-doped ZnO/p-Si diodes show very low reverse current density about 2.8×10^{-6} A/cm^2 (In 10 at. %) at -5 V and high on-off ratio (In 10 at. %) about 2.5×10^{-6} at ±5 V. The hetero structure diode exhibited typical current-voltage behaviors with turn-on voltages of 1.8 ~ 4.6 V and with series resistance of 37 ~ 99 Ω. The different diode characteristics may be related on the changed structures of ZnO films by indium doping and we discuss about the relationship between the diode characteristics and the effect of In-doping in the ZnO films. (NIPA-2009-C1090-0903-007 & Human Resource Training Project for Strategic Technology).

10:00 AM Student

DD6, Effects of High - Energy Electron Irradiation on Pd/ZnO/Si MSM Photodetector: Conduction Mechanisms and Radiation Resistance: *Franklin Catalfamo*[1]; Tingfang Yen[1]; Juhyung Yun[1]; Wayne Anderson[1]; [1]University at Buffalo

ZnO/Si metal-semiconductor-metal (MSM) photodetectors with palladium contacts were fabricated and subjected to high-energy electron beam irradiation (HEEBI) in order to observe the effects of space or other high radiation environments on the conduction mechanisms. A medical linear accelerator was used to incrementally irradiate the samples using 12 MeV electrons to a total fluence of $1x10^{13}$ cm^{-2}. Since room temperature annealing of defects in ZnO has been postulated [1-2], current - voltage measurements were performed one day and seven days post irradiation in an attempt to observe this phenomenon. For the highest fluence, $1x10^{13}$ cm^{-2}, the dark and photocurrents were documented at intervals of 3, 12, 26 and 47 days after irradiation. Space charge limited conduction (SCLC) is the dominant current transport mechanism and is attributed to the ZnO layer. I-V plots for the dark current show SCLC in the velocity saturation (ohmic) regime where $J\alpha V$, while plots for photocurrent reveal certain radiation effects on the regime of SCLC observed over a voltage range. Bias of up to 1.0 V resembles the trap-free mobility regime according to the Mott-Gurney law ($J\alpha V^2$) for lower HEEBI fluence. Higher fluence data are closer to the ballistic regime ($J\alpha V^{3/2}$). The 1.0 - 5.5 V bias region shows the mobility regime in the trap-filling transition mode according to the Mark-Helfrich Law ($J\alpha V^{m+1}$). In the bias region 5.5 - 40.0 V, a sub-ohmic I-V behavior is noted where $J\alpha V^{1/2}$. HEEBI fluence of $1x10^{13}$ cm^{-2} minimally increases dark current and decreases photocurrent. These effects are mitigated over time by an apparent room temperature annealing of radiation damage. This too is attributed to the nanocrystalline ZnO layer, thereby demonstrating not only zinc oxide's well-known radiation resistance but also its resiliency to damage incurred. 1. Auret, F.D., et al., *Electrical characterization of 1.8 MeV proton-bombarded ZnO*. Applied Physics Letters, 2001. 79(19): p. 3074-3076. 2. Tuomisto, F., et al., *Introduction and recovery of point defects in electron-irradiated ZnO*. Physical Review B, 2005. 72(8).

10:20 AM Break

10:40 AM
DD7, Late News

11:00 AM
DD8, Late News

11:20 AM
DD9, Late News

11:40 AM
DD10, Late News

Session EE: Epitaxy Materials and Devices

Friday AM
June 25, 2010

Room: 126
Location: University of Notre Dame

Session Chairs: Seth Bank, Univ of Texas, Austin; Archie Holmes, Univ of Virginia

8:20 AM Student

EE1, Overgrowth Investigation of Epitaxial Semimetallic Nanoparticles for Photonic Devices: *Adam Crook*[1]; Hari Nair[1]; Keun Park[1]; Edward Yu[1]; Seth Bank[1]; [1]University of Texas at Austin

Metallic structures with feature sizes small compared to the wavelength of optical radiation have become extremely useful for photonic devices. Surface plasmons have been exploited for various applications including molecular

sensing, light focusing, near-field optical microscopy and enhanced near-field semiconductor absorption. The integration of metallic nanoparticles (e.g. silver, gold, etc.) is currently limited to *ex situ* deposition on the device periphery, as most metal systems cannot be epitaxially integrated into semiconductors. An alternate class of materials, which is compatible with the growth of photonic devices, is required to reach the full potential of nanostructured metallic features. The rare-earth monopnictides are rocksalt semimetals that can be embedded epitaxially into III-V semiconductors. To date, most studies of ErAs nanoparticles have focused on power conversion devices and terahertz emission sources where high optical quality overgrowth in close proximity to the nanoparticles has not been of paramount importance. For monolithic integration with other photonic devices, particularly long-wavelength vertical-cavity surface-emitting lasers (VCSELs), a careful analysis of the overgrowth material must be conducted. GaAs-based tunnel junctions, with ErAs nanoparticles embedded at the p^+/n^+ interface, were grown by solid-source molecular beam epitaxy (MBE) on silicon-doped GaAs (100) substrates. Silicon and beryllium were used as the n-type and p-type dopants, respectively. Surface roughness and local conductivity were measured by atomic force microscopy (AFM) for tunnel junctions of varying p-type capping layer thickness. The RMS surface roughness versus capping layer thickness demonstrated some surface roughening during the initial stages of overgrowth. However, the RMS roughness eventually recovered to ~1 monolayer after sufficiently thick GaAs overgrowth. From the conductive AFM measurements, it was clear that the roughening was not correlated with the location of the ErAs nanoparticles. In addition to surface morphology, the optical quality of the overgrown layers was investigated with photoluminescence (PL). PL structures were grown on semi-insulating GaAs (100) substrates, under conditions nominally identical to those of the tunnel junctions. PL structures with and without ErAs nanoparticles exhibited comparable optical emission from the overgrown $In_{0.1}Ga_{0.9}As$ quantum wells. This demonstrates for the first time that the ErAs nanoparticles can be overgrown with high-quality III-Vs. Epitaxial integration of ErAs nanoparticles compatible with III-V optical devices appears quite promising for incorporation into a number of (nano)photonic devices, including long-wavelength VCSELs where smooth interfaces are critical for the quantum wells, as well as, the distributed Bragg reflector mirrors. In addition. the availability of plasmonic nanomaterials that can be monolithically integrated with III-Vs is exciting for subwavelength photonic devices and circuits for future applications. This work was supported by Dr. Mike Gerhold of ARO and DARPA through a Young Faculty Award.

8:40 AM Student

EE2, Regrown InGaAs Tunnel Junctions for TFETs: *Guangle Zhou*[1]; Haijun Zhu[2]; Paul Pinsukanjana[2]; Yung-Chung Kao[2]; Tom Kosel[1]; Patrick Fay[1]; Mark Wistey[1]; Alan Seabaugh[1]; Huili Xing[1]; [1]University of Notre Dame; [2]IntelliEPI

Interband tunnel field-effect transistors (TFETs) are under development for low-power applications because of their intrinsically low subthreshold swing and low off-state leakage. To maximize lateral tunnel current in planar TFETs, a self-aligned regrown TFET process has been proposed. In this paper, the first regrown vertical InGaAs tunnel junctions are demonstrated using molecular beam epitaxy (MBE) and current-voltage characteristics (I-V) are used to characterize the junctions. CBr_4 and elemental Si were used as the dopant sources in the MBE growth. In the same run two 2 inch n^+ InGaAs wafers were first grown with a Si doping concentration of 1 x 10^{19} cm^{-3}, below its solubility of 6 x 10^{19} cm^{-3}, capped with a 2 nm unintentionally doped (UID) InGaAs layer. After being unloaded from the chambers, one wafer was etched in $1H_2SO_4$-$8H_2O_2$-$160H_2O$ solution for 3 seconds while no pretreatment on the other. This 1:8:160 wet etch was expected to remove 15 nm InGaAs. Both wafers were then co-loaded for regrowth. A 2 nm UID InGaAs layer was first regrown, followed by a 30 nm p^+ InGaAs layer with a C doping concentration of 5 x 10^{19} cm^{-3}, below its solubility of 2 x 10^{20} cm^{-3}. The surface roughness (rms) of the regrown tunnel junctions measured by atomic force microscopy (AFM) is 2.2 nm for the etched wafer and 1.8 nm for the unetched one, respectively, over a scan size of 10 μm x 10 μm. The $In_{0.53}Ga_{0.47}As$ regrown tunnel diodes were fabricated using a self-aligned process to minimize access resistances. A contact resistance of 3.3 x 10^3 •μm^2 was measured. Current-voltage (I-V) characteristics of regrown tunnel junctions on the etched and unetched wafers clearly show negative differential resistance (NDR) under positive bias. On the etched wafer a peak-to-valley ratio of 2.4 and a peak current of 0.14 mA/μm^2 were measured. On the unetched wafer smaller peak-to-valley ratios (1.8) and smaller peak currents (0.074 mA/μm^2) were observed. In addition, we compared the regrown tunnel junctions with an as-grown $In_{0.53}Ga_{0.47}As$ tunnel junction with the same doping profile but a 3 nm UID InGaAs interlayer. With larger peak-to-valley ratio (15), the as-grown tunnel junction, however, shows smaller peak current (0.065 mA/μm^2) than both types of the regrown ones. In conclusion, NDR was observed on the regrown $In_{0.53}Ga_{0.47}As$ tunnel junctions in spite of the defects possibly incorporated at the regrowth interface. Comparison with the as-grown tunnel junctions indicates that the defects at the regrowth interface contribute to the observed higher peak current and lower peak-to-valley ratio in the regrown tunnel junctions. This work is supported by the Nanoelectronics Research Initiative (NRI) through the Midwest Institute for Nanoelectronics Discovery (MIND). The authors are thankful to Dr. Siyuranga Koswatta from IBM for helpful discussions.

9:00 AM Student

EE3, Molecular Beam Epitaxy of Very Thin Fluoride Films on Ge(111) and Its Application to Resonant Tunnelling Diodes: *Keita Takahashi*[1]; Takao Oshita[1]; Kazuo Tsutsui[1]; [1]Tokyo Institute of Technology

The heteroepitaxial structures of fluorides, such as $CaF_2/CdF_2/CaF_2$, grown on Si(111) substrates are promising candidate for producing Si-based resonant tunnelling devices [1][2]. However, strong chemical reaction of CdF_2 with Si substrate is a significant problem in this material system, so that growth temperature is reduced lower than 100ºC and crystalline quality of the epitaxial layers grown at such low temperatures is not good. We propose a Ge buffer layer introduced at the interface between fluorides and Si since Ge is less reactive with CdF_2. As a preliminary study of the idea, we investigated growth of very thin fluoride layers on bulk Ge(111) substrates, and succeeded in fabrication of fluoride resonant tunnelling diodes (RTDs) on the bulk Ge substrates. In experiments, CaF_2, $Ca_{0.42}Sr_{0.58}F_2$ (lattice matched with Ge) or SrF_2 films were grown on heavily doped n-type Ge(111) substrates by using solid source molecular beam epitaxy. The thicknesses of these films were 1.5 nm for AFM and RHEED observations of the grown surfaces and 5 nm for evaluation of *I-V* characteristics on metal-insulator-semiconductor diodes. The two-step growth method in which the fluorides were deposited at room temperature followed by an in situ annealing at 200-500ºC was employed as well as the conventional single step growth at 500ºC. RTDs were fabricated on Ge substrates by using the initial fluoride layer grown under the optimized condition. The various fluoride layers grown by the single step growth method at 500ºC always exhibited island growth. However, island formation was fond to be accommodated relatively for the $Ca_{0.42}Sr_{0.58}F_2$ film. This is probably due to lattice matching effect. Introduction of two-step growth method is strongly effective for improvement of surface condition comparing to the single step method, and annealing at 290ºC provided the best properties in smooth surface and good crystallinity. For the growth of the $Ca_{0.42}Sr_{0.58}F_2$ films grown by the two-step growth method, low leakage current was obtained for the annealing at temperatures lower than 300ºC while leakage current increased at temperatures higher than 350ºC. Therefore, $Ca_{0.42}Sr_{0.58}F_2$ film grown by the two-step growth with annealed at 300ºC was fond to be optimal condition for the initial layer on Ge(111) substrates. RTDs with $Ca_{0.42}Sr_{0.58}F_2$ (3nm) / CdF_2 (3nm) / $Ca_{0.42}Sr_{0.58}F_2$ (3nm) structure were grown at 300ºC on Ge(111), in which the initial $Ca_{0.42}Sr_{0.58}F_2$ layer was grown by the two-step method. The *I-V* characteristics showed obvious negative differential resistance. The successful RTD operation is owing to the good properties of the initial fluoride layer grown on Ge substrates. The successful growth at 300ºC indicates that reduced chemical reactivity of Ge to CdF_2 is effective, and it is significant for high quality growth of fluoride layers for good electrical properties of RTDs.

9:20 AM Student

EE4, Hole Mobility Improvement in Strained InGaSb Quantum Well with Carbon Doping: *Chichih Liao*[1]; K. Y. Cheng[1]; [1]UIUC

The low hole mobility of p-type compound semiconductors prevents the realization of high performance III-V-based field-effect transistor complementary circuits. Recently, it was shown that incorporation of compressive strain in the

channel layer could increase the in-plane two-dimensional hole gas (2DHG) mobility of antimonide-based quantum well (QW) materials [1]. Beryllium (Be) was used as the dopant in previous studies, but Be would easily diffuse out into adjacent layers during the growth process. The channel layer may thus have higher background doping with increased impurity scattering. In this research, we used carbon as the p-type dopant to avoid dopant diffusion. The growth was carried out using gas-source molecular beam epitaxy, and the p-type doping was achieved using a carbon-tetrabromide source via an ultra-high vacuum leak valve. The strained In(x)Ga(1-x)Sb QW structure was metamorphically grown on semi-insulating InP substrates, using Al(x)Ga(1-x)Sb/AlAsSb as the composite barrier layers. High-resolution X-ray diffraction (HRXRD) rocking curve of the as-grown sample showed the AlSb buffer layer was 98% relaxed and the indium composition in the strained In(x)Ga(1-x)Sb QW was 0.3. The corresponding compressive strain in the In(x)Ga(1-x)Sb QW is 1.2%. With optimization of growth conditions and modification of the barrier layer, the room-temperature hole mobility of an In(0.3)Ga(0.7)Sb QW reference structure (without carbon delta-doping) increased from 360 to 600 cm^2/V-s. Compared with pure GaSb QW structure, the hole mobility improvement is about 66% at a similar sheet carrier concentration. Carbon delta-doping was also proved to be effective, which could increase the sheet carrier concentration to 4.1E11/cm^2 with three-second flow of carbon-tetrabromide. The hole mobility decreased to 400 cm^2/V-s with the increasing carrier concentration. The results suggest that the doping concentration of the In(0.3)Ga(0.7)Sb channel can be easily controlled using carbon-tetrabromide as the delta-doping source. References[1] Bennett. B et al. Appl. Phys. Lett. 91, 042104 (2007)

9:40 AM Student

EE5, Growth and Thermal Conductivity of Polycrystalline GaAs Grown on CVD Diamond Using Molecular Beam Epitaxy: *Stephen Clark*[1]; P Ahirwar[1]; F Jaeckel[1]; C Hains[1]; A Albrecht[1]; P Schjetnan[1]; T Rotter[1]; L Dawson[1]; G Balakrishnan[1]; P Hopkins[2]; A Phinney[2]; J Hader[2]; J Moloney[3]; J Moloney; [1]CHTM; [2]Sandia National Laboratories; [3]College of Optical Sciences UA

One of the major challenges for designing heat sinks for very high-power semiconductor devices is the necessity to be in a direct physical contact with the heat source. The best heat conductor is diamond which can be manufactured in single-crystal form and in a polycrystalline form using chemical vapor deposition, with the former form being significantly more complex to realize than the latter. A simple yet extensively used configuration for thermal management in high power III-V devices consists of a diamond heat spreader mounted on a conventional copper heat sink that is subsequently cooled by chilled water or glycol. For optimal heat transfer however, it is desired to have the surface of a single-crystal diamond, polished to sub-nanometer RMS roughness, put into direct contact with the heat source thus spreading the heat from the concentrated region in the III-V to the diamond spreader. Attempts have been made to introduce either a capillary fluid (water or ethanol) or Indium alloy solder to bond the diamond to the heat source. In principle, this approach would work if the surface of the diamond were perfectly flat. However, the rough surface of the polycrystalline diamond prevents efficient wetting for either fluid or solder. Thus the currently used techniques do not fully exploit the heat-spreading capability of diamond and a better approach to bonding the III-V device to diamond is required. In the presentation made we shall discuss the use of poly-GaAs on CVD diamond as a wafer-bonding alternative to Indium solder and capillary bonding. In this paper we present the growth and characterization of polycrystalline GaAs thin-films on polycrystalline Chemical Vapor Deposition (CVD) diamond by Low-Temperature Molecular Beam Epitaxy (LT-MBE). The LT-GaAs adheres very strongly to the CVD diamond layer and can easily be polished down to an RMS surface roughness of 1 to 5 nm. This polished surface represents more than an order of magnitude in surface roughness reduction when compared to a CVD Diamond surface. This makes the polished LT-GaAs on diamond layer an ideal wafer-bonding interface for high-power semiconductor devices. The samples were grown at 0.2 µm/hr with a substrate temperature of 250ºC and a 1:8 III/V beam flux ratio. The samples were analyzed by in-situ reflective high-energy electron diffraction (RHEED) during MBE growth, X-Ray diffraction, and atomic force microscopy for surface roughness. We also measured the thermal conductivity of the GaAs layer on CVD diamond using pump-probe time domain thermoreflectance.

10:00 AM Break

10:20 AM

EE6, Thick HVPE Growth of Patterned Semiconductors for Nonlinear Optics: *Candace Lynch*[1]; David Bliss[1]; Vladimir Tassev[1]; George Bryant[1]; Cal Yapp[2]; [1]AFRL; [2]Solid State Scientific Corp.

There is a growing need within the Department of Defense for compact and efficient sources of coherent radiation operating in the mid-IR and terahertz. One approach involves frequency conversion in quasi-phase-matched (QPM) nonlinear optical materials such as GaAs and GaP. QPM in these materials is achieved by periodically inverting the crystallographic lattice orientation to yield a grating in which the sign of the nonlinear coefficient is modulated. The QPM structure is created using thick epitaxial growth on a patterned template – replication of the template produces a grating with periodic antiphase domains. However, fabrication of these structures presents three challenges – first, the final crystal must be on the order of a millimeter thick (or greater) to accommodate the pump and signal beams as they propagate across the structure. Second, the crystal must be grown with a periodic array of crystallographic inversion domains with widths as small as 15 microns (for conversion from 2 microns to mid-IR) and as large as a millimeter (for conversion to THz). Finally, the defects must be controlled to minimize optical loss mechanisms. Growth of very thick layers on the templates is especially challenging due to the need to maintain vertical propagation of the antiphase domain walls, which are initially aligned along {110} planes. When the domain walls stray from the {110} planes, the patterned structure loses coherency, decreasing the efficiency of the nonlinear interaction. Measurements indicated that the domain wall bending decreased as the growth temperature was reduced. The substrate miscut and the template design also affect the vertical propagation of domain walls. We will describe the use of low-pressure Hydride Vapor Phase Epitaxy (HVPE) to grow crystals of QPM GaAs, achieving GaAs growth rates in excess of 200 microns/hr and producing epitaxial GaAs layers of up to 1.2 mm in thickness. Utilizing templates produced by MBE GaAs/Ge/GaAs epitaxy or by wafer bonding, we have produced mm-thick QPM-GaAs with domain walls that extend through the thickness of the layer. Such materials have successfully been used to generate IR and THz radiation.

10:40 AM Student

EE7, Effects of Carrier Localization on Emission Spectra of Dilute GaAsN Materials Doped with Silicon: *Yan He*[1]; A.M. Mintairov[1]; J.L. Merz[1]; Y. Jin[2]; R.S. Goldman[2]; I. Akimov[3]; T. Goedde[3]; D. Yakovlev[3]; [1]University of Notre Dame; [2]University of Michigan; [3]Technical University of Dortmund

The dilute nitrides (i.e., GaAs containing small amounts of nitrogen) continue to be a topic of great technological interest because of the rapid decrease of the GaAs bandgap with only a few percent of nitrogen. It was shown using high-spatial-resolution photoluminescence (HSR PL) spectroscopy that these materials often contain quantum-dot-like compositional fluctuations arising from nitrogen phase separation effects.[1, 2] Here we study the effect of silicon doping on the formation of such compositional fluctuations in $GaAs_{1-x}N_x$ using conventional HSR and time-resolved PL. For these studies, undoped and Si-doped GaAsN films with free carrier concentrations of 1.4E15 cm-3, 3E16 cm-3, 6.27E16 cm-3 and 5.82E17 cm-3 were grown by rf plasma-assisted molecular beam epitaxy, and subsequently rapid thermal annealed.[3] At T ~ 10K, we observe a strong decrease of emission intensity and a definite red shift of the PL peak position in the Si-doped GaAsN films. We also observe some increase of luminescence intensity with the increase of doping level. In Si-doped GaAsN films, we do not observe sharp emission lines related to quantum dots (QDs) using HSR PL measurements. Time-resolved PL experiments reveal a nearly two times shorter emission decay times in Si-doped GaAsN film. We suppose that most of the observations can be explained assuming local modulation-doping, which leads to activation of deep band-tail states in emission spectra. The nature of these states might correlate with the formation of NN pairs.[4-6] We believe these optical results reveal new structural properties in Si-doped dilute nitride GaAs alloys. This work has been supported under NSF/DMR06-06406. References: [1]A. M. Mintairov, T. H. Kosel, K. Sun, V. Ustinov and J. L. Merz. *MRS Mater. Res. Soc. Symp. Proc. 838E (2005) O3.* [2]A.M. Mintairov, K.Sun, J.L. Merz,

H. Yuen, S. Bank, M. Wistey, J.S. Harris, G. Peake, A. Egorov, V. Ustinov, R. Kudrawiec, and J. Misiewicz. *Semicond. Sci. Technol. 24, 075013 (2009).* [3]Y. Jin, Y. He, H. Cheng, R.M. Jock, T. Dannecker, M. Reason, A.M. Mintairov, C. Kurdak, J.L. Merz, and R.S. Goldman. *Appl. Phys. Lett. 95, 092109 (2009).* [4]D.G. Thomas, J.J. Hopfield, and C.J. Frosch. *Phys. Rev. Lett. 15, 857 (1965).* [5]S. Fahy, A. Lindsay, H. Ouerdane, and E. P. O'Reilly. *Phys. Rev. B 74, 035203 (2006).* [6]L. Bellaiche and A. Zunger. *Phys. Rev. B 57, 4425 (1998).*

11:00 AM Student

EE8, Fabrication and Characterization of Free-Standing InGaAs/GaAs Quantum Dot Microbelt-like Optical Resonators: *Feng Li*[1]; Zetian Mi[1]; [1]McGill University

Recently, semiconductor tubes, formed when a coherently strained semiconductor heterostructure is selectively released from the host substrate, have emerged as a promising technique to realize a new class of nanophotonic devices. They offer many distinct characteristics for laser operation, including ultrahigh Q-factors, directional emission, and well-defined polarization. To achieve an exact tailoring of the 3-dimensionally confined optical modes, we have investigated the fabrication and emission characteristics of optical microcavities formed by such semiconductor tubes using a belt-like geometry at the inner surface, wherein self-organized InGaAs/GaAs quantum dots are incorporated as the gain media. We have measured sharp, polarized optical resonance modes in such microbelt-like tube resonators, with emission wavelengths in the range of 1.1 – 1.3 μm and Q-factors varying from 1,000 to ~ 3,000. The InGaAs/GaAs quantum dot heterostructure was grown on a 50nm AlAs sacrificial layer on GaAs substrate. Semiconductor tubes were formed when the AlAs layer was selectively etched, due to the relaxation of strain. To achieve free-standing tube structures, a U-shaped mesa, with a deeply etched region between its two side pieces, was first defined. Subsequently, a ridge waveguide was introduced by performing a very shallow (~ 5 nm) etch on the mesa. The widths and lengths of the waveguide vary from 1 – 5 μm and from 15 – 30 μm, respectively. The formation of the semiconductor tube creates a belt-like geometry at the tube inner surface, thereby leading to the unique microbelt-like optical resonator with the confined optical modes precisely controlled by the belt width, height, and length. In this experiment, the tube diameter is ~5 μm and the wall thicknesses vary from 50 to 250 nm. Optical properties of the InGaAs/GaAs quantum dot microbelt-like optical resonators were studied using micro-photoluminescence spectroscopy. The emission spectrum of a microbelt device consists of several groups of sharp optical resonance modes, with the dominant mode in each group primarily determined by the azimuthal confinement around the tube circumference. Other optical modes within each azimuthal group, however, are directly related to the optical confinement by the belt along the tube axial direction. The optical resonance modes can be exactly tailored by varying the belt width and thickness. With a belt width of ~ 1.5 μm and tube wall thickness of ~ 100 nm, only the fundamental axial mode can be observed, which exhibit a spectral linewidth of ~ 0.7 nm and a Q-factor of ~ 2,000. Emission characteristics of micro-belt tube resonators with various belt widths, tube diameters and wall thicknesses are being investigated. These results, in conjunction with the achievement of microbelt lasers and laser arrays will be presented.

11:20 AM

EE9, MBE Grown InGaAsSbN/GaSb Single Quantum Wells for Mid-Infrared Applications: *Sudhakar Bharatan*[1]; Shanthi Iyer[1]; Jia Li[1]; Thomas Rawdanowicz[2]; [1]North Carolina A&T State University; [2]North Carolina State University

In this paper we will present comprehensive study of growth and characterization of InGaAsSbN quantum well (QW) heterostructures grown on GaSb by solid source molecular beam epitaxy, using valved antimony and arsenic source and RF plasma N source for potential light-emitting devices in the mid-infrared region. A systematic study of correlating the growth conditions and effect of N incorporation on the emission, crystalline, microstructure and vibrational characteristics of the strained single QW structure, using variety of characterization techniques will be presented. 10 K PL emission at 2.28 μm, with a lowest full width at half maxima (FWHM) of 5 meV which shifted to 2.30 μm on in-situ annealing has been observed. Raman spectroscopy studies in InGaAsSb QWs indicate the presence of Sb antisite defects in these layers, as evidenced by the dominant elemental A_{1g} Sb mode. However, in InGaAsSbN QWs Sb antisites are suppressed, with the preferential formation of Sb-N defects, along with the appearance of intense 2nd order GaSb and GaN modes. The high quality of these nitride QW layers were further attested to by the presence of well resolved Pendellosung fringes on high resolution x-ray diffraction (HRXRD) and sharp, abrupt interfaces on the corresponding TEM images. This work is supported by the Army Research Office (Grant No. W911NF-07-1-0577).

11:40 AM

EE10, Late News

Session FF: Si and Ge Nanowires

Friday AM
June 25, 2010

Room: 129
Location: University of Notre Dame

Session Chairs: Diana Huffaker, University of California, Los Angeles; Chen Yang, Purdue University

8:20 AM Student

FF1, The Influence of the Catalyst on Dopant Incorporation during Si and Ge Nanowire Growth: *Justin Connell*[1]; Eric Hemesath[1]; Daniel Perea[2]; Zakaria Al Balushi[3]; Kwon Nam Sohn[1]; Jiaxing Huang[1]; Lincoln Lauhon[1]; [1]Northwestern University; [2]Los Alamos National Laboratory; [3]Pennsylvania State University

Silicon and germanium nanowires (Si and GeNWs) are promising materials for electronic applications due to their high aspect ratio and the ability to incorporate dopant molecules in-situ during growth. Unfortunately, the frequently employed gold catalyst used in vapor-liquid-solid (VLS) growth of Si and GeNWs exhibits a high solubility for dopants such as boron and phosphorous[1] - a property that leads to diffuse interfaces when attempting to grow *p-n* junctions. We have explored the abruptness of dopant homojunctions in VLS grown nanowires using atom probe tomography to correlate fundamental thermodynamic parameters with junction abruptness. Growth from alloy nanoparticles has also been explored as a potential means to rationally control dopant solubility, and hence junction abruptness, during growth. We previously demonstrated that local electrode atom probe (LEAP) tomography can be used to precisely map the three-dimensional positions and chemical identities of the atoms in a nanowire sample with sub-nm spatial resolution[1]. Si and GeNWs were grown using a hot-walled CVD reactor, with silane and germane as the semiconductor precursor sources, and p- and n-type growth was performed using diborane and phosphine, respectively. During growth, the dopant gas flows were removed, and growth was continued in order to fully deplete the catalyst of the retained dopant species. By measuring the decay in dopant concentration along the length of the nanowire using LEAP tomography, we are able to determine the dopant solubilities in Au during growth, as well as the segregation coefficients. Core-shell Au-Cu_2O nanoparticle catalysts have also been synthesized for use as alloy seeds for NW growth. Upon annealing at 450ºC, these particles form an Au-Cu alloy, with the alloy composition determined by the thickness of the Cu_2O shell. GeNW growth with these particles was performed at 320ºC, which is well below the Au-Ge and the Cu-Ge eutectic temperatures, suggesting growth proceeds via the vapor-solid-solid (VSS) mechanism. We anticipate that dopant solubility in a solid catalyst will be markedly lower than that of a liquid catalyst, which may enable the growth of atomically abrupt *p-n* homojunction NWs.

8:40 AM

FF2, Size Effects in Semiconductor Nanowire Synthesis at the Ultimate Limit: *Shadi Dayeh*[1]; Eli Sutter[2]; Peter Sutter[2]; S. T. Picraux[1]; [1]Los Alamos National Laboratory; [2]Brookhaven National Laboratory

Progress in the synthesis of semiconductor nanowires has prompted intensive discussions of the science of their growth and the technological applications they promise. While for many applications, nanowires with bulk-like electronic properties are sufficient, devices with novel functionality, such as single

electron logic, or solar cells utilizing exciton multiplication, ultimately require harnessing the quantum confinement effects that arise in ultrathin nanowires with diameters below 10 nm. At this scale, the processes involved in the widely used vapor liquid solid (VLS) technique for nanowire growth remain poorly understood. Also a minimum size below which the VLS process can no longer be used for nanowire synthesis is anticipated based on thermodynamic considerations. Here we exploit an extreme level of diameter and placement control in the VLS synthesis of germanium nanowires to establish systematic size effects at small diameters and the ultimate nanowire diameters achievable in VLS growth. Our experiments demonstrate a decrease in the nanowire growth rate at lower diameters, and a concomitant increase in the equilibrium Ge concentration of the liquid Au-Ge drop mediating VLS nanowire growth. Both effects are described quantitatively by an analytical model, based on the Gibbs-Thomson effect. Combining experimental data and this model, we establish the minimum nanowire diameter, and its dependence on growth parameters such as temperature and the addition of dopants. Our results provide a rational basis for the synthesis of semiconductor nanowires at the ultimate size limit.

9:00 AM Student

FF3, Growth and Applications of Silicon/Germanium Axial Nanowire Heterostructures: *Cheng-Yen Wen*[1]; Mark Reuter[2]; John Bruley[2]; Jerry Tersoff[2]; Suneel Kodambaka[3]; Eric Stach[1]; Frances Ross[2]; [1]Purdue University; [2]IBM; [3]University of California, Los Angeles

Silicon and germanium heterojunction nanowires are required for device applications that require tailoring of both band-gap and carrier confinement near the interface. For better device performance, interfacial defects due to large lattice mismatch should be avoided. Similarly, abrupt composition changes at the junction interface are also crucial. It has been shown that dislocation-free interfaces between two materials with a large lattice mismatch can be fabricated in nanowire structures, because the coherent lattice strain near the interface is easily relaxed. Similar results have been demonstrated in Si/Ge heterojunction nanowires using the vapor-liquid-solid (VLS) growth method; however, the resulting composition change at the interface junction is not sharp, due to a reservoir effect in the liquid catalyst: the commonly used liquid AuSi eutectic catalyst for the VLS growth method contains 20% Si. When switching the growth precursors from Si to Ge, Si can not be immediately depleted from the liquid catalyst, and, as a result, there is a gradual composition change at the interface. We show that the use of solid catalysts and the vapor-solid-solid (VSS) method can overcome this problem. We chose $AlAu_2$ alloy as the catalyst, because this compound has a higher eutectic temperature with Si or Ge than pure Au (this allows us to operate with the VSS growth with a reasonable growth rate), and it shows strong catalytic activity. Another benefit is that the medium eutectic temperature of $AlAu_2$ with Si allows us to switch the growth mode between VLS and VSS. We first grow nanowires in the VLS mode, in order to have a fast growth rate, and then cool the sample to solidify the catalyst. The heterojunction is grown by modulating the gas precursors in the VSS mode. Nearly atomically abrupt interfaces in Si/Ge nanowire junction structures can be fabricated using this approach. We can not measure the actual solubility of Si or Ge in the catalyst, but, from in-situ TEM measurements of the step flow kinetics at the interface, we find evidence that supports our assumption of low Si solubility in the catalyst. Theoretical predictions show that Si nanowires containing a thin Ge layer have different electronic properties. To further understand the properties of such structures for applications in band-gap engineering, we use the VSS technique to fabricate ultra-thin Ge layers in Si nanowires and study lattice strain near the interface using lattice images and geometrical phase analysis. Here, we first describe the growth of the Si/Ge nanowire heterostructures using in-situ transmission electron microscopy and show the abruptness and interface perfection using analytical microscopy and lattice images. We will discuss practical considerations of applying this growth method and analyze the strain field of the small Ge quantum dot structure in Si nanowires.

9:20 AM Student

FF4, SiGe/Si Selective Etch Structures for Nanowire Release and Assembly: *Sharis Minassian*[1]; Xiahua Zhong[2]; Xiaojun Weng[3]; Theresa Mayer[2]; Joan Redwing[4]; [1]Department of Chemical Engineering; [2]Department of Electrical Engineering; [3]Materials Research Institute; [4]Department of Chemical Engineering, Department of Materials Science and Engineering, Materials Research Institute, The Pennsylvaina State University

Producing monodisperse silicon nanowires (SiNWs) with uniform length has been a critical difficulty in the bottom-up assembly of nanowire devices. SiNWs grown by the vapor-liquid-solid (VLS) method attach firmly to the growth substrate, making it difficult to remove them for single nanowire device assembly. Ultra-sonic agitation is frequently used to break the wires off of the substrate; however, they break at differing lengths, degrading the yield of successful wire integration and device fabrication. To achieve uniform nanowire lengths, we have investigated the use of SiGe/Si axial-heterostructure nanowire and selective etching to remove the SiGe segment and release the SiNW segment. Preferential etching of $Si_{1-x}Ge_x$ alloys over pure Si can be obtained by using hydrogen peroxide solution when x>65%.[1] To attain Ge-rich SiGe nanowire segment at temperatures above 400ºC, which is more compatible with SiNW growth conditions, disilane (1% in H_2) and germane (2% in H_2) gases were chosen as Si and Ge sources. As opposed to silane which results in Si-rich SiGe nanowires at T>400ºC,[2] disilane enabled the growth of SiGe nanowires with a broader composition range of Ge at higher temperatures. The heterostructure nanowires were grown in a hot wall LPCVD reactor at 425ºC and 13Torr. Oxidized silicon wafers coated with 3nm Au thin film were used as substrates. A 5mm long segment of $Si_{1-x}Ge_x$ was initially grown followed by a Si segment approximately 1µm in length.

Both straight and kinked heterostructure nanowires were observed. The SiGe segments were generally tapered (~40-80nm/µm for 5 nanowires measured), but the tapering was negligible for Si segments with diameters of 51±15nm. TEM analysis showed that in a straight wire both segments were grown along [211] direction. In a kinked nanowire, the SiGe segment grew in the [111] direction, but the growth direction changed to [110] in the Si segment. The composition of the SiGe from XEDS analysis was estimated to be (85.1±0.8)at% Ge, which is in the range of interest for the selective etching process. The etching effect of H_2O_2 (30% solution for 30 minutes) was explored on SiGe and Si nanowires grown separately at similar conditions to that of heterostructure nanowires, and it was confirmed that the solution rapidly etches the SiGe nanowires but does not affect the SiNWs. The process was performed on SiGe-Si heterostructure nanowires; the as-grown SiGe segment was etched away from the substrate releasing the SiNWs off of it. The length of the released wires was measured to be 980±178nm, which is in agreement with our expectation. The impact of selective etching on the alignment yield of nanowires will also be discussed. [1] M. Stoffel et al., Semicond. Sci. Technol., 23, 085021, (2008). [2] K.K. Lew et al., J. Mater. Res., 21, 2876, (2006).

9:40 AM

FF5, Diffusion Formation of Nickel Silicides Contacts in Silicon Nanowires: Yuval Yaish[1]; *Michael Beregovsky*[1]; Alexander Katsman[2]; [1]Electrical Engineering, Technion; [2]Materials Engineering, Technion

Silicon nanowires (SiNWs) field effect transistors (FETs) with a surrounding gate may enable further scaling of CMOS devices due to their thin body and cylindrical geometry. Of fundamental importance is the method in which contacts to the nanowire channel are being formed. One promising method utilizes thermally activated axial intrusion of nickel silicides into the SiNW from pre-patterned Ni reservoirs located at both ends of the wires. Such intrusion of Ni-silicide involves different thermally activated processes such as volume, surface and interface diffusion of Ni, each being characterized by a certain time, temperature and SiNW diameter dependencies. Up to date a comprehensive understanding of these processes is still missing. In the present work these dependencies were investigated during axial growth of nickel silicide in SiNWs for a temperature range of 300-440°C and wire diameters of 30-60nm. Nickel electrodes were deposited on randomly dispersed SiNWs followed by rapid thermal annealing processes at different temperatures and for different times. Silicide intrusions were investigated by atomic force microscopy and scanning

electron microscopy. The following results were analyzed in the framework of diffusion phase formation model that we have published recently. The main part of the intrusion consists of monosilicide NiSi, as was confirmed by measuring the electrical resistance of the wire after full silicidation. Nickel silicide intrusion length, L, showed a typical diffusion dependence on the annealing time, t, and temperature, T: $L = kt^{1/2}\exp(-Q/2k_BT)$, where Q is the diffusion activation energy, and k is proportionality coefficient depending on the wire diameter. We have studied the dependence of k on the wire diameter, and the activation energy for the growth was found to be ~1.7 eV which is typical for nickel interface diffusion processes in nickel silicides. It was concluded that the growth of nickel silicide intrusion is controlled by surface diffusion of nickel along the outer surface of the silicide formed and not by nickel diffusion through the silicide bulk.

10:00 AM Break

10:20 AM Student

FF6, Comparative Study of Ni-Silicide and Germanide Formation in Contacts to Si and Ge Nanowires: *Nicholas Dellas*[1]; Sharis Minassian[1]; Joan Redwing[1]; Suzanne Mohney[1]; [1]Pennsylvania State University

Previous studies have shown that Ni-silicide phase formation in Ni contacts to SiNWs can differ from the phase formation sequence observed for thin Ni films on Si wafers. In the well-studied case of a thin film on a Si wafer, one often observes sequential phase formation beginning with orthorhombic Ni_2Si, followed by NiSi upon increased time and temperature, and finally nucleation of $NiSi_2$ at temperatures in excess of 700°C. This sequential formation is not what has been observed in previous reports of Ni-silicidation of SiNWs. We have found that the phase formed is dependent on the growth direction of the SiNW. In the case of SiNWs with a [112] growth direction, a metastable high-temperature phase, hexagonal θ-Ni_2Si, is formed and stabilized when annealed from 350 to 700°C for 2 min. We also observe that the Ni-silicide has an epitaxial orientation with respect to the SiNW of θ-$Ni_2Si[001]||[11\text{-}1]$ and θ-$Ni_2Si(100)||Si(112)$. The second case is that of SiNWs with a [111] growth direction. We find $NiSi_2$ is the first phase to form after anneals of 350, 400, 450 and 550°C for 2 min, and it also forms with an epitaxial relationship to the SiNW: $NiSi_2[1\text{-}10]||Si[1\text{-}10]$ and $NiSi2(111)||Si(111)$. After anneals of 600 and 700°C for 2 min, a conversion from $NiSi_2$ to NiSi is observed.We have performed similar experiments, substituting GeNWs for the SiNWs and studying the solid state reaction between a Ni film and a GeNW to form Ni-germanides. We find that the reaction begins axially down the GeNW at a temperature of 350°C, and the phase that forms has a similar crystal structure to the hexagonal θ-Ni_2Si phase identified to form in the reaction of Ni with SiNWs with a [112] growth direction. From indexing the diffraction patterns, the Ni-germanide phase could be either Ni_2Ge or Ni_3Ge_2; however, these two phases cannot easily be differentiated because the space groups for the two crystal structures are identical, the only difference being the occupancy of sites by Ni or Ge atoms resulting in different stoichiometries. After annealing at 400°C for 2 min, the same hexagonal Ni-germanide phase is identified, with the exception that in some cases a thin layer (10 nm) of orthorhombic NiGe is formed at the reaction front between the hexagonal Ni-germanide and GeNW. Higher temperature annealing at 500°C results in a break in the GeNW away from the germanide/Ge interface. Further work is underway to determine if Ni-germanide formation in GeNWs has a dependence on the growth direction of the GeNWs, as was previously observed for the Ni/SiNW system.

10:40 AM Student

FF7, High Responsivity Vertical Si Nanowire Photodetector Arrays: *Yi Jing*[1]; Cesare Soci[1]; Ke Sun[1]; Matt Chandrangsu[1]; Atsushi Ohoka[1]; Deli Wang[1]; [1]University of California, San Diego

Semiconductor nanowire photodetectors have attracted extensive interest for applications in sensing, imaging and optical interconnects. It has been demonstrated that nanowire photodetectors have high photoconductive gain ($>10^8$) attributing to the deep level surface trap states and reduced dimensionality. While planar nanowire photodetector arrays exhibit significantly higher sensitivity than their bulk counterparts, vertically aligned nanowire arrays can further enhance the light absorption due to the waveguiding effect caused by the refractive index difference between vertical nanowires and surrounding materials, which increases effective coupling efficiency. In this study, a vertical Si nanowire photodetector array with individually addressability was investigated and its optical characteristics were characterized. P-type (100) silicon-on-insulator (SOI) wafers with device layer thickness of 5μm and doping of ~10^{15} cm^{-3} were used in this research. E-beam lithography and a combination of Inductively Coupled Plasma (ICP) and Reactive Ion Etch (RIE) process were carried out to anisotropically etch an 8×8 vertical Si nanowire array with 4μm pitch size. The vertical photodetector devices were created by embedding the nanowires in spin-on glass and depositing the electrodes. Using crossbar structure, the photodetector array can be individually addressed. The photoresponse of each individual device were measured under uniform white light illumination to demonstrate the feasibility of this array as image sensor. The results show 100% yield functional devices and the photodetectors exhibit a high photo responsivity of greater than 550A/W at room temperature. The high responsivity mainly arises from two factors: (1) the enhancement of the carrier lifetime caused by the trapping of carriers in the surface states; (2) decrease of the carrier transit time due to small dimension of nanowire devices. Thus, a small pixel size Si nanowre image senor with high responsivity was demonstrated. The pixel size can be further scaled down by decreasing the nanowire spacing and this result can be expanded to large scale, high resolution image sensor device by nanoimprint lithography.

11:00 AM

FF8, Si Nanowire Mats for Large-Area Electronics: *William Wong*[1]; Sourobh Raychaudhuri[1]; Sanjiv Sambandan[1]; Rene Lujan[1]; Robert Street[1]; [1]Palo Alto Research Center

Silicon nanowires (Si NWs) have the potential to enhance conventional thin-film transistor (TFT) device structures that will enable high-performance devices in a wide variety of large-area electronics applications. The nanowires also provide greater options for device integration ranging from direct growth to jet-printed suspensions in a liquid. These aspects can greatly reduce fabrication complexities and increase functionality for novel large-area flexible electronics. One simple approach to device fabrication is the use of Si NW mats that replace the semiconducting thin-film layer in a TFT device. This structure can offer increase device performance compared to conventional disordered thin-film semiconductors while providing increased mechanical flexibility. In order to better understand the boundaries and limits for such devices, we have fabricated and tested Si NW field-effect transistors (FETs) using nanowire mats in place of conventional amorphous silicon films. Bottom- and top-gate FETs were fabricated using a mechanical transfer technique. Silicon nanowires were first grown from a gold seed layer by the vapor-liquid-solid process using chemical-vapor deposition onto silicon substrates. The undoped silicon nanowires were then transferred using a sliding contact method to assemble the nanowires from the growth substrate onto the device wafer. Conventional thin-film processing techniques were then used to fabricate devices with different contact metals and encapsulation materials. Bottom gate p-channel and n-channel FETs were fabricated using Ti/Au and TiW contact metals, respectively. The as-fabricated p-channel (n-channel) devices (having a thermal SiO^2 gate dielectric) showed threshold voltages of -10V (+12V), field-effect mobility of 12cm^2/Vs (15 cm^2/Vs), and on-off ratios of 10^4. Top-gate FETs, having plasma-enhanced chemical-vapor deposited SiO_2 gate dielectric layers, were used to create "wrap-around" NW-FETs. These devices were found to have improved on-off ratios of 10^5 and higher field-effect mobility (~ 100 cm^2/Vs) compared to the bottom gate devices. The NW mats were also used to fabricate a 180×160 pixel FET backplane array. Each pixel was 300 microns square with a 300 micron pitch and the resulting fabricated array showed high yield when scanned and measured by capacitive-charge mapping. We will also discuss the effect of different passivation layers on device performance and stability and how these characteristics are implemented in the fabrication of the backplane array for a reflective display.

11:20 AM
FF9, Jet-Printed and Dielectrophoretically Aligned Nanowires for Large Area Electronics: *Sourobh Raychaudhuri*[1]; William Wong[1]; Sanjiv Sambandan[1]; Rene Lujan[1]; Robert Street[1]; [1]Palo Alto Research Center

The ability to integrate Si nanowires (Si NW) on plastic substrates may greatly enhance the performance of low cost flexible electronics. Si nanowire properties can be controlled during growth and leveraged to produce nanowires which are tailored for specific applications. Being able to then harvest these wires and distribute them across a large area substrate in a controlled manner opens up many opportunities for high performance large area and flexible electronics. In this talk we report on Si NW field effect transistors (FETs) fabricated using ink-jet printing as a means to distribute Si NW mats at specified locations across a donor substrate. The Si nanowires were first grown on a Si substrate. The growths were carried out in a chemical vapor deposition system using the vapor-liquid-solid growth process with either Au nanoparticles or an Au thin film to seed the growths. The nanowires were removed from the growth substrate and suspended in water. The nanowire suspension was then loaded into a commercially available ink jet printer and printed onto device substrates. As a means to control the position and orientation of the printed nanowires, an AC electric field was applied across predefined electrodes on the device substrate. This approach to assembling printed nanowires resulted in well-aligned nanowires along the channel region of the FET having channel lengths between 3 to 13 microns and channel widths of 2 to 8 microns. The printed nanowires were then processed into top-gate and bottom-gate transistors using conventional lithographic techniques. The p-type devices showed threshold voltages of around -5 volts, hole mobilities greater than 10 cm^2/V/s and on-off ratios greater than 10^5. We will also discuss several aspects of printing necessary for good device yields and the effect of varying AC electric fields on the printing and assembly process. Finally we will discuss how to make use of these techniques in a scalable way and demonstrate how they can be used to fabricate a TFT backplane that is sufficient to drive reflective display media.

11:40 AM
FF10, Late News

Session GG: Thermoelectrics and Thermionics

Friday AM
June 25, 2010

Room: 131
Location: University of Notre Dame

Session Chairs: Joshua Zide, Univ of Delaware; Peter Moran, Michigan Technological Univ

8:20 AM Student
GG1, Bulk-like Thermionic Energy Conversion Device Fabricated from Laminated Nanostructured Metal/Semiconductor Superlattices: *Jeremy Schroeder*[1]; David Ewoldt[1]; Polina Burmistrova[1]; Robert Wortman[1]; Timothy Sands[1]; [1]Purdue University

Thermionic carrier transport in metal/semiconductor superlattices is a promising energy conversion approach based on nanocomposite materials. Current research focuses on thin-film sputter deposited transition metal nitride superlattices for improving ZT via energy barrier filtering (increased power factor) and interface scattering of phonons (suppressed thermal conductivity). However, even if these superlattices prove successful in enhancing ZT, barriers exist between research-based thin-film superlattices and practical bulk-like device structures. For example, optimal power density in thin-film thermoelectric devices requires superlattice leg lengths in the range of 50-200µm. Such leg lengths are impractical for sputtered deposited films due to lengthy deposition times, high residual growth stress, and varying crystal quality. One approach to realizing long leg lengths is through laminating multiple thin-film superlattices to create bulk-like structures. Effective laminate structures require negligible parasitics be introduced by the bonding layers. Simple analysis shows that the electrical and thermal parasitics are less than 10% when using a bonding medium of high thermal and electrical conductivity, such as copper or gold, and assuming a low contact resistance (~$1\times10^{-8}\Omega$-cm^2) between the bonding medium and superlattice. The metal/semiconductor superlattice structure offers the benefit of a metal-metal contact between the bonding medium and metal nitride, which should offer low contact resistance. Five micrometer ($Hf_{0.5}$, $Zr_{0.5}$)N/ScN superlattices with 12nm period were deposited on 2" 100-silicon substrates by reactive DC magnetron sputtering. One micrometer of gold was deposited on the superlattices followed by Au-Au thermocompression bonding of two 2" superlattices, thereby creating a bilayer structure. The structure was diced into 5mm x 5mm pieces followed by selective etching of the silicon substrates in tetramethyl ammonium hydroxide (TMAH) with the HfN buffer layer acting as an effective TMAH etch stop. The resulting 12µm superlattice bilayer foils were stress balanced with respect to the Au-Au bond interface and they were robust enough to be handled with vacuum tweezers. One micrometer of gold was then deposited on both sides of the superlattice bilayer foils followed by stacking and Au-Au thermocompression bonding of twenty bilayer foils (although the number of stacked bilayers is practically unlimited). The final 290µm thick laminate structure was an artificial bulk-like structure fabricated from 200µm of nanostructured superlattice films and 90µm of gold bonding medium. The 5mm x 5mm laminate was subsequently diced and polished into 300µm x 300µm x 290µm devices for electrical and thermal characterization. These laminate devices demonstrate a route forward towards realizing practical thermoelectric devices based on nitride metal/semiconductor superlattices.

8:40 AM Student
GG2, Epitaxial Growth of Transition Metal Nitrides on MgO via DC Magnetron Sputtering: *Robert Wortman*[1]; Jeremy Schroeder[1]; Polina Burmistrova[1]; Laura Cassels[2]; Joshua Zide[2]; Timothy Sands[1]; [1]Purdue University; [2]University of Delaware

The transition metal nitrides are an important group of materials due to their high melting temperature and hardness. These qualities make them ideal for wear and cutting surfaces. Furthermore, the group IIIa-nitrides have recently gained interest as semiconductors, specifically scandium nitride and its alloys. Scandium nitride is an indirect gap semiconductor with a bandgap of ~0.9 eV. Scandium nitride has been shown to be of interest in thermoelectric devices[1] as well as in optoelectronic and other device applications[2] in pure and alloyed form. We are reporting on the epitaxial growth of scandium nitride films via DC magnetron sputtering. MgO is the substrate of choice for epitaxial growth of ScN as both adopt the rocksalt crystal structure with comparable lattice parameters (6.4% lattice mismatch), and as an insulator, MgO is ideal for studies of the ScN film properties. Scandium nitride films grown on MgO substrates show resistivity values as high as 10 m -cm for films grown in an Ar/N2 ambient at 50 mTorr and 850°C, as well as rocking curve full width half max values as low as 0.67° for films grown at 20 mTorr and 850°C. The sputtering system is load locked and has a base pressure below 3 x 10^{-7} Torr for all growths. Growth pressure was varied from 5 to 50 mTorr, the temperature from 550°C to 850°C, and the sputtering gun power from 50W to 200W. From these studies, the optimal parameters for growing high resistivity, high mobility ScN are determined. The results of X-ray diffraction, mobility and carrier concentration will be presented. 1 J.M. Gregoire, S.D. Kirby, M.E. Turk, R.B. van Dover, Structural, electronic and optical properties of (Sc,Y)N solid solutions, Thin Solid Films, Volume 517, Issue 5, 1 January 2009, Pages 1607-1609. 2 M. Zebarjadi, Z. Bian, R. Singh, A. Shakouri, R. Wortman, V. Rawat, T. Sands, Thermoelectric Transport in a ZrN/ScN Superlattice, Journal of Electronic Materials, Volume 38, Number 7, Pages 960-963.

9:00 AM Student
GG3, Enhancement of Thermoelectric Efficiency in $Si_{1-x}Ge_x$/Si Heterostructures: *Md Hossain*[1]; Harley Johnson[1]; [1]University of Illinois at Urbana-Champaign

Thermoelectric nanostructured materials, especially quantum heterostructures, have drawn enormous attention recently due to their remarkable promise in energy generation and conversion. However, maximizing the efficiency of thermopower generation involves optimizing several interdependent transport properties including electronic conductivity, Seebeck coefficient, and thermal

conductivities of phonons and electron. Low dimensional and nanostructured materials have recently been demonstrated to exhibit superior thermoelectric properties compared to their bulk counterparts. The effect of physical dimension has been shown to reduce thermal conductivity which enhances thermoelectric efficiency – thermoelectric figure of merit or *ZT* – of the device. Although electronic structure dependent properties can influence thermopower generation at different temperature regimes and length scales, particularly where mean free path of phonons and electrons are comparable to the low dimension of the device, their role on *ZT* remains unknown. In this work, using a combination of first-principles derived electronic structure and a Boltzmann transport formalism it is revealed that alloying in heterostructures can substantially improve thermopower while small length scales lead to degradation in Seebeck coefficient *S*. At room temperature the Seebeck coefficients for pure Si and Ge are computed to be 760 μV/K and 380 μV/K respectively. At the same temperature for a 3.3 nm heterostructure with layer thickness ratio $Si_{0.5}Ge_{0.5}$:Si = 1:1 the maximum Seebeck coefficient is 336 μV/K and for a similar size heterostructure with Ge: Si = 1:1 the maximum Seebeck coefficient is 129 μV/K. The maximum values for $Si_{0.5}Ge_{0.5}$:Si = 1:1 and Ge:Si = 1:1 occur at a chemical potential (carrier density) of 0.0025 Ry ($6x10^{18}$ cm^{-3}) and 0.0058 Ry ($3x10^{19}$ cm^{-3}), respectively. This behavior changes as a function of temperature. Therefore, even though lower physical dimension reduces *S*, a combination of temperature and doping level can be sought to maximize *ZT*. Furthermore, the Lorentz number, which is defined as the ratio of electronic thermal conductivity and electronic conductivity and has a constant value according to the Wiedemann-Franz law for metals, is found to increase by a factor of 2 for lower carrier concentration. Within a reasonable doping range (less than 10^{20} cm^{-3}) no change in Lorentz number is found for the heterostructure, indicating the doping level at which it exhibits metallic transport character. To find an optimized combination of temperature, doping, carrier concentration, and layer thickness ratio for enhanced *ZT* transport, calculations are carried out with several energy dependent relaxation time functions as well as a constant relaxation time approximation. Thus, their relative effects on transport properties are also demonstrated in this work.

9:20 AM

GG4, Isothermal Method for Rapid, Steady-State Measurement of Thermoelectric Materials and Devices: *Patrick Taylor*[1]; Sudhir Trivedi[2]; Witold Palosz[2]; [1]US Army Research Laboratory; [2]Brimrose Corporation

A simple, highly accurate method for characterizing thermoelectric materials, partially assembled devices and full devices is presented. In this work, we introduce non-contact radiative heat as a new, independently controlled heat flow that can be used to force isothermal conditions during thermoelectric measurements. Under isothermal conditions, the steady-state heat flows can be determined with high accuracy because parasitic heat flows (e.g., that along the sensing thermocouples, Thomson heat) become negligible and that enables accurate determination of thermoelectric properties such as thermal conductivity. This method applies to bulk and thin-film materials, and can also be extended to determine device performance metrics including coefficient of performance. To validate the method, samples of (Bi,Sb)2(Se,Te)3 alloy bulk materials were prepared by a vertical Bridgman technique. The samples typically had an area-to-length ratio of 0.405 cm2/cm. The Seebeck coefficient was found to be +178 microvolts/Kelvin, the electrical resistivity was determined to be 0.74 milliohm-cm, and the thermal conductivity was determined to be 14.9 mWatt/cm-K. The thermal conductivity was determined by the comparison method and that was compared to that measured using the new technique.

9:40 AM

GG5, Late News

10:00 AM Break

10:20 AM Student

GG6, Thermomagnetic Transport Properties of $(Ag_xSbTe_{x/2+1})_{15}(GeTe)_{85}$ Thermoelectric Materials: *Yi Chen*[1]; Christopher Jaworski[1]; Xinbing Zhao[2]; Joseph Heremans[1]; [1]Ohio State University; [2]Zhejiang University

Nonstiochiometric $(Ag_xSbTe_{x/2+1})_{15}(GeTe)_{85}$ thermoelectric materials have been prepared by the air quenching method with x varying from 0.4 to 1.2. All samples exhibit good electrical performances and low thermal conductivities, and as a consequence, the ZT maximum reaches 1.5 when x = 0.6. Thermoelectric and thermomagnetic transport properties, including Hall and Nernst effect are measured and analyzed in this material system. We then use the "method of four coefficients" on the resistivity, Seebeck, Hall and Nernst coefficients to reveal the scattering mechanisms in these high carrier density materials, alongside with the electron Fermi energy, density-of-states effective mass, and electron mean free path.

10:40 AM Student

GG7, Thermoelectric Properties of Sn-Rich $Pb_{1-x}Sn_xTe$ Alloys Doped with Indium: *Yibin Gao*[1]; Joseph Heremans[1]; [1]The Ohio State University

It has been reported that PbTe doped with Tl has a significant increase in Seebeck coefficient and thus ZT because Tl induces a resonant impurity level in the valence band of PbTe[1]. Indium as an another Group III impurities has also been reported as a resonant level in PbTe and solid solution with SnTe. Previous studies have been focusing on $Pb_{1-x}Sn_xTe$ doped with indium on Pb-rich side[2], however, little is known about the properties of In dopant on Sn-rich side. Here we present our results on Seebeck coefficient, electrical conductivity, Hall coefficient and transverse Nernst-Ettinghausen coefficient as a function of Sn (x=0.5–1) and In concentrations in the temperature range between 80 K and 480K. Our preliminary results indicate that indium is a resonant level in these alloys and therefore can increase power factor over alkali doped material. Reference: [1] Heremans, J. P. et al. (2008). "Enhancement of Thermoelectric Efficiency in PbTe by Distortion of the Electronic Density of States." Science 321(5888): 554-557.[2] Jovovic, V et al. (2008). "Low temperature thermal, thermoelectric, and thermomagnetic transport in indium rich $Pb_{1-x}Sn_xTe$ alloys." Journal of Applied Physics 103(5): 053710-7.

11:00 AM

GG8, Incorporation of $AgSbTe_2$ to $Pb_{1-x}Sn_xTe$ by Mechanical Alloying of End Compounds: Aaron D. LaLonde[1]; Lakshmi Krishna[1]; Eric D. Hintsala[1]; *P.D. Moran*[1]; [1]Michigan Technological University

The benchmark alloys for highly functional thermoelectric material in the 500-700 K temperature range have been (y)($AgSbTe_2$)-(1-y)($Pb_{1-x}Sn_xTe$) material processed by melt alloying where nanostructures are formed as inclusions during post processing thermal treatment and have been reported to be the likely cause of the large *ZT* values. The reproduction of these structures has proven difficult by the lack of comparable results being reported in the literature. This alloy system, though promising as a highly functional thermoelectric material, will require the development of processing techniques more amenable to reproducing these non-equilibrium compositional inhomogeneities if the system's potential is to be realized. This work investigates a different approach to obtain the reported alloy structure containing areas of compositional variation reported to be responsible for increased thermoelectric functionality. The approach taken is to produce the end compounds of $Pb_{1-x}Sn_xTe$ (x=0.1, 0.2, 0.3) and $AgSbTe_2$ by mechanical alloying elemental powders followed by mixing and consolidation to form the desired (y)($AgSbTe_2$)-(1-y)($Pb_{1-x}Sn_xTe$) alloy. A 2-step mechanical alloying process was developed to produce $AgSbTe_2$ with a crystallite size of ~28 nm with only trace presence of the Ag_2Te phase present. After the end compounds were mixed and consolidated the resultant electrical conductivity, carrier mobility and carrier concentration were measured and compared to consolidated samples without the $AgSbTe_2$ addition. Analysis of all samples was done by xray diffraction and determined the lattice parameter, composition, phases present, and size and an estimation of the spacing between inclusions of any secondary phases present in the consolidated material. The consolidated material was found to be n-type for the 3 compositions investigated both with and without the inclusion of $AgSbTe_2$. It was observed that the increase in Sn composition as well as the inclusion of $AgSbTe_2$ results in the addition of p-type carriers to the material. There was no xray diffraction evidence that the mixing of the two distinct phases in powder form resulted in a two phase solid with $AgSbTe_2$ inclusions, despite having started with submicron $AgSbTe_2$ particles and having only subjected the solid to ~550 °C during consolidation. This result is consistent with $AgSbTe_2$ and $Pb_{1-x}Sn_xTe$ forming a solid solution over these compositions. The carrier mobility values have been compared to an analysis of the mobility that would result from

carrier scattering by phonons only. The room-temperature mobility observed in these materials is attributed to a contribution of electron scattering from both phonons and small amounts of SnO_2 and elemental Pb and Sn. This work provides a basis for further development for the (y)($AgSbTe_2$)-(1-y)($Pb_{1-x}Sn_xTe$) material system made by mechanical alloying and mixing of the end compounds and provides evidence that material processed by this method has potential to result in highly functional thermoelectric material.

11:20 AM Student

GG9, Electron Transport Properties of Mechanically Alloyed N-Type $Pb_{1-x}Sn_xTe$ Thermoelectric Elements: *Lakshmi Krishna*[1]; Aaron Lalonde[1]; Eric Hintsala[1]; Matthew Swanson[1]; Peter Moran[1]; [1]Michigan Technological University

Commercial thermoelectric (TE) materials for use in power generation must demonstrate a combination of high figure of merit at the operating temperature ($ZT = \sigma S^2/k$, where σ is the electrical conductivity, S is the Seebeck coefficient and k is the thermal conductivity) and must be made by a cost-effective process for large scale production of the material. Traditionally, bulk TE materials are made by melt-alloying the elemental powders of high purity(≥ 99.999 %). Recent demonstration[1] of a mechanical alloying (MA) process to transform elemental powders into solid $Pb_{0.5}Sn_{0.5}Te$ with thermoelectric functionality comparable to bulk melt-alloyed material has spurred interest in the further investigation of this approach to cost-effectively fabricate high performance thermoelectric power generation material. In order to determine the potential of the mechanically alloyed $Pb_{1-x}Sn_xTe$, the degree to which the mobility of the charge carriers is impacted by the impure starting materials and the microstructural features induced by the MA process must be determined. In this work we analyze experimental room temperature carrier concentration and mobility data in conjunction with the temperature dependence of the electronic conductivity measured from 300K to 750K and experimental Seebeck coefficient measurements from 300K to 600K taken from n-type discs of PbSnTe made by consolidating mechanically alloyed 99.9 % pure elemental Pb, Sn, Te powders with x ranging from 10 % to 30 % and compare the experimentally measured temperature dependence of the electronic mobility to that which would be expected for single crystal PbSnTe doped to the same carrier concentration. The transport coefficients that would be expected for single crystal PbSnTe are calculated by using the Boltzmann equation with an energy dependent relaxation time approximation within the framework of Kane model for energy dispersion. The non-parabolic conduction band and light hole valance band at L-point and the parabolic heavy hole valance band at the Σ-point are considered when calculating the transport properties. The major scattering mechanisms taken into account are due to phonons and alloy scattering of carriers. The impact of carrier scattering in all three bands are explicitly taken into account. At room temperature the electronic mobilities of the mechanically alloyed material are less than what would be expected for single crystal material. However, in the temperature regime (500 K to 700 K) for which the thermoelectric material is expected to operate in power generation applications, the difference between the experimentally obtained mobilities from the MA material and the values calculated for perfect single crystal material are within ~10-15 %. The processing-induced degradation of mobility observed at room temperature has little impact on the transport properties of the material in the temperature regime of interest. 1. A.D.Laonde and P.D.Moran, Journal of Electronic Materials, Vol 39, No 1, 8, 2010.

11:40 AM

GG10, Late News

Session HH: Semiconductor Processing, Surfaces and Contacts

Friday AM
June 25, 2010

Room: 138
Location: University of Notre Dame

Session Chairs: Douglas Hall, University of Notre Dame; Suzanne Mohney, Pennsylvania State University; Lisa Porter, Carnegie Mellon University

8:20 AM Student

HH1, Effect of Contact Modification on Charge Transport at Different Length Scales in Poly(3-Hexylthiophene)-Based Bottom-Contact Field-Effect Transistors: *Kumar Singh*[1]; Tomasz Young[1]; Toby Nelson[1]; John Belot[1]; Richard McCullough[1]; Tomasz Kowalewski[1]; Ponnusamy Nachimuthu[2]; Suntharampillai Thevuthasan[2]; Lisa Porter[1]; [1]Carnegie Mellon University; [2]Pacific Northwest National Laboratory

In this study we report the effect of modification of contacts on the field-effect mobility of poly(3-hexylthiophene) (P3HT) in bottom-contact field effect transistors (FETs). The Au contacts are modified by (a) recessing the contacts in the SiO_2 gate oxide surface to get *planar* OFETs and (b) using bis-trifluoromethane-benzenethiol (BTFMBT) molecules that form self-assembled monolayers (SAMs) on the contacts. Atomic force micrographs (AFM) of extremely thin P3HT films show that planarization of the contacts results in remarkable improvement in polymer morphology in the vicinity of the contacts. In the case of contact modification by the SAMs, the work function of the Au contacts increases from 5.0±0.1 eV to 5.6±0.1 eV, as measured using ultraviolet photoelectron spectroscopy. Both conditions cause a decrease in the contact resistance (R_C) in comparison with conventional bottom-contact (*normal*) OFETs. For example, R_C for *planar* OFETs, $R_{C(planar)}$ = 0.4 M , and SAM-modified OFETs, $R_{C(SAM)}$ = 0.18 M , are lower than that for the conventional OFETs, $R_{C(normal)}$ = 0.61 M at a gate voltage V_G = -80 V. Interestingly it is observed that upon contact modification, the charge transport improves only in short channel length OFETs (L ~ 3-10 μm), whereas the field-effect mobilities (μ) are less effected for OFETs with longer channel lengths (e.g., at L = 3 μm and V_D = -80 V, μ_{planar} = 0.25 $cm^2V^{-1}s^{-1}$, μ_{SAM} = 0.26 $cm^2V^{-1}s^{-1}$, and μ_{normal} = 0.15 $cm^2V^{-1}s^{-1}$; at L = 20 μm, μ_{planar} ~ μ_{SAM} ~ μ_{normal} ~ 0.06 $cm^2V^{-1}s^{-1}$). Wide area AFM scans of OFETs of channel lengths, L = 10 μm and 30 μm show that the P3HT nanofibrils extend across short channels but not across long channels. The effects on contact resistance and mobility can be explained based on a difference in charge transport for short- and long-channel devices due to the nanofibril morphologies.

8:40 AM Student

HH2, Low Pressure Chemical Vapor Deposition of Conformal Boron Thin Films on Deep RIE-Etched Si Substrates: *Nicholas LiCausi*[1]; Justin Clinton[1]; Yaron Danon[1]; James Lu[1]; Ishwara Bhat[1]; [1]Rensselaer Polytechnic Institute

Recently there has been significant research in solid-state neutron detectors since these can be used for the detection of nuclear materials necessary for homeland security applications. Many of these detectors work on the principle of converting thermalized fission neutrons into alpha-particles and detecting the ionization produced by the alpha-particles interaction with the p-n junction. This is necessary because the neutron is charge-neutral and cannot be sensed by standard semiconductor p-n junction. The conversion of neutrons to alpha-particles requires a material with high thermal neutron cross-section. Typically boron-10 or lithium-6 fluoride is used. We have selected boron-10 because it has a higher cross-section and therefore can result in higher efficiency. In order to improve detection efficiency, non-planar film geometry must be employed. This is to accommodate a fundamental mismatch in required B-10 thicknesses. To maximize the probability that an incident neutron will interact with a B-10 atom, the layer must be very thick (~45 μm). However, for the generated alpha-

particles to escape, the B-10 layer must be thin (~2-3 µm). Otherwise, the alpha-particles will be reabsorbed by the B-10. This mismatch led us to the use of high aspect-ratio holes with Si p-n junctions. A variety of high aspect-ratio trench/hole geometries of Si p-n junctions have been studied for this work. Trench depths vary from 15–60 µm and widths range from 2–8 µm. Due to the high aspect-ratio of these trenches, Low Pressure Chemical Vapor Deposition (LPCVD) is favorable for boron deposition. Also, the described LPCVD requires equipment/precursors that are existing in many manufacturing facilities, allowing for high-volume, low-cost production. Boron is deposited on deep RIE-etched Si p-n junctions in a low pressure horizontal CVD reactor. Pressures ranging from 250–1000 mtorr under a 1 sccm diborane flow have been studied. It is believed that the B_2H_6 behaves like SiH_4 in Si deposition. Experiments with temperatures from 400–700 °C have been performed. Experiments involved pre-deposition purging and temperature stabilization, then a 30 minute growth period and subsequent cooling in N_2. Films have been characterized with Scanning Electron Microscope (SEM) imaging. Growth rates as high as 1 µm/hr have been observed. Films thickness ranged from 0.2–1.0 µm. Also, conformal coverage inside the high aspect ratio holes has been studied. As the growth pressure dropped below 300 mtorr the conformal coverage improved. Additional review includes film morphology and strain. High film-stress is observed. Stress often leads to spontaneous cracking/pealing of the film within minutes or after as long as weeks. Stress for a 0.6 µm film is ~850 MPa at 300K. Future work will be discussed. This material is based upon work supported by the US Department of Homeland Security under grant award number 2008-DN-077-ARI008-003.

9:00 AM Student

HH3, Assessment of the Passivation Capabilities of Two Different Covalent Modifications on GaP (100): *David Richards*[1]; Dmitry Zemlyanov[1]; Albena Ivanisevic[1]; [1]Purdue University

The ability to manipulate semiconductor surfaces with organic molecules is attractive due to the potential of making biosensors more compatible and implantable. Silicon has been a heavily researched semiconductor surface for chemical passivation due mainly to its domination of the optoelectronic industry. Recently, the advancement of semiconductor technology has allowed other semiconductors to become attractive platforms for biosensors. Gallium phosphide is a III-V semiconductor material that is commonly used in high temperature and light-emitting devices. The potential for surface atoms to leach into the surrounding media causes problems for biocompatibility. Organic molecules are capable of tying up the loose bonds on the surface and thus preventing leaching and the formation of dissolvable oxide layers. This study compares the ability of two similar organic molecules to form covalent bonds with the GaP (100) surface. Undecenoic acid (UDA) is a terminal alkene that can potentially form Ga-C bonds and mercaptoundecanoic acid (MUA) is a thiol that can be used to generate Ga-S bonds. The conditions required for alkene grafting are less hazardous (no high temperatures or high vacuum) and less time-consuming due to the alkene's ability to form covalent bonds with the surface by way of a radical initiation step caused by irradiation with UV light. The chemical passivation capabilities of each molecule were assessed by exposing the functionalized surfaces to different media including water, various pH solutions, and various concentrations of H2O2 in saline. The surfaces were investigated by contact angle measurements, atomic force microscopy (AFM), and X-ray photoelectron spectroscopy (XPS). Toxicity levels, which are important for sensing applications, were evaluated by inductively coupled plasma – mass spectrometry (ICP-MS) on the media in which surfaces were stored in order to identify any gallium leaching from the substrates. Both molecules formed fairly disordered monolayers demonstrated by comparable oxide thicknesses. The UDA molecules demonstrated better stability compared to MUA based on water contact angle measurements. Data extracted from XPS results indicated a tilt angle of roughly 55° for UDA and 84° for MUA. In terms of coverage, UDA formed 1 – 1.5 monolayers while MUA formed less than half of a monolayer. With respect to toxicity, the UDA-functionalized GaP provided better passivation which was confirmed by less gallium leaching into water and saline solutions. Overall, the superior passivation provided by UDA demonstrates that alkene grafting has better potential for modifying GaP based devices such as implantable sensors.

9:20 AM Student

HH4, Comparison of Ga-Polar and N-Polar GaN by KOH Photoelectrochemical Etching: *Younghun Jung*[1]; Fan Ren[2]; Soohwan Jang[3]; Jihyun Kim[1]; [1]Korea University; [2]University of Florida; [3]Dankook University

III-nitride materials have made huge progress in optical devices, such as light emitting diode (LEDs), and laser diode(LDs). Wet chemical etch has been widely used in fabrication process and analysis. We studied KOH-based wet etch to optimize the process conditions and device performances. Specially, optical and structural the GaN according to the progress of wet-etch is very important. However, the comparison between N-face and Ga-face has been rarely investigated. We report the differences of the etching mechanism on each face. We studied the effects of KOH solution at each face (Ga-,N-) of GaN. To find the etching rates of each face, both faces were PEC-etched for the same time. We used various concentrations (1M, 2M, and 4M) at 50°C KOH solutions under UV illumination. The surface morphology and optical properties of G- and N- face were characterized by atomic force microscope, scanning electron microscope (SEM) and reflectivity measurements. SEM images showed the differences in surface morphologies of each face depending on the concentrations of KOH solutions. The hexagonal pyramid on the surface confirmed that c-plane growth. The summary of root mean square (RMS) data at various etching conditions shows changing of surface mophology. When the molar concentrations of KOH solution are increased in 10min etching process, the Ga-face became more flat. In contract the N-face became rough, which was in consistent with the reflectance data. The surface morphology and the optical properties had changed with the extended KOH etching. When the concentration of solution was increased, the surface roughness of the Ga-face also was increased. Detail about the mechanism of PEC etching and the results will be discussed.

9:40 AM

HH5, N-Type Electrodes for GaN-Based Vertical Light Emitting Diodes: Joon-woo Jeon[1]; Seong-Han Park[1]; Jihyung Moon[2]; June-O Song[2]; Gon Namgoong[3]; *Tae-Yeon Seong*[1]; [1]Korea University; [2]LG innotek; [3]Old Dominion University

High-power GaN-based vertical light-emitting diodes (VLEDs) are of considerable importance for their applications in solid state lighting. Formation of high-quality ohmic contacts having low-resistance and excellent reliability is essential for the fabrication of high-performance GaN-based VLEDs. For top-emission LEDs, n-ohmic contacts are easily formed on Ga-polar n-GaN using either Ti- or vanadium (V)-based schemes. However, for n-type side-up VLEDs (where the n-GaN has N-polarity), n-type ohmic contacts were shown to be difficult to achieve. For example, when Ti/Al contacts to hydride vapour phase epitaxy-grown n-GaN were annealed above 500ºC, Ga-polar n-contact showed ohmic behaviours with a contact resistivity of ~$10^{-5}\Omega cm^2$, but N-polar n-contacts exhibited non-ohmic behaviours. It was also shown that the electrical characteristics of Ti/Al contacts to N-polar n-GaN thin films prepared by a laser lift-off (LLO) process were significantly degraded upon annealing at temperatures in excess of 300 ºC. The better characteristic was attributed to the generation of polarization-induced two-dimensional electron gas caused by the formation of interfacial AlN on p-GaN. It was, however, shown that the use of 5 nm-thick Pd interlayers produced was very effective in improving the electrical properties of Ti/Ai-based contacts upon annealing at temperatures in excess of 450ºC as compared to Ti/Al contacts to LLO-prepared N-polar n-GaN. The better electrical behaviours were attributed to the formation of stable AlN at the interface. The different argument is indicative of the complicated role by which the interfacial AlN layer plays during an annealing process. In this work, in order to obviate any effects associated with the interfacial AlN, we have investigated the electrical properties of Al-free V-based contacts to different polar n-GaN. Our Ga-polar and N-polar n-GaN samples have been prepared by MOCVD, molecular beam epitaxy (MBE) and an LLO process. It is shown that regardless of the crystal polarities, all the samples exhibit similar electrical characteristics. The as-deposited samples are ohmic, but become non-ohmic when annealed at 300 - 500ºC. The samples are ohmic again at 700ºC. Based on the x-ray photoemission spectroscopy and Auger electron spectroscopy results,

the ohmic and degradation behaviours are explained in terms of the formation of donor-like surface defects and Ga vacancies, which are generated by dry etching, the outdiffusion of Ga, and the formation of nitide phases.

10:00 AM Break

10:20 AM Student

HH6, In-situ Ohmic Contacts to p-InGaAs: *Ashish Baraskar*[1]; Vibhor Jain[1]; Mark Wistey[2]; Evan Lobisser[1]; Brian Thibeault[1]; Yong Ju Lee[3]; Arthur Gossard[1]; Mark Rodwell[1]; [1]University of California, Santa Barbara; [2]University of Notre Dame; [3]Intel Corporation

Very low resistance metal-semiconductor contacts are crucial for the performance of transistors in THz bandwidths. The base and emitter contact resistivities (ρ_c) in heterojunction bipolar transistors (HBTs) must decrease in proportion to the inverse square of the transistor cutoff frequency. A ρ_c of less than $1x10^{-8}$ -cm^2 is required for III-V HBTs and FETs for having simultaneous 1.5 THz f_t and f_{max}. Ohmic contacts to p-type $In_{0.53}Ga_{0.47}As$ have been studied extensively because of its application as the base contacts in InP based HBTs. Pd has shown ρ_c = 6.3 x 10^{-8} -cm^2 to p-InGaAs, but penetrates into the semiconductor by combined chemical reaction and diffusion. Low resistivity, thermally stable contacts having < 5 nm metal penetration depth are required for HBTs having < 20 nm thick base layers. Here we report $\rho_c = (2.0 \pm 0.8)\times10^{-8}$ -cm^2 for in-situ Mo contacts to p-type $In_{0.53}Ga_{0.47}As$. The semiconductor epilayers were grown by solid source MBE. A 100 nm undoped $In_{0.52}Al_{0.48}As$ layer was grown on a semi-insulating InP (100) substrate, followed by 100 nm of carbon doped $In_{0.53}Ga_{0.47}As$. 20 nm of Mo was deposited in an electron beam evaporator attached to the MBE chamber under ultra high vacuum. Mo was deposited on half of the surface of the samples using a shadow mask. Hall measurements were done on the samples not coated with Mo. Samples coated with Mo were processed into transmission line model (TLM) structures for contact resistance measurement. Ti (20 nm)/Au (500 nm)/Ni (50 nm) contact pads were patterned on the samples using photolithography and lift-off after an e-beam deposition. Mo was then dry etched in an SF_6/Ar plasma using Ni as a mask. Resistances were measured by four-point (Kelvin) probing. The processed samples were annealed under nitrogen atmosphere at 250°C for 120 minutes, replicating the thermal cycle experienced by a base contact during transistor fabrication. The ρ_c achieved for the un-annealed samples was $(2.0 \pm 0.8)\times10^{-8}$ -cm^2, which is the lowest reported to date for Ohmic contacts to p-type InGaAs. As determined through Hall measurements, the active carrier concentration, mobility and sheet resistance was 1.1 × 10^{20} cm^{-3}, 39.6 cm^2/Vs and 150 /□, respectively. The annealed samples show a ρ_c of $(2.5 \pm 0.9)\times10^{-8}$ -cm^2. TEM images of the annealed samples show a uniform and abrupt Mo-InGaAs interface, indicating minimal intermixing of the metal semiconductor layers. We speculate that the increase in ρ_c upon annealing may be due to the presence of an interfacial carbon layer which degrades upon annealing. Although ρ_c increases to $(2.5 \pm 0.9)\times10^{-8}$ -cm^2 upon annealing, in-situ Mo remains a strong candidate for base Ohmic contacts in THz HBTs.

10:40 AM Student

HH7, Degradation of Ohmic and Schottky Contacts on InGaAs MHEMTs during Bias Stressing: *Erica Douglas*[1]; Ke Hung Chen[1]; Chih Yang Chang[1]; Lii-Cherng Leu[1]; Chien-Fong Lo[1]; Byunghwan Chu[1]; Fan Ren[1]; Stephen Pearton[1]; [1]University of Florida

Numerous studies have shown that InGaAs based metamorphic high electron mobility transistors (MHEMTs) have similar mean time to failure (MTTF) as that of InP based HEMTs, about 106 hours. However, InGaAs MHEMTs require a substantial burn-in process in order to stabilize device performance and eliminate infant mortality. Typically, drain current decreases while Ohmic contact resistance increases during electrical stress and stabilizes within 24-60 hours. In order to study the device reliability and failure mechanisms, both high temperature storage tests and DC stress tests were performed on MHEMTs. InAlAs/InGaAs MHEMTs, obtained from a vendor, were stressed for 36 hours at a drain voltage of 3V. Additional devices underwent a thermal storage test at 250°C for 36 hours. Transmission line method (TLM) structures were also stressed under similar conditions. The InAlAs/InGaAs MHEMTs employed a two finger Ti/Pt-based Schottky gate design with a length of 150 nm, a gate width of with 75 µm, and 1.2 µm spacing between both gate/drain and gate/source. The TLM patterns also present on the device chip employed 45 X 70 µm pads with gaps of 3, 6, 9, 12 and 15 µm. Under both DC and thermal stress conditions, the drain current decreased about 12.5%. Therefore, the devices suffered from an increase in parasitic resistance during stressing. The TLM patterns were stressed in order to examine the effect of the gate on the increase of the parasitic resistance and degradation of drain-source current.The total resistance of the TLM structures increased significantly with time in the first 12 hrs of thermal storage at 250°C, while the specific contact resistivity increases much more than sheet resistance. The gate characteristics of the thermal and DC stressed HEMTs showed significant degradation and gate current increased several orders in both forward and reverse bias conditions. This indicates that the contact between the Ohmic metal and semiconductor dominated the degradation during the thermal storage. Devices stressed under DC suffered from substantial gate sinking, in which the bottom Pt layer of the Pt/Ti/Pt/Au mushroom gate diffused into the InAlAs gate contact layer. The energy-dispersive x-ray spectroscopy (EDS) elemental analysis was used to analyze the Pt diffusion depth the gate region. The high current density, 1 × 10^5 A/cm2, flowing across the thin ohmic metal then across the metal semiconductor interface into the semiconductor the Ohmic metal caused the Ohmic metal to diffuse during the burn-in process. This caused the electromigration-induced voids and the formation of additional metal spikes at the edge of the Ohmic metal contact pads.

11:00 AM Student

HH8, Characterization of Thin InAlP Native Oxide Gate Dielectric Layers for GaAs MOSFET Applications: *Wangqing Yuan*[1]; Douglas Hall[1]; [1]University of Notre Dame

Due to high electron mobility, low gate leakage current and the potential for positive threshold, GaAs-based III-V MOSFETs are of interest for high-speed circuit applications. The quality of gate dielectrics is crucial for III-V MOSFET devices. The thermal grown InAlP oxide (InAlP-ox) is promising in terms of its low processing cost, excellent insulating property, as well as an inward growth mechanism, which provides a cleaner oxide-semiconductor channel interface. In the fabrication of GaAs MOSFET devices utilizing thin InAlP native oxides, the oxidation process must be accurately understood and controlled. In this work, variable angle spectroscopic ellipsometry (VASE) is utilized to both characterize InAlP oxidation kinetics and to accurately determine the final thickness of the oxide. To accurately characterize the oxidation of thin (5 nm) InAlP layers used in a MOSFET structure (to yield an ~8 nm thick native oxide dielectric layer), accurate optical constants of each material and an accurate model describing the oxidation dynamics of InAlP are required. The optical constants of InAlP and InGaP (lattice matched to GaAs) have been determined by a multi-sample VASE analysis (1.45 to 5.45 eV, 300 K) of 100 and 200 nm thick epilayers. The optical constants of InAlP-ox are determined by analysis of a 30 nm InAlP epilayer on GaAs, fully oxidized at 440°C for 85 min. The InAlP-ox optical constants are described by Tauc-Lorentz (TL) oscillator terms, and the optical constants of InAlP and InGaP are described by Hersinger-Johs parameterized semiconductor oscillator functions. Comparisons are made between the optical constants of the fully-oxidized and "over-oxidized" InAlP-ox samples (oxidation times of 128 and 170 min). Upon full oxidation, no significant thickness change of the InAlP-ox layer is observed. However, with increasing oxidation time, the oxide refractive index n~1.6 below its bandgap decreases, and the bandgap increases (from ~3.3 to ~4.5 eV). These results suggest that the oxidation rate of the aluminum component in InAlP is faster than that of the less reactive indium component, and that the indium component continues to oxidize after full oxidation of the aluminum component is reached. Accordingly, a three-layer model (ambient/InAlP-ox/EMA/InAlP/GaAs substrate) is used to test InAlP and InAlP-ox optical constants for a 100 nm InAlP film partially oxidized for 100, 120, 130 and 140 min. The effective medium approximation (EMA) layer describes the incomplete oxidation of the indium component in InAlP-ox, and excellent agreement between thickness values measured by transmission electron microscopy (TEM) imaging and VASE confirms the accuracy of our optical constants. Finally, these models have also been extended to accurately fit the thickness of <10 nm InAlP-ox gate oxides grown directly upon a multi-layer MOSFET heterostructure. The deviation of InAlP-ox thickness results

determined by VASE from those determined by TEM is within 4%.

11:20 AM
HH9, Post-Growth InGaAsP Quantum Well Intermixing for High Saturation Power Semiconductor Optical Amplifiers: *Jonathan Klamkin*[1]; Jason Plant[1]; David Chapman[1]; Douglas Oakley[1]; Antonio Napoleone[1]; Kevin Ray[1]; Paul Juodawlkis[1]; [1]Lincoln Laboratory, Massachusetts Institute of Technology

Quantum well intermixing (QWI) is a technique whereby quantum wells (QWs) can be altered following epitaxial growth. This technique provides a means for controlling the QW bandedge selectively across a semiconductor wafer, allowing for the realization of novel optoelectronic devices and photonic integrated circuits. For the InGaAsP material system, ion-implantation-enhanced interdiffusion is one of the more successful QWI techniques demonstrated. With this technique, ion implantation is used to create vacancies that promote intermixing of atoms at the interfaces of QWs and barriers during a subsequent annealing step. The intermixing reshapes the QWs and effectively increases the bandgap energy. In this work, we have developed a QWI technique specifically tailored for the bandedge shift required to realize a novel multi-section semiconductor optical amplifier (SOA) that is based on the slab-coupled optical waveguide (SCOW). The performance of SOAs can be improved with a multi-section device architecture incorporating a pre-amplifier region and a post-amplifier region. We have proposed using QWI to create a novel multi-section SOA whereby the bandedge and in turn gain spectrum can be tailored along the length of the device to improve the inherent tradeoff between gain and output power, and to increase efficiency. The QWI process used for fabricating the multi-section SOAs entails a dielectric masked selective implant of Phosphorous ions, removal of the dielectric mask by wet chemical etching, dielectric encapsulation of the sample to prevent desorption during the subsequent annealing steps, and high temperature annealing. The initial implant and the processing steps should be designed to minimize damage to the underlying QW layers. It is therefore desirable to minimize the ion distribution in the vicinity of the QWs. The implant energy and dose need to be considered, as well as high temperature processing steps prior to the annealing steps that could lead to premature diffusion of vacancies. The annealing for interdiffusion can damage the QWs by forming traps; however the damage is also repaired by the annealing. This damage can be quantified by monitoring photoluminescence (PL) peak intensity. For the multi-section SOA described, it is beneficial to tailor the QWI process based on the amount of bandedge shift desired while subsequently minimizing damage. Here we have optimized a QWI process for desired bandedge shifts for a multi-section SCOW SOA. The device design requires bandedge wavelength shifts in the range of 30-60 nm; therefore it is desirable that the PL intensity, used to quantify recovery of the damage material, be maximized for such shifts. Following experimentation, it was shown that with an implant energy and dose of 80 keV and 3.0e14 cm^{-2}, corresponding to an implant range and straggle of 89 nm and 44 nm, the PL intensity was fully recovered following the QWI process.

11:40 AM
HH10, Late News

Session II: Heteroepitaxy on Silicon

Friday AM
June 25, 2010

Room: 141
Location: University of Notre Dame

Session Chairs: Ralph Dawson, Univ of New Mexico; Ganesh Balakrishnan, Univ of New Mexico

8:20 AM Student
II1, Reduction in Operation Voltage of Light Emitting Diodes Fabricated in Si/III-V-N/Si Heterostructure: *Keisuke Yamane*[1]; Shintaro Yamada[1]; Yuzo Furukawa[1]; Hiroshi Okada[1]; Akihiro Wakahara[1]; [1]Toyohashi University of Technology

Monolithic integration of III-V(-N)-based photonics and Si-based electronics has been attracted for realizing a novel optoelectronic integrated circuits (OEICs)[1]. We have demonstrated monolithic OEIC test chip, in which Si-based MOSFETs and GaPN-based III-V-N light emitting diodes (LEDs) are integrated into a lattice-matched Si/III-V-N/Si heterostructure [2]. In this structure, however, the operation voltage of the LEDs resulted in relatively high due to the Si-capping layer grown on the III-V-N layer. In this work, we investigated the effects of the Si-capping layer on an electrical property and succeeded in the reduction in the operation voltage of the LEDs. Firstly, Si/p^+-GaPN/p-GaPN/n-GaPN (referred to as sample A) and Si/p-GaPN/n-GaPN (referred to as sample B) structure were grown on n-Si substrates by molecular beam epitaxy. Here, the carrier concentrations for p^+-GaPN and p-/n-GaPN were designed to be $5x10^{19}$ cm^{-3} and $5x10^{17}$ cm^{-3}, respectively. After the growth, in order to obtain p-Si-capping layers with carrier concentration of over $1x10^{18}$ cm^{-3}, both samples were annealed at 900°C following boron ion implantation into the Si-capping layers. These processes are based on our original fabrication process of the monolithic OEIC test chip [2]. The Al electrodes with 500 μm in diameter and AuSb broad contacts were used to form Ohmic contacts for the p-Si-capping layers and the n-Si substrates, respectively. Both samples were cleaved into 1x1 mm^2 chip and current-voltage (I-V) curves were measured. The operation voltage to obtain the current density of 1 A/cm^2 is 1.5 V in sample A. This value is almost the same as that of a typical GaPN homojunction (HJ)-LED on a Si substrate without a Si-capping layer. The operation voltage of sample B is 1 eV higher than that of sample A. The valence band offset between GaP and Si has been estimated to be 1.05 eV [3]. Due to this valence band offset, 50-nm-thick depletion layer is formed in the p-GaPN layer at the p-GaPN/p-Si heterointerface in sample B. This depletion layer acts as thick potential barrier for holes injected from the p-Si-capping layer. In the case of p^+-GaPN/p-Si heterointerface in the sample A, the depletion layer thickness is decreased to 5 nm. This thickness would be thin enough for holes to penetrate the potential barrier by the tunnel effect. Therefore, the operation voltage is lowered by adding the p^+-GaPN layer in between the p-GaPN layer and the p-Si-capping layer. [1] I. Hayashi, Jpn. J. Appl. Phys. 32 (1993) L266. [2] H. Yonezu, Y. Furukawa, A. Wakahara, J. Cryst. Growth. 310 (2008) 4757. [3] I. Sakata, H. Kawanami, Appl. Phys. Exp. 1 (2008) 091201.

8:40 AM
II2, GaN/AlN Heterostructures on Vertical {111} Fin Facets of Si (110) Substrates: *Mark Holtz*[1]; Vladimir Kuryatkov[1]; Wen Feng[1]; Mahesh Pandikunta[1]; J. Woo[2]; H. Harris[2]; D. Garcia[3]; Sergey Nikishin[1]; [1]Texas Tech University; [2]Texas A&M University; [3]SVTC

Architectures analogous to silicon fin field effect transistors (FinFETs) are of current interest for achieving high device density. The high mobility and high breakdown field of III-nitride materials, along with a wide range of alloy compositions for band structure engineering, makes devices based on vertically-oriented fins of these materials interesting for a range of applications. Fin architectures provide novel design opportunities such as the formation of non- and semi-polar surfaces, and compatibility with silicon for future integration with conventional electronics. These attributes are promising for multiple electronic device technologies operating at high speeds. In order to explore these possibilities, experiments are first needed to obtain thin (sub-micron) AlN/GaN sidewall growth on Si fin structures with high aspect ratios, and the material properties must be investigated. In this work we explore substrate structuring to produce silicon fins with vertical {111} plane sidewalls. Using these structured substrates we develop selective area epitaxy (SAE) for growing thin (0001) AlN/GaN layers on the vertical sidewalls.We will describe our recent progress using metallorganic vapor phase epitaxy to develop selective sidewall epitaxy of AlN/GaN on vertical fins of silicon. Silicon (110) wafers are structured to form fins with {111} sidewall facets. By adapting a pulsed layer epitaxy method, AlN buffer layers are grown with uniform thickness < 100 nm on vertical {111} surfaces, followed by GaN which grows selectively on the AlN to form the sidewall fin structures. Height is controlled by etching of the Si stripes and GaN width is controlled by growth duration. Raman measurements of the GaN show very narrow line widths, consistent with excellent material quality. Spatial dependence of micro-cathodoluminescence mapping of the GaN band gap emission shows compressive strain in the GaN at the AlN interface relaxes closer to the fin corners.

9:00 AM Student

II3, 2µm Thick Device Quality GaN on Si(111) Using AlGaN Graded Buffer: *Benjamin Leung*[1]; Qian Sun[1]; Christopher Yerino[1]; Yu Zhang[1]; Jung Han[1]; Hongwei Li[2]; Dong Lee[2]; Eric Armour[2]; Ajit Paranjpe[2]; [1]Yale University; [2]Veeco Compound Semiconductor, Inc.

As opposed to the conventional use of sapphire or SiC substrates, silicon enables scaling to large diameter wafers, significant cost reduction, enhanced thermal and electrical properties, and the potential for on-chip integration between GaN and Si electronics. GaN epitaxially grown on Si(111) by MOCVD has been shown not only to be a viable method of obtaining high-quality epitaxial films, but the inherent benefits of using silicon as a substrate provides significant advantages for production of light emitting diodes and high frequency/high power transistors. To overcome the large lattice mismatch (17%) and huge difference in thermal expansion coefficient (54%) in obtaining high-quality crack-free layers, techniques proposed include the use of AlGaN graded buffer layers, superlattices, and AlN interlayers. AlGaN graded buffers have been adopted by many groups as an effective way for strain management and dislocation reduction. However, there has yet to be an in-depth study revealing the stress evolution and dislocation reduction mechanism within the AlGaN graded buffer layer. Here, we present a detailed study of step-graded AlGaN buffers leading to 2µm crack-free GaN with XRD symmetric rocking curve FWHM (0002) 475 arcsec, and skew-symmetric (10-11) 1050 arcsec. The samples were grown on Si(111) in a horizontal metalorganic chemical vapor deposition reactor. Trimethylgallium (TMGa), trimethylaluminium (TMAl), and ammonia (NH3) were used as the precursors for Ga, Al, and N, respectively. A 0.2 µm AlN buffer was deposited at 1150°C, followed by step-graded AlGaN graded layer with various grading profiles and thicknesses ranging from 0.4 µm to 1.2 µm. The samples were monitored by in-situ reflectance and curvature measurements, and analyzed by ex-situ high-resolution x-ray diffraction, TEM, Nomarski and SEM to probe surface morphology, stress evolution and defect reduction mechanisms in the AlGaN graded buffer layers. By the use of AlGaN layers, in-situ reflectance shows instant oscillations indicating a quasi-2D growth mode. Surface morphology was improved by the use of thin AlGaN layers, as correlated to film stresses measured by in-situ deflectance. It is shown that the ramp sequence during high temperature surface treatment for thermal removal of oxide and Al predeposition prior to deposition of HT-AlN buffer are critical for good crystallinity of subsequent layers. Mosaic tilt is characterized by x-ray rocking curve analysis on each of the AlGaN layers, showing defect evolution through the layers. With direct visualization using reciprocal space mapping of the asymmetric (10-15) and (11-24) diffractions, the stress relaxation can be directly observed, enabling the growth of an AlGaN buffer scheme reducing the tensile stress to support a high-quality 2 µm thick crack free GaN layer. The characteristics of LED and HEMT device structures grown on this template will be presented.

9:20 AM Student

II4, Compositionally-Graded Layers Composed of Tandem InGaAs InGaP Alloys and Pure GaAsSb Alloys to Engineer the InP Lattice Constant on GaAs Substrates: *Li Yang*[1]; Mayank Bulsara[1]; Kenneth Lee[1]; Eugene Fitzgerald[1]; [1]Massachusetts Institute of Technology

InP and semiconductor alloys lattice-matched to InP enable various state-of-the-art electronic and optical devices. Our research is motivated by the desire to integrate InP-based devices on Si substrates, specifically by engineering the lattice constant from Si to that of InP. This includes three major challenges: bridging the lattice constant of Si to that of Ge, accommodating the Ge/GaAs nonpolar/polar interface, and engineering the lattice constant from GaAs to that of InP. We focus primarily on the last challenge, establishing the InP lattice constant on (001) GaAs substrates with a 6° miscut. The specification of the 6° miscut is important because it provides step structures which eliminate antiphase disorder during the growth of GaAs on Ge. Two approaches for MOCVD-grown compositionally graded metamorphic buffers, which enable virtual InP lattice constant substrates on GaAs were investigated. The first approach consisted of tandem graded layers of InGaAs and InGaP with compositional grading of the In concentration. This tandem approach is necessary because phase separation in InGaAs alloys at XIn>0.30 leads to rough surface and high threading dislocation density (TDD). We first grew InGaAs graded buffers at 700 °C with targeted In concentration of XIn=0.30 on both on-axis (001) GaAs and (001) GaAs with 6° miscut. The graded InGaAs grown on on-axis (001) GaAs did not exhibit phase separation and gave a TDD of 1.9e6 cm-2 with a surface roughness of 7.5 nm. While InGaAs grown on 6° offcut GaAs exhibited serious phase separation, resulting in high TDD (~ 5e8 cm-2) and rough surface morphology (roughness ~ 26.1 nm). However, that phase separation in the InGaAs on 6° offcut GaAs can be suppressed if we lower the growth temperature from 700°C to 450°C at higher In concentration because of the lower surface diffusivities of In and Ga atoms at lower growth temperature. The suppression of phase separation, in turn, dramatically reduces the TDD to 1.4e6 cm-2 and the surface roughness to 7.5 nm for In0.30Ga0.70As graded buffer. Using the graded InGaP system at a growth temperature of 650°C to continually grade the lattice from In0.30Ga0.70As to InP allowed us to achieve InP on 6° offcut GaAs with a TDD of 7.9e6 cm-2 and a surface roughness of 30.0 nm. The second approach used GaAsSb alloys with compositional grading of the Sb concentration. Graded mixed-anion GaAsSb alloys grown at 575°C did not exhibit phase separation, resulting in high quality InP lattice constant films on GaAs. A GaAsSb alloy (grading rate ~ 1.06% strain/um) lattice-matched to InP on 6° offcut GaAs with TDD of 4.7e6 cm-2 and roughness of 7.4 nm was demonstrated. The TDD of the GaAsSb graded buffer can be further lowered to 2.7e6 cm-2 if a lower grading rate (0.64% strain/µm) is used.

9:40 AM

II5, Characterization of Standard and Ferromagnetic Schottky Barriers on GaP/GaP and GaP/Si Epi-Layers: *Chris Ratcliff*[1]; Tyler Grassman[1]; Andrew Carlin[1]; Mark Brenner[1]; Jonas Beardsley[1]; Jon Pelz[1]; Steven Ringel[1]; [1]Ohio State University

One of the fundamental goals of current spintronics-based research is the efficient and controllable injection of electrons with a particular spin alignment into Si. Although recent success has generated interest in the possibilities of advanced silicon devices[1], much of the physics involved with the spin injection process is not yet fully understood. To this end, gallium phosphide is well suited as it is the closest lattice matched III-V material to silicon (0.37% misfit) and has a large band gap relative to silicon. The GaP/Si system has been the subject of interest for decades due to its potential as a gateway to III-V/Si integration. Recent work on MBE grown GaP/Si has resulted in high quality crystalline thin films[2]. By use of this process, which includes Si homoepitaxy and migration enhanced epitaxy III-V nucleation, GaP films free of defects related to the heterovalent interface can be grown to the precise thicknesses required for spin injection (~1-10nm). Much work remains to be done, however, on the characterization of these thin heteroepitaxial GaP/Si films and the GaP/Si interface. In addition to the fairly uncharacterized GaP/Si system, there is also little known about the nature of metal/GaP Schottky contacts, which are necessary for metal/GaP/Si tunnel-barrier spin-injection. To this end, Au/GaP and Fe/GaP Schottky diodes were fabricated to facilitate the characterization of the resulting metal-semiconductor contacts. Current-voltage data shows similar, strong rectifying behavior for both metals, and internal photoemission (IPE) experiments reveal Schottky barriers for Au and Fe to be 1.15 and 1.14eV, respectively. The negligible difference in resultant barrier heights compared to the 0.6eV difference in work functions between the two metals indicates a Fermi level pinning mechanism for Schottky barrier formation on GaP. Therefore, because Fe, a ferromagnetic metal, makes a good Schottky barrier with GaP, and the fact that the epitaxial GaP can be grown to desired doping levels and thicknesses, the effective tunneling barrier can be tailored to promote efficient spin injection into silicon. In order to fully understand the efficacy of the Fe/GaP/Si system as a spin injection tunnel barrier, we must first characterize all of the materials and interfaces involved. To this end, work will continue on the characterization of metal/GaP Schottky barriers, which in turn enables the materials level characterization of the GaP epitaxial layers through the use of such as advanced techniques as deep level transient and optical spectroscopies. Additionally, we intend to probe and will report the effects of GaP/Si interfacial quality on the barrier heights and other properties of resultant metal/GaP/Si devices. [1]Dash et al., Nature, 462, 491-494 (2009); [2] Grassman et al., Appl. Phys. Lett. 94, 232106 (2009).

10:00 AM Break

10:20 AM

II6, Silicon Nanostructures Ion Implanted with Carbon and Nitrogen as an Electron Emitting Device: *Damian Carder*[1]; Andreas Markwitz[1]; John Kennedy[1]; [1]GNS Science

The search for cold cathode electron emitters with low-turn on field, high emission current density and high stability remains an active area of research. Silicon incorporating carbon and/or nitrogen is an attractive option for this purpose. This is due to the compatibility with silicon processing technologies and the expected enhanced properties of SiC(N). A cold cathode device from this material system should be more robust, partly due to the superior high temperature performance.Here we demonstrate electron emission from silicon-based nanostructures following ion implantation with carbon and nitrogen. Self-assembled silicon nanostructures were prepared on the surface of wafer silicon, to act as a template, prior to multiple low-energy ion implantations of carbon and nitrogen. Following ion implantation the original distinct surface structure was lost. However, it is shown that a two step electron beam annealing process successfully re-establishes the nanoscale self-assembled surface features. The composition of the ion implanted and annealed layers have been studied using nuclear reaction analysis (NRA) and Rutherford backscattering spectrometry (RBS) which indicate a $Si_{0.6}C_{0.1}N_{0.3}$ layer extending from the surface to a depth of 110 - 130 nm. Electron emission has been measured from the as-implanted and post-annealed samples. The as-implanted sample has a relatively high turn on field of 44 V/µm for a current density of 0.01 mA/cm^2. The implanted and annealed sample, however, shows a low turn on field of 10 V/µm for the same current density. This is comparable to other SiC-based nanostructure electron emission devices. The field emission characteristics demonstrate the promise and feasibility of this method for silicon-based cold cathode technologies.

10:40 AM

II7, High-Quality (211)B CdTe on (211) Si Substrates Using Metal-Organic Vapor-Phase Epitaxy: *Sunil Rao*[1]; Shashidhar Shintri[1]; Justin Markunas[2]; Randolph Jacobs[2]; Ishwara Bhat[1]; [1]Rensselaer Polytechnic Institute; [2]U. S. Army RDECOM CERDEC NVESD

(211)B CdTe is the preferred buffer layer for epitaxial growth of device quality (211)B $Hg_{1-x}Cd_xTe$ films on (211) Si substrates. Molecular beam epitaxy (MBE) has been used to obtain high quality (211)B CdTe films on (211)Si substrates. The 19% lattice-mismatch between CdTe and Si has limited the threading dislocation (TD) density in state-of-the-art MBE-grown material in the mid-10^5cm^{-2} to low-10^6cm^{-2} range. Higher growth temperatures (>400^{o}C) and techniques like epitaxial lateral overgrowth (ELO) used during metal-organic vapor-phase epitaxy (MOVPE) could help in further reducing the TD density. We have previously reported on the successful MOVPE growth of (211)B CdTe on Si substrates using Ge and ZnTe interfacial layers. A cyclic annealing procedure has been used to improve crystal quality during growth of 8µm – 10µm thick CdTe films. The cyclic annealing enhances threading dislocation motion and increases the probability of dislocation interaction and annihilation reactions. Everson etch pit density (EPD) is used to characterize the TD density in (211)B CdTe films. A reduction in Everson EPD was observed for CdTe films grown using the cyclic annealing procedure, EPD was 1x10^7cm^{-2} for a 5µm thick un-annealed film compared with 4x10^6cm^{-2} for a 5µm thick film grown using a cyclic annealing procedure. The lowest EPD observed in this study was 2x10^6cm^{-2} for an 8µm thick film. The good crystal quality of the grown films was also characterized by a low x-ray diffraction (XRD) (422) rocking-curve full-width–at-half-maximum (FWHM) of 85 arc-s. This FWHM value is superior to the previous best FWHM value of 140 arc-s reported for MOVPE grown (211)B CdTe/Si. One of the current challenges in our MOVPE process is the rough surface morphology of the grown CdTe films. The films display an orange-peel-like surface texture when observed using a Nomarski contrast optical microscope. In addition, polycrystalline lumps (density varying from 1x10^3cm^{-2} to 1x10^5cm^{-2}) are also observed on the surface. A modification in the growth temperature from 325^{o}C to 350^{o}C has enabled us to eliminate these polycrystalline lumps. Efforts are currently underway to optimize the other growth process parameters in order to improve the over-all surface morphology.

This work was partially supported by US Army STTR contract W911NF-07-C-0105 through Agiltron Inc. (Dr. Matthew Erdtmann) and US ARMY STTR contract W911NF-08-C-0071 through Brimrose Corporation. Many discussions with Dr. P. Wijewarnasuriya of ARL are also appreciated. We thank Dr. William Clark of ARO for all his encouragement.

11:00 AM Student

II8, Metalorganic Vapor Phase Epitaxial Growth of (211)CdTe on Nanopatterned (211)Ge/Si Substrates Using Full Wafer Block Copolymer Lithography: *Shashidhar Shintri*[1]; Sunil Rao[1]; Huafang Li[1]; Smita Jha[2]; C Liu[2]; Thomas Kuech[2]; Witold Palosz[3]; Sudhir Trivedi[3]; Fred Semendy[4]; Priyalal Wijewarnasuriya[4]; Yuanping Chen[4]; Ishwara Bhat[1]; [1]Rensselaer Polytechnic Institute; [2]University of Wisconsin-Madison; [3]Brimrose Corp. of America; [4]U.S. Army Research Laboratory

Heteroepitaxial growth of HgCdTe on Si substrates is being pursued for the fabrication of large format infrared focal plane arrays. Prior to the growth of HgCdTe, a buffer layer of CdTe is first grown on Si. Molecular beam epitaxy has been the method of choice for growing high quality (211)B oriented CdTe on (211)Si substrates. But the 19% lattice mismatch between CdTe and Si has limited the threading dislocation (TD) density in the state-of-the-art MBE grown material to the low 10^6cm^{-2} range. To reduce the TD density further, various techniques are being pursued such as patterned growth, lateral epitaxial overgrowth etc. In this work, we have investigated MOVPE growth of CdTe on nano-patterned Ge/(211)Si substrates. MOVPE of CdTe directly on Si is difficult due to the presence of Si native oxide. However, by growing a thin Ge layer on Si using germane gas, it has been shown that single crystal CdTe films can be grown on Ge/Si substrates. First, a film (~0.3µm) of Ge is grown on (211)Si, followed by the deposition of 25nm thick SiO_2 layer. A self-assembled block-copolymer (BCP) mask layer has been used to generate a hexagonal pattern of 20 nm holes on 40 nm centers in the 25 nm SiO_2 layer. CdTe is grown on this composite substrate using dimethylcadmium and diisopropyltelluride in a low pressure MOVPE system. Initial growth conditions have been established for selectively growing CdTe within these holes leading to a dense array of small, epitaxial CdTe islands, which has been verified by SEM. The growth of CdTe was carried at temperatures ranging from 325-420°C and pressures varying from 25-250 torr to get the best conditions for selective growth. TEM of a 2µm thick film grown on nano-patterned substrate shows two types of stacking faults generated near the interface, one originating from the Ge/CdTe interface along the <111> direction (F1) and the other originating from the oxide walls and propagating perpendicular to the substrate surface (F2). Blocking of defect motion at the walls of the oxide patterns shows promise for defect reduction in the epitaxial films. A comparison has been made with the epitaxial CdTe grown on blanket Ge/Si wafers, which shows the stacking faults extending into the CdTe layer without annihilation. Selective area electron diffraction (SAED) shows that CdTe grown on blanket Ge/Si wafer is off around 2° with respect to the substrate, where as no such misorientation is observed for the layers grown on nanopatterned substrates. Further growth and characterization results including XRD and AFM of the films will be discussed during the presentation. This work was partially supported by US Army STTR contract W911NF-08-C-0071 through Brimrose Corporation.

11:20 AM Student

II9, Effects of Ex-Situ Cycle Annealing on Dislocation Densities of HgCdTe/CdTe/Si Layers: *Stuart Farrell*[1]; Gregory Brill[2]; Yuamping Chen[2]; Priyalal Wijewarnasuriya[2]; Rao Mulpuri[1]; Nibir Dhar[3]; Karl Harris[4]; [1]George Mason University; [2]U.S. Army Research Laboratory, Sensors and Electronic Devices Directorate; [3]DARPA; [4]Penn State Electro-Optics Center

HgCdTe on Si is a desirable material system for producing large format infrared focal plane arrays. However molecular beam epitaxial (MBE) growth of HgCdTe/CdTe/Si results in layers with large dislocation densities, generally measuring between mid 10^6 cm^{-2} to low 10^7 cm^{-2}. This fact has been shown to result in poorer long-wavelength infrared focal plane array performance with respect to HgCdTe grown on bulk lattice matched CdZnTe substrates. We have developed a process of ex-situ cycle annealing which is capable of consistently reducing the dislocation density in a HgCdTe/Cd/Te/Si layer to ~1x10^6 cm^{-2}.

In this technique, the HgCdTe/CdTe/Si sample is placed face down on a clean piece of a silicon wafer along with ~ 0.5 mL of Hg in a sealed quartz ample, and subjected to multiple number of annealing cycles between the temperatures of 250 °C and 400 °C. The dislocation reduction has been shown quantitatively via etch pit density (EPD) measurements and supported qualitatively via the full width at half maximum (FWHM) measurement of x-ray rocking curves. The main parameter that has been linked to lower EPD is the number of annealing cycles the sample undergoes. An increase in the annealing temperature has been shown to have a minor secondary effect on the resulting dislocation density for temperatures beyond ~400 °C. Below this temperature, there is little to no change in dislocation density. Variations in cycle duration, total annealing time and as-grown dislocation density do not seem to play a major role in the post annealed measurements of the dislocation density with respect to un-annealed material. Excessive amount of Hg during annealing resulted in serious surface pitting, which is deleterious for device applications. For comparison, thermal cycle annealing also has been performed on HgCdTe layers grown on lattice matched CdZnTe substrates. Further properties and parameters of the annealing cycles, such as ramp rate and fine control of exact temperature profiles will be presented.

11:40 AM
II10, Late News

Session JJ: Nonpolar-Semipolar III-Ns

Friday AM
June 25, 2010

Room: 155
Location: University of Notre Dame

Session Chairs: Jae-Hyun Ryou, Georgia Institute of Technology; Christian Wetzel, Rensselaer Polytechnic Institute

8:20 AM Student
JJ1, Internal Quantum Efficiency of Polar and Non-Polar GaInN/GaN Multiple Quantum Wells: *Liang Zhao*[1]; Yufeng Li[1]; Theeradetch Detchprohm[1]; Christian Wetzel[1]; [1]Rensselaer Polytechnic Institute

The heteroepitaxial growth of GaInN/GaN quantum wells (QWs) on c-plane sapphire has long been the favored approach for high power green light emitting diodes (LEDs). However, the strong electric fields in the QWs have been considered a possible reason for the rapid drop of quantum efficiency as the injection current density increases above some 10 A/cm^2. Therefore, growth along non-polar axes, e.g., on a-plane and m-plane, carries a high promise for higher quantum efficiency at higher drive current densities. In this work, we have estimated the internal quantum efficiency (IQE) as a function of excitation power density for GaInN/GaN green MQW structures of both, polar (c-plane) and non-polar (a- and m-plane), growth orientation. We measured the photoluminescence (PL) intensity, both, as function of temperature and optical excitation density. Excitation was performed in resonance with the QWs at 405 nm in cw mode. Under the assumption of negligible non-radiative recombination at T = 4.2 K we obtained an upper estimate of IQE at room temperature. At room temperature (297 K), PL peak wavelengths are 550 nm (c-plane), 485 nm (m-plane), and 510 nm (a-plane). Under optical excitation, the highest IQE value at room temperature is found at about 50% in the c-plane sample at an excitation density of 0.8 kW/cm^2. With increasing excitation density, IQE drops quickly and reaches 33% at 280 kW/cm^2. For the non-polar material the highest IQE is found in the m-plane structure with 36%. The a-plane structure reaches 28%. Furthermore, in both non-polar cases, IQE is found to increase with excitation density, reach their respective maxima at around 2 kW/cm^2. Unlike the polar c-plane case, IQE in both non-polar orientations remains roughly unchanged for higher excitation densities up to the highest tested level of 280 kW/cm^2. At the highest excitation level, IQE values in the m-plane structure actually supersede those in the c-plane material. These results suggest that non-polar a- and m-plane structures show high promise to outperform polar c-plane structures in particular at high excitation levels, such as typically achieved under higher current injection. This work was supported by a DOE/NETL Solid-State Lighting Contract of Directed Research under DE-EE0000627. This work was also supported by the National Science Foundation (NSF) Smart Lighting Engineering Research Center (# EEC-0812056).

8:40 AM Student
JJ2, Optical Polarization of Non-Polar GaInN/GaN LEDs: *Shi You*[1]; Theeradetch Detchprohm[1]; Mingwei Zhu[1]; Wenting Hou[1]; Christian Wetzel[1]; [1]Rensselaer Polytechnic Institute

For GaInN/GaN quantum well (QW) growth along the polar c-axis, huge piezoelectric fields are induced across the QWs that lead to strong Stokes shift in light emission that varies with drive current. Those effects of the piezoelectric polarization can be reduced or avoided by growth along axes perpendicular to the c-axis, e.g. along the m- and a-axes. With the crystal c-axis lying within the QW plane, anisotropic strain is induced that lifts the degeneracy of the GaInN valence band states. The result is a high degree of linear polarization of the emitted light. Linearly polarized light emitters are ideally paired with polarizer transmission modulators such as liquid crystal displays. Suppressing the polarization state of light that cannot be transmitted by the modulators can significantly enhance display system's efficiency, where only linearly polarized light can be transmitted. In this study, we have investigated the optical polarization properties of GaInN/GaN based non-polar LEDs grown on bulk GaN substrate. The polarization ratio is defined as ρ = (I_max-I_min)/ (I_max+I_min) where I_max is the maximum and I_min is the minimum light intensity when measured through a rotated linear polarizer. From the electroluminescence measurement of a green m-plane GaInN/GaN based LED, linear polarization along the a-axis dominates with a single peak at 505 nm, while the polarization component along the c-axis shows a much weaker peak at 491 nm, and the polarization ratio is found to be ρ = 0.77. The polarization ratio of a series of m-plane and a-plane GaInN/GaN MQW samples with different peak emission wavelength is analyzed by room temperature photoluminenance measurement. The excitation laser is 325 nm HeCd laser at power density 10 mW/mm^2. M-plane GaInN/GaN structures reach a polarization ratio of 0.7 at 460 nm and this value grows to 0.9 at 515 nm peak wavelength. For a-plane structures we always find lower values of 0.53 at 400 nm and about 0.6 at 480 nm – 510 nm. The optical polarization performance of c-plane and m-plane LEDs is also compared. For the m-plane LEDs with polarization ratio as large as 0.8, deployment of such device should result in a 55% power saving over a combination of non-polarized c-plane LED with a polarizing filter. Such great advantage in optical polarization of m-plane GaN based LED predicts its future application as the polarized light emitter. This work was supported by DOE/NETL Solid-State Lighting Contract of Directed Research under DE-EE0000627. This work was also supported by the National Science Foundation (NSF) Smart Lighting Engineering Research Center (# EEC-0812056).

9:00 AM Student
JJ3, Anisotropic Carrier Mobility in GaN Quantum Well Grown in Non-Polar Direction: Polarization Induced Dipole and Interface Roughness Scattering: *Aniruddha Konar*[1]; Tian Fang[1]; Nan Sun[1]; Debdeep Jena[1]; [1]University of Notre Dame

GaN-heterojunction based high-electrom mobility transistors (HEMT) has paved the way towards high speed, high power electronics. Though the built-in polarization field in polar-GaN (grown along c axis) has been exploited to achieve dopant free HEMT, for optical devices polarization field plays a negative role due to quantum confined Stark effect. GaN grown in polar direction cannot be used in bipolar devices due to unavailability of hole doping. Moreover, polar GaN-based MOSFET is hard to pinch-off due to inherent presence of two dimensional electron gas (2DEG) at GaN surface. So the recent trend is to explore optical and transport properties of GaN grown in non-polar (m or a plane) direction. Though optical properties of non-polar GaN based devices have been studied quite extensively, transport properties of these devices have not been addressed so far. In this work, we have theoretically investigated charge transport in non-polar GaN quantum well (QW) structures. Let us consider a thin non-polar GaN QW of thickness a sandwiched between aluminum nitride (AlN) barrier as shown in fig. 1a). To consider charge transport in this structure,

we have figure out all sources of disorders present in the QW. One of the most important source of scattering mechanism for thin QW is interface roughness (IRF) as a result of improper growth conditions. GaN, grown along non-polar direction (m plane) shows parallel trench/stripe like patterns which extend infinitely perpendicular to c axis in the plane of GaN. Another new source of disorder in our structure is the polarization bound charges associated with each interface roughness. The difference of in-plane polarization of GaN and AlN induces bound charges at opposite faces of each roughness as shown in fig.1b). These bound charges can be modeled as infinite line charges (fig 1c)) and carrier can scatter from the potential originating from these line charges. We have also considered remote ionized impurity scattering and polar optical phonon scattering in our calculation. Among all the scattering mechanisms mentioned in the above section, interface roughness and polarization-induced line charge scattering are anisotropic (carrier does not feel any potential along the direction of roughness and line charges) but remote ionized impurity and polar-optical phonon scattering found to be isotropic in nature. Using Fermi golden rule and Boltzmann transport equation electron mobility has been calculated. Mobility also shows anisotropic behavior as shown in fig. 2. At room temperatures mobility anisotropy washes out due to strong isotropic polar-optical phonon scattering. In conclusion, we have investigated the charge transport in GaN QW grown in non-polar direction and predicted anisotropic nature of carrier mobility.

9:20 AM

JJ4, MBE Growth of Nitrogen-Face Aluminum Nitride by Polarity Inversion Using Magnesium Overdoping: *Craig Moe*[1]; Wendy Sarney[1]; Anand Sampath[1]; Michael Wraback[1]; [1]U.S. Army Research Laboratory

The growth of aluminum nitride is attracting a great deal of research interest as its wide bandgap and alloying with other III-nitrides make it highly desirable for deep ultraviolet emitters and photodetectors. While most conventional nitride semiconductor devices are grown along the [0001] direction, recent studies have indicated potential benefits of N-face material in both optoelectronic and electronic devices. In this work, we achieve N-face AlN through the overdoping of III-polar AlN with magnesium. Samples were grown by plasma-assisted molecular beam epitaxy on sapphire substrates. An initial buffer layer of Al-face material was deposited at a thickness of 440 nm. Following this, an inversion layer of AlN heavily doped with magnesium was grown at various thicknesses and Mg beam equivalent pressures. Samples were then capped with undoped AlN and silicon-doped GaN. Polarity inversion of the material was observed first through reflection high-energy electron diffraction (RHEED) analysis of the surface, looking for the 3 × 3 reconstruction indicative of N-face nitride material [1]. Polarity was then confirmed with the etching of the top GaN layer in an aqueous solution of KOH. Since KOH selectively etches the nitrogen but not the gallium face of GaN, this results in a roughened surface only when the material is N-face. The GaN cap layer was grown for just this purpose as both faces of AlN etch in KOH. For a Mg beam equivalent pressure of 3.5×10^{8} Torr and a substrate growth temperature of 900°C, samples with a Mg overdoped layer thickness up to 110 nm did not exhibit inverted polarity, while samples with a thickness of 180 nm and above did show polarity inversion. An intermediate thickness of 140 nm displayed a 3 × 3 reconstruction but did not etch in KOH, indicating only a partial inversion of AlN domains. Moreover, when the Mg BEP was dropped to 1.4×10^{8} Torr no polarity inversion was observed for the sample containing the 180 nm-thick Mg overdoped layer. From these measurements we were able to bound the Mg flux and thickness range of the Mg doped layer required for AlN inversion at this growth temperature, which is five to eight times thicker than the values of 25 to 40 nm reported in the literature for the inversion of GaN [2]. Further studies of the dependence of this phenomenon on growth temperature, Mg flux, and Mg doped layer thickness, along with TEM studies of the Mg doped layer, will be presented. [1]E. S. Hellman, MRS Internet J. Nitride Semicond. Res. 3, 11 (1998). [2]S. Pezzagna, P. Vennegues, A. D. Wieck, and J. Massies, Appl. Phys. Lett. 87, 062106 (2005).

9:40 AM

JJ5, Electro-Thermo-Mechanical Simulation of AlGaN/GaN HFETs and MOSHFETs: *Anusha Venkatachalam*[1]; William James[1]; Samuel Graham[1]; [1]Georgia Institute of Technology

AlGaN/GaN-based heterostructure field effect transistors (HFETs) are excellent candidates for high power and high frequency applications. However, current collapse and large gate leakage currents in these devices limit the output performance. Recently, gate insulation has shown to significantly reduce the leakage currents and enable device operation under high gate biases. Several oxides such as SiO_2, Al_2O_3, MgO and Sc_2O_3 have been used as gate insulators, giving rise to metal-oxide-semiconductor HFETs (MOSHFETs) with lower gate leakage currents. Additionally, owing to the complex nature of reliability failure in these devices, it is not clear what the operational stresses are, and it becomes imperative to assess the role of these stresses in long term reliability. In this paper, we focus on the electrical, thermal and mechanical modeling of GaN-based transistors under steady state and pulse mode conditions. Using a coupled electro-thermo-mechanical procedure, we compare self-heating effects and thermal stresses in HFETs and MOSHFETs under various operating conditions, and investigate the influence of device design parameters and boundary conditions on the thermal and mechanical properties. 2-D electrical simulations were performed using the Sentaurus Device simulator, while thermal and mechanical simulations were performed with COMSOL using a one-way coupling procedure. COMSOL was used to first solve the continuum heat transfer equation using the heat generation obtained from Sentaurus Device, and then the thermal expansion strain was determined, followed by the solution of the elasticity equation. Electrical simulations were carrier out near the active regions of the device, while the domain was extended for thermal and mechanical simulations to model realistic heat diffusion. The stress in the device was modeled in two dimensions as in-plane. The active region of the MOSHFET consisted of a 30 nm $Al_{0.2}Ga_{0.8}N$ barrier, a 0.45 µm GaN channel region and a 10 nm SiO_2 insulator layer under the gate. The gate was 2 µm long and 150 µm wide. The HFET comprised of a 25 nm $Al_{0.23}Ga_{0.77}N$ barrier, a 1.2 µm GaN layer with a gate length of 1 µm and gate width of 200 µm. In both cases, the substrate thickness was assumed to be 200 µm. Temperature dependent thermal conductivities were used for the materials in the device. Thermal boundary resistances, thermal effects of metallization, and residual stresses were ignored for simplification purposes. The electrical simulations under steady state indicated that at V_{gs}=0 V, the AlGaN/GaN MOSHFET structure exhibited about 40% increase in the saturated drain current due to the presence of oxide under the gate. Thermal and mechanical simulations showed that the peak temperature at 40 V drain bias was about 10% higher in MOSHFETs and consequently, the thermal stress was also higher under steady state, with the peaks occurring near the drain end of the gate contact.

10:00 AM Break

Session KK: Indium Nitride

Friday AM
June 25, 2010

Room: 155
Location: University of Notre Dame

Session Chairs: Thomas Myers, Texas State University; Steven Durbin, University of Canterbury

10:20 AM

KK1, Mg Doped InN and Search for P-Type InN: *Ke Wang*[1]; Ryosuke Iwamoto[1]; Tomohiro Yamaguchi[1]; Kazuaki Kagawa[1]; Tsutomu Araki[1]; Yasushi Nanishi[1]; Nate Miller[2]; Marie Mayer[2]; Joel W Ager[2]; Kin Man Yu[2]; Wladek Walukiewicz[2]; [1]Ritsumeikan University; [2]Lawrence Berkeley National Laboratory

Recently Mg-doped InN epilayers have attracted much interest to achieve p-type InN in order to exploit its potential device applications. In this work, several series of Mg-doped InN layers were grown by radio frequency plasma assisted

molecular beam epitaxy (RF-MBE) and characterized by various techniques. Mg-doped InN layers were grown at 450°C on GaN/sapphire templates. Mg doping concentration is controlled by Mg cell temperature varying from 150 to 250°C. Secondary ion mass spectrometry (SIMS) measurements have shown Mg concentration increases from $2x10^{18}$ to $5x10^{20}cm^{-3}$ in this temperature range. Influence of undoped InN buffer layers from 0~60nm on Mg doping under same growth conditions has been studied as well. Electrolyte capacitance-voltage (ECV) results have demonstrated net acceptors for InN with Mg concentration from $2x10^{19}$ to $1x10^{20}cm^{-3}$. When applied bias across the interface between electrolyte and InN:Mg is high enough, the surface accumulated electrons can be depleted and thus a depletion layer on the InN side can form with further bias. As a consequence, in C^{-2} vs voltage profiles, a maximum peak can be observed. The peak position for InN with net acceptors shifts from usual n-type InN (net donors in depletion). This shift is due to different band bending and Fermi level position between n- and p-type. The C^{-2} peak shift of p-type InN from n-type is about 0.3~0.6 V, which depends on the Mg doping levels and growth conditions. The slope in depletion condition indicates net acceptor concentration from $7.2x10^{18}$ to $6.0x10^{19}cm^{-3}$. We have noticed the values can vary slightly with measuring frequency but a trend following Mg doping levels is kept. Thermopower measurements have demonstrated positive Seebeck coefficients for some samples at room temperature, confirming existence of free holes. For some samples, although ECV results have demonstrated net acceptors, the Seebeck coefficients are negative but quite close to zero. In fact, our results on a set of InN:Mg samples varying only the thickness of undoped InN buffer layers (n-type) have revealed their significant contribution to the measured Seebeck coefficients. The Seebeck coefficients dramatically changed their signs from -13 to 250μV/K when the thickness of buffer layers decreases from 60 to 0 nm, keeping all other growth conditions exactly the same. The net acceptor concentration estimated from ECV measurements is very close, from 6.0 to $3.3x10^{19}cm^{-3}$ for these samples. Therefore, the dramatic change of Seebeck coefficients is exclusively attributed to the n-type InN buffer layers. Strong PL has been observed for InN with low Mg doping levels. PL spectra clearly demonstrate two peaks: at 0.678eV due to InN band-to-band transition, and at 0.606eV, which is attributed to conduction band to acceptor level transition. Therefore, the acceptor energy level is determined to be 72meV above valence band minimum.

10:40 AM Student

KK2, Dislocation Reduction via Epitaxial Lateral Overgrowth of InN by Selective-Area-Growth of RF-MBE: *Jumpei Kamimura*[1]; Katsumi Kishino[1]; Akihiko Kikuchi[1]; [1]Sophia University

InN has potentialities for optical device applications because of its narrow bandgap of 0.6-0.8 eV. However, there is a difficulty in obtaining a high crystalline quality InN due to the low dissociation temperature and lack of lattice-matched substrates. In general, sapphire is used as a substrate for the growth of InN. So far various buffer layer techniques and an increased film thickness up to 10 μm have been employed, which were valid to some extent, but inefficient in decreasing the dislocation density below 10^9 cm^{-2}. Meanwhile, selective-area growth (SAG) provided epitaxial lateral overgrowth (ELO); it is a dramatically-effective method for reduction of threading dislocation of GaN, as well developed with HVPE and MOVPE. Contrarily, SAG of InN has not been well developed yet. The SAG by MOVPE of InN was tried on GaN template using SiO2 masks, following the conventional SAG of GaN. For preventing crystal deposition on SiO2 masks, a high temperature growth was necessary, but which induced decomposition of InN. Recently, by use of Molybdenum mask, Denker et al. reported SAG of InN at low temperature by rf-MBE. In this study, the SAG of InN was beautifully obtained, by which the first achievement of ELO in InN crystals was demonstrated. Prior to the growth, a thin Mo film was deposited on c-plane sapphire substrate by electron beam evaporation. Subsequently we prepared Mo-mask patterns through electron beam lithography and dry etching, in which hexagonally shaped holes with diameter of 433 nm were arranged in triangular lattice of lattice constant of 1000 nm. After initial nitridation of the substrate surface at 550°C, InN was grown at 510-580°C for 1-60 min. by rf-MBE, producing InN micro-crystals. The grown InN micro-crystals were evaluated with SEM, TEM and micro-PL spectroscopy. The growth of the InN micro-crystals proceeded as follows; the nucleation occurred firstly inside the holes opened in the Mo-mask and then hexagonal nano-disks were formed at 5 min. and then InN grew laterally and vertically. At 60 min., hexagonal geometry columnar InN micro-crystal arrays in closed packing scheme were prepared. The height and diameter were approximately 1.5 μm and 1.0 μm, respectively. TEM observation confirmed that a large number of threading dislocations (10^9-10^{10} cm^{-2}) arose at InN/sapphire interface and propagated in the center area of the InN micro-crystals along the crystal c-axis, while laterally overgrown side areas were nearly dislocation-free. The micro-PL spectrum at room temperature showed the PL-FWHM of 54 meV at the peak energy of 0.63eV, indicating a high quality of the InN. Acknowledgment: This study was partly supported by Grants-in-Aid for Scientific Research on Priority Areas No.18069010, and (B) No.18310079 from the MEXT, Japan.

11:00 AM

KK3, Growth Orientation Control of InN by Pulsed Excitation Deposition: *Hiroshi Fujioka*[1]; Tomoaki Fujii[2]; Atsushi Kobayashi[2]; Jitsuo Ohta[2]; Masaharu Oshima[1]; [1]The University of Tokyo, JST-CREST; [2]The University of Tokyo

We have succeeded in grown orientation control of InN by the use of YSZ substrates with various surface orientations and pulsed excitation deposition (PXD). Growth of nitride semiconductors with nonpolar and sempolar planes has attracted much attention because they can reduce the undesirable effects of the built-in fields. We have recently found that hexagonal InN grows epitaxially on YSZ substrates with various orientations while keeping the epitaxial relationship of YSZ(111)//InN(0001) and InN[11-20]//YSZ[1-10]. With this notion, we prepared YSZ substrates with various orientations to obtain InN(1-10m) and InN(11-2n) with various indices, m and n. We confirmed the growth of InN(1-105), InN(1-103), InN(2-205), InN(1-101) on YSZ(112), YSZ(113), YSZ(110), and YSZ(100), respectively. We have also confirmed the growth of InN(11-27), InN(11-26), and InN(11-24) on the YSZ substrates with the (111) plane inclined toward the YSZ[1-10] direction by 23.8°, 28.3°, and 38.9° from the sample normal. These results indicate that epitaxial relationship of InN[0001]// YSZ[111] and InN[11-20]//YSZ[1-10] is quite universal for this InN/YSZ system probably because the arrangement of atoms on the YSZ(111) plane is quite similar to that for InN(1000) and the lattice mismatch between YSZ(111) and InN(0001) is as small as 2.7%. Since we succeeded in choosing growth direction of semipolar InN at will, we have investigated the growth direction dependence of the surface morphology of semipolar InN using AFM. We have found that the growth directions with the low Miller indices lead to smooth surfaces. This fact indicates that the precise control of the surface direction of the YSZ substrates is inherently important for devices that utilize hetero-interfaces. We have also tried to grow the semipolar-AlN/InN hetero-structure which can be used for the fabrication of devices such as future InN based FETs. Although the growth of AlN on the semipolar InN films at conventional growth temperatures for AlN caused serious intermixing reactions between AlN and InN, the use of the PXD low temperature growth technique leads to formation of an atomically abrupt semipolar-AlN/InN heterointerface. In summary, we have found that we can control growth orientation of semipolar InN and fabricate the semipolar-AlN/InN heterostructure by the use of PXD and YSZ substrates with various orientations.

11:20 AM Student

KK4, Optical and Electrical Transport Properties of Nearly Intrinsic and Si-Doped InN Nanowires: *Yi-Lu Chang*[1]; Feng Li[1]; Jiale Wang[1]; Hieu Nguyen[1]; Zetian Mi[1]; [1]McGill University

InN nanowires have emerged as a promising candidate for a range of nanoelectronic and nanophotonic devices, due to its low direct bandgap, high electron mobility, and large saturation velocity. However, conventional InN nanowires exhibit tapered morphology and extremely large inhomogeneity. Consequently, a thorough understanding of their fundamental optical and electrical transport properties has not been possible, which severely limit their device applications. In this context, we have performed a detailed investigation of the molecular beam epitaxial (MBE) growth and characterization of non-tapered, nearly homogeneous InN nanowires, which exhibit a very narrow photoluminescence (PL) linewidth of ~ 10 meV, compared to the commonly

reported values of ~ 50 - 100 meV. It is further observed that both the optical and electrical transport properties of InN nanowires depend strongly on the Si-doping concentrations. In this experiment, InN nanowires were grown on Si(111) substrates using MBE. Prior to the growth initiation, a thin (~ 0.5 nm) In seeding layer was first deposited on the Si substrate, which can promote the formation and nucleation of InN nanowires. Both non-doped and Si-doped InN nanowires, with Si concentrations in the range of ~ 1×1017 – 1×1019 cm-3, were grown and characterized. The resulting InN nanowires exhibit non-tapered morphology and are nearly free of dislocations. The optical properties of InN nanowires were studied using temperature variable PL spectroscopy. We measured a record narrow spectral linewidth of < 10 meV at 5 K. With the increase of excitation power, there is a considerable blue shift in the peak energy and a drastic increase in the spectral linewidth. Such a strong band-filling effect and the absence of Burstein-Moss shift has not been previously observed, suggesting the achievement of nearly intrinsic InN nanowires. We have also measured the electrical transport properties of single InN:Si nanowires, which exhibit a resistivity of ~ 0.002 O cm. The temperature-dependent optical and electrical transport properties of such InN nanowires, as well as their dependence on Si doping concentrations are being investigated. These results, in conjunction with the achievement of single InN nanowire lasers will be presented.

11:40 AM Student

KK5, Growth Optimization of Si_3N_4 on GaN by Metal-Organic Chemical Vapor Deposition: *Brian Swenson*[1]; Ramya Yeluri[1]; Umesh Mishra[1]; [1]University of California at Santa Barbara

Si_3N_4 is commonly used in the Gallium-Nitride system (GaN, AlGaN) as both a gate insulator and as a passivation layer. Interface states exist at the interface between Si_3N_4 and GaN due to defects, dislocations and vacancies [J. Elec. Mat., Vol. 36, No. 9 (2007)] to name a few. In order to improve device performance and reliability, the growth of Si_3N_4 on GaN must be optimized to reduce the creation of interface states. The Photo-Assisted Capacitance-Voltage measurement [Swenson et al. J. Appl. Phys. 106, 064902 (2009)] was used to determine the interface state density. The growth temperature was varied from 800C to 1220C to find an optimum temperature that minimizes the generation of interface states. The optimal growth temperature was found to be at or above 1165C; the growth temperature of GaN. Temperatures above the GaN growth temperature also yielded optimal results (up to 1220C). The interface state density ranged by almost an order of magnitude from 1.15e13 cm^{-2} eV^{-1} at 800C to 2.1e12 cm^{-2} eV^{-1} at 1220C.