

Plenary Session

Wednesday AM Room: Jordan Auditorium, Mendoza College of Business
June 23, 2010 Location: University of Notre Dame

8:20 AM Awards Ceremony

8:30 AM Plenary

Epitaxial Graphene: Designing a New Electronic Material: *Walter A. de Heer*¹; ¹Georgia Institute of Technology

Since 2001 the Georgia Tech epitaxial graphene research team and its collaborators have developed the new field of epitaxial graphene electronics. The current status of epitaxial graphene research will be presented, including the production methods and recent results from various characterization investigations. Methods have been developed to grow monolayer and multilayer epitaxial graphene (MEG) on the C-face of hexagonal silicon carbide with of up to 100 graphene sheets and its extraordinary transport properties have been demonstrated, including the quantum Hall effect. The monolayer films have high mobilities and exhibit the half integer quantum Hall effect. The Georgia Tech Confinement Controlled Sublimation method to produce uniform epitaxial graphene layers will be explained. Surprisingly, the properties of MEG are closely related to monolayer graphene rather than graphite, as a result of an unusual rotational stacking of the graphene layers that causes the graphene sheets to electronically decouple. Consequently the electronic band structure of MEG is composed of Dirac cones. The charge carriers are chiral and exhibit a non-trivial Berry's phase. Weak anti-localization and quantum confinement has been demonstrated. Landau level spectroscopy further exhibits record-breaking room temperature mobilities and well resolved Landau levels below 1 T, indicating extremely low carrier densities and good homogeneity of the material. Efforts towards large-scale electronic device patterning will be reviewed.

9:20 AM Break

Session A: High-K Gate Dielectrics

Wednesday AM Room: 102
June 23, 2010 Location: University of Notre Dame

Session Chairs: John Conley, Oregon State University; Peter Moran, Michigan Technological University

10:00 AM Invited

A1, The Electrical Properties of Metal/Gd₂O₃/Si Gate Stacks and Their Dependence on the Structure of the Oxide Layer: *Moshe Eizenberg*¹; Eran Lipp¹; ¹Technion-Israel Institute of Technology

Future downscaling of metal-oxide-semiconductor (MOS) devices relies on the successful introduction of high-k dielectrics and metal electrodes, which will replace the traditional poly-Si/SiO₂ gate-stack. Gd₂O₃ is one of the only materials that have been reported to suit the industry's requirements for 2016. In addition, Gd₂O₃ has a low lattice mismatch to Si, which enables the growth of a single-crystalline oxide layer. Additional structures can be obtained by controlling the oxide growth temperature and substrate orientation. The aim of this research is to study the effect of oxide structure on the electrical properties of metal/Gd₂O₃/Si gate stacks. Electrical properties were studied by examining MOS capacitors with either Pt or Ta as the metal gates. Three different structures of Gd₂O₃ were deposited by molecular-beam epitaxy (MBE). Amorphous layers were deposited at 90°C, while layers deposited at 600°C were crystalline, and their morphology was observed to depend on the Si orientation. Single-crystalline layers were obtained on Si(111), whereas on Si(100), domain-structured layers were obtained. In the case of domain-structured Gd₂O₃, a silicate-like interfacial layer was observed at the oxide/Si contact. Electrical measurements revealed that the k-value of this interfacial layer is lower than that of the oxide itself. The

electrical properties of Gd₂O₃ were observed to be almost independent of the oxide structure. The oxide k-value was similar for all structures, however, the k-value of domain-structured Gd₂O₃ (17.7±0.8) was somewhat higher than those of single-crystalline (16.3±0.7) and amorphous (16.9±0.8) layers. The electron effective mass in crystalline Gd₂O₃ was found to be (0.1±0.02)m₀, while for amorphous layers, a value of (0.5±0.1)m₀ was obtained. The conduction mechanism through crystalline Gd₂O₃ was found to be contact-limited in most of the measured conditions; with a barrier height of (0.6±0.1) eV at Pt/Gd₂O₃ interfaces. This value is explained by the existence of a defect-related energy band in the oxide. In contrast to the oxide properties, the extent of Fermi-level pinning at metal/Gd₂O₃ interfaces was found to be significantly affected by the oxide structure. At metal/single-crystalline Gd₂O₃ interfaces, Fermi-level pinning was negligible, while at metal/amorphous Gd₂O₃ interfaces, a dominant pinning effect could be observed. These results are explained in terms of the metal-induced gap states model.

10:40 AM Student

A2, Spin Dependent Trap Assisted Tunneling in Gd₂O₃ Dielectrics: *Brad Bittel*¹; P.M. Lenahan¹; E. Lipp²; M. Eizenberg²; ¹Penn State Univ.; ²Technion-Israel Institute of Technology

We report on magnetic resonance detected via spin dependent trap assisted tunneling (SDT) in MBE deposited epitaxial single crystal Gd₂O₃¹⁻³ films 3.6nm thick on (111) Si substrates. In previous publications, we reported on the electrical properties, as well as the thermal stability of these films.³⁻⁵ SDT is a relatively new technique;⁶ this work represents the first report of the technique's utilization on Gd₂O₃ and, to the best of our knowledge, the first report of SDT on any epitaxial dielectric film on silicon. In SDT a magnetic resonance induced change in a trap assisted tunneling current is generated by simultaneously exposing the device under observation to a large magnetic field and microwave irradiation such that the microwave frequency and magnetic field satisfy the magnetic resonance condition of a defect with levels playing dominating roles in trap assisted tunneling. In our study, we observe a single magnetic resonance line characterized by g=1.9996 and a peak to peak line width of 14 Gauss. The SDT response is strongly bias dependent. We are unable to detect any SDT response for positive gate polarities and observe an SDT response in which the absolute amplitude which grows monotonically with increasing negative gate magnitudes, up to the point that our preamplifiers saturate. However, the relative strength of the SDT response, that is the ratio of the SDT induced tunneling current change divided by the absolute magnitude of the tunneling current is fairly sharply peaked, at a gate bias of approximately minus one volt. Our results are consistent with a defect with levels in the upper part of the Gd₂O₃ band gap. Such a defect level may explain the findings of our conductivity studies, which also indicate the existence of a defect-related energy state in the oxide band-gap. A fairly extensive literature dealing with conventional electron paramagnetic resonance measurements on large volume samples containing Gd₂O₃ exists.⁷⁻⁹ These studies almost invariably report observation of a spectrum with a zero crossing g = 2.0 which is generally assigned to Gd³⁺ ions. We cannot at this point in our study conclude that the observed SDT response has the same origin, and note only that such an assignment appears to be plausible. [1] M. Czernohorsky, et al., Appl. Phys. Lett. 88, 152905 (2006). [2] Q.Q. Sun, et al., Appl. Phys. Lett. 92, 152908 (2008). [3] E. Lipp, et al., MRS Proc. 996E, H03-08 (2007). [4] E. Lipp, et al., Appl. Phys. Lett. 93, 193513 (2008). [5] E. Lipp, et al., J. Appl. Phys. 106, 113505 (2009). [6] J.T. Ryan, et al., Appl. Phys. Lett. 95, 103503 (2009). [7] D.L. Griscom, J. Non-Cryst. Solids. 40, 211 (1980). [8] C.M. Brodbeck, J. Chem. Phys. 83, 4285 (1985). [9] I. Ardelean et al., J. Non-Cryst. Solids. 353, 2363 (2007).

11:00 AM

A3, Crystalline Lattice-Matched Ba_{0.7}Sr_{0.3}O on Si(001) as Gate Dielectric: *Herbert Pfnür*¹; Dirk Müller-Sajak¹; Alexander Cosceev¹; Karl Hofmann¹; ¹Leibniz Universität Hannover

The alkaline-earth metal oxides BaO and SrO as insulators with high relative dielectric constants of 34 and 14.5, and with band gaps of 4.2 and 6.3 eV, respectively, crystallize in the cubic rock salt structure and are miscible. As we have demonstrated previously, the mixed oxide Ba_{0.7}Sr_{0.3}O can be grown

epitaxially with the average lattice constant of Si (5.43 Å) as a lattice-matched monocrystalline film on Si(001), with a band gap of 4.3 eV and conduction and valence band offsets of approximately 1.0 eV and 2.2 eV to Si. Oxide films with thicknesses between 5 and 20 nm were prepared by molecular beam epitaxy with the samples at room temperature. Pure BaO and SrO grow only as amorphous layers because of their significant lattice mismatch (+2.4% of BaO, -5.2% for SrO) with respect to Si(001). For the mixture of 70% BaO and 30% SrO, however, perfectly crystalline $Ba_{0.7}Sr_{0.3}O$ films were grown, as revealed by X-ray photoelectron spectroscopy (XPS) and LEED. The interface to Si(001) is atomically sharp with no formation of SiO_2 or silicide. For the electrical measurements, $Au/Ba_xSr_{1-x}O/n-Si(001)$ MOS capacitors were fabricated by growing a 110 nm thermal SiO_2 layer, by lithographical patterning of active windows, and by deposition of the $Ba_xSr_{1-x}O$ films and Au metal gates in situ through openings in a tungsten mask overlapping the active windows. These diodes were analyzed by C-V and I-V measurements. They exhibited typical high-frequency C-V curves without frequency dispersion in the frequency range between 50 kHz and 1 MHz. All C-V curves had only negligible hystereses (<1 mV), indicating the absence of significant rechargeable trap densities in the oxides. The flatband voltages are within 0.3 V of the expected $Au/n-Si$ work function differences, suggesting the absence of larger oxide charges. The effective dielectric constants $\epsilon_{eff} = C_{acc,max} \times d_{ox} / \epsilon_0$ determined within a 3-element model are only slightly (10-15%) below the bulk values, which indicates the absence of appreciable interface layers. The leakage current density (at $V_G = V_{FB} + 1V$) is comparatively large in the amorphous diodes, but it is several orders of magnitude lower ($2.1 \times 10^{-5} A/cm^2$) in the crystalline $Ba_{0.7}Sr_{0.3}O$ diode. The $Ba_{0.7}Sr_{0.3}O$ diode has a minimum interface trap density value, D_{it} , of only $6.3 \times 10^{10} cm^{-2}eV^{-1}$, two orders of magnitude below the amorphous oxides. These very low D_{it} values are comparable to those of the SiO_2/Si interface. Both low leakage currents and low D_{it} seem to be related to the perfectly lattice matched crystalline $Ba_{0.7}Sr_{0.3}O/Si$ interface. We conclude that the crystalline gate oxide $Ba_{0.7}Sr_{0.3}O$ displays remarkable electrical properties without any (N_2/H_2) postdeposition annealing procedures: high effective dielectric constant, absence of hysteresis, low leakage currents, and very low interface trap densities in the range of SiO_2/Si .

11:20 AM Student

A4, Rare-Earth Scandates/Tin Gate Stack on High Mobility Strained SOI for Fully Depleted (FD) Mosfets: Eylem Durgun Özben¹; J. M. J Lopes¹; A. Nichau¹; R. Luptak¹; Roeckerath¹; S. Lenk¹; A. Besmehn¹; B. Ghyselen¹; Q.-T. Zhao¹; J. Schubert¹; S. Mantl¹; ¹Jülich Research Center

High permittivity materials are needed for high performance applications in CMOS technology. Among those materials, rare-earth scandates ($REScO_3$, RE = Tb, Gd, La..) have gained considerable attention due to their excellent properties [1]. They show high thermal stability on silicon ranging from 800°C to 1000°C, κ values in the range of 23-29 and large optical band gaps (>5 eV) and band offsets to silicon (2-2.5 eV) [2 and references therein]. Silicon on insulator (SOI) and strained silicon on insulator (sSOI) are considered as promising channel materials for MOSFETs due to excellent dielectric isolation between devices, reduction in parasitic capacitance and increase in circuit speed. In this study, we have investigated Terbium scandate ($TbScO_3$), Gadolinium scandate ($GdScO_3$) and Lanthanum scandate ($LaScO_3$) as gate dielectrics on SOI and sSOI substrates in fully depleted (FD) MOSFETs. $TbScO_3$ and $GdScO_3$ films were grown by electron beam evaporation while $LaScO_3$ films were grown by molecular beam deposition. Device preparations were carried out with a conventional gate last process (for $GdScO_3$) and a replacement gate process (for $TbScO_3$ and $LaScO_3$). The composition of the films was measured by Rutherford back scattering spectrometry. For all of the films, the RBS results reveal a ratio of 1:0.9-0.95 for the metallic elements (Tb:Sc, Gd:Sc, La:Sc). Film chemistry together with the silicon/high- κ interface was investigated using X-ray photoelectron spectroscopy. For as deposited samples, a silicate like interface is observed. After thermally treating the films in oxygen and forming gas ambient consecutively, the $TbScO_3$ keeps the inter-layer in silicate form, while for $LaScO_3$ a silicate- SiO_2 like interface is observed. Devices were prepared and electrically characterized. Due to process differences, in the conventional gate last MOSFETs a high series resistance has been observed which degrade the

device performance. Despite this, well behaved output and transfer curves with high output current and I_{on}/I_{off} ratios up to 10^9 with a steep subthreshold slope could be observed. The mobilities of the devices extracted either by split CV or $I_d/\sqrt{I_{g_m}}$ technique are about 147-185 $cm^2/Vsec$ for SOI and around 350-400 $cm^2/Vsec$ for sSOI devices. [1] J. Robertson, J. Appl. Phys. 104, 124111 (2008). [2] E. Durgun Özben, J.M.J. Lopes, M. Roeckerath, St. Lenk, B. Holländer, Y. Jia, D.G. Schlom, J. Schubert, S. Mantl, Appl. Phys. Lett. 93, 052902 (2008).

11:40 AM

A5, Late News

Session B: Non-Destructive Characterization

Wednesday AM
June 23, 2010

Room: 126
Location: University of Notre Dame

Session Chairs: Kurt Eyink, Wright-Patterson AFB; Gregory Triplett, University of Missouri-Columbia

10:00 AM

B1, Innovative Time-Resolved Optical Characterization Techniques for Monitoring of Carrier Dynamics in Wide Band Gap Semiconductors: Kestutis Jarasiusnas¹; Tadas Malinauskas¹; Ramunas Aleksiejunas¹; Arunas Kadys¹; Saulius Nargelas¹; Vytautas Gudelis¹; ¹Vilnius University

The given report presents innovative nonlinear optical techniques and demonstrate their metrological potential for *ex-situ* monitoring of nonequilibrium carrier dynamics in wide band gap materials and for determination of electronic parameters. We took advantage of laser-induced transient and spatial modulation of the optical properties of a semiconductor using its excitation by a short pulse of light-interference field and recording a transient diffraction grating. Development of transient grating (TG) techniques required to combine interdisciplinary knowledge in nonlinear optics, dynamic holography, semiconductor physics and technology. This novel methodological approach provided much deeper insight into materials properties due to specificity of nonequilibrium processes at isothermal relaxation stage: in contrast to linear optical properties at equilibrium state, the *nonlinear* optical spectroscopy of photoexcited semiconductors opened access to a variety of *nonequilibrium* processes. Consequently, the innovative time-resolved metrology via optical monitoring of spatial and temporal carrier dynamics provided direct and quantitative information about electronic parameters, which directly revealed materials quality and allow to predict a device performance. Experimentally, different TG schemes have been utilized to disclose various mechanisms of optical nonlinearities in pico- and nanosecond time domains. These schemes represent three cases of recording/reading the dynamic holograms - thin diffraction gratings (1), Bragg gratings (2), and transient reflection gratings (3). Combining these schemes with the mechanisms for modulation of the optical and electrical properties enabled investigation of free-carrier (and electron spin) dynamics via free-carrier (or exciton) nonlinearity (1), free carrier and space-charge filed dynamics via photorefractive nonlinearity (2), and selectively study a recovery of optically recharged deep traps in presence of other recombination channels via gratings in deep traps (3). The developed algorithms were used to extract from the diffracted optical signal the important electronic parameters, which directly revealed materials quality, namely, the nonequilibrium carrier lifetime, bipolar and/or monopolar diffusion coefficients, carrier diffusion length, recombination rate at a surface, in the bulk, or at interface, threshold of stimulated recombination, type of carriers photoexcited from deep traps, rate of recovery of recharged traps. We demonstrate the *metrological capabilities* of TG techniques by investigating carrier dynamics in various wide bandgap materials: III-nitride heterostructures grown on different substrates (sapphire, Si, SiC), InGaN alloys with varying In content, quasi-bulk GaN, In-rich and InN layers, cubic and hexagonal SiC polytypes, heavily doped III-V layers, and synthetic diamonds. Time-resolved TG technique was found more advantageous than the time-resolved photoluminescence, as it allowed to clarify the origin of fast

photoluminescence transients in thick GaN layers as carrier in-depth diffusion. Moreover, picosecond TG enabled direct determination of carrier lifetime and diffusion length in a wide range of threading dislocation density in GaN layers, to separate contributions of radiative and nonradiative recombination channels for analysis of a quantum efficiency droop problem.

10:20 AM

B2, Raman Characterization Methodologies Suitable for Determining Graphene Thickness and Uniformity: *David Tomich*¹; John Hoelscher¹; Jeongho Park¹; Bruce Clafin¹; Kurt Eyink¹; William Mitchel¹; ¹USAF/AFRL

Graphene has seen an exponential increase in interest since it was isolated by Geim et al. in 2004 via mechanical exfoliation. A brief survey of the current literature will find numerous groups using everything from mechanical exfoliation of graphite, to silicon sublimation of SiC, to chemical vapor deposition on metal crystals to produce single to few layer graphene. The attraction to graphene is due largely to its unconventional band structure which is a promising pathway towards nanoscale carbon electronics. Raman spectroscopy is a powerful non-destructive probe that has been used extensively over the past few decades to study carbon based materials, so applying confocal Raman spectroscopy to graphene is a natural extension. Several analysis methods have been used to determine the quality of graphene films and to determine the number of graphene layers present in these films. We have examined several of these methodologies and applied them to determine the uniformity of a graphene layer grown on a 2-inch 4H-SiC wafer by Si sublimation. We have examined Raman spectra from a series of 1 μm diameter spots evenly spaced across the sample and determined peak positions, peak heights, FWHM and integrated peak intensities for the D, G and 2D graphene bands after subtracting the SiC bands. These data were analyzed by looking at the G to 2D band integrated intensity ratio, SiC signal attenuation, 2D band full width at half maximum of a single Lorentzian and 2D multiple peak fitting to determine the layer thickness at each location. While most of these analyses appear to be adequate to determine cross-wafer uniformity, there is little agreement between these approaches on the number of layers present. We will discuss the different analysis methods and their relative accuracies and sources of error in relation to our data.

10:40 AM Student

B3, Characterizing the RF Properties of Semiconductors under Optical Illumination: *Youssef Tawk*¹; Alex Albrecht²; Sameer Hemmady¹; Ganesh Balakrishnan²; Christos Christodoulou¹; ¹University of New Mexico; ²Center for High Technology Materials

The ability to alter the Radio Frequency (RF) conductivity of semiconductor materials by exposing them to light of suitable wavelength is opening up several exciting possibilities in the field of reconfigurable microwave systems. For instance, such materials can be used as optically-activated switches to dynamically alter the RF behavior of microwave circuit components and antennas in a rapid and controlled fashion, thereby paving the way for reconfigurable systems such as Cognitive Radios. Characterizing the change in the RF properties of such materials (RF conductivity, loss tangent, dielectric constant, etc.) as a function of the incident light-intensity is thus critical to the proper design and engineering of such reconfigurable systems. In this talk, we present a solid-state model that predicts the change in the RF properties of semiconductor materials as a function of incident light intensity from a suitably energetic laser. We then apply this model to a piece of silicon (smaller than a wavelength at the microwave frequencies of interest) and predict the change in dielectric constant, RF conductivity and dielectric losses as a function of the laser power. This model is then experimentally validated by performing microwave measurements on a stripline circuit incorporating a silicon bridge and compared with numerical electromagnetic simulations. Finally, we show the applicability of this model to reconfigurable systems, by demonstrating the performance of a reconfigurable antenna whose RF properties are controlled by the ON/OFF state of optically activated silicon switches. Good agreement between the measured RF response of the antenna and numerical simulations validate that the solid-state model accurately describes the behavior of the semiconductor material under varying intensities of light illumination.

11:00 AM Student

B4, Admittance Spectroscopy of GaSb(100) and ALD/PEALD Al_2O_3 Dielectric Interface with Various Surface Treatments: *Ashkar Ali*¹; Himanshu Madan¹; Mantu Hudait¹; Dalong Zhao¹; Devon Mourey¹; Thomas Jackson¹; Suman Datta¹; ¹The Pennsylvania State University

Antimonide based compound semiconductors have gained considerable interest in recent years due to their superior electron and hole transport properties. Schottky gated quantum well transistor architectures using InSb [1, 2] and $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ [3] have been demonstrated with excellent electron and hole mobility. Complementary n-MOS and p-MOS quantum well FETs (MOS-HEMTS) integrating a high quality dielectric is needed to demonstrate a scalable device architecture for 15 nm logic technology node and beyond. It is hypothesized that an ultra-thin GaSb surface layer is more favorable toward high-k integration than $\text{In}_{0.2}\text{Al}_{0.8}\text{Sb}$ barrier as it avoids Al at the interface and the associated surface oxidation. Here, we study the effects of various surface passivation approaches on the capacitance-voltage characteristics of Te-doped n-GaSb(100) MOS capacitors made with ALD and Plasma Enhanced ALD (PEALD) Al_2O_3 dielectric. PEALD was employed to reduce the thermal budget of dielectric deposition, particularly important for antimonide semiconductors. The control sample without surface preparation showed a pinned Fermi level. From the admittance spectroscopy analysis, we conclude that the ALD samples show weak Fermi level pinning along with very fast interface trap response. The PEALD samples show well modulation of the Fermi level along with weak inversion. It is believed that the absence of water precursor in PEALD process, coupled with low thermal budget, leads to a better quality interface. In summary, we have demonstrated GaSb MOS capacitors with unpinned Fermi level at the oxide semiconductor interface using PEALD Al_2O_3 . XPS measurements are under progress to investigate the residual chemical species at the interface after the various surface preparation techniques.

11:20 AM Student

B5, High Temperature Coefficient of Resistance Sputtered A-Ge for Uncooled Microbolometer Applications: *Hang-Beum Shin*¹; Myung-Yoon Lee¹; David John¹; Nikolas Podraza¹; Thomas Jackson¹; ¹The Penn State University

Hydrogenated amorphous silicon, amorphous germanium, and their alloys are of interest for uncooled infrared sensing microbolometer devices. In these applications, the properties of interest include controllable resistivity, high temperature coefficient of resistance TCR values, and low 1/f noise. Amorphous silicon (a-Si) and germanium (a-Ge) films exhibit relatively high TCR, may be deposited as uniform layers, and are prepared using more mature deposition processes than the other commonly used material in these types of devices, vanadium oxide. Recently, plasma enhanced chemical vapor deposited boron doped amorphous silicon germanium ($\text{a-Si}_{1-x}\text{Ge}_x\text{:H:B}$) and magnetron sputtered silicon germanium oxide (SiGe_xO_y) films have been reported with relatively high TCR values of -2.7 %/K and -4.86 %/K for films with resistivities of 100 Ωcm and 245 Ωcm , respectively [1,2]. Optimization of the $\text{a-Si}_{1-x}\text{Ge}_x\text{:H}$ system for use in devices requires a better understanding of the relationship between TCR and 1/f noise in films with resistivity relevant to the current demands of the read out circuitry. To assess how variations in composition and structure affect these electrical characteristics, a-Ge films have been deposited using DC magnetron sputtering in mixed atmospheres of argon, hydrogen and nitrogen. After sputtering, titanium top electrodes are prepared in a transfer length method (TLM) pattern for measurement of resistivity and TCR, while resistors with three different volumes are made for volume normalization of the 1/f noise measurement. The TCR is typically measured from room temperature to 55C. Spectroscopic ellipsometry over a range from 1.2 to 3.35 eV is used to extract the a-Ge film thickness and approximate the band gap obtained by fitting the complex dielectric function spectra using a Tauc-Lorentz oscillator [3]. The TCR and equivalent activation energy can be thought of as a function of the tail states in the band structure, so that different slopes of the tail state densities influence how many carriers proportionally occupy these localized states with respect to the extended states in the conduction or valence band as temperature increases. Nitrogen dopant in germanium has been reported to have an activation energy of 0.23 eV by photoluminescence measurements with a corresponding TCR of

-3.1 %/K [4,5], which are in agreement with our TCR measurements. Thus, it is desirable to draw correlations between the deposition conditions and the 1/f and TCR characteristics in terms of the tail states. In this work, a-Ge films have been prepared under variable deposition temperatures, sputtering atmospheres containing hydrogen and nitrogen, and with boron co-sputtering to assess how variations in the electrical properties (resistivity, TCR, 1/f noise) correlate to film composition and microstructure.

11:40 AM Student

B6, Temperature Dependence of the Lattice Constant of Popular III-Sb Binary and Quarternary Alloys: *Magnus Breivik*¹; Tron Arne Nilsen¹; Saroj Kumar Patra¹; Geir Myrvågnes¹; Espen Selvig²; Bjørn-Ove Finland¹; ¹Norwegian University of Science and Technology (NTNU); ²Norwegian Defence Research Establishment (FFI)

III-Sb alloys are of great interest for mid-infrared (2-5 μm) optoelectronics. For epitaxial growth of structures based on these materials, it is important to have accurate values of the lattice constants both at room temperature and at the growth temperature, due to thermal misfit. This is particularly important when thick layers with minimal dislocation density are needed, such as AlGaAsSb cladding layers in mid-infrared laser structures. Using X-ray diffraction (XRD), the lattice constants of GaSb [1], Al_{0.90}Ga_{0.10}AsSb_{1-y} [2], and AlSb (preliminary) have been measured up to 550°C, as literature data on the lattice constant for these materials are either differing or lacking at higher temperatures. The lattice constants of unstrained AlGaAsSb and AlSb were obtained using asymmetric XRD measurements [3] of strained epilayers grown on either GaSb(001) or GaAs(001) substrates in a Varian Gen II Modular molecular beam epitaxy (MBE) system. The technique allows determination of the in-plane and out-of-plane lattice constants, from which the lattice constant of unstrained material was calculated. For GaSb, measurements were performed on epi-ready GaSb(001) wafers. The following polynomial functions for the temperature dependent lattice constants were deduced from our measurements: $a_{\text{AlSb}} = 6.1350 + 3.20\text{E-}5 * T$ $a_{\text{GaSb}} = 6.0959 + 3.37\text{E-}5 * T + 5.63\text{E-}8 * T^2 - 1.29\text{E-}10 * T^3 + 1.05\text{E-}13 * T^4$ $a_{\text{AlGaAsSb}} = 6.1310 - 0.4702 * y + 2.856\text{E-}5 * T + 5.03\text{E-}9 * T^2$ (0.003 < y < 0.065) All lattice constants are given in Å, and all temperatures are in °C. The polynomial functions are valid from room temperature up to approximately 550°C. Our data suggest that some of the literature values need revision, in particular for AlSb.

Session C: Nanoscale Characterization

Wednesday AM
June 23, 2010

Room: 129
Location: University of Notre Dame

Session Chairs: John Schlager, NIST; Lincoln Lauhon, Northwestern

10:00 AM Student

C1, Pulsed-Laser Atom Probe Tomographic Analysis of Ge-Ge/Co/Mn Thin-Film Superlattices: *James Riley*¹; Daniel Perea²; Lincoln Lauhon¹; Frank Tsui³; ¹Northwestern University; ²Los Alamos National Laboratory; ³University of North Carolina

Magnetic semiconductors can provide the basis for spintronic devices that utilize electron spin to store and transmit information. Dilute magnetic semiconductors are made by doping semiconductors with paramagnetic impurities, such as Mn, which may become ferromagnetically ordered through interactions with itinerant carriers. Magnetic dopants typically have a low solubility in the semiconductor host, making the alloys unstable with respect to the formation of small clusters and phase segregation. As clusters as small as dimers can be ferromagnetic, it is important to characterize the material inhomogeneity on the smallest length-scales and with the highest possible sensitivity. Pulsed-laser atom probe tomography (PLAP) can be used to examine variations in the composition of a material with sub-nanometer spatial resolution and single atom sensitivity, making it a uniquely powerful tool. It complements transmission electron microscopy (TEM) based techniques, which provide

excellent spatial resolution but are less sensitive to composition, and secondary ion mass spectroscopy (SIMS), which provides single atom sensitivity but has relatively poor spatial resolution. We have used PLAP to analyze a superlattice structure consisting of alternating layers of intrinsic Ge and Ge co-doped with Co and Mn. The Ge-Ge_{1-x}-yCo_yMn_x superlattice thin film was grown by the Tsui group by molecular beam epitaxy (MBE). A section of the thin film was prepared for PLAP analysis by a lift-out and milling process using a focused ion beam (FIB) to create a needle-shaped specimen with a tip diameter less than 100 nm. The specimen was analyzed using PLAP with a 523 nm laser with a pulse energy of 0.6 nJ, a pulse frequency of 100 kHz, and an evaporation rate of 0.2% at a temperature of 80 K. Approximately 4.5 million atoms were collected. Analysis of the 3-D reconstruction revealed Co and Mn rich clusters within the co-doped layers. Within an isolated co-doped layer, we determined the composition of Co and Mn within the 'clusters' to be 12% and 6%, respectively, which is nearly a factor of two higher than the average concentration within the entire layer. Further, a 1-D concentration profile taken along the PLAP analysis direction and parallel to the growth direction indicated enhanced Co and Mn concentrations at the interfaces between the intrinsic Ge and co-doped Ge layers. Co-Mn dimers are expected to inhibit Mn diffusion and stabilize the films against secondary phase formation. Radial distribution function (RDF) analysis was therefore performed on the PLAP data and compared with RDFs generated from a random alloy. The RDF analysis confirmed that the Co distribution influenced the Mn distribution, but the resolution was not sufficient to detect the Co-Mn dimers.

10:20 AM Student

C2, Atomic Scale Gate Electrode Formed by a Charged Defect on GaAs(110): *Donghun Lee*¹; Jay Gupta¹; ¹Ohio State University

Electric-field control of spin-spin interactions at the atomic level is desirable for spintronics and spin-based quantum computation. Here we demonstrate the realization of an atomic-scale gate electrode formed by a single charged vacancy on the GaAs(110) surface [1]. A low temperature scanning tunneling microscope is used to position these vacancies with atomic precision. Tunneling spectroscopy suggests that the vacancies influence the in-gap resonance of Mn, Co and Zn acceptors via an interplay of band bending and Coulomb electrostatics. We find that this electrostatic field can be used to tune the magnetic coupling between pairs of Mn acceptors. This suggests an avenue for controlling spin-spin interactions on the atomic scale. [1] D. Lee and J.A. Gupta (in preparation).

10:40 AM

C3, Ordered Assemblies of Bimetallic Nanostructure Arrays Utilizing a Self-Assembled Disilicide Nanowire Template: *Talin Ayvazian*¹; Aniketa Shinde¹; Regina Ragan¹; ¹University of California-Irvine

Metal nanostructures have demonstrated extraordinary properties: the capacity for single molecule detection in plasmon resonance biosensors, chemical sensitivity and higher performance in catalytic processes than their bulk counterparts. One of the most significant challenges is the fabrication of nanostructure arrays with monodisperse size, shape and high density using low cost and high throughput technique. We will present a unique template-based fabrication process for dense ordered arrays (~1E11 cm⁻²) of bimetallic core-shell nanostructures with monodisperse size and shape, over large area (>1mm²), and having feature size and inter-particle spacing unattainable with electron beam lithography. A combination of scanning probe microscopy and density functional theory is used to understand the fabrication of these one dimensional structures. Noble metal deposited via physical vapor deposition on a nanowire template combined with reactive ion etching produce noble metal core-shell nanowire and nanoparticle arrays with mean feature size of approximately 8 nm. Rare earth disilicide nanostructures are used as self-assembled templates on Si(001). Scanning tunneling microscopy has shown that noble metal forms clusters on RESi₂ nanowire surfaces, and scanning electron microscopy backscattered images has shown that noble metal preferentially aggregates on the nanowire surfaces as opposed to the Si substrate. Noble metal coverage is used to select nanoparticle versus nanowire arrays after reactive ion etching. Experimental variables such as annealing time and temperature are explored to optimize selective aggregation of noble metal on nanowire surfaces.

The work functions of these structures can be tuned by varying size and shape of the disilicide template, as demonstrated by Kelvin Probe force microscopy. Au and Pt core-shell structures show work functions within the range of 3.7 – 4.0 eV, less than respective bulk work functions. Using the Vienna ab initio Simulation Package, theoretical modeling is combined with scanning probe microscopy for deeper insight of thermodynamics and kinetics driving template formation. We provide a platform to answer challenging issues regarding nucleation, nanowire-substrate interface, and morphology of RESi₂-x nanowires on Si(001). Synergistic STM characterization and ab initio calculations reveal that the stable adsorption geometries of the wetting layer lead to nanowire orientation perpendicular to Si dimer rows and thereby in unidirectional nanowire arrays on vicinal Si(001) surfaces. Formation energy calculations for narrow YSi₂ nanowires provide insight into the mechanisms that stabilize nanowire structures, such as internal strain relaxation and nanowire surface reconstruction. These studies will lead to achieving more control over the template assembly to further optimize the fabrication of bimetallic core-shell nanostructures.

11:00 AM Student

C4, Scanned Probe Characterization of Self-Assembled ErAs/GaAs Semimetal/Semiconductor Nanostructures Grown by Molecular-Beam Epitaxy: *Keun Woo Park*¹; Adam Crook¹; Hari Nair¹; Seth Bank¹; Edward Yu¹; ¹University of Texas at Austin

Rare-earth mononitride semimetallic nanoparticles embedded epitaxially in III-V compound semiconductors are of outstanding interest for application in a variety of solid-state devices including multijunction tandem solar cells, thermoelectric devices, and terahertz radiation sources. In the case of multijunction tandem solar cells, the semimetallic nanoparticles have been shown to yield dramatic increases in the electrical conductivity of tunnel junctions located between individual pn junction diodes in the tandem cell stack, with this improvement postulated to occur as a consequence of a two-step, rather than a single-step, electron tunneling process enabled by the electronic states in the nanoparticles. However, verification of this hypothesis and further optimization for solar cell and other applications will require an improved understanding of the spatial distribution of, electronic structure within, and electrical current transport through and in the vicinity of the nanoparticles and nanoparticle-semiconductor interfaces. We have used atomic force, scanning capacitance, and conductive atomic force microscopy to characterize nanoscale charge distributions and current transport in ErAs nanoparticle/GaAs heterostructures grown by molecular-beam epitaxy. Sample structures consisted of n-GaAs (001) substrates on which were deposited 200nm n+ GaAs ($n \sim 5 \times 10^{18} \text{cm}^{-3}$), an ErAs nanoparticle layer, and a 5-15nm p+-GaAs cap layer ($p \sim 5 \times 10^{19} \text{cm}^{-3}$). Scanned probe microscopy studies were performed at room temperature in ambient atmosphere using a Veeco Dimension 3100 Nanoscope IIIa microscope system. Scanning capacitance images obtained with dc sample bias voltages ranging from -1.0V to +2.0V reveal marked lateral variations in local carrier accumulation behavior in the sample, at typical lateral length scales of ~20-100nm. On the basis of analytical and numerical modeling, areas for which substantial modulation of near-surface electron and hole concentrations occurs are taken to correspond to regions below which no ErAs is present. Those areas for which little near-surface carrier modulation is observed are taken to correspond to regions above ErAs nanoparticles; in these areas, the capacitance signal over a broad range of bias voltages is dominated by carrier modulation within the nanoparticles rather than in the surrounding semiconductor material, leading to a weak dependence of capacitance on dc bias voltage and suppressed scanning capacitance signal contrast. The projected coverage of the GaAs interface region by ErAs nanoparticles implied by this interpretation is in good agreement with that expected from epitaxial growth conditions. Conductive atomic force microscopy measurements performed on these structures suggest that areas for which ErAs nanoparticles are present below the surface are generally, but not universally, associated with substantially increased electrical conductivity, consistent with the improvement in tunnel junction conductivity observed in electrical device measurements. These studies provide a foundation for detailed analysis of electronic structure and current transport behavior associated with ErAs nanoparticles embedded epitaxially in GaAs, and for understanding and optimizing their consequences for device behavior.

11:20 AM

C5, Late News

11:40 AM

C6, Late News

Session D: Narrow Bandgap Semiconductor Bulk Materials and Devices

Wednesday AM
June 23, 2010

Room: 131
Location: University of Notre Dame

Session Chairs: Partha Dutta, Rensselaer Polytechnic Institute; Shekhar Guha, Wright Patterson Air Force Base

10:00 AM Invited

D1, Review of Narrow Bandgap Semiconductor Based THz-Emitters:

*Ingrid Wilke*¹; Suranjana Sengupta¹; ¹Rensselaer Polytechnic Institute

An important method to generate THz-radiation pulses is the excitation of semiconductors by femtosecond (fs) near-infrared (nir) laser pulses. The interest in THz-waves, which are located between microwaves and the infrared in the electromagnetic spectrum, is rapidly growing. This development is driven by the availability of novel electronic and optical THz-radiation sources and THz-detectors, the exploration and exploitation of materials properties in the THz-frequency range and the success of real-world THz-system applications such as THz-imaging and THz-sensing. Narrow bandgap semiconductors are great sources of THz-radiation for more compact and lightweight time-domain THz-systems operated by fs lasers lasing at wavelengths between 1.0-1.6 microns. In order to optimize THz-emission from narrow bandgap semiconductors it is important to understand the THz-emission process as determined by semiconductor properties. For this purpose we have investigated THz-emission from GaSb, GaxIn1-xSb and GaxIn1-xAs for a wide range of compositions and range of electronic properties. The III-V ternary alloy semiconductor GaxIn1-xAs is a very interesting terahertz materials system because its bandgap can be tuned from 0.36–1.42eV by variation in the Ga mole fraction from x=0 to 1. The growth of binary and particularly ternary III-V semiconductors crystals is challenging since precise control of heat and mass transport in the high temperature melt during the crystal growth is necessary for obtaining high quality application worthy material. For our experiments, a hybrid vertical Bridgman and gradient freezing directional solidification process was employed for the growth of high quality GaSb, GaxIn1-xSb and GaxIn1-xAs crystals. We review our experiments on THz-emission from narrow bandgap semiconductors excited by fs nir laser pulses. The Ga1-xInxSb material system enables the study of the influence of carrier concentrations on the THz-emission process in narrow bandgap semiconductors. The study demonstrates the existence of a compromise between the positive effect of high electron temperature provided by narrow bandgap materials and the negative effect of high intrinsic carrier concentrations. The influence of the majority and minority carrier types and concentrations on THz-emission strength was investigated using GaSb:Te. By varying the majority and minority carrier type and carrier concentrations over three orders of magnitude the THz-emission mechanism in GaSb can be tuned from being dominated by the photo-Dember effect to being dominated by surface-field acceleration. Within each regime photo-Dember based THz-emission and surface-field acceleration based THz-emission are maximized under specific majority and minority carrier concentrations. Furthermore, we have investigated the relationship between electrical and structural properties of GaxIn1-xAs and THz-radiation emission. We demonstrate that primarily optical rectification and surface-field acceleration contribute to THz-emission from GaxIn1-xAs depending on the Ga mole fraction x. A semi-large aperture Ga0.69In0.31As:Fe THz antenna emitter has superior performance compared to conventional THz-emitters because of femtosecond carrier lifetimes, ultrafast mobilities and high electrical resistivity.

10:20 AM Student

D2, Electrical and Optical Studies of Melt Grown Optical Grade $\text{InAs}_{1-y}\text{P}_y$:

Jean Wei¹; Yung Kee Yeo²; Jacob Barnes¹; Leo Gonzalez²; Shekhar Guha³; Robert Hengehold²; Geeta Rajagopalan⁴; ¹General Dynamics IT; ²Air Force Institute of Technology; ³Air Force Research Laboratory; ⁴United Semiconductors LLC

Bulk grown ternary III-V semiconductors are promising candidates for optoelectronic and photonic applications. These applications require materials free from extended defects such as inclusions, precipitates and cracks that scatter light during its propagation through the bulk of sample. Growth of optical grade bulk crystals requires stringent control over the synthesis and growth conditions in order to avoid the optical defects. Bulk ternary $\text{InAs}_{1-y}\text{P}_y$ poly-crystals with diameter up to 50 mm were grown from pseudo-binary InP-InAs melt using the vertical Bridgman technique. The electrical and optical properties of these $\text{InAs}_{1-y}\text{P}_y$ ($y = 0$ to 0.7) were investigated as a function of alloy composition and sample temperature. Data from Hall effect, photoluminescence (PL), refractive-index, and optical transmission measurements as a function of composition and temperature will be presented along with the role of growth conditions on the optical transparency. As-grown undoped crystals have been found to exhibit n-type conductivity irrespective of the alloy composition. Though the bulk $\text{InAs}_{1-y}\text{P}_y$ substrates show high optical transmission up to long wavelengths as well as high carrier mobility, they exhibit random micro-scale compositional fluctuations across the substrate area. Future advancements in crystal growth are necessary to achieve spatially homogeneous alloy compositions to avoid the random light scattering regions.

10:40 AM Student

D3, Electrical and Optical Properties of Bulk Ternary $\text{In}_x\text{Ga}_{1-x}\text{As}$:

Jean Wei¹; Austin Berstrom²; Yung Kee Yeo²; Shekhar Guha³; Leo Gonzalez²; Robert Hengehold²; Geeta Rajagopalan⁴; ¹General Dynamics IT; ²Air Force Institute of Technology; ³Air Force Research Laboratory; ⁴United Semiconductors LLC

Advances in crystal growth techniques have allowed successful growth of good optical grade melt-grown bulk ternary $\text{In}_x\text{Ga}_{1-x}\text{As}$ crystals using the vertical Bridgman technique. These crystals are promising candidates for electro-optical and photonic applications at long wavelength ranges beyond the capability of today's epilayer semiconductor devices. In order to fully utilize these ternary alloys, the electrical and optical properties of the recent melt-grown bulk $\text{In}_x\text{Ga}_{1-x}\text{As}$ ($x = 0.75$ to 1) have been investigated as a function of temperature and indium mole fraction x through photoluminescence, Hall effect, and absorption spectroscopy measurements. Hall effect measurements revealed moderate n-type doping with carrier concentrations ranging from 1.5 to $9.6 \times 10^{16} \text{ cm}^{-3}$ at 10 to 15 K. Hall mobility increased with rising indium content, and mobility values at 15 K ranged from $1.5 \times 10^4 \text{ cm}^2/\text{V}\cdot\text{s}$ for $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$ to $3.5 \times 10^4 \text{ cm}^2/\text{V}\cdot\text{s}$ for InAs . Laser excitation power dependent PL measurements at 12 K and temperature dependent PL measurements at temperatures ranging from 12 to 140 K showed band-to-band, free-to-bound, and donor-acceptor pair transitions.

11:00 AM Student

D4, Optical and Thermal Properties of III-V Bulk Ternary $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ and $\text{In}_x\text{Ga}_{1-x}\text{As}$ Crystals:

Jean Wei¹; Shekhar Guha²; Leo Gonzalez²; Jacob Barnes¹; Yung Kee Yeo²; Geeta Rajagopalan⁴; ¹General Dynamics IT; ²Air Force Research Laboratory; ³Air Force Institute of Technology; ⁴United Semiconductors LLC

$\text{In}_x\text{Ga}_{1-x}\text{Sb}$ and $\text{In}_x\text{Ga}_{1-x}\text{As}$ are ternary semiconductor materials widely used in optical fiber communication, lasers, optical switches, and infrared optical detectors. Because of the crystal lattice constant mismatch, it has been difficult to grow uncracked thick $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ and $\text{In}_x\text{Ga}_{1-x}\text{As}$ layers on binary compounds. Therefore, previous studies were focused on thin film $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ and $\text{In}_x\text{Ga}_{1-x}\text{As}$ epitaxial layers, and thus most optical parameters of bulk $\text{In}_x\text{Ga}_{1-x}\text{As}$ and $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ crystals are unknown. Recent advances in crystal growth techniques have allowed successful growth of good melt-grown bulk ternary $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ and $\text{In}_x\text{Ga}_{1-x}\text{As}$ crystals using the vertical Bridgman technique. In this work, optical properties of $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ and $\text{In}_x\text{Ga}_{1-x}\text{As}$ bulk crystals have been investigated using Michelson and Fabry-Perot interferometers and Fourier transform infrared spectroscopy. The refractive index value, n , the thermo-optical coefficient, dn/dT , and absorption coefficient were measured as a function of wavelength, temperature, and indium mole fraction x , all of which are very important parameters in optoelectronic device applications.

11:20 AM

D5, Late News

11:40 AM

D6, Late News

Session E: Materials Integration: Wafer Bonding

Wednesday AM

June 23, 2010

Room: 138

Location: University of Notre Dame

Session Chairs: Cindy Colinge, Tyndall National Institute; Mark Goorsky, University of California, Los Angeles

10:00 AM Student

E1, Investigation of Physisorbed and Chemisorbed Sulfur Species for GaAs Wafer Bonding: Michael Jackson¹; Mark Goorsky¹; ¹UCLA Materials Science and Engineering

This study demonstrates that a vacuum passivation method that exposing III-V surfaces to sulfur vapor under UV illumination can be utilized for direct bonding and is useful to study the role of sulfur at the interface. The treatment of III-V surfaces with sulfide-containing solutions is known to improve the surface electronic properties for Schottky contacts and passivation of heterojunction bipolar transistors, due to replacement of surface oxide with a sulfur-containing layer. Various sulfide solution passivation methods have been reported for direct bonding including thiourea in NH_4OH , $(\text{NH}_4)_2\text{S}$ in aqueous and alcohol solutions, with the latter treatment shown to improve the conductivity of bonded p-GaAs/n-InP. The potential of using vacuum based sulfur passivation for wafer bonding have not been explored, so this study investigates the optimization to be performed to ensure smooth bondable surfaces are maintained. Evaporation of sulfur onto the GaAs surface is not self-limiting; thus the deposited layer contains a mixture of chemisorbed and physisorbed sulfur species. This physisorbed sulfur does not facilitate good adhesion between bonded wafers, causing bond failure and surface roughening during heat treatments at temperatures up to 400°C . This physisorbed sulfur is not readily removed using common solvents. therefore, a desorption process was employed to increase the ratio of chemisorbed sulfide to physisorbed sulfur. The wafers are annealed in vacuum to remove the physisorbed sulfur, which has a vapor pressure of 10^{-4} Torr between 60 - 80°C . Through monitoring the surface quality by AFM and subsequent bonding, a 5 minute dose of UV-sulfur at 60°C under 10^{-6} Torr vacuum, followed by a 5 minute vacuum desorption at 75°C removes the physisorbed sulfur to maintain a clean surface suitable for direct bonding. The chemisorbed sulfur remains after this step, as XPS taken at surface sensitive grazing angle confirms the presence of As-S (the presence of Ga-S cannot be as conclusively determined due to the small binding energy differences for $2p_{3/2}$ Ga-O, Ga-S, and Ga-As). XPS also shows that sulfur treated surfaces have a reduced As-O and Ga-O signal compared to surfaces etched in NH_4OH , which is essential for wafer bonding where high electrical conductivity is desired. Wafer bonding of the UV-S and S desorbed samples show excellent adhesion for GaAs/GaAs and InP/InP bonded pairs that result in bulk fracture strength after annealing at 400°C and 300°C respectively, with minimal compressive forces. It has been shown that sulfur may play a key role in facilitating III-V wafer bonding with mechanically strong interfaces with minimal oxide incorporation, and further study into the reaction and desorption of sulfur on III-V surface will aid in developing a low-cost efficient procedure for materials integration without high processing temperatures or large compressive forces.

10:20 AM Student

E2, AlGaAs/GaAs/GaN Wafer Fused HBTs with Ar Implanted Extrinsic Collectors: Zongyang Hu¹; Chuanxin Lian¹; Zhen Chen²; Yu-Chia Chang²; Huili(Grace) Xing¹; ¹University of Notre Dame; ²University of California, Santa Barbara

Heterojunction bipolar transistors based on AlGaAs/GaAs/GaN structures are promising for high frequency and high power applications thanks to the high

breakdown field in GaN collector and the low contact resistances to both n- and p-GaAs. Due to the large lattice mismatch between GaAs and GaN, we have explored these heterostructures using wafer bonding instead of epitaxial growth. Previously we reported the wafer fused HBTs with DC current gains as high as 20 and breakdown voltages of ~ 35V. We have also fabricated RF HBTs exhibiting a small signal cutoff frequency $f_T \sim 2.6$ GHz. Our experiments showed that one of the challenges to increase the speed of the wafer-fused HBT was to make ohmic contacts to a thinner GaAs base without shorting to the GaN collector. To this end, we have investigated insulating extrinsic collectors by using Ar ion implantation. Ar ion implantation was first performed in the extrinsic collector region on the GaN wafer, following an alignment marker etch into GaN. The inverted emitter/base AlGaAs/GaAs wafer and the GaN collector wafer were then brought together, followed by a thermal annealing at 550°C for 1 hr. The ion implanted region on GaN remained to be insulating after this high temperature annealing. We found that the annealing temperature had to be increased from 450°C to 550°C to ensure a high bonding yield (> 80 %) when employing the ion implanted extrinsic collector. A more careful examination revealed that a ridge (~ 0.5 nm high) formed between the ion-implanted region and the region protected by the mask, which we currently believe contributes to the necessary annealing temperature increase. To understand the effects of the ion-implantation, we first compared the p-GaAs/n-GaN base/collector diode and p-GaAs/implanted GaN/n-GaN base/insulator/collector structure. We found that the base/insulator/collector structure indeed showed much lower leakage current in both forward and reverse bias directions, as desired, as well as a more uniform breakdown voltage. HBTs with the Ar+ implanted extrinsic collector were demonstrated with a current gain of 2 - 3 and a breakdown voltage of ~ 55 V. These are very encouraging results. Future improvements in device performance are expected when the fabrication processes, especially the wafer surface cleaning, are further optimized.

10:40 AM Student

E3, Effect of Surface Activation for Ge-Si Integration Using Wafer Bonding: *Ki Yeol Byun*¹; Isabelle Ferain¹; Ran Yu¹; Cindy Colinge¹; ¹Tyndall National Institute

Germanium is a candidate to replace Si in the channel of future high performance p-channel metal-oxide semiconductor field effect transistors (MOSFET) device due to its better hole transport properties. Ge to Si direct wafer bonding methods have been studied for use in high-performance photo-detectors as well as high-quality epitaxial templates for GaAs growth. In this work, we propose an alternative method for the Ge-Si integration which has less defective interfaces with low thermal budget. Structural investigations show that successful low temperature Ge to Si wafer bonding can be achieved for heterogeneous integration. In the experiment, 4-inch <100> oriented p-type Ge (Ga doped, resistivity = 0.016 Ω·cm) were selected for bonding. Prior to bonding, the Ge and Si wafers were cleaned in an SCI-equivalent solution with ozone for Si and without ozone for Ge. Wafers were then loaded into AML AW04 aligner bonder and vacuum was applied. The wafers were then exposed for 10 minutes to either oxygen or nitrogen free radicals (chamber pressure was 1 mbar at 100 W) generated by a remote plasma ring. After exposure the wafers were bonded in-situ under a pressure of 1kN applied for 5 minutes at a chamber pressure of 10-5 mbar. The wafers were annealed in-situ at 100°C for 1 hour with an applied pressure of 500N in vacuum followed by an ex-situ anneal at 200°C for 24 hours in order to enhance bond strength. The same wafers were then annealed again at 300°C for 24 hours. The ramp-up rate was set to 0.5°C/min in both cases. After anneal Ge-Si bonded pairs remained intact due to a slow ramp-up rate. Structural analysis of buried interfaces was studied by SAM and HR-TEM. The formation of interface defects during low temperature anneal depends on the surface activation technique. Due to the remote plasma configuration, ions which escape the mesh ring do not strike the wafer surface at high velocity. The latter has been confirmed by AFM and HR-TEM analysis showing that there was no significant surface damage after radical exposure of bare Ge and Si wafers. Buried interfaces of bonded pairs were inspected using SAM after annealing at 200°C 24 hours. This low temperature process using surface activation is a way to achieve high quality interfaces without activation induced surface damage. Our structural analyses show that surface activated

wafer bonding process is very suitable for Ge-Si integration with low thermal budget and low defect density at bonded interfaces. Additional experiments are being performed to characterize thoroughly the chemical properties at bonded interfaces.

11:00 AM Student

E4, Strain, Annealing, and Exfoliation in Hydrogen Implanted GaN for Layer Transfer Applications: *Eric Padilla*¹; Anthony Pangan¹; Michael Jackson¹; Mark Goorsky¹; ¹University of California, Los Angeles

Transfer of GaN layers to alternate substrates is limited by the very few efforts in this area which address how different annealing conditions impact both the implant-induced strain as well as successful exfoliation. Understanding implant-induced strain evolution has led to successful exfoliation and layer transfer in zincblende III-V and Group IV semiconductors. In this study, we modeled the strain in as-implanted GaN substrates, studied how two distinct strain related regions changed differently with annealing, and developed a series of two-step annealing processes to relate the exfoliation of GaN layers with the changes in the strain profiles. Successful GaN exfoliation of 1 μm thickness was achieved – this is significantly thicker than has been reported elsewhere. 18mm x 18mm GaN wafers were implanted with a dose ranging from 0.5×10^{17} H⁺/cm² to 1.5×10^{17} H⁺/cm². All implants were conducted at 77 K and 200 keV. Analysis and modeling of the strain distribution in as-implanted GaN via triple axis diffraction scans showed that two distinct strain peaks were present – one near the surface and the second at the projected range. Such a double peak was not observed in the implant of standard III-V or Group IV materials. After annealing at temperatures from 150°C to 375°C for extended times (1-40 hours), the shallow strain peak was observed to shift toward the substrate, indicating a reduction in strain, whereas the strain in the peak from near the projected range decreased monotonically as the annealing temperatures increased to 300°C but showed a reversal, i.e., a reduction in the strain change such that annealing at 375°C resulted in no shift to the strain peak associated with the projected range strain. This result indicated that defects from the two regions interact at lower temperatures but not at the higher annealing temperatures and thus may produce different types of defect structures. These results were used to design a two stage annealing procedure in which hydrogen-related platelets nucleate at a lower temperature and subsequently grow and induce exfoliation after higher temperature annealing. Presented here are results from low temperature steps performed at either 150°C or 375°C for 20 hours followed by high temperature annealing (> 650°C). The 150°C first step combination produced a series of small (< 1 μm) blisters whereas the 375°C first step combination led to the production of several μm-sized exfoliated sections (with removal of 1 μm thick layers) as well as large (several μm) irregular-shaped blisters, indicating that the latter process is more suitable for layer transfer. Transmission electron microscopy, atomic force microscopy and Noamrski imaging were used in addition to the high resolution x-ray scattering and dynamical scattering models.

11:20 AM

E5, Optimization of Adhesive Wafer Bonding for Silicon: *Sue Holl*¹; Srinivasulu Korrapati¹; Cindy Colinge²; ¹CSUS; ²Tyndall National Institute

Optimization of bonding parameters to develop a low temperature adhesive wafer bonding process producing a defect free and relatively strong bond in pairs of 6 inch silicon wafers was studied. SU-8 was used as the intermediate adhesive. The Key Process Input Variables of soft bake temperature, UV exposure dose and bonding temperature were studied. Three different values were chosen for each process variable and the bonding process was repeated in random order for all possible combinations of process variables. The soft bake temperature and time combinations tested were 70°C for 60 seconds, 90°C for 30 seconds and 95°C for 300 seconds. UV exposure times of 5, 10 and 15 seconds at 10 mW/cm² were used to produce exposure energies of 50 mJ/cm², 100 mJ/cm² and 150 mJ/cm² respectively. Bonding temperatures of 90°C, 115°C and 140°C for 30 minutes were studied to optimize the curing process. The quality of the wafer bonds was determined by two Key Process Output Variables: the fraction of interfacial area in intimate contact, measured by void area, and the strength of the bond interaction, measured by fracture strength. Bond characterization, including bond interface imaging to detect defects and measure void area, and

tensile testing to calculate the fracture strength, was performed on all bonded pairs. The bonded wafers were scanned using a Sonoscan Scanning Acoustic Microscope (SAM) and C-Scan images were used to determine void area. The bonded wafers were diced into 5mm X 5mm test specimens and each was scanned using SAM to determine the bond area. Tensile testing was done on the diced test specimens from each bonded pair to calculate the fracture strength. A general linear statistical model was developed to perform analysis of variance to determine the impact of the process input variables on the process output variables. The bonding parameters soft bake temperature, UV exposure dose and bonding temperature were successfully optimized to develop an adhesive wafer bonding process for 6 inch silicon wafers that produces defect free, strong bonds using SU-8 as an intermediate adhesive layer. The optimum conditions are soft bake temperature of 90°C, UV exposure of 100 mJ/cm² and bonding temperature of 115°C. This work was supported by the Science Foundation Ireland grant 07/IN/1937: Low Temperature Wafer Bonding for Heterogeneous Integration.

11:40 AM

E6, Development of Surface Activation Based Nano-Bonding and Interconnect System: *Matiar Howlader*¹; *Tadatomo Suga*²; *Akira Yamauchi*³; ¹McMaster University; ²The University of Tokyo; ³Bondtech Co. Ltd.

A nano-bonding and interconnect system (NBIS) equipment has been developed for three dimensional integration of emerging electronic and biomedical systems at room temperature. This article reports the development of NBIS with some preliminary bonding results of semiconductors and metals. The NBIS accommodates specimens as big as 2-inch wafers. The NBIS consists of a load lock chamber and bonding chamber separated by a gate valve. The load lock chamber has six stage elevators to hold the specimens. An automated transfer rod is used to transfer the specimens from the load lock chamber to the bonding chamber. An ultra high vacuum (UHV) pressure of 10⁻⁷ Pa is maintained in the bonding chamber using a high efficient turbo molecular pump. The bonding chamber is equipped with a high precision alignment system and a bonding head. An electrostatic chuck is used to hold the top specimen. Two infrared (IR) cameras are equipped to detect the alignment marks of the substrate and chip. The piezo elements attached to the bonding head and the Z axis units attached to the piezo walking table are used to perform the parallel adjustment function of the top and bottom wafers. The top and bottom specimens are activated in the bonding chamber either by Argon (Ar) ion bombardments or Ar-fast atom beam (FAB). Two FAB sources are installed at 45 degree in the bonding chamber to activate the top and bottom wafers. A single Ar ion source installed in bonding chamber is used to activate the top and bottom specimens simultaneously. After the activation, the top and bottom specimens are finally aligned by using the bottom IR camera. The alignment includes automated parallel adjustment, position detection, and alignment systems. The piezo elements installed on the bonding head serve as actuators for the top parallel adjustment. The Z-axis units mounted on the piezo walking table serve as actuators for the bottom parallel adjustment. The parallelism of the top and bottom wafers is detected through the height displacement of parallelism detection points at three Z axis units by means of the lower IR camera and is automatically adjusted through the operation of the top and bottom actuators, respectively. An automated repetitive correction enables an alignment accuracy of less than 100 nm. After the alignment, the top wafer is brought down and contacted with bottom wafer. Preliminary bonding results of Si/Si, Si/Ge and Si/GaAs using NBIS show void free interface with bonding strength equivalent to bulk fracture strength of the wafers. Further research on three-dimensional integration for high-density interconnection will be presented. For this purpose, a number of 1 millions of 3 μm size Cu bumps over an area of 5x6 mm were bonded to achieve the daisy chain structure.

Session F: Silicon Carbide Devices

Wednesday AM
June 23, 2010

Room: 155
Location: University of Notre Dame

Session Chairs: Joshua Caldwell, Naval Research Lab; Michael Dudley, Suny-Stony Brook Univ

10:00 AM Invited

F1, Applications of SiC Power Devices – A Materials and Device Perspective: *Anant Agarwal*¹; ¹Cree, Inc

The recent surge in the demand for SiC Power Schottky diodes in commercial applications suggests that a number of key material and device issues pertaining to the defects, design, production, cost, reliability and applications issues with respect to the diodes have been successfully addressed by the SiC community, at large. The relatively low voltage SiC diodes (600 to 1700 V) are currently being used in Switch Mode Power Supplies and Power Converters for Solar Cells. The next big mass-market for SiC diodes will be in the Hybrid and Plug-In Automotive segment, provided the benefits of using the SiC diodes out-weigh the cost of the diodes. In this respect, it is important to see the overall impact on the system cost rather than simply concentrating on the component cost. In this paper, we will present the cost/benefit analysis of above mentioned applications and try to identify the critical issues that may be addressed in future to improve the cost/benefit ratio in favor of using SiC diodes. For applications requiring higher voltage Schottky diodes and/or PiN diodes, the recombination-induced Stacking Faults and their effects on reverse leakage currents as well as forward conduction are important issues that need to be addressed. In addition, doping and uniformity of life-time are critical issues. Furthermore, there are significant device design challenges to optimize the design for high voltage applications such as designing for high dv/dt, avalanche and surge ratings. There are multiple well known issues with SiC power MOSFETs and IGBTs such as low inversion layer mobility, low threshold voltage and oxide reliability. While a significant research focus is being directed on these issues, many significant process integration issues, which impact the cost of the product such as high temperature ion-implantation and activation, need to be addressed. The cost/benefit analysis of MOSFETs and IGBTs for applications in Converters for Solar Cells, Hybrid and Plug-In Automotive segment and Smart Grids will be presented.

10:40 AM

F2, Review of the Dominant Scattering Mechanisms in SiC MOS Devices: *Jody Fronheiser*¹; *Vinayak Tilak*¹; *Kevin Matocha*¹; *Greg Dunne*¹; ¹GE Global Research

Silicon Carbide (SiC) based power MOS devices are well suited for high efficiency, high power and high temperature electronics. To date, the poor quality of the SiO₂/SiC interface has limited device performance and is the key technical challenge delaying insertion into commercial applications. This highly defective interface leads to a high density of interface traps, low inversion layer mobility, and instability in threshold voltage by temperature and bias stress-induced instabilities. A reduction in the interface trap density and a subsequent increase in inversion layer mobility has been achieved using a post oxidation anneal in nitric oxide yielding mediocre mobilities of 20-30 cm²/Vs. Gates oxides grown in the presence of Sodium (Na) have shown a low density of near interface traps and have demonstrated the highest reported field effect mobility on (0001) 4H MOSFETs up to 150 cm²/Vs. Despite advances in oxidation techniques to improve the SiO₂/SiC interface device performance is still below material entitlement. In this article we review the scattering mechanisms most likely responsible for the reduced inversion layer mobility. The main scattering mechanisms: Coulomb scattering, surface roughness scattering, and phonon scattering are discussed for 4H and 6H polytypes in addition to Na contaminated oxides. Similar to Silicon, Coulomb scattering in SiC dominates at low surface electric fields due to interface trapped and positive fixed charge at or near the interface. However at high surface fields SiC does not follow the universal phonon behavior seen in Silicon. This characteristic behavior shows a monotonic

decrease in mobility with increasing surface electric field. Likewise the mobility decreases with increasing temperature. In SiC, Gated Hall measurements taken on 4H MOS devices show the mobility is unchanged to both higher surface fields and increased temperature over the ranges of 0.1 – 0.7 MV/cm and 300 – 425 K respectively. On the other hand, measurements on 6H devices showed a decrease in Hall mobility as a function of temperature and surface electric field suggesting phonon limited mobility for this polytype. Furthermore, phonon limited mobility calculations show a close agreement between simulated and measured Hall effect mobility for 6H while in 4H the measured mobility is ~10 – 25 times lower than expected, suggesting surface roughness scattering. This conclusion is supported by characteristics observed in oxides grown in the presence of Na. The measured inversion charge density as a function of gate voltage for nitrated oxides is roughly 50% of the ideal inversion charge as compared to the Na sample that is nearly ideal, indicating a lower density of interface traps. Although the mobility is high it does not approach phonon scattering entitlement. These results strongly indicate that the inversion layer mobility in 4H SiC is limited by surface roughness scattering at nominal gate voltages.

11:00 AM Student

F3, A Comparative Study of Thermal and Deposited Gate Oxides on 4H SiC: Sarah Haney¹; Veena Misra¹; Mark Johnson¹; Juan-Carlos Idrobo²; Anant Agarwal³; ¹NCSU; ²Oak Ridge National Labs; ³Cree

Conventional silicon carbide (SiC) MOSFET fabrication relies on thermal oxidation of the SiC for formation of the silicon dioxide (SiO₂) gate oxide. While this direct oxidation is advantageous from a fabrication standpoint, the resulting MOS devices have exhibited significant interface trap densities, D_{it}, which reduce effective inversion layer mobility by capturing free carriers as well as via enhanced scattering. More recent studies have further linked this low mobility to a transition region between the SiC and SiO₂, on the SiC side, formed during the thermal oxidation of the SiC.[1] This region has been attributed to increased carbon concentration produced by the thermal oxidation.[2] In this work, we have investigated the atomic layer deposition, ALD, of SiO₂ onto SiC compared to thermal oxidation of SiC. The absence of the carbon out diffusion and subsequent build-up due to thermal oxidation is anticipated to result in an interface free of transition regions when depositing SiO₂ onto SiC with ALD. Capacitors have been formed on 4H-SiC with the following oxide treatments: thermal oxidation at 1175°C, thermal oxidation at 1175°C followed by an nitric oxide, NO, anneal at 1175°C, and ALD of SiC at 150°C followed by an NO anneal at 1175°C. ALD of the SiO₂ was performed using 3-aminopropyltriethoxysilane (3-APTES), ozone and water. Deposition rates of approximately 0.67Å/cycle are recorded for the process. Thermal oxidation processes consisted of dry oxidation at 1175°C followed by an argon anneal at 1175°C and finally by a 950°C wet oxidation. Capacitance-voltage curves of the samples show improved characteristics for the ALD+NO and thermal+NO samples. While this is expected due to the nitridation of the oxide, the ALD +NO capacitors showed good initial results. A flat band voltage of approximately 0V was recorded as well as D_{it} (calculated from HF and LF C-V curves) in the 7.6E+11 range at 0.2eV from the conduction band edge. This is slightly less than D_{it} values from the thermal oxidation + NO sample which recorded D_{it} of 8.6E+11 at 0.2eV from the band edge. STEM analysis of the ALD+NO sample has been completed, including electron energy loss spectroscopy (EELS) and Z-contrast imaging. Z-contrast imaging showed an amorphous SiO₂ layer and an abrupt interface, with no indication of a transition region. This abrupt interface was also seen in the EELS data which shows no appreciable difference in Si/C ratios throughout the SiC. XPS of the ALD oxides was also performed. Since the effective inversion layer mobility is, most likely, determined by D_{it} as well as transport properties of the transition layer, it is expected that FETs made with the ALD +NO process (in progress) will yield better effective mobility.

11:20 AM Student

F4, Magnetic Resonance Studies of 4H SiC MOS Structures: Brad Bittel¹; P.M. Lenahan¹; J. Fronheiser²; A. Lelis³; ¹Penn State Univ.; ²GE Global Research; ³US Army Research Lab

SiC/SiO₂ interface/near interface defects limit device performance, contributing to low effective channel mobilities and can cause large threshold

voltage instabilities. We report on series of measurements utilizing conventional electron paramagnetic resonance (EPR) as well as two electrically detected magnetic resonance EDMR techniques, spin dependent recombination (SDR) and a relatively new technique spin dependent trap assisted tunneling (SDT), to overcome the limits of previous resonance studies on SiC. Last year we reported on conventional EPR measurements utilizing both 30% ¹³C enriched epi layers and structures with the naturally abundant 1.1% ¹³C epi layers. The ¹³C acts as a “marker” allowing some measure of the physical distribution of defects. We have extended this work to EDMR on fully processed MOSFETs with 30% ¹³C isotopic enrichment. These EDMR results strongly suggest that the defects observed are not amorphous carbon clusters or carbon vacancies, and are consistent with previous EDMR studies which suggest silicon vacancies or silicon vacancy related defects. [1-3] Utilizing EDMR measurements we observe gross changes in the spectrum due to different oxidation processes including sodium enhanced oxidation and two different deposited SiO₂ oxidation techniques. These different oxidation processes result in very different field effect mobility and EDMR spectrum. The EDMR spectrum amplitude scales inversely with mobility in all cases except for the sodium enhanced oxidation. The sodium enhanced spectrum also displays an additional center not present in the other oxidation processes. This result suggests that the increased mobility from the sodium oxidation processes is not due to a reduction in interface/near interface traps. Preliminary spin dependent trap assisted tunneling (SDT) measurements on SiC MOS capacitors show an SDT spectrum that is, within the limits of the measurement to date, essentially identical to the well known E’ defect spectrum. E’ defects are the dominant deep level defects in SiO₂ in Si based MOSFETs. [4] This is the first report of SDT in SiC MOS capacitors and the technique shows great promise in helping to unravel the performance limiting defects located in SiO₂ on SiC and other material systems. [5] [1] M. Dautrich et al., Appl. Phys. Lett. 89, 223502, (2006). [2] D. Meyer et al., Mat. Sci. Form. 483, pp. 593-596, (2005). [3] C. Cochrane et al., Mat. Sci. Form. 600-603, pp. 719-722, (2009). [4] P.M. Lenahan et al., J. Vac. Sci. Technol., B, 16, pp. 2134-2153, (1998).[5]J. T. Ryan, et al., Appl. Phys. Lett. 95, 103503 (2009).

11:40 AM

F5, Influence of Geometry on Silicon Carbide JBS Diodes Conduction: Maxime Berthou¹; ¹CNM

As Silicon Carbide production qualities and quantities increase, industrial High Voltage applications become real. Industrialization of Silicon Carbide Diodes requires a cost effective production and thus simplification of the fabrication process and increase in the production yield. Because of its unipolar conduction, schottky diode presents the advantage of low current recovery. However the elevated surface electric field makes its reliability very sensitive to it schottky metal imperfections. Moreover, the reverse current is due to tunneling through the schottky barrier and thus it is modulated by surface electric field and temperature. JBS Diodes have been invented in order to reduce surface electric field by pinching the channel under the schottky contact between P boxes. However the P/N junction conduction in direct polarization makes its current recovery more important and temperature dependant. JBS diodes with different sizes and a pure schottky diode have been simulated in direct polarization. The P boxes bipolar conduction has been virtually minimized by the adjunction of a resistance symbolizing the highly resistive ohmic contact. Moreover 1.2kV diodes with the same design parameters (12µm 5.25x1015cm-3) have been fabricated and characterized with Iak(Vak) up to 4V and down to -1500V. Diodes have been fabricated with a tungsten schottky contact, a P+ implantation to create field stopper and P boxes, a P- implantation for the JTE extension and a N+ implantation for the channel stopper. Direct characterization of devices have been conducted under probe with Kelvin measurement, pure schottky diodes exhibited a dynamic resistance around 5.8mOhm.cm2 an Ideality factor of 1.08, JBS1 with 8µm schottky width and 3µm wide P boxes exhibit dynamic resistance around 7mOhm.cm2, JBS2 is 6.2mOhm.cm2 with a Schottky width of 6µm and JBS3 exhibit 5.55mOhm.cm2 for a schottky width of 8µm. schottky diodes exhibit 100uA for a revert polarization of 1250V and JBS diodes exhibit a leaking current of 100uA at 1400V for JBS3, 1500V for JBS2 and 1600V for JBS1. Simulation predicts 3.6mOhm.cm2 for the Schottky, 3.86mOhm.cm2 for JBS3 and 4.3mOhm.cm2 for JBS1. One should consider that contact resistivity

and schottky barrier imperfection have not been considered in the simulation. However measurements have been performed under probes without real Kelvin contact on back side. Results from simulation and characterization show only unipolar conduction. Moreover, current density is not proportional to the schottky areas in each chip. However, simulation results show that the current flows under the P boxes. Which explain the modulation of the resistivity only by the area of conduction under the whole diode and not only the schottky area. Thus it is possible to optimize the P boxes geometry and size so that one can take advantage of the schottky direct properties and JBS reverse advantages.

Session G: Oxide Semiconductor Thin Film Transistors

Wednesday PM
June 23, 2010

Room: 102
Location: University of Notre Dame

Session Chairs: John Conley, Oregon State Univ; Tom Jackson, Penn State Univ

1:30 PM Student

G1, Temperature Dependent Measurements of ZnO TFTs: *Devin Mourey*¹; *Dalong Zhao*¹; *Thomas Jackson*¹; ¹Penn State University

PEALD ZnO transistors on glass and polyimide substrates have field-effect mobility $> 20 \text{ cm}^2/\text{V}\cdot\text{s}$, good bias-stress stability, and circuits with $< 10 \text{ ns}/\text{stage}$ propagation delay.[1] For high-performance TFTs, self-heating can result in high temperatures on low-cost, low-thermal conductivity substrates such as glass ($1.3 \text{ W}/\text{m}\cdot\text{K}$) and polyimide ($0.15 \text{ W}/\text{m}\cdot\text{K}$). To understand thermal effects we have measured devices from 10 K to 400 K. A plot of $\ln(\mu_e)$ versus $1/T$ shows that the field-effect mobility is weakly activated between 400 K and 100 K with activation energy of $\sim 10 \text{ meV}$. For comparison, in amorphous silicon the activation energy is often $> 150 \text{ meV}$ due to the large density of localized tail states.[2] For PEALD ZnO, as the temperature decreases below 100 K the activation energy decreases and as a result PEALD ZnO TFTs operate with mobility $> 1 \text{ cm}^2/\text{V}\cdot\text{s}$ even at temperatures $< 10 \text{ K}$. The temperature behavior can be well described using a percolation model assuming a Gaussian distribution of barriers above the conduction band edge. This model has previously been applied to temperature dependent Hall-effect measurements in doped indium-gallium-zinc oxide films. [3] By fitting temperature dependent behavior at constant $V_G - V_T$ we examine how the model barrier height changes with channel carrier accumulation. In our oxide TFTs, we find that the barrier height and standard deviation steady decrease from $\sim 50 \pm 20 \text{ meV}$ at $5 \times 10^{12}/\text{cm}^2$ to $\sim 7 \pm 6 \text{ meV}$ at $1.4 \times 10^{13}/\text{cm}^2$ and the temperature independent mobility prefactor increases from 12 to $22 \text{ cm}^2/\text{V}\cdot\text{s}$. This reduction of barrier height and distribution width provides a mechanism for the carrier concentration dependent mobility observed in nearly all oxide thin films and devices. In addition, at the highest accumulations the barrier height becomes very small which is consistent with the good performance of these devices even at very low temperature. We also find a fully reversible, nearly linear positive shift in threshold voltage with decreasing temperature from 300 K to 100 K with a charge coefficient of about $-4 \text{ nC}/\text{cm}^2\cdot\text{K}$. While the origin of this charge is not fully understood, ZnO films deposited by PEALD are highly textured (002) and may exhibit a pyroelectric charge with changes in temperature, although the threshold voltage shifts below 100 K are likely not related to pyroelectric charge. The temperature dependent characteristics of these TFTs demonstrate that PEALD ZnO does not contain a large concentration of deep subgap traps as often found in other low-deposition-temperature thin film systems. [1] D. A. Mourey, et. al., IEEE Trans. on Elec. Devices, 57, 530-534, 2009. [2] T. Tiedje, et. al., Physical Review Letters, 46, 1425, 1981. [3] T. Kamiya, et. al., J. Display Technol., 5, p. 462-467, 2009.

1:50 PM Student

G2, Flexible ZnO Temperature Sensors on Plastic Substrate: *Dalong Zhao*¹; *Devin Mourey*¹; *Thomas Jackson*¹; ¹Pennsylvania State University

We have previously demonstrated plasma enhanced atomic layer deposition (PEALD) ZnO thin film transistors (TFTs) and circuits on polyimide substrates at $200 \text{ }^\circ\text{C}$ with field-effect mobility $> 20 \text{ cm}^2/\text{Vs}$, excellent bias stress stability, and circuits with propagation delay $< 20 \text{ ns}/\text{stage}$ [1]. PEALD ZnO TFTs have a linearly decreasing threshold voltage with increasing temperature and we have explored the use of arrays of these devices as flexible, thin film temperature microsensors. Flexible temperature sensors have previously been reported based on platinum resistors with small dimensions $< 100 \times 100 \text{ }\mu\text{m}$ and with good temperature resolution of $\sim 2 \text{ }^\circ\text{C}$.[2] The flexible temperature sensors described here have comparable size, but provide improved sensitivity and lower current operation, as well as simple integration with additional TFTs for sensor select and isolation. In this work, ZnO TFT temperature sensors were fabricated on $25 \text{ }\mu\text{m}$ thick polyimide substrates using PEALD at $200 \text{ }^\circ\text{C}$ and a previously described TFT fabrication process [3]. Several designs of nine individual $100 \times 5 \text{ }\mu\text{m}$ ZnO pyroelectric TFTs were fabricated on 2 cm long and $500 \text{ }\mu\text{m}$ wide flexible probes and in some designs line select TFTs were also integrated. Devices on these polyimide substrates typically had field-effect mobility of $10 - 15 \text{ cm}^2/\text{Vs}$. The temperature dependence of typical flexible devices was measured from 20 to $70 \text{ }^\circ\text{C}$ and a reversible linear shift in threshold voltage was observed, with associated pyroelectric charge coefficient of $1.5 \text{ nC}/\text{cm}^2\cdot\text{K}$. When measured in the subthreshold regime at constant gate bias, a small change in threshold voltage results in a large change in conductance, and provides good temperature sensitivity. Devices were calibrated between $20 - 35 \text{ }^\circ\text{C}$ using a surface mounted thermocouple and a gate voltage of -3 V and constant drain current of 4 nA . Sensitivity depends on the bias conditions and in the subthreshold a maximum of $> 350 \text{ mV}/^\circ\text{C}$ is observed. This change is equivalent to an effective temperature coefficient of resistance of more than 10%. Using a more complex biasing approach it is possible to adjust the sensor sensitivity and dynamic range to suit various applications. These results demonstrate that high performance ZnO pyroelectric TFTs can be used for temperature sensing on flexible substrates and may provide opportunities in novel non-planar and integrated temperature arrays. [1] D. A. Mourey, D. A. Zhao, and T. N. Jackson, IEDM, paper 8.5, 2009. [2] Y. Moser and M. A. M. Gijs, J. of Microelectromechanical Systems, 16, 1349-1354, 2007. [3] D. A. Mourey, D. A. Zhao, J. Sun, and T. A. Jackson, IEEE Trans. Electron Devices, 57, 530-534, 2010.

2:10 PM Student

G3, Improvement of InGaZnO₄ TFT Device Performance on Glass and Paper Substrates: *Erica Douglas*¹; *Wantae Lim*¹; *Youngwoo Heo*²; *David Norton*¹; *Fan Ren*¹; *Stephen Pearton*¹; ¹University of Florida; ²Kyungpook National University

InGaZnO₄ thin film transistors (TFTs) show exceptional promise for use in the backplane of active matrix organic light emitting diodes (AMOLEDs) and liquid crystal displays (LCDs) [1-3]. This is due to their high electron mobility and exceptional surface smoothness. InGaZnO₄ can also be deposited by sputtering at room temperature. This allows for TFTs to be fabricated on a variety of substrates, including glass, plastics and even paper [4]. Stability for unpassivated and SiO_x passivated devices under bias were investigated. Little to no effect to the threshold voltage (V_{TH}) and subthreshold gate voltage swing was observed for gate bias at 5V. However, at voltages greater than 10V, both unpassivated and passivated devices showed positive V_{TH} and S shifts. The positive V_{TH} and S shifts after constant gate voltage stress (+20 V) for 1000 s were 1.8 V and 0.72 V decade⁻¹ for the unpassivated devices and 1 V and 0.42 V decade⁻¹ for the passivated devices, respectively. SiO_x passivation, though, significantly reduced the shift in TFT characteristics. Dual gate TFTs were fabricated on glass for OR logic operation. Compared to bottom-gate (BG), top-gate (TG) TFTs exhibited better device performance, with higher saturation mobility, drain current on-to-off ratio, lower threshold voltage, and subthreshold gate-voltage swing. This improved performance was mainly attributed to low process-induced damage or low parasitic capacitance between gate and source/drain and low parasitic resistance between channel and source/drain in top-

contact TFT configuration (coplanar type). These results demonstrated that DG InGaZnO₄ TFTs are effective in improving device performance. This paper also reports on the fabrication of IGZO TFTs on paper, and the effect of various planarization layers in order to improve device performance. As a water and solvent barrier layer, cyclotene (BCB 3022-35 from Dow Chemical) was spin-coated on the entire paper substrate. TFTs on the paper substrates exhibited device characteristics only slightly inferior to those obtained from devices on glass substrates. The uneven surface of the paper sheet led to relatively poor contact resistance between source-drain electrodes and channel layer. The ability to achieve InGaZnO TFTs on cyclotene-coated paper substrates demonstrates the enormous potential for applications such as low-cost and large area electronics.

2:30 PM

G4, Sputtering of ZnO Thin Films for TFT on Polyimide Substrates: Xiaotian Yang¹; Chieh-Jen Ku¹; Faraz Khan¹; Pavel Reyes¹; Chung Kuo¹; Yicheng Lu¹; ¹Rutgers University

ZnO thin film transistors (TFTs) have drawn great interest over the last five years. It appears likely to find use in flat panel displays, radio-frequency electronics, and low-cost large-area electronics, depending on the device performance using various growth methods such as MOCVD, ALD, PLD or Sputtering. We report on the fabrication of flexible sputtered ZnO-based TFTs, with field-effect mobility > 1.0 cm²/Vs suitable for use in low-cost large-area flexible electronics. A 100 μm thick polyimide substrate is used as the flexible substrate, and the correlation of sputtering conditions and ZnO electrical properties were investigated. Prior to all device processing, the substrates are pretreated at 300°C for 3 hours to improve thermal dimensional stability and are passivated with 300nm PECVD silicon dioxide. Then, a 100nm thick aluminum layer was evaporated on the substrate as the common-gate electrode and a 180nm thick silicon dioxide was deposited at 250°C by PECVD as the gate dielectric. To form the semiconducting layer, a 100nm thick ZnO was deposited using rf sputtering with the substrate held at 100°C. The ZnO film was patterned with photolithographic etching and Al or Ti was deposited for the source and drain contacts with lift-off metallization. Because the stoichiometric ratio of oxygen and zinc is strongly related with the defect-associated shallow doping, dominantly zinc vacancy (V_{Zn}) and oxygen vacancy (V_O), consequently, producing the n-type carriers, we use the ratio of oxygen to argon pressure during the sputtering (0:10 to 3.3:10) to control the ZnO composition. The electrical testing shows that device performance of ZnO TFTs on flexible substrates are much improved when a lower O₂ to Ar pressure ratio is used, particularly, the on-off current ratio increases by four orders of magnitude to 10⁶ and saturation mobility improved from less than 0.01 to 1.5 cm²/Vs. This indicates that the incorporation of oxygen in ZnO films is controlled by the oxygen to argon pressure, as well as the electron concentration and conductivity. Device modeling is conducted to simulate this effect. In addition, a thermal treatment after device fabrication significantly improves I-V characteristics and the gate dielectric quality, where samples were subjected to annealing at 250°C for 3 hours in nitrogen ambient. The leakage current through gate electrode and the off state current are repressed. However, an improvement or an alternative of gate dielectric is necessary to achieve higher performance and a proper yield in comparison with state of art results today.

2:50 PM Student

G5, Zinc-Tin-Oxide Thin-Film Transistors with Al₂O₃ and ZrO₂ Gate Dielectrics: Josh Triska¹; John Conley¹; Rick Presley¹; John Wager¹; ¹Oregon State University

Amorphous hydrogenated silicon (a-Si:H) is currently the dominant material for the thin-film transistor (TFT) backplanes used to drive liquid crystal displays, but it exhibits several drawbacks which limit its use in future display technologies. The drawbacks of a-Si:H include low electron mobility that is limited to ~1 cm²/V*s, lack of transparency, and well-known instabilities under bias stress and light exposure. Despite these instabilities, the use of silicon nitride as a gate dielectric has allowed for operation stable enough that a-Si:H has dominated the flat panel display market. However, the requirements for the current driver in OLED displays, where high mobility is needed and any shifts in threshold voltage (V_{th}) will affect pixel brightness, may limit the use of a-Si:

H for this application. A new class of amorphous oxide semiconductor (AOS) has recently been developed which exhibits high mobilities (>10cm²/V*s) and can be processed at low temperatures. Thin-film transistors with AOS channels are promising candidates for OLED displays and transparent applications. In particular, zinc-tin-oxide (ZTO) is a promising channel material due to its relatively high mobility of ~15 cm²/V*s at low processing temperatures and inexpensive base elements. In this work, TFTs with ZTO channels and ALD Al₂O₃ gate dielectrics are shown to exhibit good mobility and subthreshold slope, but exhibit positive V_{th} shifts under positive gate bias stressing for up to ~10⁵ seconds. The use of a thin PECVD SiO₂ capping layer to modify the channel/dielectric interface is shown to improve device stability. Initial TFTs fabricated using ALD ZrO₂ gate dielectrics (with TEMAZ and H₂O as ALD precursors) are found to exhibit performance similar to that of Al₂O₃ devices. An investigation of ZrO₂ device stability under positive gate bias stressing is underway and will be compared to TFTs with Al₂O₃ and SiO₂ gate dielectrics.

3:10 PM Break

3:30 PM Student

G6, Study of CV and Admittance Characteristics of ALD High-K Dielectric ZnO Capacitors: Jeffrey Siddiqui¹; Du Nguyen²; Jamie Phillips¹; Kevin Leedy³; Burhan Bayraktaroglu³; ¹University of Michigan; ²Michigan State University; ³Air Force Research Laboratory

ZnO Thin Film Transistors (TFTs) have attracted attention due to high carrier mobility in the material. Many possible applications including low cost and/or flexible electronics exist. Recent results on these devices include the demonstration of high-performance operation at microwave frequencies [1]. The incorporation of high-k dielectrics is expected to further improve device performance, but there are few reports of the detailed electronic characteristics of ZnO/high-k dielectric interfaces. In this work, the characteristics of ZnO heterojunctions with high-k Al₂O₃ and HfO₂ dielectrics deposited by atomic layer deposition will be presented with emphasis on capacitance-voltage and admittance spectroscopy characteristics of metal-dielectric-ZnO structures. Materials consist of high-k dielectric thin films including Al₂O₃ and HfO₂ deposited by atomic layer deposition with and without remote oxygen plasma and ZnO thin films deposited by pulsed laser deposition. Capacitor test structures are in the bottom gate configuration using Pt/Ti/SiO₂/Si substrates with top metal contacts of Ti/Pt for metal-dielectric-metal structures and Ti/Al/Au ohmic contacts to ZnO for metal-dielectric-ZnO structures. Capacitance-voltage and current-voltage characteristics were measured using a Keithley 4200 system with CVU module. The metal-dielectric-metal capacitors indicate that Al₂O₃ and HfO₂ have dielectric constants of approximately 10ε₀ and 20ε₀ and leakage currents of less than 2x10⁻⁹ and 2x10⁻⁷ A/cm², respectively. Both films have breakdown fields of approximately 3x10⁶ V/cm. Capacitance-voltage characteristics of metal-dielectric-ZnO structures show clear accumulation and depletion behavior with varying turn-on voltage of less than 1 V for Al₂O₃ dielectrics and more than 2 V for HfO₂ dielectrics. The higher threshold voltage observed for the HfO₂ dielectrics may be due in part to interfacial defects. Admittance spectroscopy measurements were also conducted on the samples to evaluate the interface charge concentration. Variations in turn-on voltage, interfacial charge concentration, and energetic dependence of interfacial charge will be presented for the various dielectric thin films and discussed in the context of ZnO TFT performance. [1] B. Bayraktaroglu, K. Leedy, R. Neidhard, "Microwave ZnO Thin Film Transistors," IEEE Elec. Dev. Lett., vol. 29, No. 9, Sep. 2008.

3:50 PM Student

G7, Transparent Rectifying Contacts - A New Concept for Transparent Electronics: Alexander Lajn¹; Heiko Frenzel¹; Holger von Wenckstern¹; Marius Grundmann¹; ¹Universität Leipzig

Transparent electronic in combination with transparent light emitters permit the fabrication of fully transparent displays. Thus, new designs involving higher information content, better ergonomics, lower power consumption and new aesthetic aspects are feasible; e.g. in car wind shields, windows, sun glasses, monitors or cell phones. We report on the fabrication of fully transparent diodes, field-effect transistors and inverters, based on a new concept employing transparent rectifying contacts (TRC) for transparent electronics. The TRC

consist of a combination of a reactively dc-sputtered Ag_xO or PtO_y layer and a transparent and highly conducting capping layer; the total thickness is only 10 nm. With that an average transmission of 70% and 60% in the visible spectral range was achieved for the complete device structure on a ZnO thin film with Ag_xO and PtO_y , respectively. The so formed Schottky-like diodes exhibit maximum effective barrier heights of 0.87 eV, ideality factors of 1.47 and rectification ratios of 5×10^6 , which are similar to their opaque counterparts [1]. Using such kind of contacts as gate contacts in transparent metal-semiconductor field-effect transistors (TMESFET), on/off-ratios of $\sim 10^6$ and channel mobilities of up to $11.9 \text{ cm}^2/\text{Vs}$, which are only slightly lower than for opaque MESFETs [2, 3], were achieved. With that, our devices meet the requirements for the use in transparent displays formulated by Wager [4]. Moreover the TMESFETs require small voltage sweeps of only 2.7 V for switching between on and off-state. This is due to the absence of a voltage drop at a gate insulator, as it occurs in metal-insulator-semiconductor-FETs. Furthermore, with 120 mV/dec, the subthreshold slope of the TMESFETs already approaches the thermodynamic limit of 60 mV/dec. These advantages of MESFET were successfully transferred to integrated inverters, which have a maximum gain of ~ 200 at a supply voltage of 4 V and a low uncertainty level of ~ 0.3 V. Their performance is superior among the transparent inverters reported so far (e.g. [5]) and clears the way to fully transparent logic integrated circuits. This work is supported by Deutsche Forschungsgemeinschaft within the framework of Sonderforschungsbereich 762 "Functionality of Oxidic Interfaces" and the Graduate School "Leipzig School of Natural Sciences - BuildMoNa" as well as the European Social Fund and Studienstiftung des deutschen Volkes. [1] A. Lajn, et al., J. Vac. Sci. Technol. B, 27, 1769 (2009); [2] H. Frenzel, et al., Appl. Phys. Lett., 92, 192108 (2008); [3] H. Frenzel, et al., Appl. Phys. Lett., 95, 153503 (2009); [4] J. F. Wager, Science, 300, 1245 (2003); [5] J. H. Na, et al., Appl. Phys. Lett., 93, 213505 (2008).

4:10 PM

G8, Transition from Hopping to Band-like Transport in Solution-Processed Amorphous Zinc Tin Oxide Thin-Film Transistors: *Chen-Guan Lee*¹; Brian Cobb¹; Ananth Dodabalapur¹; ¹University of Texas at Austin

Amorphous oxide semiconductors have attracted much attention because of their high mobility, stability in ambient air and easy processing by solution approaches. Band-like transport is possible for amorphous oxide semiconductors because of their large neighboring ns orbital overlapping, which is insensitive to distorted Metal-Oxide-Metal chemical bonds. In this study, we combine solution-processed zinc tin oxide (ZTO) together with solution-processed high-k dielectric, ZrO_2 , to study the nature of charge transport as a function of gate bias. A top-contact configuration is employed while the substrate and the gate electrode are glass and AuPd, respectively. The ZrO_2 precursor solution was spin-coated in a nitrogen box at 2000 rpm for 30 seconds and was kept in nitrogen box for one hour to evaporate the residual solvent (2-methoxyethanol). Then, the spin-coated film was annealed on a hot plate in air at 500°C for one hour. The deposition process of gate dielectric was repeated once to achieve a thickness of ~ 90 nm. The ZTO precursor solution (0.2 M of ZnCl_2 and SnCl_4 in acetonitrile) was spin coated in nitrogen box at 6000 rpm for 30 seconds and followed by a soft bake at 100°C for 30 minutes. The spin-coated film was annealed on a hot plate in air at 500°C for one hour. Al source/drain electrodes were patterned by shadow mask with an aspect ratio of 20 ($L=50 \mu\text{m}$). The capacitance value for this dual layer ZrO_2 dielectric is $\sim 250 \text{ nF/cm}^2$, the on/off ratio is $> 10^6$ and a saturation mobility of $16 \text{ cm}^2/\text{Vs}$ is obtained at $V_G=V_D=5\text{V}$ at room temperature. The mobility is carrier concentration dependent. Transfer curves with higher carrier concentration ($V_{DS}=10\text{V}$ and $V_G=0\sim 10\text{V}$) are compared at different temperatures ranging from 77K to 333K. When plotting mobilities vs. (V_G-V_{ON}), we can find that the mobility decreases with decreasing temperature at lower sheet carrier concentration ($V_G-V_{ON}<7\text{V}$), which suggests localized transport. In contrast, the mobility decreases with increasing temperature at higher sheet carrier concentration ($V_G-V_{ON}>7\text{V}$), which suggests band-like transport. The V_{ON} is the onset voltage, which corresponds to the voltage that the carrier concentration starts to accumulate with increasing gate voltage. The activation energies at different V_G-V_{ON} are calculated and show that the activation energies decrease with increasing sheet carrier concentration. These results are in accordance with Mott's mobility edge model - at lower sheet carrier concentration

(lower V_G-V_{ON}), the Fermi level is in the band tail states and the transport is likely dominated by multiple trap and release of electrons by relatively shallow traps. However, the Fermi level moves towards the band edge at higher sheet carrier concentration and the transport is band-like. Conductivities at different sheet carrier concentrations are extracted from the linear regime of the output characteristics ($V_D I_D$) and the result shows that the conductivity increases with raising temperature for all sheet carrier concentrations. At the highest sheet carrier concentrations, the conductivity values are slightly less than 100 (S/cm) , implying that the conductivity is still in insulator regime, although approaching the metallic limit.

4:30 PM Student

G9, A Comparative Study of the Effect of Heat Treatment on the Microstructure and Properties of Colloidal ITO Films and Cold-Sputtered ITO Films: *Salil Joshi*¹; Gregory Book¹; Rosario Gerhardt¹; ¹Georgia Institute of Technology

Indium Tin Oxide (ITO) is an important transparent conductor that finds widespread applications in displays and other optoelectronic technologies. Fabrication of circuits and coatings from colloidal ITO has the advantage of being less wasteful as compared to sputtering, and may be advantageous for use on flexible and complex-shaped substrates that cannot withstand high temperatures. This study deals with the comparison of the effect of processing treatment such as oxygen plasma and heat treatment, on colloidal ITO films and cold-sputtered ITO films. Colloidal, fully crystalline ITO nanoparticles were made by a non-aqueous synthesis technique starting from acetate precursors [1]. Films were fabricated on glass and quartz substrates. ITO coatings were also fabricated using RF sputtering on identical, non-heated substrates. The microstructural changes in the ITO films were characterized through AFM and SEM. The electrical and optical properties were characterized using impedance spectroscopy and UV-visible absorption spectroscopy. The ITO films were heat treated in an atmosphere of argon or commercial air at 150°C, 300°C, and 450°C. Heat treatment of cold-sputtered ITO films changed properties such as transmittance in the visible region, optical band gap and the electrical resistivity of the films. Heat treating in air was seen to increase the resistivity, while heat treating in argon was seen to decrease the resistivity. The as-cold sputtered ITO films are amorphous, and are brown in color. Their transmittance increased significantly on heating. These changes can be related to the onset of crystallization, and changes in the carrier concentration due to the changes in the oxygen stoichiometry with heat treatment. In contrast, the colloidal ITO films are fully transparent as coated, because the colloidal nanoparticles are fully crystalline. Heat treatment at 300°C in argon caused a reduction in the transmittance in the colloidal ITO film due to charring of the organics. The electrical properties of the spin-coated colloidal ITO films were also significantly modified by the presence of the non-conducting ligands. The electrical properties vary as a function of sintering and non-stoichiometry as the oxygen content is varied. The removal of the non-conducting ligands from the colloidal ITO by oxygen plasma prior to heat treatment should improve the electrical properties. The effect of oxygen plasma on the electrical and optical properties will also be presented. [1] C. J. Capozzi, I. N. Ivanov, S. Joshi, and R. A. Gerhardt, "The effect of the atmosphere on the optical properties of as-synthesized colloidal indium tin oxide", Nanotechnology, vol. 20, p. 145701, 2009.

4:50 PM

G10, Optimization of Dielectric Passivation of ZnO-Based Schottky Diodes: *Holger von Wenckstern*¹; Stefan Müller¹; Matthias Schmidt¹; Florian Schmidt¹; Marius Grundmann¹; ¹Universität Leipzig

Schottky barrier contacts on ZnO have been studied with renewed interest in recent years. They are used in, e.g., photodetectors, metal-semiconductor field-effect transistors and gas sensors but are also of high importance for electrical characterization of ZnO by space charge layer spectroscopy since ZnO pn-diodes are not available. The optimization of Schottky diode properties focused on surface preparation and the choice of the Schottky barrier material so far. Recently it was demonstrated that the rectifying properties of high-quality Schottky contacts may degrade under reduced pressure [1]. This is caused by vacuum-activated surface conduction strongly reducing the parallel resistance

R_p , and by that increasing the leakage current of the Schottky diodes [1]. On the one hand this presents a major drawback considering the usage of, e.g., ZnO UV photodetectors in outer space; on the other hand it is disadvantageous for electrical characterization techniques performed under cryogenic conditions such as deep level transient spectroscopy. In a proof of concept study we demonstrated that dielectric passivation of ZnO Schottky diodes suppresses the formation of the vacuum-activated surface conduction path [2]. In this contribution we report on different strategies used to optimize such dielectric passivation. We used ZnO thin films grown on 2 inch sapphire wafers by pulsed-laser deposition (PLD). The samples were cut into pieces. On some pieces we reactively sputtered planar Schottky contacts prior to dielectric passivation (approach B); for other pieces the passivation was deposited prior to the Schottky contacts (approach C). The electric properties are compared to non-passivated diodes (approach A). The masks needed to define the contacts and passivations were realized by standard photolithography. The dielectric passivation, either being CaHfO_3 or Al_2O_3 , was grown at room temperature by PLD. For each passivation at least 40 Schottky contacts were produced on one sample piece and are compared to diodes realized on another piece of the same wafer in order to obtain a significant set of data. For characterization we used current-voltage measurements; selected samples were investigated by thermal admittance spectroscopy, deep level transient spectroscopy and depth-resolved cathodoluminescence (CL). The results show that dielectric passivation increases the CL UV/VIS ratio for excitation close to the surface, it does not introduce additional defects and it suppresses the formation of a vacuum-activated surface conduction path. Further, the parallel resistance of Al_2O_3 -passivated diodes is in average higher than that of non- or CaHfO_3 -passivated diodes; the scatter of R_p is largest for non-passivated diodes. Our results show that it is favorable to realize the passivation prior to the Schottky contacts (approach C). [1]M. Allen *et al.*, IEEE Transaction on Electron Devices 56, 2160 (2009). [2]von Wenckstern *et al.*, J. Electron. Mater. available online, DOI: 10.1007/s11664-009-0974-1.

contacts (30 nm). The mobilities of undoped transistors (with a contact resistance of 0.66 k Ω -cm) range from 0.9 cm^2/Vs ($L = 10 \mu\text{m}$) to 2.2 cm^2/Vs ($L = 60 \mu\text{m}$). For contact-doped transistors (with a contact-resistance of 0.38 k Ω -cm) the mobilities are between 1.3 cm^2/Vs ($L = 10 \mu\text{m}$) and 2.3 cm^2/Vs ($L = 60 \mu\text{m}$). To fabricate top-contact DNTT TFTs with sub-micron channel length, we have expanded a process reported by Tsukagoshi *et al.* [APL 91, 113508, 2007]. A narrow suspended resist bridge is defined across the Al/AIOx/SAM gate stack by electron-beam lithography using a multi-layer resist process. The organic semiconductor is deposited underneath the bridge by two angled evaporations (45° and 135°). Finally the organic dopant and the Au source/drain contacts are evaporated at an angle of 90° , so that the resist bridge serves as a high-resolution shadow mask to define the channel length. The 150 nm long transistors have a mobility of 0.05 cm^2/Vs , an on/off current ratio of 10^6 and a transconductance of 0.4 S/m. In the undoped transistors a deviation from the ideal transistor behavior is observed for small drain-source voltages (Schottky contacts). In contrast, the contact-doped transistors have a reduced contact barrier and improved transistor behavior, especially at small drain-source voltages (ohmic contacts). In summary, we have shown an improvement of top-contact organic TFTs with a channel length from 100 nm to 60 μm by introducing a molecular dopant into the contact area.

1:50 PM Student

H2, Gate Dielectric Thickness Dependence of OTFT Performance: Yuanyuan Li¹; Devin Mourey¹; Dalong Zhao¹; Haoyu Li¹; Marsha Loth²; John Anthony²; Thomas Jackson¹; ¹Penn State University; ²University of Kentucky

Solution based organic semiconductors have been widely investigated for their potential in low cost flexible electronics. Organic thin film transistors (OTFTs) fabricated using spin casting of the p-type organic semiconductor 5,11-Bis(triethylsilylethynyl) anthradithiophene (diF-TES-ADT) have demonstrated mobility $> 1 \text{ cm}^2/\text{V}\cdot\text{s}$ and a contact-related microstructure for pentafluorobenzethiol treated electrodes on thermal SiO_2 . [1,2] For organic devices and circuits on transparent and flexible substrates, dielectric materials are needed which can be easily deposited at low temperature on glass and flexible substrates. Al_2O_3 can be deposited by plasma enhanced atomic layer deposition (PEALD) at 200°C [3] and has been used to fabricate high-performance ZnO TFTs. In this work we have fabricated OTFTs with thin Al_2O_3 dielectric layers. The OTFTs for this work used a simple structure with gold source and drain electrodes photolithographically defined on a dielectric layer on a heavily doped n-type silicon wafer. We fabricated devices on 32 nm and 60 nm PEALD Al_2O_3 and 210 nm thermal SiO_2 . PFBT was used to treat the Au electrodes provide the contact related microstructure, and HMDS was used to treat the dielectric layer. A 2.5 wt% solution of diF-TES-ADT chlorobenzene was spin coated on the substrates, and the expected contact-related microstructure was observed on all samples. diF-TES-ADT TFTs fabricated with 210 nm SiO_2 with 5 μm channel length had field-effect mobility of $\sim 0.7 \text{ cm}^2/\text{V}\cdot\text{s}$, threshold voltage of $\sim 15 \text{ V}$, and on current is larger than 10^{-4} A at $V_G = -20 \text{ V}$ and $V_D = -40 \text{ V}$. Similar OTFTs fabricated with 60 nm Al_2O_3 had field-effect mobility of $\sim 0.2 \text{ cm}^2/\text{V}\cdot\text{s}$, threshold voltage of $\sim 1 \text{ V}$, and on current of $\sim 5 \cdot 10^{-5} \text{ A}$ at $V_G = -10 \text{ V}$ and $V_D = -20 \text{ V}$. Similar OTFTs fabricated on 32 nm Al_2O_3 had field-effect mobility of $\sim 0.1 \text{ cm}^2/\text{V}\cdot\text{s}$, threshold voltage of $\sim 0.5 \text{ V}$ and on current of $\sim 4 \cdot 10^{-5} \text{ A}$ at $V_G = -10 \text{ V}$ and $V_D = -15 \text{ V}$. Plotting the OTFT current as a function of the gate electrical field, including correcting for apparent threshold voltage, also shows that the OTFT current decreases with decreasing gate dielectric thickness. Preliminary two dimensional modeling suggests this unexpected result can be explained by two-dimensional electric field effects at a Schottky barrier between the organic semiconductor and source and drain contacts. [1] S. K. Park, SPIE Conference Digest, 100 (2007). [2] D. J. Gundlach, *et al.* Nature Materials, 7(3), 216-221 (2008). [3] D. A. Mourey, *et al.* IEEE Trans. Electron Dev., 57, pp. 530-4 (2010).

Session H: Materials and Devices for Flexible Electronics

Wednesday PM
June 23, 2010

Room: 126
Location: University of Notre Dame

Session Chairs: Oana Jurchescu, Wake Forest University; Alberto Salleo, Stanford University

1:30 PM Student

H1, Molecular Contact Doping in Organic Thin-Film Transistors: Frederik Antel¹; Tobias Canzler²; Ansgar Werner²; Ute Zschieschang¹; Klaus Kern³; Hagen Klauk¹; ¹Max Planck Institute for Solid State Research, Stuttgart, Germany; ²Novald AG, Dresden, Germany; ³Ecole Polytechnique Fédérale de Lausanne, Switzerland

The drain current of organic thin-film transistors (TFTs) is often limited by the energy barrier at the interface between the semiconductor and the source/drain contacts. This energy barrier can be reduced by choosing a contact metal with a work function matching the frontier orbital energy of the semiconductor [JAP 96, 7312, 2004], by modifying the metal work function with a thin oxide layer [APL 92, 013301, 2008], or by introducing a self-assembled monolayer (SAM) with an appropriate dipole moment [JACS 128, 1788, 2006]. Here we show that the contact barrier in organic TFTs can also be reduced by introducing a thin layer of a strong molecular dopant at the semiconductor/contact interface. Our TFTs are based on the organic semiconductor dinaphtho-[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT). The dopant (NDP-9, provided by Novald AG) is a small organic molecule with a LUMO energy below the HOMO energy of DNTT, so electrons are transferred from the DNTT to the dopant, increasing the local density of excess holes in the DNTT near the contacts. Transistors with a channel length between 10 and 60 μm are fabricated using polyimide shadow masks and consist of Al gates (30 nm thick), an AlOx/SAM gate dielectric (5.7 nm), vacuum-deposited DNTT (30 nm), a thin dopant layer ($\sim 1 \text{ nm}$) and Au top

2:10 PM Student

H3, Arylene Diimide-Thiophene Semiconductors for n-Channel Field-Effect Transistors: *Rocio Ponce Ortiz*¹; Hui Huang¹; Antonio Facchetti¹; Tobin Marks¹; Yan Zheng²; Raul Blanco³; Helena Herrera³; Jose Segura³; ¹Northwestern University; ²Polyera Corporation; ³Complutense University of Madrid

Oligothiophenes and arylene-diimide derivatives are among the most used semiconductors in the fabrication of Organic Field Effect Transistors (OFETs). One intriguing strategy to improve the electrical behavior and/or achieve ambipolarity in organic semiconductors would be the combination of arylene diimide skeleton with thiophene rings within the same molecular structure. To this end, we have fabricated the first family of molecules consisting of β -naphthalenediimide and β -perylene-diimide oligothiophenes. This family of semiconductors allows us to analyze the interplay of three different effects on device response: (i) oligothiophene backbone catenation; (ii) interchanging naphthalenediimide by perylene-diimide substituents, and (iii) introducing a phenylene group in the oligothiophene backbone. Amphoteric redox behavior is recorded in these molecules by cyclic voltammetry, indicating the possibility of both electron extraction and injection from/into the conjugated p-system. Electrical measurements of vapor-deposited films measured in vacuum show electron field-effect mobilities as high as $0.35 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for semiconductor NDI-1T. Lower mobilities, on the order of $0.1\text{-}10\text{-}4 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, are recorded for the remainder of the semiconductors. The remarkable variation in electrical behavior within the semiconductor family is analyzed by means of electrochemistry experiments, X-ray diffraction and Atomic Force Microscopy (AFM), and is aided by theoretical Density Functional Theory (DFT) calculations. It will be shown that the differences in carrier mobilities can be basically explained on the basis of molecular packing and film microstructural trends. Indeed, the best device performance is measured for NDI-1T films, where calculations predict the molecule to be basically flat, thus promoting a closely packed crystalline film which is consistent with a well-resolved single phase XRD pattern. Furthermore, AFM reveals the presence of large and well-connected grains. On the contrary, the poor electrical performance of NDI-3T is likely connected with the poor film crystallinity (in fact no diffraction peaks are detected in XRD experiments) and with the presence of very small grains with increased grain boundaries. Solution-processed OFETs were also fabricated and their electrical performance compared with that of the corresponding vapor-deposited films. Field-effect mobilities of $0.042 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and $0.011 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ were obtained for PDI-1T and PDI-3T, respectively.

2:30 PM Student

H4, Advanced X-Ray Peak Shape Analysis of Organic Semiconductors: Insights into Crystalline Size, Strain, Intragrain Disorder and Implications for Charge Transport: *Jonathan Rivnay*¹; Michael Toney²; Alberto Salleo¹; ¹Stanford University; ²Stanford Synchrotron Radiation Lightsource

Structure-property relations have guided the development and processing of organic electronic materials and devices over the past two decades, leading to films with field effect mobilities around $1 \text{ cm}^2/\text{Vs}$. Such studies have focused on relative crystallinity, grain boundaries, film cracking, as well as molecular packing and orientation, in attempt to understand device-scale charge transport and performance. Grain size or grain boundary density is often cited as a reason for improved or degraded device performance. However, even the determination of grain size can be difficult: grain dimensions are often extracted from top-surface scanning probe techniques, rough estimation from X-ray peak widths or optical microscopy of crystalline domains with similar polarization extinction characteristics; the latter technique is especially common (and sometimes misleading) in small molecule films. Furthermore, the details of intra-grain order are important when considering charge transport within a grain. Deviations from ideal crystal packing will affect the crystalline transport and may shed light on the origins of intrinsic charge trapping in semi/polycrystalline organic materials. The study of disorder within crystalline grains is challenging due to the instability of organic materials under the prolonged electron beam exposure necessary for transmission electron microscopy. The small grain size, often on the order of tens of nanometers, further complicates characterization. One promising analysis technique is order-dependent Fourier X-ray peak shape analysis, developed by Warren and Averbach in the early 1950's. The Warren-Averbach (WA) analysis

allows one to simultaneously extract grain size, as well as parameters relating to non-uniform strain and statistical disorder (paracrystallinity) within the grain, both of which are the primary causes of higher-order peak broadening. To this end, we present a series of datasets with crystalline order both out-of-plane and in-plane and discuss the implementation of WA analysis as a tool to extract disorder parameters. Diffraction data is collected from a number of solution processable, high performance transistor and solar cell materials, including poly(2,5-bis(3-alkylthiophene-2-yl)thieno[3,2-*b*]thiophenes) (PBTTT), poly{[N,N'-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diy]-alt-5,5'-(2,2'-bithiophene)}, P(NDI2OD-T2), and triisopropylsilane (TIPS) pentacene. We discuss how parameters extracted from WA analysis may influence charge transport. Experiments are designed to elucidate the effects of annealing, alignment and blending on grain size, inter-grain disorder and strain for a number of crystallographic directions. In general, we find that polymer grains exhibit paracrystalline disorder on the order of 2-6%, and small molecules $<1\%$. We propose that this numerical representation of deviations from ideal crystalline order along with crystalline mobility (determined from device data fitting) and simulations is important for understanding crystalline transport and trapping in organic semiconductor thin films.

2:50 PM

H5, Probing Stress Effects in Single Crystal Organic Transistors by Scanning Kelvin Probe Microscopy: *Lucile Teague*¹; Oana Jurchescu²; Curt Richter³; Sankar Subramanian⁴; John Anthony⁴; Thomas Jackson⁵; David Gundlach³; James Kushmerick³; ¹Savannah River National Laboratory; ²Wake Forest University; ³National Institute of Standards and Technology; ⁴University of Kentucky; ⁵The Pennsylvania State University

To date, scanning Kelvin probe microscopy (SKPM) has been utilized to correlate the relationship between film structure and charge transport in a number of organic thin-film transistor (OTFT) devices. This technique provides a direct measurement of the intrinsic charge transport in the active organic as well as providing a detailed view of charge injection at the source and drain contacts. For the work presented here, SKPM was used to simultaneously probe the potential distribution in electrically biased single crystal difluoro bis(triethylsilyl)ethynyl anthradithiophene (diF-TESADT) organic thin film transistors. diF-TESADT is one of a number of organic materials being studied for potential use in organic based electronics,[1] and recent studies of diF-TESADT OTFTs have shown that charge mobilities on the order of $0.4 \text{ cm}^2/\text{V}\cdot\text{s}$ can be achieved for spun-cast devices,[2] while charge mobilities of $6 \text{ cm}^2/\text{V}\cdot\text{s}$ have been achieved for single crystal devices.[3] We will discuss our recent findings which suggest that significant changes in device performance can occur when the organic crystal is stressed over a timescale of a few minutes. More specifically, we will show SKPM data that reveal changes in potential drops at the contacts as a function of time. These results suggest that active organic material can become charged over a timescale of a few minutes, decreasing the current flow in the device from source to drain. [1] Gundlach, D. J.; Royer, J. E.; Park, S. K.; Subramanian, S.; Jurchescu, O. D.; Hamadani, B. H.; Moad, A. J.; Kline, R. J.; Teague, L. C.; Kirillov, O.; Richter, C. A.; Kushmerick, J. G.; Richter, L. J.; Parkin, S. R.; Jackson, T. N.; Anthony, J. E. *Nature Mater.* 2008, 7, 216-221. [2] Jurchescu, O. D.; Hamadani, B. H.; Xiong, H. D.; Park, S. K.; Subramanian, S.; Zimmerman, N. M.; Anthony, J. E.; Jackson, T. N.; Gundlach, D. J. *Appl. Phys. Lett.* 2008, 92, 132103. [3] Jurchescu, O. D.; Subramanian, S.; Kline, R. J.; Hudson, S. D.; Anthony, J. E.; Jackson, T. N.; Gundlach, D. J. *Chem. Mater.* 2008, 20, 6733-6737.

3:10 PM Break

3:30 PM Student

H6, Study on the Resistance of Stretchable Electrodes from Surface Morphology Aided by Computer Modeling: *Wenzhe Cao*¹; Patrick Goerni¹; Oliver Graudejus²; Joyelle Jones¹; Sigurd Wagner¹; ¹Princeton University; ²Arizona State University

This gold film electrodes on polydimethylsiloxane(PDMS) substrates can be reversibly stretched up to 80% without losing their electrical conductance. The resistance increases nearly linearly with increasing mechanical strain. With improving fabrication techniques the correlation between resistance and

strain has become more and more reproducible. Practical application requires a predictive model for this correlation, but no model exists that captures it. We describe a current percolation model that starts with the image analysis of scanning electron micrographs as the basis for the finite element modeling of the electrical potential distribution in the film. The samples are made by electron beam depositing 75nm thick gold films on PDMS and glass control substrates. The films on PDMS are patterned into 100 μ m wide and 5mm long electrodes. The baseline resistivity of the film is measured on the control sample. 15 μ m x 15 μ m fields of 8-bit grayscale SEM micrographs of the cracked gold film are processed for illumination correction and noise reduction and then converted to binary images—each pixel either representing conducting gold or non-conducting cracks. The potential distribution in the field is calculated from solving for each pixel Gauss's law under current conservation. From the calculated potential distribution we calculate the current density and the equivalent resistivity for each field selected from the SEM micrograph. We first studied unstrained electrodes. Their surface morphology was imaged by SEM and analyzed by the model we built. 15 μ m x 15 μ m large fields of the micrograph are analyzed and averaged, resulting in a resistivity of $(3.05 \pm 0.14) \times 10^{-5}$ Ohmcm. Applying this value to the 100 μ m wide and 5mm long electrode resulted in a simulated resistance of 211 Ohms, which agrees well with the measured value of 215 Ohms. Potential distribution maps of the 15 μ m x 15 μ m fields show that the potential drops are most pronounced (i.e., local resistances are highest) across cracks that are longer than 1 μ m, while they are small across smaller cracks. This indicates that cracks over 1 μ m in size contribute most to the excess resistance, above that of the gold film on glass. To study strained electrodes, samples were 1-D stretched to a precise strain value, and the resistance under strain was measured. Then the strained electrode was fixed by gluing it to a sample holder, and was imaged by SEM. As observed earlier, longer cracks formed with orientation mainly perpendicularly to the stretching direction. Locally some gold film also delaminates at the edge of cracks. Both crack lengthening (which is reversible) and film delamination contribute to the increase in resistance under strain. Applying the same approach as for the unstrained electrode above, the simulated resistance of an electrode strained by 15% is 834 Ohms, again agreeing well with the measured resistance of 860 Ohms. We will compare experiment with simulation, and describe our progress toward a predictive model.

3:50 PM Student

H7, Reverse Offset Roll Printing Using High Resolution Printing Plate for Electronic Application: *Nackbong Choi*¹; Shahruckh A. Khan¹; Jean Lavelle²; Jo Gallagher²; Mikhail Laksin³; Miltiadis Hatalis¹; ¹Lehigh University; ²CIRI, Northampton Community College; ³IdeOn

Printed electronics is an emerging technology for large area electronics such as display, RFID, and flexible electronics to reduce manufacturing cost and improve throughput [1]. This research is focused on high resolution offset roll printing method to replace the expensive photolithography process which requires several steps to pattern one layer. This printing technique can also be used to directly print the soluble conductors and soluble semiconductor layer for all printed thin-film transistors (TFTs). The technique, championed by LG Display, was successfully used to demonstrate a 15" display where all etch resists were printed [2]. However, the versatility of this printing process can be further demonstrated by direct printing of soluble metals and semiconductors on flexible platform. In this work, we study reverse offset printing process and propose new method to form a high resolution printing plate. Employing this process, our work will encompass printing of high resolution electrode and devices. At first, we have focused on reverse offset printing method with particular emphasis given to blanket materials, printing plates and ink modification for fine print features. Blankets of this type of printing system require low surface energy, high hardness, smooth surface roughness, and uniform thickness. Instead of soft PDMS, silicone elastomer (methyl vinyl silicone) with high hardness is applied as blanket material. Etching methods such as wet etch, laser ablation, and dry etch are evaluated to pattern glass and Si wafers for realizing high resolution printing plate. Among these techniques, deep RIE shows good results having etch-profiles with deep and steep angles. To increase surface energy of plate, molybdenum with high surface energy is deposited on the surface of Si plate to easily take ink off of blanket with low surface energy. To print etch mask for

replacement of photolithography, instead of developing new ink, commercial resist with 25% Novolak resin is modified by mixing high boiling point solvent to retard fast drying rate of ink. Finally very well defined patterns and line spaces of around 6 μ m are achieved using this process. Using this verified process, we are in process of building TFTs where etch-resist is printed and metal layers are substituted by silver nanoparticles to achieve the small printed channel length. [1] Vivek Subramanian et al, Proceedings of IEEE, VOL. 93, No. 7, July 2005. [2] Youn Gyoung Chang et al, Journal of the SID 17/4 (2009), 301-307 (2009).

4:10 PM Student

H8, A Novel Hybrid Electrical and Chemical Barrier Material for Flexible Electronics: *Lin Han*¹; Katherine Song¹; Sigurd Wagner¹; Prashant Mandlik²; ¹Princeton University; ²Universal Display Corporation

Mechanical flexibility is attractive for many electronic applications, including flat-panel displays, electronic paper, medical X-ray sensor arrays, and photovoltaic modules. Making electronics flexible adds a new dimension to the design and utilization of electronic materials. Among the most important materials that need to be made flexible is an optically clear insulator that can function as a gate dielectric and as an environmental permeation barrier. We introduced a new SiO₂-silicone hybrid material that meets these functions. The hybrid consists of ~90% SiO₂ and ~10% silicone polymer [1], which we deposit by plasma-enhanced chemical vapor deposition from a silicone monomer and excess oxygen on substrates at room temperature. Its electrical properties were evaluated on metal/~100 nm hybrid/p-type Si capacitors from measurements with an HP 4275A LCR meter and an HP 4155A parameter analyzer. The hybrid has a relative dielectric constant of 4.0, a leakage current of 0.08 μ A/cm² at an electrical field of 1 MV/cm, and a breakdown field of 8 MV/cm. To test its mechanical flexibility in a device, the hybrid was used the a gate dielectric in hydrogenated amorphous-silicon thin film transistors (a-Si: H TFTs). The TFTs can be bent to a tensile strain of up to 10 times of that of conventional a-Si:H / SiNx TFTs [2]. To test its permeability for atmospheric gases, we conducted accelerated tests at elevated temperature and humidity of hybrid encapsulated organic light-emitting diodes (OLEDs). At 65°C and 85% relative humidity, the water vapor transmission rate is at most 10⁻⁶ g/m²/day [3]. Because the hybrid is deposited at room temperature from inexpensive sources, is mechanically flexible and electrically and chemically impermeable, it is a suitable material for flexible electronics. We report the dielectric properties of the hybrid, the electrical and mechanical performance of a-Si:H TFTs with the hybrid gate dielectric, and the permeability of the hybrid used as encapsulation for OLEDs.

4:30 PM Student

H9, Heavily Doped ZnO Thin Films for Hybrid Inorganic Organic Devices: Budhi Singh¹; *Zaheer Khan*¹; Subhasis Ghosh¹; ¹Jawaharlal Nehru University, School of Physical Sciences

Organic solar cell (OSC) and organic light emitting diodes (OLEDs) require the use of conducting transparent electrode for allowing in and out of the active region of the devices. Transparent indium tin oxide (ITO) is the standard electrode used as anode in these devices. Besides cost, which is extremely critical for OSC, there are several problems. The most important is the control of the electrical and optical properties of ITO. Recently there is a serious search for alternate transparent electrode for organic devices. Moreover, there will be great demand of such material for future transparent electronics. In this case, in addition to transparent electrode, transparent n-type and p-type semiconductors will be required. In view of all these applications, heavily doped ZnO is being investigated with great interest. To be used as transparent conductive electrode in organic and transparent electronics, ZnO thin films have to be highly transparent in the visible and near infrared spectral range with a high electrical conductivity. Aluminum doped ZnO (AZO) could be suitable alternate to ITO for its low cost, low toxicity and excellent electrical and optical properties. We have grown 2% and 4% Al doped ZnO using RF sputtering on quartz substrate, with growth temperature varying from room temperature to 600°C. Sputtering targets were prepared by conventional solid-state reaction route. Commercially available ZnO (99.99%) and Al₂O₃ (99.99%) powders from Aldrich, were mixed in stoichiometric amount, grounded for 4hrs and finally sintered at 700°C for

10 hrs. Argon and oxygen mixture (6:4) were used as sputtering gases. All the grown films were polycrystalline, monophasic and highly c-axis oriented with no evidence of Aluminum impurity. Optical reflectance was more than 90% with not much variation in the optical bandgap. AFM and STM study showed that the film morphology was grainy and intergrain connectivity increased with increasing substrate temperature. The surface roughness was less than 2.3nm and the average grain size was ~ 145nm. It has been shown that desirable properties show nonmonotonic dependence on the growth temperature. Highest electron concentration of $3 \times 10^{19} \text{cm}^{-3}$ with more than 90% transparency has been obtained in samples grown at 500°C. A hybrid p-n junction diode was fabricated by using p type organic semiconductor zinc phthalocyanine (ZnPc) and n type AZO with rectification ratio of 10^3 . In this case bottom AZO layer grown at 500°C with resistivity of 60mΩcm is used as electrode and the subsequent AZO layer grown at room temperature with resistivity of 1.70Ωcm is used as active n-layer in the hybrid pn junction diode. The electrical properties of p-n junction improve remarkably with higher growth temperature of bottom AZO electrode.

4:50 PM

H10, Late News

Session I: Nanomagnetic and Spintronic Materials

Wednesday PM
June 23, 2010

Room: 129
Location: University of Notre Dame

Session Chairs: Xinyu Liu, University of Notre Dame; Roberto Myers, Ohio State University

1:30 PM

II, An Organic-Based Magnetic/Nonmagnetic Semiconductor as a Spin Polarized Carrier Source/Channel: Moving Toward Organic Spintronics: *Jung-Woo Yoo*¹; V. N. Prigodin¹; Chia-Yi Chen¹; H. W. Jiang²; C. W. Bark²; C. B. Eom²; A. J. Epstein¹; ¹The Ohio State University; ²University of Wisconsin

Recent years witnessed increasing research for exploiting carbon-based materials as a spin transporting channel, which introduces a new avenue for device integration and functionality [1]. Molecule/organic-based magnets, that allow chemical tuning of electronic and magnetic properties, are a promising new class of magnetic materials for future spintronics [2,3]. The advantages of using organic-based magnets as spin polarizers in spintronic applications include, chemical tunability, highly spin-polarized electronic nature [4], low temperature processing, optical control of magnetism and conductivity [5], etc. V(TCNE:tetracyanoethylene)_x ($x \sim 2$) is the earliest developed room temperature molecule-based magnet [6]. It has ferrimagnetic coupling between the spins in the TCNE π^* orbital and spins in $v^1 d(t_{2g})$ orbital with $T_c \sim 400$ K. This material also can be grown as a thin film via low-temperature (40 °C) chemical vapor deposition (CVD) [7]. Besides its robust room temperature magnetic ordering, the V(TCNE)_x has unique electronic structure, as a 'half-semiconductor' [4], i.e., fully spin polarized non-overlapping valence and conduction bands. The highly spin polarized electronic state was observed by magnetic circular dichroism [8]. In this talk, we present realization of an organic-based magnetic/non-magnetic semiconductor as an electron spin polarizer/spin transporting layer in the standard spintronic device geometry [1,9]. The application of organic small molecule films as the spin transporting layer has been studied recently. However, conceptual understanding of how the spins are injected into and transport through these organic semiconductor films was missing. With careful study on film thickness, temperature, and bias dependencies, significant differences between tunneling and giant magnetoresistance were resolved [1]. In addition, the room temperature organic-based magnet, V(TCNE)_x was successfully incorporated into the standard magnetic tunnel junction device [9]. Our results unambiguously demonstrates spin filtering of current passing through a V(TCNE)_x magnetic semiconductor film, with subsequent tunneling of the spin polarized carriers through a the hybrid rubrene/LAO barrier while effectively conserving spin polarization. A detailed discussion on temperature

dependence and applied bias dependence will be presented. [1] Yoo et al., Phys. Rev. B 80, 205207 (2009). [2] Miller and Epstein, Angew. Chem. Int. Ed. Engl. 33, 385 (1994). [3] Epstein, MRS Bull. 28, 492 (2003). [4] Prigodin et al., Adv. Mater. 14 1230 (2002). [5] Yoo et al., Phys. Rev. Lett. 97 247205 (2006). [6] Manriquez et al., Science 252, 1415 (1991). [7] Pokhodnya et al., Adv. Mater. 12, 410 (2000) [8] Kortright et al., Phys. Rev. Lett. 100, 257204 (2008). [9] Yoo et al., submitted for the publication.

1:50 PM Student

12, Effect of Perpendicular Magnetic Anisotropy on Emerging Magnetic Logic Devices: *Larkhoon Leem*¹; James Harris¹; ¹Stanford University

Perpendicular Magnetic Anisotropy (PMA) materials have attracted interest as a viable material for future scaling of magnetic/spintronic devices. Recently, a number of logic devices have been proposed in magnetics/spintronics domain as a replacement for highly scaled CMOS technology [1,2]. Although PMA materials have not been adopted in these emerging devices, it may be useful for the device scaling purposes. We investigate the applicability of PMA materials to emerging devices: Magnetic Quantum Cellular Automata (MQCA) and Magnetic Coupled Spin-Torque Devices (MCSTD), through micromagnetic simulations. First, in MQCAs, the moments in the nanomagnets are initialized to the hard axis and are required to remain in that state until signals arrive. Previous work [1] utilized crystalline anisotropy along the hard axis to enhance the biaxial anisotropy. We examine the possibility of using PMA materials to induce the biaxial anisotropy: elongated shape along the nanomagnet easy axis creates in-plane magnetization stable states while the metastable state is perpendicular to the nanomagnet surface. K1 values that are used in [1] along the hard-axis are induced in a perpendicular direction for comparison. From micromagnetic simulations [3], signal propagation was unsuccessful in PMA based MQCA: dual magnetic domains or magnetization vortices were observed to prevent signal propagations. Weak anti-ferromagnetic coupling among nanomagnets in PMA based MQCAs can be explained by small saturation magnetizations and lack of a boost for hard-axis stability as in [1], where all the moments from nanomagnets point along their hard axis. Finally, incrementally scaled down nanomagnet heights made the signal propagation successful in PMA based MQCAs. Secondly, PMA materials can lower the energy consumption of MCSTD due to their low switching current density. To examine the applicability of PMA, MCSTDs with circular and elliptical cross section are simulated. For the circular structures, the switching voltage modulation due to the fringing fields from the input MTJs [2], the key switching mechanism for MCSTDs, was not observed. This also results from the small saturation magnetization of PMA materials. In addition, the free layers are too thin to create enough anti-ferromagnetic coupling between the neighboring MTJs in the perpendicular direction. Next, elongated elliptical MTJs were used to induce in-plane stable states to utilize the stronger magnetic dipole coupling among MTJs. CoFe50 with a larger saturation magnetization was used as well. Now, switching voltage modulation is demonstrated as in the original MCSTD with a significant reduction in current densities. In conclusion, PMA materials can be integrated into emerging magnetic logic devices with additional considerations to compensate for the inherent small saturation magnetizations of PMA materials. [1] D. Carlton et al., Nano Letters, vol.8, no.12 (2008); [2] L. Leem, J. Harris, J. Appl. Phys. 105, 07D102 (2009); [3] M.J. Donahue, D.G. Porter, Interagency Report NISTIR 6376, NIST (1999).

2:10 PM Student

13, Observation of Antiferromagnetic Interlayer Exchange Coupling in a GaMnAs/GaAs:Be/GaMnAs Tri-Layer: *Jonathan Leiner*¹; Hakjoon Lee²; Taehee Yoo²; Sanghoon Lee²; Brian Kirby³; Xinyu Liu³; Jacek Furdyna¹; Margaret Dobrowolska¹; ¹University of Notre Dame; ²Korea University; ³National Institute of Standards and Technology

It has been long predicted theoretically that with the correct combination of layer thickness and carrier doping, antiferromagnetic interlayer exchange coupling should be sustainable between GaMnAs layers separated by non-magnetic spacer layers. However such AF coupling was not observed until very recently when Chung and co-workers used polarized neutron reflectometry (PNR) to unambiguously identify antiferromagnetic coupling in a superlattice structure of GaMnAs separated by GaAs:Be spacers [1]. This exciting finding

has spurred recent theoretical work by Szalowski and Balcerzak [2], who point out that the RKKY-like carrier mediated magnetic exchange should be different for a superlattice from that in a single trilayer of GaMnAs/GaAs:Be/GaMnAs, due to drastically different boundary conditions. In this vein, Ref. [2] suggests that the trilayer structure provides a simpler, more fundamental system for understanding the basic exchange mechanisms in GaMnAs. Thus, there is significant interest in understanding interlayer exchange coupling in the trilayer structure. A series of GaMnAs/GaAs:Be/GaMnAs trilayers with various thicknesses and dopings of the GaAs:Be spacers were fabricated by low-temperature molecular beam epitaxy in the hope of establishing conditions under which antiferromagnetic interlayer exchange coupling (IEC) between the GaMnAs layers can occur in such structures. After cooling a trilayer with a 5 nm spacer layer and $3 \times 10^{20} \text{ cm}^{-3}$ Be doping below the GaMnAs Curie temperature in zero field, we observe increased low-field magnetoresistance and suppressed low-field magnetization below 35 K – suggesting spontaneous antiparallel alignment of the GaMnAs layers. PNR measurements taken under similar conditions were used to directly measure the field dependent magnetic depth profile, and confirm robust antiferromagnetic coupling of the separated GaMnAs layers. This result is fundamentally interesting, as theoretical work suggests that a spacer layer as thick as 5 nm should be marginal at best for supporting any type of coupling in this system. Details of how coupling varies with spacer properties, and the role of crystalline anisotropy in our trilayer samples will be discussed. [1] J.-H. Chung, S. Chung, Sanghoon Lee, B. Kirby, J. Borchers, Y. Cho, X. Liu, and J. Furdyna, *Physical Review Letters* 101, 1-4 (2008). [2] K. Szalowski and T. Balcerzak, *Physical Review B* 79, 1-11 (2009).

2:30 PM

I4, Electrical Spin Injection in a Hybrid Organic/Inorganic Spin-Polarized Light Emitting Diode (Spin-LED): L. Fang¹; D. Duman¹; C.-Y. Chen¹; P. Truitt¹; A. Epstein¹; *Ezekiel Johnston-Halperin*¹; ¹Department of Physics, The Ohio State University

The success of solid state electronics over the past sixty years has both driven and been driven by an increasingly sophisticated understanding of the electronic properties condensed matter systems. The success of the emerging field of semiconductor spintronics will require a fundamental understanding of spin in condensed matter systems comparable to this understanding of charge transport. For example, the organic-based ferromagnet V[TCNE]x is a promising spintronic material due to its room temperature ferromagnetism, semiconducting bandstructure and predicted 100% spin polarization at the Fermi energy. Here we present a recent investigation into the use of V[TCNE]x as a spin injector in a hybrid organic/inorganic spin-light emitting diode (spin-LED) structure. In this study, we detect circular polarization of the electroluminescence (0.6% at 0.1 T and 60 K) that follows the magnetization curve of V[TCNE]x. Moreover we observe that the photoluminescence from a V[TCNE]x coated LED does not show significant magnetic circular dichroism, demonstrating the first successful transfer of spin from an organic-based material into an inorganic semiconductor.

2:50 PM

I5, Properties of MnAs/GaMnAs/MnAs Magnetic Multilayers and Their Application to High Temperature Vertical Spin Valves: *Debashish Basu*¹; Hyun Kum¹; Wei Guo¹; Pallab Bhattacharya¹; ¹University of Michigan

Epitaxially grown hybrid ferromagnet/semiconductor heterostructures are currently of interest due to their potential application in spintronics devices. Lateral spin valves and devices based on such spin valves have been demonstrated. More recently, vertical spin valves and transverse magnetoresistance devices (TMR) devices consisting of semiconductor/ferromagnet multilayers have been reported. However device operation has generally been restricted to very low temperatures. We have investigated the epitaxy and properties of MnAs/GaMnAs/MnAs magnetic multilayer heterostructures. Vertical spin valves/TMR devices using these heterostructures demonstrate large magnetoresistance upto T~200K. The magnetic multilayer heterostructure was grown by molecular beam epitaxy (MBE). A 35 nm layer of ferromagnetic MnAs was first grown on a GaAs substrate at 250°C. This layer was annealed in the presence of As flux at 350°C in order to reduce the surface roughness. Thin layers (1 nm each) of

GaAs and AlAs were deposited on the MnAs layer at 250°C. This was followed by a 8 nm layer of Ga_{0.1}Mn_{0.9}As and 1 nm layers of AlAs and GaAs layers respectively. The purpose of growing thin layers of AlAs/GaAs was to prevent the segregation of Mn atoms in the GaMnAs layer due to the proximity of the MnAs interface. The top 35 nm ferromagnetic MnAs layer was left un-annealed. X-ray diffraction and TEM measurements done on this multilayer film indicate a high degree of crystallinity of the MnAs contacts and absence of Mn clusters in the Ga_{0.1}Mn_{0.9}As sandwich layer. Vertical spin valves were fabricated with these multilayer heterostructures using standard micro-fabrication techniques. The current-voltage characteristics, measured both in the presence and absence of external magnetic field indicate dependence of the resistance of the device on the direction of magnetization of the ferromagnetic pads. Asymmetric control devices with no MnAs top layer, fabricated and characterized under the same conditions, show no such dependence. Distinct peaks were observed at ~350 Oe in the magnetoresistance (MR) measurements done on the vertical spin valves. The position of the peak closely matches the values obtained from separate magneto-optic Kerr effect measurements done on the polarizer and the analyzer pads. A peak MR value of 42 % was observed at 10K at a bias current of ~ 1 nA. MR values of >12 % was measured at temperatures above 150K. The MR vs temperature characteristic, which is non-linear, is influenced by the GaMnAs sandwich layer which is ferromagnetic at temperatures below 100 K and paramagnetic above this temperature. The enhancement of the MR values is attributed to this property of GaMnAs and also to its high crystallinity. Similar effects have been previously observed in all metallic spin valves with ferromagnetic sandwich layers. The characterization of this novel multilayer system will be presented and discussed. Work supported by NSF and ONR

3:10 PM Break

3:30 PM Student

I6, The Magneto-Optic Kerr Effect (MOKE) as a Measure of Strain-Induced Ferromagnetism in EuTiO₃ Grown by Molecular-Beam Epitaxy: *Lei Fang*¹; JuneHyuk Lee²; E. Vlahos³; X. Ke³; Y. W. Jung¹; L. Fitting Kourkoutis²; P. Ryan⁴; J. W. Freeland⁵; T. Heeg²; M. Roeckerath⁶; V. Goian⁷; M. Bernhagen⁸; R. Uecker⁸; C. Hammel¹; K. M. Rabe⁹; S. Kamba⁷; J. Schubert⁶; D. A. Muller²; C. J. Fennie²; V. Gopalan³; P. Schiffer³; D. Schlom²; *Ezekiel Johnston-Halperin*¹; ¹The Ohio State University; ²Cornell University; ³Penn State University; ⁴Ames Laboratory; ⁵Argonne National Laboratory; ⁶JARA-Fundamentals of Future Information Technologies, Research Centre; ⁷Na Slovance 2; ⁸Max-Born-Strasse 2; ⁹Rutgers University

Recently biaxial strain has been predicted to induce a multiferroic ground state in EuTiO₃ and change its normally paraelectric and antiferromagnetic ground state into a state that is simultaneously ferromagnetic and ferroelectric. This multiferroic state is predicted to be a strong ferromagnet and also a strong ferroelectric. To assess these predictions that would establish EuTiO₃ as the world's strongest ferromagnetic ferroelectric, epitaxial EuTiO₃ thin films are grown on (001) SrTiO₃, (001) (LaAlO₃)_{0.29}—(SrAl_{1/2}Ta_{1/2}O₃)_{0.71} (LSAT) and (110) DyScO₃ substrates by reactive molecular-beam epitaxy (MBE). Testing for ferromagnetism in the strained EuTiO₃ films is complicated by the large paramagnetic response of the DyScO₃ substrate. If a superconducting quantum interference device (SQUID) magnetometer is used under typical measurement magnetic fields, the paramagnetic response of the thick substrate swamps the signal from the strained EuTiO₃ film. For this reason magneto-optic Kerr effect (MOKE) is used to measure the magnetization of the strained films. Longitudinal continuous-wave (CW) MOKE geometry is used to measure the in-plane magnetization in a spectral window (690 nm to 750 nm) that is sensitive to the EuTiO₃ epilayer but not the DyScO₃ substrate. The MOKE response from the strained EuTiO₃ film exhibits a clear ferromagnetic hysteresis loop, with sharp switching to full saturation. The temperature dependence reveals a Curie temperature (TC) of 4.3 K. In comparison, unstrained EuTiO₃ films grown on SrTiO₃ and LSAT substrates were also measured and no ferromagnetic feature was observed for the control samples at all temperatures. Optical second harmonic generation (SHG) reveals that the unstrained EuTiO₃ films are not polar, as expected, but that the strained EuTiO₃/DyScO₃ passes through a phase transition at about 250 K to polar point group mm2, in agreement with theory,

and in this state domain switching by electric fields is observed. Our results thus establish that strain induces a strong multiferroic state in EuTiO_3 in agreement with predictions.

3:50 PM Student

17, Magnetic Circular Dichroism (MCD) Studies on GaMnAs: *Kritsanu Tivakornsasithorn*¹; Xinyu Liu¹; M. Berciu²; J. Furdyna¹; M. Dobrowolska¹; ¹University of Notre Dame; ²University of British Columbia

Current interest in spin-based electronics has generated a demand for materials in which magnetic properties occur simultaneously with a strong spin-dependent response of charge carriers. In this connection III-Mn-V ferromagnetic semiconductors – and GaMnAs in particular – continue to attract attention. Although there is general consensus that the ferromagnetic coupling between Mn spins in GaMnAs is mediated by holes contributed by Mn ions, the nature of the hole wavefunctions as well as their location (valence band vs. an impurity band located at about 110 meV above the top of the valence band) is one of the most controversial topics in this field. There are many theoretical models discussed in the literature, but as yet there is no conclusive experimental result that can definitively resolve this issue. In order to address this controversy, we studied MCD on a series of $\text{Ga}_{1-x}\text{Mn}_x\text{As}$ layers grown by MBE, with x ranging from 0.02 to 0.06. As was shown by Berciu et al [1], the MCD signal in GaMnAs arises primarily from a difference in the density of spin-up and spin-down states in the valence band brought about by the presence of the Mn impurity band. In particular, MCD spectra, for an as-grown and an annealed sample with $x = 0.06$, show the same general features as those observed on samples with Mn concentration ~ 0.01 reported in [1]. Specifically, the signal rises sharply in the vicinity of the energy gap and forms a very broad spectrum with two (as grown) or three (annealed sample) distinct peaks. The peaks correspond to the maximum contribution to the IB from the heavy hole (lower energy peak) and light hole (higher energy peak) bands. In the annealed sample the contribution from the $\Gamma 7$ band is also clearly visible. In contrast, the spectra taken on $\text{Ga}_{0.98}\text{Mn}_{0.02}\text{As}$ samples co-doped with Be reveal that the MCD signal disappears in the vicinity of the energy gap for samples with Be concentration higher than $1 \times 10^{20} \text{ cm}^{-3}$. In the case of Be-doped samples the Fermi level lies in the valence band, and consequently interband transitions at the band gap disappear. By contrast, the strong MCD signal observed at the band gap in undoped GaMnAs samples indicates a difference in the density of spin-up and spin-down states at the top of the valence band, and consequently points to the fact that the Fermi level must lie in the impurity band. [1] M. Berciu et al., Phys. Rev. Lett. 102, 247202 (2009).

4:10 PM Student

18, Magneto-Optical Spectroscopy of MOVPE Grown Ferromagnetic Semiconductors: Giti Khodaparast¹; *Mithun M. Bhowmick*¹; Matthew Frazier¹; Bruce Wessels²; Yasuhiro Matsuda³; ¹Virginia Tech; ²Northwestern University; ³University of Tokyo

The origin of ferromagnetism, which is apparently induced by free holes, has been an open question. Several models have been proposed; however, currently, there is no single theory that can provide an accurate prediction for T_c in different III-V DMSs for different carrier density regimes. The case for ferromagnetic semiconductor such as InMnAs, grown by MOVPE, is even more complex. Films with a carrier concentration of 10^{18} cm^{-3} have T_c of 330 K and the T_c is nearly independent of carrier concentration. Recently, the magnetoresistance of InMnAs/InAs p-n heterojunctions for magnetic fields of up to 18 T has been measured. At 300 K, giant magnetoresistance effects (2680 %) at 18 T were observed. A crucial factor in the design of any spin-sensitive device, on the basis of ferromagnetic semiconductor structures, is the electron-spin-relaxation time (T_1) which must be reasonably long to allow for transport and processing of the spins. Most of the understanding of the spin relaxation in narrow gap (III,Mn)V ferromagnetic structures has been on the basis of the two color magneto-optical Kerr (MOKE) time-domain spectroscopy. The approach in this work was focused on the time and polarization-resolved differential transmission (PRDT) as well as the MOKE measurements. In the PRDT measurements, optically-injected, spin-polarized electrons were created/probed close to the fundamental gap of the ferromagnetic films, using circularly polarized pulses in the mid-infrared.

The optical polarization is decaying exponentially with a decay constant related to the spin lifetime. Our PRDT observation suggested a spin relaxation of ~ 1 ps at 290 K in an InMnAs film with 4% Mn content, consistent with our MOKE measurements. The Carrier dynamics demonstrated several relaxation regimes, strongly influenced by the initial pumping wavelength. Lowering the samples temperature to 77 K didn't change the carrier and spin relaxations time significantly. In addition, to understand the nature of the carrier states in the valence band of the ferromagnetic samples, high magnetic field cyclotron resonance (CR) measurements at 290 K and 7 K were performed. CR is a direct and accurate method for determining the effective mass and therefore the energy dispersion of carriers. We compare our results with reported studies in MBE grown InMnAs and InMnSb. Supported by: NSF-DMR-0507866, AFOSR Young Investigator Program 06NE231, NSF-Career Award DMR-0846834, NSF DMR 0804479.

4:30 PM

19, Micromagnetic Simulation of Focused Ion Beam Patterned Cobalt-Platinum Multilayers: Xueming Ju¹; Stephanie Wartenburg¹; Markus Becherer¹; Doris Schmitt-Landsiedel¹; Paolo Lugli¹; Wolfgang Porod¹; *Gyorgy Csaba*²; ¹Technical University of Munich; ²University of Notre Dame

This work introduces a computational micromagnetic model of Focused Ion Beam (FIB) irradiated Co/Pt multilayers and shows how FIB irradiation can be used to engineer field-coupled devices made from Co/Pt multilayers. Irradiation locally changes the magnetic properties of Co/Pt layer stacks and can be used as a one-step tool for defining magnetic nanostructures. High irradiation dose renders the material non-magnetic or paramagnetic, while a lower dose locally reduces anisotropy, exchange and saturation magnetization. We implemented the model of inhomogeneously irradiated Co/Pt nanomagnets in a standard micromagnetic simulation software, OOMMF [1]. Using our simulation tool we show how FIB irradiation enables the definition of nucleation sites on a nanomagnet. This changes the reversal mode of the magnet – FIB-defined dots start switching from the side that received the highest dose [2]. Additionally, irradiation changes the strength of the magnetic dipole coupling between neighboring nanomagnets. For example, a nanomagnet partially irradiated at its left side shows a stronger coupling to its left neighbor than to the right one. We show how partial irradiation can be exploited in the design of field-coupled magnetic computing devices. In magnetic field coupling, information is represented by the magnetic orientation of single-domain nanomagnets and the magnetic signal is propagated and processed by their field-interactions [3]. Operation of the device requires precise control over the magnetic ordering. This is difficult to achieve [4], since field-interactions are reciprocal – the magnets jointly interact with all their neighbors so the direction of signal flow is not defined. Asymmetric irradiation of a nanomagnets can lead to non-reciprocal signal propagation and perfectly controlled, frustration-free ordering. Even large field-coupled structures can be demagnetized (put in their computational ground state) with a homogenous external field. We will show how shift registers and logic gates can be constructed from asymmetrically irradiated dots. [1] <http://math.nist.gov/oommf/>; [2] M. Becherer, J. Kiermaier, G. Csaba, J. Rezgani, C. Yilmaz, P. Osswald, P. Lugli, D. Schmitt-Landsiedel: Characterizing magnetic field-coupled computing devices by the Extraordinary Hall-effect presented at ESSDERC, Athens Sept 14-18 2000; [3] A. Imre, G. Csaba, L. Ji, A. Orlov, G. H. Bernstein, and W. Porod: Majority Logic Gate for Magnetic Quantum-Dot Cellular Automata Science 311 (5758), 205 (2006); [4] M. Becherer, G. Csaba, W. Porod, R. Emling, P. Lugli, D. Schmitt-Landsiedel; Magnetic Ordering of Focused-Ion-Beam Structured Cobalt-Platinum Dots for Field-Coupled Computing IEEE Transactions on Nanotechnology, vol.7, no.3, pp.316-320, May 2008.

4:50 PM Student

110, Growth and Characterization of In_{1-x}Mn_xSb Ferromagnetic Semiconductor Alloys Using Metal Organic Vapor Phase Epitaxy (MOVPE): *Caitlin Feeser*¹; John Peters¹; Nidhi Parashar¹; Bruce Wessels¹; ¹Northwestern University

Dilute (III,Mn)V magnetic semiconductors have attracted interest for their potential applications in semiconductor based spintronic devices. Currently,

a major challenge in developing these materials is attaining a high Curie temperature for room temperature operation. Recent success in synthesizing phase pure ferromagnetic InMnAs (T_c of 330 K) and InMnSb (T_c of 590 K) films using MOVPE demonstrates that narrow-gap semiconductors are suitable for these devices. In this study, we focus on the In_{1-x}Mn_xSb system and the role of Mn concentration in stabilizing the ferromagnetism. The InMnSb films are deposited on semi-insulating GaAs (100) substrate using atmospheric pressure metalorganic vapor phase epitaxy. Film growth involves trimethyl indium, trimethyl antimony, and bis(methylcyclopentadienyl) manganese precursors in a palladium-purified hydrogen carrier gas. Film growth has been studied between 400 and 440°C with Mn concentration ranging from x=0 to x=0.12, and over a range of III/V ratios. The typical film thickness ranges from 200 - 250 nm. For structural characterization, double crystal x-ray diffractometer (XRD) measurements with Cu-K/945:1 radiation are used to determine the phase diagram. For x < 0.05 the films are phase pure. For x > 0.05 the films show peaks at the (101) and (102) attributed to MnSb reflections. Mn concentration in the films is determined using the electron dispersive spectroscopy and has been found to increase with increasing growth temperature for a given III/V ratio. Crystallization of antimony to form surface droplets is observed in SEM for low III/V ratios. An increase in the surface roughness is observed with an increase in Mn content and subsequent formation of a second phase. Average root mean square surface roughness was 25 nm for these films. Field and temperature dependent magnetization were measured using a SQUID magnetometer. Irreversibility occurs when a ferromagnetic second phase is present. Both phase pure and two phase films show ferromagnetism with T_c greater than 350 K.

Session J: Thin Film Photovoltaics

Wednesday PM
June 23, 2010

Room: 131
Location: University of Notre Dame

Session Chairs: Steven Ringel, Ohio State University; Christian Wetzel, Rensselaer Polytechnic Institute

1:30 PM

J1, MBE Growth of Metamorphic InGaP on GaAs and GaP for Wide-Bandgap Photovoltaic Junctions: *John Simon*¹; *Stephanie Tomasulo*¹; *Paul Simmonds*¹; *Minjoo Lee*¹; ¹Yale University

Recently, multijunction solar cells have reached efficiencies of 41.1% by combining light absorbing materials with different lattice constants*. To achieve efficiencies above 50%, additional junctions may be needed, requiring the development of a wide bandgap (2-2.2eV) material to act as the top layer. In this work we demonstrate wide bandgap In_yGa_{1-y}P grown on GaAs_xP_{1-x} via solid source molecular beam epitaxy (SSMBE). Unoptimized GaAs_xP_{1-x} buffers grown on GaAs exhibited asymmetric strain relaxation, along with formation of faceted defects (FDs) ~200 nm deep in the [01-1] direction. The density of the FDs was greatly reduced by lowering the grading rate, implying that their formation is related to the strain relaxation process. Strain relaxation increased from ~55% to ~85% for the cap layer by increasing the growth temperature from 580 to 700°C. Surface RMS roughness as low as 2.45 nm across a 30x30 μm² area was measured by AFM on buffers graded to x=0.8 while a threading dislocation density (TDD) of 7.5x10⁵cm⁻² was measured by plan-view transmission electron microscopy (PVTEM). Graded buffers with x<0.7 had elevated FD densities that could not be reduced by slower grading. Cross-sectional TEM (XTEM) studies of the graded buffers showed evidence of dislocation pileups below the FDs, as well as formation of micro-cracks along [011] in buffers with x<0.7. Graded GaAs_xP_{1-x} buffers on GaP showed symmetric and nearly-complete strain relaxation of the top layers when grown at substrate temperatures of 580°C. Surface RMS roughness of ~3.56 nm across a 15x15 μm² area was measured on buffers graded to x~0.7. No FDs or micro-cracks were observed in these buffers. A TDD of 3.2-7.5x10⁶cm⁻² was obtained by PVTEM on GaAs_{0.68}P_{0.32}. In_{0.29}Ga_{0.71}P layers were subsequently grown at 460°C on GaAs_{0.6}P_{0.4} buffers on GaP. Intense room temperature photoluminescence at 2.16eV agrees with

the composition extracted from x-ray measurements, implying a lack of CuPt ordering. Similar surface morphology and roughness as the underlying buffer were obtained. A smooth, coherent interface between the GaAs_xP_{1-x} and In_yGa_{1-y}P was observed by XTEM, with no evidence of phase separation, while selected area diffraction along [011] confirmed the lack of CuPt-B ordering. The low TDD, lack of ordering, and lack of phase separation in these In_yGa_{1-y}P layers show that they are promising candidates for use as the top junction of a future multijunction cell. *Guter, et al, *Appl Phys Lett*, 94(22), 223504 (2009).

1:50 PM Student

J2, In_xGa_{1-x}As Metamorphic Buffer Layers for Lattice Mismatched Multi-Junction Solar Cells: *Peter Dudley*¹; *Jeremy Kirch*¹; *Toby Garrod*¹; *Sangho Kim*¹; *Luke Mawst*¹; *Katie Radavich*¹; *Steven Ruder*¹; *Thomas Kuech*¹; *Sabarni Palit*²; *Nam Jokerst*²; ¹University of Wisconsin; ²Duke University

In triple junction III-V solar cells, the use of a 0.95–1.05eV third junction is necessary to improve efficiency¹. A common method for growing low defect density 1.0eV bandgap GaInAs on GaAs is to employ a graded Metamorphic Buffer Layer (MBL), which confines the defects. Recently, Wanlass and colleagues at NREL2 have produced a 38.9% efficient (81 suns) inverted triple junction cell, in which a Ga_xIn_{1-x}P MBL is employed to allow for a 1.0eV In_{0.30}Ga_{0.70}As final junction³. While such devices are quite promising, the introduction of many dislocations into the solar cell structure, within the MBL, could impact the long-term reliability of the solar cell, especially when a concentrator is used. In addition, the surface morphology of MBL structures generally exhibit cross-hatching along the orthogonal (110) directions. We are investigating the MOVPE growth of In_xGa_{1-x}As MBL structures with a focus on techniques to improve the surface morphology, optimize the lattice-matching of layers grown on top of the MBL, and lift-off devices which incorporate said layers. One method to improve the surface roughness of the MBL is through the use of Chemical-Mechanical Polishing (CMP). Preliminary results of the CMP process, showing improved surface morphology, are indicated by optical microscope images of the In_xGa_{1-x}As MBL before and after CMP. Since accurate determination of the strain for layers grown on top of the MBL via off-axis XRD measurements has proven difficult, we adopted a trial and error method to optimize material quality. By varying the In composition of bulk InGaAs layers grown on top of the MBL and measuring the FWHM of the layer peak via XRD, we find that the compositional range giving the lowest FWHM can be considered to be lattice-matched. We also show the results of an initial investigation wherein we released an InGaAs QW PL structure from the underlying MBL and substrate, after bonding the thin film to a new carrier substrate. This structure utilized a sacrificial InGaP layer grown between the MBL and PL structure and selective chemical etching is utilized to lift-off the InGaAs QW test structure. Both the as-grown and lifted-off samples displayed room-temperature photoluminescence, though the QW PL intensity was reduced by a factor of four after lift-off. Future studies will focus on the growth and lift-off of 1eV solar cell devices from the MBL and implementation of the CMP process to improve surface morphology.

2:10 PM Student

J3, Quantum Dot n-i-p-i Photovoltaic Devices: *Michael Slocum*¹; *Steven Polly*¹; *Chelsea Plourde*¹; *Christopher Bailey*¹; *Jeremiah McNatt*²; *Sheila Bailey*²; *Cory Cress*³; *David Forbes*¹; *Seth Hubbard*¹; ¹Rochester Institute of Technology; ²NASA-Glenn Research Center; ³Naval Research Laboratory, Solid State Devices Branch

State of the art space solar cells utilize epitaxially grown III-V multijunction cells, with champion devices exceeding 30% conversion efficiency under 1-sun AM0 illumination. The ultimate efficiency is limited by the dual constraints of current matching in the series stack and lattice matching within the epitaxial structure to eliminate structural defects. This paper will focus on a novel approach of combining the benefits of an intermediate band solar cell (IBSC) with a device that depends almost exclusively on drift rather than diffusion currents to collect the carriers. A quantum dot nipi (QD-nipi) architecture consisting of repeating n-i-p-i epitaxial layers has been proposed to increase the radiation hardness of a device due to a decreased dependence upon diffusion length. This architecture will allow photo generated carriers to be rapidly

converted to majority carriers by drift, and conducted laterally through selective contacts positioned at opposite sides of etched V-groove channels in the device. Enhanced spectral conversion can occur by simultaneously adding QD to the stack. Demonstration of the QD-nipi configuration in a GaAs photovoltaic cell presents several challenges to device design and epitaxial growth. This paper will describe progress in addressing the two main challenges of creating selective ohmic contacts and determining the electric field profile. Results will be presented from epitaxial regrowth of GaAs within etched V-groove channels, concentrating on structural and electrical characteristics.

2:30 PM

J4, Characterization of a *p-i-n* Photovoltaic Cell Containing InAs/GaAs Quantum Dots: *Andrey Semichaevsky*¹; Harley Johnson¹; Simon Huang²; Rachel Goldman²; ¹UIUC; ²University of Michigan

Improved external quantum efficiencies (EQE) of quantum dot (QD) intermediate band solar cells (IBSC) have been predicted theoretically¹, and the increased photocurrent densities from solar cells with QD superlattices (SL) have also been demonstrated experimentally^{2,3}. Design of QD solar cells requires a thorough understanding of the mechanisms responsible for the absorption of photons below the bulk semiconductor bandgap as well as for the charge carrier dynamics. In the present work, the spectral efficiencies of a *p-i-n* structure with InAs quantum dots (QD) in an intrinsic GaAs barrier are characterized both theoretically and experimentally for potential applications in photovoltaic solar cells. All structures are grown on Zn-doped *p*-GaAs (001) substrates by molecular beam epitaxy, using solid Ga, Be, Si, Al, In, and As sources. An initial Be-doped *p*-GaAs, a GaAs buffer layer, and a GaAs layer are grown, followed by three layers of the InAs/GaAs QD SL (2.6 monolayers of InAs and 5 nm GaAs spacer). For the QD *p-i-n* structure, the final QD layer is capped with 500 nm semi-insulating GaAs. Layers of *n*-GaAs, Al_{0.3}Ga_{0.7}As, and heavily doped *n*-GaAs are added. For the control *p-i-n* cell, QD layers are replaced with a 15 nm GaAs layer. A finite-element model of the single-particle Schrödinger-Poisson equations⁴ in oblate spheroidal coordinate basis is used to predict the QD SL minibands and absorption spectra. The confinement potentials are found for the hydrostatic lattice mismatch strain⁴, and the QD dimensions come from AFM and XSTM characterization. Calculated SL absorption spectra are then used in a macroscopic carrier transport model (carrier photogeneration and recombination, drift and diffusion currents, quantum transport in the QD SL) to determine the photocurrent density. The photogeneration and recombination rates in our model are material composition- and spatially dependent. Increased photocurrent density due to the QD SL at wavelengths above the absorption edge of bulk GaAs (870 nm) is observed in both our theoretical and experimental results. Predicted and measured spectral EQEs are in reasonable agreement, although, if quantum transport effects in the QD SL (carrier trapping and Auger recombination in QDs) are not included, predicted photocurrent densities exceed those measured experimentally. The spectral efficiency of the QD solar cell is also found to be strongly affected by QD size and by the quantum mechanical coupling between SL layers. [1] A. Luque and A. Martí, Phys. Rev. Lett. 78, 5014 (1997). [2] A. Luque, A. Martí, C. Stanley, N. Lopez, L. Cuadra, D. Zhou, J. L. Pearson, and A. McKee, J. Appl. Phys. 96, 903 (2004). [3] C.O. McPheeters, C.J. Hill, S.H. Lim, D. Derkacs, D.Z. Ting, and E.T. Yu, Journal of Applied Physics 106, 056101 (2009). [4] J.H. Davies, The Physics of Low-dimensional Semiconductors: an Introduction (Cambridge University Press, 1998), 438 pp.

2:50 PM

J5, MBE Growth of Lattice-Matched 6.1Å II-VI on GaSb Substrates: *Xinyu Liu*¹; D. Ding²; S. Wang²; S.-N. Wu²; X. Zhang²; J. Fan²; J.-J. Liu²; X. Lu²; S. Johnson²; D. Smith²; J. Furdyna¹; Y.-H. Zhang²; ¹University of Notre Dame; ²Arizona State University

Monolithic integration of lattice-matched II-VI (MgZnCd)(SeTe) and III-V (AlGaIn)(AsSb) semiconductors on 6.1 Å substrates such as GaSb and InAs provides a novel approach for ultra-high efficiency multijunction (MJ) solar cells. These materials have direct bandgaps, covering the entire solar spectrum from 3.0 eV to 0.4 eV. The simulation of a practical four-junction solar cell based on the constituent II-VI materials show that the achievable energy conversion efficiency is 40% under 1 sun and 47% under 1000 suns. It is shown

that high quality II-VI materials such as undoped ZnTe and ZnCdTe grown on GaSb substrates can be achieved. Excellent material structural, interfacial, and optical properties are revealed using post-growth characterizations including X-ray diffraction (XRD), transmission electron microscopy (TEM), and photoluminescence (PL). Moreover, we have extensively investigated short-period superlattices (SSLs) of CdSe and CdTe digital alloys grown using ZnTe buffer layers on GaSb or InAs substrates. High-resolution transmission electron micrographs showed that the CdSe-CdTe SSL had very high quality for approximately 25–50 periods closest to the substrate but that considerable stacking faults and microtwins were visible in layers near the top surface of the sample. In addition, we also successfully fabricated single-junction II-VI semiconductor heterostructure solar cells consisting of *n*-type CdSe and *p*-type ZnTe grown on GaSb substrates. The current-voltage measurements reveal expected diode-like rectifying characteristics with considerable photo current and strong photovoltaic effects under light illumination, indicating that the idea of using monolithic integration of lattice-matched II-VI and III-V semiconductors on GaSb is indeed very promising for ultra-high efficiency multijunction solar cells. It is important to note that the interfaces between II-VI and III-V materials have some very interesting properties that are yet not been thoroughly investigated. Since the constituent elements of the II-VI and III-V materials have been proven to be dopants for each other, novel devices such as tunnel junctions could be invented by taking advantage of well-controlled interdiffusion of different elements across the interfaces to create heavily doped regions near the interface. Moreover, the type-II band edge alignment between certain II-VI and III-V materials may further help to improve the performance of tunnel junctions. This paper reports our recent study of a set of carefully designed ZnTe/GaSb samples with various interface growth conditions and the re-growth of GaSb epilayers on ZnTe buffer layers. A typical sample structure of the latter consists of a 300 nm GaSb grown on ZnTe buffer layer with various thicknesses. The impact of ZnTe buffer layer thickness on the morphological and structural properties of the top GaSb epilayers has been investigated. Two-dimensional growth of GaSb epilayers is quickly obtained after the deposition of 1–2 nm GaSb on Zn-terminated surface. XRD and HRTEM measurements of these samples will be reported at the conference.

3:10 PM Break

3:30 PM

J6, ZnO/ZnTeO/ZnTe Heterojunctions for Intermediate State Solar Cells: *Weiming Wang*¹; Jamie Phillips¹; ¹The University of Michigan

A single junction solar cell with intermediate electronic states can extend the absorption spectrum by a multi-photon process without sacrificing the open-circuit voltage, where conversion efficiency as high as a triple junction cell may be possible [1]. ZnTeO has been used to demonstrate intermediate state/band solar cells using OTe substitutional impurities with resulting intermediate states at approximately 0.4eV-0.7eV below the conduction band edge and optical absorption coefficient of approximately 10⁴cm⁻¹[2]. Initially, ZnTeO solar cell devices have been implemented in a *p*-ZnTe/ZnTeO/*n*-GaAs structure since it is difficult to achieve *n*-type ZnTe. Extended optical response at longer wavelength and sub-bandgap photocurrent response have demonstrated absorption via the multi-photon process [3]. However, the device performance is severely limited by non-ideal material properties and parasitic device parameters including high dislocation density due to the ZnTe/GaAs lattice mismatch and cross doping at the ZnTe/GaAs II-VI/III-V electrical junction. In this work, *n*-ZnO is proposed as an alternative heterojunction material for ZnTeO-based solar cells. While ZnO appears to be an attractive candidate due to its potential role as a wide-bandgap window layer with low resistivity and chemical compatibility with ZnTeO, there are challenges associated with the differing crystal structure of ZnO (wurtzite) and ZnTe (zincblend). The growth, structural properties, and electrical characteristics of ZnO/ZnTe heterojunctions will be presented. Improved diode ideality factor is observed for the ZnO/ZnTe diodes (*n*<2) in comparison to ZnTe/GaAs (*n*>3). However, reverse saturation current for these devices remains high, likely due to the differing crystal structures. In order to improve these characteristics, intermediate *n*-ZnSe (zincblend) buffer layers have been incorporated to reduce leakage current and improve photovoltaic

response for diodes with ZnTe-based absorber layers. [1]A. Luque, A. Marti, "Increasing the Efficiency of Ideal Solar Cells by Photon Induced Transitions at Intermediate Levels" *Phys. Rev. Lett.* 78, 5014 (1997); [2] W. Wang, W. Bowen, S. Spanninga, S. Lin and J. Phillips, "Optical characteristics of ZnTeO thin films synthesized by pulsed laser deposition and molecular beam epitaxy", *Journal of Electrical Material*, v 38, n 1, p 119, January 2009; [3] W. Wang, A. Lin, J. Phillips, "Intermediate band photovoltaic solar cell based on ZnTeO", *Applied Physics Letter*, v. 95, 011103 July 2009.

3:50 PM Student

J7, Copper Zinc Tin Sulfide Solar Cell Development by RF Sputtering from Binary Targets: *Jeffrey Johnson¹; Ashish Bhatia¹; Haritha Nukala¹; Win Maw Hlaing Oo¹; Liz Lund¹; Mike Scarpulla¹; Loren Reith¹; ¹University of Utah*

Here we report on our research on the deposition and characterization of Cu₂ZnSnS₄ (CZTS) thin films by RF sputtering from a single CZTS target and by co-sputtering from multiple binary targets on Mo-coated glass. Grain size versus substrate versus temperature was evaluated by XRD, EBSD and AFM. Attempts to detect and identify defect levels via electrical impedance measurements and photoacoustic measurements will be discussed as well as optical transmission, resistivity and Hall effect and photoconductivity. To evaluate the electrical characteristics using the follow full cell stack molybdenum back contact, CZTS absorber layer, CdS/ZnS window layer and ZnO:Al buffer layer to measure IV curves from various light and dark condition.

4:10 PM Student

J8, Chemical Vapor Deposition of CsSn₃ Thin Films for Photovoltaic Applications: *Nicholas LiCausi¹; Sunil Rao¹; Ishwara Bhat¹; Jim Wang²; Nemanja Vockic²; Matt Pfenninger²; John Kenney²; Zhuo Chen³; Kai Shum³; ¹Rensselaer Polytechnic Institute; ²OmniPV Inc.; ³The City University of New York*

In order to lower cost of solar cells, there is a push to make high-efficient thin film solar cells which are grown on non-crystalline substrates such as glass. However, films grown on glass are typically polycrystalline or amorphous and usually have low efficiency due to defects, grain-boundaries, etc. Another alternative method to reduce cost is to use a thin film that can absorb the solar radiation broadly and reemit the energy at a narrow wavelength band suitable for absorption by silicon solar cells. For this to be cost effective, the luminescence conversion efficiency should be very high. We have explored the use of a new class of materials, namely perovskite semiconductor CsSn₃ thin films, for this purpose that luminescence at 950nm. This film has exhibited high photoluminescence conversion efficiency and shows potential for use as a "spectral down converter" in photovoltaic applications. CsSn₃ films have been grown on glass substrates in a low pressure chemical vapor deposition (CVD) reactor using cesium formate (CF), tetramethyl-tin (TET), and ethyl-iodide (EI) as the cesium, tin and iodine precursors, respectively. Both TET and EI are liquids at room temperature with sufficiently high vapor pressures and hence these could be transported to the reaction zone using standard carrier gas bubbling method. However, CF is a solid with relatively low vapor pressure and transport to the reaction zone was challenging. To evaluate whether growth by this method is possible, we used two primary methods. In the first method, cesium formate is dissolved in methanol. The glass substrate is then dipped in this solution and subsequently dried on a hotplate at 80°C. This creates a film varying in thickness from ~20-100 μm. The substrate is then loaded into the CVD chamber and heated to the growth temperature. Reaction to get CsSn₃ was accomplished by passing TET and EI precursors using hydrogen as the carrier gas. Growth proceeds for 30-40 minutes and the sample is cooled under H₂ flow. The films are characterized by photoluminescence (PL) as well as scanning electron microscopy, energy dispersive x-ray analysis and x-ray fluorescence. In the second method, CF is first transported to the wafer by passing nitrogen over CF kept in a heated crucible, followed by passing TET and EI using hydrogen as the carrier gas. The second method resulted in more uniform film compared to the first method, but the overall thickness of the films is much lower. Growth temperatures of 300 – 600°C have been explored with the best PL efficiency obtained at 475°C. Further studies on the growth and film characterization will be carried out and the results will be reported at the conference. This is the first report of CsSn₃ growth by the CVD method.

4:30 PM Student

J9, Exploring More Effective Catalysts for Metal-Induced Growth of Thin Film Si: *Peter Mersich¹; Wayne Anderson¹; ¹University at Buffalo*

Thin film microcrystalline Si (μc-Si) is an attractive material due to improved optical absorption compared to single crystal Si, as well as, increased mobility when compared to amorphous Si (a-Si). Producing high quality μc-Si at an affordable price is a particular challenge. Metal-induced growth (MIG) is a method of producing thin film μc-Si at temperatures of 625 °C and below. Similar to metal-induced crystallization, MIG has the advantage of depositing and crystallizing Si in a single step, while simultaneously forming an ohmic back contact. While MIG with a Ni catalyst has typically yielded good results, the process does not occur below 575 °C. Al and Cu offer significantly reduced crystallization temperatures, and consequently, lower cost. The mechanism by which crystallization occurs differs depending on the metal properties. Metals like Ni and Cu initially form a silicide compound. With Ni, this silicide precipitates through the Si and crystallizes it by the diffusion of Ni and Si atoms. Since Cu forms a metal-rich silicide, this compound does not precipitate and instead provides enough latent heat to activate the phase transition to crystallized Si. Al does not form a silicide. Instead, Si atoms diffuse into the metal and form nucleation sites where Si grains will grow that eventually come into contact with each other and form a continuous film. The MIG process began with thermal evaporation of the metal film. This was then coated with Co to modulate the Si grain growth and improve film quality. When Si was subsequently sputtered at an elevated temperature, the metal film acted as a catalyst to crystallize the Si and form a continuous μc-Si film. After deposition, films were annealed at 700 °C for 2 hr in forming gas. The appearance of distinct facets along the surface of the film indicated strong crystallization throughout the film. A strong presence of metal near the surface of films using Al compared to films using Ni and Cu signified metal contamination throughout the film. While x-ray diffraction demonstrated strong Si peaks with each metal, the film using Al observed extraneous peaks not indicative of μc-Si. Application of these films was explored by fabricating Schottky photodiodes, which were measured under dark and one-sun illumination conditions. Linearity in the log-log plot of dark forward bias indicated space charge limited conduction in films using Al likely due to considerable metal contamination. This trend also applied to the photo-response, where the fill factor greatly suffered. Films using Cu obtained performance closer to those with Ni. While Al is capable of reducing the crystallization temperature the most, its properties may not make it suitable for MIG. With optimized thickness, Cu may serve to realize a lower cost MIG process, while maintaining film quality.

4:50 PM Student

J10, Enhanced Light Absorption in Thin-Film Silicon Solar Cells by Scattering from Sub-Surface Dielectric Nanoparticles: *James Nagel¹; Michael Scarpulla¹; ¹University of Utah*

Thin-film silicon solar cell technology has been receiving a great deal of attention in recent years as an avenue for reducing the bulk material costs of photovoltaic devices. In particular, silicon is especially promising due to the well-established infrastructure for its production, as well as its natural abundance and non-toxicity. Unfortunately, silicon also suffers from long absorption lengths towards the red end of the visible spectrum, thereby severely limiting efficiency as the cell thickness is reduced. One common solution to this problem is to scatter light into lateral directions within the cell [1], thereby forcing light to propagate through more material over the same given depth. Unfortunately, such approaches have typically required feature sizes on the order to several microns, which is unfeasible when the cell itself is only 1-10 μm in depth. Another method that has received significant attention in recent years has focused on light-scattering from surface plasmons on noble-metal nanoparticles placed over the cell [2, 3, 4]. This method works primarily by the same principle of light-trapping via lateral scattering within the cell, and does so with particles less than 100 nm in size. However, plasmonic enhancement has yet to be demonstrated in the presence of an anti-reflective coating (ARC), which is an essential component for capturing light within a solar cell. To take advantage of both the light collection from an ARC and the path-length enhancement from lateral scattering, we propose that nano-sized scatterers be

placed directly within the bulk material of the cell itself. As a demonstration of this concept, we used numerical computations from a finite-difference time-domain (FDTD) algorithm to simulate a 1.0 μm crystalline silicon (c-Si) solar cell with a 75 nm ARC composed of Si_3N_4 . We then inserted nano-sized particles of SiO_2 directly within the active layer of the cell to scatter light after passing through the ARC. We present the results of several simple geometries, including the full absorption function across the entire visible spectrum for each case. Our results indicate total absorbed power gains on the order of 5-10% when averaged across the visible spectrum, with most of the gain falling above 400 nm in wavelength. Around narrow bandwidths, some geometries can even surpass 70% in total absorbed power. We also explore the use of Au nanospheres as plasmonic scatterers in the presence of an ARC, with results that are inferior to the use of sub-surface dielectrics.

Session K: III-Nitride Nanowires

Wednesday PM
June 23, 2010

Room: 138
Location: University of Notre Dame

Session Chairs: Aric Sanders, NIST; Debdeep Jena, Univ of Notre Dame

1:30 PM

K1, Molecular Beam Epitaxy of Catalyst-Free InGaN/GaN Nanowires on (001) Silicon and Nanowire Light Emitting Diodes: *Wei Guo*¹; Meng Zhang¹; Pallab Bhattacharya¹; ¹University of Michigan

There is a need to develop reliable white light emitting diodes (LEDs) as energy efficient light sources for the next generation. (In)GaN materials have attracted a great deal of attention due to their wide bandgap ranging from 0.7 (infrared) to 6eV (ultra-violet). (In)GaN nanowires can be grown with reduced defect density on silicon substrates since the large surface-to-volume ratio helps to accommodate the mismatch strain. We have investigated molecular beam epitaxial growth of catalyst-free (In)GaN nanowires directly on (001) silicon substrates, doping in the nanowires, and the characteristics of LEDs made with the nanostructures. Catalyst-free nanowires were grown on silicon substrates by plasma-assisted MBE using a radio frequency plasma source to activate the nitrogen. Unlike conventional III-nitride nanostructure growth, a few monolayer of gallium were first deposited at 800°C onto the substrate in the absence of N_2 plasma. In order to study the nanowire growth mechanism, silicon substrates with different orientations, (100) and (111), were employed. The InGaN and GaN nanowires were grown under highly N-rich conditions. To achieve different emission wavelengths, InGaN nanowires with varied indium compositions were synthesized at 550°C. In addition, the indium composition was changed both gradually and abruptly along the nanowires during the growth to obtain broad and “white” emission. Structural characteristics of the nanowires grown on Si were studied using SEM. High density ($\sim 10^{11}\text{cm}^{-2}$) nanowires were grown with diameters ranging from 10 to 50nm. HR-TEM image shows InGaN nanowires free of dislocations on (001) silicon. A lattice constant of 5.4 Å, which corresponds to 25% indium composition in the alloy, was derived from the SAD pattern. A cross-sectional TEM study of the GaN nanowires grown on silicon (100) and (111) substrates shows that in both cases growth proceeds along the c-axis. Room temperature PL spectra ranging from ultraviolet to red were obtained from nanowires with different indium compositions. Broad emission with 140nm FWHM was recorded from InGaN nanowires with gradually changed indium composition during epitaxy. Such emission is representative of “warm” white light. LEDs heterostructure consisting of p-type GaN, undoped InGaN with varied indium compositions and n-type GaN were grown on n-type (100) silicon substrate. After planarization and formation of p- and n-ohmic contacts, the I-V characteristics were measured. A series resistance of 50 Ω is derived from these characteristics. White light was emitted by the nanowire LED at room temperature at a forward bias current of 100 mA. These characteristics of the nanowires and LEDs will be presented.

1:50 PM

K2, Photoluminescence of Bandgap-Graded InGaN Wires Grown by Molecular Beam Epitaxy: *Vladimir Protasenko*¹; Kevin Goodman¹; Thomas Kosel¹; Huili Grace¹; Debdeep Jena¹; ¹University of Notre Dame

Due to exceptional chemical stability and excellent mechanical, thermal, and electro-optical properties, the InGaN ternary alloy is a material of a choice for light emitting diodes (LEDs) and lasers operating in UV or near-UV spectral range. The usefulness of the material also stems from bandgap tunability; energy bandgap can be adjusted over broad range by proper choice of In concentration. For strained InGaN thin films grown on GaN, as the In concentration increases above ~10%, formation of structural defects and compositional disorder have been observed by high resolution TEM and atomic force microscopies, and by X-ray diffraction. On the other hand, for GaN semiconductor, it has been already demonstrated that shift from planar two-dimensional (2D) geometry of films to one-dimensional (1D) wires substantially suppresses the density of defects. So far, our attempts in growing ternary InGaN wires by MBE with ~20% In composition (suggested emission peak ~530 nm) uniformly distributed along the growth axis yield unexpected results. While the SEM micro-photographs unambiguously demonstrate successful non-catalytical growth of wires, low temperature photoluminescence (PL) studies, performed on wire ensembles, revealed broad emission spectra covering 360-700 nm range. In contrast, photoluminescence of a ~200 nm thick InGaN thin film with ~20% In content is well centered around 530 nm. At room temperature, a broad emission of wires collapses into 500-550 nm spectral range. To pinpoint the origin of a broad photoluminescence of wire ensembles, single wire PL and energy dispersive X-ray (EDX) measurements have been carried out. In PL experiments, substantial variations of the InGaN emission spectra of individual wires have been observed. While some wires show exhibit strong single peak emission, weaker and multiple peak emission of another wires indicates the essential intra-wire fluctuations of the In composition. On a separate set of single wires, EDX revealed gradual changes of In composition along the growth axis with the maximum concentration peaked near the wire tip. The EDX data in conjunction with scanning transmission electron microscopy and atomic force microscopy allowed us to estimate low temperature emission quantum yield of single wires. The estimates resulted in QY >10% and indicated that the surface of InGaN wires does not terribly quench the emission. The room temperature QY is about 10 times less than that measured at 4K. Currently, the development of a growth model for graded InGaN wires is in the progress, but, nevertheless, our data distinctly demonstrate the successful synthesis of compositionally graded InGaN wires using plasma assisted MBE. These defect-free wires offer not only a potential solution for a material suitable for the green emission but have potential applicability to broadband emission devices possibly as integrated phosphors.

2:10 PM

K3, Growth of Dislocation-Free and High-Indium-Content InGaN/GaN Coaxial Nanowires: *Qiming Li*¹; George Wang¹; ¹Sandia National Laboratories

High indium incorporation in InGaN is highly desirable for realizing high performance green and red III-nitride based light-emitting diodes. However, the large lattice mismatch between InGaN and GaN results in a high compressive strain energy density in InGaN, which leads to limited indium incorporation and high threading dislocation densities. In this work, we demonstrate the growth of dislocation-free InGaN layers on the sidewalls of GaN nanowires grown via Ni-catalyzed metal organic chemical vapor deposition (MOCVD). Indium incorporations as high as 40-60% in the shell layers were reached, as confirmed by scanning transition electron microscopy (STEM), energy dispersive x-ray spectroscopy, and spatially resolved cathodoluminescence microscopy. In order to better understand the results, the strain energy density distribution in an InGaN/GaN coaxial nanowire was calculated using finite element analysis. The indium distribution in the InGaN shell layer was found to be influenced by the strain energy density distribution. The observed high indium incorporation and lack of dislocations in the InGaN shell growth is attributed to the unique strain relaxation of the InGaN/GaN coaxial nanowires. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the

United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

2:30 PM

K4, Threshold Studies of Optically Pumped GaN Nanowire Lasers: *John Schlager*¹; Alexana Roshko¹; Aric Sanders¹; Kris Bertness¹; Norman Sanford¹; ¹NIST

GaN nanowires grown by plasma-assisted molecular beam epitaxy (PAMBE) have shown to be made up of defect-free, c-axis-oriented, wurtzite material exhibiting hexagonal cross sections, narrow x-ray signatures, bright photoluminescence (PL), and long (> 2ns) PL lifetimes. In addition, time-resolved photoluminescence (TRPL) measurements yield room-temperature surface recombination velocity (SRV) values of $\sim 1 \times 10^4$ cm/s for both doped and undoped nanowires without any special surface treatments. These relatively low SRV values were obtained under strong excitation conditions similar to those present during nanowire laser operation. Low SRV values indicate that efficient nanowire laser operation, where radiative recombination is the preferred route for photo- or electrically generated carriers, may be possible. In this work, the lasing thresholds of twenty-one optically pumped GaN nanowires grown by PAMBE and dispersed onto fused silica were measured. The excitation source was a frequency-quadrupled, Q-switched Nd:YVO₄ laser (266nm, 15kHz repetition rate, 8ns pulse duration, 8.5mW average power). Peak power intensities at the sample were kept below 10MW/cm² to avoid nanowire and substrate damage. The dimensions and morphology of the wires were determined with field-emission scanning electron microscopy (FESEM). Wire lengths ranged from 10.5 μ m to 18.7 μ m, and wire diameters ranged from 245nm to 1212nm. The wires had varying degrees of taper and different end qualities. With diameters of greater than 200nm and a material index of refraction of ~ 2.7 , these GaN nanowires are multimode waveguides with strong confinement that can support over 20 transverse modes. The lasing thresholds were not strong functions of nanowire diameter, but depended more on wire morphology and wire-end quality. The threshold peak intensities varied from 203kW/cm² up to 3.26MW/cm². The lowest lasing threshold was obtained in a wire with no measurable taper and flat and perpendicular end facets. With increasing pump power, the wires first emitted photoluminescence (PL) at a wavelength of ~ 364 nm (3.41eV), near the room-temperature bandgap of GaN. With higher pump powers, peak luminescence shifted to the red until narrow emission lines appeared around 371nm. The peak intensities of these lines, unlike the PL at 364nm, then increased superlinearly with pump power. The lasing spectra typically exhibited multiple lines corresponding to the oscillation of multiple axial modes. The axial mode separations ranged from 0.53nm to 1.2nm and were related to the roundtrip optical path lengths of these highly dispersive nanowire laser cavities. The discrepancy between the observed axial mode spacing and that calculated with an isotropic index indicates that the crystalline or birefringent nature of GaN is important to lasing behavior. Nanowires with good morphology (low taper) and flat ends are essential for low-threshold laser operation.

2:50 PM

K5, GaN Nanowire MOSFETs with Fully Conformal Cylindrical Gates: *Paul Blanchard*¹; Kris Bertness¹; Todd Harvey¹; Aric Sanders¹; Norman Sanford¹; Steven George²; Dragos Seghete²; ¹National Institute of Standards and Technology (NIST); ²University of Colorado

Due to their unique morphology, large direct bandgap, and excellent crystalline quality, GaN nanowires (NWs) grown by molecular beam epitaxy (MBE) are a promising material for the development of next-generation nanoscale electronic devices. In particular, GaN NW field effect transistors (FETs) have attracted significant interest both for potential device applications and for their usefulness in characterizing NW properties. However, previous GaN NW FETs have relied upon gates that do not make conformal contact to the entire nanowire circumference—at best, the NW has been sandwiched between a top and a bottom gate. This approach has generally led to inefficient gating. In addition, the asymmetric gate geometry of such devices makes it difficult to accurately extract NW carrier concentration from measured threshold voltages. In this report, we demonstrate novel n-type GaN NW metal oxide semiconductor FETs (MOSFETs) with symmetric, fully conformal cylindrical

gates. After the MBE NW growth process, the as-grown NWs were conformally coated with approximately 43 nm of Al₂O₃ ($k \sim 7.6$) and 35 nm of W via atomic layer deposition (ALD). The coated NWs were then harvested from the growth substrate and aligned by dielectrophoresis across electrodes on the device substrate. After masking the central gate region of each NW with photoresist, the W and Al₂O₃ layers were removed from the two end regions (source and drain) of the NW by tungsten etchant and 10:1 buffered oxide etchant (BOE). Finally, ohmic source and drain contacts and a contact to the W/Al₂O₃ gate were deposited. The completed surround-gate MOSFETs operated as n-channel depletion mode devices, with each device containing a single NW. Threshold gate voltages were typically between -5 and -12 V, with subthreshold gate leakage current on the order of 1 pA or less. On/off current ratios as high as 10⁹ were achieved with a drain-source bias of 5 to 6 V. Maximum transconductances exceeded 10 μ S. These characteristics compare favorably with the best GaN NW-based FETs that have been previously demonstrated. By taking advantage of the radial symmetry of the gate and applying simple electrostatic analysis by use of Gauss' Law, the NW carrier concentrations were estimated from the threshold voltages to be between 4×10^{17} and 9×10^{17} cm⁻³. Although these devices had excellent pinchoff characteristics, the NW MOSFETs also showed significant memory effects in gating. Hysteresis occurred during bi-directional gate voltage sweeps. In addition, threshold voltages sometimes drifted during repeated gate bias, resulting in uncertainty in the calculation of carrier concentration. These effects are most likely due to charge trapping at the NW/oxide interface or within the ALD Al₂O₃ layer. The nature of these charge traps is the subject of ongoing investigation.

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K6, Formation Mechanisms and Kinetics of Negative Nanowires in GaN and ZnO Using In-Situ Transmission Electron Microscopes: *Bong-Joong Kim*¹; Eric Stach¹; ¹Purdue University

Crucial to nanotechnology is the creation of nanoscale building blocks of various sizes and shapes. Nanostructures of wide band-gap gallium nitride and zinc oxide are of particular interest because of their applications in short-wavelength optoelectronic devices and high-power/high-temperature electronics. Here, we present in-situ microscopy studies of formation mechanisms and kinetics of negative nanowires (analogous to hollow nanopipes) in the temperature regime where GaN and ZnO are spontaneously decomposed. By heating the GaN layers above 925 °C, nitrogen desorption first becomes visible at the thinnest edges of the sample. Concomitant with this is the preferential dissociation of GaN along the {10-10} prism planes, resulting in the formation of hexagonal vertical negative nanowires in [0001] with a slight tapering. We also find that liquid Ga droplets formed by this decomposition accumulate at the edge of the faceted wires with no need for the addition of a liquid-forming metal layer. These droplets subsequently lead to the creation of lateral negative nanowires growing in the close-packed <10-10> by the solid-liquid-vapor (SLV) mechanism and the resulting structures are often kinked. Our quantitative measurements show that the growth rates of the laterally grown negative nanowires are independent of the wire diameter, indicating that the rate-limiting step is decomposition of GaN on the gallium droplet's surface. We compare the above with evaporation of defect free ZnO layers at the annealing temperatures at 500 ~ 900 °C. Similar to GaN, we find the development of vertical negative nanowires, but no lateral negative nanowire formation, which could be related to the absence of a liquid-forming catalyst during evaporation. Similar annealing experiments were conducted by adding an evaporated Au layer on the ZnO film. Up to 900 °C, the Au drops remain solid and promote the selective evaporation of ZnO, creating vertical negative nanowires via the solid-solid-vapor (SSV) mechanism. Interestingly, the coarsening of the Au catalytic drops is found to be negligible up to 800 °C. These nanoscale features offer promise as controllable templates and patterns for the creation and integration of a broad range of nanoscale materials systems, with such potential applications as solar cells, LEDs, and FETs.

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K7, Self-Assembled GaN/AlN Nanowire Superlattices on Si toward Non-Polar Intersubband Photonics: *Santino Carnevale*¹; *J Yang*¹; *P Phillips*¹; *M Mills*¹; *R Myers*¹; ¹Ohio State University

We examine coaxial growth of m-plane AlN/GaN superlattices (SLs) formed on self-assembled nanowires (NWs). Vertically aligned, c-plane oriented NW structures are grown on economical Si (111) by plasma-assisted molecular beam epitaxy. Previous reports indicate that these NWs are nearly defect free since threading dislocations terminate at the wires' base. Here we describe studies on the coaxial growth of SLs on the m-plane NW side walls. M-plane growth avoids band bending due to polarization charge, while the radial confinement allows for intersubband transitions normal to the Si substrates. Strain accommodation in the NWs allows for the formation of heterostructures with large conduction band offsets without adding dislocations that occur in planar films. Samples are grown in the N-rich regime at temperatures ranging from 700 to 800 °C at various combinations of III/V ratio and substrate temperatures to map out the growth phase diagram. Previous NW work has examined monotonic effects of group-III-flux, active nitrogen and substrate temperature on NW growth, but are not yet mapped into a growth phase diagram. We map out the NW density and radius dependence on calibrated III/V ratio and substrate temperature. This reveals systematic variations in NW density and growth rates, as well as the boundaries between 3D NW growth and 2D planar growth of GaN in the heavily N-rich regime. Using this information, NW density is controllable over two orders of magnitude. NW SLs are formed by first nucleating GaN NWs of a desired density and size and then alternately depositing GaN and AlN. Radial and horizontal growth rates calculated from SEM and z-contrast TEM measurements are used to design NW SLs for near-infrared intersubband transitions. Preliminary optical absorption and emission measurements of NW ensembles are presented.

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K8, HVPE Homoepitaxy of p-Type GaN on n-Type Catalyst Free GaN Nanowires: *Aric Sanders*¹; *Norman Sanford*¹; *Paul Blanchard*¹; *Kris Bertness*¹; *John Schlager*¹; *Andrew Herrero*¹; *Christopher Dodson*¹; *Albert Davydov*¹; *Denis Tsvetkov*¹; *Abhishek Motayed*¹; ¹National Institute of Standards and Technology (NIST)

Hydride Vapor Phase Epitaxy (HVPE) is a well established growth technique for the deposition of high free hole concentration p-type gallium nitride. It, like other gallium nitride growth techniques, suffers from the lack of high quality lattice matched substrates. We present the growth of p-type HVPE GaN using catalyst free GaN nitride nanowires as a lattice matched substrate. The nanowires were grown using plasma assisted molecular beam epitaxy (PAMBE), which has been shown to produce GaN of excellent quality on Si(111) substrates[1]. After wire growth, the n-type, silicon doped nanowires were used as a growth scaffold for p-type magnesium doped gallium nitride grown using HVPE. For small thicknesses of HVPE growth the resultant n-p material takes the form of core-shell nanowires. Scanning electron micrographs show distinctive dopant contrast between the p-type material and the n-type nanowires[2]. This contrast shows that the n-doped nanowire cores retain their hexagonal profile during the HVPE growth process. In addition, X ray diffraction under three symmetric and three asymmetric conditions reveal that the a and c lattice parameters of the nanowires remain unchanged after the HVPE deposition. The lattice parameters for three nanowire growths before and after HVPE growth fell between .518432 nm and .518536 nm for the c parameter and .31888 nm and .31910 nm for the a parameter. This is in agreement with other reported values for strain free GaN[3,4]. Photoluminescence at 4K for before HVPE growth shows near band emission at 3.472eV with clear phonon replicas and no observable sub bandgap features. After HVPE growth of p-type material, photoluminescence reveals the appearance of energy features at 2.8-3.0eV and 3.3eV that are associated with Mg incorporation in gallium nitride[5]. The spatially resolved morphology emission properties of the nanowires using electron microscopy will also be discussed. Finally, several electrical measurements determining material conductivity and carrier polarity will be presented. 1. K. Bertness et al., Catalyst-free growth of GaN nanowires. *Journal of Electronic Materials* (2006), 35, (4), 576-580. 2. M. El-Gomati et al., Why is it possible to detect doped regions of semiconductors

in low voltage SEM? *Surf. Interface Anal.* (2005); 37: 901-911. 3. Moram and Vickers, X-ray diffraction of III-nitrides, *Rep. Prog. Phys.* 72 (2009) 036502. 4. S.Porowski, Bulk and homoepitaxial GaN-growth and characterisation, *J. Cryst. Growth* 190, 153 (1998). 5. Reshchikov and Morkoc, Luminescence properties of defects in GaN. *JAP* 97, 06301 (2005).

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K9, Homoepitaxial Nucleation of GaN Nanowires in Grooves: *Alexana Roshko*¹; *Kris Bertness*¹; *Todd Harvey*¹; *Aric Sanders*¹; *Matthew Brubaker*¹; *Devin Rourke*¹; ¹NIST

In an effort to elucidate their nucleation mechanism, GaN nanowires were grown homoepitaxially by plasma-assisted molecular beam epitaxy on grooved substrates. The GaN templates consisted of 10 µm thick GaN (0001) films on Al₂O₃ substrates, with mechanically scribed grooves along the [11-20] and [1-100] directions and at 45 ° between these directions. It was found that the nanowires nucleated only in grooves on the GaN templates, not on the smooth (0001) surfaces. Based on the six sided nature of the nanowires it is concluded that they have a [0001] growth axis, as do GaN nanowires grown on Si (111) and on Al₂O₃ (0001) substrates with AlN buffers.¹⁻³ Also, analogous to many heteroepitaxial GaN nanowire growths, a matrix layer was formed across the entire substrate.²⁻⁴ This matrix was comprised of dense hexagonal pits which were quite uniform on the smooth substrate surface but had steeper side walls and were less regular in the substrate grooves. Unlike growths on Si (111) and Al₂O₃ (0001), where the majority of nanowires grow perpendicular to the substrate surface,^{1,4} the homoepitaxial nanowires grew at a wide range of orientations relative to the substrate normal. In addition the nanowires grew with a wide range of diameters (30 to 1000 nm), probably due at least in part to nanowire coalescence. In spite of their substantial variations in growth orientation and diameter, the nanowires have similar heights. The nanowire growth in the mechanically scribed grooves varied substantially from one groove to another and also frequently within a groove as well. These variations included: grooves completely filled with wires, grooves with almost no wires, grooves with both regions of wires and regions with no wires, and grooves with "rows" of wires. Interestingly the average nanowire diameter frequently differed from one "row" of wires to another along the same groove, indicating that the nanowire nucleation process was influenced by surface orientation or extent of damage/strain introduced by scribing. Growth of nanowires on substrates with etched grooves will also be discussed. 1. M. Yoshizawa, et al. *Jpn. J. Appl. Phys.* 36 L459 (1997). 2. E. Calleja, et al. *Phys. Rev. B* 62, 16826 (2000). 3. K.A. Bertness, et al. *Phys. Stat. Sol* 2, 2369 (2005). 4. A. Trampert, et al. p. 167 in *Proc. 13th Int. Conf. on Microscopy of Semicond. Matls*, edited by A. G. Cullis and P. A. Midgley, IOP Conf. Ser. No. 180 (2003).

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K10, Growth and Lift-off of High-Quality GaN Thin Films Using Self-Assembled Silica Microsphere Monolayers: *Qiming Li*¹; *George Wang*¹; ¹Sandia National Laboratories

We demonstrate that self-assembled monolayers of silica microspheres can be used as inexpensive, selective growth masks for both significant threading dislocation density reduction and laser-free lift-off of GaN epilayers and devices. Silica microspheres self-assemble into a close-packed monolayer on the surface of an initial GaN epilayer on sapphire using a Langmuir-Blodgett method. In a subsequent GaN regrowth, the silica microspheres effectively terminate the propagation of threading dislocations. As a result, the threading dislocation density, measured by large area AFM and CL scans, is reduced from 3.3 × 10⁹ cm⁻² to 4.0 × 10⁷ cm⁻². This nearly two orders of magnitude reduction is attributed to a dislocation blocking and bending by the unique interface between GaN and silica microspheres. The sequential wet etching of the samples in HF solution removes the silica microspheres sandwiched between the GaN epilayers and the growth template. Further wet etching of the samples in KOH solution successfully detaches the GaN epilayers from the growth templates. Micro-channels are created on the GaN epilayers by plasma etching in order to facilitate the uniformity of the wet etches. This laser-free lift-off technique may be potentially applied to lift-off GaN homoepitaxial thin film device from GaN bulk substrates. Sandia is a multiprogram laboratory operated by Sandia

Corporation, a Lockheed Martin Company, for the United States Department of Energy under contract DE-AC04-94AL85000.

Session L: III-N HEMTs I

Wednesday PM
June 23, 2010

Room: 155
Location: University of Notre Dame

Session Chairs: Siddharth Rajan, The Ohio State University; Debdeep Jena, University of Notre Dame

1:30 PM

L1, Formation of Structural Defects in AlGaIn/GaN High Electron Mobility Transistors under Electrical Stress: *Prashanth Makaram*¹; Jungwoo Joh¹; Carl Thompson¹; Jesus Del Alamo¹; Tomas Palacios¹; ¹Massachusetts Institute of Technology

Gallium nitride (GaN) based devices are of interest for a variety of radar and communication applications due to their ability to operate at high-power and high frequency. We have previously carried out extensive electrical reliability characterization of AlGaIn/GaN high electron mobility transistors (HEMTs) and found that degradation is driven by electric field. High-voltage stress results in an increase in off-state gate current, I_{Goff} and drain resistance, RD, along with a decrease in maximum drain current, I_{Dmax} . Transmission electron microscope (TEM) cross sectional image has shown that electrical degradation is closely related to structural damage in the GaN cap and AlGaIn barrier layers. Although the TEM analysis shows a detailed cross section of the defect area, it is an extremely localized technique. In order to better understand the structural degradation of AlGaIn/GaN HEMTs under electrical stress, a planar view of defect formation is required. In this work, we study plane view structural degradation of AlGaIn/GaN HEMTs after electrical stress by removing the SiN passivation layer and all the metals from the sample. We then use atomic force microscope (AFM) and scanning electron microscope (SEM) to image the semiconductor surface. In a series of OFF state (low ID, high VDS) experiments, identical devices were step-stressed up to various VDG's from 15 to 57 V at 150 C of base plate temperature. The critical voltage V_{crit} for which a sharp increase of gate current occurs [2] was determined to be around 20 V for this condition. For $V_{stress} > V_{crit}$, significant permanent decrease in I_{Dmax} of up to 10% as well as a large increase in current collapse took place. While the surface of a non-stressed device was found to be smooth after gate removal, AFM images of stressed devices revealed that a line-shaped indentation developed along the gate edge on the drain side for all stressed devices. For devices stressed at high voltage, the same feature, but more shallow, was found on the source side as well. In addition, beyond the critical voltage we observed nanopipe or pit formation at the drain side edge of the gate. These pits grow in density and size along the gate as the stress voltage increases. In order to understand time evolution of these crystallographic defects, we have also performed OFF-state stress tests at VDG=50 V. Two devices were stressed for 10 and 1000 minutes, respectively. We observe that as the device is stressed for longer times, the pits grow and merge to form a continuous defective region along the gate finger. This represents the first planar view of structural defects in electrically stressed GaN HEMTs. The methodology described here will enable better understanding of the evolution of defect formation under various electrical stress conditions.

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L2, Electrical Properties of GaN/AlN/GaN Heterostructures: Presence of 2DHG: *Satyaki Ganguly*¹; Debdeep Jena¹; ¹University of Notre Dame

Large band offsets coupled with the highest possible spontaneous and strain induced polarization fields in AlN/GaN heterostructures have led to the formation of two-dimensional electron gas (2DEGs) with densities in excess of $1 \times 10^{13} \text{cm}^{-2}$. However, it is necessary to grow a thin epitaxial cap layer of GaN on top of the AlN/GaN heterostructure in many device applications. In this work we study the total charge density and mobility of the resulting conducting channels with respect to the GaN cap thicknesses. For this study the MBE growths were

performed under metal rich conditions. A series of samples with a thin 1.5nm AlN nucleation layer (to eliminate the buffer leakage), followed by 235nm UID GaN, 3.5nm AlN barrier and GaN cap thicknesses ranging from 0nm to 40nm were grown. 'In' contacts in the van-der Pauw geometry were made for Hall Effect measurements. With the increase of the GaN cap layer thickness, the measured carrier density increased from $1 \times 10^{13} \text{cm}^{-2}$ (no GaN cap) to $\sim 5 \times 10^{13} \text{cm}^{-2}$ (40nm GaN cap) at RT. The trend obtained here is contradictory to an earlier report. The carrier mobility measured in this work shows a slight increase at the beginning ($1000 \text{cm}^2/\text{V-s}$ for no GaN cap to $1100 \text{cm}^2/\text{V-s}$ for 4nm GaN cap) and then decreases steadily from $1100 \text{cm}^2/\text{V-s}$ (4nm GaN cap) to $\sim 529 \text{cm}^2/\text{V-s}$ (40nm GaN cap) at RT. The trend as obtained from the experimental data is well explained by considering the formation of two-dimensional hole gas (2DHG) at the GaN/AlN interface near the surface. With the increase of GaN cap layer thickness, the valence band edge in the GaN cap layer starts approaching the Fermi level, resulting in the formation of a 2DHG. A simple analytical model considering the formation of both 2DEG and 2DHG (which was overlooked in earlier report) reveals the decreasing and increasing trend of 2DEG and 2DHG respectively with the increase of GaN cap thickness. The total carrier density and total mobility formulated from the two carrier Hall model, is given as $n_t = (n\mu_n + p\mu_p)^2 / (p\mu_p^2 - n\mu_n^2)$; $\mu_t = (p\mu_p^2 - n\mu_n^2) / (n\mu_n + p\mu_p)$. Assuming $\mu_n \sim 1000 \text{cm}^2/\text{V-s}$ (which is quite reasonable as evident from the experimental data), $\mu_p \sim 400 \text{cm}^2/\text{V-s}$ (to fit the experimental data) and calculating n and p from the analytical model, the total carrier charge density and mobility with varying GaN cap thicknesses are determined. It has been found that the experimentally obtained and the analytically calculated total carrier charge density and mobility are in reasonable agreement. The simultaneous presence of 2DEG and 2DHG in this structure opens the possibility of various novel applications such as GaN based natural super junctions for high voltage switching.

2:10 PM Student

L3, Study of Cause of G_m -Collapse for Higher Gate Voltages in N-Polar GaN HEMTs with Scaled GaN Channels: *Nidhi Nidhi*¹; Oliver Bierwagen¹; Sansaptak Dasgupta¹; David Brown¹; Stacia Keller¹; James Speck¹; Umesh Mishra¹; ¹University of California Santa Barbara

N-polar GaN/AlGaIn HEMTs have been of interest to the nitrides community recently due to their several advantages over Ga-polar GaN-based HEMTs such as lower contact resistance, better electron confinement and enhancement mode operation. Currently, N-polar GaN HEMTs are being scaled to achieve X and Ka band performances. Scaling in N-face HEMTs, however involves scaling of GaN channel along with gate-length, in comparison to Ga-face where the barrier material is scaled instead of the channel. Scaled self-aligned HEMTs on N-face with regrown access regions reported by Nidhi et. al. at IEDM 2009 demonstrated significant reduction in access resistance. However, even though g_m remained flat for large values of current due to no source choke in a self-aligned structure, it was observed that g_m fell rapidly with higher gate biases even before the gate was forward biased. In this paper, this anomalous g_m -collapse for higher gate voltages has been studied by using low temperature Hall and gated TLM measurements. It has been proposed that as the GaN channel thickness is scaled, application of higher gate biases shifts the centroid of the 2-dimensional electron-gas towards the GaN/SiNx-insulator interface, thereby causing mobility degradation which then causes the transconductance to collapse. It is proposed that the insertion of AlN interlayer above the GaN channel could help prevent the penetration of electron wavefunction into the SiNx due to the barrier created by the band-edge discontinuity and reverse polarization fields, and hence reduce the interface roughness and remote impurity scattering from the SiNx interface.

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L4, Polarization-Engineered Low-Leakage Buffers for Nitride HEMTs Grown by MBE: *Yu Cao*¹; Guowang Li¹; Ronghua Wang¹; Chuanxin Lian¹; Tom Zimmermann¹; Grace Xing¹; Debdeep Jena¹; ¹University of Notre Dame

Buffer leakage is a vexing problem in the development of nitride HEMTs. It degrades the on/off ratio in digital devices, decreases the device speed in high-speed analog applications, and compromises the breakdown property in high-voltage switching applications. This problem exists in HEMTs grown on both

semi-insulating (SI) SiC and GaN substrates/templates. On SI GaN templates, high-quality Al(Ga)N/GaN heterojunctions can be achieved using just a few hundred nm GaN buffer layer, which greatly reduces required epitaxial resources and time. Recently, we reported a dopant-free approach by engineering the polarization effect. Insertion of an ultrathin AlN nucleation layer (NL) greatly reduces the buffer leakage, and leads to a much steeper subthreshold slope of HEMT devices and the on/off ratio increased from 10^2 to 10^6 . Motivated by this prior result, we have performed a systematic study of the buffer leakage dependence on the AlN nucleation layer thickness, and growth conditions. Two series of AlN/GaN HEMTs were grown by MBE to investigate the buffer leakage as a function of a) the metal fluxes and the b) NL thickness in MBE growth. In the first series (a), the AlN NL thickness was fixed at 1.5 nm, while the Al flux $F(\text{Al})$ for this NL was varied from $\sim 4.0 \times 10^{-8}$ Torr to $\sim 1.7 \times 10^{-7}$ Torr. The NL grown in Al metal-rich regime results in high buffer leakage. The NL grown in the intermediate regime shows good buffer insulation at low bias, but breaks down rapidly at high bias. The N-rich growth condition is found to result in the most insulating buffer, where the leakage current density is less than 10 nA/mm at 10 V DC bias. The nitrogen-rich grown AlN NL prohibits the diffusion of the n-type impurities like silicon and oxygen from the substrate into the GaN buffer. Meanwhile, a natural AlN back barrier is formed, which provides better 2DEG confinement and prevents electrons flowing to the regrowth region under bias. The second series (b) were grown with NL thicknesses 1.5 nm, 3.0 nm, 4.5 nm and 9.0 nm. The buffer leakage mapping across a $1 \times 1 \text{ cm}^2$ sample with a 1.5 nm AlN NL shows leakage less than 5 nA/mm in all dies except the one. In samples with thicker AlN NLs, the leakage current has large spans, sometimes varying from nA/mm to mA/mm. It is clear that thick AlN NLs are not suitable for HEMTs. We conclude that the nucleation layer needs to be well designed to avoid forming new conducting paths in the buffer layer. A 1.5 nm AlN nucleation layer grown in the N-rich regime with Al flux of $\sim 4.1 \times 10^{-8}$ Torr achieves highly insulating buffer with a high degree of uniformity. This result presents an attractive route towards GaN-based digital and high voltage devices in the future.

2:50 PM Student

L5, The Influence of High-k Gate Dielectrics on Deep Traps in AlGaIn/GaN High Electron Mobility Transistors Measured by Deep Level Spectroscopy
Methods: *Qilin Gu*¹; Aaron Arehart¹; Andrew Malonis¹; Omair Saadat²; Tomas Palacios²; Steven Ringel¹; ¹The Ohio State University; ²Massachusetts Institute of Technology

Surface passivation by dielectric layers has been extensively used to address reliability issues related to gate leakage current associated with surface states for GaN electronics. For this purpose, high-k dielectric materials with excellent thermal stabilities are of great interest and recent efforts demonstrated that AlGaIn/GaN HEMTs passivated by Al_2O_3 , Ga_2O_3 , and HfO_2 exhibit significant reduction in gate leakage and enhancements in drain current.¹ However, the effects of high-k dielectrics on the presence and evolution of trap states are relatively unexplored. Given the connection between traps, passivation and reliability, this area is of great interest. Here, we employed constant-drain-current-based deep level optical and transient spectroscopies² (Cl_D -DLOS/ Cl_D -DLTS) to investigate correlations between deep levels and specific high-k dielectrics in AlGaIn/GaN HEMTs. Ga-face AlGaIn/GaN devices with 2 nm GaN cap layers were grown on Si (111) substrate by Nitronex using metalorganic chemical vapor deposition. One sample was processed without passivation, whereas two other samples were passivated by 15 nm Al_2O_3 and 15 nm HfO_2 high-k dielectrics, respectively, deposited by atomic layer deposition to form metal-oxide-semiconductor (MOS)-HEMTs. Cl_D -DLOS measurements revealed trap levels at $E_c - 3.10 \text{ eV}$ and $E_c - 3.85 \text{ eV}$ for un-passivated devices, matching those observed earlier for AlGaIn layers,^{2,3} an additional level at $E_c - 1.68 \text{ eV}$, and a level at $\sim E_c - 2.6 \text{ eV}$ likely due to the V_{Ga} in GaN. Passivation resulted in significant differences in the DLOS spectra. The most obvious result is a $>5X$ increase in total trap concentration for the HfO_2 passivated device – noting that sources for most of these traps have been previously assigned to carbon or cation vacancy defects in GaN and AlGaIn.^{3,4} More striking is the appearance of a new trap with an $\sim E_c - 1.8 \text{ eV}$ onset and concentration of $\sim 1.2 \times 10^{12} \text{ cm}^{-2}$, which might be associated with the HfO_2/GaN interface or the HfO_2 itself. The high

trap concentration creates a large threshold voltage shift upon optical excitation of individual traps. This effect was not apparent for the Al_2O_3 -passivated sample, which revealed relatively little impact based on Cl_D -DLOS alone. We are presently performing Cl_D -DLTS measurements to observe traps closer to E_c than possible by Cl_D -DLOS to obtain a comprehensive picture. However, pulsed I-V results from these devices are also revealing and consistent with the trap spectroscopy results where the HfO_2 passivated device displays the largest drain-current dispersion while Al_2O_3 passivation both reduces dispersion and increases the drain current magnitude compared to the un-passivated device – both of which may result from successful passivation of shallower states that we are currently exploring by Cl_D -DLTS. [1] O. I. Saadat, et al., IEEE Electron Device Lett., 30, 1254 (2009). [2] A. Arehart, PhD dissertation, The Ohio State University, 2009. [3] A. Armstrong et al., Appl. Phys. Lett., 89, 262116 (2006). [4] A. Hierro et al., Appl. Phys. Lett., 77, 1499 (2000).

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L6, PECVD-SiN, Si or Si/Al₂O₃-Capped ED-Mode AlN/GaN Inverters:
*Tom Zimmermann*¹; Yu Cao¹; Guowang Li¹; Ronhua Wang¹; Patrick Fay¹; Greg Snider¹; Debdeep Jena¹; Huili Xing¹; ¹University of Notre Dame

Enhancement-depletion-mode subcritical barrier AlN/GaN inverters have been fabricated. In subcritical heterostructures there is no 2DEG at the AlN/GaN interface. Additional cap-layers on top of the ultra-thin AlN barrier can reliably enhance a 2DEG at the heterointerface with high 2DEG-densities in excess of 10^{13} cm^{-2} . CAT-CVD-, Silicon- and Si/CAT-CVD-caps got already explored but Silicon caps proved instable over time in air and PECVD-SiN with a sheet-resistance-optimized thickness of about 15 nm is too thick for gate-dielectrics. In contrast, a thin Si (2 nm / ALD- Al_2O_3 (4 nm) cap layer reliably enhances a 2DEG in subcritical AlN/GaN heterostructures with 1.5 nm AlN barrier and highly insulating buffer. The induced 2DEG results in a low heterostructure sheet resistance of $\sim 320 \text{ Ohm/sq}$. with a very high sheet charge density of $\sim 4 \times 10^{13} \text{ cm}^{-2}$. The demonstrated inverter is operating at $V_{DD} = 5 \text{ V}$ and consists of an enhancement- and depletion-mode HEMT with 1.5 nm thin subcritical AlN barrier, a low-power PECVD-SiN cap-layer and ebeam- Al_2O_3 gate oxide. The low-power SiN deposition in a standard PECVD shall avoid plasma-damage to the heterostructure. Ohmic contacts are deposited on top of SiN layer and get RTP-annealed. Gate-length for e-mode and d-mode FET are 3 μm and 2 μm , respectively. The sub-threshold slope of $\sim 600 \text{ mV/decade}$ and a threshold voltage $V_{th} = -1.2 \text{ V}$ for the depletion-mode FET in the inverter has similar absolute values like the used enhancement-mode FET with $\sim 620 \text{ mV/decade}$ ss-swing and $V_{th} = +1.1 \text{ V}$. Further technological optimization especially of ohmic contacts will lead to similar high DC-output current levels in e- and d-mode subcritical AlN/GaN devices and will enable the monolithic integration of enhancement- and depletion-mode AlN/GaN HEMTs for digital logic applications.

3:50 PM

L7, Late News

4:10 PM

L8, Demonstration of Enhancement Mode AlN/Ultrathin AlGaIn/GaN HEMTs Using Selective Wet Etching: *Travis Anderson*¹; Marko Tadjer²; Michael Mastro¹; Jennifer Hite¹; Karl Hobart¹; Charles Eddy¹; Fritz Kub¹; ¹Naval Research Laboratory; ²University of Maryland

The AlGaIn/GaN High Electron Mobility Transistor (HEMT) has attracted considerable attention as a candidate next-generation device for both microwave and high power switching applications. While significant progress has been made toward developing depletion mode devices, a normally-off device is highly desirable for two key applications: power converters and digital logic circuits. Most efforts toward normally-off operation have focused on plasma processing methods to selectively modify the charge distribution only in the region under the gate, either by inductively coupled plasma (ICP) etching or fluorine-based plasma exposure. In this work, a reliable and selective wet etch structure is demonstrated. This structure consists of a GaN buffer layer, an ultrathin AlGaIn layer ($<8 \text{ nm}$) for threshold voltage control, and an AlN cap

layer to increase the polarization charge and reduce resistance in the source-drain access regions. A selective wet etch process has been developed based on literature reports that AlN is etched in heated AZ400K photoresist developer. A set of test samples with an 8 nm AlGaIn layer were initially used to study the wet etch process and verify selectivity. XPS characterization confirmed that the etch is selective to AlN, and stopped on layers containing Ga. SEM images were taken on ungated samples, and indicated lateral etching of the AlN layer due to the isotropic nature of the wet etch process. A study of threshold voltage indicated a shift from -1.3V on an unetched structure to -0.4V after 10 minutes of etching, then no further change up to 70 minutes, supporting the etch stop hypothesis. The current level degraded with each subsequent etch step, which was thought to be due to the increase in the resistance in the source-drain access regions due to the lateral etching. This is consistent with measurements of the on-resistance from gated device testing. A sample with a 4 nm AlGaIn layer, etched using the optimized etch time, demonstrated a threshold voltage of +0.21V, shown in Figure 3. The threshold voltage values for both 8 nm and 4 nm AlGaIn layers are consistent with theoretical calculations and literature reports from structures with comparable AlGaIn thickness. While current density was low, it is comparable to that found in an unetched structure with similar sheet resistance and charge density.

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L9, Growth and Characterization of InGaIn Heterojunction Bipolar Transistors: Zachary Lochner¹; Hee Jin Kim¹; Suk Choi¹; Yi-Che Lee¹; Yun Zhang¹; Jae-Hyun Ryou¹; Shyh-Chiang Shen¹; Russell Dupuis¹; ¹Georgia Institute of Technology

The device operation of InGaIn/GaN heterojunction bipolar transistors (HBTs) grown by metalorganic chemical vapor deposition is examined. InGaIn is used in the p-type base layer for NpN III-nitride HBTs due to its improved p-type electrical properties, as well as its lower bandgap energy relative to that of GaN, resulting in reduced base contact and sheet resistance. The strain induced between the InGaIn base and outer GaN emitter and collector layers leads to material defects, such as dislocation and V-defects, degrading the quality of the base and emitter, and hence inhibiting the device performance. Thus a graded base-collector (BC) and base-emitter (BE) structure was previously developed to improve crystal qualities at each interface and improve the current gain. This study compares structures with two different Indium concentrations, 3% and 5%, each employing the graded junction design. The HBT structures presented in this study consists of a 70 nm n⁺⁺-GaIn:Si (n=1×10¹⁹ cm⁻³) emitter, a 30 nm n⁺⁺-In_xGa_{1-x}N:Si (n=1×10¹⁹ cm⁻³ x=0.03/0.05-0) graded emitter, a 100 nm p⁻-In_xGa_{1-x}N:Mg base (p=2.5×10¹⁸ cm⁻³, x=0.03, 0.05), a 30 nm In_xGa_{1-x}N:Si graded collector (n=1×10¹⁸ cm⁻³, x=0-0.03/0.05), a 0.5 μm n-GaIn:Si collector (n=1×10¹⁷ cm⁻³), and 1.0 μm n⁻-GaIn:Si subcollector (n=2×10¹⁸ cm⁻³). The BC grading layer was grown by ramping the trimethylindium (TMI) flow rate, while the BE grading layer utilized both TMI and temperature ramping. The Indium composition was varied by adjusting the base growth temperatures to 850°C and 820°C for 3% and 5% respectively. Separate samples were grown just up to the base to compare the surface morphology of In_{0.03}Ga_{0.97}N and In_{0.05}Ga_{0.95}N by atomic force microscopy. The In_{0.05}Ga_{0.95}N base-only sample had a higher pit density than the In_{0.03}Ga_{0.97}N counterpart, as is expected from higher strain conditions. The effects of these defects are reflected in the device performance. If we consider the band offset between the InGaIn base and GaN layer, the HBTs with p-In_{0.05}Ga_{0.95}N base are expected to show higher current gain than HBTs with p-In_{0.03}Ga_{0.97}N base. However, typical current gains for HBTs with p-In_{0.03}Ga_{0.97}N base were found to be around 82 and the current gains for HBTs with p-In_{0.05}Ga_{0.95}N base were around 35, lower than that of the HBTs with p-In_{0.03}Ga_{0.97}N base. It is supposed that the higher defect density compromises the benefits of the lower bandgap. Several other device configurations have also been considered in order to improve performance, including a single quantum well and superlattice base structure. It is theorized that the quantum confinement will aid lateral carrier transport within the base.

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L10, High Temperature Transport Properties of GaN HEMTs with Various Heterostructure Designs: Ronghua Wang¹; Yu Cao¹; Guowang Li¹; Tom Zimmermann¹; Chuanxin Lian¹; Xiang Gao²; Shiping Guo²; Debdeep Jena¹; Huili Xing¹; ¹University of Notre Dame; ²IQE RF LLC

GaN based HEMTs are being developed for high-temperature, high-power and high-frequency applications. The advantages over traditional GaAs and Si based electronic devices are the wide band gap, and high carrier densities. At high current levels, the channel reaches high temperatures in AlGaIn/GaN HEMTs, with a corresponding drop in the conductance of the two-dimensional electron gas (2DEG). To improve the high-power and high-temperature device performance, it is necessary to understand the high temperature transport properties of nitride transistors. In this work, high temperature Hall-effect measurements were performed for GaN HEMTs employing various heterostructures. Five different HEMT heterostructures were studied in a comparative fashion-(a) Al_{0.28}Ga_{0.72}N/GaN, (b) Al_{0.28}Ga_{0.72}N/AlN/GaN, (c) Al_{0.83}In_{0.17}N/AlN/GaN, (d)Al_{0.80}Ga_{0.20}N/AlN/GaN, and (e) AlN/GaN. Mesa-isolated van der Pauw geometries with annealed Ti/Al/Ni/Au contacts were used for Hall-effect measurements, which were performed with a Lakeshore HMS system over the temperature range 25°C<T<475°C. The 2DEG density N_s drops slightly from 25 to 200°C and then increases monotonically for Sample (a)-(c), but increased slowly from 25 to 400°C, and then sharply till 475°C in Sample (d)-(e). The charge density in each sub-band N_s (i) is related with Ef-Ei and T, and N_soT in our study arrange with a constant Ef-Ei. But the band gap shrinkage with increasing temperature leads to a smaller Ef-Ei, and therefore N_s decreased first in Sample (a)-(c). But in Sample (d) and (e), thermal expansion should be considered because both structures have a very large piezoelectric polarization, which strongly depends on the strain. For all the samples, N_s increased sharply for T>400°C. This is possibly associated with the thermal ionization of deep-levels and traps in GaN buffers, but needs more work to verify. The 2DEG mobility drops with increasing temperature, and merges to ~200 cm²/V.s at 475°C irrespective of the heterostructure design. Taking Sample (a) and (b) as examples, acoustic phonon (AP) scattering, longitudinal optical (LO) phonon scattering, and alloy disorder scattering mechanisms were taken into account to model the mobility temperature-dependence, and resulted in a good match with the experimental results. When the temperature is higher than 200°C, LO phonon scattering becomes dominant, and the mobility becomes independent of the specific nature of the heterostructure. When the temperature is lower than 200°C, the slight mobility variation is related with the 2DEG density; LO phonon scattering is stronger for higher carrier density, leading to a lower mobility. In summary, high temperature transport properties in various GaN HEMT heterostructures from 25 to 475°C have been investigated using Hall-effect measurements. The 2DEG density change varies in different structures but increases generally, and the mobility drops as temperature increases. At temperatures higher than 400°C, LO phonon scattering limits the mobility to 200 cm²/V.s for all studied heterostructures.