

53rd ELECTRONIC MATERIALS CONFERENCE and Exhibition

June 22-24, 2011
University of California - Santa Barbara
Santa Barbara, California

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TMS
FOUNDATION

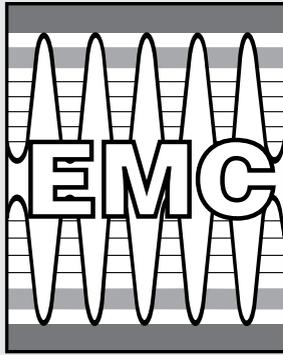
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FINAL PROGRAM

www.tms.org/EMC.html

ELECTRONIC MATERIALS CONFERENCE



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It's Time to Get Electrified!

Welcome to the 53rd Annual Electronic Materials Conference (EMC)

Sponsored by the



This is the premier annual forum on the preparation and characterization of electronic materials.

Your Registration Fee Includes

- Admission to All Technical Sessions
- Access to the Exhibition
- Wednesday Night Welcoming Reception
- Coffee Breaks
- Gainey Vineyard Social Event*

**One day registration does not include the Gainey Vineyard event.*

Value for Your Cost

EMC is being coordinated with the Device Research Conference, also held at the University of California - Santa Barbara from June 20 to 22. Badges will be accepted for admittance to both conferences on Wednesday, June 22.

Table of Contents

	Page
About the Conference/Location	1
Maps.....	2-3
Networking & Social Events	4
Exhibition	4
Awards.....	5
Proceedings.....	6
Publications	6
Organizers	6
Technical Program	10

ABOUT THE CONFERENCE

Technical Sessions

The technical program commences with the EMC Student Awards Ceremony and Plenary Lecture on Wednesday, June 22 at 8:20 a.m. All sessions will be held on the campus of the University of California – Santa Barbara.

Conference Registration

The on-site registration desk in the University Center will be open beginning Tuesday afternoon and extending through Friday morning during the following hours:

Tuesday, June 21.....	3 to 5 p.m.
Wednesday, June 22.....	7:30 a.m. to 5 p.m.
Thursday, June 23.....	7:30 a.m. to 5 p.m.
Friday, June 24.....	7:30 to 10 a.m.

About the Conference Location

The University of California, Santa Barbara, is situated on 1,055 acres along the picturesque California coast about 100 miles northwest of Los Angeles.



Computer/Network Facilities



Wireless computer access is free on campus. On-campus attendees will receive a code when they check in that can be used at the residence halls, as well as at the University Center.

Off-campus attendees will be given a list of access codes at the registration desk in the University Center.

CAMPUS DINING

DE LA GUERRA Dining Hall

Only credit card payment accepted. We accept Mastercard and Visa. On-campus lodging fee includes meals.

Dining Prices:

Breakfast	\$12
Lunch.....	\$12
Dinner.....	\$12

Serving Hours:

Breakfast	7 to 8 a.m.
Lunch.....	11:45 a.m. to 1:15 p.m.
Dinner.....	5:30 to 7 p.m.

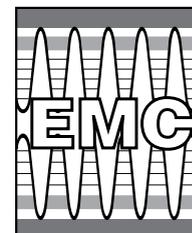
Parking

“PAY & DISPLAY” PARKING PERMIT MACHINES

EMC participants staying in hotels or other off-campus accommodation will drive directly to the parking lot assigned for the conference. Machines selling “Pay & Display” permits are located in each parking lot.



ELECTRONIC MATERIALS CONFERENCE 2011



2011



Conference Facilities

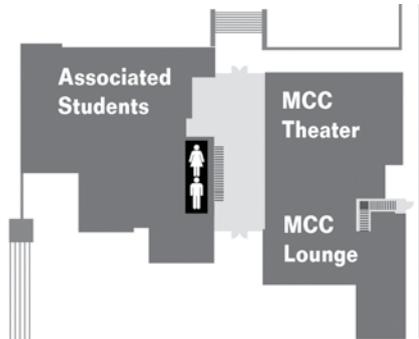
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- Accessible Parking
- Motorcycles
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- Parking Dispensers
- Parking

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UNIVERSITY CENTER

MAIN LEVEL



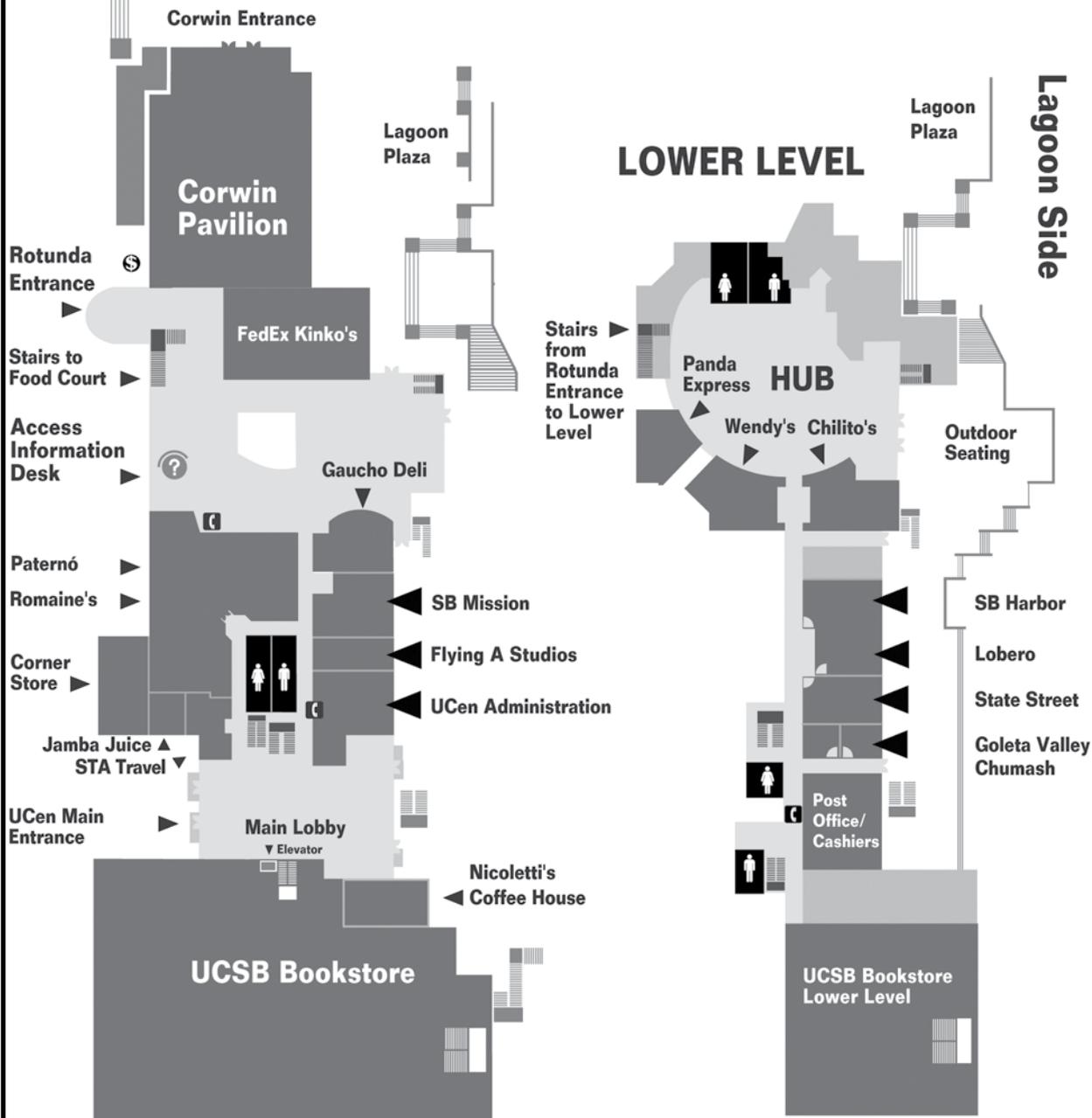
MEETING ROOMS

MAIN LEVEL

SB Mission
Flying A Studios

LOWER LEVEL

SB Harbor
Lobero
State Street
Goleta Valley
Chumash



NETWORKING & SOCIAL EVENTS

Welcoming Reception/Exhibit Viewing

Wednesday, June 22 - 6 to 8 p.m.
University Center – Lagoon Plaza

This event and exhibition is open to all attendees of EMC 2011. After your first full day of programming, reacquaint yourself with familiar colleagues or develop new connections in a casual atmosphere. Enjoy refreshments and peruse the exhibition for the latest products available for the electronic materials field.

Social Event at the Gainey Vineyard

Thursday, June 23 - 6:30 to 9 p.m.

The 85-acre Gainey Vineyard is located in the heart of Santa Barbara's wine country. Conference attendees will enjoy an evening of great food, fine wine and networking in this beautiful setting.

Ticket included with Full Conference and Student registration.

Guests and One-day registrants - \$70 Adult and \$35 Children 12 and younger

NOTE: Tickets are limited for this event. Please contact TMS staff for availability.

Buses to the event will board from 5 to 5:15 pm at University Center – Lagoon Plaza
Buses will board for the return trip from the event site from 8:45-9 p.m.

Coffee Breaks

University Center – Lagoon Plaza
Coffee breaks will be continuously available throughout the day.

GENERAL INFORMATION

Dress

Casual clothing is appropriate attire, along with a sweater or light jacket occasionally needed for the evenings. Layered clothing is recommended for cooler days or in air-conditioned buildings. Comfortable walking shoes, a light raincoat and an umbrella are also recommended, as the university is essentially a walking campus.

Campus Smoking Policy

The university prohibits smoking in all buildings, including residence halls. Smoking is permitted in designated areas outside and twenty-five feet from structures.

Audio/Video Recording Policy

TMS reserves the rights to any audio and video reproduction of all presentations at every TMS- sponsored meeting. Recording of sessions (audio, video, still photography, etc.) intended for personal use, distribution, publication, or copyright without the express written consent of TMS and the individual authors is strictly prohibited.



Americans With Disabilities Act

TMS strongly supports the federal Americans with Disabilities Act (ADA) which prohibits discrimination against, and promotes public accessibility for, those with disabilities. In support of, and in compliance with, ADA, we ask those requiring specific equipment or services to indicate their needs on the enclosed housing form or contact TMS Meeting Services in advance.

Cell Phone Use

In consideration of attendees and presenters, TMS kindly requests your cooperation in minimizing disturbances which may occur during technical sessions due to cell phone use. Please place cell phones or other electronic devices in "silent mode" while you are in meeting rooms.

EMC Exhibition

To complement the engaging technical programming and networking, EMC 2011 also offers an exhibition of electronic materials technology and related services. Take advantage of this opportunity to meet these providers and discover these cutting edge products.

Exhibit Location

University Center – Lagoon Plaza

Exhibit Hours

Wednesday, June 22: 9:30 a.m. to 1:30 p.m., 3 to 4 p.m. and 6 to 8 p.m.

Thursday, June 23: 10 a.m. to 1:30 p.m. and 3 to 4 p.m.

Exhibitors (as of June 1)

- Big C
- Lake Shore Cryotronics
- Omicron US
- SAFC Hitech
- Veeco Instruments
- United Mineral & Chemical Corp
- IXRF Systems
- MMR Technologies
- Riber
- Structured Materials, Inc
- Wafer Technology

AWARDS

John Bardeen Award

Established in 1994, this award recognizes an individual who has made outstanding contributions to, and is a leader in the electronic materials field.



2011 Recipient:
Stephen Pearton,
Professor, University of Florida

Citation: For pioneering advances in the science and application of advanced electronic and photonic device fabrication techniques for compound semiconductor devices used in cell phones, wireless communication systems, collision-avoidance radar, high density DVDs, satellite systems,

wireless local area networks, GPS, broad-band satellite services and automotive radar-smart-cruise control, traffic lights and other displays.

"TMS is an enormously respected society and the John Bardeen award is one of its premier honors. I am deeply grateful to the society for this recognition and to the collaborators I have worked with over the years at the Australian Atomic Energy Commission, UC Berkeley, Bell Labs and now University of Florida for their many contributions. John Bardeen was one of the greatest scientists of the modern age and the previous winners of this award have all been esteemed leaders in the fields of semiconductors and related materials. I am very pleased and deeply honored to join this select group and to be a proud TMS member."

How to Nominate a Colleague and for Additional Information

For award criteria and additional information, visit the TMS Honors & Awards site at <http://www.tms.org/society/tmsawards.aspx>.

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Materials Society Marketplace**

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2010 Best Oral Presentation Student Award Winners

Ashish Baraskar,
University of California, Santa Barbara
Paper: "In-situ Ohmic Contacts to p-InGaAs"
Advisor: Prof. Mark Rodwell

Anthony Rice,
North Carolina State University
Paper: "Morphological Development of Homoepitaxial AlN Thin Films Grown by MOCVD"
Advisor: Dr. Zlatko Sitar

James Riley,
Northwestern University
Paper: "Pulsed-Laser Atom Probe Tomographic Analysis of Ge-Ge/Co/Mn"
Advisor: Prof. Lincoln Lauhon

The 2010 awards will be presented during the EMC Student Awards & Plenary Lecture on Wednesday, June 22 at 8:20 a.m. in the Corwin Pavilion.

NEW PROFESSIONAL HONOR...

Journal of ELECTRONIC MATERIALS

JEM Best Paper Award

TMS is accepting nominations for the *JEM* Best Paper Award.

The accolade will recognize outstanding scientific or engineering contributions to the *Journal of Electronic Materials*. Papers published in *JEM* from July 2010 through June 2011 are eligible. Nominations will be accepted from anyone, including the *JEM* editor and associate editors, through October 15, 2011. The final decision will be made by the Editorial Oversight Board, which is devoid of editors.

The winner will receive a waiver to attend either the TMS 2012 Annual Meeting or EMC 2012 to accept the award.

To nominate a paper, please submit a copy of the paper along with the nominator's letter of endorsement and recommendation to TMS Awards & Recognition, awards@tms.org.

This award is supported by *JEM* and the TMS Electronic, Magnetic & Photonic Materials Division.

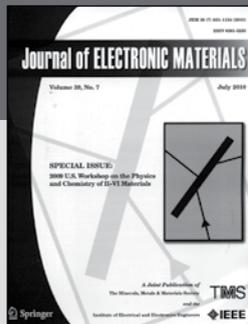
PROCEEDINGS/PUBLICATIONS

NEW for EMC 2011!

For the first time, *The Journal of Electronic Materials* (JEM) is asking presenters of the Electronic Materials Conference to submit manuscripts of their work for an all-EMC special issue containing all collected papers from the conference at: www.editorialmanager.com/jems/

All manuscripts will be peer-reviewed and must meet the same high standards for publication as regular papers.

The deadline for the all-EMC special issue is August 1, 2011.



About JEM

JEM is published monthly by The Minerals, Metals & Materials Society (TMS), the Institute of Electrical and Electronics Engineers (IEEE) and Springer Science + Business Media. Articles are reviewed, selected and edited by peers who serve as voluntary members of the editorial-board, associate editors, and guest editors. Editor-in-chief: Suzanne Mohnney

JEM Subscription

A special JEM issue will include manuscripts of papers presented at EMC. Individuals may subscribe to JEM by contacting Springer, the journal's publisher:

In North America

Telephone (800) 777-4643
E-Mail journals-ny@springer.com

Outside North America

Telephone (212) 460-1500 or
+49 (0) 6221-345-4303
E-mail subscriptions@springer.com

CONFERENCE ORGANIZERS

Energy Conversion & Storage Materials

This technical area was organized by the following individuals:

Photovoltaics: Organic and Hybrid

David Janes, Purdue University
Reuben Collins, Colorado School of Mines
David Gunlach, National Institute of Standards and Technology
Julia Hsu, Sandia National Laboratories
Peter Dinolfo, Rensselaer Polytechnic Institute

Highly Mismatched Dilute Alloys

Doug Hall, University of Notre Dame
Charles Tu, University of California – San Diego
Rachel Goldman, University of Michigan
Kin-Man Yu, Lawrence Berkeley National Laboratory
Thomas Kuech, University of Wisconsin

Next Generation Solar Cell Materials and Devices

Mark Goorsky, University of California-Los Angeles
Christian Wetzel, Rensselaer Polytechnic Institute
Jerry Woodall, Purdue University
Steve Ringel, Ohio State University
Debdeep Jena, University of Notre Dame

Thermoelectrics and Thermionics

Tim Sands, Purdue University
Pete Moran, Michigan Technical University
Mayank Bulsara, Massachusetts Institute of Technology
Joshua Zide, University of Delaware

Ionic Conductors for Solid Oxide Fuel Cells and Batteries

Pete Moran, Michigan Technical University
Alec Talin, National Institute of Standards and Technology
Jerry Woodall, Purdue University
Eric Wachsma, University of Maryland

Issues for Wide Bandgap Materials

This technical area was organized by the following individuals:

Group III-Nitrides: Growth, Processing, Characterization, Theory and Devices

Andrew Allerman, Sandia National Laboratory
Russ Dupuis, Georgia Institute of Technology
Mike Manfra, Purdue University
Huili Grace Xing, University of Notre Dame
Theeradetch Detchprohm, Rensselaer Polytechnic Institute
Thomas Myers, Texas State University

UV Detectors and Emitters: Materials and Devices

Debdeep Jena, University of Notre Dame
Jerry Woodall, Purdue University
Michael Wraback, U.S. Army Research Laboratory

Silicon Carbide: Growth, Processing, Characterization, Theory and Devices

Robert Stahlbush, Naval Research Laboratory
Mike Capano, Purdue University
Brett Hull, Cree, Inc.
Joshua Caldwell, Naval Research Laboratory
Michael Dudley, State University of New York at Stony Brook

Oxide Semiconductors: Growth, Doping, Defects, Nanostructures and Devices

Len Brillson, Ohio State University
Tom Jackson, Pennsylvania State University
Jamie Phillips, University of Michigan
John Conley, Oregon State University
Yicheng Lu, Rutgers University
Mike Gerhold, Army Research Laboratory

Indium Nitride: Growth, Processing, Characterization, Theory and Devices

Christian Wetzel, Rensselaer Polytechnic Institute
Joel Ager, Lawrence Berkeley Laboratory
Yasushi Nanishi, Ritsumeikan University
Debdeep Jena, University of Notre Dame

Point Defects, Doping and Extended Defects

Christian Wetzel, Rensselaer Polytechnic Institute
Andrew Armstrong, Sandia National Laboratory
James Speck, University of California-Santa Barbara
Jerry Woodall, Purdue University
Steve Ringel, Ohio State University
Eugene Fitzgerald, Massachusetts Institute of Technology

Nanoscale Science and Technology in Materials

This technical area was organized by the following individuals:

Graphene and Carbon Nanotubes

Huili Grace Xing, University of Notre Dame
Walt de Heer, Georgia Institute of Technology
Randall Feenstra, Carnegie Mellon University
Mike Spencer, Cornell University
Avik Ghosh, University of Virginia
Suneel Kodambaka, University of California-Los Angeles
Randy Sanhu, Northrup Grumman Space Technology

Nanotubes and Nanowires

Joan Redwing, Pennsylvania State University
William Wong, University of Waterloo
Suzanne Mohny, Pennsylvania State University
Kris Bertness, National Institute of Standards and Technology
Raymond Tsui, Raydis LLC
Cheng Yang, Purdue University

Low-Dimensional Structures: Quantum Dots, Wires and Wells

Jim Merz, University of Notre Dame
Akio Sasaki, Kyoto University of Japan
Ben Shanabrook, Naval Research Laboratory
Diana Huffaker, University of California-Los Angeles
Glenn Solomon, National Institute of Standards and Technology

Nanoscale Characterization: Scanning Probes, Electron Microscopy and Other Techniques

Ed Yu, University of Texas at Austin
Lincoln Lauhon, Northwestern University
Sarah Olsen, Newcastle University, UK
Suneel Kodambaka, University of California, Los Angeles

Molecular Electronics: Devices, Materials and Sensors

David Janes, Purdue University
Alec Talin, National Institute of Standards and Technology
Theresa Mayer, Pennsylvania State University

Enabling Technologies

This technical area was organized by the following individuals:

Metamaterials

Kitano Masao, University of Kyoto
Laura Rea, Air Force Research Laboratories
Jacob Khurgin, John Hopkins University
Sasha Boltasseva, Purdue University

Flexible and Printed Thin Film Electronics

Tom Jackson, Pennsylvania State University
William Wong, University of Waterloo
Thomas Kuech, University of Wisconsin
Oana Jurchescu, Wake Forest University

Organic Thin Film and Crystalline Transistors: Devices, Materials and Processing

Tom Jackson, Pennsylvania State University
Alberto Salleo, Stanford University
Michael Chabynyc, University of California-Santa Barbara
David Gundlach, National Institute of Standards and Technology
Oana Jurchescu, Wake Forest University

Nano-Magnetic, Magnetic Memory and Spintronic Materials

Ian Appelbaum, University of Maryland
Michael Flatte, University of Iowa
Xinyu Liu, University of Notre Dame
Shriram Ramanathan, Harvard University
Nitin Samarth, Pennsylvania State University
Masaaki Tanaka, University of Tokyo

Contacts to Semiconductor Epilayers, Nanowires, Nanotubes and Organic Films

Suzanne Mohny, Pennsylvania State University
Jerry Woodall, Purdue University
Martin Allen, University of Canterbury
Lisa Porter, Carnegie Mellon University
Tae-Yeon Seong, Korea University

Epitaxial Materials and Devices

Archie Homes, University of Virginia
Kurt Eyink, Air Force Research Laboratories
Kei-May Lau, Hong Kong University of Science and Technology
Alan Doolittle, Georgia Institute of Technology
Steve Ringel, Ohio State University
Christine Wang, MIT Lincoln Laboratory
Amy Liu, IQE, Inc.
Seth Bank, University of Texas-Austin
Charles Lutz, Kopin Corporation
Michael Tischler, OCIS Technology

Narrow Bandgap Materials and Devices

Bob Biefeld, Sandia National Laboratory
Ralph Dawson, University of New Mexico
Brian Bennett, Naval Research Laboratory
Partha Dutta, Rensselaer Polytechnic Institute
Ganesh Balakrishnan, University of New Mexico
Suman Datta, Pennsylvania State University

Nondestructive Testing and In Situ Monitoring and Control

Mark Goorsky, University of California-Los Angeles
Kurt Eyink, Air Force Research Laboratories

Semiconductor Processing: Oxidation, Passivation, and Etching

Suzanne Mohny, Pennsylvania State University
Doug Hall, University of Notre Dame
Maria Losurdo, CNR-IMIP

Materials Integration: Wafer Bonding and Engineered Substrates

Mark Goorsky, University of California-Los Angeles
Maria Losurdo, CNR-IMIP
Pete Moran, Michigan Technical University
Cindy Colinge, Tyndall National Institute
Eugene Fitzgerald, Massachusetts Institute of Technology
Karl Hobart, Naval Research Laboratory
James Lu, Rensselaer Polytechnic Institute

Oxide Thin Film Integration: Alternative Dielectrics, Epitaxial Oxides, Multifunctional Oxides, Superlattices and Metal Gates

Pat Lenahan, Pennsylvania State University
John Conley, Oregon State University
Evgeni Gusev, Qualcomm MEMS Technologies

Si-Based Heterojunctions

Sarah Olsen, Newcastle University, UK
Eugene Fitzgerald, Massachusetts Institute of Technology
Michael Tischler, OCIS Technology
Ya-Hing Xie, University of California-Los Angeles

Compound Semiconductor Growth on Si Substrates (Heteroepi on Si)

Eugene Fitzgerald, Massachusetts Institute of Technology
Steve Ringel, Ohio State University
Kei-May Lau, Hong Kong University of Science and Technology
Ralph Dawson, University of New Mexico
Jerry Woodall, Purdue University

ATTENTION STUDENTS!

Become a member of the Material Advantage student program for only \$25 and reap the benefits of affiliations with four varied materials organizations!

ACerS: *The American Ceramic Society*

AIST: *Association for Iron & Steel Technology*

ASM: *ASM International*

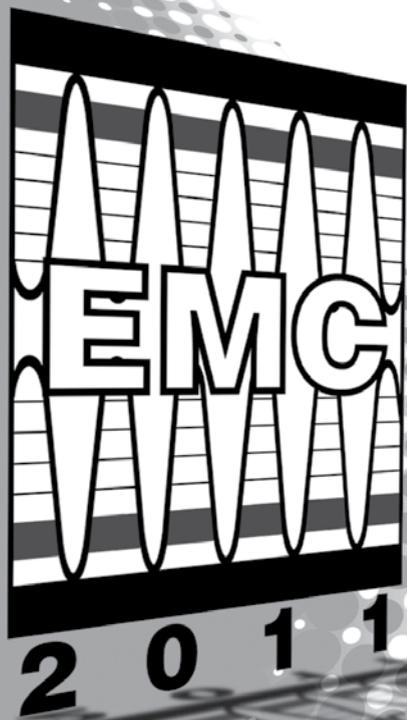
TMS: *The Minerals, Metals & Materials Society*

For full details on benefits, including scholarships and awards totaling more than \$600,000, visit: www.materialadvantage.org.

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**53rd
ELECTRONIC
MATERIALS
CONFERENCE
and EXHIBITION**

CONTENTS	PAGE
Sessions Listing.....	10
Sessions and Abstract Titles	20
Index.....	125

Session Listing

WEDNESDAY AM

EMC Student Awards and Plenary Lecture *Corwin Pavilion*

8:20 AM		Awards Ceremony
8:30 AM	Wladek Walukiewicz	New Concepts and Materials for Solar Power Conversion
9:20 AM		Break

Session A: III-Nitrides: MBE Growth *Flying A*

10:00 AM	K. Scott Butcher	A1, Nitride Film Growth by Migration Enhanced Afterglow (MEAglow)
10:20 AM	Michael Moseley	A2, Observation and Elimination of Indium Surface Segregation
10:40 AM	Wenyuan Jiao	A3, (Student) Depth Resolved Strain and Composition Studies on InGaN and AlInN Films Grown by Plasma-Assisted Molecular Beam Epitaxy
11:00 AM	Christophe Hurni	A4, (Student) Low Temperature p-GaN Grown by NH ₃ -MBE
11:20 AM	Craig Moe	A5, Epitaxial Lateral Overgrowth of Aluminum Nitride by Molecular Beam Epitaxy
11:40 AM	Jai Verma	A6, (Student) Effect of Superlattices and Surfactants on AlN Homoepitaxy by MBE

Session B: Thermoelectrics and Thermionics I *Lobero*

10:00 AM	Eric Toberer	B1, Phonon Engineering through Crystal Chemistry
10:40 AM	Alex Zevkink	B2, (Student) Ca ₃ AlSb ₃ and Ca ₃ Al ₂ Sb ₆ ; Inexpensive, Non-Toxic Thermoelectric Materials for Waste Heat Recovery
11:00 AM	Lakshmi Krishna	B3, The Impact of Nano-Inclusions Introduced by Mechanical Alloying on Thermoelectric Transport in Pb _{1-x} Sn _x Te: Experimental Results and Theoretical Predictions
11:20 AM	Aaron LaLonde	B4, Reevaluation of PbTe _{1-x} I _x as High Performance n-Type Thermoelectric Material
11:40 AM	Paothep Pichanusakorn	B5, The Universal Optimal Seebeck Coefficient for Maximum Power Factor

Session C: Nanoscale Characterization *Lotte Lehmann*

10:00 AM	Steven Hunt	C1, (Student) Scanning Gate Spectroscopy: A New SPM Technique for Nano-Devices on Oxide Surfaces
10:20 AM	Xuan-Dung Dang	C2, Measurement of Nanoscale External Quantum Efficiency of Plastic Solar Cells by Photoconductive Atomic Force Microscopy
10:40 AM	Yuya Murata	C3, Role of Ethylene on Thermal and Chemical Stability of TiO ₂ (110)
11:00 AM	Nadeemullah Mahadik	C4, Combined XSTM and High Resolution XRD Study for Quantitative Structural Descriptions of Type-II Superlattice IR Detectors
11:20 AM	Shu Hu	C5, (Student) In Situ Transmission Electron Microscopy and Photoluminescence Study of Ge-Core/SiGe-Shell Nanowires
11:40 AM	Ferran Ureña	C6, (Student) Local Strain Characterization of MEMS-Based Silicon Beams by Raman Spectroscopy



Plenary Speaker:

Wladek Walukiewicz

Lawrence Berkeley National Laboratory, Berkeley, California.

Title: "New Concepts and Materials for Solar Energy Conversion"

Summary: Efficient conversion of solar photons into other forms of energy has become one of the primary objectives of the modern science and technology. The core presentation will focus on methods to engineer the energy band structure of semiconductor materials for specific energy related applications.

This presentation was developed in collaboration with Solar Energy Materials Research Group and Supported by the Division of Materials Science and Engineering, U.S. Department of Energy.

Dr. Walukiewicz has been at Lawrence Berkeley National Laboratory in the Materials Sciences Division since 1984 and is currently a senior staff scientist and leader of the Solar Energy Materials Research Group. He also has served as the chief technical officer for RoseStreet Labs Energy since 2006. Walukiewicz is the recipient of the LBNL Technology Transfer Award in 2005, the R&D 100 Award in 2006 and has been a Fellow of the American Physical Society since 2007. Walukiewicz received his Ph.D. in Physics in 1974 and his Doktor Habilitat in Sciences in 1980 from the Institute of Physics of the Polish Academy of Sciences in Warsaw.

Session Listing

Session D: Plasmonics and Metamaterials *Multicultural Center Lounge*

10:00 AM	Yan Mui Kitty Yeung	D1, (Student) Tuning of Plasmonic Cavity Resonances Using Atomic Layer Deposition
10:20 AM	Naresh Das	D2, Tunable Infrared Absorption of Nano Plasmonic Structures
10:40 AM	Lirong Sun	D3, In Situ Spectroscopic Ellipsometric Analysis of Thin Silver Films Deposited Using DC Magnetron Sputtering and HiPIMS Techniques
11:00 AM	Akio Sasaki	D4, Second Harmonic Generation in a Metamaterial Resonating at Fundamental and Second Harmonic Frequencies
11:40 AM	Neil Murphy	D5, (Student) Optical Dispersion of Amorphous Germanium Thin Films as a Function of Thickness and Deposition Parameters
12:00 PM		D6, Late News

Session E: Organic, Printed and Flexible Electronics *Multicultural Center Theatre*

10:00 AM	Seonghoon Lee	E1, Quantum Dot Red/Green/Blue/White Light-Emitting Electroluminescent Devices with a Low Turn-on Voltage and High Brightness
10:20 AM	C. Doran	E2, (Student) Fabrication of Flexible Single-Crystal Devices on Electrically-Conductive Substrates
10:40 AM	Do Kyung Hwang	E3, A Compensation Mechanism for Flexible and Electrically Stable Solution-Processed Organic Field-Effect Transistors
11:00 AM	Dilek Isik	E4, Ambipolar Charge Carrier Transport in Organic Thin Films
11:20 AM	Shinyoung Park	E5, (Student) Application of Vapor Forms 1-Octanethiol Coated Copper Conductive Ink for Ink-Jet Printing
11:40 AM		E6, Late News

Session F: Devices Utilizing Low Dimensional Structures *Santa Barbara Harbor*

10:00 AM	Victor Patel	F1, (Student) Design and Growth of InAs Quantum Dash Based MWIR VECSELS
10:20 AM	Simon Huang	F2, (Student) Influence of Surface Patterning on Droplet Epitaxy and Photovoltaic Properties of InAs/GaAs Quatum Dots
10:40 AM	Supriya Karmakar	F3, (Student) Novel 3-State Quantum Dot Gate FET in Silicon-on-Insulator Substrate
11:00 AM	Yuncheng Song	F4, (Student) Visible Light Emitting Diodes Based on Self-Assembled In _{0.5} Ga _{0.5} As Quantum Dots on GaP
11:20 AM	Chun-Yung Chi	F5, (Student) Large Area Growth of GaAs Solar Cell Based on Nanowire Structure
11:40 AM	Yan Zheng	F6, (Student) Output Polarization Dependence of Asymmetric Current Injection VCSELS on Crystalline Direction and Ion Implantation

Session G: Photovoltaics: New Materials and Characterization *State Street*

10:00 AM	Jeffrey Bosco	G1, (Student) Molecular Beam Epitaxial Growth of Zn ₃ P ₂ /GaAs and ZnS/GaAs Heterostructures for Photovoltaics
10:20 AM	Lise Lahourcade	G2, ZnSnN ₂ : A New Earth-Abundant Semiconductor for Solar Energy Conversion
10:40 AM	Maqsood Ali Mughal	G3, (Student) Electrodeposition of Indium Sulfide Films from Organic Electrolytes
11:00 AM	Thomas Dufaux	G4, (Student) Spatially Resolved Responses of Nanoscale Photovoltaic Model Devices
11:20 AM	Jeffrey Lindemuth	G5, Challenges of Hall Measurements on Low Mobility Materials and How to Overcome Them
11:40 AM		G6, Late News

Conference Registration

The on-site registration desk in the University Center will be open beginning Tuesday afternoon and extending through Friday morning during the following hours:

Tuesday, June 21.....	3 to 5 p.m.
Wednesday, June 22.....	7:30 a.m. to 5 p.m.
Thursday, June 23.....	7:30 a.m. to 5 p.m.
Friday, June 24.....	7:30 to 10 a.m.

Session Listing

WEDNESDAY PM

Session H: III-Nitrides: Electronics I *Flying A*

1:30 PM	Vincent Lee	H1, (Student) Quantization and Bias Effects on Gate Capacitance of Scaled GaN HFETs
1:50 PM	Anup Sasikumar	H2, (Student) Direct Correlation between $E_c-0.57$ eV Trap Generation and Field-Induced Degradation in AlGaIn/GaN High Electron Mobility Transistors
2:10 PM	Erica Douglas	H3, (Student) Temperature Dependent Off-State Degradation of AlGaIn/GaN HEMTs
2:30 PM	Devin Rourke	H4, Noise Measurements of Nanowire FET Sensors for Sensitivity Determination
2:50 PM	Goutam Koley	H5, (Student) Piezoresistive Microcantilever with Embedded AlGaIn/GaN HFET for Sensing Applications
3:10 PM		Break
3:30 PM	Dan Denninghoff	H6, (Student) N-Polar GaN HEMTs Grown by MBE and MOCVD with fmax of 255 and 250 GHz, Respectively
3:50 PM	Pil Sung Park	H7, (Student) Flattened Transconductance (gm) in a Highly Scaled AlGaIn/GaN HEMT Using a Polarization-Induced 2D/3D Hybridized Channel Design
4:10 PM	Patrick Waltereit	H8, Fabrication of AlGaInN/GaN Transistors with ft and fmax Exceeding 100 GHz
4:30 PM	Stephen Kaun	H9, (Student) Effects of Threading Dislocation Density on the Gate Leakage of AlGaIn/GaN Heterostructures for High Electron Mobility Transistors
4:50 PM	Zachary Lochner	H10, (Student) Growth and Characterization of npn-GaN/InGaIn/GaN Double-Heterojunction Bipolar Transistors on a Free-Standing GaN Substrate

Session I: Thermoelectrics and Thermionics II *Lobero*

1:30 PM	Tsutomu Kanno	I1, A Tubular Thermoelectric Generator with Piled Conical Rings Structure
1:50 PM		I2, Late News
2:10 PM	Hong Lu	I3, Thermoelectric Properties of ErSb:In _x Ga _{1-x} Sb Thin Films Grown by MBE
2:30 PM	Peter Burke	I4, (Student) Nanoparticle Size Dependence of the Electrical, Thermal, and Optical Properties of Er-Doped In _{0.53} Ga _{0.47} As
2:50 PM	Laura Cassels	I5, (Student) Improving Thermoelectric Power Generation Efficiency with Epitaxial TbAs/III-V Nanocomposites
3:10 PM		Break
3:30 PM	Takehiro Onishi	I6, (Student) The MOCVD Growth of Erbium Antimonide Nanocomposite Embedded III-V Host Materials and Characterization for Thermoelectrics
3:50 PM	Pankaj Jha	I7, (Student) Cross-Plane Transport Properties of p-Type La _{0.67} Sr _{0.33} MnO ₃ /LaMnO ₃ Perovskite Oxide Metal/Semiconductor Superlattices
4:10 PM	Kejia Zhang	I8, Temperature-Dependent Thermal Properties of HgCdTe Superlattices
4:30 PM	Alexander Szein	I9, (Student) Development of III-Nitride Materials for Thermoelectric Applications
4:50 PM	Benjamin Curtin	I10, (Student) Highly Ordered Vertical Silicon Nanowire Arrays Embedded in Polymer for Thin-Film Thermoelectric Devices

Session J: Nanowire Transport and Devices *Lotte Lehmann*

1:30 PM	Seongmin Kim	J1, Molecular Surface Passivation Effects on Indium Oxide Nanowire Transistors
1:50 PM	Sheng Chu	J2, (Student) Electrically Pumped ZnO Nanowire p-n Junction Laser
2:10 PM	Ye Shao	J3, (Student) Electrical Transport Study of Schottky Barrier Based ZnO NanoWire FETs
2:30 PM	Jongwon Yoon	J4, (Student) ZnO Nanowire-Based Field Effect Transistors with Non-Volatile Memory Function Using Mobile Protons
2:50 PM	Lawrence Robins	J5, Raman and Electrical Probes of Carrier Concentration in Si-Doped GaN Nanowires Grown by Plasma-Assisted MBE
3:10 PM		Break
3:30 PM	Suprem Das	J6, (Student) Electrodeposited InSb Nanowires: Structural Properties and Transistor Performance
3:50 PM	Hanshuang Liang	J7, (Student) Electron Transport in One-Dimensional InAs Nanowire Transistors
4:10 PM	Christoph Gutsche	J8, Electrical Properties of Axial and Radial Nanowire pn-Junctions – A Comparison
4:30 PM	Hao Wu	J9, (Student) GaAs Core-Shell Nanowire-Based Vertical p-n Diodes
4:50 PM	Dongkyun Ko	J10, (Student) Role of Defect States in Charge Transport in Semiconductor Nanowires

Session Listing

Session K: Silicon Carbide Growth, Characterization and Devices *Multicultural Center Lounge*

1:30 PM	Brett Hull	K1, The Evolution of the SiC Power MOSFET from Lab Demonstration to Commercial Product
2:10 PM	David Spry	K2, A Bondable Metallization Stack that Prevents Diffusion of Oxygen and Gold into Monolithically Integrated Circuits Operating above 500 °C
2:30 PM	Lin Cheng	K3, High-Low Temperature Performance of 20 A, 1200 - 1700 V 4H-SiC Power MOSFETs
2:50 PM	Kunhwa Jung	K4, (Student) Improved Microstructure and Ohmic Contact of Nb Electrode on N-Type 4H-SiC
3:10 PM		Break
3:30 PM	Paul Klein	K5, Slow Thermal Emission from Traps in 4H-SiC Epilayers
3:50 PM	S. Byrappa	K6, (Student) Deflection of Threading Dislocations with Burgers Vector $c/c+a$ Observed in 4H-SiC Substrates and Axial Slices with Associated Stacking Faults
4:10 PM	Nadeemullah Mahadik	K7, Stacking Faults Originating from BPDs in High-Doped Buffer Layers
4:30 PM	Sabih Omar	K8, (Student) Step Controlled Epitaxy on 4° and 1° Off-Cut 4H and 6H-SiC Substrate Using Dichlorosilane
4:50 PM	Yu Zhang	K9, (Student) Defect Structures of $B_{12}As_2$ Single Crystalline Epitaxial Layers on Off-Axis (0001) 4H-SiC Substrates

Session L: Graphene Fabrication and Devices *Multicultural Center Theatre*

1:30 PM	Andras Kis	L1, Single-Layer MoS ₂ Transistors
2:10 PM	Youngki Yoon	L2, Role of Optical Phonon in Graphene Nanoribbon Tunnel Transistors: Strategy for Abrupt Switching from Material's Point of View
2:30 PM	W. S. Hwang	L3, Fabrication of Top-Gated Sub-10 nm Epitaxial Graphene Nanoribbon FETs Using Hydrogen Silsesquioxane (HSQ)
2:50 PM	Frank Tseng	L4, (Student) Semiconducting Graphene: Prospects and Challenges
3:10 PM		Break
3:30 PM	Takafumi Kamimura	L5, Influence of Trapped Single Charges in Single Walled Carbon Nanotube Transistor with SiN _x /Al ₂ O ₃ Double Wrapped Layers
3:50 PM	Mark Fanton	L6, Deposition and Characterization of AlN Dielectric Films on Graphene
4:10 PM	Chongmin Lee	L7, (Student) Graphene as a Heat-Spreading Layer in Blue LEDs
4:30 PM	Xuelei Liang	L8, RCA Clean Assisted Transfer of CVD Grown Graphene
4:50 PM	Jian Lin	L9, (Student) Electrical Property and Photoconductivity of Highly Dense and Vertically Aligned ZnO Nanowires Using Graphene as Electrodes

Session M: III-Nitrides: Defects and LEDs *Santa Barbara Harbor*

1:30 PM	Normand Modine	M1, A Defect-Based Mechanism for Efficiency Droop in Nitride Light Emitting Diodes
1:50 PM	Andrew Armstrong	M2, Impact of Extended and Point Defects on InGaN LED Efficiency
2:10 PM	Suk Choi	M3, (Student) Effect of In _x Al _{1-x} N Electron Blocking Layer on Quantum Efficiency in Visible Light-Emitting Diodes Grown by Metalorganic Chemical Vapor Deposition
2:30 PM	Roy Chung	M4, (Student) Semipolar AlGaN Buffers for Deep Ultraviolet Diode Lasers
2:50 PM	Andrew Allerman	M5, Low Dislocation Density Al _{0.32} Ga _{0.68} N by Overgrowth of Patterned Templates
3:10 PM		Break
3:30 PM	Jeomoh Kim	M6, (Student) Enhancement of Hole Transport and Carrier Distribution in InGaN/GaN Multiple Quantum Wells by Controlling Indium Content of p-Type Layer in Visible Light-Emitting Diodes
3:50 PM	Scott Newman	M7, P-Side-Down, Ga-Polar, Green-Emitting Single Heterostructure LEDs
4:10 PM	Christoph Stark	M8, Characterization of Green Semi-Polar (10-11) GaInN/GaN Light Emitting Diodes
4:30 PM	Vladimir Protasenko	M9, Optical Properties of Molecular Beam Epitaxy Grown High in Content (~20%) InGaN film Emitting in Green (540 nm)
4:50 PM	Yu Huang	M10, (Student) Effects of Dislocations on Luminescence in m-Plane InGaN Quantum Wells

Session N: Next Generation Solar Cell Materials and Devices *State Street*

1:30 PM	Masakazu Kobayashi	N1, Preparation of the Red Phosphor Nanoparticle Films for the Application to Silicon Solar Cells
1:50 PM	Giacomo Mariani	N2, (Student) GaAs Nanopillar Photovoltaics Based on Catalyst-Free Patterned Growth
2:10 PM	Nikholas Toledo	N3, (Student) Wafer Bonded GaAs-Sapphire for Photovoltaic Applications via Adhesive Bonding
2:30 PM	Senthil Sambandam	N4, Thin Film III-V Photovoltaics on Flexible Metal Substrates and Defect Mitigation Strategies
2:50 PM		N5, Late News
3:10 PM		Break
3:30 PM	Charles Teplin	N6, Towards >15% Solar Cells on Metal Foils: Heteroepitaxial Crystal Silicon on Alumina
3:50 PM	Jordan Lang	N7, (Student) High External Quantum Efficiency and Fill-Factor InGaN-Based Solar Cells Grown by NH ₃ -MBE
4:10 PM	James Nagel	N8, (Student) Design Principles for Light-Trapping in Thin Silicon Films with Embedded Dielectric Nanoparticles
4:30 PM	Li Bo	N9, (Student) Single Crystalline Si Substrate Growth by Lateral Diffusion LPE Technology for PV Applications

Session Listing

THURSDAY AM

Session O: III-Nitrides: UV Emitters and Detectors *Corwin East*

8:20 AM	Shrawan Jha	O1, Fabrication of UV Emitting Devices Using Vertical ZnO Nanorod Arrays on the p-GaN Films
8:40 AM	Jieying Kong	O2, Low-Threshold ZnO Random Laser Diode Realized by Double Heterojunction Structure
9:00 AM	Gema Tabares	O3, (Student) ZnMgO-Based Photodetectors for Short Wavelength and Light Polarization Detection
9:20 AM	Ramón Collazo	O4, Fabrication and Characterization of 265 nm Light Emitting Diodes on AlN Single Crystal Substrates
9:40 AM	Gregory Garrett	O5, Time-Resolved Photoluminescence of AlInN/AlN Multiple Quantum Well Active Regions for Mid-UV Emitters
10:00 AM		Break
10:20 AM	Sriram Krishnamoorthy	O6, (Student) Enhanced Inter-Band Tunneling by Polarization Engineering in InGaN/GaN Quantum Wells
10:40 AM	Chad Gallinat	O7, Effects of Polarization Interface Charge on GaN/SiC Separate Absorption and Multiplication Avalanche Photodiodes
11:00 AM	Matthew Laurent	O8, Low-Temperature Growth and Characterization of p-GaN and Graded p-InGaN Layers by MOCVD for Photovoltaic Applications
11:20 AM	Animesh Banerjee	O9, (Student) Carrier Lifetimes and Recombination Phenomena in InGaN/GaN Quantum Dot and Quantum Well LEDs: A Comparative Study
11:40 AM	Mary Miller	O10, Characterization of Ultraviolet LEDs by Electrical Analysis and Laser-Based Failure Analysis Techniques

Session P: Oxide Semiconductor Devices *Corwin West*

8:20 AM	Matthew Pickett	P1, Memristance and Current-Driven Phase Transition in Multifunctional Binary Oxide Nanodevices
9:00 AM	Jing Qi	P2, Switching Characteristics and Mechanism of Nano-Scale Memristors Based on Epitaxial ZnO Nano-Islands
9:20 AM	Stefan Müller	P3, (Student) Investigation of Multi-Barrier ZnO-Schottky Contacts
9:40 AM	Jeffrey Siddiqui	P4, (Student) Interface Charge Characteristics of HfO ₂ /ZnO Thin Films
10:00 AM		Break
10:20 AM	Michael Lorenz	P5, (Student) Low-Temperature Processed Schottky-Gated Field-Effect Transistors Based on Amorphous Gallium-Indium-Zinc-Oxide
10:40 AM	Se-I Oh	P6, (Student) High Pressure Hydrogen Annealing of Indium-Gallium-Zinc Oxide Thin Film Transistors
11:00 AM	Chieh-Jen Ku	P7, (Student) The Effect of Ga Doping on Bias Stress Stability of ZnO TFT
11:20 AM	Jungbae Kim	P8, Electrically Stable Amorphous InGaZnO Thin-Film Transistors and High-Gain Inverters
11:40 AM	Kathryn Greenberg	P9, (Student) Growth and Investigation of Hexagonal Zinc Oxide Microdisk Resonators

Session Q: III-Nitrides: Electronics II *Flying A*

8:20 AM	Satyaki Ganguly	Q1, (Student) ALD Al ₂ O ₃ Thickness-Dependent Study of AlN/GaN MOS-HEMTs
8:40 AM	Seshadri Kolluri	Q2, (Student) Al ₂ O ₃ Based Etch-Stop Technology for the Gate Recess in N-Polar AlGaIn/GaN MIS-HEMTs with Si _x N _y Passivation
9:00 AM	Jia Guo	Q3, (Student) MBE Regrown Ohmic Contacts with Rc of 0.15 ohm-mm in InAlN/GaN High Electron Mobility Transistor
9:20 AM	Hyeongnam Kim	Q4, Pre- and Post-Treatment Investigations of Al Oxide by Atomic Layer Deposition in Schottky Metal/Al Oxide/AlGaIn/GaN MOS Diodes
9:40 AM	Edwin Piner	Q5, GaN/Diamond AlGaIn/GaN/AlGaIn DH-HEMT Produced by Epi-Inverted Wafer Processing
10:00 AM		Break
10:20 AM	Daniel Billingsley	Q6, Al _x In _{1-x} N/GaN Heterostructures Grown by MEMOCVD
10:40 AM	Digbijoy Nath	Q7, (Student) Lateral Confinement of Electrons and Quasi-1D Channels Based Devices
11:00 AM	Hyeongnam Kim	Q8, Polarization-Engineered GaN-Based Heterostructure for Normally-Off High-Electron Mobility Transistors
11:20 AM	Peter Kordos	Q9, Tunneling Current via Dislocations in AlGaIn/GaN Schottky Contacts
11:40 AM	Benjamin Reuters	Q10, (Student) Growth Studies on Quaternary AlInGaIn Layers for HEMT Application

Session R: Narrow Bandgap Materials and Devices *Lobero*

8:20 AM	Maya Narayanan Kuttu	R1, (Student) Improved Performance of Long-Wave Infrared InAs/GaSb Strained Layer Superlattices Detectors by Novel ZnTe Passivation
8:40 AM	Jae-Hyun Ryou	R2, Strain-Engineered Binary and Ternary Type-II Superlattice Structures and Photodiodes Grown by Metalorganic Chemical Vapor Deposition
9:00 AM	Ding Wang	R3, (Student) Study of Minority Carrier Lifetime and Background Carrier Concentration in GaSb-InAs Strained-Layer Superlattices and Bulk Epitaxial Layers by Optical Modulation Response
9:20 AM	Corey Shemelya	R4, (Student) Increased Thermophotovoltaic Efficiencies Using a Two Dimensional Photonic Crystal Cavity
9:40 AM	Patrick Hopkins	R5, Effect of Dislocation Density on Thermal Boundary Conductance across GaSb/GaAs Interfaces
10:00 AM		Break
10:20 AM	Ashish Agrawal	R6, (Student) Low Field Electron Transport in Mixed Arsenide Antimonide Quantum-Well Heterostructures
10:40 AM	Siyuan Gu	R7, (Student) AlGaSb/InAs-Based Staggered Heterojunction Tunnel Diodes
11:00 AM	Stephen Clark	R8, (Student) Growth and Characterization of AlInSb Metamorphic Buffers on GaSb and GaAs Substrates for the Growth of MWIR Lasers
11:20 AM	Richard Moug	R9, Optimization of MBE Growth for the Development of Mid-IR II-VI Quantum Cascade Lasers
11:40 AM	P. Ahirwar	R10, (Student) Growth of III-Sb VECSELS for High-Power Continuous Wave Operation

Session Listing

Session S: Nanowire Synthesis and Characterization *Lotte Lehmann*

8:20 AM	Steven Palefsky	S1, (Student) Photoluminescence of Chemical Vapor Deposition-Grown Diamond Nanowires
8:40 AM	Trevor Buehl	S2, (Student) Properties of ErAs and ErSb Nanorods Embedded in High-Index III-V Semiconductors
9:00 AM	Santino Carnevale	S3, (Student) Dynamic Control of Growth Kinetics for Three-Dimensional Semiconductor Nano-Heterostructures
9:20 AM	Joshua Shapiro	S4, (Student) Structural Characterization of InGaAs Axial Inserts in GaAs Catalyst-Free Nanopillars Grown by Selective-Area MOCVD
9:40 AM	Simon Watkins	S5, Control of III-V Nanowire Epitaxy by Precursor Chemistry
10:00 AM		Break
10:20 AM	Jiebin Zhong	S6, (Student) Temperature-Dependent Growth Direction of Epitaxial InSb Nanowires by Chemical Vapor Deposition
10:40 AM	Suneel Kodambaka	S7, (Student) Effect of Precursor Flow Rates on the Growth of InPSb Nanowires on InP(111)B
11:00 AM	Aric Sanders	S8, Precise Placement and Diameter Control of Catalyst-Free Molecular Beam Epitaxy Grown GaN Nanowires
11:20 AM	Ebraheem Azhar	S9, (Student) Synthesis and Fabrication of ZnTe Nanosheet Field Effect Transistors for Photonic Applications

Session T: Growth of Graphene and Carbon Nanotubes *Multicultural Center Theatre*

8:20 AM	Michael Bolen	T1, (Student) Epitaxial Graphene Formation on Step-Free 4H-SiC(0001)
9:00 AM	Mark Fanton	T2, Effects of Substrate Orientation and Growth Environment on the Structural and Electronic Properties of Epitaxial Graphene on SiC(0001)
9:20 AM	Mark Fanton	T3, High Mobility Epitaxial Graphene on Sapphire via Metal-Free CVD
9:40 AM	Biplob Daas	T4, (Student) Study of Epitaxial Graphene on Non-Polar 6H-SiC Faces
10:00 AM		Break
10:20 AM	Maziar Ghazinejad	T5, (Student) Synthesis of a Pillared Graphene Nanostructure: A Three-Dimensional Hybrid Carbon Architecture
10:40 AM	Kevin Daniels	T6, (Student) Electrochemical Graphane Conversion Using E-beam Evaporated Metals for Catalytic Enhancement
11:00 AM	Yohei Yagishita	T7, Highly Reproducible Growth of Carbon Nanotubes for Practical Applications in Electronics
11:20 AM	Bruce Willner	T8, Graphene and Carbon Nanotube Growth in Vacuum Systems

Session U: Highly Mismatched Alloys *Santa Barbara Harbor*

8:20 AM	Ashish Bhatia	U1, (Student) Synthesis of $\text{Ge}_{(1-x)}\text{Sn}_x$ Alloy Thin Films Using Ion-Implantation and Pulsed Laser Melting (II-PLM)
8:40 AM	Holger Eisele	U2, Nitrogen Ordering in Ga(NAs) at the Atomic Scale
9:00 AM	Nimai Patra	U3, (Student) A Study of MBE Grown $\text{InSb}_{1-x}\text{N}_x$ on GaAs for Long-Wavelength IR Applications
9:20 AM	Alejandro Levander	U4, (Student) Highly Mismatched $\text{GaN}_{1-x}\text{As}_x$ Alloys across the Entire Composition Range
9:40 AM	Ding Wang	U5, (Student) Band Edge Optical Transitions in Bulk GaSbN and InAsN Dilute-Nitride Materials
10:00 AM		Break
10:20 AM	Paothep Pichanusakorn	U6, (Student) Non-Monotonic Change/Variation in the Seebeck Coefficient of $\text{GaAs}_{1-x}\text{N}_x$ Thin Film Thermoelectrics Due to the Addition of N ($x = 0.5\%$ to 1.5%)
10:40 AM	Alejandro Levander	U7, (Student) $\text{GaN}_{1-x}\text{Bi}_x$: Extremely Mismatched Alloys
11:00 AM	Pernell Dongmo	U8, (Student) Electrical and Thermal Properties of $\text{InGaBi}_x\text{As}_{1-x}$
11:20 AM	Ryan France	U9, Incorporation of Bismuth into GaAs and InAs Grown by Molecular-Beam Epitaxy
11:40 AM	Marie Mayer	U10, (Student) Highly Mismatched Oxide Alloy for Photovoltaic and Photoelectrochemical Applications

Session V: Organic Photovoltaics and Photoelectrochemical Cells *State Street*

8:20 AM	Reuben Collins	V1, Alkanethiol Island Formation on Single Crystal Zinc Oxide Surfaces
9:00 AM	Jung Hwa Seo	V2, Improved High Efficiency Organic Solar Cells via Incorporation of a Conjugated Polyelectrolyte Interlayer
9:20 AM	Bright Walker	V3, (Student) A Systematic Approach to Solvent Selection Based on Cohesive Energy Densities in a Molecular Bulk Heterojunction System
9:40 AM	Jason Lin	V4, (Student) Structure-Function-Property Relationships of Diketopyrrolopyrrole-Based Materials for Applications in Solution Processed Organic Solar Cells
10:00 AM		Break
10:20 AM	Yi Wei Chen	V5, (Student) ALD- TiO_2 to Enable Si as a Corrosion Resistant Photoelectrode for Water Oxidation and in Photoelectrochemical Solar Cells
10:40 AM	Alireza Kargar	V6, Performance Optimization of Branched Nanowire Heterostructure-Based Photoelectrochemical Cells for Water Solar Splitting
11:00 AM	Peter Dinolfo	V7, Layer-By-Layer Assembly of Light Harvesting Arrays for Molecular Based Solar Cells
11:20 AM	Gede Adhyaksa	V8, (Student) Low Temperature Fabrication of Hybrid Carbon Nanotube Gel as a Counter Electrode for Efficient Dye Sensitized Solar Cells

Session Listing

THURSDAY PM

Session W: III-Nitride: Bulk Growth and Epitaxy *Corwin East*

1:30 PM	Christopher Yerino	W1, (Student) Shape Transformation of Nanoporous GaN by Annealing: Buried Cavities and Nanomembranes
1:50 PM	Siddha Pimputkar	W2, (Student) Bulk GaN Growth on GaN Seeds of Varying Orientations in Supercritical Basic Ammonia
2:10 PM	Yu Zhang	W3, (Student) Large-Area, Free Standing GaN by an Novel Nanoetching Process and Substrate Recycling
2:30 PM	Cyrus Dreyer	W4, (Student) Effect of Strain on Effective Masses in GaN and AlN
2:50 PM	Benjamin Bryant	W5, (Student) Quasi Equilibrium Crystal Shapes and Kinetic Wulff Plots of Gallium Nitride Grown by Hydride Vapor Phase Epitaxy
3:10 PM		Break
3:30 PM	Jarod Gagnon	W6, (Student) In Situ Stress Measurements during GaN Growth on Ion Implanted AlN/Si Substrates
3:50 PM	Dongjin Won	W7, (Student) Effect of Indium Surfactant on N-Polar GaN Epilayers Grown by Metalorganic Chemical Vapor Deposition
4:10 PM	James Tweedie	W8, (Student) Schottky Barrier Height and Interface Chemistry for Metals Contacted to Low Dislocation Density AlGaIn Grown on C-Oriented AlN Wafers
4:30 PM	Hironori Okumura	W9, (Student) Generation Mechanism of Threading Dislocations in Heteroepitaxial Growth of 2H-AlN on 6H-SiC (0001) Substrates
4:50 PM	Eunjung Cho	W10, Impact of AlN Wetting Layer on the Strain Development in GaN Layer Grown on Chemical Mechanical Polished 4H - SiC Substrates

Session X: Oxide Thin Films *Corwin West*

1:30 PM	Andrew Carter	X1, (Student) Gate First $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{Al}_2\text{O}_3$ MOSFETs with In-Situ Channel Surface Cleaning
1:50 PM	Corey Cochrane	X2, (Student) Structure of Electronic Defects near the SiC/SiO ₂ Interface
2:10 PM	Ramya Yeluri	X3, Interface State Density for Positive Band Offset Dielectrics (Al_2O_3 , SiO_2) on GaN
2:30 PM	Gregory Burek	X4, (Student) Comparison of Metal Deposition Methods by CV Analysis of ALD Al_2O_3 on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$
2:50 PM	Guangle Zhou	X5, (Student) Passivation Effects of ALD Oxides on Self-Aligned $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InAs}/\text{InP}$ Vertical Tunnel FETs
3:10 PM		Break
3:30 PM	Yoontae Hwang	X6, (Student) Influence of Trimethylaluminium (TMA) Exposure on the Growth and Electrical Characteristics of $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ Gate Stacks
3:50 PM	Nasir Alimardani	X7, (Student) Investigation of Electrode Roughness and High-K Dielectric Barrier on Metal-Insulator-Metal Tunnel Diode Operation
4:10 PM	Peter Lam	X8, Co-Sputtering of Barium Strontium Titanate (BST) and Barium Oxide-Boron Oxide Flux ($\text{BaO-B}_2\text{O}_3$) for Thin Film Applications
4:30 PM	Chen-Guan Lee	X9, (Student) Solution-Processed Zirconium Oxide and Integration with Zinc-Tin Oxide Thin-Film Transistors
4:50 PM	Nick Sbrockey	X10, Epitaxial $\text{LaAlO}_3/\text{SrTiO}_3$ Heterostructures by Atomic Layer Deposition

Session Y: Point, Defects, Doping and Extended Defects *Flying A*

1:30 PM	Tania Henry	Y1, The Influence of Al Composition on AlGaIn Point Defect Incorporation
1:50 PM	Luke Gordon	Y2, (Student) Hybrid Functional Calculations of DX Centers in AlN, GaN and AlGaIn
2:10 PM	Zeng Zhang	Y3, (Student) Deep Traps in M-Plane GaN Grown by Ammonia MBE
2:30 PM	Holger Eisele	Y4, Intrinsic Surface States and Dislocations at GaN(10-10) Surfaces Investigated by Scanning Tunneling Microscopy
2:50 PM	Emre Gur	Y5, Defect Characterization of InGaIn Layer by Deep Level Transient and Optical Spectroscopies
3:10 PM		Break
3:30 PM	Po Shan Hsu	Y6, (Student) Misfit Dislocation Formation in Partially Strain-Relaxed (11-22) Semipolar InGaIn
3:50 PM	Matthew Hardy	Y7, (Student) Observation of m-Plane Slip and Relaxation Orthogonal to the Projected c-Direction in (20-21) InGaIn/GaN Partially Relaxed Layers
4:10 PM	Vishwanath Sarkar	Y8, (Student) Stress Mapping Analysis by Ray Tracing (SMART): A New Technique for Residual Strain/Stress Measurement of Single Crystal Material Using Synchrotron White Beam
4:30 PM	Aniruddha Konar	Y9, (Student) Charged Basal Stacking Fault (BSF) Scattering in Wide Band-Gap Semiconductors
4:50 PM	Reid Juday	Y10, (Student) Hydrogen-Related Cathodoluminescence in Mg-Doped GaN

Session Z: Epitaxial Materials and Devices I *Lobero*

1:30 PM	Adam Crook	Z1, (Student) Growth of Epitaxially-Embedded ErAs Films in GaAs
1:50 PM	Rodolfo Salas	Z2, (Student) Improved Conductivity of GaAs-Based Tunnel Junctions Containing ErAs Nanostructures via Compositional Grading
2:10 PM	Robert Chen	Z3, (Student) Photoluminescence from the Direct Bandgap of $\text{Ge}_{1-x}\text{Sn}_x$ Alloys Grown by Molecular Beam Epitaxy
2:30 PM	Seongjae Cho	Z4, Fabrication and Characterization of Whispering Gallery Mode (WGM) Microdisk Resonator Based on Epitaxially Grown GeSn
2:50 PM	Hai Lin	Z5, (Student) Raman Study of Strained $\text{Ge}_{1-x}\text{Sn}_x$ Alloys
3:10 PM		Break
3:30 PM	Gregory Brill	Z6, Study of Molecular Beam Epitaxial Grown HgCdSe for Infrared Applications
3:50 PM	Keita Ito	Z7, (Student) XMCD Measurement of Molecular Beam Epitaxy $\gamma\text{-Fe}_2\text{N}$ Thin Films on $\text{LaAlO}_3(100)$ and $\text{MgO}(100)$ Substrates
4:10 PM	Ryan France	Z8, Sb Surfactant Use during GaInP and GaInAs Strain Relaxation
4:30 PM	Denzil Roberts	Z9, (Student) Sensitivity of Strained and Unstrained Structure Growth on GaAs (111)B
4:50 PM	Xiuling Li	Z10, Ternary $\text{In}_x\text{Ga}_{1-x}\text{As}$ Nanowires on Silicon Substrates: 1D Heterogeneous Epitaxy, Bandgap Engineering, and Photovoltaics

Session Listing

Session AA: Four Dots and a Dash *Lotte Lehmann*

1:30 PM	Paul Simmonds	AA1, Self-Assembled, Tensile-Strained III-V Islands on (110) and (111)A Substrates
1:50 PM	Andrea Lenz	AA2, Atomic Structure of InAs/InGaAsP/InP(001) Quantum Dashes and Decomposition of the InGaAsP Matrix Material
2:10 PM	Bor-Chau Juang	AA3, (Student) Photoluminescence and Thermal Carrier Activation in Type-II ZnTe/ZnSe Quantum Dots
2:30 PM	Nahid Jahan	AA4, (Student) Temperature Dependent Photoluminescence of Ensemble and Single InAs/InGaAlAs Quantum Dots
2:50 PM	Holger Eisele	AA5, Atomic Structure and Optical Properties of Submonolayer InAs/GaAs Depositions
3:10 PM		Break

Session BB: Fundamentals of Low-Dimensional Structures *Lotte Lehmann*

3:30 PM	Jason Kawasaki	BB1, (Student) Local Density of States and Semimetallic Behavior of Rare Earth-V Nanoparticles Embedded in a III-V Semiconductor Matrix
3:50 PM	John Petropoulos	BB2, (Student) A Simple Thermodynamic Model for the Doping and Alloying of Nanoparticles
4:10 PM	Nahid Jahan	BB3, (Student) Band Structure and Thermal Escape Processes of Strained InGaSb/AlGaSb Quantum Wells
4:30 PM	Kevin Grossklaus	BB4, (Student) Formation and Templating of III-V Semiconductor Nanospikes by Focused Ion Beams
4:50 PM	Rahul Makhijani	BB5, (Student) A Detailed Temperature-Dependent Photoluminescence Investigation into the Growth Pause Induced Ripening of InAs/GaAs Quantum Dot Heterostructures

Session CC: Graphene Characterization and Applications *Multicultural Center Theatre*

1:30 PM	Yuya Murata	CC1, In Situ High-Temperature Scanning Tunneling Microscopy Studies of Graphene Growth on 6H-SiC(0001)
1:50 PM	Travis Anderson	CC2, Electrical Characterization of Graphene-Semiconductor Heterojunctions
2:10 PM	Mohammad Nomani	CC3, (Student) Correlated Conductivity and Work Function in Epitaxial Graphene
2:30 PM	Mark Fanton	CC4, Response of Graphene-Based Field Effect Devices Exposed to Gamma and Neutron Irradiation
2:50 PM	Shamaita Shetu	CC5, (Student) Surface Adsorption and Charge Transport in Epitaxial Graphene on 6H-SiC
3:10 PM		Break
3:30 PM	Khan Shahil	CC6, (Student) Graphene Reinforced Composites as Efficient Thermal Interface Materials
3:50 PM	Berardi Sensale-Rodriguez	CC7, (Student) Frequency Domain THz Characterization of Graphene
4:10 PM	Bo Gao	CC8, Charge Carrier Dynamics in Graphene: Suspended vs. Supported
4:30 PM	Bjplob Daas	CC9, (Student) Polariton Enhanced IR-Reflectivity of Epitaxial Graphene on SiC
4:50 PM	Jennifer Reiber Kyle	CC10, (Student) CVD Graphene Metrology with Fluorescence

Session DD: Nano-Magnetic, Magnetic Memory and Spintronic Materials *Santa Barbara Harbor*

1:30 PM	Wei Han	DD1, (Student) Enhanced Spin Injection and Spin Lifetimes in Graphene
1:50 PM	Elizabeth Golovatski	DD2, (Student) Enhancement of Spin Torque by Proximity to Other Domain Walls
2:10 PM	Kurtis Wickey	DD3, (Student) Spin Seebeck Effect in MnAs/GaMnAs Bilayers
2:30 PM	Shinobu Ohya	DD4, Universal Valence-Band Picture of the Ferromagnetic Semiconductor GaMnAs Obtained by the Resonant Tunneling Spectroscopy
2:50 PM	Paul Riechers	DD5, (Student) Fe ₃ O ₄ /GaAs Hybrid Ferromagnet/Semiconductor Nanostructures
3:10 PM		Break
3:30 PM	J. Leiner	DD6, (Student) Magnetic Depth Profile of Mn-Graded (Ga,Mn)As
3:50 PM	Petra Reinke	DD7, Manganese-Doping of Group IV Semiconductor Surfaces and Nanostructures
4:10 PM	Laura Steren	DD8, Unexpected Exchange-Bias Effect at Paramagnetic/Ferromagnetic Interfaces in Oxide-Based Structures
4:30 PM	Yota Takamura	DD9, (Student) Formation of Half-Metallic Ferromagnet Tunnel Junctions of Co ₂ FeSi/SiO _x N _y /Si Using Radical Oxynitridation Technique
4:50 PM	Mitsuhiro Satoh	DD10, (Student) Characterization of L2 ₁ -Ordered Full-Heusler Co ₂ FeSi _{1-x} Al _x Alloy Thin Films Formed by Silicidation Technique Employing Silicon-on-Insulator Substrate

Session EE: Organic Thin Film and Crystalline Transistors: Devices and Materials *State Street*

1:30 PM	Jonathan Rivnay	EE1, (Student) Quantitative Analysis of Lattice Disorder and Crystallite Size in Organic Semiconductor Thin Films, and Implications for Charge Transport
1:50 PM	Louisa Brown	EE2, (Student) Following Charge-Trapping Chemical Reactions in Pentacene Films by Selective Chemical Doping and Wavelength-Resolved Electric Force Microscopy
2:10 PM	Frederik Ante	EE3, (Student) Molecular Contact Doping for Organic n-Channel TFTs and Fast Complementary Circuits
2:30 PM	Rodrigo Noriega	EE4, (Student) Charge Trapping and Localization Due to Paracrystalline Disorder in High Performance Polymeric Semiconductors
2:50 PM	Justin Cochran	EE5, (Student) Probing the Microstructure of Buried Polymer-Polymer Interfaces with Thin Film Transistors
3:10 PM		Break
3:30 PM		EE6, Late News
3:50 PM	Hagen Klauk	EE7, Materials Requirements for Low-Voltage Flexible Organic Transistors and Circuits
4:30 PM	Martin Burkhardt	EE8, Organic Transistor-Based Memory
4:50 PM	Jeremy Ward	EE9, (Student) From Nano- to Micro-Scale Control of Crystalline Order in Soluble Small-Molecule Organic Semiconductors

Session Listing

FRIDAY AM

Session FF: Epitaxy Material and Devices II *Corwin East*

8:20 AM	Wayne Johnson	FF1, n+GaAs Sheet Resistance Saturation and Implications to BiHEMT Growth
8:40 AM	Yan Gao	FF2, (Student) Metamorphic p-i-n InGaAs Photodetectors Grown by MOCVD
9:00 AM	Jiayi Shao	FF3, (Student) Optimized Growth Condition and Dot Geometry in InAs/InGaAs Sub-Monolayer Quantum Dot Infrared Photodetector
9:20 AM	Jae-Hyun Ryou	FF4, Epitaxial Growth of InGaAs/InAlAs/InP Quantum Cascade Lasers by Metalorganic Chemical Vapor Deposition
9:40 AM	Tomas Sarmiento	FF5, (Student) GaInNAsSb Quantum Wells with Strain-Compensating GaAsP Layers for GaAs-Based 1.55 μm Lasers
10:00 AM		Break

Session GG: III-Nitrides: Non-Polar and Semi-Polar Devices *Corwin East*

10:20 AM	Yuji Zhao	GG1, (Student) Highly Polarized Spontaneous Emission from Semipolar (20-2-1) InGaN/GaN Light-Emitting Diodes
10:40 AM	Liang Zhao	GG2, (Student) Characterization of Green Semipolar (20-21) GaInN/GaN Multiple Quantum Well Light-Emitting Diodes Grown on Freestanding GaN Substrate
11:00 AM	Benjamin Leung	GG3, (Student) Optical Emission Patterns in Semipolar (11-22) GaN Light Emitting Diodes on Planar m-Plane and Etched r-Plane Sapphire
11:20 AM	Sebastian Metzner	GG4, (Student) Microscopic Optical Properties of Semi-/Nonpolar GaN with InGaN SQWs on Top Grown Directly on Patterned Si Substrate
11:40 AM	Ingrid Koslow	GG5, (Student) Strain Relaxation in Semipolar Nitrides for Optoelectronic Device Applications

Session HH: Oxide Semiconductors: Growth, Doping and Defects *Corwin West*

8:20 AM	Stephan Lany	HH1, Surface Donors Dominate the Conductivity of In_2O_3 Thin Films
8:40 AM	Daniel Doutt	HH2, (Student) The Role of Native Point Defects in Highly n-Type Degenerate (Zn,Ga)O Films
9:00 AM	Simon Watkins	HH3, High Resolution Photoluminescence Spectroscopy of Donors in Undoped and Indium-Doped ZnO Grown by Metalorganic Vapor Phase Epitaxy
9:20 AM	Knut Erik Knutsen	HH4, (Student) Trap-limited Li diffusion in melt grown ZnO
9:40 AM	Zhichun Zhang	HH5, (Student) Identification of Acceptor States in Li Doped ZnO Using Nanoscale Depth-Resolved Cathodoluminescence Spectroscopy
10:00 AM		Break
10:20 AM	Jizhi Zhang	HH6, Zn(Mg,Cd)O Epitaxy for Optoelectronic Applications
10:40 AM	Yuanyuan Li	HH7, (Student) ZnO and Al_2O_3 Thin Films Deposited by Plasma Enhanced Atomic Layer Deposition and Plasma Enhanced Chemical Vapor Deposition
11:00 AM	Juhung Yun	HH8, (Student) Thin Films of ZnO Prepared by Reactive Pulsed Arc Molecular Beam Deposition
11:20 AM	Patrick Kung	HH9, Atom Probe Tomography of ZnO Nanowires
11:40 AM	Junyi Zhu	HH10, Strain: A New Strategy of Tuning Doping Site and Type in Semiconductors

Session II: Intersubband Devices: AlInN and InGaN Materials Characterization *Flying A*

8:20 AM	Philipp Ebert	II1, Absence of Electron Accumulation at InN(11-20) Cleavage Surfaces
8:40 AM	Liang Tang	II2, (Student) MBE Growth Study of AlInN and AlInN/GaN Heterostructures for Intersubband Device Applications
9:00 AM	Colin Edmunds	II3, Room Temperature near-Infrared AlInN/GaN and AlGaIn/GaN Quantum Well Photodetectors Grown by Molecular Beam Epitaxy
9:20 AM	Wei Kong	II4, (Student) Characterization of Lateral and Vertical Inhomogeneities in InAlN Grown by Plasma-Assisted Molecular Beam Epitaxy
9:40 AM	Alexander Woolf	II5, (Student) Electrical Tuning of InGaN Quantum Dots in GaN Photonic Crystal Cavities
10:00 AM		Break
10:20 AM	David Browne	II6, (Student) Investigation of Indium and Impurity Incorporation of InGaN Films on Polar, Nonpolar, and Semipolar GaN Orientations Grown by Ammonia MBE
10:40 AM	Adrian Bayraktaroglu	II7, (Student) Piezoresponse Force Microscopy of InGaN/GaN Quantum Dots
11:00 AM	Ting-Wei Yeh	II8, (Student) InGaN/GaN Core-Shell Nanorod Arrays Grown by Selective Area Growth for InGaN-Based Light Emitting Diodes
11:20 AM	Ke Wang	II9, Molecular Beam Epitaxial Growth and Characterization of InN Nanocolumns on GaN Templates
11:40 AM	Elias Warde	II10, Vertical Transport in GaN/AlGaIn Resonant Tunneling Diodes and Superlattices

Session JJ: Compound Semiconductor Growth on Silicon Substrates *Lobero*

8:20 AM	Bernardette Kunert	JJ1, Growth Investigations of Lattice-Matched III/V Compound Materials on (001) Si Substrate for Optoelectronics
9:00 AM	Nicholas Julian	JJ2, (Student) Coalescence Phenomena in Narrow-Angle Stripe Epitaxial Lateral Overgrown InP by MOCVD
9:20 AM	Phil Magee	JJ3, Growth Habit Control of Epitaxial Lateral Overgrown InP on Si Substrates by MOCVD
9:40 AM	Guan Huang	JJ4, Integration of InAs/GaAs Nano/Micro Structures with Silicon by Selective Area Epitaxy
10:00 AM		Break
10:20 AM	Madhavi Edirisooriya	JJ5, The Electrical Nature of Structural Defects in InSb Synthesized by Molecular Beam Epitaxy on Si (100) and GaAs (100)
10:40 AM	Li Ming	JJ6, Low Leakage Current AlGaIn/GaN HEMTs on Si Substrates with Partially Mg-Doped GaN Buffer Layer by MOCVD
11:00 AM	Md Rakib Uddin	JJ7, (Student) Effect of Growth Temperature on Composition of InAlN Alloy Grown by GSMBE on Si (111)
11:20 AM	Shashidhar Shintri	JJ8, (Student) Vapor Phase Epitaxial Growth of (211)B CdTe on Nanopatterned Si for HgCdTe Based Infrared Device Applications
11:40 AM	Jhih-hong Peng	JJ9, (Student) Synthesis and Characterization of ZnTe Grown by VLS Method

Session Listing

Session KK: Nanowire Growth and Applications *Lotte Lehmann*

8:20 AM	Shruti Thombare	KK1, (Student) Size Effects in Ni Catalyzed Germanium Nanowire Growth
8:40 AM	Sung Hwan Chung	KK2, (Student) Effects of Annealing on Sub-Eutectic Heteroepitaxial Growth of Germanium Nanowire on Si (111) Substrate
9:00 AM	Marika Gunji	KK3, (Student) Catalyzed Vapor-Liquid-Solid Oxidation: Germanium Oxide Nanowires
9:20 AM	Steven Boles	KK4, Catalyst Proximity Effects on the Synthesis of Si Nanowires for In Situ Scanning Electron Microscope Li Intercalation Experiments
9:40 AM	Sourobh Raychaudhuri	KK5, A-Si / Si Nanowire Hybrid Photovoltaics
10:00 AM		Break
10:20 AM	Qiming Li	KK6, Internal Quantum Efficiency in Nanorod LED Arrays Created by Top-Down Techniques
10:40 AM	Asaduzzaman Mohammad	KK7, (Student) Electrochemically Deposited Branched Indium Antimonide (InSb) Nanowire Arrays as "In-Situ" Anti-Reflective Structures
11:00 AM	Kyeong-Sik Shin	KK8, Aligned Assembly of Nanowire Arrays with Intrinsic Control
11:20 AM	Shrawan Jha	KK9, Nanostructure Decorated AlGaIn/GaN HEMTs for Chemical Sensing
11:40 AM	John Conley	KK10, Environmental Stabilization and Functionalization of ZnO Nanobridge Sensors Fabricated Using Carbonized Photoresist

Session LL: Materials Integration: Wafer Bonding and Engineered Substrates *Multicultural Center Theatre*

8:20 AM	Xiaolu Kou	LL1, (Student) Electrochemical Etched InP Porous Layer Formation for Layer Transfer
8:40 AM	Wayne Chen	LL2, (Student) Ion-cut Transfer of InP-Based High Electron Mobility Transistors Using Adhesive Bonding
9:00 AM	Caroline Moulet	LL3, Investigation of PECVD Silicon Nitride Deposition on Porous Si
9:20 AM	Anne-Sophie Stragier	LL4, (Student) Double Layer Transfer Made by the Smart Cut™ Technology and Embedded Porous Silicon Layer
9:40 AM	Bruno Imbert	LL5, LiNbO ₃ Thin Single Crystal Layer Transfer by Smart Cut™ Technology
10:00 AM		Break
10:20 AM	Shalini Lal	LL6, (Student) InGaAs-InGaN Wafer-Bonded Current Aperture Vertical Transistors
10:40 AM	Brenda Long	LL7, Electrical Conductivity of Directly Bonded Silicon/Germanium Hetero-Structures
11:00 AM	Michael Jackson	LL8, (Student) Interface Barrier Height Reduction in Wafer Bonded n-GaAs / n-GaAs by Sulfur Passivation Methods
11:20 AM	Ki Yeol Byun	LL9, (Student) Comprehensive Investigation of Ge-Si Bonded Interfaces Using Surface Activation
11:40 AM	Michael Jennings	LL10, 3C-Silicon Carbide Epitaxy by Means of Silicon Carbide-on-Silicon Wafer Bonding

Session MM: Semiconductor Processing: Oxidation, Passivation, Etching and Contacts *Santa Barbara Harbor*

8:20 AM	Angie Lin	MM1, (Student) Surface Preparation of GaP for Regrowth on Epitaxially-Inverted Structures on Silicon
8:40 AM	William O'Brien	MM2, (Student) Oxide Surface Passivation of Ge for Optoelectronic Applications
9:00 AM	Christopher Seibert	MM3, (Student) Oxygen-Enhanced Wet Thermal Oxidation of In _{0.53} Ga _{0.47} As
9:20 AM	Seungyong Jung	MM4, (Student) Wet Etching Technique for Fabrication of GaSb Based Mid Infrared Single Lateral Mode Lasers
9:40 AM	Andrew Hollowell	MM5, (Student) Fabrication of GaAs Micromechanical Resonator Arrays for Single Molecule Detection
10:00 AM		Break
10:20 AM	Hang-Beum Shin	MM6, (Student) Hydrogenated Amorphous Silicon-Carbon Alloy Thin Films for Uncooled Microbolometers
10:40 AM	Petra Reinke	MM7, Metal and Semiconductor Contacts (Si, V, Au) to Organic Molecules: The Fullerene Model System
11:00 AM	Wei Tang	MM8, (Student) Silicide/Silicon/Silicide Heterostructures with Ultra-Thin Silicon Gap and Realization of FET Device
11:20 AM	Tae-Yeon Seong	MM9, Improved Electrical Properties of N-Contacts to N-face GaN for Vertical Light-Emitting Diodes by Laser-Annealing
11:40 AM	Wenting Hou	MM10, (Student) Resistance and Transparency Study of Contacts to p-Type GaN

Session NN: Molecular Electronics / Sensor / Ionic Conductors *State Street*

8:20 AM	Patrick Carpenter	NN1, (Student) Au-Molecule-GaAs Devices with Graphene Barrier Layer
8:40 AM	Shanying Cui	NN2, (Student) Gap Mode Plasmonic Cavity with Coupled Organic Gain Medium
9:00 AM	Dominique Vuillaume	NN3, Conductance Statistics of Molecular Junctions Fabricated with a Large Array of Sub-10 nm Single-Grain Au Nanodots Electrodes
9:20 AM	Paul Bertani	NN4, (Student) Surface Functionalization of Si Nanowires on SOI Substrates for Biosensing Applications
9:40 AM	Byungjin Cho	NN5, (Student) Switching Characteristics of Nonvolatile Organic Resistive Memory Devices with Interfacial Oxide Layers Tuned by O ₂ Plasma Treatment
10:00 AM		Break
10:20 AM	Leela Mohana Reddy Arava	NN6, (Student) Synthesis and Lithium Battery Applications of Nitrogen Doped Graphene Films
10:40 AM	Leela Mohana Reddy Arava	NN7, (Student) Conformal Coating of Thin Polymer Electrolyte Layer on Nanostructured Electrode Materials for 3D Battery Applications
11:00 AM	Raghavender Tummala	NN8, (Student) Nanostructured Co ₃ O ₄ Supercapacitors via Solution Precursor Plasma Spray
11:20 AM	Olubukun Oloniyo	NN9, (Student) Performance of MnO ₂ Crystallographic Phases in Rechargeable Lithium-Air Oxygen Cathode
11:40 AM	Amrita Jain	NN10, Investigation on Activated Charcoal-Carbon Fabrics Composite Electrode Materials for Supercapacitor Application

EMC Student Awards and Plenary Lecture

Wednesday AM Room: Corwin Pavilion
 June 22, 2011 Location: Univ. of California-Santa Barbara

8:20 AM Awards Ceremony

8:30 AM Plenary

New Concepts and Materials for Solar Power Conversion: *Wladek Walukiewicz*¹; ¹Lawrence Berkeley National Laboratory

Efficient conversion of solar photons into other forms of energy has become one of the primary objectives of the modern science and technology. In the presentation I will briefly review the various large scale energy related research projects at Berkeley. The core presentation will focus on methods to engineer the energy band structure of semiconductor materials for specific energy related applications. I will discuss recent progress on applications of group III-nitride semiconductor alloys for full solar spectrum, high efficiency multijunction solar cells. The second part of the presentation will discuss the recent advances in using highly mismatched semiconductor alloys for intermediate band solar cells. I will present most recent results on demonstration of the first intermediate band photovoltaic device.¹ Finally, I will discuss potential applications of the highly mismatched alloys for the photoelectrochemical solar water splitting. In collaboration with Solar Energy Materials Research Group (<http://emat-solar.lbl.gov/>). **Supported by the Division of Materials Science and Engineering, US DOE. ¹N. Lopez, L. A. Reichertz, K. M. Yu, K. Campman, and W. Walukiewicz, Phys. Rev. Lett., 106, 028701 (2011).

9:20 AM Break

Session A: III-Nitrides: MBE Growth

Wednesday AM Room: Flying A
 June 22, 2011 Location: Univ. of California-Santa Barbara

Session Chairs: Michael Manfra, Purdue University; Debdeep Jena, University of Notre Dame

10:00 AM

A1, Nitride Film Growth by Migration Enhanced Afterglow (MEAglow): *K. Scott Butcher*¹; *Penka Terziyska*¹; *Dimiter Alexandrov*¹; ¹Lakehead University

Recent advances in migration enhanced epitaxy have led us to develop a new technique for nitride semiconductor film growth that we have coined MEAglow (migration enhanced afterglow). Migration enhanced epitaxy is a low temperature film growth method whereby the less volatile metal precursor of a compound semiconductor is allowed extra time to migrate on the semiconductor surface to suitable lattice sites by adatom diffusion, before dosing the growth front of the material with an active nitride species to form largely stationary compound molecules. The migration of the metal species allows material of improved crystal quality to be deposited. This film deposition is done in multiple cycles to build up an adequate film thickness for the nitride compound. Traditionally the migration enhanced epitaxy of nitride films is quite slow as only a wetting layer of a couple of monolayers of metal is usually deposited per cycle. The mechanical switching of flows becomes a limiting factor, in a similar fashion to atomic layer epitaxy. However, recently it has been shown that quite thick metal layers can be deposited resulting in smooth semiconductor films despite the formation of small liquid metal droplets during the metal dosing process. This breakthrough allows migration enhanced epitaxy to be achieved at higher growth rates. MEAglow takes advantage of this recent breakthrough in MBE technology, but we have migrated the technique to a metalorganic CVD type environment capable of being scaled to large area

deposition. Instead of ammonia, a scalable nitrogen plasma source is used to provide active nitrogen species. A prototype MEAglow system has been built and initial experiments have shown that nitride films with RMS surface roughness of less than 2 nm can be achieved, and some films with RMS surface roughness of less than 2 Angstrom – as measured by atomic force microscopy. Other results of MEAglow film growth will be described as well as details of the growth technique itself. Results will be presented for both gallium nitride and indium nitride films.

10:20 AM

A2, Observation and Elimination of Indium Surface Segregation: *Michael Moseley*¹; *Brendan Gunning*¹; *Jonathan Lowder*¹; *W. Alan Doolittle*¹; ¹Georgia Institute of Technology

InGaN alloys have an outstanding potential for the field of optoelectronics due to the tunable bandgap which spans the entire visible spectrum. However, these alloys, especially those with high indium contents, are notoriously difficult to obtain as a result of thermal decomposition due to weak In-N bonds, indium surface segregation, and phase separation via spinodal decomposition. To solve these problems, low growth temperatures, fast growth rates, and in situ surface analysis must be employed to improve thermal stability, kinetically limit spinodal decomposition, and prevent surface segregation. These limitations make Metal-Modulated Epitaxy (MME) a promising candidate for growth. MME is a growth technique applied to Group-III nitrides in which metal and dopant cell shutters are periodically opened and closed while active nitrogen flux remains constant. This technique uses metal-rich fluxes that would rapidly accumulate droplets in traditional MBE growth, taking advantage of the enhanced adlayer mobility provided by excess metal. In this study, MME is applied to the growth of InGaN. Transient RHEED intensities are monitored for differing metal shutter open times (1.5s to 3.25s) as shown in Figure 1. It is found that these RHEED transients are the result of a traditional RHEED oscillation associated with the buildup and eventual consumption of the metal adlayer. This allows for observation and control of fractions of adsorbed metal monolayers. However, there is a drastic difference between the RHEED transients of low metal shutter open times (1.5s to 2.5s) with bright streaky/spotty RHEED patterns and high metal shutter open times (2.5s to 3.25s) with dim, streaky RHEED patterns. This difference is attributed to indium surface segregation, resulting in leftover indium on the surface that does not form InN at these elevated temperatures. A model for adlayer buildup and consumption is then developed for MME of InGaN. A key RHEED signature is identified as the onset of indium surface segregation. The thickness of the adsorbed metal at this onset can be calculated from the model if growth rate is known, and is found to be between 1 and 2 ML. Samples grown using this technique with careful attention of adlayer thickness exhibited single phase x-ray diffraction spectra and less than 1 nm RMS roughnesses as detected by AFM, and are shown in Figure 2. At the low temperatures required for high indium-content InGaN, an intermediate growth regime in MBE does not exist,⁷ and thus traditional MBE growth cannot produce metal-rich InGaN without droplets or indium surface segregation. Because the onset of indium surface segregation ($1 < x < 2$ ML) occurs below droplet accumulation ($< \sim 2.3$ ML),⁸ this study confirms that for metal-rich InGaN growth, some form of modulation must be employed.

10:40 AM Student

A3, Depth Resolved Strain and Composition Studies on InGaN and AlInN Films Grown by Plasma-Assisted Molecular Beam Epitaxy: *Wenyuan Jiao*¹; *Wei Kong*¹; *Tongho Kim*¹; *April Brown*¹; ¹Duke University

Recently, studies on In-based III-N alloys have attracted great attention for device applications. InGaN possesses wide tunability of the band gap from 0.7 to 3.4 eV and is therefore important for light-emitting diodes (LED) and solar cells. Also, lattice-matched AlInN grown on GaN has great potential for both optoelectronic and electronic devices due to its large spontaneous polarization and conduction band offset. However, the growth of these materials is challenging due to the large differences in the lattice constant and thermal stabilities of AlN, InN and GaN. The alloy's strain states and composition variations may profoundly affect its defect microstructure and its electronic and optical characteristics. Thus, we have explored the depth-resolved strain

and composition of several InGaN (~200 nm) and AlInN (~50 nm) samples grown by Plasma-Assisted Molecular Beam Epitaxy (PAMBE). InGaN films are grown on commercial MOCVD grown-GaN templates on sapphire at temperatures of 580 to 620°C with fixed beam fluxes of In and Ga under the same nitrogen plasma condition. High-resolution x-ray diffraction (HRXRD) is used to study the strain and defect microstructure of the samples. The average relaxation is determined from the asymmetric (1 0 5) reciprocal space map (RSM). The InGaN samples vary from pseudomorphic to increased relaxation with varied In content. Grazing-angle x-ray diffraction reveals the evolution of strain with depth: for example, we can observe a nearly-relaxed surface layer and a higher strained state towards the InGaN/GaN interface. XPS sputter depth profiling is then used for the first time to study the composition variation of MBE-grown InGaN along the growth direction. The In content in a 10 to 20 nm surface layer of InGaN samples is much higher than that in the bulk InGaN, indicating In clustering at the sample surface. While the near-surface region (~95 nm) of InGaN samples shows uniform In content, the bottom region is characterized by an In concentration that decreases linearly. AlInN samples are grown between temperatures of 400 to 540°C on GaN templates under N-rich and near stoichiometric conditions. Using the techniques mentioned above, all the InAlN samples are found to be grown pseudomorphically at or near the lattice-matched condition. The AlInN samples show the opposite In incorporation behavior to that of InGaN: the In increases from the surface to AlInN/GaN interface. Finally, the relation between strain states and composition variations are studied. We believe the strain states influences the surface interaction potential thus changing the In incorporation coefficient.

11:00 AM Student

A4, Low Temperature p-GaN Grown by NH₃-MBE: *Christophe Hurni*¹; Peter Burke¹; Jordan Lang¹; Brian McSkimming¹; Erin Young¹; Umesh Mishra¹; James Speck¹; ¹University of California, Santa Barbara

Ammonia molecular beam epitaxy (NH₃-MBE) offers many advantages for the growth of GaN. Indeed NH₃-MBE, contrary to Plasma assisted MBE, achieves the best material under N-rich conditions. This allows the growth of extremely low leakage vertical devices and a wider growth temperature window, which is promising for InGaN based devices. InGaN is known to decompose when capped by high temperature layers. Therefore, low resistivity, low temperature grown p-GaN is of great interest. We investigated the dependence of the electrical properties of 200 nm of GaN:Mg grown by NH₃-MBE on growth temperature (750 C to 850 C) and Mg flux. The samples were grown on semi-insulating 3.5 μm thick MOCVD GaN:Fe templates on sapphire. One growth temperature series was grown at a Mg concentration of 3-5x10¹⁹cm⁻³ (Series A) and another one with Mg concentrations of 8-9x10¹⁹cm⁻³ (Series B), checked by SIMS. The samples were processed into mesa isolated Hall and TLM structures with Pd/Au ohmic contacts. The parasitic current in between mesas was negligible. The growth temperature was found to have almost no influence on the Mg incorporation. However, for Series A, Hall measurement showed that the hole concentration was around 2x10¹⁸ cm⁻³ for the lower temperature GaN:Mg and only 5x10¹⁶ cm⁻³ for the high temperature GaN:Mg. The mobility did not change with growth temperature and stayed around 8-9 cm²/Vs for Series A. The resistivity is as low as 0.5-1 Ωcm for the low temperature GaN:Mg and as high as 10-20 Ωcm for the high temperature p-GaN for Series A and the specific contact resistance is as low as 2x10⁻³ Ωcm² for the low temperature GaN:Mg and only 3x10⁻² Ωcm² for the high temperature GaN:Mg for Series A. Series B follows similar trends. The mobility, hole concentration and resistivity of the low temperature p-GaN are among the best reported for p-GaN, whereas the high temperature p-GaN has a lower hole concentration, and higher resistivity than usually reported p-GaN. Earlier studies state that an increase in the hydrogen concentration for samples grown at a higher temperature in NH₃-MBE could be responsible for the decrease in the hole concentration, like for MOCVD grown GaN:Mg. However SIMS showed that the concentration in hydrogen was similar for all our samples and a 700 C 15 min annealing did not change the hole concentration. Alternatively, preliminary temperature dependent Hall measurements seem to show that the activation energy is lower the low temperature GaN:Mg, (110meV to 140meV) and higher for the high temperature GaN:Mg (190meV to 240meV). This

values are still within the range of previously reported activation energies for GaN:Mg. This could be due to early heavy doping effects or Mg precipitates and is still under investigation.

11:20 AM

A5, Epitaxial Lateral Overgrowth of Aluminum Nitride by Molecular Beam Epitaxy: *Craig Moe*¹; Jonathan Wright¹; Anand Sampath¹; Michael Wraback¹; ¹U.S. Army Research Laboratory

The growth of aluminum nitride is attracting a great deal of research interest as its wide bandgap and alloying with other III-nitrides make it highly desirable for deep ultraviolet emitters and photodetectors. As non-native substrates such as [0001] sapphire remain the most inexpensive material upon which to deposit AlN, many of the films produced contain high amounts of dislocations, on the order of 10¹⁰ cm⁻². Epitaxial lateral overgrowth (ELO) is a typical method of reducing the dislocation density of GaN films grown by metalorganic chemical vapor deposition (MOCVD), but is considerably less successful when applied to AlN or molecular beam epitaxy (MBE) due to the reduced Al adatom mobility and resulting slower lateral growth rates. In this work, we report on the lateral growth of AlN by molecular beam epitaxy. AlN films in both the [0001] and the [000-1] orientations, the latter achieved through inversion via overgrowing with magnesium, were processed into a ridge-and-trench structure with conventional photolithography. Trench widths were varied between 750 nm and 3 μm. E-beam deposited nickel was used as an etch mask to prevent the reactive ions of the etch from attacking the ridge structures. The samples were etched by inductively-coupled reactive ion etching (ICP-RIE) to depths of 300 to 500 μm, and then returned to the MBE chamber to have an additional 880 nm of AlN regrown upon the patterned templates. With careful optimization of the V/III ratio, stripe orientation, and substrate temperature, coalescence of the narrower trenches was achieved, resulting in a smooth planar film for further growth of optoelectronic devices. There is no selectivity to the AlN growth; AlN is deposited on both the upper and lower faces, as well as the sidewalls, but the narrow trench spacing and the depth of the lower surface results in lateral deposition that overgrows the AlN depositing on the trench floor. The N-face material was shown to coalesce faster than that of the Al-face. Simultaneous regrowths upon N-face and Al-face regions of the same sample show a reduced vertical AlN growth rate on N-face material. We attribute the faster coalescence of the N-face to this slower growth in the [000-1] direction. These results do indicate that lateral growth is obtainable by MBE for both polarities of AlN, however, and can be used as a template for full devices. Results of such device structures as well as transmission electron microscopy images of the epitaxial lateral overgrowth material will also be presented.

11:40 AM Student

A6, Effect of Superlattices and Surfactants on AlN Homoepitaxy by MBE: *Jai Verma*¹; Guowang Li¹; Debdeep Jena¹; ¹University of Notre Dame

AlN has a large band gap (6.2 eV), high breakdown field and thermal conductivity in combination with the high polarization fields along c-axis. AlN is an attractive material for III-V nitride HEMTs and deep UV-LEDs. Koblmüller et. al. had studied the growth diagram of AlN thin films grown on sapphire substrates using plasma assisted Molecular Beam Epitaxy (PAMBE). Stoichiometric conditions favor smooth AlN thin films with low dislocation density. In this work we demonstrate the effect of AlN/GaN superlattice buffer layers and excess Ga surfactants on AlN thin films grown near stoichiometric conditions by PAMBE on AlN-on-sapphire templates. AlN/GaN superlattice buffer layers have been known to improve the structural quality of GaN films by releasing strain. In structure (a) we incorporate the superlattice buffer layers to obtain smooth AlN thin films. The superlattice is grown at a substrate thermocouple temperature T_c~660°C at RF power of 180W with Al and Ga fluxes 8x10⁻⁸ Torr and 1.6x10⁻⁷ Torr respectively. Thereafter AlN is grown at T_c~720°C and RF power 240W for 90 minutes. The spotty (rough film) RHEED pattern of the AlN template before growth changes to the streaky (smooth film) RHEED pattern after growth of structure (b). The AFM scans confirm crack free growth and show the reduction in rms roughness from ~0.9 nm for AlN template to ~0.25 nm for structure (b), respectively, for a 2x2 μm² area. Another method to improve AlN thin film morphology has been to use excess Ga as a

surfactant while growing AlN near stoichiometric conditions. Structure (c) was grown at $T_c \sim 720^\circ\text{C}$ with Al flux of 8×10^{-8} Torr at 240W whereas structure (d) utilized Ga flux of 8×10^{-8} Torr while growing AlN at the same conditions. The in-situ RHEED pattern was obtained as spotty for structure (c) but streaky for structure (d) after growth. The cracks observed in the AFM scan for structure (c) disappeared in structure (d) and rms roughness decreased from $\sim 3.3\text{nm}$ to $\sim 0.8\text{nm}$ for $2 \times 2 \mu\text{m}^2$ area. From the cross-section TEM image, MBE grown AlN was found to be 95nm thick for a growth time of 40 minutes. The lattice image of MBE grown AlN was used to measure the lattice constants to be $c=5.0\text{\AA}$ and $a=3.1\text{\AA}$, implying pseudomorphic AlN growth. The cross-section STEM scan for structure (d) shows no visible Z-contrast between AlN template and MBE grown AlN thin film. The low dislocation density pseudomorphic AlN thin films will aid in the growth and fabrication of high efficiency deep UV-LEDs finding application in water purification, microscopy and chemical analysis.

Session B: Thermoelectrics and Thermionics I

Wednesday AM Room: Lobero
June 22, 2011 Location: Univ. of California-Santa Barbara

Session Chairs: Hong Lu, UCSB; Peter Moran, Michigan Technological University

10:00 AM Invited

B1, Phonon Engineering through Crystal Chemistry: *Eric Toberer*¹; *Alex Zevalkink*²; *G. Jeffrey Snyder*²; ¹Colorado School of Mines; ²Caltech, Materials Science

Controlling heat flow is critical to applications ranging from jet turbines to microelectronics to thermoelectrics. In energy applications, thermal engineering frequently determines system efficiency, lifetime, and cost. In thermoelectrics, many of the dramatic improvements in efficiency in the last decade have been driven by reductions in thermal conductivity. The discovery of complex, bulk thermoelectric materials with low thermal conductivity (e.g., Yb14MnSb11, Ba8Ga16Ge30, XyCo4Sb12) has led to a renewed investigation of the fundamental mechanisms of thermal conductivity. This talk explores how crystal chemistry affects both the phonon group velocity and scattering rates and develops strategies for tailoring these properties. To consider complex materials, we begin by developing models which capture the frequency-dependent group velocity and phonon scattering in simple materials. We then extend this understanding to more complicated thermoelectric materials such as Yb14MnSb11 and thermal barrier coating materials such as La2Mo2O9 (which have 104 and 624 atoms in the primitive unit cell, respectively). We conclude by considering the ongoing debate about ‘rattling’ compounds such as Ba8Ga16Ge30 and XyCo4Sb12. Using models discussed above, the role of resonant phonon scattering or group velocity is considered for the source of low lattice thermal conductivity in these materials.

10:40 AM Student

B2, Ca_3AlSb_3 and $\text{Ca}_3\text{Al}_2\text{Sb}_6$; Inexpensive, Non-Toxic Thermoelectric Materials for Waste Heat Recovery: *Alex Zevalkink*¹; *Eric Toberer*¹; *Wolfgang Zeier*¹; *Espen Flage-Larsen*²; *Jeff Snyder*¹; ¹Caltech; ²University of Oslo

Ca_3AlSb_3 and $\text{Ca}_3\text{Al}_2\text{Sb}_6$ are Earth-abundant, non-toxic Zintl compounds, with promising thermoelectric properties. Both compounds have crystal structures consisting of infinite, parallel chains of corner sharing AlSb_3 tetrahedra, surrounded by calcium cations. However, the relative deficiency of calcium in $\text{Ca}_3\text{Al}_2\text{Sb}_6$ causes the formation of Sb-Sb bonds between the chains, which results in tetrahedral ‘ladders’. The structural complexity of Ca_3AlSb_3 and $\text{Ca}_3\text{Al}_2\text{Sb}_6$ (26 and 28 atoms per unit cell, respectively) contributes to their extremely low lattice thermal conductivity, which approaches the amorphous limit at high temperatures ($\sim 0.6 \text{ W/mK}$ at 1050 K). High temperature Hall and Seebeck measurements confirm that both compounds are charge-balanced

semiconductors, as expected from Zintl charge-counting conventions. Optimization of electronic properties is achieved via control of the p-type carrier concentration through sodium doping. To first order, the high temperature electronic behavior of the doped samples can be well described by a single parabolic band model. Electronic structure calculations for Ca_3AlSb_3 reveal a valence band edge containing nested parabolic bands, and dominated by Sb p states. A maximum zT of 0.8 and 0.6 is obtained at 1000 K for sodium-doped Ca_3AlSb_3 and $\text{Ca}_3\text{Al}_2\text{Sb}_6$, respectively. In both cases, we attribute the high thermoelectric efficiency to a combination of low lattice thermal conductivity and a band gap sufficiently large to delay the detrimental effect of minority carriers on the Seebeck coefficient until high temperatures.

11:00 AM

B3, The Impact of Nano-Inclusions Introduced by Mechanical Alloying on Thermoelectric Transport in $\text{Pb}_{1-x}\text{Sn}_x\text{Te}$: Experimental Results and Theoretical Predictions: *Lakshmi Krishna*¹; ¹Michigan Technological University

In this work we analyze experimentally measured electrical conductivity data and Seebeck coefficient data measured from 300 K to 700 K from two n-type $\text{Pb}_{1-x}\text{Sn}_x\text{Te}$ samples ($1.2 \times 10^{19}/\text{cm}^3$ and $3.8 \times 10^{18}/\text{cm}^3$) made by mechanical alloying with differing amounts of Sn ($x=0.066$ and 0.269 , respectively). It is determined by X-ray diffraction analysis that approximately 2 vol.% of both alloys are $\sim 15\text{nm}$ diameter SnO_2 inclusions. To analyze the impact of the secondary phase inclusions on $\text{Pb}_{1-x}\text{Sn}_x\text{Te}$ alloys we first compare the experimental data to a three-band model of what would be predicted [1] if electron scattering were to be dominated by just phonons and alloy scattering. For both alloys, the experimentally measured mobility is much smaller than what would be expected near room temperature, but is close to the calculated phonon-dominated mobility at higher temperatures. However, the magnitude of the experimentally measured Seebeck coefficient is significantly larger over the entire temperature range than what would be expected if phonon and alloy scattering were to dominate. The impact of electron scattering by nano-inclusions can be modeled in the framework of the Boltzmann transport equation using the relaxation time approximation. A scattering term with a $E^{3/2}$ relaxation time energy dependence has been proposed by Faleev, et al. [2] to be appropriate. When this term is incorporated into the theoretical calculations, it is found that the calculations agree with the experimentally measured conductivity data and Seebeck coefficient data over the entire temperature range investigated. We conclude that the $\sim 15 \text{ nm}$ diameter SnO_2 inclusions present in mechanically alloyed $\text{Pb}_{1-x}\text{Sn}_x\text{Te}$ increase the magnitude of the Seebeck coefficient due to an energy filtering effect that is consistent with the expected $E^{3/2}$ dependence of the relaxation time characterizing their contribution to electron scattering. The impact of this on the material’s thermoelectric figure of merit as a function of temperature will be discussed.

11:20 AM

B4, Reevaluation of $\text{PbTe}_{1-x}\text{I}_x$ as High Performance n-Type Thermoelectric Material: *Aaron LaLonde*¹; *Ynazhong Pei*¹; *G. Jeffrey Snyder*¹; ¹California Institute of Technology

Thermoelectric transport properties of n-type $\text{PbTe}_{1-x}\text{I}_x$ with carrier concentrations ranging from 5.8×10^{18} - $1.4 \times 10^{20} \text{ cm}^{-3}$ are reinvestigated from room temperature to 800 K. The electronic transport properties, resistivity and Seebeck coefficient, in this study are effectively consistent with prior reports, however the thermal conductivity has been found to be historically overestimated. The reassessment of the thermal transport properties, in combination with careful control of the carrier density by iodine doping, reveals a significantly larger figure of merit, $zT_{1.4}$, than often previously reported for n-type PbTe. The results and analysis of the data from this study lead to a redetermination of zT for this historical thermoelectric material and provide a renewed interest in n-type PbTe based materials.

11:40 AM

B5, The Universal Optimal Seebeck Coefficient for Maximum Power Factor: *Paothep Pichanusakorn*¹; *Prabhakar Bandaru*¹; ¹UCSD

The efficiency of thermoelectric material is measured through the Figure of merit, $Z=(S^2s)/(ke+kL)$, which is constituted from both electronic (the Seebeck

coefficient: S , the electrical conductivity: s , and the electronic part of the thermal conductivity: ke) and lattice properties (lattice thermal conductivity: kL). The denominator of Z , S_2n , also called the power factor, can be further break down into $(S_2n)e\mu$, where n is the carrier concentration, μ the electron mobility, and e the electron's charge. Typically, when one increases the carrier concentration, there is a corresponding decrease in S , which limits the S_2n term and Z . Consequently, one has to find the optimal carrier concentration that yields the maximum S_2n . This optimal carrier concentration differs according to materials and the temperature at which it is used. However, through analytical work, we have found that while the optimal carrier concentration may change with material and temperature, there is a corresponding 'optimal Seebeck coefficient', with values in the range of 130 to 186 $\mu\text{V/K}$, which is largely independent of material and temperature. The existence of this universal optimal Seebeck coefficient is made obvious when one examine the relationship between the reduced Fermi level, the band structure, the carrier concentration, and the Seebeck coefficient itself. In practical term, the optimal Seebeck coefficient will serve as a direct guide for finding the optimal carrier concentration for any material at any temperature. Furthermore, the same analysis and conclusion also applies to quantum-confinement device such as quantum wells and nanowires.

enabling us to build a transmission model specific to different types of defects, for example.

10:20 AM

C2, Measurement of Nanoscale External Quantum Efficiency of Plastic Solar Cells by Photoconductive Atomic Force Microscopy: *Xuan-Dung Dang*¹; Thuc-Quyen Nguyen¹; Alexander Mikhailovskiy¹; ¹UCSB

Conversion of the Sun's usable solar energy reaching the surface of the Earth in a single hour into the electricity can meet all the global energy need for an entire year. With their potential for cheap, light-weight, flexibility, and ease of processing and installation, plastic solar cells are expected to be next energy generation technology for the future. Although, there is much progress in this field, the technology is still far from practical application for mass production. Fundamental understanding of nanoscale photoactive morphology and device physics is needed to achieve higher device efficiency. In this presentation, we demonstrate the application of photoconductive atomic force microscopy (pc-AFM) to probe charge generation and nanoscale external quantum efficiency (EQE) of polymer bulk heterojunction solar cells based on poly[2-methoxy-5-(3,7-dimethyloctyloxy)-1,4-phenylenevinylene (MDMO-PPV) and [6,6] phenyl-C71-butyric acid methyl ester (PC71BM). Nanoscale EQE reveals the complex morphology and photocurrent generation of MDMO-PPV:PC71BM films. Not only electron transfer from the photoexcited donor to the fullerene, but also hole transfer process from photoexcited fullerene to the donor phase due to HOMO offset is observed. The difference in performance between toluene and chlorobenzene-cast devices is explained by the variation of relative contributions from two charge transfer mechanisms. This obtained result is a significant advance in the pc-AFM development for plastic solar cell characterization.

Session C: Nanoscale Characterization

Wednesday AM
June 22, 2011

Room: Lotte Lehman
Location: Univ. of California-Santa Barbara

Session Chair: Suneel Kodambaka, University of California, Los Angeles (UCLA)

10:00 AM Student

C1, Scanning Gate Spectroscopy: A New SPM Technique for Nano-Devices on Oxide Surfaces: *Steven Hunt*¹; Elliot Fuller¹; Brad Corso¹; Phil Collins¹; ¹Department of Physics and Astronomy, University of California at Irvine

Electronic devices at the nanoscale have reached such small dimensions that scanning probe techniques are critical for their characterization. Understanding the operating mechanisms of nanoscale field effect transistors, quantum point contacts, and nanowire sensor devices all require nanometer-resolution electronic measurements. Of the scanning probe techniques frequently used, however, few provide the energy-dependent information that clearly illuminates device operation. Tunneling spectroscopy, while enormously successful, is severely limited for field effect devices built upon insulating oxides. Our research has therefore focused on atomic force-based electrical characterization, such as Kelvin force microscopy, electrostatic force microscopy, and scanning gate microscopy (SGM), and specifically attempts to extend these techniques towards true spectroscopies. Here we describe an energy-resolved version of SGM named scanning gate spectroscopy (SGS). In traditional SGM, a conductive AFM probe is used as a source of localized electric fields that can gate a device or change its conductance. By correlating conductance changes with probe position, SGM produces qualitative maps of device gate sensitivity. The new SGS technique operates in a similar manner but continuously varies the electrostatic potential of the probe. The gating characteristics of the entire device are mapped out both spatially and electronically, revealing the energy-dependent effects of local defects and inhomogeneities. For example, the difference in scattering as particular sites move into and out of resonance with the Fermi level becomes straightforward to observe; even more importantly, the SGS mapping return quantitative information that enables accurate modeling of device operation. We apply the technique to carbon nanotube field-effect transistors (CNTFETs), which are an ideal test case because of they have multiple, independent mechanisms of gate sensitivity. A typical CNTFET might have a semiconducting bandstructure, a Schottky barrier contact, and one or more defect sites, all of which are gate sensitive under different conditions. The SGS technique clearly distinguishes between these three mechanisms and provides new information about each,

10:40 AM

C3, Role of Ethylene on Thermal and Chemical Stability of TiO₂(110): *Yuya Murata*¹; Vania Petrova²; Ivan Petrov²; Suneel Kodambaka¹; ¹University of California, Los Angeles (UCLA); ²Frederick-Seitz Materials Research Laboratory, University of Illinois Urbana-Champaign

Using in situ high-temperature (700-1000 K) scanning tunneling microscopy (STM), in combination with density functional theory (DFT), we studied the influence of ethylene on the surface dynamics of rutile-structured TiO₂(110). STM images were acquired as a function of time, oxygen and ethylene partial pressure, and temperature. During annealing in ultra-high vacuum, we observe the reduction of TiO₂(110)-1x1 to TiO₂(110)-1x2 due to the desorption of oxygen atoms from the surface. In presence of oxygen, the opposite behavior, i.e. conversion of Ti-rich TiO₂(110)-1x2 to TiO₂(110)-1x1 is expected and was observed. Interestingly, in the presence of a gas mixture composed primarily of ethylene with small amounts of oxygen, we observed an enhanced rate of conversion from Ti-rich surface to stoichiometric TiO₂(110)-1x1 and an associated accumulation of surface mass. That is, we observe a net increase in the surface coverage of Ti and O atoms at a rate that increases with increasing ethylene pressure and decreasing temperature. We attribute this surprising result to the ethylene-catalyzed dissociation of O₂ molecules on TiO₂(110).

11:00 AM

C4, Combined XSTM and High Resolution XRD Study for Quantitative Structural Descriptions of Type-II Superlattice IR Detectors: Michael Yakes¹; Syed Qadri¹; Kevin Matney²; Changyun Yi¹; Ed Aifer¹; *Nadeemullah Mahadik*¹; ¹Naval Research Laboratory; ²Jordan Valley Semiconductors

The type-II superlattice (T2SL) material system has made great progress towards infrared devices with state of the art performance using band structure engineering to develop new designs. In order to fully understand the material effects on device quality we believe it is essential to determine the structural properties in as much detail as possible. We have developed a powerful approach to accomplishing this using atomic scale resolution cross sectional scanning tunneling microscopy (XSTM) to identify the microscopic structure in small regions of a given sample, and then incorporating this information into detailed simulations of the XRD spectra. This technique yields a detailed quantitative description of the structure on a macroscopic scale. XRD and dynamical simulation of the x-ray rocking curves are well-established and powerful tools

for characterizing such structural properties as composition, thickness, and strain in complex heterostructures composed of multiple superlattice regions. Typically, the SL period is estimated from the satellite peak separation, and the average SL lattice constants are estimated from the position of the 0th order satellite peak. More detailed structural information may also be obtained by simulating the XRD spectra using the intended structure and composition using an automated fitting procedure with a set of free parameters and arbitrary tolerances. However, the success of such a fit depends critically on appropriate choice of the independent variables and their ranges of uncertainty, therefore without a reliable knowledge of the microstructure this approach is unlikely to provide fitting results that can be used with confidence. Instead of using idealized parameters from the growth design, we use inputs derived from XSTM images which yield local structural and compositional parameters with atomic scale precision. Our XSTM images give local information on the lattice thickness, interface roughness, interface bonding, and group V cross incorporation. High resolution x-ray measurements of multiple reflections from the same sample were performed using a Rigaku four-circle diffractometer and an 18 kW generator equipped with Cu-anode. The incident x-ray beam was monochromated to CuK α 1 radiation by using two Ge(220) channel-cut crystals. This arrangement provided an angular resolution of 3.6 arcseconds in 2 θ . A full dynamical XRD fitting was then performed using the commercially available Bede RADS simulator, in conjunction with initial parameters and tolerances provided by the XSTM measurements. When the structural and compositional values from the XRD fit were incorporated into the band structure algorithm, the recalculated energy gaps were in better agreement with the measured photoluminescence than the gaps derived from the intended structure. We believe that this combined approach of the microscopic XSTM measurements with the statistical XRD probe and simulation will allow a more reliable picture of the superlattice structure on the wafer scale.

11:20 AM Student

C5, In Situ Transmission Electron Microscopy and Photoluminescence Study of Ge-Core/SiGe-Shell Nanowires: *Shu Hu*¹; Yoko Kawamura²; Kevin Huang¹; Irene Goldthorpe¹; Ann Marshall¹; Mark Brongersma¹; Paul McIntyre¹; ¹Stanford University; ²Keio University

Group IV coaxial nanowire heterostructures can significantly improve the performance of nanoelectronic and nanophotonic devices. Germanium (Ge) has large intrinsic carrier mobilities and a small band gap. Ge nanowires (NWs) offer particularly interesting opportunities for on-chip light sources and detectors as their absorption wavelengths can be matched to telecommunication standards. However, small diameter wires have large surface area-to-volume ratio, and carrier scattering and recombination at the surface may significantly degrade their performance in devices. For instance, the number of photoluminescence (PL) studies involving Ge NWs is still limited, because it is challenging to detect sufficient emission intensity from Ge NWs without appropriate surface passivation. This is an important technological issue towards realization of Ge NW-based devices. In the present report, epitaxial growth of a Si or SiGe shell around a Ge NW core is proposed to achieve surface passivation and carrier confinement by using Si/SiO₂ passivation and by creating core-shell band offsets. We have previously shown that by inhibiting surface roughening of a Si or SiGe shell around a Ge NW during growth, highly strained, dislocation-free, coherent core-shell NWs are obtained. In this new work, Au-catalyzed, chemical vapor deposited Ge NWs are first synthesized, followed by heteroepitaxial deposition of a SiGe shell. Dislocation-free NWs can be synthesized with controlled coherency strains in the core and shell, and with various core and shell radii. We have successfully observed PL from the Ge-core/SiGe-shell NWs with significant intensity in the near-infrared region. The emission wavelength maximum from the bulk Si reference sample was attributed to indirect band-to-band transitions. For the core-shell NWs, while the PL from the Si substrate was measured at the same peak position as for the bulk Si, we found that the PL also peaked at around 1766 nm, which was in agreement with the indirect transition of bulk Ge. However, these as-grown NWs with large Si composition gradient and core-shell lattice mismatch are not in thermodynamic equilibrium. The effects of thermal annealing on atomic motion leading to core-shell strain relaxation are not yet understood.

We focus on strain relaxation mechanisms, including Si-Ge interdiffusion, stress-driven surface roughening and associated dislocation formation, in the initially coherent core-shell NWs during post-growth thermal annealing. In situ Transmission Electron Microscopy is employed to characterize the time evolution of nanowire surface roughness and dislocation density at various annealing temperatures. Si and Ge composition line profiles across core-shell interfaces are characterized using energy-dispersive x-ray spectroscopy before and after in situ annealing. Results are then compared to reported model predictions to determine the mechanism by which strain is relaxed. In summary, our study provides valuable insights regarding the electronic structure and thermal stability of strained core-shell nanowire heterostructures.

11:40 AM Student

C6, Local Strain Characterization of MEMS-Based Silicon Beams by Raman Spectroscopy: *Ferran Ureña*¹; Sarah Olsen¹; Enrique Escobedo-Cousin¹; Lidija Siller¹; Umesh Bhaskar²; Jean-Pierre Raskin²; ¹Newcastle University; ²Université catholique de Louvain

State-of-the-art electronic devices are nowadays well into the nanometer regime. Raman spectroscopy is a non-destructive technique for chemical and mechanical analysis which can be used for local strain characterization of nanoscale devices. By measuring the inelastic scattering of light due to lattice vibrations and electronic excitations, the frequency shift in scattered light is compared with unstrained material to extract residual or applied strain. In this work, we show strain measurements in MEMS-based silicon beam structures fabricated following an original technique[1] which makes use of the internal stress present in an "as-deposited" silicon nitride actuator in order to induce controlled levels of deformation in the released silicon beams. The stress magnitude depends on the structure geometry and it enables the fabrication of structures arrays over a wide range of strain levels. The tensile strain was assessed by Raman spectroscopy using two lasers with a different penetration depth which allowed the study of strain both at surface and bulk levels. Excellent agreement of strain is shown across the entire range of beam lengths measured by Raman and compared with scanning electron microscopy (SEM). It is also demonstrated that important discrepancies may arise from the incorrect use of phonon deformation potentials (PDP) used to relate the Raman frequency shift with strain. Different PDPs have been reported for silicon[2-4]. In early experiments[2-3] the laser used was not able to penetrate through the entire material and the PDPs are therefore expected to be affected by relaxation of stress near the surface. To rectify this, later experiments[4] were carried out using a laser with greater penetration depth which enabled the extraction of more accurate PDPs. Nevertheless the migration from bulk silicon devices to nanostructures means that such PDPs are no longer appropriate. Furthermore, many groups currently use UV Raman with a penetration depth of roughly 10 nm to study thin layers. However, the PDPs chosen often remain those suitable for bulk silicon or are omitted from analysis. Our work highlights the need of an appropriate selection of PDPs for an accurate analysis of strain from Raman data. To date, no experimental values for PDPs suitable for strain determination in small devices have been reported. As a consequence some reports present results only in terms of Raman shift rather than strain while in other works a particular set of PDPs is arbitrarily chosen. Our work shows that in the case of silicon nanostructures, an improved agreement with theory is demonstrated by using older PDP values rather than the more recent values which relate primarily to bulk. Results indicate that in some cases errors up to 25% in strain determination are possible as a consequence of using a wrong set of PDPs.

Session D: Plasmonics and Metamaterials

Wednesday AM
June 22, 2011

Room: MCC Lounge
Location: Univ. of California-Santa Barbara

Session Chair: Rachel Goldman, University of Michigan

10:00 AM Student

D1, Tuning of Plasmonic Cavity Resonances Using Atomic Layer Deposition: Yan Mui Kitty Yeung¹; Kasey Russell¹; Evelyn Hu¹; ¹Harvard University

Metal-based optical cavities utilizing surface plasmon polaritons (SPPs) to confine electromagnetic energy can have sufficient ratio of quality Q to cavity mode volume V to modify the fluorescence of nano-emitters. It was demonstrated by our group that a plasmonic cavity could be formed in the gap between a Ag nanowire (NW) and a Ag substrate with PbS quantum dots (QDs) inside. The optical signature of the QDs was modified by their presence within the plasmonic cavity. A critical issue for the coupling of QDs to cavities is the ability to tune the two into resonance. This work describes a facile method to achieve the tuning of the modes of the cavity over tens of nanometers without degradation of the cavity Q. This tuning should enable unambiguous determination of quantum electrodynamics effects in plasmonic cavities by providing a mechanism to tune cavity resonances through the gain spectrum of coupled emitters. A dielectric Al₂O₃ layer approximately 3 nm thick was sputtered on a smooth, template-stripped Ag substrate. One to two monolayers of PbS QDs were stamped onto the dielectric layer and were covered by an additional ~6 nm of sputtered Al₂O₃. Ag NWs of 1-5 μm in length and ~100 nm diameter were deposited onto the sample in a droplet of ethanol that was allowed to dry. Photoluminescence spectrum of an as-fabricated cavity was taken which displayed well-defined modes. We then added thin, well-controlled layers of a dielectric onto the cavity structure, which resulted in systematic shifts in the mode frequencies. The dielectrics were formed by atomic layer deposition (ALD) - a process that allows conformal deposition through self-limiting chemical reactions, as well as precise control of layer thickness. It is able to deposit Al₂O₃ into the areas of the cavity adjacent to the line of contact between the nanowire and dielectric. Each 'layer' of Al₂O₃ is approximately 0.1 nm thick. ALD results in tuning of the cavity resonances by increasing the index of refraction from 1 to ~1.5 in these regions. Deposition of 70 layers of ALD at 60 °C continuously tunes the cavity resonances to longer wavelengths without significant alteration of the width of the modes. The maximum (45 nm) tuning available is limited by the strong mode confinement of the as-fabricated structure: the effective index can only be increased for the evanescent tail of the mode that is not initially contained within the dielectric gap. Nevertheless, we observe sufficient tuning to enable the cavity modes to be shifted by more than their half-width, allowing a mode initially in resonance with an emitter to be completely detuned.

10:20 AM

D2, Tunable Infrared Absorption of Nano Plasmonic Structures: Naresh Das¹; Wayne Chang¹; ¹Army Research Laboratory

Surface plasmon, although predicted long time ago, have recently been the subject of renewed interest as many applications are foreseen in nano or micro optics, solar cells or metamaterials [1]. The localized plasmon resonance in metallic nano particles (MNP) can cause near field enhancement and enhanced scattering cross section and both of them can be used to enhance the absorption in solar cell. It is also reported that the surface plasmon resonance frequency of the nano metallic layer depends on the shape, size, types of metal and the surrounding medium. Though most of the surface plasmon experiments dealt with MNP for devices in visible spectral region, very few papers have reported the results from infrared (IR) regions [2]. However, many defense application including infrared counter measure and sensor applications require device operation in mid to far infrared regions. We report here the infrared absorption

by gold nano plasmon structure of various geometries. Grating mask of different square sizes of 1.25, 2.5 and 3 micron square is used to generate Gold (Au) nano plasmon layer. We have performed experiment with different Au metal layer thickness ranging from 10-100 nm. The same grating mask is used to generate crescent structure with 3 micron long and 0.4 micron width. Crescent structure is fabricated by e-beam evaporation of Au nano metal layer at different angles. We used Fourier transform infrared (FTIR) spectrometer to obtain the absorption spectra. We observed tunable absorption in the infrared range of 2.5-20 micron by gold nano-plasmon metal layer. The absorption peak corresponding to 1.25, 2.5 and 3 micron square Au metal layer are 4.9, 14 and 17.1 micron respectively. We did not observe appreciable shifts in peak absorption wavelength due to different Au metal layer thickness even though we varied the metal layer thickness from 10-100 nm. For crescent structure, we observed a polarization dependence of absorption. For example for 3 micron long and 0.4 micron width crescent structure, transverse electric (TE) absorption peak occurs at 14.2 micron whereas transverse magnetic (TM) absorption occurs at 4.0 micron. The absorption characteristics of our periodic crescent structures are higher than the previously reported results [2] from randomly generated crescent structures by using polystyrene nanoparticles. Our tunable absorption characteristics show that proposed nano plasmon structures can be used to enhance the performance of either IR detectors or emitters.

10:40 AM

D3, In Situ Spectroscopic Ellipsometric Analysis of Thin Silver Films Deposited Using DC Magnetron Sputtering and HiPIMS Techniques: Lirong Sun¹; Neil Murphy¹; Adam Waite¹; John Jones¹; Rachel Jakubiak¹; ¹Air Force Research Laboratory

Very dense, thin films of noble metals are required in many optical coating and metamaterial applications. Using DC magnetron sputtering (DCMS) the initial growth of Ag on an oxide substrate follows the Volmer-Weber model with island formation followed by percolation and eventually continuous growth (coalescence). The islands and voids can be problematic in optical coatings because of losses due to scattering and strong optical absorptions associated with plasmonic resonances [1]. Additionally, below the coalescence threshold the optical dispersion in the visible and near IR regions deviates significantly from that of bulk Ag [2]. Highly energetic deposition methods such as high power impulse magnetron sputtering (HiPIMS) decrease the coalescence threshold by improving the cohesion between the Ag film and the substrate. This can be measured in real time using in situ spectroscopic ellipsometry (SE). In situ SE is a non-intrusive and non-destructive method for obtaining film thickness and optical dispersion in real-time during film growth. This real-time analysis provides valuable information about the dynamic optical properties of each stage of film growth starting with island formation, followed by percolation and coalescence into a continuous film. With this data in hand the growth of the films can be stopped at an optimal thickness. Ag films grown on Si and glass substrates using DCMS and HiPIMS with a 2-inch diameter Ag target were studied and compared. The in situ SE data, Ψ and Δ, at an incidence angle of 700 at 593 wavelengths in the range of 371-1678 nm were acquired every 16 seconds with the acquisition period synchronized with the substrate rotation period. The film thickness, the index of refraction and the extinction coefficient were determined with dynamic fittings of a Lorentz oscillator model. The film thickness as a function of deposition time was virtually monitored; thereby the coalescence threshold was detected in real time during film growth. The Ag film deposited by DCMS at 4mTorr of pressure grew linearly with deposition time above 10 nm. Below 10 nm, the surface roughness is maximized at 8.6 nm, and it dropped significantly between 8.6 to 10 nm. This indicates the coalescence threshold is at a thickness of 10 nm. The Ag thin films prepared via HiPIMS were investigated by varying process pressure, pulse duty cycle, time-average power. Monitoring with in situ SE, the HiPIMS process was optimized to grow a fully continuous film at the lower percolation threshold with low surface roughness compared to those deposited by DCMS.

11:00 AM Invited

D4, Second Harmonic Generation in a Metamaterial Resonating at Fundamental and Second Harmonic Frequencies: Yasuhiro Tamayama¹; Tetsuo Kanazawa¹; Toshihiro Nakanishi¹; Masao Kitano¹; *Akio Sasaki*¹; ¹Kyoto University

Metamaterials are arrays of artificial structures having dimensions that are much smaller than the wavelength of electromagnetic waves. Metamaterials are used to realize unusual refraction, reflection, and propagation of electromagnetic waves that cannot be achieved using only naturally occurring media. The properties of metamaterials are determined by the shape and material of the constituent, and, therefore, devices with desired functions can be obtained by designing the constituent. Pendry and co-workers showed that when a constituent of a metamaterial is a resonant conductive element, electromagnetic energy is squeezed into a small volume of the constituent at the resonant frequency. They predicted that if a nonlinear material is placed in the volume, the nonlinear behavior of the material is enhanced. Thus far, this phenomenon has been applied to second harmonic (SH) and higher-order harmonic generations and other nonlinear phenomena. In this study, we propose a more efficient method of generating SH waves in a resonant metamaterial, as compared to previously proposed methods. We found from electric circuit models of resonant metamaterials that the SH generation can be further enhanced by introducing a resonator for the SH frequency in addition to a resonator for the fundamental frequency. Based on the circuit analysis, we designed and fabricated a doubly resonant metamaterial in the microwave region. A unit cell of the doubly resonant metamaterial consists of two resonators: the primary resonator and the secondary resonator. The primary resonator includes a Schottky diode, which acts as a nonlinear element, and resonates at the fundamental frequency. The secondary resonator resonates at the SH frequency. These resonators are coupled with each other. For the experimental demonstration of the enhancement of the SH generation, we performed transmission measurements of the doubly resonant metamaterial. The mono-layer doubly resonant metamaterial was placed in a parallel plate waveguide. A pair of ultra wide band dipole antennas was used as a transmitter and a receiver. The transmitting antenna was excited by a signal generator and the receiving antenna was connected to a spectrum analyzer. We observed that the radiated SH power from the doubly resonant metamaterial was 4.6 times as large as that from the metamaterial without the secondary resonator. We compared the measured data with the result of the circuit analysis. The measured dependence of the radiated SH power on the coupling strength between the primary and secondary resonators was consistent with the result found from the circuit analysis. Thus, we conclude that the SH generation is resonantly enhanced in the secondary resonator coupled with the primary resonator.

11:40 AM Student

D5, Optical Dispersion of Amorphous Germanium Thin Films as a Function of Thickness and Deposition Parameters: *Neil Murphy*¹; Lirong Sun¹; Adam Waite¹; John Jones¹; Rachel Jakubiak¹; ¹Air Force Research Laboratory

Amorphous Germanium films were fabricated using pulsed DC magnetron sputtering and analyzed by way of in-situ ellipsometry. Preliminary results indicate that the complex index of refraction within the visible to near-infrared wavelength region increases with film thickness. The thickness of the films was varied by systematically changing deposition parameters such as power, pulse frequency, working distance, and inert gas concentration. Based on the data acquired, the real component of the index of refraction (n) has been shown to increase proportionately with film thickness, while the extinction coefficient (k) has demonstrated significantly less sensitivity. One possible explanation for effect of film thickness on the refractive index is a potential change in density between thin and thick films. Since growth of magnetron sputtered Ge films typically follows the Volmer-Weber model, initial deposition of Ge creates islands of material on the substrate that coalesce into a uniform film above a thickness threshold of around 40 Å [1]. Therefore, it is expected that films not exceeding this threshold will have minimal densities due to the discontinuity of the layer. Above the coalescence threshold, films become fully conformal,

leading to higher density values. In addition to island coalescence, protracted deposition time is suspected to facilitate the growth of nanocrystallites that have high density due to increased packing efficiency. This follows the relationship between density and refractive index as given by the Gladstone-Dale approximation. Given that thickness is a critical parameter in any optical coatings application, it is necessary to be able to obtain the desired refractive index within the prescribed geometric constraints. Currently, pulsed DC magnetron sputtering techniques have not proven to be ideal for preserving the refractive properties of Ge at lower thicknesses. Methods such as high power impulse magnetron sputtering (HiPIMS), however, have shown promise due to their ability to sustain high density plasma while decreasing deposition rate by as much as 75% [2]. The increased power output, coupled with the low sputtering rate, indicates that the incident atoms deposited via HiPIMS will possess sufficient energy to promote densification and layer continuity.

12:00 PM D6, Late News

Session E: Organic, Printed and Flexible Electronics

Wednesday AM
June 22, 2011

Room: MCC Theatre
Location: Univ. of California-Santa Barbara

Session Chairs: William Wong, University of Waterloo; Oana Jurchescu, Wake Forest University

10:00 AM

E1, Quantum Dot Red/Green/Blue/White Light-Emitting Electroluminescent Devices with a Low Turn-on Voltage and High Brightness: *Seonghoon Lee*¹; ¹Seoul National University

Red/Green/Blue/White light-emitting diodes (R/G/B/WLEDs) based on colloidal quantum dots have a great opportunity for flexible large-area displays or energy-efficient light sources due to the ease of color tunability and cost-effective solution processibility. However, QLEDs reported ever have not satisfied the requirements such as brightness and operation voltage for practicable usages. Here, we present bright and low-voltage driven R/G/B/White-QLEDs with an inverted device architecture. Dichromatic (blue & yellow), trichromatic (blue, green, & red), and tetrachromatic (blue, cyan, yellow, & red) white-QLEDs exhibiting luminance of 500 ~ 5,000 cd m⁻² at an applied bias below 6 V have been accomplished with mixed QD active layers in an inverted device structure. In addition, practical applications of white-QLEDs such as traffic signals, display back-lights, and white illumination sources are exemplified. Our approaches and present results demonstrate remarkable progress in device performances of R/G/B/White-QLEDs and also provide reasonable guidelines for the practicable realization of R/G/B/White-QLEDs.

10:20 AM Student

E2, Fabrication of Flexible Single-Crystal Devices on Electrically-Conductive Substrates: *C. Doran*¹; W. Chen¹; K. Henttinen²; T.L. Alford³; S.S. Lau¹; ¹Department of Electrical and Computer Engineering, University of California, San Diego; ²Okmetic Oyj; ³School for Engineering of Matter, Transport and Energy, Arizona State University

Flexible circuits are widely seen as desirable for their advantages of light weight, toughness, and their ability to bend and tailor-fit in applications with physical constraints. Three particular devices that could demonstrate the benefit of this technology are light-emitting diodes (LEDs), photovoltaic (PV) cells, and photodetectors. Flexible LEDs can be incorporated in bendable displays, and larger-area PV in particular can greatly benefit from being able to bend over the contours of vehicle bodies, rooftops, or the constantly-flexing realm of backpacks or tactical apparel that incorporate the capacity to charge electronic devices. Most current flexible device technology, especially that which relates to silicon, utilizes hydrogenated amorphous, microcrystalline, or even nanocrystalline material. Monocrystalline silicon would be advantageous

by offering much higher mobility. Previous successful research into this has taken various approaches. One method is to etch away the buried oxide layer of silicon-on-insulator (SOI) wafers, and transfer the top Si device layer to flexible substrates. For this to work, etchant ions must be able to diffuse throughout the thin sandwiched oxide layer from the sides. Unfortunately, this process can become prohibitively slow for large-area samples. We will discuss our work in the transfer of larger-area monocrystalline silicon layers of thickness 3 microns or less onto flexible polymer substrates. Our methodology involves bonding the device layer of SOI to the substrate with an electrically-conducting adhesive, and subsequently removing the donor material. The donor substrate is first mechanically lapped to rapidly remove the majority of material; it is subsequently chemically etched to more gently remove the remaining material, up to the buried-oxide etch stop layer. After HF-driven removal of the exposed oxide face, thin and flexible monocrystalline silicon is left on an electrically-conductive substrate which serves as the backside contact. A demonstration Schottky-barrier diode is made with the transferred silicon, and its electrical and physical characteristics will be discussed. Also demonstrated are flexible monocrystalline GaAsP LEDs fabricated using a similar process. Furthermore, we will discuss the extensibility of this technique to other semiconductor materials for higher solar absorption in PV, improved LEDs, and other electronic devices. NSF-DMR support of this research is gratefully acknowledged.

10:40 AM

E3, A Compensation Mechanism for Flexible and Electrically Stable Solution-Processed Organic Field-Effect Transistors: *Do Kyung Hwang*¹; Canek Fuentes-Hernandez²; Junbae Kim¹; Willliam Pottsavage¹; Bernard Kippelen¹; ¹Georgia Institute of Technology

Organic field-effect transistors (OFETs) have been extensively studied because they could be a cost-effective solution that enables pervasive printable low-end circuit applications. Prototypes of electronic devices such as drivers for flat-panel displays, complementary circuits, and various sensors have already been demonstrated on flexible substrates. However, operational instabilities such as hysteresis and variations of the drain current with bias stress are still issues that need to be addressed to transition this technology into commercial applications. The origins of operational instability can be attributed to three main mechanisms: trapping of electrical charges at the semiconductor/dielectric interface, field-induced dipolar orientation inside the gate dielectric, and injection of charges into the gate dielectric from the gate electrode. The stability of FETs can in general be rationalized by one, or a combination of these mechanisms. Here we describe the concept of using compensating effects to demonstrate OFETs on rigid and flexible substrates, with excellent operational stability. These transistors were comprised of a bi-layer top-gate insulator of CYTOP and a high-*k* Al₂O₃ layer grown by atomic layer deposition (ALD), and a hole-transporting semiconductor composed of a 6,13-bis(triisopropylsilyl)ethynyl pentacene (TIPS-pentacene) and poly(triarylamine) (PTAA) blend fabricated on rigid glass substrates or flexible polyethersulfone (PES) substrates. Changing from a glass substrate to a flexible one can be a challenging task as differences in surface energy and roughness of the substrate are likely to affect the properties of the semiconductor layer and consequently the performance of the transistor and its stability. We show that in these OFETs, compensating degradation mechanisms are introduced due to the use of a CYTOP/Al₂O₃ top gate dielectric bi-layer. Electrical stability under constant dc bias stress up to 24 h and under 20,000 cycles of the transfer characteristics was achieved without significant changes of mobility or threshold voltage. We also show that these OFETs are stable in air for up to 7 months. Furthermore, we verify the potential of these OFETs to form circuit components by connecting them to external load resistors, thereby creating a resistive-load inverter. We demonstrate that in such inverters the switching threshold voltage remained almost unchanged after a constant dc bias stress for 2 h due to the excellent electrical stability of the transistor.

11:00 AM

E4, Ambipolar Charge Carrier Transport in Organic Thin Films: *Dilek Isik*¹; Clara Santato²; ¹Département de Génie Physique – École Polytechnique de Montréal; ²École Polytechnique de Montréal

The study of ambipolar charge carrier transport in organic thin films transistors (OTFTs) is relevant to understand the device physics of light emitting organic transistors. Ambipolar OTFTs require injection of holes (h⁺) and electrons (e⁻), which translates into a good matching between the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) energy levels of the organic semiconductor and the work function of the electrodes used for h⁺ and e⁻ injection. Within this context, we report on two cases of study. The first case concerns a novel class of S-oxide and S,S-dioxide inner-core dithienothiophene oligomers showing tunable electron affinities and structure-property relationships in solution-deposited films¹. The second case concerns solution-deposited films of a pentacene derivative, 2,3-dicyano-6,13-bis-(triisopropylsilyl)ethynyl)pentacene (2,3-CN2-TIPS-Pn). In these films, a well balanced ambipolar charge transport is observed (the values of the h⁺ and e⁻ mobility are both about 2·10⁻³ cm²/Vs). The positions of the HOMO and LUMO of 2,3-CN2-TIPS-Pn with respect to the work function of the Au charge-injecting electrode and the arrangement of the molecules in the film, as deduced by grazing incidence X-ray diffraction analysis, contribute to explain the charge transport properties of 2,3-CN2-TIPS-Pn films². ¹C.Santato*, L.Favaretto, M.Melucci*, A.Zanelli, M.Gazzano, M.Monari, D.Ipýk, D.Banville, S. Bertolazzi, S.Loranger, F.Cicoira J. Mater. Chem. (2010) 20, 669-676. ²D. Ipýk, Y. Shu, G. Tarabella, N. Coppedè, S. Iannotta, F. Cicoira, L. Lutterotti, J. E. Anthony, C. Santato* Ambipolar organic thin film transistors based on a soluble pentacene derivative, accepted for publication in the journal Appl. Phys. Lett.

11:20 AM Student

E5, Application of Vapor Forms 1-Octanethiol Coated Copper Conductive Ink for Ink-Jet Printing: *Shinyoung Park*¹; Jinhyeong Kwon¹; Jaehak Her¹; Md. Momtunul Haque¹; Young-Suk Kim²; Caroline Sunyong Lee¹; ¹Hanyang University; ²Korea Electronics Technology Institute

Copper (Cu) nanoparticles are of great interest in various fields, especially in microprinting technology such as inkjet, letterpress, screen printing for application in printable electronics and etc. Among them, conductive inks and pastes used for printing various electronic components is the major application for Cu nanoparticles. However, Cu nanoparticles are easily oxidized and that has been a major obstacle. Until recently, researchers have tried to prevent Cu from oxidation by wet method and the wet method has several problems; such as short lifetime for oxidation, occurrence of hazardous chemicals, complex processes and etc. To overcome these problems, a vapor form of 1-octanethiol (CH₃(CH₂)₇SH) was coated as self-assembled multi-layers (SAMs) on the surface of Cu nanoparticles. Ultra high vacuum (UHV) condition (4.0 x 10⁻⁶ torr) was used to coat sub-100nm-sized Cu nanoparticles by bonding sulfur at the end of 1-octanethiol chain to the surface of pure Cu nanoparticles. We conducted ink-jet printing of Vapor formed 1-octanethiol copper conductive ink on glass to form Cu conductive patterns. The printing patterns were sintered by thermal treatment in hydrogen (H₂) atmosphere. In this study, TGA was used to find removal temperature of 1-octanethiol and sintering temperature of 100nm-sized Cu nanoparticles. Moreover, no residual 1-octanethiol after thermal treatment was confirmed through XPS analysis. As a result, the bonding structures between copper and sulfur can be successfully removed before sintering Cu patterns so that high density of copper line can be achieved. Furthermore, Resistivity of sintered Copper sample was measured to be 2.77 x 10⁻⁵ ohm-cm which is close to the reference resistivity value of copper lines. Therefore, this dry coating method has proven to be an alternative coating method for oxidation inhibition and for forming a successful inkjet-printed line.

11:40 AM E6, Late News

Session F: Devices Utilizing Low Dimensional Structures

Wednesday AM Room: Santa Barbara Harbor
June 22, 2011 Location: Univ. of California-Santa Barbara

Session Chair: Diana Huffaker, University of California, Los Angeles

10:00 AM Student

F1, Design and Growth of InAs Quantum Dash Based MWIR VECSELS: Victor Patel¹; Simon Reissmann¹; Thomas Rotter¹; Pankaj Ahirwar¹; Stephen Clark¹; Alexander Albrecht¹; Huiwen Xu¹; Christopher Hains¹; Larry Dawson¹; Ganesh Balakrishnan¹; ¹Center For High Technology Materials (CHTM), University of New Mexico

Antimonide Quantum Well (QW) based active regions currently dominate MWIR Vertical External Cavity Surface Emitting Lasers (VECSELS). The lack of etch stop layers in the antimonide material system (6.1 Å family) has made the fabrication of high power lasers rather difficult, since the high-power results depend on effective substrate removal techniques. The InAs Quantum Dash (QDash) based VECSEL can become an effective alternative to the antimonides due to the presence of very mature etch stop layers in the InP material system. QDash active regions exhibit broader gain bandwidth compared to QWs and therefore can result in superior tunability and mode locking. Furthermore, the QDash's highly coherent strain can help suppress the Auger non-radiative recombination and lead to more efficient MWIR lasers. The InAs nanostructures grown on lattice matched (Al_{1-x}Ga_x)_{0.47}In_{0.53}As buffers on InP substrates form asymmetric structures called Quantum Dashes in the Stranski Krastanov growth mode due to the 3.2% compressive strain with respect to InP. The three dimensional structures provide a way to release the compressive strain by elastic strain relaxation. Since the structures are free of dislocations, QDashes exhibit good optical properties. The Dashes are elongated in the [1-10] direction. Since InAs/InP are less mismatched alloys compared to InAs/GaAs they are capable of being grown with more InAs coverage, which results in emission wavelength covering 1.5 to 2.1 μm. The QDash based active regions have been used to realize 2 μm edge-emitting lasers. In this presentation we shall discuss the design and growth of a 2 μm InAs Quantum Dash VECSELS. This is grown as a bottom-emitting structure where the active region is grown on an InP substrate and the distributed Bragg Reflector (DBR) is grown on top. QDashes are incorporated in a 1% compressively strained quantum well to form a dashes-in-well (DWELL) based active region. The DWELL structure improves the carrier capture efficiency. Carriers that are captured in the QWs have a greater probability of being captured by the QDashes. A metamorphic AlSb/GaSb DBRs is utilized; this offers a better index contrast compared to lattice matched ternaries on InP. The chip is then mounted such that the DBR is bonded to a CVD diamond chip and the InP substrate is etched off.

10:20 AM Student

F2, Influence of Surface Patterning on Droplet Epitaxy and Photovoltaic Properties of InAs/GaAs Quantum Dots: Simon Huang¹; Jia-Hung Wu¹; Rachel Goldman¹; ¹University of Michigan, Ann Arbor

Quantum dot (QD) superlattices (SLs) have been proposed for improving solar cell efficiency by providing intermediate energy bands to allow sub-bandgap photon absorption [1], and to enhance the photocurrent in tandem solar cells [2]. Although photocurrent enhancement from QD-based solar cells has been demonstrated [3], QD cells usually exhibit lower open-circuit voltages (V_{oc}) and conversion efficiencies than the GaAs reference cells due to a bandgap reduction from the InAs QDs and their corresponding wetting layers (WLs). To avoid the limited QD density and the WL resulting from the misfit-driven Stranski-Krastanov QD growth process, we are pursuing an alternative approach, droplet epitaxy (DE). For DE of InAs QDs, nanoscale In droplets are deposited on GaAs and converted to InAs QDs via exposure to an As₂ flux. In this case, the QD size and density are determined primarily by the surface

droplet size and density, which are not limited by the misfit between the QD and host matrix. Thus, DE provides a means to achieve ultra-high densities of ultra-small QDs, expected to enhance absorption and cell performance. For this purpose, we have investigated the influence of In exposure time on QD sizes and densities, revealing an increase in QD size homogeneity with decreasing In exposure. Specifically, for 2.5 ML equivalent of In deposition, a uniform distribution of QDs with an average diameter of ~20 nm is observed. To date, we have identified the appropriate In exposure time and substrate temperature to produce QD densities in excess of 3x10¹⁰ cm⁻². To further enhance the QD densities while maintaining a specific spatial arrangement of QDs, we are also exploring the influence of surface patterning on the formation of InAs/GaAs QDs by DE. For a buffer consisting of 2 ML equivalent of In deposited on GaAs at 100°C, a high density of mounds elongated along [-110] is apparent. These mounds are expected to enhance the QD densities due to preferential nucleation of QDs at the mound edges [4]. The effects of GaAs droplet homoepitaxy nano-mound templates on the sizes, densities, and spatial arrangements of InAs QDs will be presented. In addition, we will discuss the influence of DE QD active regions on the photovoltaic properties of p-i-n structures.

10:40 AM Student

F3, Novel 3-State Quantum Dot Gate FET in Silicon-on-Insulator Substrate: Supriya Karmakar¹; John A Chandy¹; Faquir C Jain¹; ¹University of Connecticut

According to Moore's law, semiconductor industries move from small scale integration (SSI) to ultra large scale integration (ULSI) technology. Nowadays, semiconductor industries move to nanometer scale integration. There are so many state of art issue in nm scale integration than large scale integration. One way to overcome this problem can be to fabricate novel device using conventional CMOS process which can handle more number of bits. Our work can highlight on that solution to some extent. In this paper, we demonstrate the three state behavior of quantum dot gate field effect transistor (QDFET) on silicon-on-insulator (SOI) substrate. A conventional field effect transistor (FET) acts like a switch which produces only two states in their transfer characteristics based on the input gate voltage. The structural difference between conventional FET and QDFET is the presence of two layers of quantum dots on top of the gate insulator in the QDFET. The HRTEM image shows the presence of two layers of quantum dots in the gate region of a fabricated QDFET device. The presence of quantum dots in the gate region, produces one intermediate state "i" in the QDFET, between it's ON and OFF state. The transfer characteristics shows a very little change of drain current (ID) with respect to gate-source voltage (VGS) of a QDFET in the intermediate state. The self consistent Schrödinger and Poisson Equation solution shows that, as the gate-source voltage increases, the tunneling of charge carrier from the inversion channel to the different layers of quantum dots in the gate region, changes the threshold voltage of a QDFET which produces the intermediate state "i". The presence of three states in their transfer characteristics, enable this device to handle more number of bits in multivalued logic circuits. Besides this, we can design compact comparator circuit which decreases device count 32:1 compared to conventional comparator circuit. They are also useful to design resistor free analog-to-digital converter (ADC) circuits which can resolve R-2R ladder problem. In this work, we fabricate QDFET on SOI substrate to get better isolation between individual FET for integrated circuit application.

11:00 AM Student

F4, Visible Light Emitting Diodes Based on Self-Assembled In_{0.5}Ga_{0.5}As Quantum Dots on GaP: Yuncheng Song¹; Paul Simmonds¹; Minjoo Lee¹; ¹Yale University

We report the growth and fabrication of light-emitting diodes (LEDs) based on buried In_{0.5}Ga_{0.5}As self-assembled quantum dots (SAQDs) on GaP (001) substrates. Although GaP has been grown on Si with minimal anti-phase disorder and low extended defect densities, [1,2] its indirect bandgap makes it unsuitable for most photonic device applications. We recently demonstrated the growth and luminescence properties of In_{0.5}Ga_{0.5}As SAQDs on GaP (001) as a new approach to achieving efficient light emission on GaP.[3] We grew various coverages of In_{0.5}Ga_{0.5}As on GaP buffers,

capped with 85 nm GaP. Dot densities and average dot dimensions were estimated by plan-view TEM. Cross-sectional TEM showed strain contrast typical for buried SAQDs, while the presence of a wetting layer confirmed the Stranski-Krastanov growth mode. Numerous two-beam imaging conditions showed no evidence of dislocations in either the SAQDs or the GaP cap. Photoluminescence (PL) spectroscopy was performed at 80 K using a 404 nm pump laser. SAQD-containing samples exhibited intense, single-peak PL emission, while GaP buffer layers without SAQDs showed only broad, overlapping defect peaks. We speculate that the radiative recombination process in the SAQDs is significantly faster than other defect-mediated radiative recombination occurring either in the substrate or the epitaxial GaP layers. By increasing the $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ coverage from 2.0-11.0 ML, the PL peak energy could be red-shifted from 2.00 eV to 1.88 eV, which we attribute to an increase in average SAQD size. For the highest $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ thicknesses studied, we observed a ~ 5 times decrease in PL intensity compared with that from the 5.0 ML sample, likely due to dislocation nucleation. Across our samples, the FWHM of PL peaks was 115-125 meV resulting from the relatively large SAQD size variance. An LED structure consisting of a semi-insulating layer of $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ SAQDs embedded within the i-region of a GaP p-i-n diode was grown to investigate electroluminescence (EL) properties. Testing was performed at 80K, and for a given P-I-N sample, similar peak energies were measured with both EL and PL. Both PL and EL emission was visible to the unaided eye in room light. We are currently investigating the possible use of $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}/\text{GaP}$ SAQDs for laser applications. Initial results in which our $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}/\text{GaP}$ SAQDs are incorporated into a micro-disc cavity will be presented. We believe that this work serves as a starting point for a new approach to III-V optoelectronic device integration on Si.

11:20 AM Student

F5, Large Area Growth of GaAs Solar Cell Based on Nanowire Structure: *Chun-Yung Chi*¹; Anuj Madaria¹; Maoqing Yao¹; Ruijuan Li¹; Chongwu Zhou¹; Paul Dapkus¹; ¹University of Southern California

III-V compound semiconductor nanowires are expected to provide excellent performance in photovoltaic applications, because of their superior light absorption and excellent carrier transport properties. Nanowire structure can also help increase light absorption rates by re-absorbing reflected light from nanowire facets and release strain due to a dissimilar lattice constant which has made high-quality III-V compound semiconductor growth possible on a Silicon substrate. Although selective-area growth for nanowire can avoid unintentional doping from a catalyst, compared to vapor-liquid-solid growth, nano mask preparation for selective-area growth takes a long time with electron-beam lithography, which makes large area growth of nanowire difficult. We have successfully fabricated a large-area GaAs nanowire growth using a novel lithography: nano-sphere lithography. In this paper, we describe nano-sphere lithography, which can shorten the processing time of selective-area growth samples and thus make feasible the growing of large samples of nanowires, including wafer scale samples. GaAs nanowire growth on a Silicon (111) substrate has been studied: different sample treatments and growth conditions have been investigated and revealed that the atomic flatness of a Silicon substrate is essential for vertical and uniform nanowire growth. GaAs nanowire growth has also been achieved on both nano-sphere patterned and electron-beam patterned GaAs (111)B substrates. Optical results demonstrate the enhancement of light absorption with a nanowire structure, and the extent of enhancement is close to the simulation result. Electrical measurements of nanowires, including doping level and resistivity, will also be detailed in this paper.

11:40 AM Student

F6, Output Polarization Dependence of Asymmetric Current Injection VCSELs on Crystalline Direction and Ion Implantation: *Yan Zheng*¹; Chin-Han Lin¹; Matthias Gross²; Larry Coldren¹; ¹University of California Santa Barbara; ²Ziva Corporation

Vertical-cavity surface-emitting lasers (VCSELs) have emerged as a valuable platform because of their reliability, high-speed characteristics, and ability for on-chip integration. Recent work has also demonstrated the possibility

of output polarization control. By leveraging the advantages of the VCSEL platform, innovative solutions in imaging, sensing and military applications are possible. We demonstrate control between two orthogonal polarization states via asymmetric current injection (ACI) utilizing a novel dual intracavity contacted circular mesa design. Modulation doping is used in the contact layer to reduce optical loss. Deuterium (D^+) isolation implantation in the p-contact layer was also investigated to reduce lateral current spreading. Devices were grown using molecular beam epitaxy (MBE) on undoped (001) GaAs starting with 18 periods of GaAs/AlAs for the bottom DBR mirror followed by 420nm of Si doped GaAs for the n-contact layer. The p- and n-contact layers were grown close together to increase current directionality. The active region consists of three 8nm thick $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ quantum wells separated by 8nm GaAs barriers surrounded by a $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ separate confinement heterostructure (SCH). Due to the large optical field in the p-contact region, only the standing wave nulls were doped to reduce free carrier absorption. Carbon was used in this modulation doping scheme because of its low diffusivity. The top mirror consists of 32 periods of 85% AlGaAs/GaAs. A wedding cake structure is created using standard lithographic procedures and an oxide aperture is created through a wet oxidation process. Metal contacts are laid out in a cross pattern to separately inject current in two orthogonal directions. The whole cross layout is also rotated relative to the crystal axis to investigate its effect on output polarization. Deuterium was also implanted into the p-contact layer in areas that straddle current injection paths to reduce lateral current spreading. Light output (LI) first passes through a focusing lens/rotating polarizer combination and is then measured by a Si photodetector. Each arm of the diode is biased separately and the output polarization is measured. A measured phase difference of 90° means that the two outputs are orthogonally polarized relative to each other. By rotating the current injection directions relative to the crystal axes it was found that the amount of splitting between the two polarization states follows a $\cos^2(\alpha)$ dependence. The largest offsets between polarization states occurred every 90° with respect to the $\langle 110 \rangle$ axis. Minimal polarization phase offsets were found to occur when current was aligned to the $\langle 010 \rangle$ and $\langle 100 \rangle$ directions. For one device that did not display polarization splitting from ACI as grown, after D^+ implantation the output polarization showed a polarization phase offset of approximately 90° , demonstrating the ability to suppress crosstalk between polarization paths with ion implantation.

Session G:

Photovoltaics: New Materials and Characterization

Wednesday AM
June 22, 2011

Room: State Street
Location: Univ. of California-Santa Barbara

Session Chairs: Jerry Woodall, Purdue University; David Janes, Purdue University

10:00 AM Student

G1, Molecular Beam Epitaxial Growth of $\text{Zn}_3\text{P}_2/\text{GaAs}$ and ZnS/GaAs Heterostructures for Photovoltaics: *Jeffrey Bosco*¹; Gregory Kimball¹; Harry Atwater¹; ¹California Institute of Technology

The prospect of terawatt-scale PV requires a low-cost, earth abundant photovoltaic material with excellent optoelectronic properties. Zinc phosphide (Zn_3P_2) is a strong candidate for an efficient thin-film absorber, with a direct band gap of 1.5 eV and long minority-carrier diffusion lengths ($>5\mu\text{m}$). Due to difficulties in achieving n-type conductivity, previous research focused on the performance of Mg-Schottky diodes fabricated on Zn_3P_2 wafers. However, device efficiencies were limited by reflection losses from Mg-metal and poor barrier formation resulting from interface states. In order to avoid these issues, we propose the fabrication of Zn_3P_2 solar cells implementing an n-type heterojunction partner. Zinc sulfide (ZnS) is an attractive heterojunction partner with a wide band gap (3.6 eV), high achievable donor concentrations ($>10^{18}$), and a low electron affinity (3.9 eV). In this work, we report epitaxial growth of Zn_3P_2 and ZnS on GaAs(001) substrates by molecular beam epitaxy

(MBE). GaAs was chosen as a growth substrate since the phosphorus sublattice of α -Zn₃P₂ is similar to that of arsenic and the room-temperature lattice mismatch is less than 1.3%. Films of approximately 0.1 to 1 μm in thickness were grown with substrate temperatures ranging from 50 to 350°C. Prior to deposition, an arsenic-free substrate pretreatment was used to create a smooth epi-ready surface. This procedure was similar to those employed for epitaxial growth of II-VI compounds on GaAs. Surface evolution during growth was monitored using reflective high energy electron diffraction (RHEED). The optimum epitaxial growth window for each material was determined via *ex situ* structural and optoelectronic film characterization. The Zn₃P₂ growth rate varied with both substrate temperature and Zn/P beam flux ratio, with typical rates falling between 0.05 and 0.2 nm-s⁻¹. RHEED studies demonstrated both polycrystalline and amorphous growth at temperatures below 300°C. Highly crystalline three-dimensional growth was obtained via appropriate control of substrate temperature and Zn/P flux ratio. Epitaxial growth of zincblende ZnS was possible at substrate temperatures as low as 50°C. For both materials, the Zn sticking coefficient dominated the growth rate at higher temperatures. Film orientation was confirmed by high resolution X-ray diffraction (HRXRD) measurements. For Zn₃P₂/GaAs(001), (201) and (004) orientations were observed with the (004) peak dominating at higher growth temperatures. The Zn(002) peak was occasionally observed for films grown at sub-optimal Zn/P flux ratios. Alternatively, for ZnS/GaAs(001), only the (002) and (004) peaks were observed over the entire range of growth conditions. In addition to HRXRD, film orientation and composition were further investigated using transmission electron microscopy (TEM) and X-ray dispersive spectroscopy (EDS). Finally, Hall Effect measurements were performed to assess the electronic properties of the films. This approach allows us to achieve low defect, electrically active semiconductor films, and ultimately efficient ZnS/Zn₃P₂ heterojunction solar cells.

10:20 AM

G2, ZnSnN₂: A New Earth-Abundant Semiconductor for Solar Energy Conversion: *Lise Lahourcade*¹; Naomi Coronel¹; Harry Atwater¹; ¹California Institute of Technology

The grand challenge of terawatt-scale solar energy conversion motivates a search for new materials that can simultaneously meet a high efficiency, material abundance and low cost. Since current compounds such as CdTe and Cu_x(In_yGa_{1-y})₂Se₂ face scalability and cost challenges, we are looking for alternative earth-abundant semiconductors to meet these demands. In this context, we investigate Zn-IV-N₂ compound materials. Here, we report the first successful synthesis of ZnSnN₂, a potential photovoltaic semiconductor. The few studies of Zn-IV-N₂ materials predict direct band gaps of 1.37 eV, 2.87 eV and 4.42 eV for ZnSnN₂, ZnGeN₂ and ZnSiN₂ respectively. Hence, similar to their III-N counterparts, they have potential for optoelectronic applications throughout the visible spectrum. In particular, the band gap of ZnSnN₂ matches the solar spectrum, making it a good candidate as an active absorber layer in a solar cell. Calculations also indicate that the band alignment of ZnSnN₂ and ZnGeN₂ is type II, suggesting the possibility of photovoltaic heterojunction devices, designed for direct charge separation at the ZnSnN₂/ZnGeN₂ interface. In this work, we report on the synthesis and physical properties of ZnSnN₂ grown by reactive RF sputtering on *c*-plane sapphire substrates. Thin films were synthesized from a 50:50 at.% ZnSn target, under 7 mTorr of an Ar:N₂ plasma, at various temperatures and Ar:N₂ ratios. From X-ray reflectivity measurements, we calculated a growth rate of about 1 nm/min for deposition in a 50% N₂ plasma. Energy-dispersive X-ray analysis indicates a Zn:Sn:N ratio of approximately 1:1:2 at.% for room temperature growth, and shows a decreasing Zn concentration with increasing temperature due to the high vapor pressure of Zn. Moreover, X-ray θ -2 θ measurements of all samples give rise to reflections attesting to the synthesis of orthorhombic ZnSnN₂ on *c*-plane sapphire with the lattice parameters expected from the literature¹. Room temperature samples exhibit amorphous and polycrystalline features with the coexistence of (210), (002), (021) and (400) orientations. However, increasing the growth temperature tends to favor epitaxy in the (021) orientation relative to the others. Room temperature Hall measurements indicate *n*-type films with an electron carrier concentration of about $n = 8 \times 10^{18} \text{ cm}^{-3}$, and a mobility of $\mu_n = 45 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$. Additionally, initial IR transmission measurements indicate that the

direct band gap lies at approximately $E_{\text{dir}} = 1.56 \text{ eV}$ for these ZnSnN₂ layers. We will report a comprehensive analysis of the composition and phase of the as-deposited layers determined from X-ray diffraction and energy dispersive X-ray spectroscopy, and further dielectric function information for ZnSnN₂. We will also present electron microscopy measurements to understand the growth morphology.

10:40 AM Student

G3, Electrodeposition of Indium Sulfide Films from Organic Electrolytes: Robert Engelken¹; Jason Newell¹; *Maqsood Mughal*¹; John Hall¹; Joshua Vangilder¹; Frederick Felizco¹; ¹Arkansas State University

We report research on electrodeposition of indium sulfide films. In₂S₃ has received attention as an alternative to CdS buffer layers in heterojunction solar cells [1]. Although having a 2.0 eV bandgap relative to CdS's 2.5 eV value, the lower toxicity and environmental impact of indium relative to cadmium, and significant photosensitivity, compel continuing research. Innovations with such may also translate into improved electrodeposition of CuIn₃Se_{2-x}. Numerous organic and organic/aqueous baths were investigated. Organics included various glycols, triethanolamine, dimethylsulfoxide, propylene carbonate, formamide, N, N-diethylformamide, N, N-dipropyl formamide, and propionic acid. Solutes consisted of 0.05 M InCl₃ and 0.1 M NaCl, and molecularly dissolved sulfur (gross molarity 0.1). Sulfur usually only partially dissolved to yield saturated yellow solutions. With pure organics, temperatures were 100-170°C, limited by solvent boiling and charring. Voltages ranged between -0.6 V and -1.2 V (vs. Ag/AgCl with a filling solution of ethylene glycol saturated in KCl). Substrates included indium tin oxide-coated glass, molybdenum, and titanium, with graphite or indium anodes. Rapid stirring was used. Deposition was sluggish in all electrolytes. Some yielded no deposition, while some yielded mixed indium sulfide phases, delimited by yellow In₂S₃ and brown InS. Uniformity was typically poor, with some regions on the cathode plated and others devoid of deposit. The best films were deposited from formamide baths. However, these decompose at temperatures above 150°C, yielding In₂S₃ insolation. Also, toxicity may be a concern. The next best baths were ethylene glycol and 1, 2-propanediol, from which golden-yellow films were deposited. Brown InS films were sometimes deposited with temperatures near 100°C, or large currents. Uniformity was improved with an initial 20-second indium "flash" at voltages negative of -1.0 V to establish closely-spaced nucleation sites. Cyclic voltammetry elucidated reversible potentials for deposition, spurious reactions, and photoactivity from chopped white illumination. Although uniformity and color were better with pure organics, the greatest photocurrents were observed with a mixed bath containing ethylene glycol, propionic acid, and water. Voltammograms indicated sluggish indium/indium sulfide deposition on the cathodic sweep, but anodic photocurrents on the reverse sweep, consistent with In₂S₃'s *n*-type conductivity. Research is ongoing, with plans to investigate indium sulfamate as a solute, since aqueous indium sulfamate baths are excellent for indium metal plating. Electroplated indium sulfide films will then be mated with CdTe and CuInS₂ layers to form heterojunctions for characterization of photovoltaic performance. This work is jointly sponsored by EPSCoR grants from NASA and NSF, with administration through the Arkansas Space Grant Consortium and the Arkansas Science and Technology Authority, respectively.

11:00 AM

G4, Spatially Resolved Responses of Nanoscale Photovoltaic Model Devices: *Thomas Dufaux*¹; Jens Boettcher¹; Jens Dorfmueller¹; Ralf Vogelgesang¹; Marko Burghard¹; Klaus Kern¹; ¹Max Planck Institute for Solid State Research

Nanoscale materials are promising for improving the performance of optoelectronic devices. One example are nano-structured solar cells comprising vertically aligned arrays of nanowires [Nano Lett. 2006, 6, 215]. In this manner, a high surface area is combined with separated pathways for electron and hole transport, thus limiting losses due to recombination. However, the performance of the entire solar cell depends on the efficiency of each single element in such an array. In order to further enhance the efficiency of nano-structured solar cells, it is hence important to first optimize these single elements. A useful technique to study a single, nanoscale, photoactive interface

is scanning photocurrent microscopy (SPCM) [Nano Lett. 2005, 5, 507]. Herein, a focused laser spot is scanned across the sample surface while the photocurrent is measured as a function of illumination position. In parallel, also a reflection image is recorded. By overlapping the two types of images, features in the spatially resolved photocurrent can be directly correlated with the structures on the sample. Graphene has emerged as a novel promising electrode material. Its high transparency and excellent electrical conduction makes it a good candidate to replace other transparent electrode materials like indium tin oxide (ITO). However, it is difficult to obtain a high quality electrical connection between a sp²-bonded carbon material and a semiconductor without disrupting the carbon framework. Accordingly, studying this interface is important for further improving the performance of nano-structured solar cells based on graphene electrodes. We investigate the photoelectric properties of the interface between graphene and Cadmium Sulfide (CdS) as a widely used II-VI semiconductor [Small 2010, 6, 1868]. In this model system, a CdS nanowire serves to transport electrons to the opposite metal contact. In the corresponding SPCM map a photo response appears at the intersection of the CdS NW and the graphene flake. By chemical tailoring of this interface the short circuit current can be increased by a factor of hundred. Some of these nanoscale solar cells show additional photoresponses at the metal edges of the contacting electrodes which can be explained by the excitation of surface plasmons. We exploit this effect to fabricate an electrical surface plasmon (SPP) detector [APL 2010, 97, 161110], in which a surface plasmon is launched at a small grating on an aluminum stripe. The SPP propagates along the metal until it intersects with the Schottky contact of a CdS nanowire. There, the electrical field of the surface plasmon excites charge carriers which are separated in the field of the electrical contact, yielding an electrical current, even under zero source-drain bias.

11:20 AM Student

G6, Challenges of Hall Measurements on Low Mobility Materials and How to Overcome Them: *Jeffrey Lindemuth*¹; Shin Mizuta²; ¹Lake Shore Cryotronics; ²Toyo Corp

Making Hall measurements of amorphous materials, organic materials or other low mobility materials is known to be very difficult¹⁻³. There are two intertwined problems for Hall measurements on these materials. The first is an instrument problem. Experience has shown that instruments do not provide reliable results when making Hall measurements of materials with high resistivity and low mobility materials. In these materials, the true Hall voltage is often overwhelmed with large offset voltages. A common example of this is the anomalous sign of the carrier as measured by the Hall effect. Repeated measurements of the small Hall voltage can often give conflicting signs of the Hall voltage due to noise and large offset voltages in the measurement. If the measured sign of the Hall voltage is ambiguous, then assigning an anomalous sign of the carrier to material properties is dubious at best. Experiences like this have dispelled researcher's confidence in the capability of these instruments to perform said measurements. The second problem is that even with perfect Hall measurements, transport properties in these materials are not always as simple to characterize, or as easily understood as transport properties in semiconductors. To overcome these problems, first it is necessary to explicate and demonstrate a method that produces reliable, consistent results for Hall measurements of low mobility materials. With this knowledge, the researcher can then begin to confidently attribute "strange" results to the material, rather than to the instrument. We propose a method using AC magnetic fields for measuring the Hall effect in low mobility materials. The Hall voltage is measured using phase sensitive detection. With this method, it is possible to separate, in frequency space, the unwanted offset voltages from the desired Hall voltage. In addition, the desired Hall voltage is separated from the inductive voltage in phase space. We have calculated the limits of the measurement method and show measurements of amorphous and microcrystalline silicon which confirm these limits. AC field Hall can expand the limits of mobility that can be reliably measured by a factor 100 or more.

11:40 AM G6, Late News

Session H: III-Nitrides: Electronics I

Wednesday PM
June 22, 2011

Room: Flying A
Location: Univ. of California-Santa Barbara

Session Chairs: Edwin Piner, Texas State University; Michael Manfra, Purdue University

1:30 PM Student

H1, Quantization and Bias Effects on Gate Capacitance of Scaled GaN HFETs: *Vincent Lee*¹; Atsushi Ohoka¹; Lingquan Wang¹; Peter Asbeck¹; ¹University of California, San Diego

In this paper, we show that in recent highly-scaled, high f_T GaN HFET designs, the gate capacitance is expected to decrease by up to 20-25% compared to classically expected values, due to quantization and bias effects on carrier distribution. Quantum confinement effects for a representative HFET structure are simulated using a self-consistent 1D Poisson-Schrödinger solver, including, for the first time, the effects of electron heating due to fields in the source-gate region, and drain bias. The reduced capacitance is expected to decrease FET transconductance. Quantization of electron states within a FET channel is widely known to reduce gate capacitance. For Si MOSFETs, quantum effects must be considered to model devices with relatively thin gate oxides (< 2nm). Effects of finite density of states (DOS) are even more severe in GaN. Unlike silicon which has six conduction band minima, GaN only has one; also, it has a smaller DOS electron effective mass. Traditionally, GaN HFETs have relatively thick barrier layers of ~20nm AlGaIn, corresponding to effective oxide thickness (EOT) ~8nm. However, as device dimensions are scaled down, dielectric thickness in recent experimental GaN HFETs has been dramatically reduced to maintain control of short channel effects. Consequently, the gate-to-channel distance has reached 6nm (EOT~2nm). Thus, the adverse impacts of finite DOS and other quantum effects in scaled HFETs have now increased. Our representative HFET structure consists of 2.5nm GaN cap/2nm AlN barrier/20nm GaN channel/Al_{0.08}Ga_{0.92}N buffer, with EOT corresponding to ~2nm. Using a self-consistent 1D Poisson-Schrödinger solver that considers all relevant subbands, quantum states in the channel are simulated to find the dependence of sheet carrier density (N_s) on gate bias and to extract effective gate capacitance $q(dN_s/dV_g)$. Capacitance is affected by finite DOS in GaN, separation between 2DEG and AlN/GaN interface, and by electron heating. For the simulated HFET structure, the centroid of charge distribution lies ~1nm from the AlN/GaN interface, which is larger than classical Poisson expectations. With increasingly high drain bias, channel electron density decreases with diminishing contribution from drain-to-source moving electrons. Capacitance further decreases from electron heating effects. For GaN, electron temperature distribution is likely to shift above 300K, since electron heating often occurs due to electric fields in source-to-channel access region and in the channel. Overall, average electron heating, finite depth of wave function centroid and finite DOS contribute to a decrease in capacitance of order 20-25% for the representative structure, compared to classical considerations. The total reduction in gate capacitance undermines the transconductance of the FET by weakening the gate modulation of channel carrier density. The overall input capacitance also decreases, although this effect may be considerably masked by parasitic capacitances. The primary impact of reduced capacitance is decrease in transconductance for scaled HFETs.

1:50 PM Student

H2, Direct Correlation between E_c -0.57 eV Trap Generation and Field-Induced Degradation in AlGaIn/GaN High Electron Mobility Transistors: *Anup Sasikumar*¹; Aaron Arehart¹; Stephen Kaun²; Man Hoi Wong²; James Speck²; Umesh Mishra²; Steven Ringel¹; ¹The Ohio State University; ²University of California, Santa Barbara

Deep levels are prominent and mostly undesirable in wide band-gap devices, especially AlGaIn/GaN high electron mobility transistors (HEMTs). These

levels are considered responsible for RF-to-DC dispersion, knee-walkout, and threshold voltage V_T shifts among other reliability issues in HEMTs¹. In order to address such reliability issues, it becomes imperative to understand these levels and the role they play in HEMT degradation. Here we perform constant drain current-based deep level optical and (thermal) transient spectroscopy² (CI_D -DLOS/DLTS) on AlGaIn/GaN HEMTs before and after electrical DC stressing to investigate the impact of stress and its correlation to defects within the material structure. The HEMTs in this study are 30 nm $Al_{0.3}Ga_{0.7}N/800$ nm GaN structures grown on 4H-SiC using plasma assisted molecular beam epitaxy (PAMBE). The access regions were passivated with 180 nm of SiN_x using plasma enhanced chemical vapor deposition. A typical device had a $V_T = -4.5$ V and a maximum drain current of 1.1 A/mm at $V_{GS} = 0$ V. These HEMTs were subjected to semi-on DC stressing for 13 hours with $V_{GS} = -2.25$ V, $V_{DS} = 17.5$ V, and $I_{DS} \sim 0.45$ A/mm and compared to unstressed devices with nearly identical electrical behavior. Constant current-based drain-access sensitive 'drain-lag' measurements reveal a dominant exponentially decaying transient with time-constant $\tau \sim 30$ ms. This transient has been observed previously^{3,4} and attributed to a $E_C - 0.57$ eV electron trap physically located in the HEMT access region. These previous studies^{3,4} were performed on AlGaIn/GaN HEMTs from three different sources grown by metalorganic chemical vapor deposition (MOCVD). In this work, on PAMBE HEMTs, the signature $E_C - 0.57$ eV drain-lag signal increased by $\sim 2x$ post-DC stressing similar to the Arehart *et al.*³ report on MOCVD HEMTs post-RF stressing. Drain access sensitive CI_D -DLOS measurements revealed even deeper levels at $E_C - 1.3$ eV and $E_C - 3.8$ eV matching previous results for AlGaIn⁵ with total trap concentrations $n_T \sim 9 \times 10^{12}$ cm⁻² that remained unaffected by DC-stressing. Room temperature 500 ns pulsed I - V show a knee-walkout in the DC stressed sample with negligible V_T shift. The knee-walkout in the pulsed I - V observed in the stressed sample suggests an increase in drain access resistance. The negligible change in deep trap concentrations extracted from CI_D -DLOS values suggests that observed knee-walkout in the pulsed I - V measurements was mostly due to the $E_C - 0.57$ eV electron trap thereby directly correlating it with HEMT degradation. We are presently performing under-gate sensitive CI_D -DLTS/DLOS to probe deep traps in the gated region and better understand the negligible V_T -shift post DC-stressing.

2:10 PM Student

H3, Temperature Dependent Off-State Degradation of AlGaIn/GaN HEMTs: Erica Douglas¹; C. Y. Chang¹; Lu Liu¹; S. J. Pearton¹; F. Ren¹; ¹University of Florida

AlGaIn/GaN High Electron Mobility Transistors (HEMTs) have garnered a great deal of interest due to their high performance capabilities. As this technology has become a key component for high frequency and high power applications, the need to understand the degradation mechanisms that affect the long-term reliability has become increasingly important. High power operation requires the use of large voltages, which in turn results in considerable electric fields in the device. Previous studies have shown an electric field driven degradation mechanism under high reverse gate bias. Under high reverse gate bias, gate leakage current in AlGaIn/GaN HEMTs is seen to steadily increase. Once a critical voltage (VCRI) is reached, the gate leakage currents increase by up to several orders of magnitude. This sharp rise in current has been attributed to the inverse piezoelectric effect. High reverse gate bias step-stress from -10 V to -42 V on AlGaIn/GaN HEMTs were performed and resulted in an increase in gate leakage current about 5 orders of magnitude, with a sharp one order of magnitude increase in current at the critical voltage. Numerous devices were step-stressed at temperatures ranging from 25°C to 150°C. During elevated temperature stress tests, AlGaIn/GaN HEMTs were found to exhibit a negative temperature dependence of the critical voltage (VCRI) for irreversible device degradation to occur during bias-stressing. VCRI follows a log relationship of the form $VCRI = V_0 \exp(-E_a/kT)$ where the activation energy is 38 meV and the value for V_0 is around -28 V at room temperature in our devices. Though the stress temperatures were well below reported thermal instability for Ni/Au on AlGaIn, previous research has shown consumption of a native oxide layer between the Schottky contact and AlGaIn layer after high reverse gate bias stress at room temperature. At elevated temperatures, devices exhibited similar

gate leakage currents before and after biasing to VCRI, independent of both stress temperature and critical voltage, indicating a current-driven degradation mechanism. Gate and drain lag measurements were also performed of devices stressed at elevated temperatures in order to further investigate the role of shallow and deep traps. For devices stressed at 40°C, gate lag increased five times the original value of fresh devices while drain lag increased by more than twice the unstressed value. As stress temperature increased to 150°C, gate and drain lag show an exponential decay.

2:30 PM

H4, Noise Measurements of Nanowire FET Sensors for Sensitivity Determination: Devin Rourke¹; Mary Rowe¹; Paul Blanchard¹; Aric Sanders¹; Kristine Bertness¹; Norman Sanford¹; ¹NIST Boulder

We investigate a bio-molecule sensing scheme where the conducting channel of a functionalized nanowire (NW) field-effect transistor (FET) can be gated by the presence of a charged analyte. The favorable geometry of these NW sensors leads to a promise of single molecule detection sensitivity. Although sensor devices based on NWs have been demonstrated and their basic operating principles have been realized, sensor sensitivity and selectivity remain important areas of ongoing study. There are two elements that determine the sensitivity of these devices: the device noise and the signal size for single molecule detection. These factors can be combined to determine a sensor's sensitivity number, i.e. the lowest number of molecules that can be detected. We present noise measurements performed on bioFET devices that demonstrate this sensitivity metrology. Test structures were fabricated with c-axis MBE grown GaN NWs that are described at length elsewhere^[1]. Nanowires were released from their growth substrate into isopropanol via ultrasonic agitation, forming a suspension of wires that was then pipetted and aligned using dielectrophoresis onto photolithographically-deposited Ti pads. The resulting two-terminal bridge structure was capped with a layer of Ti/Al, pinning the wires to the substrate and forming two conformal electrical contacts. A protective SiN_x hard mask was deposited over the entire device, and functionalization windows above the NW surface were etched. We measured the current noise spectrum by applying a voltage to our device in series with a measurement resistor, whose resistance was approximately matched to the device resistance. The voltage across the device alone ($V_{bias} = 1.0$ V) was offset, amplified, and filtered before being measured by a spectrum analyzer. Using the known circuit resistance values the measured voltage noise was converted to current noise. The current noise spectral density, S_p , followed a $1/f$ frequency dependence. Using the parametrization of $S_i = B^2/f$ we found that $B = 8 \times 10^{-10}$ A. The contribution to the channel current from a single carrier induced by a single surface charge is $\Delta I_1 \sim \mu e V_{bias} / L_2$. Here μ , e , and L are mobility, single charge, and wire length. Using $\mu = 500$ cm²V⁻¹s⁻¹ [2] and $L = 5.8$ μ m we found $\Delta I_1 = 0.2$ nA. The value of B needed for single molecule detection is $B_1 = 0.2 \Delta I_1 = 4 \times 10^{-11}$ A^[3]. The sensitivity number of our device, which is the ratio of the measured B coefficient and B_1 , was therefore 20. The noise level of shorter devices has yet to be investigated, but this is one possible approach to improving device sensitivity toward single-molecule detection.

2:50 PM Student

H5, Piezoresistive Microcantilever with Embedded AlGaIn/GaN HFET for Sensing Applications: Muhammad Qazi¹; Md. Nomani¹; Goutam Koley¹; ¹Department of Electrical Engineering, University of South Carolina

GaN based materials have attracted wide research interest in optoelectronics and high power microelectronic devices because of their exceptional physical and chemical properties. Additionally, GaN related materials exhibit high mechanical and thermal stability coupled with piezoelectric properties which make them strong candidate for miniaturized sensors for harsh environments. An important property of AlGaIn/GaN heterostructure that has opened up the possibility of its integration with microelectromechanical systems (MEMS) for sensing application is its strain dependent 2-dimensional electron gas (2DEG). In this work, we have investigated the effect of cantilever bending on the 2DEG of AlGaIn/GaN HFET embedded on a microcantilever and its applicability as a transducer element for microcantilever based sensors. AlGaIn/GaN HFETs were fabricated at the base of GaN microcantilevers with dimensions

350µm×50µm×2µm fabricated from AlGaIn/GaN wafer grown on (111) silicon substrate. AlGaIn/GaN HFETs were fabricated using common lithographic process followed by cantilever release through anisotropic Si etch (Bosch process) from the back side, through the wafer. The Id-Vg measurements on the AlGaIn/GaN HFET indicated that the threshold voltage and 2DEG carrier mobility were $V_{th} = -2$ V, and $\mu = 110$ cm²/Vs; C-V measurements showed that the 2DEG sheet carrier concentration was 3.3×10^{12} cm⁻². The output characteristic (Id-Vd) curves were measured in lighted conditions with 20 and 40µm downward bending for gate biases of 0 and -0.6V. The drain current of the HFET increased with downward bending of the cantilever and the change in drain current was 0.08 % per 1/956m bending for zero gate bias. With lower gate bias of -0.6V the 2DEG concentration reduced, resulting in higher change in drain current with bending (0.15% change for 1 µm bending). For zero gate bias, the gauge factor $[(\Delta R/R)/\epsilon]$ was -42.25. Whenever the cantilever is bent downward, both the AlGaIn and GaN layers undergo tensile stress (compressive stress for upward bending) and additional bending induced piezoelectric polarization is introduced in both the layers. Due to the difference in the piezoelectric constants of AlGaIn and GaN, the 2DEG density in the channel increases, reducing the channel resistance. DC Drain current transients were also measured at $V_d = 2$ V, and the responses for upward and downward bending of the cantilever by 50µm, were recorded. Interestingly, the drain current changed sharply with cantilever bending, but returned back slowly to almost its original value. The changes in drain current for upward and downward bending of cantilever were found to be asymmetric, and this asymmetry was affected by the gate bias. To investigate the effect of bending in absence of current collapse we also performed ac drain current measurements at 0.8 V rms and 1 kHz, which led to a sensitivity of 0.043% drain current change per 1µm bending, and no transients were observed.

3:10 PM Break

3:30 PM Student

H6, N-Polar GaN HEMTs Grown by MBE and MOCVD with fmax of 255 and 250 GHz, Respectively: *Dan Denninghoff*¹; *Sansaptak Dasgupta*¹; *Jing Lu*¹; *David Brown*²; *Stacia Keller*¹; *Jim Speck*¹; *Umesh Mishra*¹; ¹University of California Santa Barbara; ²HRL

We report measured fmax data of 255 and 250 GHz on N-polar GaN HEMTs grown by MBE and MOCVD, respectively. To our knowledge, these are the highest fmax values reported to date for N-polar GaN HEMTs. This study illustrates the RF equivalence of two nominally similar device structures with different growth methods. The extremely rapid performance advances of N-polar GaN HEMTs are a significant indication of their relevance and viability in modern electronic device applications. The advantages of HEMTs on N-polar GaN include low contact resistance, a built-in back-barrier for improved electron confinement and modulation efficiency, and ability to scale the barrier thickness independently of 2DEG channel charge. As the predicted performance advantages are being realized, it is important to compare N-polar devices of the same nominal structure and design grown by both MBE and MOCVD. The similarities of the MBE and MOCVD devices in this study include: 10-nm GaN channel with 5-nm high-temperature MOCVD SiN gate dielectric, nominally similar graded AlGaIn backbarriers, 50-nm-thick MBE N+ GaN regrowth for source-drain contacts, 350-nm source-drain regrowth spacing, and similar processing sequence. The device processing sequence is as follows: selective-area N+ GaN regrowth, high-temperature SiN gate dielectric deposition, source-drain contact metallization, mesa isolation, probe pad metallization, and a gate-last T-gate formation approximately centered between source and drain. The differences between the devices include an 80-nm gate length and 25-µm gate width for the MBE sample and a 70-nm gate length and 50-µm gate width for the MOCVD sample. The dc performance data are reported in normalized units for ease of comparison. The sheet resistances for both samples as measured by Lehighton were between 550 and 560 Ohm/square. At $V_{ds} = 5$ V, the extrinsic transconductance values were 327 mS/mm for the MBE sample and 315 mS/mm for the MOCVD sample. A relatively high on-resistance of 2.6 Ohm-mm and 2.1 Ohm-mm resulted in an intrinsic transconductance that was degraded by the corresponding

high source resistance from 541 and 464 mS/mm for the MBE and MOCVD samples, respectively. The RF data of the two devices were measured using an Agilent E8361A PNA, after which the probe pads were de-embedded from the measured data to yield the extrinsic device data. Extrapolating the de-embedded h21 and U measured data at a 20-dB-per-decade decay, the fT/f_{max} was 150/255 GHz for the MBE sample and 130/250 GHz for the MOCVD sample. These peak fmax values were obtained at bias points of $V_{gs} = -1$ V, $V_{ds} = 10$ V for the MBE sample and $V_{gs} = -2.25$ V, $V_{ds} = 9$ V for the MOCVD sample. The important point of the study is that very comparable state-of-the-art RF performance for N-polar devices was observed from both growth methods.

3:50 PM Student

H7, Flattened Transconductance (gm) in a Highly Scaled AlGaIn/GaN HEMT Using a Polarization-Induced 2D/3D Hybridized Channel Design:

*Pil Sung Park*¹; *Digbijoy Nath*¹; *Sriram Krishnamoorthy*¹; *Siddharth Rajan*¹; ¹the Ohio State University

We demonstrate a flat transconductance (gm) while maintaining relatively high gm (~170mS/mm for extrinsic ~ 320mS/mm for intrinsic) and current (~ 1A/mm) with a new graded AlGaIn/GaN high electron mobility transistor (HEMT) structure (t_{cap} = 11nm). The graded structure is constructed with an abrupt junction between high and low Al-composition of AlGaIn layers, and a linearly graded AlGaIn layer forming a 3 dimensional electron gas (3DEG) profile with 5~6 nm of vertical channel depth which enables the transconductance tailoring. A tailored gm and device scaling are essential to have linearly operating devices and very high frequency operation while maintaining efficiency. Although conventional HEMT structures have been successfully scaled down, the modification of its gm-Vgs profile presents significant challenges. Channel doped metal-semiconductor FETs (MESFETs) and polarization-doped FETs (PoLFETs) showed tailored gm-Vgs characteristic, however, they do not lend themselves to device scaling-down with maintaining high carrier density. The new polarization-induced graded AlGaIn/GaN HEMT adopts advantages of both HEMT (high scaling factor) and PoLFET structure (gm tailoring). The graded-channel and conventional HEMTs are discussed. The polarization-induced 3-D channel is formed by adding a linearly graded layer (from GaN(bottom) to Al_{0.15}Ga_{0.85}N(top) over 5nm) into the conventional HEMT structure. The processing technology including the gate-recess process (12nm of the etch depth) for a conventional Ga-polar AlGaIn/GaN HEMTs is used for both devices. The devices fabricated were 150 µm wide, 1.5 µm of the gate length and 4 µm of the source-drain spacing. These devices gave Id,max and peak extrinsic gm of 720 mA/mm and 159 mS/mm, respectively, for the conventional HEMT and 970 mA/mm and 168 mS/mm, respectively, for the graded-channel HEMT. However, the graded-channel HEMT maintains a flat gm value (~155mS/mm) over the wide output current range (0.1~0.9 A/mm) while the gm of conventional HEMT immediately degrades after reaching its peak value. To measure the large signal source resistance (Rs) for extracting the intrinsic gm and the gate-channel bias (Vgc), we introduce a new method fitting the gate-source turn-on bias of transistor (3-terminal) into the one of the gate-source diode (2-terminal). The Rss for the graded-channel and the conventional HEMTs were extracted as 3 Ω-mm and 4.8 Ω-mm, respectively. The intrinsic gms ($g_{mi} = g_m/(1-R_{sgm})$) and the electron velocities are estimated from measured gm, Rs and C-V. The peak gmi and electron velocity values are found 675 mS/mm and 1.1×10^7 cm/s, respectively, for the conventional HEMT, and 321 mS/mm and 0.55×10^7 cm/s, respectively, for the graded-channel HEMT. The flattened gmi and electron velocity profile are also found in the graded-channel HEMT. However, the small signal source resistance (rs) is under-estimated due to a relatively long Lg that limits the electron velocity and gmi for the graded-channel.

4:10 PM

H8, Fabrication of AlGaInN/GaN Transistors with f_t and f_{max} Exceeding 100 GHz: Taek Lim¹; Patrick Waltereit¹; Rolf Aidam¹; Rüdiger Quay¹; Lutz Kirste¹; Peter Brückner¹; Rudolf Kiefer¹; Oliver Ambacher¹; ¹Fraunhofer IAF

High-electron-mobility-transistors based on GaN can provide the highest power density among all contemporary semiconductor power-amplifying devices for microwave frequencies. Up to now, such devices have mostly been manufactured using AlGaInN/GaN heterostructures which suffer from the inherent tensile stress in the AlGaIn barrier and corresponding relaxation effects for high Al-content required for high-frequency operation. As an alternative material, we present quaternary AlGaInN at compositions nearly lattice-matched to GaN but with high spontaneous polarization difference with respect to GaN giving high sheet electron densities around $1.9E13\text{cm}^{-2}$. Compared to the often used AlInN system, these materials have a better miscibility and thus offer larger growth windows. For epitaxial growth, molecular-beam-epitaxy in a Veeco GEN20A system with a nitrogen plasma source has been performed. Using 4H-SiC substrates, an AlN nucleation layer, a thick GaN buffer including the channel, an AlN/GaN/AlN spacer, and a thin (around 5nm) Al_{0.40}Ga_{0.53}In_{0.07}N-barrier have been grown. The quaternary alloy composition has been provided by X-ray diffraction analyses on an AlGaInN layer and an auxiliary AlGaIn layer with the same Al/Ga-ratio. The surface of the samples is smooth (roughness around 0.5nm) with atomic steps clearly visible. As an integral part of the transistor structure, the AlN/GaN/AlN spacers have a total thickness of 2.5-3nm and serve to ensure an electronic separation between channel and barrier to improve electron mobility. Heterostructures and devices using the triple-layer structure achieve an electron mobility up to $1590\text{cm}^2/\text{Vs}$, a maximum current density up to 2.3A/mm and peak transconductance up to 675mS/mm clearly outperforming similar structures with an AlN single interlayer. We do not observe a significant current collapse under pulsed conditions indicating a low trap density. Leakage currents and breakdown behavior are addressed as one of the main challenges with the AlGaInN-barrier devices. First, an increase in the growth temperature of the AlGaInN barrier from 580°C to 600°C shows very effective in reducing the leakage currents. Second, the addition of a 2nm GaN cap layer on top of the barrier also results in significantly better breakdown properties. By combining both an increased barrier growth temperature and an additional GaN cap, a three-terminal breakdown voltage of more than 50V for devices with 4750nm source-drain spacing is achieved. Power measurements ($10\text{GHz}, 30\text{V}$) on devices ($L_g=250\text{nm}$) processed with our standard gate technology yield a power-added-efficiency beyond 40%, an output-power-density close to 6W/mm and a linear-gain around 15dB. For these devices we arrive at transit frequencies f_t around 35GHz. Very recently, we have also processed wafers with a 100nm gate length technology with reduced parasitic capacitances, thus enabling to explore the potential of thin barriers and high transconductance for high frequency operation. Devices processed using this technology show an f_t around 110GHz and a maximum frequency of oscillation f_{max} around 130GHz.

4:30 PM Student

H9, Effects of Threading Dislocation Density on the Gate Leakage of AlGaInN/GaN Heterostructures for High Electron Mobility Transistors: Stephen Kaun¹; Man Hoi Wong¹; Sansaptak Dasgupta¹; Soojeong Choi¹; Umesh Mishra¹; James Speck¹; ¹University of California, Santa Barbara

AlGaInN/GaN heterostructures were regrown on semi-insulating GaN templates with varying threading dislocation density (TDD). Regrowths were carried out under Ga-rich conditions by plasma-assisted molecular beam epitaxy (PAMBE) to assess the correlation between threading dislocation density and gate leakage. It has been proposed that Ga-decorated threading dislocation cores in Ga-rich PAMBE-grown GaN may provide conductive channels for vertical leakage [1]. Semi-insulating GaN templates with TDD of (i) $\sim 2 \times 10^{10}$, (ii) $\sim 5 \times 10^8$, and (iii) $\sim 5 \times 10^7 \text{ cm}^{-2}$ were selected, with regrown layers yielding the same TDD as that of the template. Template i was grown by Ga-rich PAMBE on a 4H-SiC substrate. Template ii was grown by MOCVD with Fe-doping on 4H-SiC, and template iii was grown by MOCVD with Fe-doping on a Lumilog free-standing GaN substrate. In order to provide low

leakage buffer layers, C-doping was applied to compensate donor impurities at the regrowth interface. Growth of the GaN:C layer and subsequent GaN buffer were modulated to control Ga droplet accumulation. An AlGaInN/GaN heterostructure was also grown by Ga-rich PAMBE directly on 4H-SiC for comparison with the regrown heterostructures. HRXRD data was used to determine the structural quality of the regrown films, as well as the thickness and Al content of the Al_xGa_{1-x}N cap. The resulting heterostructures were Al_xGa_{1-x}N/GaN with $x=0.25 \pm 0.03$ and Al_xGa_{1-x}N thickness of $28 \pm 1 \text{ nm}$. AFM was used to characterize the surface morphology of the samples (Fig. 1). After etching the AlGaIn layer between the source and drain, spaced $1 \mu\text{m}$ apart, buffer leakage measurements were performed. Drain biases to reach a buffer current of 1 mA/mm were 160-180 V, 55-65 V, 50-60 V, and 20-35 V for the direct growth, regrowth on template i, regrowth on template ii, and regrowth on template iii, respectively. Gate leakage measurements (Fig. 2) were performed on large-area Schottky diodes for all samples. Decreasing TDD from $\sim 2 \times 10^{10}$ to $\sim 5 \times 10^7 \text{ cm}^{-2}$ yielded up to a 45-fold decrease in mean gate leakage at -10 V bias. Passivated recess gate HEMT structures were fabricated and subjected to three-terminal breakdown measurements biased 1 V below pinch-off. To reach 1 mA/mm , drain biases of 15-20 V, 20-25 V, and 30-33 V were applied to the direct growth, regrowth on template i, and regrowth on template ii, respectively. The breakdown voltage of template iii was limited by buffer leakage. An AlGaInN/GaN heterostructure has been regrown on template iii with a lightly C-doped buffer layer to reduce buffer leakage.

4:50 PM Student

H10, Growth and Characterization of npn-GaN/InGaN/GaN Double-Heterojunction Bipolar Transistors on a Free-Standing GaN Substrate: Zachary Lochner¹; Hee Jin Kim¹; Yun Zhang¹; Suk Choi¹; Yi-Che Lee¹; Jae-Hyun Ryou¹; Shyh-Chiang Shen¹; Russell D. Dupuis¹; ¹Georgia Institute of Technology

A common problem with the epitaxial growth of high-quality III-nitride (III-N) thin films is the lack of native substrates. Large lattice mismatches are inevitable when growing on common substrates such as sapphire. Although buffer layer techniques have enabled heteroepitaxy of III-N on foreign materials, the resulting differences in lattice constant and coefficient of thermal expansion still yield significantly high dislocation densities, layer strain, and even cracking in the epitaxial layers. While complex structures can still be grown, and functioning devices can still be fabricated, their full potentials are not realized due to this limitation. Native GaN substrates have recently become available, allowing these limitations to be overcome. Thus, it is now possible to grow layers and epitaxial structures with a lower density of threading dislocations. As a result, improved device performance characteristics are expected and this will especially benefit the electronic devices utilizing diffusion and vertical transport of carriers, such as heterojunction bipolar transistors (HBTs). FS-GaN also has a relatively larger thermal conductivity than sapphire, which is advantageous for epitaxial growth and also useful as a built-in heat-spreader for high-power device applications. In this study, we have grown npn GaN/InGaN/GaN double-HBTs (DHBTs) using metalorganic chemical vapor deposition on a FS-GaN substrate. The layer structure consists of a 600 nm undoped GaN underlying layer, $1.0 \mu\text{m}$ n+-GaN:Si subcollector, a $0.5 \mu\text{m}$ n-GaN:Si collector, a 30 nm In_xGa_{1-x}N:Si graded collector, a 100 nm p+-In_{0.03}Ga_{0.97}N:Mg base ($p=2.5 \times 10^{18} \text{ cm}^{-3}$), a 30 nm n++-In_xGa_{1-x}N:Si graded emitter, and a 70 nm n++-GaN:Si emitter. A similar structure was grown on a sapphire substrate for comparison purposes, but with the addition of a $2 \mu\text{m}$ GaN buffer layer as is necessary for strained heteroepitaxy. After growth and material characterization, the layers were then fabricated into $20 \times 20 \mu\text{m}^2$ devices. The lower dislocation density afforded by the growth on FS-GaN improved material quality of the epitaxial structure in terms of reduced dislocation density and V-defects and thus the device operation of the HBT. The d.c. gain (β) is close to 90 and maximum differential gain (h_{fe}) is ~ 115 for the DHBTs on FS-GaN, more than double that of the similar device grown on sapphire. The maximum collector current density is also higher on FS-GaN, with 12.5 kA/cm^2 , versus 7.2 kA/cm^2 for the sapphire device. These improvements are attributed to the reduced base recombination current resulting from fewer dislocations which act as carrier trap sites. Via the

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equation $\beta = 2L_n^2/W_B^2$, the minority carrier diffusion length in the base (L_n), is calculated to be 46% higher for the FS-GaN sample. We will report further on the growth of these structures and the characteristics of fabricated DHBTs.

Session I: Thermoelectrics and Thermionics II

Wednesday PM Room: Lobero
June 22, 2011 Location: Univ. of California-Santa Barbara

Session Chairs: Lakshmi Krishna, Michigan Technological University;
Joshua Zide, University of Delaware

1:30 PM

II, A Tubular Thermoelectric Generator with Piled Conical Rings

Structure: Tsutomu Kanno¹; Akihiro Sakai¹; Kouhei Takahashi¹; Atsushi Omote¹; Hideaki Adachi¹; Yuka Yamada¹; ¹Panasonic Corporation

Recent years have witnessed a growing interest in geothermal energy for its huge potential capacity as an energy resource. Although current research activities in thermoelectric technology mainly focus on improving material ZT via nanostructuring and other methods, it is also required to realize practical devices especially suited for geothermal electricity generation. In this work, we developed a tubular thermoelectric generator which itself introduces heated fluid inside and efficiently captures thermal energy without external heat exchangers. The tubular generator is based on transverse thermoelectric effects, by means of which electric junctions can be arranged without impeding heat transfer. In order to operate in a transverse mode, high material anisotropy is needed and can be achieved by pile-structure of two dissimilar materials, namely, $\text{Bi}_{0.5}\text{Sb}_{1.5}\text{Te}_3/\text{Ni}$ and Bi/Cu . Before moving on to a tubular device, we investigated a planar one so as to elucidate basic properties of transverse thermoelectric generation. The planar device was made of 44 Bi/Cu tilted multilayer legs connected electrically in series and the overall dimension was $28 \times 26 \times 2 \text{ mm}^3$. Temperature difference was established by two heat sink blocks, one of which was heated by hot water and the other was cooled by cold water. Open circuit voltage and maximum output power were measured to be 280 mV and 40.3 mW, respectively, when a difference in water temperature was 63 K. After confirming the performance of the planar device, we fabricated a tubular thermoelectric generator, using Ni and $\text{Bi}_{0.5}\text{Sb}_{1.5}\text{Te}_3$. Firstly, conical rings of each material were prepared by melt-casting, and then the rings made of different materials were alternately piled up to form a hollow cylindrical shape. Sn-Bi solder paste was used to make electrical contacts. The length and outer diameter of the tube were approximately 100 mm and 14 mm, respectively. This miniature tube was immersed in water maintained at 20°C, and hot water of 50°C was supplied inside the tube to evaluate thermoelectric performance. Open circuit voltage was approximately 40 mV and generated electricity successfully lighted a white LED by way of a step-up dc converter (LTC3108, Linear Technology Corp.). Since the present tubular device is simple in structure, future works on optimal design and manufacturing will make firm steps forward to practical geothermal generators.

1:50 PM I2, Late News

2:10 PM

I3, Thermoelectric Properties of $\text{ErSb}:\text{In}_x\text{Ga}_{1-x}\text{Sb}$ Thin Films Grown by MBE:

Hong Lu¹; Peter Burke¹; Nathan Hackman¹; John Bowers¹; Arthur Gossard¹; ¹UCSB

Engineering of materials with nanostructures can result in improvement in the thermoelectric figure-of-merit, ZT. We have shown enhanced thermoelectric properties of III-V semiconductors by incorporating nanostructures of rare-earth compounds. In this work, $\text{ErSb}:\text{In}_x\text{Ga}_{1-x}\text{Sb}$ is discussed as an example. Thin films of $\text{ErSb}:\text{In}_x\text{Ga}_{1-x}\text{Sb}$ with different In composition have been grown on semi-insulating GaAs substrates using molecular beam epitaxy (MBE). By carefully dealing with the As-Sb interface, the highest In composition x has been pushed up to 0.73 with a lattice mismatch of 12.8% while good crystalline quality is maintained. The concentration of ErSb in these samples is kept at

0.8% by volume and the formation of ErSb nanoparticles within the $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ matrix has been observed by TEM. All the samples are codoped with beryllium for p-type behavior as is required for thermoelectric power generator modules. Thermoelectric properties, including electrical conductivity (σ), Seebeck coefficient (S) and thermal conductivity (κ) of the $\text{ErSb}:\text{In}_x\text{Ga}_{1-x}\text{Sb}$ samples have been measured from room temperature up to 600K. The electrical conductivity was measured on van der Pauw geometry and the Seebeck coefficient was measured on a Seebeck bar sample for more accuracy. The thermal conductivity was measured using the 3ω method. Surface passivation by $\text{SiN}_x/\text{SiO}_2$ was done to prevent the sample from melting and evaporating. Then lithography was used to define the contact areas followed by metal deposition for good ohmic contacts. Measurements were made under a vacuum of $\sim 1 \times 10^{-4}$ torr. Among the $\text{ErSb}:\text{In}_x\text{Ga}_{1-x}\text{Sb}$ samples with different In compositions, the one with high In composition $x=0.69$ yields the highest $ZT \approx 0.57$ at 530K. Higher thermoelectric power factor ($S^2\sigma$) and ZT are achieved with higher In composition over the whole temperature range. Enhancement of thermoelectric properties by the ErSb nanoparticle incorporation is also shown by comparison of sample $\text{ErSb}:\text{In}_{0.69}\text{Ga}_{0.31}\text{Sb}$ and sample $\text{In}_{0.71}\text{Ga}_{0.29}\text{Sb}$. At 530K, an improvement of 46% in ZT is achieved in this sample by 0.8% ErSb. The electrical contribution from the semi-insulating GaAs substrate starts to show up when the temperature reaches 500K, which prevents us from observing an increasing power factor and ZT. Therefore substrate removal and thin film transfer are important for reliable higher temperature measurements and currently in progress.

2:30 PM Student

I4, Nanoparticle Size Dependence of the Electrical, Thermal, and Optical Properties of Er-Doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$: Peter Burke¹; John Bowers¹; Arthur Gossard¹; ¹University of California, Santa Barbara

The codeposition of Er in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ by molecular beam epitaxy (MBE) has been shown to form nanoparticles $\sim 2\text{-}3 \text{ nm}$ in diameter and decrease thermal conductivity as compared to $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ [1,2]. Er also acts as an n-type donor in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ to increase electrical conductivity as compared to $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ [3]. This is promising for thermoelectric applications, which require material with high electrical conductivity and Seebeck coefficient, and low thermal conductivity. In order to better understand the relation between particle size and thermal conductivity, a series of Er-doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ thin films was grown by MBE at growth temperatures from 430-525°C on semi-insulating Fe-doped (001) InP substrates. The Er beam flux was kept constant for all samples, anticipating an ErAs composition of 0.6% calculated nominally by volume. The electrical properties were determined with Hall effect measurements at room temperature and at 77 K. Carrier density and conductivity decrease with increasing growth temperature while the mobility remains relatively constant. The thermal conductivity and Seebeck coefficient are being measured and compared to theory. Optical absorption measurements were made at room temperature from 3000-800 nm. A peak in the absorption coefficient is identified at $\sim 0.7 \text{ eV}$ for the sample grown at 490°C and at $\sim 0.6 \text{ eV}$ for the sample grown at 525°C. No clear peak is identified for the samples grown at lower temperature. A shift of the band edge to higher energies is consistent with the increase in carrier density for the samples grown at lower temperature, due to Fermi-level band filling [5]. Fabry-Perot fringes are visible with a peak spacing of $\sim 0.1 \text{ eV}$, which corresponds well to the 2 $\mu\text{-thick}$ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ epitaxial layer. The changes in carrier density and optical absorption coefficient are both consistent with a change in the number and dimension of nanoparticles as growth temperature is varied.

2:50 PM Student

I5, Improving Thermoelectric Power Generation Efficiency with Epitaxial TlAs/III-V Nanocomposites: Laura Cassels¹; Ashok Ramu²; Gilles Pernot³; Trevor Buehl²; Peter Burke²; Art Gossard²; Chris Palmstrom²; John Bowers²; Ali Shakouri³; Joshua Zide¹; ¹University of Delaware; ²University of California, Santa Barbara; ³University of California, Santa Cruz

We present the details of the recent growth and characterization of terbium arsenide/III-V semiconductor nanocomposites designed for the improvement of efficiency in thermoelectric power generation. An efficient thermoelectric

generator will exhibit a high thermoelectric figure of merit, $ZT=S^2\sigma T/\kappa$, where S is the Seebeck coefficient, σ is electrical conductivity, T is temperature, and κ is thermal conductivity. Semi-metallic rare earth-group V nanoparticles, particularly ErAs and ErSb, epitaxially-embedded in III-V semiconductors have been proven to increase thermoelectric conversion efficiency by reducing thermal conductivity (through phonon scattering), increasing Seebeck coefficient (through electron filtering or energy-dependent electron scattering) and increasing electrical conductivity (through nanoparticle donation of electrons).^{1,2} In this work, we exploit the expected benefits of TbAs over ErAs and ErSb, while seeking to optimize the rare earth concentration, the semiconductor matrix, and additional doping for the highest efficiency.³ These novel materials are grown by molecular beam epitaxy (MBE), co-depositing Tb during III-V growth, such that TbAs nanoparticles precipitate when the solid-solubility limit of Tb in the matrix is exceeded. We use x-ray diffraction (XRD), Rutherford backscattering spectrometry (RBS), electron microscopy, Hall effect and Seebeck coefficient measurements to determine the structural, electrical, and thermoelectric properties of TbAs within (In) Ga(Al)As matrices. Electrical and thermal transport properties are measured over a wide temperature range to determine the suitability of these materials for thermoelectric power generation. Additionally, the reduction in thermal conductivity by nanoparticle phonon scattering is shown at room temperature and over a wide temperature range, and results from two measurements techniques, time-domain thermoreflectance (TDTR) and the 3ω method, are compared. Preliminary results show that these materials behave comparably to the successful ErAs:III-V systems at room temperature, but appear to perform significantly better at higher temperature. Progress towards optimization of these materials for thermoelectric applications will be presented. Specifically, their viability will be evaluated in terms of thermoelectric power factor ($S^2\sigma$), ZT, and efficiency, and prospects for practical devices will be discussed.

3:10 PM Break

3:30 PM Student

I6, The MOCVD Growth of Erbium Antimonide Nanocomposite Embedded III-V Host Materials and Characterization for Thermoelectrics: *Takehiro Onishi*¹; Tela Favalaro¹; Ali Shakouri¹; Elane Coleman²; Gary Tompa²; Nobuhiko Kobayashi¹; ¹UCSC; ²Structured Materials Industries, Inc.

In the growing energy demand and the seeking of the carbon free energy sources, technologies harvesting unused and wasted energy are getting strong attention. Thermoelectrics are one of the more environmentally friendly power sources under growing investigation. Thermoelectrics convert heat directly into electric power. Despite the several decades quest to improve thermoelectric materials, the conversion efficiency is still far behind its theoretical limit, which has limited broad implementation of thermoelectrics. However, recent advances using properties associated with the nanoscale have shown great promise in advancing thermoelectrics to their theoretical limits. Nanostructures are one of the promising technologies of new material development and tuning enabling the drastic enhancement of electrical, optical, and thermal properties of the energy conversion materials. In particular, we focus on nanocomposites embedded in host materials having significantly different physical properties and dimensions. In this research, we demonstrate co-deposition of erbium monoantimonide (ErSb) nanoparticles or nanocolumns in bulk group III-V ($\text{In}_{1-x}\text{Ga}_x\text{Sb}$ and $\text{InAs}_y\text{Sb}_{1-y}$) ternary alloys with dopant (Zn) for the carrier tuning. The nano scale composites work to maintain electrical properties and optimize heat transport properties of the host materials working as the efficient mid to long-wavelength phonon scattering source along with randomly replaced groups III or V atoms in the host material crystals and the filter of low energy carriers. The net result appears in lower thermal conductivity than that of the alloy-limit and fairly identical level of Seebeck coefficient and electrical conductivity implying the enhancement of the dimensionless figure of merit ZT. Taking advantage of low-pressure Metal Organic Chemical Vapor Deposition (MOCVD), we have developed the growth recipe of erbium antimonide (ErSb) nanocomposites embedded in the zinc (Zn) doped indium gallium (arsenic) antimonide (InGa(As)Sb) host materials. The size of ErSb nanocomposites, carrier density and alloy composition of the host materials are tuned by the

control of the growth temperature; flow rate and duration time of component material precursors supply. The structural analyses focusing on surface morphology, crystallographic properties, chemical composition of the Zn doped InGa(As)Sb host materials, and growth features of ErSb nanocomposites. Techniques such as Scanning Electron Microscopy (SEM), Fourier Transform Infra-Red-absorption (FTIR), Atomic Force Microscopy (AFM), X-Ray Diffraction (XRD), and Transmission Electron Microscopy (TEM) were used to obtain information on the co-deposited ErSb nanocomposites and InGa(As)Sb:Zn film on n-type InSb (100) substrate separated with unintentionally doped (UID) InSb buffer layer. Combined with the temperature dependency of Seebeck coefficient and electrical conductivity of InSb host material on InSb substrate by MOCVD, thermal conductivity of ErSb:InGa(As)Sb:Zn, the quality of MOCVD-grown ErSb-InGa(As)Sb is comparable to that of MBE grown films. That suggests the ZT enhanced nanocomposites embedded thermoelectrics materials will be possible to produce in the large scale and at high growth rate by MOCVD.

3:50 PM Student

I7, Cross-Plane Transport Properties of p-Type $\text{La}_{0.67}\text{Sr}_{0.33}\text{MnO}_3/\text{LaMnO}_3$ Perovskite Oxide Metal/Semiconductor Superlattices: *Pankaj Jha*¹; Timothy D. Sands²; Laura Cassels³; Tela Favalaro⁴; Benjamin Kirk⁵; Philip Jackson⁴; Polina Burmistrova¹; Xianfan Xu⁵; Joshua Zide³; Ali Shakouri⁴; ¹Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University; ²ECE, MSE and Birck Nanotechnology Center, Purdue University; ³Material Science and Engineering, University of Delaware; ⁴Electrical Engineering, University of California, Santa Cruz; ⁵Mechanical Engineering and Birck Nanotechnology Center, Purdue University

Metal/semiconductor superlattices with cross-plane transport offer a novel approach towards improving the thermoelectric figure of merit (ZT). Lanthanum strontium manganate ($\text{La}_{0.67}\text{Sr}_{0.33}\text{MnO}_3$, i.e., LSMO)/lanthanum manganate (LaMnO_3 , i.e., LMO) perovskite oxide metal/semiconductor superlattices were investigated as a potential novel p-type thermoelectric generator element. Growth optimizations were performed using pulsed laser deposition to achieve epitaxial superlattices of LSMO (metal)/LMO (p-type semiconductor) on strontium titanate (STO) substrates. In-plane Seebeck results validated the p-type semiconducting and metallic behavior in LMO and LSMO thin films, respectively. Thermal conductivity measurements via the photo-acoustic (PA) technique showed that LSMO/LMO superlattices exhibit a room temperature cross-plane thermal conductivity (0.89 W/m·K) that is lower than individual thin films of either LSMO (1.60 W/m·K) or LMO (1.29 W/m·K). The lower thermal conductivity of LSMO/LMO superlattices may help overcome one of the limitations of oxides as thermoelectrics. In addition to a low cross-plane thermal conductivity, a high ZT requires a high power factor ($S^2\sigma$). Cross-plane electrical transport measurements were carried out on cylindrical pillars etched in LSMO/LMO superlattices via reactive ion etching (ICP-RIE). Cross-plane electrical resistivity results suggest a shift of the magnetic transition temperature from ~250K to ~330K. Considering the novel combination of LSMO/LMO heterostructures for thermoelectric, it is evident that there is much more to understand about the cross-plane transport. A magnetic transition peak around room temperature may be promising for low-magnetic field magnetoresistance devices, sensors and magnetic data storage applications.

4:10 PM

I8, Temperature-Dependent Thermal Properties of HgCdTe Superlattices: *Kejia Zhang*¹; Abhishek Yadav¹; Lei Shao¹; Ramana Bommena²; Jun Zhao²; Silviu Velicu²; Kevin Pipe¹; ¹University of Michigan; ²EPIC Technologies, Inc.

HgCdTe has demonstrated high performance for mid- to long-wavelength infrared detection applications; in particular, HgCdTe-based superlattices have shown promise as a means to tune the cutoff wavelength by adjusting the constituent layer thicknesses. Furthermore, because of its high electrical mobility and low thermal conductivity, HgCdTe has potential as a high-efficiency thermoelectric material. Optimizing the thermoelectric properties of HgCdTe superlattices could lead not only to thermoelectric modules with high thermoelectric figure-of-merit but also to microscale thermoelectric coolers

that are monolithically integrated with infrared detector pixels for localized cooling. Because of the reductions in thermal conductivity known to occur in superlattices due to increased phonon scattering, measurements of the thermal properties of HgCdTe SLs are important both for the thermal management of infrared detectors as well as the improvement of the material's thermoelectric figure-of-merit. As with other materials for infrared detection, HgCdTe is most commonly used at low temperatures to increase signal-to-noise. In this work we present measurements of the thermal properties of MBE-grown Hg_{0.8}Cd_{0.2}Te/Hg_{0.2}Cd_{0.8}Te (200Å/400Å) superlattices over a range of temperature (80K – 295K). In particular, we show measurements of the cross-plane thermal conductivity obtained using a differential 3 ω method on samples with SL thicknesses of 600nm to 2.4 μ m. These measurements confirm a superlattice thermal conductivity that is significantly lower than the bulk values of either binary (HgTe or CdTe) or the ternary (Hg_{1-x}Cd_xTe). A 3 ω heater wire was first lithographically defined on each sample; samples were then mounted on the cold finger of a cryostat using a removable copper block. The contact pads of the heater wire were wirebonded to external beryllium oxide chips with separate heatsinks; the beryllium oxide chips were in turn connected to a 10-pin vacuum feedthrough using copper wires. A copper cylinder was used as a radiation shield to remove parasitic temperature gradients caused by radiative heat transfer between the cold finger and surroundings. The electronic measurement setup included a harmonic oscillator used to drive a bidirectional current source; the bidirectional current source consisted of a Howland current pump circuit and buffer amplifier to increase the current output. The current through the heating wire was determined by connecting a precision heat sink resistor in series with the wire and measuring the I ω voltage drop across it using a lock-in amplifier. The temperature coefficient of resistance was determined by slowly heating the wire from 80K to 295K and measuring the resistance of the wire using a four-probe method while simultaneously measuring the sample temperature. The 3 ω voltage (from which thermal conductivity was derived) was measured using a lock-in amplifier.

4:30 PM Student

I9, Development of III-Nitride Materials for Thermoelectric Applications: *Alexander Szein*¹; John Haberstroh¹; Hiroaki Ohta¹; Steven Denbaars¹; John Bowers¹; Shuji Nakamura¹; ¹UCSB

The development of novel strategies for improving the efficiency of thermoelectric materials, along with an increasing global need for energy efficiency, has created a huge increase in thermoelectric research in the past two decades. At the same time, there has also been a rapid rise of the GaN, InN and AlN material systems due to their suitability for light emitting diodes, laser diodes, and power conversion devices. There remains however, remarkably little known about the thermoelectric properties of these III-Nitride materials. These materials have several important advantages in that they have good temperature stability, a wide bandgap, are non-toxic, and can take advantage of the developing infrastructure and knowledge base that is being driven by optical and power conversion devices. Initial experimental results show that these materials hold promise for high temperature thermoelectric energy generation, as well as integrated on-chip spot cooling applications and warrant significant investigation. The high temperature regime is particularly important because there are many heat sources, such as automobile exhaust, in this temperature range. In this report, current results for n-type GaN and InGaN are presented, with particular attention given to the effects of InGaN doping and composition. The doping of In_{0.08}Ga_{0.92}N material is shown to be an important optimization factor resulting in a peak power factor of 6.3e-4 W/mK² at a doping of 1e19 cm⁻³. In addition, both the Seebeck Coefficient and electrical conductivity are shown to decrease with increasing Indium composition, making this another important optimization parameter, as thermal conductivity decreases with increasing Indium composition. Since the III-Nitride materials are expected to be most competitive in the high temperature regime, it is very important to measure the thermoelectric properties at the elevated temperatures in which they will be operating. To this end, the thermoelectric properties of GaN are measured and shown to improve through a temperature of at least 600 K. Finally, thermal conductivity measurements are currently under way with preliminary measurements of In_{0.14}Ga_{0.86}N showing a decrease in thermal

conductivity from 140 W/mK for GaN to 5 W/mK, which results in an order of magnitude increase in ZT to near 0.05 at room temperature. In addition, a theoretical model based on the Boltzmann Transport Equation and the relaxation time approximation is presented in order to increase understanding and predict the relevant thermoelectric materials properties. This model is shown to have good agreement with experimental results. The rapidly growing industries based on III-Nitride materials, along with their promising thermal stability and emerging thermoelectric properties, make the III-nitride materials an important candidate for high temperature thermoelectric applications.

4:50 PM Student

I10, Highly Ordered Vertical Silicon Nanowire Arrays Embedded in Polymer for Thin-Film Thermoelectric Devices: *Benjamin Curtin*¹; John Bowers¹; ¹Department of Electrical and Computer Engineering, University of California, Santa Barbara

Silicon nanowires have shown promise as a thermoelectric material due to a reported 100-fold reduction in thermal conductivity over bulk silicon while maintaining comparable power factors at room temperature^{1,2}. While these studies focus on individual nanowire properties, large area nanowire arrays fabricated with conventional silicon processing techniques are necessary for thermoelectric micropower generators and on-chip coolers. In this work, interference lithography was used to pattern a two-dimensional, square lattice photoresist template over 2.5cm x 2.5cm areas. Through pattern transfer from the photoresist template to a hard etch mask, a highly ordered vertical array of silicon nanowires was etched into degenerately doped n-type Si using a single-step deep reactive ion etch. The resulting array is 1 μ m tall and the individual nanowires have vertical sidewalls, diameters that are ~80nm, and areal fill factors approaching 20%. Optimization of multiple thin-film layers to achieve high quality photoresist templates with interference lithography is discussed. The silicon nanowire arrays were embedded in PMGI, a polymer with high thermal stability and low thermal and electrical conductivity, to form a dense composite material for both thin-film devices and thermoelectric characterization. We use a self-aligned process to contact the wires by etching back the PMGI with an O₂ plasma to expose the top of the nanowire array and then contacting with Ni/Au. Low contact resistance with ohmic contact behavior was observed with transmission-line (TLM) measurements. Preliminary measurements of the cross-plane Seebeck coefficient using a differential method between samples with different composite thicknesses will be presented. Thermal conductivity of the composite and individual nanowires will also be discussed to show the applicability of using silicon nanowire arrays as a thin-film thermoelectric material.

Session J: Nanowire Transport and Devices

Wednesday PM
June 22, 2011

Room: Lotte Lehman
Location: Univ. of California-Santa Barbara

Session Chairs: David Janes, Purdue University; Raymond Tsui, Raydis LLC

1:30 PM

J1, Molecular Surface Passivation Effects on Indium Oxide Nanowire Transistors: *Seongmin Kim*¹; Patrick Carpenter¹; Rand Jean¹; Sanghyun Ju²; David Janes¹; ¹Purdue University; ²Kyonggi University

In₂O₃ is an attractive candidate for next-generation nano-electronics, because of its chemical stability, wide bandgap, and compatibility with low temperature processes. Recent advances in nanowire based electronics include integration of transparent and/or flexible circuitry, which could enable easy-to-read, lightweight, transparent and flexible electronics. In order to develop In₂O₃ nanowire transistors with suitable performance for commercial nano-electronics, however, it is still necessary to improve and stabilize the transistor characteristics of nanowire devices. We have fabricated In₂O₃ nanowire transistor devices (NWT; gate insulator = 30 nm ALD Al₂O₃) using Al contacts and shown that

passivation of the channel with 1-octadecanethiol (ODT) results in improved subthreshold slope (~ 78 mV/dec). The n-channel NWTs utilized single-crystal In_2O_3 nanowires ($d \sim 20$ nm) and channel lengths of 1.5-2 microns. In order to improve and optimize device performance in terms of on-current, current on-off ratio ($I_{\text{on}}/I_{\text{off}}$), subthreshold slopes (S) and mobility, nanowire source/drain contact regions were polished with O_2 plasma before Al deposition, followed by ozone treatment at the nanowire channel and laser annealing at the contacts after metallization. Following device fabrication, the device wafer was rinsed in ethanol, and then immediately put in a 5mM ODT solution in ethanol for 8 hr at 70°C followed by ethanol rinse. In order to investigate the effects of ODT on In_2O_3 NWTs, the device electrical characteristics were measured before and after ODT treatment. Before passivation, the devices show $S \sim 180$ mV/dec, threshold voltage (V_T) ~ 0.3 V at $V_{\text{ds}} = 0.5$ V. After ODT passivation, the device exhibited $S \sim 78$ mV/dec and $V_T \sim 0.8$ V. Steep $S \sim 78$ mV/dec close to the conventional limit ($S = 60$ mV/dec) is among the lowest value reported to date for metal oxide material based NWTs and is comparable to previous reports on As-doped In_2O_3 nanowire-based TFTs ($S \sim 88$ mV/dec). X-ray photoelectron spectroscopy (XPS) studies of the ODT passivated nanowires indicate that ODT molecules are bound to In_2O_3 nanowires through the thiol linkages and In-S bonds. The low frequency ($1/f$) noise in single In_2O_3 nanowire transistors was investigated before and after ODT passivation. The amplitude of the current noise spectrum (S_i) is found to be proportional to I_d^2 in the transistor operating regime, and the extracted Hooge's constants (α_H) are $\sim 3.65 \times 10^{-2}$ for unpassivated devices and $\sim 8.47 \times 10^{-3}$ for ODT passivated devices. The reduction of α_H after ODT treatment implies that the In-S bonds passivate the surface states on the nanowires, reducing the interface trap densities, resulting in steep subthreshold slope and positive shift in threshold voltage of the NWTs. This study reports that ODT passivation is a promising optimization technology for the realization of fast switching transparent/flexible display circuits.

1:50 PM Student

J2, Electrically Pumped ZnO Nanowire p-n Junction Laser: *Sheng Chu¹, Guoping Wang¹, Jianze Zhao¹, Jieying Kong¹, Lin Li¹, Jingjian Ren¹, Jianlin Liu¹; ¹University of California Riverside*

In this contribution, a laser diode with p-type Sb doped ZnO nanowire and n-type ZnO film was fabricated. The vertically aligned nanowires were synthesized by Chemical Vapor Deposition (CVD) on n-type ZnO film. The ZnO thin film was grown by Molecular Beam Epitaxy. For the nanowires, Sb was used as dopant in the CVD furnace to realize p-type ZnO as well as forming the p-n junction. Nanowire field effect transistors were made and confirmed the p-type conductivity. Indium tin oxide and Au/Ti were used as p-type and n-type contacts, respectively. The Current-Voltage gave good rectifying behavior. Electron Beam Induced Current measurement confirmed the formation of p-n junction between the nanowires and film. The device yielded very strong ultraviolet emission. Multiple spike-like peaks emerged in the electroluminescence spectra when applied current was larger than 50 mA, which came from stimulated emission in the ZnO p-n junction laser. The threshold behavior in the plot of emission intensity versus injected current also confirmed the lasing behavior. Furthermore, the spacing between lasing peaks matched well with the vertical cavity length which consists of the ZnO films and the nanowires. These results suggest that this method for making ZnO nanowire laser is promising for future optoelectronics.

2:10 PM Student

J3, Electrical Transport Study of Schottky Barrier Based ZnO NanoWire FETs: *Ye Shao¹, Jongwon Yoon², Hyeongnam Kim¹, Venkatesh Balasubramanian¹, Takhee Lee², Jae-Hyung Jang², Wu Lu¹; ¹Ohio State University; ²Gwangju Institute of Science and Technology*

Zinc oxide (ZnO) nanowires (NWs) have attracted theoretical and experimental attention as an important material for electronic and optoelectronic device applications. However, due to its complexity, the electrical transport in ZnO NW is often thought to be controversial. Here we present our research on electrical transport in ZnO NW gate all around Schottky-barrier field effect transistors (SBFETs). N-type ZnO NWs are grown by chemical vapor deposition with a doping concentration of $\sim 10^{17}$ cm⁻³. SBFETs are fabricated

on SiO_2/Si substrates where the degenerated Si substrates are used as the back gate. Three different metals including Pt, Al and Ti are deposited as Schottky contacts by e-beam evaporation. The physical spacing between Schottky barrier source/drain electrodes is $3.2\mu\text{m}$. Based on Vd-Ids Characteristics, Pt SBFETs exhibit a higher turn-on voltage and a higher saturation drain bias because the higher work function of Pt is expected to result a higher schottky barrier than Al and Ti SBFETs. Pt SBFETs also exhibit the highest current level at the same drain and gate biases beyond a critical field after the devices are turned on. This suggests that the non-depletion region becomes dominant in electron transport beyond the critical field as Pt SBFETs have a shorter non-depletion region, leading to a higher drain current than Al and Ti SBFETs. Temperature dependent current measurements dependence on gate bias at a drain bias of 0.3V are performed from 210K to 260K for a better understanding of electron transport in these devices. The results show that the gate threshold voltage is strongly dependent on temperature. As the temperature decreases, the threshold voltage shifts toward the negative direction and the drain current decreases, likely due to the Involvement of surface/interface states in electron transport of ZnO NWs. Based on Arrhenius plots, the extracted channel peak activation energies of Pt, Al and Ti SBFETs are 0.448eV at -22.5V, 0.25eV at -11.5V, and 0.37eV at -9.8 V, respectively, all peaking at about the threshold voltages, indicating that Pt Schottky contacts have a higher barrier height for injecting carrier in the NW channel. Overall, we suggest that in the high drain bias regime the non-depletion channel region is dominant for electron transport while the depletion region is critical at the low drain bias regime for electron injection. Current efforts are being focused on the analysis of roles of surface and interface traps on electron transportation in ZnO NW.

2:30 PM Student

J4, ZnO Nanowire-Based Field Effect Transistors with Non-Volatile Memory Function Using Mobile Protons: *Jongwon Yoon¹, Woong-Ki Hong², Minseok Jo¹, Gunho Jo¹, Minhyeok Choe¹, Woojin Park¹, Jung Inn Sohn², Hyunsang Hwang¹, Mark Welland², Takhee Lee¹; ¹Gwangju Institute of Science and Technology; ²Nanoscience Centre*

One-dimensional semiconducting nanowires have attracted significant attention due to their unique properties including highly anisotropic geometry and large surface-to-volume ratio. In particular, the interface of nanowires with large surface-to-volume ratio plays an important role for modification of fundamental electronic properties in nanowire-based field effect transistor (FET) devices. For example, the threshold voltage can be tuned through surface roughness control of ZnO nanowire with various growth substrates and memory function can be created by interface control using self-assembled molecules and ferroelectric dielectric films. In this study, we demonstrated the ZnO nanowire-based transistor memory device by introducing mobile protons, which are generated by hydrogen annealing process under high pressure and at relatively low temperature (400°C , 10 atm), in the SiO_2 film. We observed that reversible hysteresis behavior in transfer characteristics (drain current versus gate voltage) and reproducible ON/OFF switching behavior. These memory characteristics are attributed to manipulation of interface properties, such as effective electric field, surface charge density, and surface barrier potential, through movement of protons with gate electric field, which is consistent with the UV photo-response characteristics of our nanowire memory devices.

2:50 PM

J5, Raman and Electrical Probes of Carrier Concentration in Si-Doped GaN Nanowires Grown by Plasma-Assisted MBE: *Lawrence Robins¹, Norman Sanford¹, John Schlager¹, Kris Bertness¹, Paul Blanchard¹; ¹NIST*

Carrier concentrations in GaN nanowire clusters grown by plasma-assisted MBE on Si(111) wafers were measured by Stokes Raman spectroscopy with 1.96 eV (633 nm) excitation. A simple model of longitudinal optical (LO) phonon - plasmon coupling was used to estimate the carrier concentration from the blue shift of the LO phonon peak in doped relative to undoped samples. The LO phonon peak occurred at 739.5 cm^{-1} in a nominally undoped sample. Carrier concentrations of the doped samples, as determined by the peak shift method, varied from $1 \times 10^{17}\text{ cm}^{-3}$ to $8 \times 10^{17}\text{ cm}^{-3}$. In addition, carrier concentrations and mobilities of single-nanowire electrical devices, fabricated

from the as-grown samples examined by Raman spectroscopy, were estimated from UV-excited photocurrent-voltage measurements. Carrier concentrations obtained from the Raman and UV photocurrent measurements were compared. Strong Raman peaks, comparable in intensity to the LO phonon peak, were observed in the 670 cm^{-1} to 730 cm^{-1} wavenumber range, in the frequency gap between the transverse optical (TO) and LO phonon modes of bulk GaN. The peaks in the 670 cm^{-1} to 730 cm^{-1} range are ascribed to Frohlich modes localized near the surfaces of the nanowires, or interfaces between the nanowires and unintentional surface adsorbates. Spatially resolved Raman measurements were performed along the radial direction of a 76 mm diameter wafer, from the center to the edge of the wafer, and compared with changes in nanowire growth morphology along the radial direction, which were observed by electron microscopy. The intensity ratio of the Frohlich modes to the LO phonon - plasmon mode was observed to increase from the center to the edge of the wafer. In addition, the $E_2(\text{high})$ Raman peak (at 568 cm^{-1}) was observed to broaden and shift to lower wavenumber from the center to the edge, which suggests an increase in tensile stress in the material grown near the edge of the wafer. The tensile stress may arise from GaN material with a faceted, non-nanowire morphology, which was observed to grow between the nanowires.

3:10 PM Break

3:30 PM Student

J6, Electrodeposited InSb Nanowires: Structural Properties and Transistor Performance: *Suprem Das*¹; Collin Delker¹; Dmitri Zakharov¹; Yong Chen¹; Timothy Sands¹; David Janes¹; ¹Purdue University

InSb is a promising candidate for high speed/low power devices due to its low electron effective mass and high mobility at room temperature. Nanowires of this material are of interest for nanoelectronic, nanophotonic, and thermoelectric device applications. The use of nanowires, rather than bulk, can mitigate lattice mismatch problems found in InSb epilayer growth [1]. Nanowire growth using chemical vapor deposition typically employ the vapor-liquid-solid mechanism, which suffers from difficulties in achieving sharp heterointerfaces and potentially from diffusion of gold from the catalyst particle into the sidewalls of the nanowire [2-3]. Electrochemical growth within an appropriate template can overcome these problems. In this work, InSb nanowires of 100nm diameter were grown inside the nanochannels of porous anodic alumina templates using electrodeposition. Post annealed nanowires exhibited a zinc blende crystal structure with lattice constant of 6.478 \AA as confirmed from the x-ray diffraction data. High resolution TEM studies showed the wires to be single crystalline along the entire length of the wire with a [111] growth direction. Transistors were fabricated using individual InSb nanowires as channels. As fabricated devices showed current-voltage characteristics with evidence of significant Schottky barrier effects at the contacts. Following annealing at 300°C in Ar ambient for 10 minutes, the I-V characteristics were more linear at small drain voltages, indicating more transparent contacts, and better current saturation was observed. An $I_{\text{on}}/I_{\text{off}}$ of $40\mu\text{A}$ (with a V_{ds} of 1V) and $I_{\text{on}}/I_{\text{off}}$ 16-20 were obtained from the output characteristics and the transfer characteristics respectively. Room temperature field effect mobility extracted from transconductance was $1200\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$. The transport characteristics were explained on the basis of a velocity saturation model

3:50 PM Student

J7, Electron Transport in One-Dimensional InAs Nanowire Transistors: *Hanshuang Liang*¹; Ganesh Subramanian¹; Hao Wu¹; Hongbin Yu¹; Ping-Show Wang²; Joshua Shapiro²; Diana Huffaker²; ¹Arizona State University; ²University of California at Los Angeles

Semiconductor nanowires are considered to be potential building blocks for small scale electronic and photonic devices applications due to their unique one-dimensional structure. InAs bulk materials have high mobility, which is promising for fabricating high-speed devices. Vertically placed nanowires directly grown on the substrate of interest would enable high-density integration of such devices and new functionalities. It has been shown these vertically aligned nanowires can be grown at desired locations on the nanopatterned surface prepared through lithographic processes. However, detailed electrical characterization of nanowires grown with such technique is

necessary to understand their properties. In this work, we performed electrical measurements on InAs nanowires by placing them horizontally on device templates. InAs nanowires are first grown on semi-insulating InAs (111)B substrates without doping using a catalyst-free technique via selective-area MOCVD growth. The nanowire arrays are designed to have a pitch of 300 nm / 600 nm. Typically, the nanowires are $5\text{ }\mu\text{m}$ - $7\text{ }\mu\text{m}$ in length and have diameters of around 100 nm. InAs nanowire field-effect transistors are fabricated by mechanically transferring them to a silicon substrate covered with a 200 nm thick SiO_2 layer. The four-electrode patterns for contacts are made by electron-beam lithography (EBL) followed by metal deposition (20 nm Cr and 200 nm Au). Prior to metal deposition, however, the substrate is dipped in ammonium hydroxide to remove the native oxide layer formed on the nanowire surface. Currents I_d vs source-drain voltage V_{ds} were measured at room temperature with three different back gate bias. We observe response with different back gate bias, indicating electron as conducting carriers as expected from the undoped InAs, although, shining light on the devices do not alter their I-V characteristics as much. We attribute this insensitivity to light as the effect of the InAs Fermi level pinning in the conduction band thereby making it more metal-like; the proportion of charge carriers created by the excitation of light is not insignificant hence inducing no appreciable change in the current. Due to the same reason, gate bias does not significantly re-distribute the charges within the nanowires, and therefore we observe I_d do not vary strongly with different bias - V_g , in contrast to many other semiconductor nanowires. The gate response measurements are performed at room temperature. From these plots, it can be seen that the current can not be shut-off even for large values of V_g , which is consistent with similar reports from several other reports. The observed data suggest that the on/off ratio of the devices tested is less than 2 orders of magnitude (which is consistent for most of our devices).

4:10 PM

J8, Electrical Properties of Axial and Radial Nanowire pn-Junctions – A Comparison: *Christoph Gutsche*¹; Andrey Lysov¹; Ingo Regolin¹; Werner Prost¹; Franz-Josef Tegude¹; ¹University of Duisburg-Essen

III-V semiconductor nanowires hold the promise to act as key element e.g. in next generation photovoltaic (PV) devices due to their possible higher conversion efficiencies compared to thin film devices combined with the ability to use relatively inexpensive silicon substrate material. Currently, it is under discussion whether axial or radial pn-junctions are more target-aimed. The latter allows an optimal light absorption and an effective light collection but the shell growth is restricted to the similar strain considerations as thin films. In contrast the first enables the creation of multijunction PV with a relative small absorption area. Here we will present and compare the electrical properties of axial and radial nanowire pn-junctions. Both, axial and radial junctions are formed by Au assisted vapour-liquid-solid MOVPE growth on (111)B GaAs substrates. Radial pn-diodes were formed between n-doped GaAs nanowire core ($n \sim 1 \cdot 10^{18}\text{ cm}^{-3}$) with a diameter of 100 nm and 100 nm thick p-doped GaAs shell ($p \sim 3 \cdot 10^{18}\text{ cm}^{-3}$). An additional 30 nm thick nominally undoped InGaP region was inserted into the structure to allow selective wet etching of the outer shell. Details of axial GaAs pn-junction growth can be found elsewhere. The as-grown structures were transferred to special pre-patterned carriers and finally contacted by electron beam lithography and lift-off technique. Ohmic contacts were obtained using Ge/Pd/Au as n-contact system and Pt/Ti/Pt/Au as p-contact system, followed by subsequent rapid thermal annealing for 30 s at 280°C and 360°C , respectively. The growth, basic process scheme, doping profiles, and electronic properties of both diode types will be presented, compared and discussed with respect to possible applications. The unique strength of axial pn-junctions is the ultra-low reverse current giving rise to an on/off ratio of about 10^6 . Radial nanowire diodes exhibit a worse reverse current and higher forward current because of the larger area of the junction region. The lower diffusion voltage of radial pn-junctions as compared with axial structures (0.5 V and 1 V respectively) is also observed in other works and fits to first numerical simulations of other groups. It is attributed to defect states at the contact/semiconductor interface as well as between the nanowire shells. In conclusion, radial as well as axial high current single GaAs nanowire pn-diodes are demonstrated. The comparison shows that there is high potential

for device optimisation in terms of doping profiles, junction abruptness and surface passivation.

4:30 PM Student

J9, GaAs Core-Shell Nanowire-Based Vertical p-n Diodes: *Hao Wu*¹; Hanshuang Liang¹; Hongbin Yu¹; Joshua Shapiro²; Ping-Show Wong²; Diana Huffaker²; ¹Arizona State University; ²University of California at Los Angeles

As semiconductor technology reaches 22 nm node, current combination of materials and device architectures have met their bottle-necks due to several fundamental limits in physics. Semiconductor nanowires (NWs) have been considered as an attractive alternative for next generation electronics. Among all the nanowires devices, the p-n junction is one of the most fundamental structures and exhibits rectifying current-voltage (I-V) characteristics. In this work, the fabrication and electrical characterization of GaAs nanowire-based vertical p-n diodes are reported. Temperature dependent I-V characteristics are measured, showing a qualitative agreement with the prediction of ideal p-n diode theory. The vertical p-n diode in this work consists of GaAs nanowires with multiple p-n core-shell structures formed *in-situ* during the catalyst-free MOCVD nanowire growth on nanopatterned p+ GaAs (111)B substrates. The doping concentration, calibrated for bulk materials on the GaAs (001) semi-insulating substrate by Hall measurements, is $1.0 \times 10^{18} \text{ cm}^{-3}$ and $1.0 \times 10^{17} \text{ cm}^{-3}$ for the n and p sections, respectively. After growth, a low-k insulating layer of polyimide was spin-coated onto the substrate followed by O₂ reactive-ion etching (RIE) to etch back polyimide, revealing the top 200 nm of the GaAs nanowires. Diluted (NH₄)₂S was used for nanowires surface treatments to remove the native oxide and form good metal-semiconductor contacts. Top electrodes of vertical p-n diodes were first defined by Electron beam lithography (EBL) followed by 20 nm Ti and 250 nm Au of top electrode metal deposition using e-beam evaporation. Electrical characterization was performed by grounding the GaAs substrate back contact and applying the bias to the top contact. The current-voltage (I-V) characteristics of p-n diodes with top electrodes covering different amounts of nanowires ranging from ~2 to ~180 NWs are measured. As more nanowires are covered by electrode, the forward bias current exhibits higher exponential increase and larger reverse saturation current as well. By fitting the experimental I-V curves to the ideal diode behavior, ideality factors ranging from 1 to 4, dependent of the number of NWs, are observed. Ideality factor of nearly 1 is obtained from diodes with ~40 NWs and ~180 NWs while large ideality factor comes from diodes with fewer NWs. This indicates that non-ideal effects are prominent in p-n diodes with fewer NWs. Temperature-dependent I-V curves for GaAs p-n diodes are also characterized. The larger forward and reverse currents at higher temperatures indicate that thermally activated processes are involved in this device.

4:50 PM Student

J10, Role of Defect States in Charge Transport in Semiconductor Nanowires: *Dongkyun Ko*¹; Xianwei Zhao¹; Kongara Reddy¹; Oscar Restrepo¹; Wolfgang Windl¹; Nitin Padture¹; Nandini Trivedi¹; Fengyuan Yang¹; Ezekiel Johnston-Halperin¹; ¹The Ohio State University

Charge transport mechanisms are investigated in Se-doped InP nanowires grown via pulsed laser deposition (PLD). Current-voltage (I-V) curves reveal that transport is limited by trapped space charge at high bias rather than Schottky current in most temperature regimes while at low bias electron mobility calculations indicate that hopping between defect states plays a dominant role. This model is further supported by careful temperature-dependent studies of the low-bias resistance that reveal a transition between hopping mechanisms at a crossover temperature of ~ 158 K. Nearest neighbor hopping (NNH) dominates in the high temperature regime (>158K) where resistance is found to depend on $\exp(T_0/T)^{1.03}$ and Efros-Shklovskii variable range hopping (ES-VRH) dominates in the low temperature regime (<158K) where resistance is found to depend on $\exp(T_{ES}/T)^{0.49}$. For increasing positive gate bias the transition temperature is found to decrease from 158 K to 130 K and the exponent for both high temperature and low temperature regimes deviates from theoretically predicted values (1 and 1/2, respectively). These results highlight the increased importance of defect states in quasi-1D systems and the gate dependence of the crossover temperature, as well as of the related

hopping parameters, suggests that applying a gate bias can tune the strength of electron correlations in these systems.

Session K: Silicon Carbide Growth, Characterization and Devices

Wednesday PM
June 22, 2011

Room: MCC Lounge
Location: Univ. of California-Santa Barbara

Session Chairs: Joshua Caldwell, Naval Research Laboratory; Robert Stahlbush, Naval Research Laboratory

1:30 PM Invited

K1, The Evolution of the SiC Power MOSFET from Lab Demonstration to Commercial Product: *Brett Hull*¹; Jon Zhang¹; Mrinal Das¹; Sei-Hyung Ryu¹; Michael O'Loughlin¹; Al Burk¹; Anant Agarwal¹; John Palmour¹; ¹Cree, Inc.

The potential benefits of SiC as a material for power electronic devices have been recognized for decades. The large bandgap and high thermal conductivity were identified early in the days of Si power device development as the ideal parameters for semiconductor devices meant to handle large currents while blocking high voltages. However, it took much longer for SiC technology to mature to the point at which the fundamental material properties could be exploited. The technology development was a tremendous collaborative effort among a great many individuals from many different institutions, and included such critical topics as single crystal growth for substrates, high quality homoepitaxy, and the refining of wafer fabrication techniques for the specific demands of SiC. All of this collaboration culminated with the successful commercialization of SiC Schottky diodes in the early 2000s. However, it will take the commercial introduction of a functional, MOS-controlled SiC switch for the power electronics community to fully appreciate the promised benefits of SiC power electronic devices. With the recent introduction of the 1200V SiC MOSFET, Cree, Inc. has furthered the SiC power electronics revolution. This presentation will concentrate on the many facets of research successes that were required in order to bring the SiC power MOSFET to market – and will highlight key areas where further advances will greatly benefit future evolutions. The first step in taking the SiC power MOSFET into production was to figure out if it could be made large enough in area to satisfy the needs of the market, and could it be made in large enough volumes at a sufficiently low cost. Device size is limited by defect densities in all facets of production, from micropipes and polytype inclusions in the single crystal substrates, to crystalline defects in epitaxy, to process induced defects during device fabrication. All of these defect reduction efforts were being performed in parallel with efforts to increase wafer size, which has reached 100 mm – large enough to drive the financial viability. Other considerations that are paramount to success are figuring out what performance levels are sufficient for a first generation product. One key component of the SiC MOSFET that many claimed was too large a barrier for successful development of a viable SiC MOSFET was the quality of the oxide. There has been a tremendous research effort over the years to improve the quality of the oxide, and it has reached the point of being of sufficient quality for a first generation MOSFET.

2:10 PM

K2, A Bondable Metallization Stack that Prevents Diffusion of Oxygen and Gold into Monolithically Integrated Circuits Operating above 500 °C: *David Spry*¹; Dorothy Lukco²; ¹NASA Glenn; ²ASRC

In this report we investigate the use of tantalum silicide (TaSi₂-4000Å)/platinum (Pt-2000Å)/iridium (Ir-2000Å)/platinum (Pt-2000Å) as simultaneously being both a bond metal and a diffusion barrier. This bondable metallization that also acts as a diffusion barrier can prevent oxygen from air and gold from the wire-bond from infiltrating silicon carbide (SiC) monolithically integrated circuits operating above 500°C for over 1000 hours in air. This TaSi₂/Pt/Ir/Pt metallization is easily bonded for electrical connection

to off-chip circuitry and does not require extra anneals or masking steps. The TaSi₂/PtIr/Pt metallization can be used directly on ohmic contact metals, dielectric insulating layers, or interconnect metal because it adheres to silicon dioxide (SiO₂), silicon nitride (Si₃N₄), titanium (Ti), and TaSi₂. Previous work of Okojie used Ti as an ohmic contact to n-type SiC with TaSi₂/Pt layers annealed at 600 °C in nitrogen for 30 minutes to form Pt₂Si, which acts as an oxygen and gold diffusion barrier. This works well for probe station tests; however, it leaves Pt₂Si at the surface, which is not easy to wire-bond. A second TaSi₂/Pt layer can then be deposited and not annealed in order to have a bondable surface; however, this adds more processing steps. In this study we investigate the use of the new metallization of TaSi₂/PtIr/Pt on a Ti-SiC contact annealed at 600 °C for 30 minutes in nitrogen, which allows the TaSi₂ layer to react with the first Pt layer to form the Pt₂Si diffusion barrier at the Pt-Ir interface. Since the iridium layer does not readily form a silicide, it prevents the silicon from migrating into the topmost platinum layer during further annealing or high temperature integrated circuit operation. This leaves a pure platinum layer at the surface ideal for gold wire-bonding. We will discuss the characteristics of the TaSi₂/PtIr/Pt metallization at 500 °C after 10, 100, and 1000 hours in air ambient and N₂ ambient. Auger Electron Spectroscopy (AES) depth profiles of the metallization and Field Emission Scanning Electron Microscopy-Focused Ion Beam (FESEM-FIB) cross-sections will be presented. Additionally, straightforward wire bonding and pull tests done under different anneal conditions will be discussed.

2:30 PM

K3, High-Low Temperature Performance of 20 A, 1200 - 1700 V 4H-SiC Power MOSFETs: *Lin Cheng*¹; Anant Agarwal¹; Sarit Dhar¹; Sei-Hyung Ryu¹; Brett Hull¹; John Palmour¹; ¹Cree, Inc.

4H-SiC power MOSFETs have been attracting tremendous attention for high-power applications in a wide range of operating temperatures, owing to their normally-off characteristics, high speed switching operation, avalanche capability, and low on-resistance. To optimize performance of the 4H-SiC MOSFETs for various applications at different temperatures, it is important to understand the mechanisms of temperature-dependence of the key parameters, such as on-resistance and threshold voltage. In this work, we present an investigation on the DC performance of 20 A, 1200 - 1700 V 4H-SiC MOSFETs at cryogenic and high temperatures (-187.4°C to 300°C). Details of the device fabrication can be found elsewhere. Prior to the measurement, the device was packaged in a modified TO-258 metal package with an additional electrical insulation. The device is turned on by applying a positive V_{GS} beyond the threshold voltage, which forms an MOS inversion between the source and the JFET regions. Before the measurement at each temperature, the device was soaked for 5 minutes to allow the temperature to stabilize. The forward DC characteristics of the MOSFET were then studied from -187.4°C to 300°C, including forward conduction and transient behaviors. It is found that the drain current, which was measured at a drain bias of 1 V and under gate bias of 15 V and 20 V, was first increased and then decreased with increasing the temperature from -187.4°C to 300°C. This phenomenon indicates an existence of at least two different trends in two different temperature regimes. We suspect that such a change may be caused by different dominating factors of the MOS channel resistance in the two different temperature regimes. To verify this observation, a 200 μm by 200 μm lateral MOS test device was then measured to extract the MOS channel mobility (μ_{eff}) within the same temperature range. As expected, a similar temperature dependence of the MOS channel mobility was observed. To investigate the transient behavior of the MOSFET, the sub-threshold characteristics were also studied at temperatures from -187.4°C to 300°C. The threshold voltage of the MOSFET monotonically decreases with temperature, while the device remains normally-off throughout the entire range of temperatures at a drain current of 1 μA. More detailed analysis on both 1200 V and 1700 V 4H-SiC MOSFETs, including the variation of the inversion layer mobility and bulk mobility with temperature, will be presented in the full paper.

2:50 PM Student

K4, Improved Microstructure and Ohmic Contact of Nb Electrode on N-Type 4H-SiC: *Kunhwa Jung*¹; Yuji Sutou¹; Junichi Koike¹; ¹Tohoku Univ.

Silicon carbide (SiC) has been considered for an advanced power device material under the conditions of high temperature, high power and high frequency. In order to operate SiC devices, metallic electrodes are necessary. One of the important requirements for the electrode materials is ohmic behavior with a low contact resistivity. A number of different metals have been proposed as the electrode materials for SiC. Nickel electrodes have been widely investigated for n-type 4H-SiC. In spite of the electrical benefits, there are major issues related to the microstructure of Ni on n-SiC; broadening of the metal SiC interface, rough interface morphology with void formation, excess carbon segregation, and rough contact surface. In this research, Niobium was investigated as a new electrode material for SiC devices with an aim to improve these disadvantages of the Ni electrode, especially to prevent carbon precipitation and void formation at the interface by the formation of niobium carbide. Nb film was deposited to the thickness of 100 nm on SiC substrates by RF sputtering. A lift-off process was used to form a transmission-line-method (TLM) pattern. The obtained specimens were annealed at 700, 800, 900, 1000 °C for 10 min under high vacuum condition to form ohmic contact. Microstructure was observed in cross section with a transmission electron microscope (TEM). Reaction phases were examined by X-ray diffraction (XRD). Composition depth profile was investigated by secondary ion mass spectrometry (SIMS). Obtained results showed the formation of niobium carbide and niobium silicide without any voids by solid-state displacement reaction. Furthermore, the formation of Nb carbide prevented carbon precipitation on the electrode surface. As for electric properties, I-V results indicated that rectifying behavior changed to ohmic behavior after annealing at 1000 °C. The specific contact resistance (ρ_c) of this sample was 1.53E-4 Ocm², which was similar to that of Ni electrode (4.27E-4 Ocm²). Finally, wedge wire-bonding was performed with 25μm-diameter gold wires on the Al/Ni or Al/Nb pads having a 1.2μm Al thickness. The wire bonding of the Al/Ni pads showed the success rate of only 10% because of the carbon precipitation on the Ni electrode surface which lead to a poor adhesion at Al/Ni interface. On the contrary, the formation of Nb carbide improved the success rate of wire-bonding up to 90 % due to the prevention of carbon precipitation on the electrode surface. The Nb electrode is a good candidate for reliable and high performance SiC power devices.

3:10 PM Break

3:30 PM

K5, Slow Thermal Emission from Traps in 4H-SiC Epilayers: *Paul Klein*¹; Amitesh Shrivastava²; Tangali Sudarshan²; ¹Naval Research Laboratory; ²University of South Carolina

Advances in 4H-SiC material growth and post-growth processing have led to the realization of epitaxial layers with much lower concentrations of the Z_{1/2} lifetime killer, such that this defect no longer controls the lifetime. Carrier lifetimes have consequently increased, but are still too short for >10kV device applications. Recently, we reported that in low- Z_{1/2} epilayers grown both at USC and at NRL, the carrier lifetime is dominated by surface recombination (SR)¹. In the present work we have observed that, in addition to the primary initial decay dominated by SR, as determined in the previous work, in the USC samples a slow decay component is also observed that exhibits a thermally activated recombination rate. This slow component was observed in all of the USC samples and in none of the NRL samples, suggesting a defect-related origin. This behavior is suggestive of the slow thermal emission of minority carriers from a trapping level. Evidence for the existence of this type of trap in 4H-SiC was reported by Grivickas et al.², and has been treated theoretically by Ichimura³. This has been investigated here through the temperature dependence of the slow component of the carrier lifetime, measured over a wide temperature range using low-injection, time-resolved photoluminescence. The results have been analyzed by a simple carrier dynamics model in which recombination is dominated by SR at relatively short time intervals after excitation, while a fraction of the photo-excited carriers are trapped at the defect. At later times, the free hole population results primarily from thermal emission from

the defect, and the hole lifetime is determined by the slower (i.e. rate-limiting process) of either the SR rate, which removes free holes from the valence band, or the *net* rate of hole emission from the defect, that generates them. Fitting the data with this model accounts well for the observed variations away from Arrhenius behavior at lower temperatures (competing electron capture) and at higher temperature (SR becomes the rate-limiting process). The resulting fitting parameters for the three samples USC1, USC2, and USC3, respectively, were: $E_t = (0.37, 0.58, 0.50)$ eV, $\sigma_n = (7.8, 0.3, 2) \times 10^{-18} \text{cm}^2$ and $\sigma_p = (0.5, 12, 8) \times 10^{-17} \text{cm}^2$. These results can help to identify the defect, as we are considering a trap at $\approx E_v + (0.4-0.6)$ eV with a small capture cross-section for holes ($\leq 10^{-16} \text{cm}^2$). Limiting the search of capacitance transient data to *as-grown layers*, only the “D” and “i” centers fit the criteria. However, other considerations tend to eliminate these two defects as well. Consequently, the defect remains unidentified at present.

3:50 PM Student

K6, Deflection of Threading Dislocations with Burgers Vector $c/c+a$ Observed in 4H-SiC Substrates and Axial Slices with Associated Stacking Faults: *S. Byrappa*¹; F. Wu¹; H. Wang¹; B. Raghothamachari¹; G. Choi¹; S. Sun¹; M. Dudley¹; E.K. Sanchez¹; D. Hansen¹; R. Drachev¹; S.G. Mueller¹; M.J. Laboda¹; ¹Stony Brook University

From its inception SiC has attracted lot of attention due to its superior properties compared to conventional semiconductor materials, but the high defect density and its implications on device performance have precluded it from being used on a large commercial scale. Here Synchrotron White Beam X-ray Topography (SWBXT) studies have been presented of threading dislocations with Burgers vector c and $c+a$, which get deflected onto the basal plane by the overgrowth of a macrostep. These deflected dislocations in turn produce stacking faults with different fault vectors. Three different stacking faults have been observed in SiC to date: Shockley faults, Frank faults and those comprising a combination of these two. First, Shockley faults are known to be caused by the expansion of dissociated Si- and C- core partials, whose existence in SiC has been explained due to its low stacking fault energy. Secondly, Frank faults have been considered to be “in-grown” stacking faults and are thought to result from overgrowth of c -axis screw dislocations. Lastly, a combination of Frank and Shockley faults with fault vectors $1/12\langle 4-403 \rangle$ have been previously observed although no model was presented to explain this phenomena. Dudley et al [1] recently have reported the mechanism for their formation which is due to the deflection of threading dislocations of different Burgers vector onto the basal plane and the simultaneous dragging of the BPD partials pinned at their cores resulting in large stacking faults. These faults arise when dislocations with Burgers vector $c+a$ protrude onto the terrace created by deflection of c -axis screw dislocations, whose surface growth spiral steps are separated into $c/4$, $c/2$ and $3c/4$ step heights and by the simultaneous growth of macrostep at this juncture. The model for deflection of threading dislocations with Burgers vector $n[0001]$ and $1/3\langle 11-23 \rangle$ type along with the formation mechanism of stacking faults with fault vectors $1/12\langle 40-43 \rangle$ will be discussed in greater detail. Topographic evidence will also be provided for the presence of $c+a$ dislocations from slices cut parallel to the growth axis, which was only postulated for many decades but not observed in SiC until recently.

4:10 PM

K7, Stacking Faults Originating from BPDs in High-Doped Buffer Layers: *Nadeemullah Mahadik*¹; Robert Stahlbush¹; Eugene Imhoff¹; Karl Hobart¹; Rachael Myers-Ward¹; Charles Eddy Jr.¹; D Gaskill¹; Fritz Kub¹; ¹Naval Research Laboratory

Stacking faults (SF) originating from basal plane dislocations (BPDs) in 4H-Silicon Carbide (SiC) expand and cause forward voltage drift in minority carrier SiC devices. Reverse bias breakdown voltage degradation with stacking fault expansion has also been observed. The SFs expand under device operating conditions via the electron-hole recombination enhanced dislocation glide process and this expansion leads to device degradation. Previously it was thought that SF expansion could be mitigated in the active drift layer by converting most of the BPDs to threading edge dislocations (TED) within a highly doped buffer layer grown before the active drift layer. Since TEDs do not

form SFs during device operation, their effect on device operation is relatively benign. However, BPD motion and faulting in highly doped epilayers during carrier injection has not been previously studied. In this work using electron-hole creation by UV excitation, we image the motion and faulting of BPDs buried in the buffer layer and show that SFs originating in that layer expand into the device drift region. A 25 μm thick n-type ($3 \times 10^{18} \text{cm}^{-3}$) SiC buffer layer was grown on 4° offcut SiC substrate, followed by a 30 μm thick n-type ($1 \times 10^{15} \text{cm}^{-3}$) drift layer using standard propane and silane chemistry in a commercial chemical vapor deposition reactor. Whole wafer ultraviolet photoluminescence (UVPL) imaging was performed using the 351 nm excitation line of an Ar ion laser. The UVPL images were taken in the emission wavelength range of 600 -1000 nm. BPDs in the higher doped buffer region appeared as dark regions, and were contrasted to the BPDs in the drift layer that appeared as bright lines. The specific regions of the wafer having BPDs in the buffer were imaged at higher magnification to observe their motion in the buffer region. Variable UV illumination power densities ($100-4000 \text{W cm}^{-2}$) were used to effectively change the excess carrier concentration within the buffer layer. Upon high power UV illumination of $\sim 300 \text{W cm}^{-2}$ the buffer buried BPDs faulted to form SFs at the buffer-drift layer interface. These SFs expanded throughout the buffer regions and into the drift layer, which could then result in device failure. Once the BPDs entered the drift layer they extended up to the sample surface at a much faster expansion rate. The BPDs faulting in the buffer region was correlated with the carrier density in the buffer to understand the various effects like carrier lifetime, buffer thickness, etc. These correlations provide an insight on minimizing buffer layer BPD faulting and SF propagation into the drift layer.

4:30 PM Student

K8, Step Controlled Epitaxy on 4° and 1° Off-Cut 4H and 6H-SiC Substrate Using Dichlorosilane: *Sabih Omar*¹; Haizheng Song¹; Iftekhar Chowdhury¹; MVS Chandrashekar¹; Tangali Sudarshan¹; ¹University of South Carolina

We demonstrate homoepitaxial growth on 1° and 4° off-angle 6H and 4H-SiC substrates by chemical vapor deposition (CVD) in a chimney type hot wall CVD reactor. The growth was done over the temperature range of 1450°C ~ 1550°C while the growth pressures used were in the range of 50~100 torr. Dichlorosilane (DCS) was used as a chlorinated precursor instead of silane, the conventional precursor. Specular surfaces with very low densities of morphological defects were obtained. X-ray diffraction (XRD) rocking curve showed narrow peaks with typical FWHM ~9 arcsec, indicating good crystal quality. Effect of temperature and C/Si ratio on surface features was investigated using Nomarski optical imaging and atomic force microscopy (AFM). Fourier Transform Infrared Spectroscopy (FTIR) showed growth rates in the range of 0.5 – 7 $\mu\text{m/hr}$ for the 10 6H-SiC samples and 1-15 $\mu\text{m/hr}$ for the 40 4H-SiC samples. The growth rate was inferred to be limited by desorption of reaction species at high temperatures. Doping of the epitaxial films was achieved by unintentional doping through site competition epitaxy.

4:50 PM Student

K9, Defect Structures of B_{12}As_2 Single Crystalline Epitaxial Layers on Off-Axis (0001) 4H-SiC Substrates: *Yu Zhang*¹; Hui Chen¹; Michael Dudley¹; Yi Zhang²; James Edgar²; Yinyan Gong³; Silvia Bakalova³; Martin Kuball³; Lihua Zhang⁴; Dong Su⁴; Yimei Zhu⁴; ¹Stony Brook University; ²Kansas State University; ³University of Bristol; ⁴Brookhaven National Laboratory

As a member of icosahedra borides, B_{12}As_2 (abbreviated as IBA) has a wide band gap of 3.2eV, possessing many exceptional properties such as high hardness, high melting point, large Seebeck coefficient at high temperatures and extraordinary resistance against radiation damage via “self-healing” mechanism, which make it promising for the fabrication of high temperature thermoelectronics and high-power beta-voltaic cells. A detailed analysis of the microstructure in IBA single crystalline epitaxial layers grown on (0001) 4H-SiC substrates with 7° offcut toward [1-100] direction and with mixed offcut toward [1-100] and [11-20] directions is presented and compared. Synchrotron white beam x-ray topography (SWBXT) revealed that only one orientation of IBA was present in all the epitaxial layers grown along (111) surface normal, which was also confirmed by cross-sectional high resolution

transmission electron microscopy (HRTEM). For IBA epilayers grown on (0001) 4H-SiC substrates with 7° offcut toward [1-100] direction, much higher quality of the films were observed with no intermediate layer between the epilayer and substrate. The slight diregistry between domains which expand and coalesce from nucleation sites can lead to the formation of translational domain boundaries while the in-plane mismatch between substrate and the film (~3.7%) can be accommodated by networks of interfacial dislocations. For IBA epilayers grown on (0001) 4H-SiC substrates with mixed offcut toward [1-100] and [11-20] directions, higher strain level was observed in IBA epilayers with the presence of a disordered transition layer, which is shown to be created by the coalescence of a mosaic of translational variant domains nucleated at the various types of nucleation site available on substrate surface. In this transition layer, competition between the growth of the various domains is mediated in part by the energy of the boundaries created between them as they coalesce. Boundaries between translational variant domains are shown to have unfavorable bonding configurations and hence high energy. These high energy boundaries can be eliminated during mutual overgrowth by the generation of Frank partial dislocations which effectively eliminates the translational variants. The growth mechanism of IBA on off-axis c-plane 4H-SiC are also proposed, which suggests that off-axis c-plane 4H-SiC may be a suitable substrate to grow IBA single crystals.

Session L: Graphene Fabrication and Devices

Wednesday PM Room: MCC Theatre
June 22, 2011 Location: Univ. of California-Santa Barbara

Session Chairs: Debdeep Jena, University of Notre Dame; Avik Ghosh, University of Virginia

1:30 PM Invited

L1, Single-Layer MoS₂ Transistors: Branimir Radisavljevic¹; Aleksandra Radenovic¹; Jacopo Brivio¹; *Andras Kis*¹; ¹EPFL

We have exfoliated single layers 6.5 Angstrom thick from bulk crystals of semiconducting MoS₂, using the micromechanical cleavage technique commonly used for the production of graphene. Our nanolayers are mechanically and chemically stable under ambient conditions. Unlike graphene, single layer MoS₂ is a direct band gap semiconductor with a 1.8eV gap. We have fabricated transistors using conventional electron beam lithography. Our electrical contacts have ohmic behaviour. From our measurements we extract single layer mobility in the 200-800 cm²/Vs range, higher than 2nm thin-film silicon or graphene nanoribbons with 400meV band gap. All our transistors are n-type. By incorporating a thin layer of high-k dielectric HfO₂ and top gate we can control our transistor in a local way and observe room temperature current on/off ratio above 10⁸ and extremely low leakage currents (25 fA/μm). Our results shown that single-layer MoS₂ could be suitable for the fabrication of electronic circuits and could act as an alternative to graphene in applications that require materials with a band gap. Being a thin, transparent semiconducting material, MoS₂ monolayers also present a wealth of new opportunities in areas that include mesoscopic physics, optoelectronics and energy harvesting.

2:10 PM

L2, Role of Optical Phonon in Graphene Nanoribbon Tunnel Transistors: Strategy for Abrupt Switching from Material's Point of View: *Youngki Yoon*¹; Sayeef Salahuddin¹; ¹University of California - Berkeley

Tunnel field-effect transistors (TFETs) have been attracted a lot of interests for low-power applications since it may provide excellent switching characteristics using quantum tunneling phenomena. In contrast to a conventional metal-oxide-semiconductor field-effect transistor (MOSFET) where a modulation of thermal barrier height is dictated by the Boltzmann factor, subthreshold swing (SS) –voltage requirement to change a current by one order of magnitude – can be less than the classical limit of 60 mV/dec at room temperature. In this study,

by using an atomistic quantum transport simulation, we show that optical phonon (OP) significantly limits the steepness of switching characteristics in tunnel transistors. For a modeled device, we have used a strip of graphene – so-called graphene nanoribbon (GNR) for an active material. The electronic transport is calculated by solving the Schrödinger equation using non-equilibrium Green's function (NEGF) formalism. Phonon dispersion relations are plotted using dynamical matrix to obtain optical phonon energy and sound velocity of acoustical phonon, which are used to describe electron-phonon (e-ph) interaction. Scattering self-energy is solved by using self-consistent Born approximation. Notably, our self-consistent simulation has been performed very rigorously to accurately calculate the scattering self-energy since we focus on low current levels in tunnel transistors. Our simulation results show two significant changes with phonon scattering: (i) the minimum leakage current in a TFET can be significantly increased; (ii) therefore, SS can also be affected negatively. In general, for an abrupt switching, a channel length should be long enough so as to avoid a considerable direct source-to-drain tunneling current through the channel. In fact, when the channel length is not too short and the direct source-to-drain current is sufficiently small, a phonon-assisted band-to-band tunneling current limits the minimum leakage current of the device. According to our simulation result, in the presence of phonon scattering, the SS cannot be as small as what is predicted by a simple ballistic picture. We may achieve an abrupt switching characteristic by suppressing phonon-assisted BTBT current. For this, we have performed extensive studies with asymmetric doping and a larger bandgap, but it turns out that those are ineffective in obtaining steeper subthreshold slope. Instead, if we can choose a material that has smaller optical phonon energy and/or weaker e-ph interaction, the SS can be significantly reduced, which is demonstrated by our simulation results. In summary, we have performed an atomistic quantum transport simulation for a graphene nanoribbon tunnel transistor. We found that the minimum leakage current and subthreshold swing are significantly affected by phonon scattering and an abrupt switching as predicted by ballistic transport could not be observed due to the phonon scattering in a graphene nanoribbon.

2:30 PM

L3, Fabrication of Top-Gated Sub-10 nm Epitaxial Graphene Nanoribbon FETs Using Hydrogen Silsesquioxane(HSQ): *W. S. Hwang*¹; K. Tahy¹; J. L. Tedesco²; R. L. Myers-Ward²; P. M. Campbell²; C. R. Eddy Jr.²; D. K. Gaskill²; H. Xing¹; A. C. Seabaugh¹; D. Jena¹; ¹University of Notre Dame; ²U. S. Naval Research Laboratory

Graphene has been investigated as one of the promising candidates to replace current channel materials for FET application due to its high carrier mobility. Creation of a bandgap, by quantum confinement of the carriers in patterned nanometer size graphene ribbons (GNRs) [1-3], continues to be a significant technical challenge. To date, GNRs have been fabricated from exfoliated graphene and operated by back gates, or nanometer scale ribbons were produced by 'explosive' methods that are not controlled and reproducible. Thus, graphene nanoribbons (GNRs) fabricated by lithography and operated by top gates on large-area graphene has not been demonstrated yet. In this work, we report the fabrication of top-gated GNR transistors on epitaxial graphene (graphene on Si-face SiC) substrates, showing, for the first time, the opening of a substantial bandgap (exceeding 0.1 eV at a ribbon width of 13 nm) in epi-graphene based GNRs. Hydrogen silsesquioxane (HSQ), a negative-tone electron-beam resist, was used to form sub-10-nm GNRs. It was found that at higher developer temperature, the resolution of HSQ patterns increases and the fine gratings were obtained. This is attributed to the increase of differential dissolution rate between exposed and unexposed regions at higher developer temperature [4]. In addition, the HSQ line developed at a higher temperature (38 °C) shows a better uniformity. Nano-gratings of 12 nm line width and 10 nm spacing were obtained after optimization of spin coating, soft baking, hard baking, electron beam dose, and development methods. HSQ lines (width ~10 nm) on graphene were fabricated and then the HSQ line patterns were successfully transferred into graphene, leading to GNRs with line width of ~10 nm. The gate stack consists of electron-beam evaporated Au on Al₂O₃ deposited by atomic layer deposition (ALD) on HSQ on graphene on Si-face SiC. HSQ was used in this work not only as a GNR patterning mask but also

as the seeding layer for the ALD deposition of Al₂O₃. The gate dielectric (Al₂O₃/HSQ) was found to have a small hysteresis; thus the chosen gate stack enables an investigation of the GNR transistor characteristics. 2D graphene devices ($W = 20 \mu\text{m}$) transistors using the same gate stack show appreciable gate modulation ($\sim 3\times$). The ID vs. VDS curve of a 13 nm wide GNR shows the opening of bandgap of more than 0.1 eV. At a VGS = -12.5 V, the Fermi level is in the bandgap of the GNR, and in the highly nonlinear I-V region, the conductance gap $2\Delta V_{DS}$ can be interpreted as the bandgap of the GNR. In conclusion, sub-10 nm top-gated GNR transistors were demonstrated for the first time with a bandgap of more than 0.1 eV using HSQ in the gate stack.

2:50 PM Student

L4, Semiconducting Graphene: Prospects and Challenges: *Frank Tseng*¹; Avik Ghosh¹; ¹University of Virginia

Graphene's zero-bandgapped linear dispersion is an embodiment of the Wigner-Von Neumann theorem, which postulates that bands derived from states with the same group theoretical symmetry do not exhibit any anti-crossing. Since the two component dimer pz basis sets creating the graphene bands transform into each other over a 30 degree rotation, opening a band-gap in graphene involves either breaking the sublattice symmetry, or imposing quantization, such as in a nanoribbon geometry that allows a discrete sampling of k-points, ushering ultimately in semiconducting subbands. Using Extended Huckel Theory (EHT), we study band-gap opening in ultra narrow patterned graphene nanoribbons (GNR), as well as bilayer graphene (BLG) with various stacking geometries. Geometry optimization of edge-hydrogenated GNR shows that the lack of metallicity and chirality arise from the chemistry and distortion of armchair edges which break the sublattice symmetry and opens bandgaps for all chiral widths under 50nm. The symmetry breaking is attributed to the dimerized strain along the armchair edge caused by missing third planar carbon atoms that are hydrogenated. Reduced armchair edge bond lengths form partially resonant benzene-like bonds with increase intra-dimer overlap, but reduced inter-dimer overlap. Conversely the lack of edge dimerization in zigzag-GNRs ensures metallicity and preserves the zero crossings at the K-point. The chiral signatures thereby imposed are washed out by atomic edge roughness. Similar symmetry arguments apply for bilayer graphene (BLG). Having benchmarked the bandstructures of both AA' and AB' stacking schemes with EHT, we calculated the bandstructure of various intermediate stacking schemes, some of which produce bandgaps even in the absence of electric fields. The bandgap can further be extended with some interlayer compression. Despite the evolution of the bandstructure with lateral shift of top and bottom layers, the high-energy carrier velocities are still largely consistent with velocity of single layer graphene (SLG). Recent work has showcases the decoupling of rotationally stacked graphene sheets towards SLG[3]. This has important implications in device architecture, as the bottom layers can screen charged impurities while recovering the large mobility of SLG. We investigated the possible angles of stacked rotations, illustrating how the bandstructure evolves. This requires determining the supercell structure, which can be worked out from the numerical diffraction patterns. It is worth emphasizing however that there is a fundamental trade-off between the effective mass (mobility) and the band-gap. Opening a band-gap eliminates the very origin of low mass electrons. While mesoscopic experiments conducted at a fixed sheet charge density do not pick up this trade-off, a device with constant gate overdrive will exhibit a charge mobility that will fundamentally decrease with increase in ON-OFF ratio.

3:10 PM Break

3:30 PM

L5, Influence of Trapped Single Charges in Single Walled Carbon Nanotube Transistor with SiN_x/Al₂O₃ Double Wrapped Layers: *Takafumi Kamimura*¹; Kazuhiko Matsumoto²; ¹National Institute of Advanced Industrial Science and Technology; ²Osaka University

Single walled carbon nanotube (SWNT) has the very high sensitivity for the charges because of the around 1 nm size diameter. We fabricated the SWNT transistor with ultra-short gate electrode and observed influence of the single charges trapped in the gate insulator. The device was fabricated as follows.

The SWNT was grown by the chemical vapor deposition process on the SiO₂ substrate. The bottom side substrate of the SWNT is etched and the SWNT bridges between source and drain electrodes. Then, the SWNT is wrapped around by double-layer of SiN_x of 27 nm over Al₂O₃ of 3 nm using atomic layer deposition process (FlexAL, Oxford inst.). The Top gate electrode of 10 nm width is fabricated on the insulator. The drain current is modulated discretely by the applied top gate voltage. The discrete drain current level is observed more than seven levels. When the round-trip top gate voltage is applied, the drain current shows hysteresis characteristic. The width of the hysteresis characteristic also increases discretely with increasing the applied top gate voltage width. Each discrete increase of the hysteresis characteristic width, which is corresponding to the discrete shift of the threshold voltage, shows almost same value. Therefore, the discrete modulation of the drain current is attributed to the influence of the trapped single charge at the interface of the SiN_x and Al₂O₃ layers. The top gate electrode width is as narrow as 10 nm and influences at very narrow area. In the narrow area, the trap site is not dense. Therefore, the single charge is trapped there one by one with increasing applied top gate voltage. After the constant top gate voltage is applied, the drain current stays constant value, even though the top gate voltage is returned back to 0 V. This is the memory effect by the single charge trap. At least three levels of the discrete drain current levels show the memory effect. In conclusion, we fabricated the SWNT transistor with ultra-short gate electrode of 10 nm. The device shows the multiple level memory effect by the influence of the trapped single charges.

3:50 PM

L6, Deposition and Characterization of AlN Dielectric Films on Graphene: *Mark Fanton*¹; Joshua Robinson¹; David Rearick¹; Michael LaBella¹; Kathleen Trumbull¹; Randal Cavalero¹; Matthew Hollander¹; Zachery Hughes¹; David Snyder¹; ¹Penn State University

Traditional semiconductor field effect structures rely on the use of thin oxide films to isolate the gate electrode from the channel. The use of oxides on carbon-based structures presents some unique challenges considering the high thermodynamic driving force for reaction between carbon and oxygen. In this work AlN was successfully used as a dielectric for fabricating field effect structures on epitaxial graphene on semi-insulating SiC. A process was developed for deposition of 5-10nm thick AlN films on graphene by molecular beam epitaxy (MBE). Films were grown by RF-plasma-assisted MBE at deposition temperatures between 50°C and 350°C. Careful initiation of growth was critical for avoiding damage to the graphene film. Damage due to exposure to the N-plasma as well as metal rich growth initiation was studied via Raman spectroscopy. Al-rich growth conditions resulted in significant increases in the Raman D/G peak ratio. X-ray photoelectron spectroscopy (XPS) indicated that this was due to Al-C chemical bonding, which is thermodynamically favorable in the absence of N. Similarly, the N-plasma power and gas flow rate were found to significantly impact defect generation in the graphene film. The optimum plasma conditions are discussed in terms of the flux of molecular N and charged species. Near simultaneous introduction of the N-plasma and the Al source resulted in little or no damage to the graphene films as characterized by Raman spectroscopy. Prior to deposition of AlN the graphene films exhibited a mobility of 800cm²/V-s, and a sheet carrier density of 8x10¹²cm⁻², as measured by Hall effect. In the worst cases, after deposition of the dielectric the mobility decreased to as low as 350cm²/V-s and the carrier concentration increased to as much as 1.5x10¹³cm⁻². Changes in mobility and carrier concentration will be discussed in terms of structural changes observed by Raman spectroscopy and transmission electron microscopy and changes in chemistry as monitored by x-ray photoelectron spectroscopy. The dielectric properties of the AlN films will be discussed in terms of relative dielectric constant and dielectric loss as a function of frequency up to 1GHz.

4:10 PM Student

L7, Graphene as a Heat-Spreading Layer in Blue LEDs: *Chongmin Lee*¹; Younghun Jung¹; Jihyun Kim¹; ¹Korea University

Graphene with 2-D honeycomb structure is a promising material because of its exceptional properties (high thermal conductivity, high transparency and

fast carrier mobility). Graphene can be obtained by mechanical exfoliation, high temperature annealing of SiC, chemical oxidation-reduction and CVD (Chemical Vapor Deposition) methods. These properties of graphene can be employed for thermal management in high brightness LEDs due to its superior thermal conductivity. We report that graphene which was grown by CVD method can be used for transparent conductive electrode of blue LEDs. After the substrate metal was etched, FLG (few layer graphene) was transferred on silicon dioxide/Si wafer. Graphene on the silicon dioxide/Si wafer was coated with photoresist, followed by Buffered Oxide Etchant wet etching. The FLG with photoresist (PR) were floated on the Langmuir-Blodgett trough. After PR/graphene on the LED substrate was removed by acetone, graphene was successfully deposited on LEDs. The peaks of D, 2D and G were observed by Micro-Raman Spectroscopy after FLG was deposited on the GaN LED. The shape of graphene was shown clearly when the blue LED was on. Heat simulation by using the finite element method confirmed that Graphene is more effective than Indium Tin Oxide (ITO) in thermal management, where ITO can be replaced by graphene as thermal-spreading layer with high conductivity and transparency. In summary, we present that ITO which is commonly used as transparent conductive electrode for LED can be replaced by graphene that is more thermally and electrically conductive. Details of experiments and results will be discussed in the meeting.

4:30 PM

L8, RCA Clean Assisted Transfer of CVD Grown Graphene: Xuelei Liang¹; Brent Sperling¹; Irene Calizo¹; Guangjun Cheng¹; Christina Hacker¹; Qin Zhang¹; Yaw Obeng¹; Kai Yan²; Hailin Peng²; Qiliang Li³; Xiaoxiao Zhu³; Curt Richter¹; ¹National Institute of Standards and Technology; ²College of Chemistry and Molecular Engineering; ³Department of Electrical and Computer Engineering

Graphene, a monolayer of sp²-bonded carbon atoms, is currently the hottest electronic material due to its unique electronic and optoelectronic properties. High quality large area monolayer graphene can be obtained by using a chemical vapor deposition (CVD) growth method on copper. Considering its low cost and high growth efficiency, CVD grown graphene is very promising for large scale electronic devices application as compared to other methods of producing graphene such as mechanical exfoliation and epitaxy on SiC. For electronic device fabrication, the CVD grown graphene has to be transferred to another substrate from the metal surface. Iron nitrate, iron chloride and ammonium persulfate are commonly used copper etchants to remove Cu under graphene. Although these etchants can remove Cu effectively, many small metal particle residues remain which can be seen under optical microscope. They are difficult to clean even with long time etching. These residue particles may contaminate the fabricated graphene devices and degrade their performance. Therefore, a clean graphene transfer process must be developed. In this work, we compared the above three copper etchants and found iron chloride was the best choice considering defects and cracks induced in graphene during copper etching process. After copper etching, an RCA clean was used to remove the metal particle residues. Different concentrations and combinations of SC-1 and SC-2 steps were tried with varying temperature. Clean and repeatable graphene transfer without metal particle residues was obtained under proper conditions. XPS measurements confirmed no Cu residue remains under these optimized RCA clean conditions. Raman measurements show that the graphene quality was not significantly degraded by the RCA clean process.

4:50 PM Student

L9, Electrical Property and Photoconductivity of Highly Dense and Vertically Aligned ZnO Nanowires Using Graphene as Electrodes: Jian Lin¹; Jiebin Zhong¹; Miroslav Penchev¹; Mihri Ozkan¹; Cengiz Ozkan¹; ¹University of California Riverside

One dimensional ZnO nanostructures have been widely explored due to their unique physical properties, which make them potential candidates for applications in solar cell, photodetectors and nanogenerators. Since discovered in 2004, graphene, two-dimensional material with unique electrical and photonic properties, has drawn great attention from researchers all over the world. The idea of combining these 1D nanowires (NWs) and 2D graphene

for the applications would be interesting to be explored. However, despite the remarkable advances made in previous work on single ZnO nanowire transistor, the electrical characteristics and the photoconductivity of highly dense and vertically aligned ZnO NWs over graphene electrodes have not been thoroughly investigated. In this work we report the fabrication of graphene/ZnO NWs/graphene heterostructure, consisting of ZnO NWs vertically synthesized over large-area CVD grown graphene bottom electrode by hydrothermal method, and the other top graphene electrode connected to ZnO NWs. Raman characterization shows that graphene grown on copper foil by controlled CVD process is few layer graphene (around 9 layers). And scanning electron microscopy (SEM) images exhibit that high density vertical ZnO NWs with diameter ranging from 40 nm to 100nm were synthesized over the graphene layers. In addition, we investigated the electrical and photoconductive properties of large-array ZnO NWs using graphene as electrodes. The current-voltage characteristic in dark shows Ohmic electrical contact characteristics for 90% of 20 devices tested (70% with perfect linear I-V characteristics and 20% with non-linear I-V characteristics), with a 10% of devices exhibiting Schottky rectifying behavior. The Ohmic contact or Schottky contact depends on the relative work function of graphene and ZnO NWs. Interestingly, the leakage current between -0.1V and 0.1V exhibits the almost linear characteristics from the measured I-V curve, which indicates that this leakage current comes from Ohmic junction between some of ZnO NWs to graphene. The photoconductive property of graphene/ZnO/graphene devices was also investigated by the UV illumination (365 nm) to evaluate their potential in optoelectronic application. The conductance pronouncedly increases over the entire voltage bias range for devices with both linear and non-linear I-V characteristics upon UV illumination. The observed relatively small photo-current gain (around 3-5 times) results from the graphene high absorption of UV light at wavelength of 365nm proved by the UV spectrum. The continuing decreased conductance upon the UV illumination process on graphene/ZnO/graphene devices can be attributed to due to and photodesorption of gas molecules from top graphene electrode. These results provide an important groundwork for the future applications of graphene/ZnO/graphene in solar cell, field emission devices and photo-detector.

Session M: III-Nitrides: Defects and LEDs

Wednesday PM
June 22, 2011

Room: Santa Barbara Harbor
Location: Univ. of California-Santa Barbara

Session Chairs: Andrew Allerman, Sandia National Laboratories; Russell Dupuis, Georgia Institute of Technology

1:30 PM

M1, A Defect-Based Mechanism for Efficiency Droop in Nitride Light Emitting Diodes: Normand Modine¹; Andrew Armstrong¹; Mary Crawford¹; Weng Chow¹; ¹Sandia National Laboratories

Efficiency droop is a serious concern in InGaN/GaN light emitting diodes (LEDs) in which the radiative efficiency decreases as the current through the device increases. Droop is widely believed to be associated with a non-radiative recombination mechanism that increases with carrier concentration faster than the approximately quadratic dependence of radiative recombination. In modeling nitride LEDs, defect-induced recombination is often assumed to depend linearly on the carrier concentration. However, this is not generally true. Many defects in semiconductors have multiple charge states and therefore multiple defect levels. Any given defect can only be in one of its charge states at a given time, and changes in charge state are associated with the capture or emission of carriers. As the carrier concentration increases, the predominant charge state of the defect can shift, opening up new defect levels for recombination. We will show that such multilevel defects can induce recombination that has a highly non-linear dependence on carrier concentration. Furthermore, using a microscopic InGaN/GaN LED model,

we will show that a multilevel defect with plausible properties (concentration, defect levels, and capture cross-sections) can reproduce the essential features of the experimentally observed droop phenomenon for InGaN/GaN LEDs in the absence of Auger recombination. This work was supported by Sandia's Solid-State Lighting Science Energy Frontier Research Center, sponsored by the Department of Energy Office of Basic Energy Science. Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under Contract DE-AC04-94AL85000.

1:50 PM

M2, Impact of Extended and Point Defects on InGaN LED Efficiency: *Andrew Armstrong*¹; *Tania Henry*¹; *Daniel Koleske*¹; *Mary Crawford*¹; ¹Sandia National Laboratories

Defects produce non-radiative recombination in InGaN/GaN light-emitting diodes (LEDs). Significant incorporation of both extended and point defects is anticipated for InGaN LEDs grown heteroepitaxially on mismatched substrates and with multi-quantum well (MQW) heterolayers grown at disparate and non-optimum temperatures. However, the origin of defects, their dependence on growth parameters and substrate character, and the extent to which they impact EQE are poorly understood. This incomplete understanding arises from the lack of a deep level spectroscopy method applicable to LEDs that is quantitative, sensitive to non-radiative defects, able to interrogate mid-band-gap states, and has sufficient spatial resolution to isolate defects located in the nanoscopic MQW region. Developing such a technique would advance InGaN LED technology, especially in less mature areas such as yellow-green emitters, semi-polar devices and GaN-on-Silicon. We extended deep level optical spectroscopy (DLOS) to 1) quantitatively study and discern among deep level defects in the MQW and n-side regions of InGaN/GaN LEDs and 2) determine the origin of defects and their impact on EQE. To exemplify the utility of DLOS to correlate defects and LED performance, two LED samples were grown simultaneously via metal-organic vapor-phase epitaxy on c-plane GaN-on-sapphire templates with threading dislocation density (TDD) of 7.6 or 28x10⁸ cm⁻². TDD was controlled via template nucleation growth and film coalescence. LEDs consisted of a GaN:Si n-side, 2.4-nm-thick Ga_{0.87}In_{0.13}N well/7.5-nm-thick GaN:Si barrier 5x-MQW stack, 30-nm-thick Al_{0.15}Ga_{0.85}N:Mg electron-block layer and a GaN:Mg p-side. Electroluminescence was significantly improved for the lower TDD LED. To ascertain the specific role of TDD on LED performance, DLOS was performed at room temperature using a broad-band lamp coupled to a monochromator for tunable, sub-band-gap excitation. Deep level energies were determined by measuring the defect optical-cross-section using differential photocapacitance analysis. Defect location was determined by the evolution of DLOS spectra as the bias-controlled depletion region was extended from within the MQW region out to the n-side. Spectral analysis enabled distinction among InGaN- and GaN-related defects. Defect density (Nt) was measured using lighted capacitance-voltage. It was found that Nt increased with TDD for every InGaN- and GaN-related defect. The role of threading dislocations in non-radiative recombination and to facilitate excess point defect incorporation in InGaN LEDs will be discussed. This work was supported by Sandia's Solid-State Lighting Science Energy Frontier Research Center, sponsored by the Department of Energy Office of Science. Sandia National Laboratories is a multi-program laboratory operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under Contract DE-AC04-94AL85000.

2:10 PM Student

M3, Effect of In_xAl_{1-x}N Electron Blocking Layer on Quantum Efficiency in Visible Light-Emitting Diodes Grown by Metalorganic Chemical Vapor Deposition: *Suk Choi*¹; *Mi-Hee Ji*¹; *Jeomoh Kim*¹; *Hee Jin Kim*¹; *Jaehyun Ryou*¹; *P. Douglas Yoder*¹; *Russell Dupuis*¹; *Kewei Sun*²; *Alec Fischer*²; *Fernando Ponce*²; ¹Georgia Institute of Technology; ²Arizona State University

In this study, we have investigated the effect of In_xAl_{1-x}N layers nearly lattice-matched to GaN as active-layer-friendly electron-blocking layers

(EBLs) on the quantum efficiency and efficiency droop at high current densities in visible III-nitride-based light-emitting diodes (LEDs). The lower growth temperature, larger conduction-band offset, and flexibility in lattice-matching and strain engineering offered by InAlN EBLs are expected to enhance the quantum efficiency of visible blue and green LEDs, compared to conventional AlGaIn EBLs, by reducing the thermal budget during the EBL growth, and providing a larger electron confinement effect. However, the wide bandgap of InAlN may act as a large hole blocking barrier in the valence band, resulting in reduced hole injection efficiency. A thinner EBL can reduce the hole barrier height, but this also will lower the electron blocking efficiency. The strain-engineered InAlN EBL with higher indium (In) composition is another technique for enhancing hole injection. Higher In composition will reduce the bandgap of InAlN, thus decreasing height of both electron blocking barrier and hole blocking barrier. However, the compressive strain of the layer will induce piezoelectric field and reduce band bending of InAlN EBL inserted between the p-layer and InGaN/GaN the active region. This helps to maintain the effective height of the electron barrier maintaining under forward bias conditions. The band structure calculation at the zero bias indicates that the height of electron barrier at the multi-quantum-well (MQW) side remains almost unchanged while that of hole barrier at the p-type layer side is greatly reduced with increased In composition and layer strain. Therefore, the effect of various EBL structures on the luminescence performance of LED should be closely examined. All epitaxial layer structures were grown by low-pressure metalorganic chemical deposition on c-plane sapphire substrates. InAlN EBLs with different thicknesses from 5 nm to 20 nm, with different In composition from 19% to 27%, and conventional Al_{0.2}Ga_{0.8}N are inserted between the GaN:Mg p-type layer and the InGaN/GaN MQW active region of a blue LED structure. Electroluminescence (EL) measurements of LEDs were performed using pulse-mode currents with a duty cycle of 10% up to 360 A/cm². In the quantum efficiency comparison, LEDs with a 20 nm In_{0.19}Al_{0.81}N EBL show only an 18% efficiency droop in contrast to the LEDs with an Al_{0.2}Ga_{0.8}N EBL which show a droop of ~32%. LEDs without an EBL which suffer from a high efficiency droop of over 50%. These results indicate that the In_{0.19}Al_{0.81}N EBL is confining electrons within the active region more effectively than an Al_{0.2}Ga_{0.8}N EBL. A detailed comparison and analysis of the EL intensity and quantum efficiency of LEDs including InAlN EBLs with different thickness will be also reported.

2:30 PM Student

M4, Semipolar AlGaIn Buffers for Deep Ultraviolet Diode Lasers: *Roy Chung*¹; *Erin Young*¹; *Dan Haeger*¹; *Steven DenBaars*¹; *James Speck*¹; *Dan Cohen*¹; ¹University of California Santa Barbara

Semipolar substrates offer a number of advantages for UV emitting AlGaInN based laser diodes, including higher gain, an ability to operate with nearly transverse electric (TE) optical modes, and an ability to provide pseudo-substrates with tailorable lattice constants, something unavailable from bulk c-plane AlN substrates. When high aluminum content buffer layers are grown on semipolar bulk GaN substrates, strain relaxation via glide of threading dislocations forestalls cracking, with the MD segments constrained to the heterointerface, allowing subsequent growth of laser quality material. Al_xGa_{1-x}N layers with 0.1 < x < 0.5 have been grown on (20-21) bulk GaN substrate by metal organic chemical vapor deposition (MOCVD). InGaN/GaN multiple quantum wells (MQW) were grown on top of 1.2 μm thick relaxed Al_{0.22}Ga_{0.78}N on (20-21) GaN and directly on GaN. While strained MQW on GaN clearly showed TDs from cathodoluminescence (CL), MQW on relaxed AlGaIn showed dark lines, suggesting the generation of MDs and disappearance of TDs. As the aluminum composition in AlGaIn increased, single Al_{0.4}Ga_{0.6}N layer started showing cracks along c-projection direction at about 300 nm. This could be due to too much strain and gliding of TDs is no longer enough to release the strain for high aluminum content AlGaIn directly grown on GaN. We have also grown AlGaIn on (20-21) GaN, step grading to higher aluminum composition. This allows relaxation of AlGaIn without generation of new TDs, ultimately leading to high quality AlGaIn template for laser diode growth. On-axis reciprocal space mapping of the graded AlGaIn showed tilt at each interface associated with the presence of MDs. This is a

clear indication of the relaxation of each AlGaIn layer. When more than 1 μm thick $\text{Al}_{0.45}\text{Ga}_{0.55}\text{N}$ layer was grown on the graded AlGaIn, the crack healing was also observed. The diode operation of near UV light emitting diodes ($\lambda\sim 385\text{ nm}$) on the relaxed buffer has been shown and is a promising result for device application of relaxed AlGaIn template. In this study, we report on the growth of semipolar AlGaIn with high aluminum content on bulk (20-21) semipolar GaN. Single AlGaIn and step graded AlGaIn layers were grown by MOCVD and characterized by various analytical techniques such as CL and x-ray diffraction to understand the relaxation mechanisms in semipolar AlGaIn layer.

2:50 PM

M5, Low Dislocation Density $\text{Al}_{0.32}\text{Ga}_{0.68}\text{N}$ by Overgrowth of Patterned Templates: *Andrew Allerman*¹; *Mary Crawford*¹; *Stephen Lee*¹; *Karen Cross*¹; *Mary Miller*¹; *Jonathan Wierer*¹; *Blythe Clark*¹; ¹Sandia National Laboratories

Realization of compact, low cost and highly efficient light sources in the deep-UV region would benefit a number of applications. Laser diodes with emission from 250 to 340 nm are a critical element that enables fluorescence-based biological agent detection. Incoherent sources (LEDs) would find applications in air and water purification, and also in fluorescence-based bio-detection. While a number of materials problems limit the performance of current device designs, the reduction of threading dislocations in the starting AlGaIn epilayer has reliably resulted in higher device efficiency, power, and lifetime. In this work, $\text{Al}_{0.32}\text{Ga}_{0.68}\text{N}$ templates were fabricated with a threading dislocation density (ρ) of $1\text{--}2 \times 10^8\text{ cm}^{-2}$ uniformly distributed over large, wafer-size areas. We epitaxially grew $\text{Al}_{0.32}\text{Ga}_{0.68}\text{N}$ over parallel trenches etched into previously prepared $\text{AlGaIn(Si)/AlN/sapphire}$ templates ($\rho = 2\text{--}3 \times 10^9\text{ cm}^{-2}$). Regions of high dislocation density ($\sim 10^9\text{ cm}^{-2}$) over mesas and at the center of trenches [1] were eliminated by optimizing mesa width, period, and etch depth of the trench patterned into the starting AlGaIn template. Unlike previous reports [1], the overgrown AlGaIn layer is doped with Si ($\text{No} \sim 2 \times 10^{17}\text{ cm}^{-3}$), reducing the sheet resistance of front-side contacted devices and allowing for easier fabrication of vertically conducting emitters. Since dislocation densities are spatially uniform across the wafer, laser diodes can be processed without aligning to the underlying pattern and the entire device area of LEDs utilizes low dislocation material. Cathodoluminescence was used to measure the density and spatial distribution of threading dislocations in AlGaIn epilayers grown over patterned AlGaIn/AIn templates. Consistent with the low dislocation density results from cathodoluminescence, photoluminescence from GaN-AlGaIn quantum wells (QWs) is 7x higher when grown on a patterned AlGaIn template compared to QWs grown on an unpatterned AlGaIn template. Similarly, on-wafer electroluminescence under low current injection ($\sim 13\text{ A/cm}^2$) is 12x higher for laser diode structures grown on patterned vs. unpatterned AlGaIn templates. Finally, we have recently extended this approach to higher Al compositions exceeding 0.60, achieving a low 10^8 cm^{-2} dislocation density at compositions suitable for solar-blind photodetectors and LEDs emitting at 280 nm. Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

3:10 PM Break

3:30 PM Student

M6, Enhancement of Hole Transport and Carrier Distribution in InGaIn/GaN Multiple Quantum Wells by Controlling Indium Content of p-Type Layer in Visible Light-Emitting Diodes: *Jeomoh Kim*¹; *Mi-Hee Ji*¹; *Suk Choi*¹; *Jae-Hyun Ryou*¹; *Russell Dupuis*¹; *Kewei Sun*²; *Reid K. Juday*²; *Alec M. Fischer*²; *Fernando A. Ponce*²; ¹Georgia Institute of Technology; ²Arizona State University

The quantum efficiency of III-nitride-based light-emitting diodes (LEDs) rapidly decreases with increasing drive current, commonly referred to as efficiency droop. Several possible mechanisms for the origin of the efficiency droop have been suggested including carrier overflow, Auger recombination, carrier delocalization, and limited hole injection. Achieving a uniform carrier distribution in active region consisting of the multiple-quantum well (MQW)

has been proposed as one of the solution to mitigate the efficiency droop. In order to accomplish the uniform distribution of carriers in the active layer, effective hole transport is considered to be a key factor. The limited hole transport between the MQWs results from the relatively large effective mass of the holes as well as the height, doping, and thickness of QW barriers (QWB). The engineering of effective mass of the hole and QWB design is, however, in many cases, limited by the fact that it is often accompanied by sacrifice of internal quantum efficiency of the MQWs. In this study, we report on the enhanced hole transport effect in the MQW active region by controlling the indium (In) content in the p-type layer of the LED. The Mg-doped p-type GaN or $\text{In}_x\text{Ga}_{1-x}\text{N}$ layer that acts as a hole injection and contact layer is grown in typical LED epitaxial structures. In particular, we introduce the triple-wavelength (TW)-emitting MQW design in order to experimentally verify the improvement of hole transport in the active region. Each InGaIn QW has a different In content so that it emits its own characteristic color. The epitaxial structures of the LEDs were grown on c-plane (0001) sapphire substrates by metalorganic chemical vapor deposition and fabricated into substrate-emitting devices. For the TW-LEDs having p-GaN layers with different p-type doping concentrations, the electroluminescence (EL) showed no difference, suggesting that hole concentration (at least in the range of variation in this experimental set) does not affect the hole transport significantly. In addition, the TW-LED with p-GaN experienced rather severe efficiency droop behavior, which is currently thought to be related to hole injection behavior difference. For the TW-LEDs with different indium mole fraction in the p-type layers, however, the EL showed improved luminescence of the QW far from the p-type layer with increasing indium mole fraction in the p-type layer, which suggests that there is improved hole transport. As the In content in the p-type layer increases, the EL intensity from the first QW closed to n-type layer is increased. In addition, the EL intensities from each QW are more uniformly distributed. We believe that these EL spectrum changes among measured LEDs are strongly related to the enhancement of hole transport effect by increasing In content in the p-type layer and it will be further discussed.

3:50 PM

M7, P-Side-Down, Ga-Polar, Green-Emitting Single Heterostructure LEDs: *Scott Newman*¹; *Jonathan Wright*¹; *Chad Gallinat*¹; *Ryan Enck*¹; *Anand Sampath*¹; *Hongen Shen*¹; *Meredith Reed*¹; *Michael Wraback*¹; ¹US Army Research Laboratory

Currently, there is a great interest in developing wurtzite, InGaIn-based green LEDs and LDs for display and general lighting applications. However, these devices suffer from lower external quantum efficiencies (EQE) and efficiency droop at lower current densities than blue InGaIn-based LEDs [1], possibly due to the polarization fields related to the larger positive polarization charge at the p-(Al)GaIn/n-InGaIn interface in higher Indium composition Ga-polar InGaIn/GaN heterostructures, which leads to larger electron leakage and poorer hole injection, as well as degradation of higher indium composition InGaIn layers and InGaIn/GaN quantum well intermixing associated with the higher temperatures required for the growth of the wider bandgap AlGaIn and GaIn capping layers in conventional p-up Ga polar devices. These problems can be alleviated by reversing the polarization fields and creating a negative polarization charge at the p-(Al)GaIn/n-InGaIn interface by growing a p-side-down LED on the Ga-polar plane. Furthermore, our simulations show that one can design a Ga-polar, p-side-down GaN:Mg/InGaIn:Si single heterostructure (SH) LED that will have a two-dimensional hole gas (2DHG) at the heterojunction. Together with a large conduction band offset, this structure is expected to effectively confine electrons and holes near the heterojunction under operation up to large current densities. We previously used Hydride Vapor Phase Epitaxy (HVPE) to produce p-side-down SH LEDs emitting at 480 nm with only 10% EQE droop at 500 A/cm². [2] In this work, we used Molecular Beam Epitaxy to produce SH LEDs on sapphire and HVPE GaIn templates from TDI (Oxford Instruments) with longer peak emission wavelengths ranging from 530 – 580 nm. At 100 mA, 0.25 mm² LEDs with peak emission wavelengths of 530, 558, and 579 nm had voltages of 13.3, 8.3, and 7.2 V, respectively. These high voltages result primarily from a fabrication process that included a standard RIE dry etch to make contacts to the bottom GaN:Mg layer, for which the

p-contacts were always Schottky. This data is consistent with reports in the literature that dry etching p-GaN produces n-type surface defects [3-5]. To avoid making contacts to etched p-GaN, a SiO₂-masked regrowth process is under development. Pulsed testing with a 1% duty cycle of a 0.10 mm² LED emitting at 550 nm showed minimal efficiency droop up to 90 mA (nominally 90 A/cm²), the maximum current tested. Most of the emission from this device came from the perimeter of the n-InGaN mesa due to current crowding in the p-GaN layer, leading to a much larger current density. These results suggest that development of n-InGaN/p-GaN p-side down Ga-polar LEDs may be a promising approach for extending the emission to longer wavelengths with reduced droop and greater integrity of the InGaN active region without the necessity of a high temperature-grown (Al)GaN capping layer.

4:10 PM

M8, Characterization of Green Semi-Polar (10-11) GaInN/GaN Light Emitting Diodes: *Christoph Stark*¹; Shi You¹; Liang Zhao¹; Theeradetch Detchprohm¹; Christian Wetzel¹; Edward Preble²; Tanya Paskova²; ¹Rensselaer Polytechnic Institute; ²Kyma Technologies, Inc.

The promise of for energy efficient, droop-free, color-stable, high brightness GaN light emitting diodes (LEDs) in the green-yellow spectral region has led to the exploration of epitaxial GaInN/GaN quantum well growth on the non-polar and semi-polar planes of GaN. Such structures avoid or at least reduce the large internal electric fields typical for polar c-plane-grown structures. These fields cause a strong variation of emission wavelength and most likely play a major role in the efficiency droop at high current densities. After achieving green LEDs on non-polar a- and m-planes we here explore the potential of semi-polar (10-11) plane for the same application. This plane frequently occurs as a highly stable facet in the growth of nanopillars. The residual electric fields are expected to promote longer emission wavelengths and to reduce optical re-absorption. GaInN/GaN multiple quantum well structures were grown in metal organic vapor phase epitaxy on the (10-11) prepared plane of hydride vapor phase c-axis grown bulk GaN. The LEDs structure includes an n-GaN layer, eight QWs, an AlGaN electron-blocking layer, and a p-GaN top contact layer. We reach a peak emission wavelength of up to 527 nm at 43 A/cm², indicative of better Indium incorporation efficiency in the QWs, as compared to similar structures with nonpolar orientation. The film morphology is assessed by AFM, XRD, and TEM. Under variation of the drive current density over the device relevant range of 14 -- 94 A/cm², the peak emission wavelength shows a minimal blue shift of less than 2 nm. The quantum efficiency and degree of optical polarization will be compared with competing structures. The wavelength stability around the desired operating current densities combined with the long emission wavelength makes this semi-polar crystallographic plane a highly promising candidate for the epitaxial growth of high power green LEDs as part of RGB solid state lighting solutions. This work was supported by a DOE/NETL Solid-State Lighting Contract of Directed Research under DE-EE0000627. This work was also supported by the National Science Foundation (NSF) Smart Lighting Engineering Research Center (# EEC-0812056).

4:30 PM

M9, Optical Properties of Molecular Beam Epitaxy Grown High in Content (~20%) InGaN Film Emitting in Green (540 nm): *Vladimir Protasenko*¹; Jai Verma¹; Guowang Li¹; Huili (Grace) Xing¹; Debdeep Jena¹; ¹University of Notre Dame

InGaN ternary alloy quantum wells with low In content have been the material of choice for highly efficient diodes and lasers emitting at blue. Incorporation of higher than >10% concentration In leads to high strain, resulting in compositional segregation and generation of structural defects. As a result, such materials exhibit poor optical properties. Recent successful growths of thin InGaN/GaN quantum wells on non-polar and semi-polar GaN substrates have pushed the operational wavelength of LEDs and lasers into the green region of the spectrum. However, the growth of thick InGaN films remain challenging. Such thick high In-content InGaN films are required, for example, for GaN-based multijunction solar cells. In this work, we present the structural and optical properties of thick high In-content InGaN films emitting in the green (540 nm) grown by MBE. The growths were performed

in a Veeco Gen 930 MBE system with a plasma source for active nitrogen, on semi-insulating Ga-polar (0001) GaN-on-sapphire templates. Approximately 200 nm thick InGaN films were grown on the template at 520C and 450 W RF power with $\sim 1.2e-7(6.0e-8)$ Torr In(Ga) fluxes. Atomic force microscopy revealed an rms roughness of ~ 2.4 nm over $2 \times 2 \mu m^2$ scans, a relatively smooth surface for the high In content InGaN. Complementary X-Ray diffraction and photoluminescence measurements yielded $\sim 21\%$ In content in the InGaN layer. The optical properties of the InGaN layers were investigated by complementary photoluminescence (PL), photocurrent action spectra, UV-VIS absorption, and lifetime experiments conducted in 4-300K temperature range and under various excitation powers. Photoluminescence and photocurrent spectra were measured using excitation from a 488 nm laser, which selectively excites just the InGaN layer, and not the underlying GaN substrate. UV-Vis absorption spectra yielded a clear band-edge slightly blue-shifted to the PL peak emission at 540 nm at room temperature, confirming the high In content in the InGaN layer. For photovoltaic applications, a high conversion efficiency of absorbed photons to free carriers is desired, combined with large carrier lifetimes. To that end, time-resolved PL (TRPL) at various temperatures were used to evaluate the carrier lifetimes and were found to be ~ 0.8 ns. The PL peak at 540 nm saturates at temperatures below 20 K. In addition, finite photocurrent was measured at 4K, indicating that the emission quantum yield cannot be 100% at that temperature. This is especially relevant because much of emission efficiencies reported assume a 100% QY at 4K. This work presents the successful growth of high In-content InGaN by MBE, and measured photocurrent lifetimes.

4:50 PM Student

M10, Effects of Dislocations on Luminescence in m-Plane InGaN Quantum Wells: *Yu Huang*¹; Kewei Sun¹; Alec Fischer¹; Qiyuan Wei¹; Reid Juday¹; Fernando Ponce¹; R. Kato²; Toshiya Yokogawa²; ¹Arizona State University; ²Panasonic Corporation

Group III nitride semiconductors thin film for light emitting devices are typically grown on c-plane sapphire substrates, and have encountered important materials challenges, notably polarization fields due to the absence of a center of symmetry in the wurtzite crystal structure. In addition, the strain due to lattice mismatch between InGaN and GaN produces strong piezoelectric fields, which cause the spatial separation of electrons and holes in the active region by the quantum-confined Stark effect (QCSE), leading to lower radiative recombination efficiencies. A preferred approach to reduce or nullify the QCSE is to rotate the crystal growth direction so that the net polarization field lies parallel to the interface plane. This can be accomplished by growing nitride materials on a-plane or m-plane substrates. Such non-polar device structures are expected to have no internal fields in the quantum well (QW) region. It has been observed, but not reported, the appearance of two peaks in the luminescence of InGaN QWs grown on the m-plane configuration. The origin of the double-peak emission is not understood. In this talk, we report on a study of the structural and optical properties indicating that *in-plane* piezoelectric fields are introduced by lattice mismatch relaxation that breaks the continuity of the quantum wells, resulting in regions where PE fields produce the red-shifted peak. A correlation has been established between the optical and structural properties of blue light-emitting diode structures with an indium composition of about 15% in the active region grown on free-standing m-plane GaN. An inhomogeneous spatial distribution in the InGaN quantum well emission is observed with two distinct peaks at 428 and 462 nm at room temperature, which are associated with the presence of dislocations originating at the InGaN layers. The difference in peak energy positions is consistent with the presence of *in-plane* piezoelectric fields within the dislocated regions compared to the absence of such fields in the dislocation-free regions. The longer wavelength peak exhibits a continuous blue-shift with increasing injection current, attributed to enhanced screening of the piezoelectric fields. It also exhibits slow recombination rates at low temperatures, attributed to carrier separation by piezoelectric fields along the *in-plane* polar c-direction in the dislocated regions, an effect that is reduced by carrier thermal activation at higher temperatures.

Session N: Next Generation Solar Cell Materials and Devices

Wednesday PM
June 22, 2011

Room: State Street
Location: Univ. of California-Santa Barbara

Session Chairs: Christian Wetzel, Rensselaer Polytechnic Institute; Mark Goorsky, University of California, Los Angeles

1:30 PM

N1, Preparation of the Red Phosphor Nanoparticle Films for the Application to Silicon Solar Cells: *Masakazu Kobayashi*¹; *Ayaka Yagi*¹; *Miwa Inaguma*¹; *Sayako Hamaguchi*¹; ¹Waseda University

Expansion of clean energy generation is a crucial issue all over the world. Silicon solar cells are versatile material system, and these solar cells are widely used. One of the serious problem silicon solar cells own is the spectroscopic response near the ultra violet region. In order to solve the problem, red color transparent ink utilizing nanoparticle phosphors was studied. Since those materials emit red colors through the excitation by the ultraviolet light, formation of those layers on top of Si solar cells would result in the improvement of spectroscopic response in the ultraviolet region. Nanoparticles are recently synthesized by many methods. Most of nanoparticles are formed by build-up methods. One disadvantages of the build-up method is the difficulty in preparing alloy materials since the stoichiometric control become harder by increasing the number of elements in the material. A breakdown method, namely ball milling method, was used to prepare nanoparticles of conventional phosphor materials. Binary alloys as well as ternary alloys including CdSe, ZnS:Mn, BaAl₂S₄:Eu, and SrGa₂S₄:Eu have been successfully prepared by this method. Green color transparent ink has been demonstrated using SrGa₂S₄:Eu nanoparticles [1]. Red color phosphor materials including Ba₂ZnS₃:Mn (BZS) and CaSiAlN:Eu were ball milled in this study and sprayed on the glass substrate. During the processing, nanoparticles were annealed at high temperatures. Both BZS and CaAlSiN:Eu phosphors emit red light peaking at around 640nm. Even after the mechanical milling, the photoluminescence spectrum shapes were unchanged indicating the crystal quality of the host material hasn't been seriously affected by the ball milling. Atomic Force Microscopy (AFM) was used to characterize the surface structures of the nanoparticle sprayed substrate surface. It was revealed that well dispersed nanoparticles were uniformly covering the substrate surface. Judging from the surface image, substantial area was not covered by nanoparticles, which would contribute to the high transparency of the ink (sprayed film). Transparency was studied as a function of the wavelength (400 nm to 800 nm). The degree of transparency was affected by the amount of sprayed ink, but the transmittance all over the visible region could be above 90%. The shorter wavelength region was more sensitive to the amount of the sprayed material than the longer wavelength region. When the Si solar cell was placed under the transparent ink, light of the longer wavelength region would not be absorbed by the ink layer; the performance of the solar cell would not be damaged by the ink layer. Those nanoparticle phosphor films could be used to improve the conversion efficiency of the Si solar cells. This work is supported in part by Waseda University High Tech Research Center Project, Organization for University Research Initiatives, and MEXT KIBANKEISEI.

1:50 PM Student

N2, GaAs Nanopillar Photovoltaics Based on Catalyst-Free Patterned Growth: *Giacomo Mariani*¹; *Ping-Show Wong*¹; *Joshua Shapiro*¹; *Diana Huffaker*¹; ¹University of California, Los Angeles

In this work, we present nanostructured core-shell solar cells based on patterned GaAs nanopillars grown by MOCVD. The patterns are photolithographically defined and center-to-center pitch, hole size and mask arrangement can be precisely pre-determined at nanometric resolution. Our inherently catalyst-free growth mode eliminates any metal (i.e. Au) diffusion into the nanopillars that could hinder the electron-hole pair extraction, paramount in photovoltaics. The lattice-matched growth capability also avoids

threading dislocations that normally act as recombination centers, worsening the leakage current in pn-junction based devices. The study aims at evaluating different contact workfunctions for the transparent top electrode applied to GaAs nanopillar photovoltaic devices. Electronic transport along the photo-junction and carrier extraction can be hugely hindered by a non-purely ohmic contact, resulting in low power conversion efficiencies. Aluminum-doped Zinc Oxide (AZO)₂ and Indium-doped Tin Oxide (ITO) are chosen as front electrodes. Comparisons are made in terms of photocurrent density-voltage (J-V) characteristics (under dark and standard AM 1.5 conditions) and external quantum efficiency (EQE), both standard figures of merit in the photovoltaic field. Devices with ITO as top contact are measured along with devices with AZO as front electrode. The best device with AZO as top contact exhibits an open circuit voltage (VOC) of 0.2V, short circuit current density (JSC) of 6.6 mA/cm² and a fill factor (FF) of 37% whereas the best device with ITO as top electrode showed a VOC=0.39V, JSC=17.8 mA/cm² and a fill factor FF above 34% with a power conversion efficiency of 2.54%, the highest achieved to date in GaAs nanowire photovoltaics. The main figures of merit (J-V characteristics, external quantum efficiencies) are presented in a final comparative study.

2:10 PM Student

N3, Wafer Bonded GaAs-Sapphire for Photovoltaic Applications via Adhesive Bonding: *Nikholas Toledo*¹; *Carl Neufeld*¹; *Michael Scarpulla*²; *Trevor Buehl*²; *Samantha Cruz*²; *Arthur Gossard*²; *Steven Denbaars*²; *James Speck*²; *Umesh Mishra*¹; ¹Department of Electrical and Computer Engineering, University of California, Santa Barbara; ²Materials Department, University of California, Santa Barbara

High-efficiency solar cells have been developed by epitaxially growing multi-junction solar cells. In these devices, the highest bandgap material currently used does not exceed 2.0 eV. Improvements in photovoltaic efficiency can be achieved by incorporating wide bandgap solar cells into these solar cells. III-nitrides have recently been demonstrated as potential photovoltaic device material. The large lattice mismatch between InN and GaN however, makes it difficult to grow good quality high In-composition InGaN films due to InN segregation and V-pit formation thereby limiting the achievable range of bandgap that the III-N material system can currently achieve. To improve the efficiency of current multi-junction solar cells, we propose to combine mature IV and III-V based solar cell technologies which work well at bandgaps ≤ 2.0 eV with III-N based solar cells which have currently been demonstrated to work well above 2.0 eV. Due to the large lattice mismatch, the material layers are combined by adhesive bonding. To demonstrate this concept, ITO-coated sapphire is bonded to a GaAs solar cell using a benzocyclobutene (BCB) interlayer. BCB produces high-quality void-free bonds, has excellent thermal stability and can withstand subsequent processing of the transferred films/structures. Moreover, it is a transparent film that allows for optical coupling between the two materials being bonded. The BCB film is spin-coated on the GaAs and then pre-cured at 100°C for 90 seconds. The ITO-coated sapphire is then stacked on the GaAs. The stacked sample is then thermally-compressed at 250°C for 1 hour. After bonding, the GaAs substrate and AlGaAs etch stop layer are then removed thus exposing the GaAs solar cell epilayers. Standard processing methods are then employed to create the solar cell structure. The resulting bond is strong and relatively void-free. The voids can be avoided by optimizing the pre-curing step. In the bonded solar cell device structure proposed, light is transmitted through the sapphire, ITO and BCB interlayers before reaching the GaAs solar cell. The LIV characteristics of a 500 μ m x 500 μ m bonded device show a $J_{sc} = 14.2$ mA/cm² and a $V_{oc} = 0.875$ V. In principle, an InGaN solar cell can be grown between the sapphire and the ITO layers to form a wide bandgap solar cell that is in tandem and optically coupled to the GaAs solar cell. The ITO layer acts as the contact layer for the InGaN solar cell. Furthermore, the GaAs solar cell can be substituted by non-III-nitride multi-junction solar cells in which case, the InGaN solar cell can potentially improve the overall efficiency of current high-efficiency multi-junction solar cells. In summary, we demonstrated a platform for enabling the stacking of III-nitride and non-III-nitride solar cells via adhesive bonding. Optimization of the design of each subcell may lead to more efficient photovoltaic devices.

2:30 PM

N4, Thin Film III-V Photovoltaics on Flexible Metal Substrates and Defect Mitigation Strategies: *Senthil Sambandam*¹; *Aarthi Sundaram*¹; *Akhil Mehrotra*¹; *Alex Freundlich*¹; *Venkat Selvamani*¹; *University of Houston*

We have recently established a program to develop technology that combines the low-cost advantages of thin film PV with the high efficiencies only achieved with single crystalline photovoltaics. III-V photovoltaics have exhibited efficiencies above 40%, but have found only a limited use because of the high cost of single crystal substrates. At the other end of the spectrum, polycrystalline and amorphous thin film solar cells offer the advantage of low-cost fabrication, but have not yielded high efficiencies. Our program is based on single-crystalline-like thin film photovoltaics on polycrystalline substrates using biaxially-textured templates made by Ion Beam-Assisted Deposition (IBAD). MgO templates made by IBAD on flexible metal substrate have been successfully used for epitaxial growth of germanium films. In spite of a 4.5% lattice mismatch, heteroepitaxial growth of Ge was achieved on CeO₂ that was grown on IBAD MgO template. Refraction index and extinction coefficient values of the Ge films were found to match well with that measured from a reference Ge single crystal. GaAs has been successfully grown epitaxially on Ge on metal substrate by molecular beam epitaxy. RHEED patterns indicate self annihilation of antiphase boundaries and the growth of a single domain GaAs. The GaAs is found to exhibit strong photoluminescence signal and, an existence of a relatively narrow (FWHM~20 meV) band-edge excitons measured in this film indicates a good optoelectronic quality of deposited GaAs. While excellent epitaxial growth has been achieved in GaAs on flexible metal substrates, the defect density of the films as measured by High Resolution X-ray Diffraction and etch pit experiments showed a high value of 5×10^8 per cm². Cross sectional transmission electron microscopy of the multilayer architecture showed concentration of threading dislocations near the germanium-ceria interface. The defect density was found decrease as the Ge films were made thicker. The defects appear to originate from the MgO layer presumably because of large lattice mismatches between the various layers. The defect density in GaAs was reduced by a factor of five by adding a step of in-situ deposition of Ge by MBE on the sputtered Ge prior to GaAs growth. A simple non-intrusive photoresist based lithographic process has been used to define high quality patterns on GaAs coated on flexible substrates in a single mesa etch and metal evaporation/resist lift-off. Patterns resolution of few microns with well-defined grid line of 30 μ m has been realized on flexible templates. Solar cells of GaAs have been fabricated and defects caused by various mechanisms including diffusion of germanium have been observed. Outcomes of various strategies being pursued to mitigate defects in the III-V photovoltaic films on flexible substrates will be discussed in this presentation.

2:50 PM N5, Late News

3:10 PM Break

3:30 PM

N6, Towards >15% Solar Cells on Metal Foils: Heteroepitaxial Crystal Silicon on Alumina: *Charles Teplin*¹; *M. Parans Paranthaman*²; *Thomas Fanning*³; *Kirstin Alberi*¹; *Lee Heatherly*²; *Kyunghoon Kim*²; *Frederick List*²; *Jon Bornstein*³; *Claudia Cantoni*²; *Paul Schroeter*³; *David Young*¹; *Howard Branz*¹; ¹National Renewable Energy Lab; ²ORNL; ³Ampulse

We investigate heteroepitaxial growth of silicon solar cells and silicon-compatible buffer layers, with the goal of producing inexpensive, large-grained crystal silicon solar cells on metal foils. Here, we report two key achievements: 1) epitaxial growth of silicon on buffered, oriented and large-grained metal foils and 2) demonstration of scalable heteroepitaxial silicon photovoltaics on Al₂O₃. Silicon films are grown on cube-textured Ni-3%W (NiW) foils, with (100)-oriented ~50 μ m grains. Epitaxial MgO and γ -Al₂O₃ buffer layers are first grown on the foils using electron-beam evaporation in order to establish a surface chemically compatible with subsequent silicon epitaxy. We then deposit silicon layers using hot-wire chemical vapor deposition (HWCVD) epitaxy, a scalable technique that achieves high growth rates at temperatures low enough to avoid any signs of metal-contamination of the Si layer. X-ray diffraction (XRD), electron backscattered diffraction (EBSD) and transmission

electron microscopy (TEM) confirm that the silicon layer is epitaxial at above 740°C. At lower temperatures, the silicon layer is not epitaxial with the γ -Al₂O₃ buffer. Interestingly, this minimum epitaxy temperature is over 100°C higher than for homoepitaxial growth on (100) silicon surfaces in the identical HWCVD reactor (Teplin, APL 2010). To confirm heteroepitaxial silicon quality, photovoltaic devices were fabricated on single crystals of both (1-102) α -Al₂O₃ (r-plane sapphire) and (100) γ -Al₂O₃. For the devices on sapphire, single crystal sapphire substrates were used. For devices on (100) γ -Al₂O₃, alumina layers were grown on (100) SrTiO₃ substrates using pulsed-laser deposition (PLD). Doped silicon back contact and absorber layers (1-2 microns thick) were grown by HWCVD at 800°C. Amorphous silicon heterojunctions and Sn-doped In₂O₃ layers were subsequently grown to fabricate solar cells. The initial solar cells are promising: we achieve open circuit voltages of 425 mV and 380 mV on the sapphire and γ -Al₂O₃ surfaces, respectively. The currents in these thin devices (8-10 mA/cm²) are small because no light trapping is employed. We believe these are the first heteroepitaxial silicon solar cells. Hydrogen passivation, rapid thermal processing, light trapping and device optimization will improve these devices. Together, the replication of the large biaxially-textured grains in NiW foils into silicon films and the demonstration of heteroepitaxial silicon solar cells indicate the promise of low-cost c-Si solar cells on inexpensive, flexible metal foil.

3:50 PM Student

N7, High External Quantum Efficiency and Fill-Factor InGaN-Based Solar Cells Grown by NH₃-MBE: *Jordan Lang*¹; *Carl Neufeld*¹; *Christophe Humni*¹; *Samantha Cruz*¹; *Elison Matioli*¹; *Umesh Mishra*¹; *James Speck*¹; ¹University of California, Santa Barbara

The tunable bandgap and predicted radiation resistance of the III-Nitride materials system is promising for integration into high-efficiency photovoltaic systems. The recent success of MOCVD-grown GaN/InGaN bulk and multi-quantum-well (MQW) solar cells have demonstrated that high-quality devices are achievable by this relatively mature and widely-used Nitride growth technique. While high alloy composition InGaN has been demonstrated by nitrogen plasma-assisted MBE (PAMBE), current-leakage problems have plagued vertical device structures, presumably because of group-III atom decorated threading dislocations. In contrast, record high ideality and low leakage vertical diodes have been demonstrated by NH₃-MBE growth. By combining the benefits of high vacuum, wide temperature window, and N-rich growth environment of this technique, NH₃-MBE will help provide valuable contributions to the development of III-Nitride photovoltaic technology. Here, we present a demonstration of high quality InGaN-based solar cell devices, which achieve performance parity with MOCVD results. GaN/InGaN/GaN P-i-N double-heterostructure solar cells were grown with 90 nm of In_{0.11}Ga_{0.89}N thickness and 50, 100, and 150 nm of p-GaN top-contact window layer thicknesses. Standard effusion cell sources were used for the group-III sources and dopants, while 0.2-0.5 SLM of NH₃ was used to provide the group-V. InGaN growth was performed at a calibrated optical pyrometer temperature of ~615°C. Testing under 1-Sun AM0 broadband illumination of 0.5 mm x 0.5 mm mesa devices demonstrates excellent properties with a V_{oc} of 1.75V, J_{sc} of 1.11 mA/cm² and Fill-Factor of 73% for the 100 nm p-thickness sample. The comparison of different p-GaN thicknesses show drastically increased short wavelength spectral EQE (external quantum efficiency) for reduced p-GaN thickness, without significantly affecting the high peak EQE of greater than 55%. Because of the very high absorption coefficient (~10⁵ cm⁻¹) of GaN, it is likely that the majority of the photons with $\lambda < 365$ nm are absorbed in this p-layer and that the primary minority carrier loss mechanism responsible for low EQE in this spectral range is bulk recombination. Additionally, with optical absorption measurements in conjunction with EQE, one can decouple optical losses from carrier collection losses. By this method, an IQE (internal quantum efficiency) for the device can be extracted. Absorption was measured using a spectrometer with integrating sphere in transmission and reflection, and calculated as the difference of these from unity (Absorption(λ) = 1 - Transmission(λ) - Reflection(λ)), assuming all scattered light is captured by the integrating sphere. The comparison of average EQE data from 9 devices spanning the optical measurement region demonstrates an IQE for the InGaN region of greater than 90%.

WEDNESDAY PM

4:10 PM Student

N8, Design Principles for Light-Trapping in Thin Silicon Films with Embedded Dielectric Nanoparticles: *James Nagel*¹; Michael Scarpulla¹; ¹University of Utah

Photovoltaic technology based on thin silicon films is attractive as it reduces the bulk material costs of manufacture. Unfortunately, photon absorption in the near-infrared spectrum is very weak in silicon, thereby resulting in significant loss of potential photocurrent. Much research is therefore focused on advanced methods for trapping light in thin silicon films as an avenue for recovering this unused power. In our recent work, we explored a concept for optical absorption enhancement using embedded dielectric nanoparticles inside an infinite silicon half-space. The absorbed power in the top 1.0 μm of the silicon was increased by 6% based solely on excess path length of the first optical pass. In this work, we explore the effects of embedded nanoparticles in finite structures capable of waveguiding and non-trivial path-length enhancement. We first consider the influences of varying the geometric parameters relating to SiO₂ nanospheres embedded in a 1.0 μm layer of crystalline silicon sandwiched between a 75nm Si₃N₄ anti-reflective coating and an Al back contact. The layout for an embedded nanosphere is defined by a characteristic diameter D, depth z, and pitch p. Using numerical simulations based on the finite-difference time-domain method (FDTD), we explore the effects of varying each parameter by calculating the net absorption gain in incident solar photons within the active semiconductor layer. Under ideal conditions, absorption gains due to embedded spheres of SiO₂ can reach as high as 23% relative to an identical geometry without the embedded nanoparticles. We also infer a series of design principles from our results that include trade-offs between light-trapping, displacement of active semiconductor material, out-coupling through the top surface, and silicon absorption at long wavelengths. Absorption gain may be further increased beyond 30% by embedding coated metallic spheres, which possess a stronger scattering efficiency in silicon than pure dielectrics. Using a tandem design based on crystalline and amorphous silicon, we also simulate the effects of surface texturing and embedded particles both in isolation and in combination. We then infer another series design principles based on advanced, hybrid approaches that attempt to maximize light-trapping in tandem cells.

4:30 PM Student

N9, Single Crystalline Si Substrate Growth by Lateral Diffusion LPE Technology for PV Applications: *Li Bo*¹; Adrian Kitai¹; Huaxiang Shen¹; ¹McMaster University

Lateral Diffusion Liquid Phase Epitaxy (LDLPE) is a new, modified LPE technology and it is a candidate technology for curf-free semiconductor substrate production. LDLPE shares the same advantages as conventional LPE technology: low cost, high growth rate, premium quality of grown crystal, feasibility of selective epitaxy and lateral growth with high aspect ratio. Furthermore, LDLPE enhances the lateral growth and increases the aspect ratio. If used with temperature gradient technology, LDLPE can achieve continuous epitaxial growth, making it possible to grow self-supported single crystalline semiconductor substrate for photovoltaic applications. As a demonstration, single crystalline silicon substrate is grown by LDLPE. A silicon dioxide layer is grown on an n-type <111> single crystalline silicon substrate. The SiO₂ mask is formed by lithography and it is patterned with a set of parallel 100 μm width opening windows as seed lines, which are aligned to <211> orientation. With conventional LPE technology, P-type silicon is epitaxially grown on seed lines. Two single crystalline silicon strips are formed on one single seed line, one strip on either side of the seed line. And there is a gap between these two strips. The typical dimensions of the silicon strip are 70 μm x 40 μm x 5mm (the length of the seed line). To achieve LDLPE, a special graphite slide boat is designed: a silicon bar (1mm-3mm width and entirely covered by SiO₂) is placed 250 μm ~ 750 μm above the seed line. This bar can restrain the increasing of silicon strip thickness by blocking the diffusion pathway of silicon atoms from the bulk indium/silicon melt to the top surface of the silicon strip. Silicon atoms in the bulk indium/silicon melt can only access the silicon strip's side wall. Therefore, under the continuous LDLPE growth condition (when temperature gradient technology is applied, Si source is supplied continuously), when the strip grows to a certain size, the strip does not increase its' thickness anymore,

but increase it's width continuously, forming a single crystalline Si substrate. Both simulation and experiment results demonstrate that the new technology, LDLPE, can grow self supported single crystalline silicon strips with higher aspect ratio than that achieved by the conventional LPE technology. These silicon substrates can be peeled off from the substrate for low cost high efficiency silicon solar cells.

4:50 PM N10, Late News

Session O: III-Nitrides: UV Emitters and Detectors

Thursday AM
June 23, 2011

Room: Corwin East
Location: Univ. of California-Santa Barbara

Session Chairs: Michael Wraback, US Army Research Lab; Leo Schowalter, Crystal IS, Inc.

8:20 AM

O1, Fabrication of UV Emitting Devices Using Vertical ZnO Nanorod Arrays on the p-GaN Films: *Shrawan Jha*¹; Oleksandr Kutsay¹; Igor Bello¹; Shuit-Tong Lee¹; ¹City University of Hong Kong

We report UV light emitting devices (LEDs) based on integration of n-ZnO nanorods and p-GaN films. Reported UV LEDs show stable and repeatable Electroluminescence (EL) and Current-Voltage (I-V) characteristics. To fabricate these devices, integration of ZnO nanorods on the GaN substrates was studied in detail using standard material and optical characterization techniques and then the knowledge was applied in fabrication process of the UV LEDs. A low temperature hydrothermal growth process was used to grow vertical n-ZnO nanorods on p-GaN templates. Analytical techniques (X-ray diffraction, EDX and TEM) suggested good quality epitaxial growth of nanorods on the films. A small lattice mismatch between ZnO and GaN lattice could allow an epitaxial growth. From Scanning Electron Microscopy (SEM) inspection of LED samples, it was observed that most of the nanorods have hexagonal radial cross-section and flat faceted top and side surfaces. Nanorods had a typical diameter of 200 nm, and nanorod-to-nanorod separation of ~50 nm. Baseline GaN technology was used to fabricate LED device structures and Ni/Au ohmic contacts were created over the p-GaN. The p-n junction area was seeded with ZnO and exposed to a nanorod growth solution. Silver ohmic contacts were applied to the ZnO nanorods. Devices were packaged in a modified dual-in-line ceramic package and subjected to further characterization. Electrical characterization (I-V measurements) of the fabricated devices was performed using a Keithley-4200 Semiconductor Parameter Analyzer. UV LEDs showed a rather low turn-on voltage in the range 2.4 V ~ 3.0 V. All the LED devices showed a perfect I-V curve with a large rectification ratio (>300), which is typical of a good quality p-n junction. In addition it was encouraging to note that the devices emit light at a reasonably small injection current of the order 10-2 A/cm². Only a good heterointerface between ZnO nanorods and GaN films could facilitate all these impressive electrical behaviour. Electroluminescence characterization of the LEDs was performed using ACTON SpectraPro 500i monochromator equipped with a PI-MAX ICCD camera. EL spectra of the studied UV LEDs showed a peak in the range 370 nm ~ 385 nm, which was identified as shifted band-to-band transition from ZnO nanorods. A range of UV peak in the EL spectra can be explained considering individual emission behaviour of different nanorods. Further, transient EL spectra were accumulated at different bias voltages and it was established that the devices switch almost instantaneously when electrical pulse to the device is switched on and off. Again, it reflects the quality of the electrical interface between the two materials. This work was supported by the RGC Hong Kong under grant No CityU 110208 and CityU 110209.

8:40 AM

O2, Low-Threshold ZnO Random Laser Diode Realized by Double Heterojunction Structure: *Jieying Kong*¹; Sheng Chu¹; Zheng Zuo¹; Jingjian Ren¹; Mario Olmedo¹; Jianlin Liu¹; ¹University of California, Riverside

Semiconductor laser diodes (LD) play an important role in daily life in the fields of healthcare, information storage, and defense. Lowering threshold current is a key goal on which scientists and engineers put a great deal of efforts in the past half century. ZnO has potential as an alternative to III-V nitride, due to its direct band gap of 3.4 eV and large exciton binding energy of 60 meV. However, the current issue is the difficulty of p-type doping, which restricts the realization of electrically pumped LDs. Previously, our group realized p-type

ZnO by Sb doping. In this study, we report a diode structure with embedded MgZnO/ZnO/MgZnO DH structure, where the MgZnO barrier is thick and the ZnO well is wide. The structure was grown on n-type Si (100) substrate (1-20 O·cm) using plasma-assisted molecular beam epitaxy (MBE) system. A thin magnesium oxide (MgO) buffer layer was first deposited at 350 °C to reduce the lattice mismatch between Si and ZnO, followed by 200 nm Ga-doped n-ZnO at 550°C. After the growth of n-ZnO, a Mg_{0.1}Zn_{0.90}/intrinsic ZnO/Mg_{0.1}Zn_{0.90} heterostructure was grown. Then the temperature was increased to 600°C and 200nm Sb-doped p-ZnO was grown. High-temperature post-annealing at 750°C was performed to activate acceptor dopants. As-grown sample exhibits closely packed columnar structure with size of 200 nm on average, as a result of large lattice mismatch between Si and ZnO. The elemental distribution of Zn, O, Mg, Ga, Sb and Si was obtained by performing secondary ion mass spectroscopy (SIMS) measurements, showing clear MgZnO/ZnO/MgZnO well structure at around 200 nm depth under surface. Current-voltage characteristic of the device shows Ohmic behaviors of n-contacts and p-contacts and the rectifying characteristic of a p-n diode. Turn-on voltage can be determined to be about 5V. Lasing emission was collected from mesa surface as the diode was biased under DC forward voltages. Electroluminescence spectra of the diode show clear laser breakout as drive current increases above 30 mA. Both the number and intensity of sharp lasing mode peaks in the spectra region increase as the injection current increases. This is due to the formation of additional random cavities. Optical gain is realized due to multiple scattering from column walls. Because of random scattering, random close loops are formed to realize laser emission.

9:00 AM Student

O3, ZnMgO-Based Photodetectors for Short Wavelength and Light Polarization Detection: *Gema Tabares*¹; Adrián Hierro¹; Christiane Deparis²; Christian Morhain²; Jean-Michel Chauveau²; ¹ISOM-Dept. Ingenieria Electronica, Universidad Politecnica de Madrid; ²CNRS-CRHEA.

ZnO is becoming a strong competitor for next-generation UV photodetection due to its wide band gap energy, the possibility to do bandgap engineering by alloying with Mg, and the fact that it is relatively easy to deposit structures with non-polar orientations. Not only that, the recent availability of ZnO substrates is starting to allow homoepitaxy, which can lead to very high crystal quality layers, and thus to highly improved figures of merit. In this work, we have analyzed the spectral response of a set of ZnMgO-based Schottky photodiodes and their performance as a light polarization-sensitive UV photodetectors. A high performance semitransparent Au-Schottky contact (100 Å) was fabricated on non-polar Zn_xMg_{1-x}O films and structures with ten ZnO/Zn_xMg_{1-x}O multiple quantum wells (MQW's). These structures were grown by MBE with a-plane orientation both on ZnO and on sapphire substrates to provide control over the strain state and to serve as a comparison of the different technologies. The spectral response of all ZnMgO-based Schottky photodiodes has been measured under reverse biases, with typical UV/visible contrasts of about 10³-10⁴. All of the detectors based on ZnO/ZnMgO MQW's exhibit quantum confinement, and in the case of the homoepitaxial structures, a high responsivity up to 0.1 A/W with a quantum efficiency near unity, and indeed, with photoresponse times of 1-2 s. Long absorption energies can be obtained using single ZnMgO layers grown on ZnO reaching above 4 eV, and still having an excellent contrast and quantum efficiency. The dependence of the responsivity on bias voltage has been studied as well, finding that after a certain voltage, the slope of the curve increases dramatically leading to the presence of gain. This onset is around -2 to -3V for the MQW photodiodes. Furthermore, these non-polar ZnMgO-based Schottky photodiodes show an intrinsic in-plane optical anisotropy that leads to light polarization sensitivity. By using structures grown on ZnO and sapphire, one can control the type of strain, as well as the absorption magnitude, both of which are also dependent on the Mg content. Taking into account the fact that the ZnO layers in the ZnO/ZnMgO MQW's grown on ZnO are strain-free, a clear shift of the absorption edge by 40 meV is obtained between light polarization parallel and perpendicular to the c-axis (in plane), together with a maximum contrast of R_{||}/R_⊥ ~3.3. In non-polar ZnO/ZnMgO MQW's grown on sapphire, the responsivity shows a polarization sensitivity of ~20 meV and a R_{||}/R_⊥ contrast close to 7, which match well the calculations for the A, B, and C

excitons, taking into account the compressive strain along the c-axis as well as the tensile strain perpendicular to it present in these films.

9:20 AM

O4, Fabrication and Characterization of 265 nm Light Emitting Diodes on AlN Single Crystal Substrates: Ramón Collazo¹; Seiji Mita²; Jinqiao Xie²; Anthony Rice¹; James Tweedie¹; Rafael Dalmau²; Baxter Moody²; Raoul Schlessler²; Ronny Kirste³; Axel Hoffmann³; Zlatko Sitar¹; ¹North Carolina State University; ²HexaTech, Inc.; ³Technical University Berlin

AlGa_xN alloys on AlN single crystal substrates have attracted considerable attention as the building blocks of current deep UV light emitting diode technology. In previous studies, AlGa_xN films with varying compositions and doping levels were deposited on homoepitaxial AlN layers grown on AlN single crystal substrates. If relaxation is not essential for a given application, relaxation schemes can be avoided altogether in favor of pseudomorphic AlGa_xN films on AlN. For compositions above 65% Al, the films were pseudomorphic. A light emitting diode grown on AlN single crystal substrates based on pseudomorphic AlGa_xN films will be described. In addition, an estimation of the internal quantum efficiency based on photoluminescence measurements for multi-quantum wells emitting at wavelengths between 245 nm and 270 nm was obtained. The structure was grown on a vicinal cut (0001)-oriented AlN single crystal substrate with an absorption coefficient of less than 50 cm⁻¹. MOCVD was used for its deposition, using the typical precursors. The n-type layer was doped with Si to 1x10¹⁹ cm⁻³, while the p-type layers were doped with Mg to 4x10¹⁹ cm⁻³. The corresponding Si doping in this Al_{0.75}Ga_{0.25}N film yielded a sheet resistance of 100 Ω/□. The structure was finished with a 200 nm p-GaN layer as hole injection layer. The active layer consists of a periodic structure of 5 nm AlN/ 1.5 nm Al_{0.60}Ga_{0.40}N repeated 4 times. The optical properties of this active layer were characterized by temperature dependent photoluminescence measurements from which an internal quantum efficiency (IQE) was estimated. These measurements were performed on different structures, emitting at three different wavelengths: 244 nm, 252 nm, and 261 nm. LED fabrication consisted of reactive ion etching to define the mesa structure and subsequent Ohmic contact metallization for the n- and p-type layers. The external quantum efficiency (EQE) is the product of the IQE and the light extraction efficiency. For emission around 260 nm, with an IQE of 43%, a light extraction efficiency of 12% is needed to achieve an EQE of 5%. For the fabricated LED described above, a rectification ratio of 10000 at 16 V is observed, along with a maximum current of 207 mA at 19 V. The turn-on voltage for this diode is below 10 V. Such a high turn-on voltage is expected if a GaN layer is used as the p-type layer for the junction, arising from the heterojunction discontinuity. The relatively larger turn-on voltage limits the possible wall-plug efficiency to 40% of the EQE, thus if an EQE of 5% is expected, the maximum wall-plug efficiency will be around 2%. The electroluminescence spectra showed LED emission at 265 nm with a FWHM of 11 nm. Precise EQE measurements and reliability measurements will be presented for the described LEDs.

9:40 AM

O5, Time-Resolved Photoluminescence of AlInN/AlN Multiple Quantum Well Active Regions for Mid-UV Emitters: Gregory Garrett¹; Hongen Shen¹; Michael Wraback¹; Hee Jin Kim²; Zachary Lochner²; Jae-Hyun Ryou²; Russell Dupuis²; ¹US Army Research Laboratory; ²Georgia Institute of Technology

AlInN/AlN multiple quantum wells (MQWs) offer the possibility of reduced polarization fields and may provide opportunities for improved radiative efficiency through carrier localization relative to their more commonly employed AlGa_xN/Al(Ga)N counterparts. In this paper we present time-integrated and time-resolved photoluminescence (TRPL) studies of AlInN/AlN MQWs. The sample studied consisted of four AlInN QWs, 2 nm thick, with 2 nm AlN barriers and cap. This was on a 1 μm thick AlN buffer layer all grown by low pressure metalorganic chemical vapor deposition (MOCVD) on a c-plane sapphire substrate. Indium composition in the AlInN well was estimated to be 12% by high resolution x-ray diffraction. Temperature dependent TRPL was taken using a time-correlated single photon counting technique with 25 ps resolution. The excitation pulse source was a quadrupled Ti:Sapphire at 199.5 nm, allowing for increased carrier density through

absorption in the AlN barriers. The excitation fluence ranged from ~0.75 to 100 μJ/cm². Photoluminescence scans showed a peak at 276.7 nm at 13 K that shifted to 280.8 nm at 166 K while the intensity saturated and became sub-linear at high pump-powers. From 166 K to 300 K the PL shifted back toward 278 nm while becoming super-linear in intensity at all powers. At high fluence the peak was seen to blue-shift at all temperatures. A substantial low energy tail was also seen. The observation that the blue-shift with increasing fluence does not lead to a superlinear increase in PL emission at low temperature suggests a minimal electric-field contribution to emission from the deep and narrow wells, as carrier-induced screening of the polarization field should lead to enhanced wave function overlap and an improved radiative recombination rate. Rather, the blue-shift and sublinear PL emission intensity with increasing pump power imply band-filling of localized states in the wells, with a potentially reduced radiative recombination rate associated with delocalization of carriers at high pump power. The transition from sub- to super-linear intensity with temperature increase from 166K to room temperature shows the dominance of non-radiative recombination involving saturation of trap states, as reflected by the approximated IQE of 3% taken from the ratio of the room- to low-temperature PL. TRPL scans were dominated by a pronounced stretched exponential decay that is often associated with emission from excitons localized in an ensemble of tail states. At room temperature, the stretched decay is still observed at longer times, but the initial decay time shrinks from 186 ps at low temperature to 92 ps at room temperature, consistent with the low IQE. These studies suggest that carrier localization in AlInN MQWs may have a more pronounced effect on radiative recombination than that observed in traditional AlGa_xN structures, providing an intriguing alternative for mid-UV devices incorporating bulk AlN.

10:00 AM Break

10:20 AM Student

O6, Enhanced Inter-Band Tunneling by Polarization Engineering in InGa_xN/GaN Quantum Wells: Sriram Krishnamoorthy¹; Aaron Arehart¹; Digbijoy Nath¹; Fatih Akyol¹; Pil Sung Park¹; Michele Esposito¹; Steve Ringel¹; Siddharth Rajan¹; ¹The Ohio State University

The III-Nitride material system has demonstrated its potential for a broad range of optoelectronic and electronic applications. There have been no reports of efficient III-Nitride tunnel junctions, mainly due to challenges stemming from the large band gaps found in this material system. In this work, we show that with unique properties such as the polarization, huge band bending can be created over smaller distances in nitride heterostructures by utilizing the high field due to the polarization charges that are induced at the polar heterointerfaces. In this work, we design and demonstrate GaN/InGa_xN/GaN tunnel junction with a record high current density of 118 A/cm² at a reverse bias of 1 V by utilizing a 6.4 nm thin In_{0.33}Ga_{0.67}N barrier material. N-polar p-GaN/In_{0.33}Ga_{0.67}N/n-GaN heterostructure designed for tunneling close to zero bias was grown by plasma assisted molecular beam epitaxy by choosing the critical thickness of InGa_xN barrier appropriately. N-Polar orientation was chosen due to higher indium uptake in this orientation. The tunnel junction sample shows five orders of magnitude higher current at a reverse bias of 1 V as compared to a standard p+/n+ GaN sample. The tunneling turn-on observed close to zero bias, and the maximum current density of 9.1 kA/cm² achieved in this work demonstrates the potential incorporation of such polarization-engineered tunnel junctions in nitride optical emitters. Two distinct regimes of transport are identified based on the temperature dependent I-V measurements. At lower reverse bias, defect assisted tunneling with strong temperature dependence is found to dominate. In this regime, a plot of ln(J/E) vs E^{1/2} shows a linear behavior suggesting a Frenkel-Poole emission mechanism due to the high field in the InGa_xN quantum well. A direct band to band tunneling regime resulting in weak temperature dependence that arises from band gap variation with temperature is observed from a reverse bias of 1 V. A decrease in current density is observed with increase in temperature in the range of 77-150 K and this can be attributed to the presence of band tail states which has been observed previously in In face InGa_xN. We have explored the design of

these quantum well tunnel junctions. Although higher indium compositions yield higher band to band tunneling probability, calculations using a simplified kane model reveal that the wider depletion region in n GaN due to higher band offset considerably reduces the net tunneling probability indicating that very high indium compositions might not be beneficial to the device performance. Calculations also reveal the need for very high doping in the n GaN layer so as to minimize the depletion region thickness in order to achieve very high current densities. These calculations can guide future tunnel junctions with better performance characteristics.

10:40 AM

07, Effects of Polarization Interface Charge on GaN/SiC Separate Absorption and Multiplication Avalanche Photodiodes: *Chad Gallinat¹, Anand Sampath, Ryan Enck¹, Paul Rotella¹, Paul Shen¹, Michael Wraback¹, Qiugui Zhou², Dion McIntosh², Joe Campbell²,* ¹Army Research Lab; ²University of Virginia

We have demonstrated III-nitride/SiC separate absorption and multiplication avalanche photodiodes (SAM APDs) for high sensitivity detectors operating in the near ultraviolet wavelength region. We have further shown the importance of device design accounting for the formation of polarization induced positive interface charge arising from the difference in the spontaneous polarizations of 4H-SiC and GaN at the hetero-interface. This charge can be sufficient to fully confine the electric field within the SiC multiplication region of the device that would likely reduce hole collection efficiency due to (1) a reliance on the diffusion of photo-generated holes into the multiplication region and (2) the presence of a high density of defects at the hetero-interface resulting in these carriers being lost to defect-mediated recombination. Finally, we demonstrate that the net interface charge density may be tailored to optimize device performance by introducing an interface charge control layer doped with acceptors to offset the positive polarization induced charge. GaN/SiC SAM APDs were fabricated employing a 2 μm thick p+- SiC layer, a 480 nm thick v- SiC multiplication region, a \sim 300 nm thick v-GaN absorption region and capped with a thin 10-50 nm thick n+-GaN layer. The role of the interface charge was explored by varying the thickness of a p-type interface charge control layer (PICCL) from 0-15 nm. 130 μm diameter APDs exhibited dark currents less than 0.1 nA at 156V; similar to what is observed for a wholly SiC APD. This result suggested that the reverse leakage currents in these devices were limited by the SiC multiplication region despite the presence of threading dislocations at the hetero-interface. It is important to note that the dark current in these devices was \sim 1000x lower than what has been observed for GaN APDs despite having \sim 25x larger device areas. APDs with PICCLs less than 15 nm were found to exhibit spectral responses whose shape is consistent with results modeling the collection of photo-generated holes directly in the SiC multiplication region through a 300 nm thick GaN filter for all reverse biases. This result is attributed to the inefficient collection of photo-generated holes in the GaN absorption region due to the predicted confinement of the electric field within the SiC multiplication region from excess polarization induced interface charge. In contrast, devices having a 15 nm thick PICCL exhibit a similar SiC related response at low and moderate reverse biases and a gradual transition to a GaN dominated response for biases greater than \sim 150V and before avalanche breakdown at $>$ 158V. This transition is attributed to the gradual rather than sharp depletion of the GaN absorption region with increasing bias above 150V.

11:00 AM

08, Low-Temperature Growth and Characterization of p-GaN and Graded p-InGaN Layers by MOCVD for Photovoltaic Applications: *Matthew Laurent¹, Ajay Raman¹, Daniel Denninghoff¹, Stacia Keller¹, Umesh Mishra¹,* ¹UC Santa Barbara

In the development of high-efficiency thin-film solar cells in the III-N system, it is critical to maximize the figures of merit relating to overall power conversion efficiency. Open circuit voltage (V_{oc}), short-circuit current density (J_{sc}) and fill factor (FF) of the device are dependent upon the crystal quality and number of photons converted to electron-hole pairs. For $\text{In}_x\text{Ga}_{1-x}\text{N}$ -based photovoltaics, which are being considered as a top cell in multi-junction solar cells, it is necessary to increase the indium fraction, x, in the crystal such that

the absorption edge extends into the green portion of the visible spectrum. p-GaN growth on top of the unintentionally doped active region becomes a significant challenge for two main reasons: 1. defect propagation from the active region can provide significant leakage pathways for the device, thus decreasing shunt resistance and the fill factor of the device; and 2. high-conductivity p-GaN favors higher temperature growth, which damages the underlying $\text{In}_x\text{Ga}_{1-x}\text{N}$ layer. The development of InGaN-based photovoltaics requires growth of p-type layers near active layer growth conditions with high crystal quality and low sheet resistance. High sheet resistance increases the overall series resistance of the device, which degrades the FF. Previous reports have shown that the optimal thickness for p-GaN in III-N photovoltaics is between 100 and 150 nm. This paper presents the electrical characteristics of low-temperature films of p-GaN and graded p-InGaN alloys grown on c-plane sapphire by MOCVD. The grading of the doped layer is beneficial in the nitride material system, since grading distributes the polarization charge throughout the layer. The negative polarization charge is compensated by ionization of additional Mg acceptors. If graded properly, phenomenon can result in the valence band being pulled above the Fermi level, thus forming a three-dimensional hole gas. Samples were graded to $x = 0.10$ to ensure valence band degeneracy. Polarization doping has been exhibited in graded p-AlGaIn layers on the N-face of GaN, and in multiple quantum well samples on the Ga-face. For Ga-face devices, it is more desirable to have a single graded layer with no heterojunction barriers. Hall measurements were performed on samples with 155-nm-thick graded p-InGaIn layers. We report a decrease in sheet resistance by a factor of three (from 9×10^5 to $3 \times 10^5 \Omega/\square$) and an increase in charge carrier density by an order of magnitude (from 1.09×10^{17} to $1.06 \times 10^{18} \text{ cm}^{-3}$) over typical p-GaN layers, but with decreased mobility. For device application, indium content in the p-layer should be minimized to avoid absorption. Simulations show that layers graded to as little as $x = 0.03$ will be effectively polarization-doped. With such band engineering, it should be possible to significantly reduce the series resistance in solar cells, and therefore the FF and power conversion efficiency.

11:20 AM Student

09, Carrier Lifetimes and Recombination Phenomena in InGaN/GaN Quantum Dot and Quantum Well LEDs: A Comparative Study: *Animesh Banerjee¹, Meng Zhang¹, Boon Ooi², Pallab Bhattacharya¹,* ¹University of Michigan; ²KAUST

The development of nitride-based quantum well visible light emitting diodes (LEDs) has been impeded by the observed loss of efficiency at high injection levels – a phenomenon generally termed “efficiency droop”. The problem is more serious for longer wavelengths – blue to green – since the large In content in the wells leads to a higher polarization field and clustering effects. It has been shown, theoretically and experimentally, that the polarization field and the resulting quantum confined stark effect (QCSE) are significantly lower in self-organized InGaIn/ GaN quantum dots (QDs). Superior performances in green-emitting quantum dot LEDs have been demonstrated by us recently. In order to gain a better understanding, we have performed temperature-dependent differential carrier lifetime measurements on QD LEDs with peak emission $\lambda_p \sim 420$ nm. The results have been compared with those obtained from identical measurements on InGaIn/ GaN multi quantum well (MQW) LEDs. InGaIn/ GaN QD LED heterostructures were grown on c-plane GaN-templated SiC substrates by plasma-assisted MBE. The dot density in a layer of quantum dots is determined from independent AFM measurements to be $\sim 8 \times 10^{10} \text{ cm}^{-2}$ for the growth conditions used. The peak emission is observed at $\lambda_p \sim 420$ nm. InGaIn/ GaN MQW LED heterostructures emitting at $\lambda_p \sim 452$ nm were grown by MOCVD. Light-current characteristics of both kinds of devices were measured in pulsed mode and the external quantum efficiency as a function of injection current were obtained from these characteristics. The droop in efficiency for the QD LED occurs at 200 A/cm^2 , compared to $\sim 10 \text{ A/cm}^2$ for the MQW LED. The estimated peak of external quantum efficiency (EQE) of the QD device is $\sim 11 \%$, noting that no optimization of light extraction has been done in these heterostructures. The measured peak internal quantum efficiency (IQE) is 77.8 %. Differential carrier lifetime (τ) measurements were made with a small AC signal (10 MHz, $V_{max} = 250 \text{ mV}$) superimposed on the

varying DC current bias. τ is obtained from the phase delay between the input electrical signal and the output optical signal. The radiative and non-radiative lifetimes, τ_r and τ_{nr} , are then derived from the measured τ and internal quantum efficiency (IQE) at room temperature. The nature of variation of these lifetimes have been analyzed and explained. The lifetime data for both devices were analyzed with the A-B-C model to determine these coefficients. Here C is the Auger coefficient. It is seen that the values of the Auger coefficient are very similar. The superior performance of the QD LEDs is attributed to the lower carrier density n in the wells for the same J due to a more uniform distribution of carriers over all the dot layers.

11:40 AM

O10, Characterization of Ultraviolet LEDs by Electrical Analysis and Laser-Based Failure Analysis Techniques: *Mary Miller*¹; Edward Cole Jr.¹; Paiboon Tangyonyong¹; ¹Sandia National Laboratories

Even though ultraviolet light emitting diodes (UV LEDs) are now commercially available with wavelengths as short as 240nm, there are a number of formidable material issues that act as roadblocks to the production of efficient, long lifetime UV LEDs. In this work, we expand the use of thermally-induced voltage alteration (TIVA) and light-induced voltage alteration (LIVA) to localize potential precursors that may lead to premature failure in deep UV LEDs. UV LEDs were imaged using lasers with wavelengths of 532, 1064 and 1340nm. In LIVA and TIVA, a laser is rastered across a device under constant current bias. Dark or bright spots are generated in an applied voltage map, dictated by increases or decreases in the voltage of the LED and localized by the laser position. When the UV LEDs were scanned, dark and distinct defect spots were localized. Some defect spots which only appeared only under 532nm stimulation are likely areas of electron-hole pair generation since the spots appeared dark. Other defect spots were present under all wavelengths. Current-versus-voltage (IV) curves were also measured under laser interaction. When the devices were subjected to uniform heating, the current over the entire measured voltage range (-3 to 8V) increased with increasing temperature. In contrast, an increase in current occurred only on a specific part of the measured voltage range (-3 to ~4V) when the devices were subjected to localized heating with the 532nm laser on the defect position. This suggests that stimulation with the 532nm laser produces an effect that is not entirely thermal. Also, this increase in current only occurred with any significance when the defect was spotted with the 532nm laser. This again suggests that the effect is more of an e-h pair transition, rather than a thermal effect, involving energies of 2.33eV or higher. Plotting the voltage map intensity of the imaged TIVA/LIVA defect spots against the IV curve showed that a secondary slope in the IV curve between ~3 and 4V matched the onset and termination voltage of the electrically active defect spots identified in the applied voltage map. Almost all of the devices with no defects in the voltage maps do not have the secondary slope. When the 532nm laser was spotted on the defect, the slope did not change but the current increased. When the laser was spotted off of the defect, the slope decreased or disappeared, mimicking a device IV curve with no electrically active defects. This suggests that the secondary slope within the IV curve directly relates to the presence of the observed defect within the material. This work highlights how the TIVA/LIVA techniques can be used in characterizing electrically active defects in UV LEDs.

Session P: Oxide Semiconductor Devices

Thursday AM
June 23, 2011

Room: Corwin West
Location: Univ. of California-Santa Barbara

Session Chairs: Jamie Phillips, The University of Michigan; Patrick Shea, Northrop Grumman Corporation

8:20 AM Invited

P1, Memristance and Current-Driven Phase Transition in Multifunctional Binary Oxide Nanodevices: *Matthew Pickett*¹; Julien Borghetti¹; J. Joshua Yang¹; Gilberto Medeiros-Ribeiro¹; R. Stanley Williams¹; ¹Hewlett-Packard Laboratories

Nonvolatile bipolar resistance switching in binary oxides was discovered in the early 1960s but has gained interest more recently as a potential competitor in the nonvolatile memory market. As a result, a recent wave of research on the phenomenon has dramatically advanced the understanding of material switching mechanisms. Additionally, an important link has been drawn between bipolar resistance switching and the mathematical formalism of Chua's memristor. As such, metal/oxide/metal devices which exhibit the phenomenon are now frequently referred to simply as 'memristors'. In Chua's formalism the resistance is governed by a dynamical state variable, the dynamics of which is determined by a characteristic differential equation. In a specific example, the current-voltage relation of a titanium oxide memristive system has been modeled as an insulating barrier which migrates, via oxygen vacancy motion, at a speed that depends nonlinearly on the polarity and magnitude of applied current. A fundamentally different switching phenomenon of binary oxides (e.g. oxides of V, Nb, Ti and Fe) was also discovered in the early 1960s. Commonly described as 'threshold switching', this phenomenon is characterized by a current-voltage behavior which exhibits current-controlled negative differential resistance (CC-NDR). The switching effect is volatile in the sense that the conductive state can only be maintained while current is flowing through the device. Threshold switching has previously been attributed to current-induced heating which locally heats these oxides above an insulator-metal phase transition temperature. In this case the discrete drop in resistivity which occurs when the device self-heats past the critical phase transition temperature has an unstable positive feedback effect on the current. This results in the formation of a metallic phase conductive filament, a necessary condition of bulk CC-NDR. Here we present an analytical model for and demonstrate the controllable coexistence of memristance and phase-transition-driven CC-NDR in a single nanoscale TiO₂-based metal/oxide/metal device. We show that the coexistence of both phenomena yields a rich behavior which can be reliably modeled. We analyze the electrical oscillations that arise from the CC-NDR of the device in order to characterize the dynamics of the phase transition. Finally, we demonstrate a notable application of this multifunctional device: a tunable voltage-controlled oscillator with efficiency greater than 1% capable of injecting AC energy into nanoscale oxide-based circuits.

9:00 AM

P2, Switching Characteristics and Mechanism of Nano-Scale Memristors Based on Epitaxial ZnO Nano-Islands: *Jing Qi*¹; Mario Olmedo¹; Jingjian Ren¹; Ning Zhan¹; Jianze Zhao¹; Jianlin Liu¹; ¹University of California, Riverside

Resistive random access memory (RRAM) has been attracting attention for high-density, high-speed, and low-power nonvolatile memory technology owing to its simple structure, high-density integration, low-power consumption, fast operation and strong potential for fabricating multilevel-per-cell memories. However, the mechanism for resistive switching is still controversial, especially at the nanoscale. Furthermore, to achieve high-density memory, it is crucial to scale down the size of RRAM cells and the distance between the two electrodes beyond the limitation of current lithography length scale. In this presentation, ZnO nano-islands with diameters of 20-60nm and

heights of about 40nm were deposited on silicon substrates using plasma-assisted molecular beam epitaxy system. Bipolar resistive switching memory effect with memory windows up to 10^7 for single ZnO nano-scale memristors is demonstrated at different current compliance from 50 μ A to 500 μ A, in which p⁺-Si (100) substrate, C-AFM tips, and ZnO nano-islands act as bottom, top contacts and resistive switching active layer, respectively. All four different states (initial, electroformed, ON and OFF) of the nano-scale memristors were measured by conductive atomic force microscope (C-AFM) immediately after the voltage sweep was applied. C-AFM images show that for initial state, the nano-island is evenly conductive for the whole top area of the nano-island. After electroforming, current distribute discretely on the edge area of the nano-island. The density and area of higher current spots for ON state are larger than that of OFF state. According to these results, the model of conducting filament is proposed to explain the memory switching behavior. This research suggests that ZnO is promising for future RRAM at the scaled technology nodes.

9:20 AM Student

P3, Investigation of Multi-Barrier ZnO-Schottky Contacts: *Stefan Müller¹; Holger von Wenckstern¹; Jörg Lenzen¹; Otwin Breitenstein²; Marius Grundmann¹; ¹Universität Leipzig; ²Max-Planck-Institut für Mikrostrukturphysik*

We report on investigations of Schottky contacts (SC) on ZnO thin films that exhibit spatial discrete variations of the barrier height. Current-voltage (IV)-characteristic of multi-barrier SCs on hydrothermal bulk ZnO and ZnO thin films were already published and exhibit kinks in the forward direction, however, a discussion was not given. We determined the area ratios between regions of different barrier height in dependence on temperature, visualized regions of low barrier height by dark lock-in thermography (DLIT) and provide chemical analysis hinting on the origin of low barrier regions. For this study we used nominally undoped ZnO thin films grown on a ZnO:Al buffer on 2 inch a-plane sapphire wafer by pulsed-laser deposition. On the nominally undoped layer about 500 circular PdO₂/ZnO-SCs were fabricated by reactive de-sputtering. The areas of the SCs are in the range from 1.8×10^{-4} to 4.4×10^{-3} cm². About 100 of the prepared SCs exhibit one or more kinks in the room temperature (RT) IV-characteristic being a clear indication for the existence of multiple barriers. Selected multi-barrier SC were further investigated by temperature-dependent IV measurements. The characteristics were modelled by assuming a parallel connection of two or more individual diodes. From the model sets of the characteristic parameters (ideality factor and barrier height) for the low and high barrier region are deduced, e.g. RT values of (1.33, 0.73 eV), (1.9, 0.81 eV) and (2.36, 0.88 eV), respectively. Using DLIT low-barrier patches were visualized for small forward currents. Current transport at low forward voltages for low temperatures occurs primarily through such patches. The low-barrier regions were investigated with additional techniques, like electron beam induced current and scanning electron microscopy. The origin for the local decrease of barrier height was traced by energy dispersive X-ray spectroscopy on a cross section prepared by focused ion beam and is due to aluminium oxide particles in the buffer layer. However, this explanation cannot be extended to multi-barrier behaviour SC on bulk ZnO.

9:40 AM Student

P4, Interface Charge Characteristics of HfO₂/ZnO Thin Films: *Jeffrey Siddiqui¹; Jamie Phillips¹; Burhan Bayraktaroglu²; Kevin Leedy²; ¹University of Michigan; ²AFRL Wright-Patterson*

ZnO thin film electronics have received much attention due to the high electron mobility of ZnO thin films in comparison to amorphous silicon and organic thin films. The integration of high dielectric constant (high-k) dielectrics in ZnO thin film transistors (TFTs) has demonstrated performance advantages including reduced operating voltage, increased I_{on}/I_{off} ratios, and larger transconductance. HfO₂ has emerged as a high-k dielectric of choice for both silicon microelectronics and thin film electronics, due to the high dielectric constant (~25), low leakage current, and low synthesis temperature. However, there are potential drawbacks for integrating HfO₂ in ZnO thin film transistors including decreased device operation stability in the form of I_D - V_G hysteresis and degradation of subthreshold slope characteristics, which may be

linked to defects at the HfO₂/ZnO interface. I_D - V_G hysteresis and subthreshold slope analysis on TFTs have reported interface state densities (N_{it}) of $\sim 2.7 \times 10^{11}$ and 5.38×10^{12} cm⁻² for HfO₂/ZnO and 2.47×10^{12} cm⁻² for Ta₂O₅/ZnO. Further studies are desired to both understand the influence of these interface states on device behavior and to determine the physical origin and characteristics of the defects. In this work, the electronic properties of HfO₂/ZnO interface states are studied by DC current-voltage, and AC Admittance Spectroscopy on metal/HfO₂/ZnO capacitor and thin film transistor structures. Materials of ZnO and HfO₂ were deposited by pulsed laser deposition and atomic layer deposition, respectively, and device structures were fabricated using standard photolithography and etching techniques. Subthreshold behavior of the transistors indicate an interface state density of $N_{it} = 7.2 \times 10^{12}$ cm⁻². Frequency dependent parallel conductance reveals the energetic dependence of interface state density with a sharp increase near the conduction band edge with D_{it} values ranging from 4.1×10^{11} to 3.2×10^{13} cm⁻²eV⁻¹ for energies within 0.8eV of the bandedge. The integrated value of energy dependent D_{it} is $N_{it} = 5.6 \times 10^{12}$ cm⁻² which is consistent with subthreshold and previously reported results. The interface state characteristics have a time constant of $\tau_{it} = 0.7 \mu$ sec-50 μ sec and capture cross section in the range of $\sigma_n = 4 \times 10^{-20}$ - 2×10^{-8} cm². Further details of the interface state characteristics will be described and related to performance and stability of TFT operation.

10:00 AM Break

10:20 AM Student

P5, Low-Temperature Processed Schottky-Gated Field-Effect Transistors Based on Amorphous Gallium-Indium-Zinc-Oxide: *Michael Lorenz¹; Alexander Lajn¹; Heiko Frenzel¹; Holger von Wenckstern¹; Marius Grundmann¹; Pedro Barquinha²; Elvira Fortunato²; Rodrigo Martins²; ¹University of Leipzig; ²CENIMAT, I3N, FCT-UNL*

We demonstrate metal-semiconductor field-effect transistors (MESFET) based on amorphous oxide channel material. The gallium-indium-zinc-oxide (GIZO) thin films and the Ag_xO-Schottky gate electrodes were deposited at room-temperature. Annealed thin film devices exhibit a subthreshold swing of $S = 112$ mV/decade and gate sweep voltages of 2.4 V. The field-effect mobility is 15 cm²/Vs and on-off-current ratios $> 10^7$ are achieved. Compared to as-grown thin film transistors increased reproducibility and lower gate leakage currents are attained on annealed thin films. Oxide based electronics have recently gained more attention in the research, e.g. due to their applicability in transparent electronics. The current research in this field is entirely focused on metal-insulator-semiconductor field-effect transistors. We demonstrate that the MESFET device concept is not only compatible with polycrystalline zinc oxide thin films, but also with amorphous oxide channel materials. GIZO thin films were grown by radio frequency magnetron sputtering at room temperature on Corning 1737 glass substrates. Subsequent annealing at 150 °C has strong effects on the electrical properties of the thin films (e.g. Hall-effect mobility) and on device characteristics of the transistors, e.g. increased field-effect mobility. The MESFET were fabricated by standard photolithography using lift-off technique. The ohmic source and drain electrodes were sputtered using an Au target in an argon atmosphere. The Schottky gate contacts were sputtered by means of an Ag target in a mixed argon/oxygen atmosphere, which yields a partial oxidation of Ag and hence to higher effective barrier heights for the Schottky contact. The effective barrier height of the Schottky contacts on GIZO channel material, extracted assuming thermionic emission only, is 0.95 eV. The ideality factors of contacts on GIZO were determined for the annealed thin films to be $n = 1.9$ and for the as-grown thin film $n = 2$.

10:40 AM Student

P6, High Pressure Hydrogen Annealing of Indium-Gallium-Zinc Oxide Thin Film Transistors: *Se-I Oh¹; Jae-Hyung Jang¹; Dae-Seok Lee¹; Hyunsang Hwang¹; ¹GIST*

High pressure hydrogen annealing (HPHA) process was employed to introduce hydrogen into the amorphous indium gallium zinc oxide (a-IGZO) channel material more effectively to improve the electrical performance of a-IGZO thin film transistors (TFTs). For the comparative study, a-IGZO TFTs annealed in N₂ ambiance was also fabricated and their electrical performances

were compared with those annealed in high pressure hydrogen ambiance. The electrical characteristics of the as-fabricated devices include the field effect mobility (μ_{eff}) of 0.01 cm²/Vs, subthreshold slope (S) of 2.31 V/decade, and on/off current ratio of 1.42×10^5 . High pressure hydrogen annealing was carried out by controlling hydrogen gas pressure from 1 to 15 atm at 250°C for 20 min. For the control devices, rapid thermal annealing process in N₂ ambiance was applied to the as-deposited TFTs at 300°C for 10, 15, and 20 min. Both the post-annealing processes improved the performances of the TFTs significantly when they are compared with those of the as-fabricated devices. For the N₂-annealed devices, the best performances were obtained from the devices annealed for 15 min. These devices exhibited the S of 1.22 V/decade, the μ_{eff} of 1.03 cm²/Vs, and the on/off current ratio of 1.87×10^8 . Meanwhile, it was found that the performance of the devices annealed in hydrogen ambiance strongly depended upon the hydrogen gas pressure. The field effect mobility increased with the hydrogen pressure. The maximum μ_{eff} of 10.33 cm²/Vs was obtained from the devices annealed at 15 atm. However the best on/off current ratio and the lowest S were obtained from the devices annealed at 5 atm. When the devices were annealed at hydrogen pressure of 10 atm, the carrier density increased a lot, but the field effect mobility did not change much. For the devices annealed under the hydrogen pressure of 15 atm, the current density did not change much, but the field effect mobility was improved around two times when the device performances are compared with those annealed at the hydrogen pressure of 10 atm. From these results, it can be concluded that the hydrogen incorporated in the IGZO channel material effectively increased the carrier concentration leading to the increased current density. When the devices are annealed under the higher hydrogen pressure such as 15 atm, the hydrogen in the IGZO channel effectively passivate the defects in the material so that the field effect mobility was dramatically improved. In summary, by introducing hydrogen in the annealing process, the field effect mobility was order of magnitude improved when it is compared with that of the devices annealed in N₂ ambiance. More detailed experimental procedures, material characteristics, and device performances will be presented. This work was supported by AFOSR grant monitored by Dr. Gregg Jessen and WCU program funded by MEST.

11:00 AM Student

P7, The Effect of Ga Doping on Bias Stress Stability of ZnO TFT: Chieh-Jen Ku¹; Ziqing Duan¹; Yicheng Lu¹; ¹Rutgers University

ZnO based thin film transistors are promising for application in the next generation large-area electronics, such as active matrix liquid crystal displays. Compared to typical amorphous and polycrystalline silicon based TFTs, ZnO based TFTs possess several superior properties including high electron mobility, low temperature processing, and good radiation hardness. For the display application, the bias stressing may lead to instabilities of TFT performances such as charge trapping and defect creation in the channel layer. Therefore, study and improvement of the bias stress stabilities of ZnO based TFTs become one of most critical issues to realize next generation large-area electronics. In this paper, we report the effects of Ga doping on the electrical characteristics and bias stress stabilities of ZnO TFTs. Bottom gate ZnO TFTs are fabricated on heavily-doped n-type Si wafers with a 100 nm thermally grown SiO₂. The 50nm - channel layers are grown by MOCVD at 350°C. Different in-situ Ga-doping levels are realized by controlling the TeGa flow rate [0 sccm (sample A), 5sccm (sample B) and 15 sccm (sample C)] during the growth. Figure 1 shows the transfer characteristics of three TFTs with different TeGa flow rates. The highest field effect mobility of 45 cm²/V-s and lowest subthreshold swing of 286mV/dec are obtained in sample B with a VT of 0.54Vas. As the TeGa flow rate increases to 15 sccm, the subthreshold swing of sample C remains 290 mV/dec but the field effect mobility degrades to 30 cm²/V-s. Moreover, the VT of sample C is shifted to -2.3V, turning the device into a depletion mode which is not desirable for the large area electronics application. In comparison with sample B, the pure ZnO TFT (sample A, without Ga-doping) exhibits larger subthreshold swing of 700mV/dec, lower field effect mobility of 33 cm²/V-s and a VT of 0.2V. Figure 2 shows the positive bias stressing (PBS) results. A gate voltage of +20 V is applied to sample A and sample B with a time period of 5,000s. The shift of threshold voltage (ΔV_T) of sample A and sample

B are +0.5V and +1.3V, respectively. The positive shift of threshold voltage is mainly due to electron trapping in the channel layers or at the dielectric/channel interface without creation of new defects. Thus, the better positive bias stressing stability of sample B can be attributed to lower bulk trap density in the channel layer. In summary, we have investigated the effect of Ga doping on the positive bias stress stability of ZnO TFTs. The improvement of PBS stability is obtained for the lightly doped Ga:ZnO TFT, where the lower positive shift of threshold voltage is mainly attributed to the lower bulk trap density in the channel layer after Ga incorporation.

11:20 AM

P8, Electrically Stable Amorphous InGaZnO Thin-Film Transistors and High-Gain Inverters: Jungbae Kim¹; Canek Fuentes-Hernandez¹; Do Kyung Hwang¹; Hyeunseok Cheun¹; Shree Tiwari¹; Bernard Kippelen¹; ¹Georgia Institute of Technology

High-performance thin-film transistors (TFTs) that use oxide semiconductors such as ZnO and amorphous InGaZnO (a-IGZO) are becoming an attractive alternative to hydrogenated amorphous silicon (a-Si:H) and organic-based materials because of their high electron mobility values and low processing temperatures, making them compatible with flexible substrates and opening the potential for low production costs. However, as with other TFT technologies, achieving long-term operational stability is also a major challenge faced by metal-oxide semiconductor TFTs. The degradation of the performance of a TFT during operation is reflected by changes of its current characteristics that can result from changes of mobility, threshold voltage or variations of the capacitance density. Here, we report on the fabrication of electrically stable amorphous InGaZnO TFTs that can be tuned to operate in either in depletion (D) or enhancement (E) mode without losing its electrical stability. The use of different annealing environments such as air, nitrogen (N₂), and air/N₂ with the control of the annealing temperatures leads to E- and D-mode operations of TFTs with high electrical stability showing less than 6% degradation of the drain currents after 1 hr direct current (DC) bias stress at a voltage of 8 V. In contrast, the current in an un-annealed TFT drops to 52% its initial value. These TFTs showed hysteresis-free voltage transfer characteristics with saturation mobility values of 7 ± 1 and 6 ± 1 cm²/Vs, and threshold voltage values of 2.0 ± 0.5 and -1.5 ± 0.5 for E- and D-mode TFTs, respectively. Here, we also demonstrate that high-gain inverters composed of electrically stable n-channel enhancement-mode (E-mode) and depletion-mode (D-mode) TFTs can be fabricated on a single substrate. As expected from the hysteresis-free current voltage characteristics, the inverters also show hysteresis-free voltage transfer characteristics (VTCs) with the maximum gain values of -62, -53, and -38 V/V at different VD = 8, 7, and 6 V with nearly constant switching threshold voltage (VM) value of 2.8 V. After electrical stress using multiple scans up to 500 cycles and 1 hr DC bias, VTCs of the inverters are slightly changed due to the small current variations of the a-IGZO TFTs. Here, the maximum static gain values at VD = 8, 7, and 6 V were -90, -82, and -52 V/V with VM of 2.5 V. Because p-channel metal-oxide TFTs are proven difficult to realize, the use of these electrically stable inverters based on electrically stable E-mode and D-mode a-IGZO TFTs could be an attractive alternative to a conventional complementary metal-oxide technologies which require the use of a p-channel and an n-channel TFTs.

11:40 AM Student

P9, Growth and Investigation of Hexagonal Zinc Oxide Microdisk Resonators: Kathryn Greenberg¹; John Joo¹; Evelyn Hu¹; ¹Harvard University

Semiconductor microdisk resonators have received considerable attention over the past several years due to their novel approach of using total internal reflection of light in the cavity to create whispering gallery modes. Traditionally, microdisks have been fabricated using a top-down approach, utilizing either dry or wet etching to create the desired size and shape of the microdisk. Here we report the fabrication of hexagonal ZnO microdisks using a bottom-up approach. ZnO microdisks are grown in aqueous solutions of zinc nitrate and ammonium hydroxide. In addition, sodium citrate is added to the solution to slow the growth of the zinc oxide in the vertical direction. The creation of microdisks using a bottom-up approach allows for ease of

fabrication, little waste of material, and the ability to implant structures into the microdisk and continue the growth process. Zinc oxide is a wide bandgap (~3.3eV) semiconductor with a large exciton binding energy (~60meV) making it a desirable material for optoelectronic devices. Here we present the fabrication process of our hexagonal ZnO microdisks and several scanning electron microscope images of ZnO microdisks with various growth parameters, including the concentration of both the zinc nitrate and sodium citrate in the solution as well as the growth time. Using our novel approach, we are able to create an undercut in our microdisks without the use of etching. In addition, photoluminescence spectroscopy is performed to investigate the optical characteristics of the ZnO microdisk cavities. The results obtained from photoluminescence spectroscopy are compared with finite difference time domain (FDTD) simulations to design and optimize the microdisk structure and determine the modes of the resonator and the maximum quality factor of these modes. Overall, we demonstrate the ability to grow zinc oxide microdisks in solution and by varying various parameters change the size of the disks. This novel approach in the fabrication of microdisks presents many advantages over the traditional approach and allows for the possibility of incorporating numerous structures (e.g. quantum dots or nanodiamond) into the microdisks during growth which is difficult with other fabrication techniques. In addition, FDTD simulations and photoluminescence spectroscopy measurements allow us to better understand the quality of the ZnO microdisk cavities we have created and the optical properties of the ZnO that we are growing. Current work is focused on further characterizing and optimizing the conditions for formation of the microdisks, by detailed optical characterization of the structures, as well as developing better control over the shape of the resonators.

Session Q: III-Nitrides: Electronics II

Thursday AM Room: Flying A
June 23, 2011 Location: Univ. of California-Santa Barbara

Session Chairs: Russell Dupuis, Georgia Institute of Technology; Huili Grace Xing, University of Notre Dame

8:20 AM Student

Q1, ALD Al₂O₃ Thickness-Dependent Study of AlN/GaN MOS-HEMTs: Satyaki Ganguly¹; Jai Verma¹; Guowang Li¹; Huili Xing¹; Debdeep Jena¹; ¹University of Notre Dame

In recent years AlN/GaN based high electron mobility transistors (HEMT) have proved attractive for high frequency, high voltage and high power operation. However, the gate leakage current, which limits the drain breakdown voltage, limits the performance of these devices. Therefore atomic layer deposited (ALD) high band gap (6.5eV), high k (9.1) Al₂O₃ has drawn attention of the community due to its excellent dielectric property coupled with thermal and chemical stability. In this work we present a comprehensive study of AlN/GaN MOS-HEMT gate stacks for various ALD Al₂O₃ thicknesses ranging from 2nm to 8nm. For this study the AlN/GaN HEMT structures were grown in a Veeco Gen 930 molecular beam epitaxy (MBE) system on semi insulating 0001 GaN templates (2µm) on sapphire under metal rich conditions. Ga flux of ~2.1 X 10⁻⁷ Torr, Al flux of ~1.6 X 10⁻⁷ Torr and N₂ supplied from a Veeco rf source at a plasma power of 240W were used. The MBE layer structure consisted of a thin 1.5nm AlN nucleation layer (to eliminate the buffer leakage), followed by 235nm UID GaN, and 4nm AlN barrier layer grown at a substrate thermocouple temperature of 660°C. Mesa isolation was achieved with BCl₃/Cl₂ plasma reactive ion etching, followed by source/drain ohmic metalization using Ti/Al/Ni/Au (15/120/40/60 nm) stack deposition followed by rapid thermal annealing in N₂/Ar atmosphere for 30sec at 600°C. A saturation current of 1.3 Amps/mm was measured. The sample was then cleaved into four parts, and four different Al₂O₃ thicknesses (2nm, 4nm, 6nm, 8nm) were deposited on the AlN surface by ALD (with TMA and H₂O as the precursors). Finally, a Ni/Au (50/150 nm) gate metal stack was deposited. The lattice image confirms the thicknesses of

the ALD layers, along with thickness variation within an acceptable window. In order to examine the effect of the ALD Al₂O₃ thickness on the pinch-off voltage of the HEMTs, capacitance-voltage (C-V) characteristics were measured at 1 MHz on circular diode patterns of area A=πx(10 µm)² on the four samples with different oxide thicknesses. The pinch-off voltage increased with the thickness of the ALD oxide layer, from -3.5 V for t_{ox}=2nm to -8.8V for t_{ox}=8nm. The carrier profile extracted from the C-V measurement indicates the varying depth of the two-dimensional electron gas from the gate metal. It was also found that the gate leakage current decreases with increasing t_{ox}, the property that will enable high breakdown voltages in AlN/GaN HEMTs. Thus, for high speed performance, thinner gate oxides are necessary for high gain, whereas for high breakdown devices, thicker oxides would be necessary at the expense of gain. This study will help provide metrics towards choosing optimal thicknesses depending on the application.

8:40 AM Student

Q2, Al₂O₃ Based Etch-Stop Technology for the Gate Recess in N-Polar AlGaIn/GaN MIS-HEMTs with Si_xN_y Passivation: Seshadri Kolluri¹; David Brown¹; Andrew Carter¹; Stacia Keller¹; Steven DenBaars¹; Umesh Mishra¹; ¹University of California, Santa Barbara

Recent N-polar AlGaIn/GaN MIS-HEMTs, using High Temperature CVD (HTCVD) grown Si_xN_y as the gate insulator, have demonstrated small-signal and large-signal performances comparable to Ga-polar devices. A recessed gate structure with integrated slant field plates, obtained by a timed etch through the PECVD Si_xN_y passivation, is normally used to prevent DC to RF dispersion in these devices. However, such a timed gate recess etch is very unreliable due to poor selectivity between PECVD Si_xN_y used for surface passivation, and HTCVD Si_xN_y used as the gate dielectric. This leads to either a high gate leakage (for over-etching), or a low transconductance (for under-etching). Despite these issues, HTCVD Si_xN_y is still preferable over other gate dielectrics, because it is a more mature technology and it can be deposited in-situ in MOCVD chamber. This work presents an Al₂O₃ based etch-stop technology for N-polar devices with Si_xN_y passivation, to improve the reproducibility and accuracy in etch depth for the gate recess. A CF₄/O₂ plasma based etch, using reactive-ion-etching (RIE) process, has been characterized to study the etch-selectivity between PECVD Si_xN_y and Al₂O₃ deposited by Atomic Layer Deposition (ALD). A high Si_xN_y to Al₂O₃ etch-selectivity of 86 was obtained with CF₄/O₂ flow rates of 20/2 sccm, and a chamber pressure of 20mT. Lower chamber pressures are desirable for vertical gate recess etch in deep-submicron devices. Hence, the influence of chamber pressure on etch selectivity was characterized. Though the etch selectivity decreased with decreasing chamber pressure, a good selectivity of 37 was obtained even at a 5mT pressure. Based on the above observations, a 1.5 nm Al₂O₃ layer was used as an etch-stop in an N-polar GaN MIS-HEMT, to characterize its influence on the device properties. The device was grown by MOCVD on a sapphire substrate and was processed using standard techniques, except for the inclusion of the etch-stop layer. The gate recess was over-etched by 20%, using CF₄/O₂ plasma, to completely etch the PECVD Si_xN_y under the gate. Next, the Al₂O₃ under the gate region was removed by a wet etch, using AZ-726-MIF developer, followed by Ni/Au/Ni gate deposition. The Al₂O₃ etch-stop layer did not cause any noticeable degradation in device properties. The reverse gate to drain leakage was less than 1µA/mm up to a drain bias of -40V, suggesting that no additional leakage paths were created. Pulsed I-V measurements showed no current collapse, indicating good dispersion control in the device. RF power measurements to further validate the etch-stop technology are under progress. In summary, the presented selective etch technology greatly improved the reproducibility of gate recess, without degrading the device properties. This technology would also be valuable for devices employing high-K dielectrics such as Al₂O₃ and HfO₂ for the gate insulator, with Si_xN_y passivation.

9:00 AM Student

Q3, MBE Regrown Ohmic Contacts with Rc of 0.15 ohm-mm in InAlN/GaN High Electron Mobility Transistor: Jia Guo¹; Jai Verma¹; Yu Cao¹; Xiang Gao²; Shiping Guo²; Ed Beam³; Andrew Ketterson³; Michael Schuette³; Paul Saunier³; Mark Wistey¹; Debdeep Jena¹; Huili (Grace) Xing¹; ¹University of Notre Dame; ²IQE RF LLC; ³Triquint Semiconductor

GaN-based high electron mobility transistors (HEMTs) have been adopted as power amplifiers in the wireless communication base stations and switches in power conditioning applications. To further improve the device performance and reliability, e.g. operating at higher frequencies and higher efficiency, it is highly desirable to minimize parasitics. Among all parasitics ohmic contact resistance is an important one to minimize since that in GaN-based HEMTs, due to its large bandgap, is generally 3-5 X higher than that in InGaAs-based HEMTs. Numerous approaches, including ion implantation, ohmic regrowth, recessed ohmics and plasma pre-treatment, have been studied with various degrees of success on GaN based HEMTs. In this work, we report our results on ohmic regrowth on metal face lattice matched InAlN/GaN HEMTs heterostructures. A total contact resistance of 0.15 ohm-mm was obtained, which is the lowest reported to date on InAlN/AlN/GaN HEMTs. Temperature dependent measurements indicate that there is a minimal barrier (< 74 ueV) existing between the regrown n++GaN and the 2-dimensional electron gas (2DEG) channel. The InAlN/GaN sample used in this work was grown by metal-organic chemical vapour deposition (MOCVD) on SiC substrate at IQE RF LLC. It consists of 5.2 nm InAlN barrier with 1 nm AlN on top of semi-insulating GaN. SiN mask was first deposited using plasma-enhanced chemical vapour deposition (PECVD) and then patterned by reactive ion etching (RIE). With the patterned SiN as mask InAlN/AlN/GaN was etched down for 50 nm in the ohmic region. Heavily doped GaN:Si of 100 nm was then grown on top of the patterned sample by molecular beam epitaxy (MBE) using the conditions described by Yu Cao. Polycrystalline GaN deposited on top of SiN mask during regrowth was lifted off by HF. Ohmic contacts were formed by deposition of Ti/Al based metallization stack and annealed at 800°C. Rc ~ 0.15 ohm.mm was obtained at room temperature from transmission line method (TLM) measurement and TLM gaps were measured by a scanning electron microscope (SEM). It was found that Rc remained almost constant to 77 K and then increased to ~ 0.24 ohm.mm at 4 K, accompanied by monotonic decrease of sheet resistance from 474 ohm/sq. at room temperature to 243 ohm/sq. at 4 K. This small contact resistance observed over a large temperature window, particularly at cryogenic temperatures, indicates that a minimal barrier for electron flow was introduced at the regrowth interface. High resolution transmission electron microscope (TEM) images also confirmed that the regrown GaN is in an intimate contact with the HEMT channel. This study coupled with variations of process and regrowth conditions thus allows us to further optimize these regrown contacts.

9:20 AM

Q4, Pre- and Post-Treatment Investigations of Al Oxide by Atomic Layer Deposition in Schottky Metal/Al Oxide/AlGaIn/GaN MOS Diodes: Hyeonnam Kim¹; Wu Lu¹; ¹The Ohio State University

GaN-based heterostructures are one of the most promising materials for power switching devices that can contribute to energy saving and can be used as smart power grid interfaces for solar, wind and other renewable energy generations, and traction drives in electric or hybrid electric vehicles. For simplicity and reduction of power loss, normally-off devices are usually required in power switching circuits. Recently, enhancement-mode AlGaIn/GaN field-effect transistors (FETs) by thinning AlGaIn barrier have been reported. However, it is challenge to achieve simultaneously both positive threshold voltage and higher turn-on voltage for higher power capability with lower power loss. Thus, introduction of gate dielectrics between Schottky metal and the thin AlGaIn barrier is inevitable for higher breakdown voltage and higher current capability required for power switching devices. In this work, Al oxide formed by atomic layer deposition (ALD) is used because of its large dielectric constant, large bandgap, and high breakdown field. For a 15-nm thick ALD Al oxide, the results show that the reverse leakage current density (J_{REV}) of Ni/as-deposited ALD-Al oxide/AlGaIn/GaN MOS diodes is lower by up to one order of magnitude than

Ni/AlGaIn/GaN Schottky diodes. However, the MOS-diodes with as-deposited ALD-Al oxide exhibit even higher current at a low reverse and forward bias (-3 V to 1 V), suggesting that there is probably an unintentional current path along the oxide films or the Al oxide/AlGaIn interface. To study this, pre- and post-treatments ALD Al oxide are investigated to modify properties of ALD-Al oxide/AlGaIn interface. AlGaIn/GaN samples after ohmic metallization are pre-treated before ALD Al oxide deposition in three different methods: 1) zero bias O_2 plasma oxidation in an inductively-coupled plasma (ICP) system, 2) high-pressure O_2 plasma oxidation in a reactive ion etching (RIE) system, and 3) rapid thermal annealing (RTA) at 550 °C in O_2 ambient. For post-deposition treatments, samples are annealed at different temperatures under O_2 ambient in an RTA system after ohmic metallization and ALD of Al oxide. The results show that all three pre-treatments reduce J_{REV} of GaN-based MOS diodes at -10 V by one to several orders of magnitude and increased turn-on voltage (V_{on}) of the diodes (3 V to 6 V). Post-deposition annealing improves V_{on} if the annealing temperature is below 500 °C, while the reverse current is similar to Schottky diodes. However, significant degradation is observed in both forward and reverse current-voltage characteristics if the annealing temperature is higher than 500 °C. These results suggest that the leakage current path at low biases for untreated ALD Al oxide is at the oxide/AlGaIn interface and this leakage current can be effectively suppressed by a pre-ALD plasma or thermal oxidation process.

9:40 AM

Q5, GaN/Diamond AlGaIn/GaN/AlGaIn DH-HEMT Produced by Epi-Inverted Wafer Processing: Edwin Piner¹; John Roberts²; ¹Texas State University; ²Nitronex Corporation

The performance potential of GaN FETs is substantially limited by device thermal requirements. Diamond is the highest thermal conductivity material, while GaN FETs on Si offer the best pathway for producing highly reliable AlGaIn/GaN HEMTs. A novel technique has been developed to apply the diamond directly on top the AlGaIn/GaN/AlGaIn DH material structure. Two critical aspects of the wafering technique are the III-nitride etch and the interfaces. The III-nitride etch is a multi-step process. The III-nitride nucleation and transition layers, comprised of AlN and AlGaIn, respectively, are etched with an ICP Cl₂-based process. The etch effluent is monitored and when the process has reached the GaN buffer layer, it is manually terminated. The remaining GaN buffer layer is dry-etched with a proprietary process that has an exceptionally high selectivity between GaN and AlGaIn ($> 1,000:1$). The sacrificial handle wafer bonding process is challenged by the roughness of the CVD diamond film. The CVD diamond coated 100 mm GaN-on-Si epiwafer has a matte gray appearance indicative of the very rough surface. The RMS roughness from AFM is 235 nm. This translates to a peak-to-valley height variation of as great as 2.5 μ m. Poly-Si deposition then polishing is used to smooth the diamond surface. The poly-Si coated and polished CVD diamond wafer has a specular, shiny surface. The RMS roughness determined with AFM is 2.8 nm, or a reduction of ~ 84X over the original CVD diamond surface. This surface is adequate for bonding to the sacrificial handle wafer with a variety of processes. The most ideal process is a Si-Si fusion bond. High resolution STEM analysis of the material stack has been used to study the bulk material and interface quality. A key achievement of the program to date is the full-wafer AlGaIn/GaN/AlGaIn HEMT with PECVD SiNx transfer and selective etch. The selective etch control is indicated by the ability of the very thin AlGaIn etch stop layer, ~ 10 monolayers thick, to inhibit the etch process. In this structure, with the CVD diamond included and ready for device fabrication, the 2DEG defining AlGaIn barrier layer is decoupled from where the ohmic and Schottky contacts will reside. Because of this decoupling, there is no longer a necessity to compromise high-speed / high-frequency performance (e.g., through gate recess or epi structure design) and 2DEG characteristics. The material development aspects of this program will be presented along with the latest results from the epi-inverted N-polar GaN DH FET device fabrication and testing.

10:00 AM Break

10:20 AM

Q6, Al_xIn_{1-x}N/GaN Heterostructures Grown by MEMOCVD: *Daniel Billingsley¹; Ajay Sattu¹; Xuhong Hu¹; Jianyu Deng¹; Grigory Simin¹; Max Shatalov¹; Michael Shur¹; Jinwei Yang¹; Remis Gaska¹;* ¹Sensor Electronic Technology

III-Nitrides have become a popular material system for visible and ultraviolet light emitters and for microwave and high power devices mainly due to the success of AlGaIn/GaN heterostructures. Although impressive results have been obtained with these AlGaIn/GaN devices, the device reliability is affected by the inverse-piezoelectric effect. To circumvent this issue, recent work has focused on AlInN alloys which are lattice-matched to GaN to provide the spontaneous polarization component for 2DEG formation while eliminating the piezoelectric component responsible for decreased device reliability. AlInN/GaN heterostructures are promising due to their increased polarization charge and conduction band discontinuity, compared to traditional AlGaIn/GaN heterostructures. In this work, high-quality AlInN/GaN heterostructures were grown by MEMOCVD to investigate the influence of indium incorporation on the electrical properties. Utilizing MEMOCVD allows for improved control of indium incorporation, allowing for increased growth temperatures, which increases adatom surface mobility and improves film quality. The growth temperature and precursor modulation schemes were optimized, resulting in XRD Al_xIn_{1-x}N(0002) rocking curve FWHM ~200 arcsecs. AlInN/GaN heterostructures grown by MEMOCVD exhibited maximum 2DEG sheet charge density of ~4.1x10¹³ cm⁻², maximum 2DEG mobility of ~1270 cm²/Vs and record wafer-level sheet resistance as low as 180 Ω/+. Device structures deposited on these films exhibited record low TLM sheet resistance measurements of 215 Ω/+ with an Rc of 0.27 Ω-mm. DC measurements of HFET structures exhibited drain saturation current of 1.05 A/mm for LSD = 5 μm. Additionally, when SiC substrates were used, the AlInN/GaN devices achieved drain saturation current of 2.1 A/mm for a 2x150x0.08 μm gate periphery. These promising results illustrate the potential of MEMOCVD in producing high-quality AlInN/GaN heterostructures for high power devices.

10:40 AM Student

Q7, Lateral Confinement of Electrons and Quasi-1D Channels Based Devices: *Digbijoy Nath¹; Pil Sung Park¹; Michele Esposto¹; David Brown²; Stacia Keller²; Umesh Mishra²; Siddharth Rajan¹;* ¹The Ohio State University; ²UC Santa Barbara

Devices based on 1D transport such as carbon nanotubes, Si nanowire FETs, etc. are being increasingly investigated as performance of conventional planar MOSFETs and HEMTs are pushed to limits due to aggressive scaling of device dimensions. Fabricating an array of aligned nanowires for useful device applications however presents significant lithographic challenges. In this work, we demonstrate the first non-lithographically defined quasi 1D channels using polarization engineering. Vertical confinement provided by heterostructure engineering and lateral confinement provided by electrostatic polarization engineering lead to 1D confinement of the electrons in these structures. We also propose a simple theory to compare device performance for 1D and 2D regimes and compare the device performance of the fabricated channels to the theoretical prediction. Devices fabricated on MOCVD grown N-polar AlGaIn/GaN HEMT structures on vicinal sapphire substrate (40 miscut towards a-plane) were found to exhibit anisotropy in current and channel pinch-off voltages. Channels parallel to the miscut direction pinched off at lower gate biases and hence carried more 2DEG charge than the perpendicular direction as measured by direction-dependent C-V profiling. An electrostatic model, which predicts a saw-tooth energy band profile in the lateral direction, has been proposed to explain the charge anisotropy. Each atomic terrace, characteristic of the surface morphology of vicinal GaN, with its corresponding saw-tooth energy profile is proposed to exhibit quasi 1D confinement. Extending the above idea, we obtained pure anisotropy without a gate, using controlled recess etching of the GaN channel. The intrinsic 2DEG density was gradually reduced in both directions by etching the channels in small steps of channel-recess. At a critical etch depth, drain current ID (up to 150 mA/mm) is found to flow in

the parallel direction, while no current flows perpendicular to the steps. This indicates the formation of quasi-1D channels along the steps. Using C-V, we investigated the charge-dependent current properties of the channels. We found that for the same charge density, quasi-1D channels carried more current than 2D channels. We believe this may be attributed to the fundamental transport properties of 1D channels. To verify, we developed a simple theory based on optical phonon scattering that anticipates our experimental results. We will discuss the consequences of these differences in electron transport between 1D and 2D channels for device performance.

11:00 AM

Q8, Polarization-Engineered GaN-Based Heterostructure for Normally-off High-Electron Mobility Transistors: *Hyeonnam Kim¹; Digbijoy Nath¹; Siddharth Rajan¹; Wu Lu¹;* ¹The Ohio State University

GaN-based heterostructures have been considered to be promising materials for high power switching applications as well as high power microwave applications. In particular, high breakdown voltage and high speed characteristics of GaN-based high-electron mobility transistors (HEMTs) allow us to reduce on-state loss and switching loss in power electronic applications. However, normally-off GaN-based HEMTs are required for simplification of conventional power electronic circuits while conventional GaN-based HEMTs are normally-on. Therefore, novel heterostructures and gate recess processes have been extensively investigated for realization of normally-off channel in III-nitride heterostructures. In this work, we report a new GaN-based heterostructure with GaN cap layer and AlGaIn/p-GaN back barrier for normally-off channel, and also present fabrication procedure and electrical characterization results of enhancement mode GaN based HEMTs using the proposed heterostructures. Our device design eliminates the need for a gate recess etch, making the device processing more repeatable and reliable. The layer structure consisting of GaN 40 nm GaN cap, 5 nm Al_{0.3}GaN_{0.7}N, 100nm GaN, 5 nm Al_{0.2}Ga_{0.8}N, p-GaN, and GaN layers were grown on GaN template by molecular beam epitaxy. The GaN cap layer depletes 2-dimensional electron gas (2DEG) at Al_{0.3}GaN_{0.7}N/GaN interface, and Al_{0.2}Ga_{0.8}N and p-GaN layers act as a back barrier and deplete 2DEG. The simulation results show that the structures essentially have no 2DEG but removal of GaN cap layer induces 2DEG of 3.9x 10¹² cm⁻² when the hole carrier density in p-GaN with a thickness of 110 nm is 2x 10¹⁸ cm⁻³. This is confirmed in ohmic-to-ohmic test structures that GaN cap removal by selective etching against AlGaIn barrier creates 2DEG as shown in the simulation result. Circular fat field-effect transistors (FETs) are fabricated by mesa-isolation, ohmic metallization, gate metallization, and selective dry etching with Cl₂/O₂/N₂ at zero DC bias by using ohmic and Schottky contacts as etch masks. The selective dry etching is a self-aligned process which doesn't need an additional lithographic step. A circular GaN-based FET with a gate length of 80 μm and gate width of 628 μm, exhibits a positive threshold voltage of ~0.2 V and transconductance of 2.6 mS/mm at a fixed drain voltage of 5 V. In addition, unlike a gate recess process required for channel-off, our fabrication process with the new heterostructures does not induce any damage under the gate which could degrade switching speed. In summary, we demonstrated a normally-off GaN-based FET with a new heterostructure engineered by polarization. This heterostructures and device fabrication process enable normally-off operation of GaN FETs with a plasma damage-free channel for power switching applications. The absence of gate recess etching is promising for uniform and repeatable threshold voltage control in normally of AlGaIn/GaN HEMTs.

11:20 AM

Q9, Tunneling Current via Dislocations in AlGaIn/GaN Schottky Contacts: *Peter Kordos¹; Jaroslav Kovac¹; Roman Sramaty¹; Jaroslava Skriniarova¹; Alexander Satka¹; Ales Chvala¹; Daniel Donoval¹;* ¹Department of Microelectronics

We present a study of the gate current in the Ni/AlGaIn/GaN Schottky contacts by temperature dependent measurement of I-V characteristics and their analysis considering various transport mechanisms. Commercial AlGaIn/GaN/SiC structure and conventional device processing with Ti/Al/Ni/Au ohmic and Ni/Au Schottky contacts were used. The gate characteristics

were measured at temperatures between 150 and 550 K. The main results obtained can be summarized as follows: (i) The forward gate current vs voltage characteristics measured at different temperatures were successfully fitted considering thermionic emission, generation-recombination, and tunneling and leakage currents (fitting error <20%). These can be divided, in general, into three distinguish regions concerning the current transport mechanism. (ii) It is found that the thermionic emission dominates only at higher biases and thus it is not coincident with the measured I-V characteristic as commonly supposed. This is the reason of incorrectly evaluated low barrier heights and their increase with temperature (e.g. 0.16 eV at 80 K and 0.86 eV at 410 K [1], or 0.81 eV at 300 K and 1.27 eV at 475 K [2]). From our analysis it follows that the barrier height at room temperature is 1.36-1.39 eV with slightly negative temperature coefficient. (iii) Tunneling current dominates in the main part of I-V characteristics at all used temperatures. This can be explained by consideration that the current is caused by tunneling through dislocations in the space charge region. The saturation tunneling current can be described as $I_{TU,s(0K)} = q \cdot v_D \cdot N_{dis} \cdot \exp(\phi_B/E_{TU})$ [3]. The dislocation density $N_{dis} = (3-5) \times 10^8 \text{ cm}^{-2}$ was evaluated using experimental $I_{TU,s} = f(T)$ dependence. This reliable N_{dis} value confirms our assumption that high number of dislocations affects significantly the current flow through the gate contact in AlGaIn/GaN structures. (iv) At low biases the leakage current dominates, as expected. However, this current depends on the structure used. It is shown that the gate current of the mesa-type device is higher than that of the planar devices and this additional current shows ohmic behavior. Mapping by EBIC yielded enhanced current located on the mesa-sidewall where the gate contact is placed. Two-dimensional simulation of the device structure confirms this observation and shows that the additional gate leakage current is originated by a current path through the mesa sidewall.

11:40 AM Student

Q10, Growth Studies on Quaternary AlInGaN Layers for HEMT Application: Benjamin Reuters¹; ¹RWTH Aachen University

Quaternary barrier layers for GaN-based high electron mobility transistors (HEMT) have recently reached the focus of interest because of the possible lattice-matched growth to GaN. This results in a reduction of strain-related defects, while having the option of adjusting the bandgap separately. The benefit to achieve high polarisation and high mobility simultaneously is promising to improve the performance of such devices. In this work, we report on the growth and characterisation of $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}/\text{GaN}/\text{AlN}$ structures deposited on 2-inch sapphire substrates in AIXTRON MOCVD reactors. The growth was initiated with a 300 nm thick AlN layer, followed by a 3 μm thick 90% relaxed GaN buffer. $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layers within the range of 16-50% Al, 2-3% In and 48-82% Ga were deposited at a surface temperature of 805°C. From high-resolution XRD reciprocal space mappings (RSM) (20-24) and (0004), we determined the nominal lattice parameter and the strain by regarding Vegard's law and the Poisson ratio. Additionally, the composition was estimated by wavelength-dispersive X-ray spectroscopy (WDX). The bandgaps (E_g) were obtained by spectroscopic ellipsometry. On thin HEMT samples, Hall and Van der Pauw measurements were performed to collect electrical data. The composition was changed by reducing the TMAI/TEGa ratio from 2.0 to 0.3 while keeping the TMIn flow constant. Whereas the In concentration remains stable at 2-3%, the Al content decreases (Ga content increases) for lower TMAI/TEGa gas phase ratio. An almost linear correlation between the TMAI/TEGa gas phase ratio and the Al/Ga content ratio can be observed. The bandgaps (E_g) were found to decrease from 4.56 eV to 3.74 eV with decreasing TMAI/TEGa ratio and hence a lower Al content. The layers exhibit high tensile in-plane strain ($\epsilon_{xx} = 0.64\%$) to almost no strain ($\epsilon_{xx} = 0.03\%$), with better crystal quality in less strained samples. XRD (10-15) rocking curves yielded excellent FWHM values down to 316 arcsec, due to reduced strain-related defects. For the sample with the highest strain, a shift and broadening of the (10-15) HRXRD reciprocal lattice point are observed, which indicates partial relaxation of the 116 nm thick layer. Samples with lower Al content show pseudomorphic growth also up to a thickness of 153 nm, due to less strain. By reason of the lowered Al content, the spontaneous and piezoelectric polarisation in AlInGaIn/GaN HEMT structures is reduced. In addition the

conduction band offset is reduced due to a smaller bandgap. HEMT with about 20 nm thin AlInGaIn barrier layers yielded average two-dimensional carrier densities in the range of $1.00\text{-}2.21 \cdot 10^{13} \text{ cm}^{-2}$, systematically decreasing with lower Al content. Mobilities increase up to $1761 \text{ cm}^2/\text{Vs}$ at room temperature and $6060 \text{ cm}^2/\text{Vs}$ at 77 K, revealing high interface quality. The results show the potential of adjusting electrical parameters in quaternary HEMT.

Session R: Narrow Bandgap Materials and Devices

Thursday AM
June 23, 2011

Room: Lobero
Location: Univ. of California-Santa Barbara

Session Chairs: Ganesh Balakrishnan, University of New Mexico; L. Ralph Dawson, University of New Mexico

8:20 AM Student

R1, Improved Performance of Long-Wave Infrared InAs/GaSb Strained Layer Superlattices Detectors by Novel ZnTe Passivation: Maya Narayanan Kutty¹; Elena Plis¹; Svyatoslav Smolev¹; Nutan Gautam¹; Mikhail Naydenkov¹; Stephen Myers¹; Ralph Dawson¹; Weiming Wang²; Jamie Phillips²; Sanjay Krishna¹; ¹University of New Mexico; ²The University of Michigan

Present-day fabrication of SLS based detectors involves termination of periodic crystal structure while performing individual pixel isolation (Mesa structures). Amid this process, unsatisfied (dangling) chemical bonds are formed on the exposed sidewalls responsible for generation of surface states within the bandgap and enhanced leakage currents. In order to overcome the limitation imposed by surface leakage currents, a stable surface passivation layer is needed. However, passivation treatment applied on rough surfaces, or surfaces contaminated by native oxides or foreign particles will result in little or no improvement of device performance. Definition of mesa sidewalls that are free of native oxide and defects is the crucial step in InAs/GaSb SLS FPA fabrication process. We have previously found that the smoothest sidewall profile of large-area ($400\mu\text{m} \times 400\mu\text{m}$) LWIR ($\lambda_{50\%}$ cut-off $\sim 14\mu\text{m}$) InAs/GaSb SLS detectors was obtained after chemical HCl-based etch ($\text{H}_2\text{O}_2 : \text{HCl} : \text{H}_2\text{O} = 1 : 1 : 4$) while the plasma-assisted etch performed on the same material, generated a lot of damage, in particular, etch residues and two-step sidewall profile was observed. However, the same chemical etch utilized for the isolation of $24\mu\text{m} \times 24\mu\text{m}$ mesas (the FPA pixels) resulted in significant lateral etch ($\sim 9\mu\text{m}$ each side) and rough sidewall. Plasma-assisted (ICP) etch resulted in smooth vertical sidewalls of individual FPA pixels free from any etch residuals with no undercut (with respect to mask) observed as well as clean FPA grooves. However, it's known that plasma-assisted etch produces inevitable degradation of sidewall surface electronic properties due to ion bombardment or unwanted deposition of etch by-products. We tried to partially restore damage produced during the dry etch may be subsequent chemical treatment with HCl-based etch. The application of chemical etch subsequent to the plasma-assisted etch resulted in undercut estimated to $\sim 8\mu\text{m}$ on each side of FPA mesa. Thus, the final size of defined mesa is only $8\mu\text{m} \times 8\mu\text{m}$, which is not acceptable for the subsequent FPA fabrication steps. To compensate the surface damage induced by ICP etch and further reduce the surface leakage currents, passivation needs to be applied on the etched sidewalls. Chalcogenide passivation such as ZnS or ZnTe successfully saturates dangling bonds and reduces the possibility of native oxide (such as Ga_2O_3 , Sb_2O_3) formation. We found that quality of ZnS is poor, probably, due to the deposition process (e-beam dielectric evaporation). We developed ZnTe passivation as an alternative to the ZnS, and we expect to achieve the better passivation quality since ZnTe is deposited through the molecular-beam epitaxy (MBE) technique. During the presentation the etch study results for InAs/GaSb LWIR SLS FPAs will be presented along with the novel ZnTe passivation device results.

8:40 AM

R2, Strain-Engineered Binary and Ternary Type-II Superlattice Structures and Photodiodes Grown by Metalorganic Chemical Vapor Deposition: Yong Huang¹; *Jae-Hyun Ryou*¹; Russell Dupuis¹; Elizabeth Steenbergen²; Jin Fan²; Yong-Hang Zhang²; Daniel Zuo³; Ben Kesler³; Adam Petschke³; Martin Mandl³; Shun-Lien Chuang³; Hefei Hu³; Kyohyun Kim³; Yen-Ting Lu³; Jian-Min Zuo³; ¹Georgia Institute of Technology; ²Arizona State University; ³University of Illinois at Urbana-Champaign

Type-II superlattice (T2SL) structures containing III-Sb alloys have been exploited as photodetectors operating in a wide range of the infrared (IR) spectral region covering from mid-IR to very-long-wavelength-IR. Although there are several approaches to T2SL photodetector design, recent research efforts have been focused on InAs/GaSb strained T2SL on GaSb substrates employing InSb-like interfacial (IF) layers grown by molecular beam epitaxy (MBE). Such an InSb-like IF layer used in MBE for strain balancing cannot be easily adopted in metalorganic chemical vapor deposition (MOCVD). In order to develop T2SL-based photodetectors grown by MOCVD, new approaches for strain balancing in T2SLs structures are required. In this study, we report on the characterization of several T2SL epitaxial structures with a focus on strain balancing. The structures include: (1) InAs/GaSb SLs on GaSb with various IF layers; (2) InAs/InAs_{1-x}Sb_x SLs on GaSb; and (3) InAs/GaSb SLs on InAs. During growth of the InAs/GaSb SLs by MOCVD, the gas switching sequence and IF layer control are of critical importance. InAsSb and InGaSb IF layers are introduced to compensate the tensile strain and hence to improve the overall material quality of the SL structures. As suggested by the X-ray diffraction (XRD) and atomic force microscopy (AFM) results, the optimal morphology and lowest strain are achieved via a combined IF layer scheme with 1 monolayer (ML) InAsSb + 1 ML InGaSb layers. RMS (root-mean square) surface roughness is ~0.172 nm and the separation between the SL 0th-order peak and the substrate is ~448 arcsec., corresponding to an in-plane lattice mismatch of ~0.17%. In the case of InAs/InAs_{1-x}Sb_x SLs on GaSb, the strain-balancing can be achieved by employing a ternary layer and simple precursor flow switching scheme. Excellent surface morphology with a RMS surface roughness value as low as ~0.108 nm is obtained. XRD ω -2 θ scans exhibit narrow and intense satellite peaks, indicating superior structural quality and sharp interfaces. The average in-plane strains are only ~0.07 % and ~0.02 %, which indicate that the SLs are nearly strain-balanced. In addition, as shown in a comparative study of experimental and simulation XRD curves, under certain growth conditions, the InAs/GaSb SLs can be grown without any intentional IF layer, and data suggest the existence of an additional tensile-strained layer, which is believed to be a 1-ML-thick GaAs. While this additional layer is detrimental in strain balancing on GaSb substrates, it is beneficial on InAs substrates. The strain engineering of InAs/GaSb SLs on InAs is under further investigation and the latest results will be reported. In summary, the structural and optical properties of various MOCVD-grown T2SLs are studied and *p-i-n* photodiodes employing these T2SLs and T2SL photodetectors are demonstrated and described.

9:00 AM Student

R3, Study of Minority Carrier Lifetime and Background Carrier Concentration in GaSb-InAs Strained-Layer Superlattices and Bulk Epitaxial Layers by Optical Modulation Response: *Ding Wang*¹; Dmitri Donetsky¹; Stefan Svensson²; Sergei Suchalkin¹; Gregory Belenky¹; Amy Liu³; Joel Fastenau³; Dmitri Lubyshev³; ¹Stony Brook University; ²US Army Research Laboratory; ³IQE, Inc

Shockley-Read-Hall (SRH), radiative and Auger recombination processes in n- and p-type GaSb-InAs Strained Layer Superlattices (SLS) are compared to those in bulk materials. The carrier lifetime values up to 32 ns in long-wave infrared (LWIR) SLS and 75 ns in mid-wave infrared (MWIR) SLS at T=77 K were measured by the optical modulation response technique from the dependences of the minority carrier lifetimes on excess carrier concentration. The background carrier concentration was determined from the dependences of PL intensity and carrier lifetime on excitation. The radiative recombination coefficients for the MWIR SLS materials were calculated using the measured fundamental absorption spectra and the lateral and vertical effective masses.

The latter were obtained from cyclotron resonance measurements in the Faraday and Voigt configurations. Haugan et al. have earlier demonstrated that MWIR SLS structures can be designed with a variety of cell periods, while maintaining the same energy gap [1]. Following this procedure we grew a set of samples with primitive cell periods ranging from 2.08 nm to 5 nm without any interface engineering. The total thickness was 2 micron and the number of periods was varied ~2.5 times in the set. No scaling up of the carrier lifetime with SLS period was observed. Reducing the strain did not lead to improvement in lifetime. Doubling of the interface density did not increase the rate of recombination suggesting that interfaces are not location of the carrier recombination centers but the binary layers are. Since holes are highly localized, GaSb is the likely place where carrier recombination occurs. The tendency of carrier lifetime improvement was observed with decrease of the relative volume of GaSb in the SLS structure. Experimental data confirmed that in LWIR GaSb-InAs SLS materials with the background doping concentration level of 10¹⁶ cm⁻³ the carrier lifetime is defined by the SRH processes rather than Auger recombination. A low photon state density justified the minor role of the radiative recombination. A rapid change of the carrier lifetime with excess carrier concentration in low doped LWIR SLS materials versus relatively slow change in moderately doped structures indicated the important role of population of the acceptor-like mid-gap states in the SRH processes. The carrier lifetime in undoped epitaxial layers of GaSb at T=77 K was found to be increasing by a factor of 3 with increase of the growth temperature from 440 C to 510 C while the carrier lifetime in InAs did not degrade over the same temperature range. The phenomenon is explained with decrease of the defect concentration.

9:20 AM Student

R4, Increased Thermophotovoltaic Efficiencies Using a Two Dimensional Photonic Crystal Cavity: *Corey Shemelya*¹; Dante Demeo¹; Thomas Vandervelde¹; ¹Tufts University

We investigate the enhancements provided by a two dimensional hexagonal photonic crystal pattern and a back reflection layer on a gallium antimonide thermophotovoltaic cell. The photonic crystal pattern and back reflecting layers have been shown to increase the optical intensity within the active diode region, to increase the photon/exciton interaction time, and to decrease the number of recombination events. The end result is a TPV cell with a greater overall conversion efficiency, as well as, a larger external quantum efficiency and internal quantum efficiency. Thermophotovoltaic generators have traditionally been a three stage devices (emitter, filter, diode) which converts heat incident on the emitter (infrared photons) into a current out of the TPV cell. Present research in TPV devices demonstrate maximum conversion efficiencies of only around 20%. However, theory predictions that total system efficiencies of 30-40% can be reached. Our focus is on increasing the efficiency of the Gallium Antimonide (GaSb) TPV cell, a PN-photodiode through the use of a two dimensional photonic crystal cavity. A photonic crystal (PhC) is a periodic array of dielectric rods embedded in a different dielectric material. The periodic nature of a photonic crystal creates a photonic band diagram, and at specific wavelengths of light, a standing wave is generated within the PhC. The dimensions and geometries of a PhC can be changed in order to determine at which wavelength the standing wave occurs resulting in significant tunability. The resulting standing wave slowly leaks into the surrounding material, and has been found to increase detectivity in photodetectors. A photonic crystal cavity was first designed and optimized in Lumerical FDTD to create a PhC standing wave corresponding to the bandgap of GaSb. It was determined that the addition of both a back reflection layer and photonic crystal cavity increased the optical intensity within the active region of the TPV cell by 16% as well as increasing the photon/exciton interaction time by 223%. The PhC cavity was constructed in an ohmic contact to GaSb resulting in a decreased travel time for excitons and therefore a decreased number of potential recombination events. We also predict an increase in conversion efficiency from the low energy "filtering effect" of the PhC resulting in a much more effective TPV diode stage.

9:40 AM

R5, Effect of Dislocation Density on Thermal Boundary Conductance across GaSb/GaAs Interfaces: *Patrick Hopkins*¹; John Duda¹; Leslie Phinney¹; Stephen Clark²; Christopher Hains²; Thomas Rotter²; Ganesh Balakrishnan²; ¹Sandia National Laboratories; ²University of New Mexico

Thermal transport across solid interfaces, which is a major inhibitor of heat flow in nanosystems, is quantified by the thermal boundary conductance, h . A greater understanding of h at III-V interfaces can lead to mitigation and control of heat transfer in optoelectronic structures, thereby furthering device engineering and development. In this work, we measure h across GaSb/GaAs interfaces with time-domain thermoreflectance (TDTR). We grow GaSb films on GaAs substrates via two different epitaxial techniques leading to different dislocation densities around the GaSb/GaAs boundary. In addition, these different growth techniques cause the dislocation densities of the GaSb films to vary, thus changing the surface morphology of the films. Therefore, we also study the effect of dislocation density and interface roughness on h at Al/GaSb interfaces, as a thin 100 nm Al film is deposited on the GaSb surface for TDTR measurements. Our measurements indicate that dislocations around the GaSb interface cause a large reduction in h . We quantify the phonon scattering with a variation of the diffuse mismatch model (DMM) in which phonon propagation and scattering parallels photon attenuation. Our model fits the measured data well, and the resulting phonon attenuation coefficients are independent of dislocation density. This indicates that attenuating phonon scattering events around GaSb interfaces are intrinsic to the materials comprising the interface. These thermal results have implications for the design, growth, and selection of materials in laser diodes and other gallium-based optoelectronics. P.E.H. is appreciative for funding from the LDRD program office through the Sandia National Laboratories Harry S. Truman Fellowship Program. J.C.D. is appreciative for funding from the National Science Foundation Graduate Research Fellowship Program and the Student Intern Program at Sandia National Laboratories. Sandia is a multiprogram laboratory operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the United States Department of Energy's National Nuclear Security Administration under Contract DE-AC04-94AL85000.

10:00 AM Break

10:20 AM Student

R6, Low Field Electron Transport in Mixed Arsenide Antimonide Quantum-Well Heterostructures: *Ashish Agrawal*¹; Ashkar Ali¹; Rajiv Misra¹; Peter Schiffer¹; Brad Boos²; Brian Bennett²; Suman Datta¹; ¹The Pennsylvania State University; ²Naval Research Lab

Antimonide based compound semiconductors have gained considerable interest in recent years due to their superior electron and hole transport properties [1]. Mixed anion $\text{InAs}_y\text{Sb}_{1-y}$ quantum wells (QW) with high electron mobility are excellent candidates for direct integration with high hole mobility $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ QW for ultra-low power complementary logic applications [2]. Quantum well FET structure consists of $\text{InAs}_{0.8}\text{Sb}_{0.2}$ as channel material, $\text{In}_{0.2}\text{Al}_{0.8}\text{Sb}$ barrier layer and an ultra-thin GaSb surface layer for avoiding surface oxidation of Al in the barrier. Energy band diagram of the QW structure has been studied with the composite Al_2O_3 -GaSb gate stack using Schrodinger-Poisson simulation, which indicates strong electron confinement in the QW. In this paper, we study the low field transport properties of electrons in the high mobility InAsSb quantum well. Hall measurements were performed on the device layers by varying the temperature from 4K-300K. We extract the dominant scattering mechanisms that are responsible for limiting the mobility at low and high temperatures. The relaxation time approximation (RTA) applied to the Boltzmann transport equation (BTE) is the theoretical framework employed to estimate the scattering rates. The scattering of the electrons confined in the quantum-well consists of a variety of mechanisms having unique temperature dependences which explain the overall mobility characteristics of the fabricated heterostructure. The inverse of the total relaxation time, t_{tot}^{-1} , can be calculated from the sum of the scattering rates for the individual scattering processes. There are six scattering mechanisms limiting the electron mobility: acoustic deformation potential scattering, polar

optical phonon scattering, remote ionized impurity scattering, alloy disorder scattering, interface roughness scattering, and coulomb scattering due to charge trapped at the barrier and channel interface (Tamm States) [3]. Study of subband occupation indicates that the significant contribution of carriers from the second subband near room temperature mandates the inclusion of both intersubband and intrasubband scattering. The rates are finally derived using the Fermi's golden rule. Hall mobility of InAsSb quantum well has been modeled using above mentioned scattering mechanisms, showing excellent agreement with the experimental results. Study of Quantitative Mobility Spectrum Analysis (QMSA) of carriers at 77K, 200K and 300K has been performed. The higher conductivity peak corresponds to the InAsSb QW, indicating the absence of parallel conduction channel. In conclusion, high electron Hall mobility of 13,300 cm^2/Vs is achieved on the fabricated InAsSb QW FET device. Excellent agreement between experimental and modeled results for a wide range of temperature has been achieved.

10:40 AM Student

R7, AlGaSb/InAs-Based Staggered Heterojunction Tunnel Diodes: *Siyuan Gu*¹; Gerry Sullivan²; Lingquan Wang³; Peter Asbeck⁴; ¹UC San Diego; ²Teledyne Scientific Company; ³Global Foundries; ⁴University of California San Diego

To solve the crucial power dissipation issue at the end of the conventional CMOS roadmap, there has been intense interest in tunneling field-effect transistors (TFETs), which are expected to offer superior subthreshold slope and high current drivability. The material system based on AlGaSb/InAs and related compounds is promising for the implementation of TFETs, since it can provide a staggered heterojunction band lineup, with a controllable, small energy gap E_{cv} between the valence band of the AlGaSb and the conduction band of InGaAs or InAlAs, which can enhance the junction tunneling probability. In this work we have fabricated and studied tunnel diodes in this material system, in order to allow device characterization with 2 terminal structures rather than the more complex FETs. We designed heterostructures with different compositions, which provide a set of band alignment values (heterojunction band-gaps E_{cv}) of 0.1eV and 0.2eV by adjusting mol-fractions in the III-V compounds. The carrier injector was AlGaSb, while the carrier collector (channel material in the corresponding FET) was InAlAs. Compositions were selected to maintain small lattice mismatch to allow high quality pseudomorphic growth. The AlGaSb/InAlAs heterojunctions were grown on InAs substrates by molecular beam epitaxy. The MBE growth used Si as the dopant species for n InAlAs and Be for p AlGaSb and p+ GaSb cap layers. AFM measurements showed RMS roughness smaller than 0.20nm. The carrier injector, AlGaSb was found to be chemically stable in air for weeks, even as its Aluminum mol-fraction approached 60%. Tunnel diodes in mesa-shape were fabricated by citric chemistry and Ohmic contacts formation, followed by Benzocyclobutene sidewall coverage. Four-probe Kelvin I-V characterization proved that the currents in both forward and reverse bias scale with the mesa area, which suggested no leakage current from the sidewall. The reverse and forward bias characteristics are believed to be dominated by tunneling of carriers and recombination of carriers respectively through Synopsis Setaurus modeling. Both samples exhibited I-V slopes in reverse bias almost invariant with temperature (over the range 150K to 400K), which is a significant sign of tunneling behavior. For the sample with the 0.1eV heterojunction band-gap, the reverse biased I-V slope was sharper than kT/q at 400K (as needed for applications). By extrapolation from the measurements, we estimate the tunneling diodes could reach current density of $10^6\text{A}/\text{cm}^2$ at a low bias of 0.4V, without considering series resistance. This makes the system promising for achieving a 0.5mA/um on-current in future III-V tunneling MOSFETs. The sample with 0.1eV heterojunction band-gap showed higher current in forward bias than the 0.2eV sample, due to rapid recombination of carriers at the AlGaSb/InAlAs heterojunction. This implies that in tunneling MOSFETs design, generation-recombination leakage must be controlled while pursuing high tunneling current with small heterojunction band-gap.

11:00 AM Student

R8, Growth and Characterization of AllInSb Metamorphic Buffers on GaSb and GaAs Substrates for the Growth of MWIR Lasers: *Stephen Clark*¹; *P. Ahlwar*¹; *V. Patel*¹; *S. Reissmann*¹; *T. Rotter*¹; *A. Albrecht*¹; *H. Xu*¹; *C. Hains*¹; *L. Dawson*¹; *Y. Picard*²; *G. Balakrishnan*¹; ¹CHTM; ²Carnegie Mellon University

The applications of MWIR lasers include remote sensing, LADAR, trace gas sensing, intelligence, surveillance and reconnaissance (ISR) and infrared countermeasures (IRCM). Though MWIR lasers have been developed using lead (Pb) salts, and II-VI compound semiconductors, the most promising technological advances have been achieved using III-V compound semiconductor materials lattice matched to GaSb substrates. With the use these substrates, room temperature (RT) and near-room temperature operation of laser diodes has been achieved at wavelengths $> 3.0 \mu\text{m}$. Groups have tried various active regions to achieve operation at the desired wavelength range of $3 \mu\text{m}$ to $4 \mu\text{m}$ including Type I, Type II, inter-cascade, and quantum cascade. While Type I based InAsSb QW devices have been shown to operate in this range, when pumped optically, miscibility-gap issues severely affect device performance and restrict the emission wavelength to less than $3.8 \mu\text{m}$ (at 77 K). Conversely, recent advances in Type II 'W', quantum-cascade and inter-cascade laser technology have resulted in $>100 \text{ mW}$ CW output power at room temperature throughout the spectral range of interest. The use of antimonide metamorphic buffers has shown promise in extending the wavelength range of antimonide type-I lasers. The most successful instance of such a laser was by Lester et al. where AllInSb metamorphic buffers were used to achieve greater than $3.3 \mu\text{m}$ room temperature lasing under pulsed conditions. In this abstract we present the growth and characterization of AllInSb metamorphic buffers grown on GaSb and GaAs substrates to establish a lattice constant in the 6.13 to 6.2 \AA range that can then be used for the growth of $>3.5 \mu\text{m}$ type-I active regions. We shall grow the buffers in the form of single step buffers (directly from GaSb to the final lattice constant) and step graded buffers. We shall also explore the growth of these buffers through the use of a digital alloy technique. A large parameter space of III:V ratios, substrate temperatures and growth rates will be used in development of these buffers. These buffers will be characterized using a variety of techniques including X-ray diffraction, atomic force microscopy (AFM), cross-section transmission electron microscopy (XTEM) and Electron Channeling Contrast Imaging (ECCI). We shall also make use of InGaSb quantum well structures to analyze the suitability of the material for laser growth.

11:20 AM

R9, Optimization of MBE Growth for the Development of Mid-IR II-VI Quantum Cascade Lasers: *Richard Moug*¹; *Humara Sultana*¹; *Yu Yao*²; *Adrian Alfaro-Mantinez*¹; *Le Peng*¹; *Thor Garcia*¹; *Aidong Shen*¹; *Claire Gmachl*²; *Maria Tamargo*²; ¹City College New York; ²Princeton University

Quantum cascade (QC) lasers operating in the mid-IR are being intensely pursued for environmental sensing and other important technological applications. Having demonstrated mid-IR electroluminescence (EL) from a II-VI intersubband device based on ZnCdMgSe on InP, a drive has been undertaken to produce a QC laser from these materials. To achieve lasing, waveguiding layers that straddle the active region used in the EL structure must be included. This addition dramatically increases the total thickness of the structure and has required some modifications to the MBE growth procedure. All of our samples are grown in a dual chamber Riber 2300 MBE system. InP substrates are used and the oxide is removed by the standard procedure. An InGaAs buffer layer 15 nm thick is grown prior to transfer to the II-VI chamber. Once in the II-VI chamber a (LT) low temperature (170°C) ZnCdSe layer is grown to improve the III-V/II-VI interface prior to growth of the II-VI structure at 270°C . Initial attempts to grow of a full QC laser structure revealed several materials problems: 1. The RHEED would develop unusual features and over time become spotty, indicative of 3D growth. 2. The surface after growth exhibited a marked crosshatched pattern. 3. The X-Ray diffraction (XRD) and photoluminescence (PL) spectrum would be weak and un-resolved. Since ZnCdMgSe has a small optimal MBE growth window a calibration of our substrate temperature was undertaken. It was seen that our growth

temperature had drifted $\sim 30^\circ\text{C}$ below the optimum. Once this correction was made to both the LT buffer and the growth temperature improvements were seen in time period before deterioration of the RHEED pattern occurred. As these structures are thicker than the earlier ones, efforts were made to minimize the lattice mismatch of all three constituents of the structure, InGaAs, ZnCdSe, and ZnCdMgSe. Control of the mismatch of the ZnCdSe and ZnCdMgSe, measured by (004) XRD scans, was very sensitive to small changes in the Cd:Zn ratios, suggesting that the layers might not be fully relaxed. Asymmetric (115) reflection measurements were done on a ZnCdMgSe single layer grown under the optimized conditions, which did not exhibit RHEED deterioration. The results indicated that the sample was pseudomorphic even at a thickness of 1600 nm with a -0.5% mismatch, far above the expected critical thickness. The XRD studies also indicated that there was a preference for tensile strain to grow good quality material. Incorporating these corrections has culminated in the recent growth of QC laser structures that exhibit streaky RHEED patterns, smooth surfaces, and high resolution XRD and PL spectra indicative of high quality materials. This work was supported by NSF Grants No. EEC-0540832 (MIRTHE-ERC) and HRD-0833180 (CENSES).

11:40 AM Student

R10, Growth of III-Sb VECSELS for High-Power Continuous Wave Operation: *P. Ahlwar*¹; *Thomas Rotter*¹; *Alexander Albrecht*¹; *Stephen Clark*¹; *Victor Patel*¹; *Simon Reissmann*¹; *Huiwen Xu*¹; *Christopher Hains*¹; *Larry Dawson*¹; *Ganesh Balakrishnan*¹; *Jorg Hader*²; *Jerome Moloney*²; ¹Center for High Technology Materials; ²University of Arizona

We present growth and design of III-Sb vertical-external-cavity-surface-emitting-lasers (VECSELS) on GaAs substrates for continuous-wave (CW) operation. The lack of effective thermal management in a VECSEL active region is the most significant limitation for the CW operation. Transparent intracavity heat spreaders such as natural diamond can efficiently extract the generated heat but the high cost, stimulated photon absorption and unwanted etalon effects limit their usefulness. Another approach that has yielded excellent result is the removal of the substrate on which the VECSEL is grown and subsequently bonding the chip to a low-cost CVD diamond such that the diamond is outside the cavity. This configuration is however very difficult to achieve in antimonide semiconductors on account of poor etch stop layers in the 6.1 \AA family. In this presentation, we demonstrate the bonding of III-Sb VECSELS to CVD diamond by first growing these lasers on GaAs substrates. The growth of such lasers on GaAs provides us with unique epitaxial designs that can take advantage of the superior AIAs based etch-stop layers and therefore vastly improved etch results. We shall investigate two kinds of VECSEL structures based on the growth of III-Sb epilayers on the GaAs lattice constant - (a) a Top-emitter design and (b) a Bottom-emitter design. The structures are designated as top or bottom emitters based on the sequence in which the DBR and active regions are grown. In a Top-emitter VECSEL structure the antimonide quantum wells and barriers are typically grown on top of a MOCVD grown GaAs/AlGaAs DBR. The antimonide growth is done in a molecular beam epitaxy (MBE) reactor while the GaAs/AlGaAs DBRs are grown using metal-organic chemical vapor deposition (MOCVD). In case of a bottom-emitter VECSEL structure, the antimonide active regions are grown on a GaAs substrate followed by an AlSb/GaSb DBR. The top-emitter while grown on GaAs/AlGaAs DBRs is extremely difficult to process due to the fact that the bonding of the laser is done after the removal of the substrate, making it very difficult to handle the $7 \mu\text{m}$ thick VECSEL structure. The bottom emitter design is more suitable for processing since the laser is first bonded to the diamond followed by substrate removal. The CVD diamond therefore acts as wafer handle for the VECSEL epi-layers that have been released from the substrate. We shall in the presentation describe in greater detail the growth of the above structures. We shall also present characterization results of the semiconductors through techniques such as X-ray diffraction (XRD), photoluminescence (PL), surface Nomarski microscopy and atomic force microscopy (AFM).

Session S: Nanowire Synthesis and Characterization

Thursday AM
June 23, 2011

Room: Lotte Lehman
Location: Univ. of California-Santa Barbara

Session Chairs: Chen Yang, Purdue University; Kris Bertness, National Institute of Standards and Technology

8:20 AM Student

S1, Photoluminescence of Chemical Vapor Deposition-Grown Diamond Nanowires: *Steven Palefsky*¹; *Chih-Hsun Hsu*¹; *Sylvain Cloutier*²; *Jimmy Xu*¹; ¹Brown University; ²University of Delaware

Diamond has been one of the most studied materials in recent decades. It has a very wide band gap (5.5 eV), high electron and hole mobilities and a negative electron affinity. Due to these characteristics, it has been used in a broad range of applications, including ultraviolet light detectors and emitters¹, field effect transistors², and position-sensitive biochemical substrates³. The discoveries of diamond nanostructures and nanorods^{4,6}, including the recent finding of chemical vapor deposition (CVD)-synthesized diamond nanowires by our laboratory⁷, open up a new area of research, which combines the advantages of diamond with those of 1D semiconductors; these include large surface-to-volume ratio, high device density, and high spatial resolution. In particular, the unique optical properties of diamond have spurred a recent interest in diamond nanowires for photonic applications, including the use of nitrogen-vacancy (NV) centers in reactive ion-etched DNWs as single-photon emitters. In principle, diamond nanowires grown in a CVD process should naturally contain nitrogen-vacancies or other defects, and hold certain advantages over the etched nanowires, such as better crystallinity, a higher quality surface, and better uniformity along the length. In this study, we measured the emission spectrum of CVD-grown diamond nanowires. The samples were fabricated in an atmospheric pressure CVD process using methane and hydrogen flow over iron catalyst at 900°C, as detailed by Hsu et al⁷. The sample was excited with a nitrogen laser with wavelength 337 nm, and the emission was collected with a silicon ICCD array. The DNWs grown in the CVD reactor are straight and uniform in diameter (60-90 nm) over the entire lengths of tens of microns. Spectroscopic analysis, electron diffraction and transmission electron microscopy provided confirmation that these nanowires are crystalline diamond, with large crystal domains (at least 30 nm x 30 nm) and high structural uniformity, and are encased in a graphitic shell. A photoluminescence spectrum of the diamond nanowires shows a strong, broad peak at 415 nm whose full-width at half-maximum (FWHM) is 23 nm. The 415 nm feature indicates the presence of the N3 center in diamond⁸. This defect is common in natural diamond⁸, and has been observed in diamond films and nanoparticles⁹. The N3 center is modeled by three substitutional nitrogen atoms and a vacancy. This emissive center could prove useful for various applications, such as resonant-cavity enhanced spontaneous light emitting devices (LED) and low-threshold below-bandgap lasers. Although further study is needed to determine its properties – such as lifetime, photostability and quantum efficiency – before its suitability for functions such as single-photon emission can be assessed. The extreme straightness and uniformity of the diameter of our CVD-grown DNWs should lend itself to waveguiding, which can enhance both excitation of the luminescence center and collection of the resultant photons¹⁰.

8:40 AM Student

S2, Properties of ErAs and ErSb Nanorods Embedded in High-Index III-V Semiconductors: *Trevor Buehl*¹; *Christopher Palmström*¹; *Arthur Gossard*¹; ¹UCSB

Over the last decade, a number of interesting thermoelectric and terahertz device applications have arisen from research into embedded rare-earth mononitride particles in III-V semiconductors on (100) oriented substrates. For example, nearly spherical nanoparticles of ErAs embedded in semiconducting materials such as (100) GaAs were found to exhibit ultrafast recombination of

electron-hole pairs and to significantly alter their optical properties. Previously, we reported that low (up to 10%) atomic concentrations of Er codeposited with Ga and As produced ordered arrays of ErAs nanorods embedded within GaAs when grown on (411)A GaAs, in contrast to ErAs nanoparticles embedded in (100) GaAs and (411)B GaAs. We have also reported that using the same growth conditions as found in reference 3, we were able to grow embedded ErAs nanorods on (111)A, (211)A, and (311)A GaAs. These are very interesting structures due to their potential anisotropic electrical conductivity and thermal conductivity as one can tailor the growth direction and size of the nanorods by modifying the growth conditions. Additionally, the fact that the semimetallic ErAs nanorods are embedded within the GaAs matrix may provide new methods of contacting semiconductors. We present cross-sectional and plan view transmission electron microscopy (TEM) and high-angle annular dark field scanning transmission electron microscopy (HAADF STEM) results that can elucidate the growth mechanism involved in the formation of these ErAs nanorods. ErAs nanorods form by phase-separating at the growth surface during growth that can be controlled by changing the growth parameters used. Increasing the growth temperature as well as the Er concentration used increases both the size of the nanorods as well as the spacing between them. Nanorod orientation can be altered by growing on different GaAs surfaces. We present results obtained for other high-index growth surfaces such as (111) A GaAs, (211)A GaAs, (311)A GaAs, and (511)A GaAs.⁴ For example, ErAs nanorods were found to form on (111)A GaAs, (211)A GaAs and (311)A GaAs for a range of Er atomic concentrations and a range of growth temperatures. ErAs nanorods on (111)A GaAs were found to align themselves along the [111] whereas those on the (211)A and (311)A GaAs surface aligned themselves along the [211] direction, similar to that observed on (411)A GaAs. We show that the ErAs nanorods and the surrounding GaAs matrix are of high crystalline quality and have a continuous As sublattice across their interface. Growth of GaAs on top of these codeposited ErGaAs layers is free of strain contrast as observed in TEM – allowing for heterostructures to be grown above the codeposited layer.

9:00 AM Student

S3, Dynamic Control of Growth Kinetics for Three-Dimensional Semiconductor Nano-Heterostructures: *Santino Carnevale*¹; *Jing Yang*¹; *Patrick Phillips*¹; *Michael Mills*¹; *Roberto Myers*¹; ¹Ohio State University

The geometry of semiconductor nanowires (NWs) allows for both vertical and coaxial heterostructures, while only vertical heterostructures can be formed using planar structures. This is especially important for III-nitride NWs because crystallographic directions in which heterostructures are formed largely determine the magnitude of internal electric fields due to polarization. Here we describe a method to control the relative vertical and coaxial growth rates in catalyst-free GaN/AlN NW heterostructures grown on Si(111) substrates by plasma-assisted molecular beam epitaxy*. A growth phase diagram is established relating NW density to substrate temperature and III/V ratio. This diagram reveals a reduction in effective growth rate and an increase in nucleation time caused by GaN decomposition. A two-step growth method using dynamic conditions (determined by growth phase diagram) is developed to control NW density independently from deposition time. This method also allows for active tailoring of growth kinetics which is shown to tune the ratio of vertical to coaxial rates. We demonstrate the effectiveness of this method by forming multiple period GaN/AlN (2 nm / 2 nm) superlattices along either the vertical or coaxial NW axis that exhibit atomically sharp compositional profiles. This work is supported by the ONR under grant N00014-09-1-1153. * S.D. Carnevale, J. Yang, P.J. Phillips, M.J. Mills, and R.C. Myers. *Nano Lett.* (Article ASAP, 2011)

9:20 AM Student

S4, Structural Characterization of InGaAs Axial Inserts in GaAs Catalyst-Free Nanopillars Grown by Selective-Area MOCVD: *Joshua Shapiro*¹; *Diana Huffaker*¹; ¹UCLA

This work presents a study of axial GaAs/InGaAs hetero-interface formation in catalyst-free nanopillars grown by selective-area MOCVD. GaAs nanopillars (NPs) with multiple axial InGaAs inserts are characterized by photo-

luminescence (PL), dark-field scanning transmission electron microscopy (DF-STEM) and energy dispersive x-ray spectroscopy (EDS). Fractional indium content increases in longer inserts and in smaller diameter wires. The position of axial hetero-interfaces are analyzed and used to develop a growth model that accounts for the selective area pattern geometry and diffusion. Controlled growth of axial heterostructures is a key capability for enabling efficient nanopillar light emitters and detectors, and preliminary light-emitting devices with axial double heterostructures grown on silicon will be presented.

9:40 AM

S5, Control of III-V Nanowire Epitaxy by Precursor Chemistry: Omid Salehzadeh¹; Simon Watkins¹; ¹Simon Fraser University

A key requirement for the realization of nanowire (NW) devices is the ability to control axial and radial growth. Despite the extensive literature on this subject there have been relatively few reports of the role of precursor chemistry in the growth on NWs by metalorganic vapor phase epitaxy (MOVPE). Recently we have shown that the choice of Ga precursor can have dramatic effects on the morphology of GaAs NW grown by the vapor-liquid-solid (VLS) mechanism. The vast majority of previous MOVPE works on this topic have employed methyl-alkyl precursors such as trimethylgallium (TMGa). In core shell structures, control over axial vs. radial growth is usually achieved by varying the growth temperature. At low temperatures, lateral growth is inhibited, resulting in enhanced axial growth, while at high temperatures, lateral growth competes with VLS growth, enabling the formation of shell structures. A similar effect can be achieved by changing precursor chemistry by using less stable precursors whose vapor-solid (VS) growth rate is not kinetically inhibited. In this work we show that the use of triethylgallium greatly enhances lateral growth, permitting the formation of core shell heterostructures without changing the growth temperature. TEGa decomposes at lower temperatures than TMGa, resulting in gas diffusion limited growth for planar films at temperature $\sim 80^\circ\text{C}$ lower than TMGa. The formation of NWs by the VLS mechanism requires the kinetic hindrance of vapor solid growth on the substrate surface and nanowire sidewalls. NWs grown with TMGa generally exhibit low tapering/sidewall growth because VS growth is suppressed except at the highest temperatures. The use of TEGa results in increased competition for Ga vapor flux, resulting in the formation of much higher levels of tapering in NWs grown with TEGa alone, due to the much increased lateral growth. This suggests a strategy for growth of core shell homoepitaxial or heteroepitaxial structures by simply changing group III precursors. We have employed this technique to form InAs/GaAs heterostructures using trimethylindium (TMIn) and either TMGa or TEGa. The precursor sequence TMIn followed by TMG results in axial heterostructures with relatively abrupt interfaces as determined by EDS. In contrast under identical growth conditions, the sequence TMIn followed by TEGa results in InAs-core/GaAs-shell structures with little GaAs axial growth. We have also investigated the effects of carbon doping with CBr_4 dopant. Carbon is an excellent p-type dopant for planar growth of GaAs and other III-Vs. We show that the combination of TEGa and CBr_4 is ideal for the formation of p-type GaAs NW shells. In addition the use of diethyltellurium is reported as an n-dopant for GaAs NW cores. This combination of precursors enables us to form n-core p-shell structures, which are the building blocks for potential device applications such as NW photovoltaics.

10:00 AM Break

10:20 AM Student

S6, Temperature-Dependent Growth Direction of Epitaxial InSb Nanowires by Chemical Vapor Deposition: Jiebin Zhong¹; Jian Lin¹; Miroslav Penchev¹; Maziar Ghazinejad¹; Mihri Ozkan¹; Cengiz Ozkan¹; ¹University of California Riverside

Recently, one dimensional (1D) semiconductor nanowires (NWs) have received many attentions in both fundamental and applied electronic areas. Indium antimonide (InSb) NW, as a III-V semiconductor material, is attractive nano-building blocks for high-speed and low-power electronics, infrared detectors and thermal-electric (TE) devices due to its high bulk electron mobility ($77000\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ at 300k), narrow direct band gap (0.17 eV at 300k) corresponding to long-wave infrared regions and smallest effective mass

predicted to possess highest TE figure of merit (ZT). Regarding the controlled growth of NWs, the study of controlling NWs growth direction is one of the most active research fields. However, there are limited reports regarding the growth parameters effect on III-V semiconductor NWs, especially for InSb NWs. In this study, we have investigated growth temperature effect on the growth direction of InSb NWs. First of all, Au-assisted InSb NWs have been grown in a temperature range from 300°C to 450°C on InSb (100) substrate by chemical vapor deposition (CVD). InSb powder is placed at the high temperature zone (570°C) of the furnace while Au nanoparticles-coated InSb substrates are kept at the downstream positions, corresponding to different growth temperature. Ar and Hydrogen with 1:1 ratio are introduced into the furnace as carrier gas. NW growth directions are compared between the growth temperature at 350°C and 450°C . This comparison shows that the growth direction of InSb NWs cannot be easily distinguished from the scanning electron microscopy (SEM) image at 350°C , while three major growth directions of $\langle 111 \rangle$, $\langle 110 \rangle$ and $\langle 211 \rangle$ are observed at 450°C . It is well known that NWs prefer the growth direction possessing the minimum surface energy [1]. Finally we achieved uniform growth direction of InSb NWs by optimizing the growth temperature. InSb NWs with uniform growth direction of $\langle 110 \rangle$ direction were grown at 410°C . A 60° tilted SEM shows a 26.6° rotated angle to a InSb NW, which is initially observed as horizontal from the top view SEM image. This suggests a 45° inclined angle with respect to the substrate, which is one of the plane angles between $\{110\}$ and $\{100\}$. High resolution transmission electron microscopy (HRTEM) confirms the growth direction by measuring the d-spacing. These results indicate that growth temperature plays an important role when controlling the InSb NWs growth direction and comparable to those published III-V semiconductor NWs works [2][3]. Our findings provide experimental basis for further investigation of controlled growth of InSb NWs, also serve as a general purpose for in-depth study of III-V semiconductor NWs growth mechanism and applications.

10:40 AM Student

S7, Effect of Precursor Flow Rates on the Growth of InP/Sb Nanowires on InP(111)B: Chilan Ngo¹; Marta Pozuelo¹; Matthew Mecklenburg²; Hailong Zhou³; Chris Regan²; Robert Hicks³; Suneel Kodambaka¹; ¹UCLA Department of Materials Science; ²UCLA Department of Physics and Astronomy; ³UCLA Department of Chemical and Biomolecular Engineering

Group III-V semiconductors possess high carrier mobilities and small band gaps, making them an important class of materials with applications in nanoelectronics and optoelectronics. One-dimensional structures, such as nanowires, of these materials are attractive because, their properties can, in principle, be controllably tuned to realize desired functionality. Nanowires are most commonly grown from the vapor phase using an external metal catalyst via vapor-liquid-solid (VLS) or vapor-solid-solid (VSS) processes. Other variants of this approach involve the use of a sacrificial catalyst, for example the group III element, or using an oxide template. Recent studies have shown that InP and $\text{InP}_{1-x}\text{Sb}_x$ nanostructures of desired shape, structure, and composition can be grown via metalorganic chemical vapor deposition (MOCVD) using liquid indium droplets as catalysts. Here, we focus on the influence of the metalorganic precursor flow rates on the structural and compositional evolution of $\text{InP}_{1-x}\text{Sb}_x$ alloy nanostructures.

11:00 AM

S8, Precise Placement and Diameter Control of Catalyst-Free Molecular Beam Epitaxy Grown GaN Nanowires: Aric Sanders¹; Kris Bertness¹; Andrew Herrero¹; Alexana Roshko¹; Norman Sanford¹; John Schlager¹; Todd Harvey¹; Devin Rourke¹; ¹National Institute of Standards and Technology (NIST)

The high material quality of catalyst-free GaN nanowires has been well established, and the integration of nanowires into functional devices is common practice. However, in order to realize true device scalability and repeatability a method of controlling diameter and nanowire placement is needed. Several approaches for selective growth of nanowires of predetermined diameter and location have been developed. We present one based on a SiN_x masking technique that offers unique advantages. A Si (111) substrate with an AlN buffer

layer is masked with a low stress SiN_x mask. Openings are defined in the mask using a combination of standard photolithography, electron beam lithography and reactive ion etching. The choices of electron beam resist, cleaning methods and SiN_x thickness plays a critical role in the placement and size of the nanowires. We will discuss how the physical mask determines the nanowire properties, and similarly we will discuss the appropriate temperature and Ga:N ratio to create conditions of almost perfect selectivity. Under these conditions, uniform growth in mask openings is observed with the absence of growth on the mask surface for over 95% of the usable area of a 76 mm diameter Si(111) substrate. In addition, the diameters of the resulting nanowires are controlled by the size of the mask openings. Openings of approximately 500 nm or less produce single nanowires with symmetrically faceted tips.

11:20 AM Student

S9, Synthesis and Fabrication of ZnTe Nanosheet Field Effect Transistors for Photonic Applications: *Ebraheem Azhar*¹; *Jih-Hong Peng*¹; *Ganesh Subramanian*¹; *Sandwip Dey*¹; *Hongbin Yu*¹; ¹Arizona State University

Zinc Telluride (ZnTe) is recently becoming an attractive material due to its direct bandgap of 2.26 eV at 300K, making it widely researched for a number of applications. To date, there are no reports of synthesis or of device fabrication of ZnTe nanosheets. Nanosheets offer the advantage of a completely exposed planar surface, as opposed to rounded nanowires, while maintaining confinement. This is particularly appealing for photonic applications such as detectors or photovoltaics where an even surface is advantageous for absorption. In this work, we report the fabrication of ZnTe nanosheets through a high temperature growth process followed by low temperature device fabrication on transferred silicon substrate. First, single crystal ZnTe nanosheets were grown on silicon (Si) with gold (Au) seed by heating ZnTe powder in a tube furnace at 519°C—promoting high quality of ZnTe nanosheets free from high density defects. X-ray diffraction shows the as-synthesized nanosheets have preferential orientation and scanning electron microscopy indicate ordered and single crystalline sheets have been obtained. The nanosheets were then transferred to device a substrate, in this case highly doped and conductive Si, through a mechanical transfer technique performed at room temperature. A photolithography process was then used to pattern electrodes, followed by a Cr/Au deposition and liftoff. The current-voltage characteristics were used to study the transport behavior of the nanosheet. Predominant p-type behavior was observed, an on/off ratio of 5x10⁴ was found, and an early voltage of 1.86 V was determined. The device was also annealed at 280°C for 30 minutes and increased conductivity as well as reduced hysteresis were observed. Photoconductivity of individual ZnTe nanosheets were also investigated under white light with varying intensity. A photoconductive gain of 600 was found and a responsivity of 37 A/W was also determined. These values are quite comparable to similar ZnTe nanodetector devices. The mechanism for photoconductive gain in ZnTe has largely been attributed to surface states creating trap recombination centers leading to longer carrier lifetimes. These results reveal that single ZnTe nanosheets are excellent candidates for applications for nanoscale photoconductive detectors.

11:40 AM S10, Late News

Session T: Growth of Graphene and Carbon Nanotubes

Thursday AM
June 23, 2011

Room: MCC Theatre
Location: Univ. of California-Santa Barbara

Session Chairs: Mike Spencer, Cornell University; Randall Feenstra, Carnegie Mellon University

8:20 AM Student

T1, Epitaxial Graphene Formation on Step-Free 4H-SiC(0001): *Michael Bolen*¹; *Bob Colby*¹; *Eric Stach*²; *Michael Capano*¹; ¹Purdue University; ²Brookhaven National Laboratory

The thermal decomposition of silicon carbide (SiC) has proven itself as a feasible technique for producing high-quality graphene. Thanks to the efforts of researchers from around the globe, progress has been made towards better understanding and controlling epitaxial graphene formation on SiC. For instance, it is now well-known that SiC thermal decomposition begins at ledges, which are intrinsic to SiC substrates with a vicinal off-cut. This knowledge is due, in part, to the fact that all decomposition studies to date have begun with SiC substrates with varying degrees of vicinal off-cut. This raises a poignant question: How would a step-free surface affect thermal decomposition? For the first time, step-free SiC was homoepitaxially grown and subsequently thermally decomposed at various temperatures under vacuum (low-10⁻⁵ mbar) to explore graphene formation in the absence of surface steps. Mesas with various percentages of step-free coverage were formed to create stepped and step-free regions next to each other on the exact same mesa. Atomic force microscopy (AFM), Raman spectroscopy, and high-resolution transmission electron microscopy (HRTEM) were used to study graphene formation on step-free surfaces and contrast the formation against vicinally stepped surfaces. Through AFM studies, it was found that graphene formation on step-free surfaces begins with the clustering of surface vacancies. These clusters form triangular pits that grow in area through lateral erosion along the SiC {1-100} planes. As erosion continues through Si desorption, the triangular pits merge and leave behind a graphitized surface. This formation is in contrast with stepped surfaces that erode along the existing ledges created by the vicinal cut of the substrate. Further differences in the graphene film on the step-free and stepped region are apparent from Raman spectroscopy and HRTEM. After thermal decomposition at 1475C for 10 min, Raman spectroscopy demonstrates that stepped regions have a blueshifted 2D peak position of 16 cm⁻¹ and a larger peak width by nearly 40 cm⁻¹ as compared to step-free regions. This difference is attributed to film thickness, which is measured by cross-sectional HRTEM. Stepped regions have a graphitic film nearly 2 nm thick as compared to less than 0.7 nm for step-free regions. This thickness variation is attributed to differences in surface energy of the stepped and step-free regions as described by the terrace-ledge-kink model. The vicinal ledges have a relatively higher surface energy as compared to the step-free surface. As such, the vicinal surface ledges are prone to faster Si desorption and faster graphene formation.

9:00 AM

T2, Effects of Substrate Orientation and Growth Environment on the Structural and Electronic Properties of Epitaxial Graphene on SiC(0001): *Joshua Robinson*¹; *Kathleen Trumbull*¹; *Michael LaBella*¹; *Randall Cavalero*¹; *Matthew Hollander*¹; *Michael Zhu*¹; *Maxwell Wetherington*¹; *Mark Fantoni*¹; *David Snyder*¹; ¹Penn State University

We investigate carrier transport and graphene structural properties as a function of silicon carbide (SiC) wafer orientation and growth ambient. Monolayer epitaxial graphene is found to exhibit Raman 2D/G ratios greater than 0.85, while multilayer graphene 2D/G ratios average 0.50. Additionally, increased terrace edges are observed as wafer orientation diverges from the (0001) crystallographic direction, which leads to increased carrier density and decreased mobility. We report that while those angles closest to the (0001)

direction produce superior transport properties (room temperature mobility (μ_e) up to $2400\text{cm}^2/\text{Vs}$), the presence of uncontrolled terrace formation can result in significant scatter in the carrier mobility. As the SiC surface normal diverges from (0001), the terrace edge formation becomes uniform and parallel, leading to a significant improvement in Hall transport uniformity across the wafer. Raman spectroscopy maps of the same Hall cross provide evidence that the G peak intensity, 2D-peak intensity, and 2D/G peak ratio are all affected by the presence of the SiC terrace edge. The G-peak intensity doubles at the terrace edge, while the 2D peak is significantly less affected. As a result, we find that the 2D/G peak ratio is reduced from >1 at the terrace center to $0.4 - 0.5$ at the terrace edge. This alone does not constitute layer thickness variation; however, according to Lorentzian fitting of the 2D peak from individual Raman spectra the graphene on the terrace center and edge is monolayer and bilayer graphene, respectively. Hall transport measurements indicate that room temperature carrier density and mobility are affected by the presence of step edges. Hall crosses exhibiting high mobility also exhibit zero or one narrow step edge (Figure 1a), while highly doped samples exhibit multiple ($= 2$) step edges. When miscut is 0.02 degree or greater, the carrier transport properties become significantly more uniform, with deviation around the mean averaging $< 6\%$. However, in addition to improved uniformity, the average carrier density and mobility is changed by as much as $+30\%$ and -40% , respectively, compared to the 0.02 degree sample. Finally, Ar growth ambient is shown to result in carrier mobilities three times that of graphene grown in He, indicating that graphene transport properties may be further improved via growth in heavy molecular weight gaseous environments. This is due to the reduced probability for Si evaporation as the molecular weight of the gas ambient increases.

9:20 AM

T3, High Mobility Epitaxial Graphene on Sapphire via Metal-Free CVD: Mark Fanton¹; Joshua Robinson¹; Conor Puls¹; Brian Weiland¹; Michael LaBella¹; Kathleen Trumbull¹; Richard Kasarda¹; Casey Howsare¹; Joseph Stitt¹; David Snyder¹; ¹Penn State University

We present a novel method for the direct metal-free growth of graphene on sapphire that yields graphene films comparable to that of graphene grown on the (0001) face of SiC. Film nucleation and quality are a strong function of methane concentration, growth time, and growth temperature. In all cases the graphene is believed to be significantly strain free, with no evidence of an interfacial buffer layer. There is a strong correlation between the graphene structural quality and carrier mobility. Graphene films were deposited on 50mm diameter c-plane sapphire wafers (Crystal Systems, Inc) in a commercial high temperature semiconductor CVD tool. Process gases consisted of a mixture of 10% methane (CH_4) in hydrogen (H_2) in an argon (Ar) carrier gas. Growth was performed at $1425\text{C}-1700\text{C}$ at a pressure of 600 Torr. Raman spectroscopy suggests the formation of monolayer and bilayer graphene, with improved structural quality as deposition temperature increased. Using the D/G peak ratio, the domain size increased from an average low of 32 nm at $1425-1450^\circ\text{C}$ ($\text{D}/\text{G} = 0.42$) to greater than 270 nm ($\text{D}/\text{G} = 0.05$) at 1575C . In all cases, the 2D/G ratio was greater than 1.5 and the 2D peak was fit to either one or four Lorentzians. Similar to graphene on SiC(000), films on sapphire exhibit wrinkling, which likely serve as sources of strain relief. On sapphire the wrinkles exhibit heights of $0.4 - 1.5$ nm. XPS was used to study Al-O-C bonding at the graphene/sapphire interface. Peaks from the Al-O-C interaction would be present if an interfacial layer were to exist. However, it is clear from the C 1s spectra that there are no Al-C bonds (281.5eV) and no Al-O-C bonds (282.5eV) present on the surface confirming the absence of an interfacial layer between graphene and sapphire. Room temperature Hall effect mobilities were measured to be as high as $3200\text{cm}^2/\text{Vs}$. Additional electronic transport measurements of van der Pauw devices were carried out at 2K and magnetic fields up to 9T. Measurements of longitudinal resistance and low field ($|H| < 2\text{ T}$) Hall coefficient in multiple devices suggest Hall mobilities reach as high as $10,500\text{cm}^2/\text{Vs}$, while higher magnetic fields yield non-constant Hall coefficients due to the emergence of quantum transport phenomena in the graphene films.

9:40 AM Student

T4, Study of Epitaxial Graphene on Non-Polar 6H-SiC Faces: Biplob Daas¹; KM Daniels¹; S. Shetu¹; TS Sudarshan¹; MVS Chandrashekar¹; ¹University of South Carolina

Graphene, a two-dimensional (2D) form of honeycomb crystal structure, exhibits unusual electronic and optical properties [1]. Epitaxial graphene (EG), grown by thermal decomposition of the polar c-plane of SiC in ultra high vacuum and high temperature is well documented, while that of the non-polar faces is not. The knowledge of the growth on these faces is technologically important as it will provide greater insight into the differences in growth between the Si and C-faces, currently a standing issue. Here we study EG grown on non polar n-type 6H-SiC, both on a-plane ($11\bar{2}0$), EG-a and m-plane($11\bar{0}0$), EG-m faces, by the well known thermal decomposition technique in an inductively heated RF furnace at temperatures $1350-14500\text{C}$ and pressures $<10^{-6}$ Torr while a witness polar Si-face c-plane sample was included for comparison. Atomic force microscopy (AFM) and Raman measurement were carried out on grown EG-a and EG-m where both EG-a and EG-m exhibit nanocrystalline graphite-like features, with an underlying long range periodicity that may be from steps on the surface. Raman analysis of EG-a and EG-m for different growth condition shows, G peak (1586 to 1590cm^{-1}), D peak ($1334-1348\text{cm}^{-1}$) and 2D peak ($2657-2678\text{cm}^{-1}$) confirm the presence of graphene. All peaks are red shifted attributes strain on surface with increasing growth temperature possibly due to the interaction with the substrate on EG in both the cases. The disorder ratio(D/G) for EG-m decreases from 1.1 to 0.5 as the growth temperature varied from 13500C to 14500C , indicating increasing grain size while D/G for EG-a does not vary significantly. The reason for this difference is at present unclear, and is currently being investigated. Both EG-m and EG-a exhibit much greater disorder than the polar Si-face (<0.1 , optimized). X-ray photoelectron spectroscopy (XPS) showed that both EG-m and EG-a layers are thicker than their corresponding polar c-plane Si-face sample. This may be due to a greater density of carbon atoms on the non-polar faces than on the polar Si-face. Infrared (IR) reflectivity measurements were carried out to find thickness(N) in monolayer(ML), Fermi level position(E_f) and scattering time (τ) by fitting theory with experiment [3]. Thickness measurements were also correlated with XPS. At 13500C EG-a has 2ML with $\tau=15\text{fs}$ whereas EG-m has 4ML with $\tau=1\text{fs}$. As expected, the non-polar faces are thicker than the polar Si-face, with shorter τ , consistent with the smaller grain size. Further investigation is underway to clarify these differences.

10:00 AM Break

10:20 AM Student

T5, Synthesis of a Pillared Graphene Nanostructure: A Three-Dimensional Hybrid Carbon Architecture: Maziar Ghazinejad¹; Shirui Gue¹; Rajat Paul¹; Mihri Ozkan¹; Cengiz Ozkan¹; ¹University of California, Riverside

Using chemical vapor deposition (CVD) technique a novel 3D carbon nano-architecture called a pillared graphene nanostructure (PGN) is synthesized in situ. The fabricated novel carbon nanostructure consists of CNT pillars of variable length grown vertically from large-area graphene planes. A one-step CVD process for large-area PGN fabrication through combination of surface catalysis and in situ vapor-liquid-solid mechanisms is described. The dependence of the morphology of the large-area PGN on the synthesis process conditions was investigated by optical microscopy, SEM, TEM, HRTEM, and Raman spectroscopy techniques. The highly crystalline interface between the CNT pillar and graphene floor confirmed the seamless contact between the two carbon allotropes. Moreover, to tune the PGN architecture, arrays of catalyst particles with controlled size and separation distance are fabricated using block copolymer films as template. This strategy yields tunable diameter and separation distance of pillar carbon nanotubes, and provides control over the amount of final carbon structure surface area. The successful transfer of the large area PGN onto arbitrary substrates, while keeping the 3D architecture intact, was also accomplished. The new synthesis methodology offers a promising pathway for fabricating novel 3D nanostructures with huge potential in hydrogen storage and supercapacitors, and provides a powerful means to fulfill Department of Energy's targets for energy storage.

10:40 AM Student

T6, Electrochemical Graphane Conversion Using E-Beam Evaporated Metals for Catalytic Enhancement: *Kevin Daniels*¹; *Biplob Daas*¹; *Rui Zhang*¹; *John Weidner*¹; *Christopher Williams*¹; *Tangali Sudarshan*¹; *MVS Chandrashekhara*¹; ¹University of South Carolina

Graphene hydride, or better known now as graphane is as thermodynamically stable as comparable hydrocarbons, more stable than metal hydrides and more stable than graphene by ~ 0.15 eV. While bulk graphite has been observed to be chemically inert to most chemicals, graphene has demonstrated the ability to react with some atoms such as fluorine, and most importantly hydrogen. When hydrogen bonds with the p-bonds of graphene, the delocalized p-electron now becomes localized at the C-H bond, decreasing the conductivity, changing the bond hybridization from sp^2 to sp^3 and increasing the C-C bond length $\sim 7\%$ from 1.42 Å to 1.52 Å. The electron localization at the sp^3 bond leads to a decrease in conductivity, and opens up a bandgap varying from 0-3.5 eV depending on the degree of hydrogenation. This enables new applications in bandgap engineered electronics using carbon-based materials. The difficulty with forming graphane is the need for atomic hydrogen. While other groups have formed graphane by in situ development of atomic hydrogen by hydrogen plasma or pumping explosive gases into the growth furnace, it was recently shown that graphane can also be formed ex situ electrochemically. In this paper, we demonstrate an enhanced electrochemical means to generate atomic hydrogen, by evaporated metal to improve hydrogen incorporation into graphane during the conversion process. On-axis, semi-insulating, 6H-SiC substrates were used to form epitaxial graphane at $\sim 1400^\circ\text{C}$ in vacuum as starting material for graphane production. All samples were chosen from the same wafer to maintain consistency in conversion. The ratio of the graphene Raman G-peak to the disorder D-peak was >10 , showing the high quality of the starting material. Then 10 Å-30 Å of either Pt or Au were evaporated onto the graphene surface. Atomic hydrogen was generated using a home-built electrochemical setup with current applied through a 10% sulfuric acid solution, with a Pt wire and exposed graphene as the anode and cathode, respectively. Successful hydrogenation was confirmed by a marked increase in resistance, presence of C-H bond peak at $\sim 2930\text{ cm}^{-1}$ and peak shift, narrower than expected from damage and increase in D peak. It was observed that graphane samples with evaporated Pt were more reactive than Au evaporated samples and much more reactive than plain graphene according to Raman. The increase in resistance was also more substantial on the Pt converted samples $\sim 10\times$ as compared to that of Au $\sim 2\text{ k}\Omega$, plain converted graphene $\sim 1.7\text{ k}\Omega$ and unconverted graphene $\sim 1\text{ k}\Omega$. AFM images show interesting features in the unconverted and converted Au and Pt evaporated samples where before conversion evaporated metal looks conformal and after conversion the metal particles on both samples appear to clump together exposing the underlying graphene surface. After conversion graphene steps were present in the Pt and absent in the Au.

11:00 AM

T7, Highly Reproducible Growth of Carbon Nanotubes for Practical Applications in Electronics: *Yohei Yagishita*¹; *Daiyu Kondo*¹; *Ikuo Soga*¹; *Taisuke Iwai*¹; ¹Fujitsu Laboratories Ltd

Carbon nanotubes (CNTs) are promising candidates for LSI interconnects and heat-dissipation bumps in the future [1, 2] because of their tolerance to higher current density and their higher thermal conductivity than that of copper used generally in electronics. Highly reproducible and uniform growth of CNTs with a high CNT density ($>10^{10}/\text{cm}^2$) and definite length (10–100 μm) has to be realized so that the practical use of CNTs in such applications can be achieved. However, it has been observed that the reproducibility in terms of CNT length and density is low in the case of growth of CNTs at a low density ($\sim 10^9/\text{cm}^2$) on a silicon substrate. In this study, we have demonstrated a highly reproducible and uniform growth of CNTs with high CNT density. CNTs were grown by thermal chemical vapor deposition (CVD). The CVD process was carried out in a vacuum chamber with a load-lock system. A mixture of acetylene and argon gases was used as the carbon source and introduced into the CVD chamber. The substrate temperature and total pressure were around 650°C and 1–4 kPa, respectively. To maintain the same CNT growth conditions, the temperature deviation from the growth temperature ($\pm 5.7^\circ\text{C}$) was improved to be below

$\pm 1.0^\circ\text{C}$. An iron film sputtered on a silicon substrate with 300-nm-thick silicon dioxide was used as the catalyst. The iron films had a thickness of 1.0 to 5.0 nm. By optimization of the CVD process, we achieved high reproducibility in terms of CNT length (deviation of CNT length: 11%), which was less than half the reproducibility achieved previously (deviation of CNTs length: 28%). In addition, uniform growth of CNTs across the 3-inch substrate (deviation of CNTs length: 1.5%) was achieved under the same optimized conditions; this uniform growth might be because the temperature deviation in the CVD chamber is small. These results imply that low temperature deviation from the growth temperature is important for achieving good reproducibility and uniformity. Moreover, synthesis of CNTs with a higher density ($\sim 10^{10}/\text{cm}^2$) was performed by optimizing the CVD conditions. Finally, the electrical properties of CNT bundles synthesized by optimizing the growth conditions were measured and compared with the electrical properties of CNTs obtained before optimization. The electrical properties of CNT bundles synthesized by optimizing the growth conditions were considerably better than those reported previously [2]. This clearly indicates that the density of CNTs synthesized by adopting the present optimized CVD conditions is higher than that of CNTs synthesized before optimization.

11:20 AM

T8, Graphene and Carbon Nanotube Growth in Vacuum Systems: *Bruce Willner*¹; *Tom Salagaj*¹; *Virgil Shields*²; *Michael Spencer*²; *Nick Sbrockey*¹; *Gary Tompa*¹; ¹Structured Materials Industries, Inc.; ²Cornell University

Nanoscale carbon structures, including graphene and carbon nanotubes, has drawn intense interest for study and for applications over a broad range of industries and fields due to the highly unusual structure and properties of the materials. Graphene consists of a single flat layer of carbon atoms, densely bound in a honeycomb structure. While discovered earlier, it is perhaps easiest to describe carbon nanotubes as a layer of graphene rolled into a cylinder. Graphene has been shown to be highly conductive, durable, flexible, and impermeable. Likewise, carbon nanotubes demonstrate exceptional strength and conductivity. Both graphene and carbon nanotubes have been fabricated by several methods. Among them, vacuum growth techniques, including sublimation (for graphene) and chemical vapor deposition (for both) hold the greatest promise for scalable, controlled production of high quality materials. Sublimation and chemical vapor deposition (CVD) have been used to produce single and multi-layer graphene films. We are developing an array of processes and process specific tools for graphene manufacturing on a variety of substrates. In this presentation, we review results we have achieved using several of these techniques, and compare reactor designs and process tradeoffs with the different tools. The earliest technique for graphene formation on large scale substrates was silicon sublimation from SiC, based upon graphitization of SiC surfaces, a well known phenomenon. Sublimation formation of graphene on the surface of a SiC wafer has been performed in a vertical reactor under ultra high vacuum (UHV) and in an Ar atmosphere at 1300° to 1650°C . Dramatically different growth characteristics are seen for the C face and the Si face of SiC, including growth rate and self-limiting characteristics. CVD of graphene has been achieved on a variety of substrates including dielectrics and metals, with different substrates requiring different process conditions. CVD on metal has been widely demonstrated using copper, nickel, and iridium substrates at temperature of 900 – 1000°C . Recently, the Cornell research team has demonstrated graphene CVD on a wide range of dielectrics as well, including: 6H-SiC (both Si-face and C-face), SiO₂, and sapphire in the 1300°C to 1650°C range. In contrast to the sublimation approach with SiC, this carbon addition technique allows multi-layer graphene formation with controlled thickness (3 – 100 monolayers). Carbon nanotubes can be grown utilizing the same tools at 600 – 900°C using ethylene or methane for multi-wall or single wall nanotubes, respectively. Our team is refining process tools for the different growth regimes as well as for large area graphene production. We will present an overview of these approaches, the results, and directions being pursued.

11:40 AM T9, Late News

Session U: Highly Mismatched Alloys

Thursday AM
June 23, 2011

Room: Santa Barbara Harbor
Location: Univ. of California-Santa Barbara

Session Chairs: Rachel Goldman, Univ of Michigan; Joshua Zide, University of Delaware

8:20 AM Student

U1, Synthesis of $\text{Ge}_{(1-x)}\text{Sn}_x$ Alloy Thin Films Using Ion-Implantation and Pulsed Laser Melting (II-PLM): *Ashish Bhatia*¹; Win Hlaing Oo¹; Gene Siegel¹; Peter Stone²; Kin-Man Yu²; Michael Scarpulla¹; ¹Materials Science and Engineering, University of Utah; ²Lawrence Berkeley National Laboratory, Berkeley

Germanium (Ge) has an indirect band gap of 0.67 eV at the *L* point in the Brillouin zone but $\text{Ge}_{(1-x)}\text{Sn}_x$ has been shown to exhibit a direct band gap of 0.35 < E_g < 0.80 eV for $0 < x < 0.1$. However, the equilibrium room-temperature solubility of Sn in Ge is limited to less than $x=0.01$. This is primarily caused by the large difference (14.7 %) in covalent radius of the Sn ($r_{\text{Sn}} = 140.5$ pm) and Ge ($r_{\text{Ge}} = 122.3$ pm) atoms. The growth of epitaxial $\text{Ge}_{1-x}\text{Sn}_x$ films has been reported using growth techniques that take advantage of interfacial kinetics such as molecular beam epitaxy (MBE) [1], sputtering [2], and organometallic vapor phase epitaxy (OMVPE) [3]. Major problems encountered in MBE-grown and sputtered films include the propensity for Sn segregation, inferior crystallinity, and poor thermal stability. [3] On the other hand, high quality $\text{Ge}_{1-x}\text{Sn}_x$ and related group IV alloy films have been grown using difficult-to-synthesize organometallic precursors. Here, we report on our work using ion-implantation of Sn into Ge followed by pulsed laser melting (II-PLM) to synthesize $\text{Ge}_{1-x}\text{Sn}_x$ alloy thin films. A low and a high dose (Sn^+/cm^2) sample were prepared using a combination of 35 and 150 keV acceleration voltages so as to create a near-uniform profile of Sn in Ge over a depth of 60 nm. These samples were then irradiated in air by a single pulse from a KrF excimer laser ($\lambda=248$ nm, pulse width ≈ 25 ns). The heating by the laser and subsequent heat diffusion into the substrate drives a process of melting followed by rapid solidification at rates that can exceed the diffusive velocity in the liquid. This departure from local equilibrium resulting in solute trapping has been exploited to synthesize metastable semiconductor alloys such as $\text{Ga}_{1-x}\text{Mn}_x\text{As}$ [4], $\text{Zn}_{1-x}\text{Mn}_x\text{Te}_{1-y}\text{O}_y$ [5]. In this work we explore whether epitaxial films of $\text{Ge}_{1-x}\text{Sn}_x$ may be formed similarly using II-PLM. First, the KrF pulse fluence was varied from 0.25-0.45 J/cm^2 based on heat flow predictions of the fluence required for complete melting of the implanted layer. It was found from observations of the surface that some of the Ge was ablated at the higher fluences but that this effect was minimal at lower fluences. Fourier transform infrared spectroscopy (FTIR) reveals increased absorption below the Ge band edge for $\text{Ge}_{(1-x)}\text{Sn}_x$ thin films. Incorporation of Sn was also corroborated by a blue shifting of the Ge-Ge Raman scattering and direct observation by Rutherford back scattering spectrometry (RBS). The crystallinity of these films is significantly lower than that of epitaxially-grown films and inadvertent incorporation of O was seen. Reasons for these film imperfections and strategies for overcoming them in further investigations will be discussed.

8:40 AM

U2, Nitrogen Ordering in Ga(NAs) at the Atomic Scale: *Vivien Voßbürger*¹; *Lena Ivanova*²; *Andrea Lenz*²; *Nadine Oswald*²; *Kakhaber Jandieri*¹; *Mario Dähne*²; *Wolfgang Soltz*¹; *Kerstin Volz*¹; *Holger Eisele*²; ¹Philipps University Marburg; ²Technische Universität Berlin

Diluted nitride III/V semiconductors offer a wide range of applications for laser devices and solar cells. The incorporation of N into III/V semiconductors enables to achieve technologically relevant wavelength ranges and lattice-mismatch engineering at the same time. This is important for the III/V integration on non-polar substrates like Si or Ge. Typical quaternary dilute nitride material systems are Ga(NAsP) for the growth on Si and (GaIn)(NAs). (GaIn)(NAs)

with low In concentrations around 8% can be used to improve triple junction solar cells on Ge. (GaIn)(NAs) laser material containing up to 30 % of In can be grown compressively strained on GaAs. It is well known that (GaIn)(NAs) materials show a strong improvement of their optoelectronic properties by a post growth annealing. It is speculated that this improvement can be attributed to a dissolution of local N-ordering in (GaIn)(NAs). In a first step, we studied the atomic structure of ternary Ga(NAs) by cross-sectional scanning tunneling microscopy and spectroscopy (XSTM and XSTS) to quantify the degree of N ordering in this system. For this purpose, pseudomorphic dilute nitride Ga(NAs) layers were grown on GaAs(001) substrates by metalorganic vapor phase epitaxy and molecular beam epitaxy. To clearly identify the distribution of N atoms in XSTM we compare the experimental results with simulations based on crystal models, obtained from density functional theory (DFT) and a combination of DFT and valence force field (VFF). At atomically resolved XSTM images we are able to identify N atoms in the topmost layer of the (110) cleavage surface, and distinguish them from other possible defects, as e.g., arsenic vacancies. We directly measure a clustering and even an ordering of N atoms along growth direction at the Ga(NAs)(110) cleavage surface, deviating from the statistical distribution of N atoms for the deposited N concentration. The clustering as well as the ordering of N atoms can be assigned to a preferential built-in of N atoms at places, where the lattice is locally strained at the (001) growth surface by underlying N atoms. This observation of ordering is further confirmed by Cs-corrected high resolution transmission electron microscopy. Furthermore, the observed clustering and ordering of the N atoms strongly influences the electronic structure. This can be observed directly as changes of the density of states of the conduction band in an energetic interval slightly above its minimum, as revealed from XSTS measurements.

9:00 AM Student

U3, A Study of MBE Grown $\text{InSb}_{1-x}\text{N}_x$ on GaAs for Long-Wavelength IR Applications: *Nimai Patra*¹; *Sudhakar Bharatan*¹; *Jia Li*¹; *Shanthi Iyer*¹; ¹North Carolina A&T State University

Indium antimonide (InSb) is known to have the smallest band gap energy amongst the III-V semiconductor alloys. Incorporation of dilute nitrogen into this alloy lowers its bandgap further, making it a suitable material for infrared imaging and outer space applications in 8-12 μm wavelength range. Further, Auger suppression in InSbN makes it a better material than the existing HgCdTe based systems for device applications. However, incorporation of nitrogen leads to defects, due to its smaller atomic size. In this work we present a comprehensive study of growth and characterization of InSbN layers grown on semi-insulating GaAs (001) substrate by solid source molecular beam epitaxy. A systematic study on the crystalline, optical, morphological and vibrational properties correlating the growth conditions and effect of N incorporation has been carried out. InSbN epilayers of thickness ~ 0.8 μm were grown on 1.5 μm thick InSb buffer layer at three different substrate temperatures 290 $^\circ\text{C}$, 330 $^\circ\text{C}$ and 380 $^\circ\text{C}$. Additionally, 2 μm thick InSbN epilayers were grown at 330 $^\circ\text{C}$ and 380 $^\circ\text{C}$ for transmission and reflection measurements. High resolution x-ray diffraction (HRXRD) (004) scan of these nitride samples exhibit a tensile strained epilayer peak with the lowest full width at half maxima of 198 arc-sec, except for the sample grown at 380 $^\circ\text{C}$ where no distinct peak corresponding to InSbN is observed. The N composition in these samples are estimated to be around 1.4% based on the x-ray simulation data on similar InSbN samples grown on InSb substrates. The nitrogen incorporation in all the above samples was also evident from the observation of N 1s peak in the corresponding x-ray photoelectron spectra (XPS). The sample grown at 380 $^\circ\text{C}$ demonstrates the highest percentage of In-N-Sb bonding, responsible for the band gap reduction in InSbN material system. However majority of the nitrogen was found to be in the form of In-N bonding. Absence of interstitial N-N in XPS is expected to lead to lower carrier concentration for improved device performance. Micro-Raman spectroscopy performed on all the above as-grown epilayers exhibit only longitudinal optical (LO) and transverse optical (TO) modes, indicating absence of Sb antisite and nitride related defects. InSbN sample grown at 380 $^\circ\text{C}$ exhibits the least TO/LO intensity ratio, indicating the best quality of the crystal structure. Atomic force microscopy studies showed a relatively smooth surface of root mean square roughness in the order of 5 nm for the nitride

sample grown at 380 °C as compared to all other samples. Absorption edge for these samples occurred in the wavelength region of 6- 6.2 μm. Variation of this absorption edge with N concentration will also be presented. This work is supported by the Army Research Office (Grant No. W911NF-10-1-0316, technical monitor Michael Gerhold).

9:20 AM Student

U4, Highly Mismatched GaN_{1-x}As_x Alloys across the Entire Composition

Range: *Alejandro Levander*¹; Sergei Novikov²; Zuzanna Liliental-Weber¹; Iraida Demchenko³; Jonathan Denlinger¹; Franziska Luckert³; Robert Martin³; Oscar Dubon⁴; Tom Foxon²; Junqiao Wu⁴; Wladek Walukiewicz¹; Kin-Man Yu¹; ¹Lawrence Berkeley National Laboratory; ²University of Nottingham; ³Strathclyde University; ⁴University of California - Berkeley

Typically only dilute (up to ~10%) highly mismatched alloys (HMAs) can be grown due to the large differences in atomic size and electronegativity of the host and the alloying elements. Recently, we overcame the miscibility gap of the GaN_{1-x}As_x system using low temperature molecular beam epitaxy (LT-MBE) and successfully synthesized alloys over a wide composition range. In the intermediate composition range (0.10 < x < 0.75) the resulting alloys are amorphous. Including the amorphous alloys, the band gap energy of the GaN_{1-x}As_x alloy spans from ~0.8 eV – 3.4 eV opening a wide range of possible applications, especially for multi-junction solar cells with a single semiconductor material system. It is important to note that the amorphous alloys have been grown on sapphire, silicon, and inexpensive glass substrates. Transmission electron microscopy (TEM) selected area diffraction (SAD) patterns and high resolution micrographs show that the alloys in the intermediate composition range are homogeneously amorphous. The optical absorption spectra show very sharp absorption edges and a systematic shift of the absorption edge energy with composition indicating strong local ordering of the amorphous alloy. The band gap energy has also been confirmed by measurements of photomodulated reflectance, which probes the critical points of the density of states. We have also performed soft x-ray absorption and emission (XAS/SXE) measurements to probe the valence and conduction band density of states and determine the position of the band edges of GaN_{1-x}As_x with various As content. The thermal stability of these highly non-equilibrium alloys is important since device fabrication often requires high temperature processes. We have investigated the stability of these alloys in both furnace anneals and rapid thermal anneals (RTA). The a-GaN_{1-x}As_x films are stable in the amorphous phase for one hour anneals in temperatures up to 600°C. The films are also stable for 700°C-10sec RTAs, but above this temperature the alloy phase segregates into the constituent binary semiconductor phases. The resulting GaAs and GaN nanocrystals are uniformly distributed throughout the film and the relative size of the nanocrystals depends on the initial film composition and annealing conditions. The stability of the amorphous phase also suggests that the cations and anions in the as-grown a-GaNAs alloys are indeed randomly distributed. We will discuss our initial efforts to quantify the local structural order using extended x-ray absorption fine structure (EXAFS).

9:40 AM Student

U5, Band Edge Optical Transitions in Bulk GaSbN and InAsN Dilute-Nitride Materials: *Ding Wang*¹; Stefan Svensson²; Leon Shterengas¹; Gregory Belenky¹; ¹SUNY at Stony Brook; ²Army Research Laboratory

Dilute-nitride GaSbN and InAsN were grown by molecular beam epitaxy on GaSb and InAs substrates, respectively. Photoluminescence (PL) and optical absorption measurements demonstrate strong bandgap reduction with increasing nitrogen incorporation in both materials. GaSbN samples with nitrogen composition ranging up to 1.4% show a redshift of absorption edge by up to 300 meV; while for InAsN, bandgap decreases by approximately 60 meV per atomic percent of nitrogen content. Three times faster bandgap shrinkage in GaSbN indicates stronger interaction between GaSb conduction band edge and nitrogen resonant states. Carrier relaxation lifetimes were studied using an ultra-fast PL up-conversion technique. GaSbN alloys show very short recombination lifetimes in the order of several picoseconds, in accordance with theoretical predictions that GaSbN should have deep nitrogen complex levels in the bandgap. InAsN alloys demonstrate low excitation minority carrier

lifetimes of 8 ns for sample with 1% of nitrogen and about 5 ns for sample with 2% of nitrogen at 77 K. Difference in energetic position of nitrogen complex states can be responsible for the observed difference. At room temperature InAsN with 1% nitrogen content still has a minority carrier lifetime of 2.5 ns. More than three orders of magnitude improvement in minority carrier lifetime as compared to GaSbN encourage development of the InAsN as potential material for mid-IR detector applications.

10:00 AM Break

10:20 AM Student

U6, Non-Monotonic Change/Variation in the Seebeck Coefficient of GaAs_{1-x}N_x Thin Film Thermoelectrics Due to the Addition of N (x = 0.5% to 1.5%): *Paothep Pichanusakorn*¹; Yanjin Kuang²; Prabhakar Bandaru¹; Charles Tu²; Hua Li²; Calvin Patel¹; ¹UCSD-MATS; ²UCSD-ECE

The performance of thermoelectric material is quantified by the figure of merit (ZT). Recent advances have shown that it may be possible to increase ZT of some materials via the dilution of another element with strong electronegativity, whose impurity levels can lead to drastic increase in the density of states of the host material. One such material system is the “dilute nitride”, which consists of III-V semiconductors, such as GaAs or GaP, which has been lightly alloyed with N. Compared to GaAs, the GaAs_{1-x}N_x may have significantly different band structure with a noticeable peak in the density of states. Overall, it was predicted that the inclusion of N should lead to increased effective mass of the density of states, which should then lead to increased Seebeck coefficient (S) and, if the electrical resistivity and thermal conductivity is unchanged, an increase in the ZT as well. Hence, we have sought to investigate the relationship between the atomic percentage of N (N%) and the Seebeck coefficient of GaAs_{1-x}N_x. Specifically, we explored the variation of N content in GaAs_{1-x}N_x in the range of 0.5% to 1.5%, which, to our knowledge, has not yet been investigated. The thin film GaAs_{1-x}N_x (~200 nm thick) was grown by a Gas-Source Molecular Beam Epitaxy on semi-insulating GaAs substrate. Since the Seebeck coefficient also depends on the carrier concentration as well, our samples were grown over a range of N% (0.5-1.5%), but approximately the same concentration (~4.6E17 cm⁻³). The characterization of the materials, which includes the measurement of the resistivity, carrier concentration, mobility, and Seebeck coefficient, was achieved via circuitry that is directly fabricated onto the material via standard photolithography techniques. Our results, in addition to confirming a previously-observed trend that S decreases with small amounts (~ 0.4 atomic %) of added Nitrogen also exhibits new behavior. It was observed that the S shows a minimum around 1% N and then increases at higher N concentrations. This decrease in S at low N% could be due to a reduction in bandgap and the effective mass, while the increase in S at higher N% could be explained by the overlapping of multiple conduction bands, both of which could be predicted through the k.p theory.

10:40 AM Student

U7, GaN_{1-x}Bi_x: Extremely Mismatched Alloys: *Alejandro Levander*¹; Sergei Novikov²; Zuzanna Liliental-Weber¹; Alex Tseng³; Jonathan Denlinger¹; Oscar Dubon³; Tom Foxon²; Junqiao Wu³; Wladek Walukiewicz¹; Kin-Man Yu¹; ¹Lawrence Berkeley National Laboratory; ²University of Nottingham; ³University of California - Berkeley

Semiconductor alloying is a common method for tailoring material properties for specific applications. In the class of semiconductors known as highly mismatched alloys (HMAs) component atoms are partially substituted with isoelectronic elements with very different atomic radius and/or electronegativity. Here we present an extreme case of group III-V HMAs where nitrogen with electronegativity of 3.5 eV and atomic radius of 75 pm is partially replaced with bismuth, which has a much smaller electronegativity of 1.8 eV and much larger atomic radius of 155 pm. Films of GaN_{1-x}Bi_x alloys with x up to 0.11 were grown at the temperature of ~100°C on sapphire substrates using non-equilibrium low temperature molecular beam epitaxy (LT-MBE). The bismuth content increases monotonically with decreasing growth temperature. Although the dominant Bi-containing phase is amorphous however, due to the extreme anion mismatch. X-ray diffraction (XRD) shows a presence of a small number of GaN crystals, possibly distributed throughout

the film. A dramatic reduction in the optical band gap from 3.4 eV in GaN to < 1.2 eV for $x \sim 0.11$ has been qualitatively explained by the formation of a narrow band originating from the band anticrossing (BAC) interaction between localized Bi states and the extended states of the GaN matrix. Lowering the growth temperature further to $\sim 80^\circ\text{C}$ and using the bismuth beam equivalent pressure to alter the Bi content, the GaN crystalline phase was eliminated from the XRD pattern and a completely amorphous $\text{GaN}_{1-x}\text{Bi}_x$ alloy with Bi content of up to $\sim 20\text{-}25\%$ was achieved. A systematic study varying the Ga and Bi flux during growth revealed that a Ga-rich condition was necessary to grow $\text{GaN}_{1-x}\text{Bi}_x$ alloys with III/V ratio = 1. We have also studied the electronic structure of $\text{GaN}_{1-x}\text{Bi}_x$ using soft x-ray absorption and emission (XAS/SXE) to probe the valence and conduction band density of states and determine the position of the band edges. These experiments verify the interaction of localized states introduced by the extremely mismatched Bi atoms with the extended states of the host valence band states. The electronic and optical properties of $\text{GaN}_{1-x}\text{Bi}_x$ will be correlated with the microstructure revealed by transmission electron microscopy studies.

11:00 AM Student

U8, Electrical and Thermal Properties of InGaBi_xAs_{1-x}: *Pernell Dongmo*¹; John Petropoulos¹; Yujun Zhong¹; Joshua Zide¹; ¹University of Delaware

Dilute bismuthides (a/k/a bismides) are a fairly new and promising material for optoelectronics and thermoelectrics in III-V semiconductors. Similar to dilute nitrides, dilute bismuthides exhibit bandgap narrowing due to band anticrossing. In contrast to dilute nitrides, however, most of the band narrowing in dilute bismuthides occurs in the valence band. It has been reported that the bandgap reduces by about 84 meV/%Bi, which is a significant reduction compared to other III-V alloys [1]. The ability to manipulate the bandgap is ideal for new narrow bandgap optoelectronic devices such as lasers and detectors. For thermoelectrics, more specifically thermoelectric power generation (TPG), dilute bismuthides show promise due to bismuth's heavy mass and large atomic cross-section. Applications for TPGs include automobiles, solar cells, and UAVs. In the past, researchers have tried increasing ZT by increasing the thermoelectric power factor (S^2 s) and decreasing the thermal conductivity. Unfortunately, all of these parameters are coupled; increasing the electrical conductivity (σ) decreases the Seebeck coefficient (S) while increasing the thermal conductivity (κ) and vice-versa. The incorporation of nanoparticles into materials has been shown to reduce the thermal conductivity passed the alloy limit due to phonon scattering. Most of the research done in the dilute bismuthide community has been focused on incorporating bismuth into GaAs and finding the ideal growth conditions. Previous work has shown that greater than 10% Bi incorporation is achievable [2][3]. However, there is relatively limited research done on incorporating bismuth into InGaAs, particularly lattice-matched to InP. We present and discuss our progress on epitaxially-grown InGaBiAs on InP (both lattice matched and mismatched) by molecular beam epitaxy. We consider the effects of growth conditions (specifically, substrate temperature, As/III ratio, and Bi flux) on the bismuth incorporation. We also explore the electrical, optical, and structural properties of the films using Hall Effect, spectrophotometry, and x-ray diffraction. Finally, we consider the prospects of these materials for both optoelectronic and thermoelectric devices.

11:20 AM

U9, Incorporation of Bismuth into GaAs and InAs Grown by Molecular-Beam Epitaxy: Aaron Ptak¹; Ryan France¹; ¹NREL

Dilute bismuthides are highly-mismatched alloys that are complimentary to the well-studied case of dilute nitrides. In the dilute bismuthides it is the valence band that is highly perturbed, leading to a giant band gap bowing and a large spin-orbit splitting. For GaAsBi grown on GaAs substrates, this leads to potential applications in high-efficiency solar cells, heterojunction bipolar transistors, spintronics and near-infrared devices. Bismuth can be incorporated into InAs as well, reaching wavelengths much further out in the infrared. Incorporation of Bi into either GaAs or InAs requires growth conditions that are far from ideal for III-V materials. Unusually low substrate temperatures and As/Ga ratios are necessary to get significant Bi into the lattice. Here we present a study of the conditions necessary for Bi incorporation in both GaAs

and InAs. For constant growth temperature and As flux, Bi incorporation in GaAs increases linearly with increasing Bi flux up to at least 14%. Similar Bi fluxes yield approximately equal Bi compositions in both GaAs and InAs. The lattice constant of InBi is not known so a direct comparison cannot be made from x-ray diffraction measurements of the pseudomorphically-strained layers. We also measure the dependence of Bi incorporation as a function of both As flux and substrate temperature using a multi-beam optical stress sensor (MOS) that measures the wafer curvature during growth. This measurement system allows us to map out Bi incorporation for a range of growth conditions during a single growth run. Results generated by MOS agree well with the measured Bi incorporation from individual samples grown under a specific set of growth conditions. We find that Bi incorporation in GaAs is constant at low temperatures and begins to decrease for substrate temperatures above $\sim 330^\circ\text{C}$ with very little Bi incorporating above 350°C . Bi incorporation also falls off rapidly for increasing As flux. Bi incorporation is equal when just slightly above and just slightly below a surface atomic As/Ga ratio of unity. Increasing the As flux above an atomic ratio of ~ 1.8 decreases Bi incorporation to practically zero. Very similar trends are found for InAsBi grown on InAs. The linear incorporation with Bi flux and the temperature dependence described here are in contrast to previously published data on Bi incorporation in GaAs [1]. That study found a saturation of Bi incorporation with Bi flux and a continually increasing Bi content with decreasing substrate temperature.

11:40 AM Student

U10, Highly Mismatched Oxide Alloy for Photovoltaic and Photoelectrochemical Applications: *Marie Mayer*¹; Derrick Speaks¹; Roberto dos Reis¹; Zuzanna Liliental-Weber¹; Kin Man Yu¹; Samuel Mao¹; Eugene Haller¹; Wladek Walukiewicz¹; ¹LBNL

Because of material stability and low cost, oxides are appealing for solar power conversion in photovoltaics and photoelectrochemical cells but are limited by a wide band gaps that are not a good match to the solar spectrum. It is now established that substitution of small fraction of anion atoms with an isovalent element leads to a dramatic restructuring of the valence (conduction) band due to an anticrossing interaction between the localized states of the substitutional ions and the extended valence (conduction) band states of the host semiconductor. Although much work has been performed on III-V and some II-VI Highly Mismatched Alloys (HMAs), not much is known about oxygen rich HMAs. Here, as a first step toward narrowing the band gap of oxides, we report the structural and optical properties of $\text{ZnO}_{1-x}\text{Se}_x$ alloys synthesized by pulsed laser deposition. X-ray diffraction and transmission electron microscopy indicate growth of hexagonal columnar films oriented in the ZnO 0002 direction. No Se inclusions are observed through transmission electron microscopy indicating uniform Se distribution and no phase separation at low compositions ($x < 0.12$). Dilute alloy compositions were measured by both XRD and RBS. Optically, a dramatic red shift of the absorption edge is observed for just small amounts of incorporated Se. The upward movement of the valence band edge is similarly confirmed by x-ray emission and absorption studies. Through use of an electrochemical junction, we show that charge carriers can be extracted using photons with energies as low as 2 eV, dramatically below the ZnO band gap of 3.27 eV. In order to explain the spectral dependence of the absorption coefficients we developed a modified valence band anticrossing (VBAC) model that considers interactions between localized states of the Se atoms and the valence band ZnO host matrix. Fitting the model to the experimental data allowed determination of the energy level of Se as 0.9 eV above the valence band and the VBAC coupling constant as 1.2 eV. Combining these results with previously determined parameters we were able to predict composition variation of the band gap as well as the valence and conduction band offsets in the whole composition range of $\text{ZnO}_{1-x}\text{Se}_x$.

Session V: Organic Photovoltaics and Photoelectrochemical Cells

Thursday AM
June 23, 2011
Barbara

Room: State Street
Location: Univ. of California-Santa

Session Chairs: David Janes, Purdue University; David Gundlach, National Institute of Standards and Technology

8:20 AM Invited

V1, Alkanethiol Island Formation on Single Crystal Zinc Oxide Surfaces: Andrea Yocom¹; Darick Baker¹; Thomas Brenner¹; Heather Hunt¹; Dana Olson¹; Thomas Furtak¹; Timothy Ohno¹; *Reuben Collins¹*; ¹Colorado School of Mines

Zinc oxide (ZnO) has shown promise as a high-mobility, stable electron collector in organic solar cells. In addition, ZnO is an important material for short wavelength lasers, field effect transistors, and sensors. An attractive feature of ZnO is the ease with which it can be fabricated into nanostructures, such as nanorods and quantum dots, which optimizes its function in composite organic/inorganic systems. In these applications it is common to use organic molecules to modify the oxide surface to improve chemical processing, surface stability, interfacial energy alignment, or charge transfer. The details of how these modifications work, however, are not well understood for surfaces and nanostructures processed outside of UHV. Solution modification of ZnO surfaces with alkanethiol molecular layers provides an important example. Alkanethiols have been used to change the magnetic properties of ZnO nanorods, to quench the growth of ZnO quantum dots, and to improve the performance of bi-layer ZnO/poly(3-hexylthiophene) organic photovoltaic devices. The structure and bonding of the alkanethiol layer on ZnO is of particular interest in interpreting all of these results since incomplete monolayer formation may affect each treatment's efficacy. In particular, a complete alkanethiol monolayer forms an insulating layer which would not be expected to improve a photovoltaic device. In this study contact angle measurements, infrared spectroscopy, XPS and AFM have been used in concert to characterize octadecanethiol (ODT) treated single crystal ZnO facets. Before treatment, the crystals were annealed to produce atomically flat terraces on the crystal face with well-defined terminations. We find that ODT forms islands on the oxygen-terminated hexagonal face of ZnO instead of a molecular monolayer as has commonly been assumed. The islands are likely to be self-assembled crystals of zinc dithiolate, which spontaneously form under typical surface treatment conditions. Regions between islands appear to be bare ZnO. Treatment of the Zn terminated hexagonal face results in less thiol on the surface and differences in the type of surface bonding. These results suggest that alkanethiol treatment of polycrystalline ZnO films often used in device studies likely gives rise to inhomogeneous coverage with both ODT islands and exposed ZnO on the surface. Such inhomogeneity is, in fact, observed in AFM studies of sol-gel processed ZnO films and may require reinterpretation of how thiol modifiers influence ZnO interfaces in organic/inorganic devices. Support of the National Science Foundation under grant DMR-0907409 and through the Renewable Energy Materials Research Science and Engineering Center is gratefully acknowledged.

9:00 AM

V2, Improved High Efficiency Organic Solar Cells via Incorporation of a Conjugated Polyelectrolyte Interlayer: *Jung Hwa Seo¹*; Andrea Gutacker²; Yanming Sun³; Hongbin Wu⁴; Fei Huang⁴; Yong Cao Cao⁴; Ullrich Scherf²; Alan J. Heeger Heeger³; Guillermo C. Bazan³; ¹Dong-A University; ²Bergische Universitaet Wuppertal; ³University of California Santa Barbara; ⁴South China University of Technology

The power conversion efficiencies (PCE) of bulk heterojunction (BHJ) solar cells can be increased from 5% to 6.5% by incorporating an ultra-thin conjugated polyelectrolyte (CPE) layer between the active layer and the metal cathode. Poly[N-9'-hepta-decanyl-2,7-carbazole-alt-5,5-(4',7'-di-2-

thienyl-2',1',3'-benzothiadiazole)] (PCDTBT) and [6,6]-phenyl C70-butyric acid methyl ester (PC71BM) were chosen for the photoactive layer. CPEs with cationic poly-thiophenes, in both homopolymer and block copolymer configurations, were used to improve electronic characteristics. The significant improvement in device performance and the simplicity of fabrication by solution processing suggest a promising pathway for improving polymer solar cells with high efficiencies.

9:20 AM Student

V3, A Systematic Approach to Solvent Selection Based on Cohesive Energy Densities in a Molecular Bulk Heterojunction System: *Bright Walker¹*; Arnold Tamayo²; Duc Duong¹; Xuan-Dung Dang¹; Chunki Kim¹; Jimmy Granstrom¹; Thuc-Quyen Nguyen¹; ¹University of California Santa Barbara; ²Colorado School of Mines

We measured the solubilities of two organic semiconductors; 3,6-bis(5-(benzofuran-2-yl)thiophen-2-yl)-2,5-bis(2-ethylhexyl)pyrrolo[3,4-c]pyrrole-1,4-dione (DPP(TBFu)2) and [6,6]-phenyl-C71-butyric acid methyl ester (PC71BM) in a series of solvents. We then used this data to calculate the Hansen solubility parameters of the two materials. The dispersion, polar, and H-bonding parameters of DPP(TBFu)2 and PC71BM were found to be (19.3, 4.8, 6.3) and (20.2, 5.4, 4.5) MPa^{1/2}, respectively, with an error of 0.8 MPa^{1/2}. Based on the solubility properties of the two materials, we were able to select three new solvents (thiophene, trichloroethylene and carbon disulfide) for the DPP(TBFu)2:PC71BM system which, after device optimization, led to power conversion efficiencies up to 4.3%.

9:40 AM Student

V4, Structure-Function-Property Relationships of Diketopyrrolopyrrole-Based Materials for Applications in Solution Processed Organic Solar Cells: *Jason Lin¹*; ¹UCSB

Investing in an alternative renewable and clean energy source at lower prices is in urgent need and has been recognized by several government agencies including the Department of Energy and the National Science Foundation. One such energy source which has the potential to meet all of these requirements is organic solar cells. The use of small molecules in organic solar cells is desirable because they often exhibit long range ordering and can be readily synthesized and functionalized with high purity. My thesis focuses on how conjugation length and alkyl chain length of diketopyrrolopyrrole-based materials influence on the optical and charge transport properties, molecular packing, thin film morphology, and the overall device performance. For all studies, we use [6,6]-phenyl C71 butyric acid methyl ester as an electron acceptor. We use a combination of techniques such as atomic force microscopy to probe surface morphology and donor-acceptor domain sizes, differential scanning calorimeter to measure the glass transition temperature, x-ray diffraction to gauge crystallinity, ultraviolet photoelectron spectroscopy to measure HOMO-LUMO levels, and single charge carrier diodes to study hole and electron mobilities. The results from these studies will provide design guidelines for new generation of diketopyrrolopyrrole-based materials for applications in organic solar cells.

10:00 AM Break

10:20 AM Student

V5, ALD-TiO₂ to Enable Si as a Corrosion Resistant Photoelectrode for Water Oxidation and in Photoelectrochemical Solar Cells: *Yi Wei Chen¹*; Jonathan Prange¹; Marika Gunji¹; Christopher Chidsey¹; Paul McIntyre¹; ¹Stanford University

Efficient and clean fuel synthesis methods have been actively researched in recent years in response to fossil fuel depletion and global warming concerns. By absorbing solar energy with a semiconducting photoelectrode, efficiency enhancement can be achieved for clean fuel production, such as in the case of electrochemically synthesizing hydrogen from water. One can also configure a solar cell with liquid phase photoelectrochemical redox reactions, which has the advantage of active cooling with liquid coolant circulation. To achieve these tasks, however, the photoelectrochemical anode (photoanode) must be able to withstand oxidative biases and harsh pH environments. This

stability requirement has typically limited semiconductor selection to wide bandgap materials, such as TiO₂ (bandgap ~ 3 eV) and Fe₂O₃ (bandgap 2.3 eV). These materials are known to be oxidatively stable semiconductors but very limited in photoabsorption efficiency. Ideally, small bandgap semiconductors (e.g. Si) are desirable photoanodes because of their efficient photoabsorption properties. Such materials are, however, easily oxidized at the potentials required of photoanodes, resulting in either insulating oxide surface passivation or dissolution. In this work, we protect the small bandgap Si with a thin, pinhole-free layer of atomic-layer-deposited TiO₂ (ALD-TiO₂) to create a stable and efficient photoanode. In the case of water oxidation, an ultrathin, optically transparent, Ir layer was deposited on the top to serve as a water oxidation catalyst and electron transfer mediator. This nanocomposite photoanode is stable during continuous water oxidation for periods greater than 24 hours in 1M NaOH, an alkaline solution that would very rapidly oxidizes an unprotected Si electrode. With AM1.5G illumination, a 550 mV photovoltage was obtained, and the onset of water oxidation occurred at ~200 mV below the thermodynamic equilibrium potential, with saturation current density approaching the 36 mA/cm² theoretical limit for AM1.5G illumination of a Si photoanode. The photovoltage approaches the open circuit voltages of the best Si solar cells, while the saturation current density is four to five times larger than the current state-of-the-art Fe₂O₃ electrodes. Electron transport through the protective oxide coating on the Si occurs by tunneling for the thin (2-3 nm) TiO₂ films prepared by ALD. A photoelectrochemical solar cell using the ALD-TiO₂ protected photoanode was also demonstrated with ferri/ferrocyanide solutions as the redox medium. Large open circuit voltages and short circuit currents have been obtained. This ALD-TiO₂ passivation approach is quite general and may be applied to other semiconductor anodes used in water splitting or in other electrochemical reactions.

10:40 AM

V6, Performance Optimization of Branched Nanowire Heterostructure-Based Photoelectrochemical Cells for Water Solar Splitting: *Alireza Kargar¹; Ke Sun¹; Deli Wang¹; ¹UC San Diego*

Hydrogen has high energy density and is very attractive clean fuel, which is currently produced through steam reforming from hydrocarbons (fossil fuels), electrolysis and thermolysis of water, and biomass, etc. Direct water splitting is very attractive as a potentially environmentally clean process, however, it will not be clean in electrolysis and thermolysis processes if the power (electricity and heat) are from coal-burning power plants. On the other hands, direct solar water splitting using photoelectrochemical (PEC) cells promises cost-effective and carbon emission free hydrogen generation and has attracted a lot of interests. The semiconductor photoelectrodes are paramount to the PEC cell performance and hydrogen generation efficiency, and key parameters to consider in design are broad absorption spectrum and effective light absorption, effective charge transfer and energy band matching to H₂ and O₂ energy levels, long-term stability, and high photocurrent (for high photo-to-hydrogen conversion efficiency). Moreover, low-cost materials and easy to fabricate and scale up the photoelectrodes are also important for practical applications. Recently, we have demonstrated a 3-D branched nanowire heterostructures consisting of Si nanowire cores and ZnO nanowire branches, which offer the tunable and optimal properties for efficient light absorption due to light trapping effect, enhanced charge separation, large surface area, and show great promise in high efficiency for PEC electrodes. In addition, this 3-D branched ZnO/Si heterostructure is synthesized by a cost-effective and low-temperature solution based method. In this paper, we report an optimization of cell performance for this unique 3-D structures, particularly with consideration on the three important factors (absorption, photocurrent, and stability). By detail study of different branched structures using various etching and growth times, we show that smaller ZnO nanowire branches on Si nanowire cores provide higher absorption. This can also be confirmed by the change of sample's color with different ZnO nanowire growth times. The photocurrent of diverse 3-D branched heterostructures is compared and optimized, and we demonstrated that smaller ZnO nanowires on longer Si nanowires present larger photocurrent under the illumination due to higher absorption and increased surface area for chemical reactions. Photocurrent variations versus potential are similar to those

reported for TiO₂ coated n-Si nanowire arrays. Furthermore, the cell stability (photocurrent measurement as a function of time in electrolyte) of different branched heterostructures is studied.

11:00 AM

V7, Layer-By-Layer Assembly of Light Harvesting Arrays for Molecular Based Solar Cells: *Peter Dinolfo¹; ¹Rensselaer Polytechnic Institute*

We have developed a new layer-by-layer (LbL) fabrication technique for the controlled growth of molecular multilayer assemblies on oxide and electrode surfaces. The nanoscale thin-film structures have been synthesized using copper(I) catalyzed azide alkyne cycloaddition (CuAAC) as both a means of anchoring the films to the substrate surface and coupling of the individual molecular layers together. The flexibility and versatility of this process permits us to incorporate a wide variety of individual molecular building blocks into the multilayer thin-films. This in turn allows us to target specific electrochemical and photophysical properties for a variety of electro-optical applications including advanced light harvesting arrays for molecular based solar cells. Herein, we describe the optical properties and growth patterns of the films as followed by UV-vis absorption, as well as the electrochemical characteristics as studied by cyclic voltammetry. Additionally, film properties such as thickness and optical constants were characterized by X-ray reflectivity (XRR) and spectroscopic ellipsometry, while surface roughness was determined by tapping mode atomic force microscopy (TM-AFM). The molecular multilayers show consistent growth over tens of layers and moderate ordering in their molecular structure. This molecular LbL system is designed to be fully adaptable and easily tunable, allowing for the rapid adjustment of the optical and electrical properties of the thin film composites. Preliminary photocurrent data is presented for the multilayer sensitization of ITO electrodes in a Dye-Sensitized Solar Cell configuration.

11:20 AM Student

V8, Low Temperature Fabrication of Hybrid Carbon Nanotube Gel as a Counter Electrode for Efficient Dye Sensitized Solar Cells: *Gede Adhyaksa¹; Jin Park¹; Ga Lee¹; Jeung Kang¹; ¹KAIST*

Herein will be reported highly efficient dye-sensitized solar cells (DSSCs) made by hybrid carbon nanotube gels as a counter electrode, in order to tackle the drawbacks of conventional Pt which are relatively expensive and fabricated in the high temperature. The gels was composed of multi-wall carbon nanotube (MWCNT) dispersed in 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide (EMIm-TFSI) ionic liquid electrolyte. Afterward acetonitrile, as a surfactant, was added into the mixture. The mixture fastly had become a gel after applying high voltage in ultra-sonication horn for less than 10 seconds. The gel was then applied on the fluorine tin oxide (FTO) glass by doctor-blade method. A hybrid gel counter electrode was obtained after placing it in the 100 deg C vacuum oven, and ready to be sandwiched for assembling a dye-sensitized solar cells. The role of each component will be discussed according to the result from raman spectrum, XPS, and SEM images. It showed the EMIm-TFSI has played an important role as a conductive binder of MWCNT, and also in making finely entangled nanotube bundles due to its high dielectric properties. The existence of acetonitrile into the void of cross-linking nanotube-bundles has a significant influence in both increasing fill-factor and supporting the solubility of the gel. We utilized 3 different electrolytes, room-temperature ionic liquid (RTIL), MWCNT-RTIL composite, and commercial iodide electrolyte (Solaronix), and the efficiency utilizing this concept was achieved up to 4.3 % under 1.5 AM sun illumination (100mW/cm²). We investigated how the fill factors were proportionally dependent to gel thickness up to 6 μm. Moreover the analysis by ac impedance spectroscopy revealed that even under low temperature fabrication, the hybrid gel has exhibited a remarkable performance as a catalyst on the cyclic redox iodide/triiodide comparable with conventional Pt counter electrode Gel.

11:40 AM V9, Late News

Session W: III-Nitride: Bulk Growth and Epitaxy

Thursday PM
June 23, 2011

Room: Corwin East
Location: Univ. of California-Santa Barbara

Session Chairs: Theeradetch Detchprohm, Rensselaer Polytechnic Institute; Edwin Piner, Texas State University

1:30 PM Student

W1, Shape Transformation of Nanoporous GaN by Annealing: Buried Cavities and Nanomembranes: *Christopher Yerino*¹; *Yu Zhang*¹; *Benjamin Leung*¹; *Jung Han*¹; ¹Yale University

Though GaN has emerged as one of the most important semiconductors of our era, its chemical inertness constrains patterning to rely almost exclusively on dry etching. Recently we reported an electrochemical process to create nanoporous (NP) GaN [1,2], allowing tunability in optical, electrical, and mechanical properties. The present work investigates morphological metastability of the NP medium, which transforms in shape at typical growth temperatures, as explained by models of capillary-driven mass transport. We exploit this property to shape and micromachine GaN into structures or configurations not easily attainable, demonstrating novel, proof-of-concept structures such as buried cavities and nanomembranes. EC etching was carried out in an oxalic acid electrolyte using a voltage-controlled mode [1,2]. The GaN samples containing one or more n-type layers ($N_D = 1-10 \times 10^{18} \text{ cm}^{-3}$) on top of undoped GaN were grown on sapphire by metalorganic chemical vapor deposition (MOCVD). For sample annealing, EC etched samples were cleaned, loaded back into the MOCVD, and heated to 1000 °C in N_2/NH_3 or H_2/NH_3 ambient for up to 1 hour. Previous work on the annealing of porous silicon has shown that lateral merging of the porous volume occurs as does sealing of the porous surface to yield extended voids buried inside the crystal. We observe similar results when annealing NP GaN. A critical porosity is found below which the surface seals and the GaN encapsulates bubble-like voids. By adjusting the porosity beneath the sample surface and annealing, coalescence of the voids was achieved, forming an expansive, plate-shaped void 1 μm wide beneath a 1 μm thick membrane across the entire sample surface (~0.5 cm^2 area), suspended by isolated columns. The annealing results can be understood based on curvature-driven mass transport whereby nanopores partition vertically into voids, which can in turn coalesce laterally. These results were extended to the nanoscale by precisely controlling the porosity profile of the EC etch. The resultant 200 nm thick nanomembrane and the accompanying gap underneath span the entire 0.5 cm^2 sample area. Plan view TEM shows that the nanomembrane is single crystalline, and defect generation due to annealing and regrowth is rarely observed. The demonstrated structures may have significant impact on future GaN technologies. The formation of embedded airgaps opens up exciting possibilities in shaping, releasing, and separating GaN layers, while smaller, discontinuous voids may be used to engineer the index of refraction and light extraction. Device quality nanomembranes may enable novel GaN applications including nanoelectrical-mechanical systems, compliant substrate epitaxy, and flexible electronics. [1] Y. Zhang, S. W. Ryu, C. Yerino, B. Leung, Q. Sun, H. Cao and J. Han, *Phys. Status Solidi b* 247, 1713 (2010) [2] Y. Zhang, Q. Sun, B. Leung, J. Simon, M. L. Lee and J. Han. *Nanotechnology* 22, 045603 (2011).

1:50 PM Student

W2, Bulk GaN Growth on GaN Seeds of Varying Orientations in Supercritical Basic Ammonia: *Siddha Pimpulkar*¹; *Shinichiro Kawabata*²; *James Speck*¹; *Shuji Nakamura*¹; ¹Materials Department, University of California - Santa Barbara; ²Optoelectronics Laboratory, Mitsubishi Chemical Corporation

High-quality, large GaN substrates are needed to produce improved optoelectronic and electronic group-III nitride devices. Current growth rates in the m-plane direction for GaN using the basic ammonothermal method are

currently 4 to 10 times slower than in the c-direction presenting a challenge to produce large non-polar substrates. Methods need to be found to enhance growth rates in both non-polar and polar directions. One method would involve growing on a plane vicinal to a boule facet which remains flat without faceting into two or more slower growing singular facets during steady state growth. The present work attempts to find such a steady state vicinal plane and investigates the effect of vicinality on the growth rates, crystal quality, surface morphology, and impurity incorporation of the ammonothermally grown GaN crystals. This was done by preparing freestanding, HVPE grown, atomically flat GaN substrates with the following nominal surface off-orientations: (10-10) towards (11-20): 0, 2, 3, 4, 5, 10 deg; (10-10) towards (0001): 1, 2, 5, 10, 15, 28, 47 deg; (10-10) towards (000-1): 2, 5, 10, 28, 47 deg; (11-20) towards (0001): 4, 17, 29, 32, 37 deg; (11-20) towards (000-1): 4, 17, 29 deg. The seed crystals were placed into the hot zone of a 25mm diameter René 41 autoclave, along with polycrystalline GaN held in a Ni-Cr mesh basket, which was placed in the lower temperature zone. Baffles were placed in between the two zones along with sodium metal. The autoclave was filled with ammonia and heated to 500-600°C to produce pressures of 150-250MPa. Six growth runs were performed between six and 35 days after which the autoclave was cooled, the ammonia released, and the crystals removed. Upon investigating surface morphologies using SEM various unique growth regimes and features were found. From preliminary analysis, it appears that there may be a window between on axis m-plane and (10-1-1) in which the surface does not facet, yet it remains to be investigated if it remains dominant during extended steady state growth. Additionally, the surface of all five investigated crystals between on axis m-plane and five degrees towards a-plane appear to have a c-axis component off-orientation of one degrees towards (000-1). The crystals were analyzed for crystal quality using XRD and the resulting FWHMs of the ω rocking curves revealed no improvement in crystal quality, yet values closely duplicating the seed crystal quality were found. Growth rates varied depending on the initial growth orientation. Impurity incorporation as a function of seed crystal orientation using SIMS was analyzed and will be presented. Absorption measurements were performed on the (10-10) towards (11-20) series with a clear increase in absorption in the longer wavelengths for the crystals within 10° of (11-20).

2:10 PM Student

W3, Large-Area, Free Standing GaN by an Novel Nanoetching Process and Substrate Recycling: *Yu Zhang*¹; *Qian Sun*¹; *Benjamin Leung*¹; *John Simon*¹; *Minjoo Lee*¹; *Jung Han*¹; ¹Yale University

GaN has emerged, in the past two decades, as one of the most important semiconductors with applications such as solid state lighting and power electronics. Separation and transfer of GaN device layers could produce measureable improvements in light extraction, thermal management, leakage reduction, and strain mitigation. Laser lift-off (LLO) is a relatively established process to separate GaN from sapphire substrates. However, issues such as yield, homogeneity, processing time, and cost make such a process still cumbersome. Lateral undercut etching of GaN has been accomplished with bandgap-selective photoelectrochemical etching in an InGaN/GaN heterostructure, or a conductivity-selective electrochemical etching. A few groups have investigated the growth of sacrificial layers such as AlInN and CrN that are compatible with epitaxial process yet amenable to wet etching. In this work, we present a new scheme in splitting and lifting-off GaN using nanoporous (NP) GaN medium by a simple and robust electrochemical (EC) etching process. This procedure can be considered an implementation of the "smart-cut" principle using nanoscale wet etching and is compatible to wafer-level scaling up. The NP GaN produced by the EC etching offers a new way to selectively weaken the mechanical strength of GaN, making it possible to split and separate epitaxial GaN layer. The use of the nanoetching leads to a flexible process in forming columnar pores during the initial vertical drilling, followed by localized isotropic etching deep in the layer to create lift-off. This procedure can be applied to almost all semiconductors but is especially pertinent to GaN with its given its chemical inertness. We demonstrate that large area (=1 cm^2), free-standing GaN layers, with a thickness from 0.5 to a few microns, can be separated in less than 20 minutes, and the mono-crystallinity of the lift-off GaN

layers is well preserved by this process. The substrate was recycled after large area GaN liftoff. Acknowledgement: Yu Zhang would like to express his thanks to Dr. Zhenting Jiang for help with Raman measurement.

2:30 PM Student

W4, Effect of Strain on Effective Masses in GaN and AlN: *Cyrus Dreyer*¹; Anderson Janotti¹; Chris Van de Walle¹; ¹University of California, Santa Barbara

The characteristics of high-power, high frequency transistors based on GaN/AlGaIn are affected by the presence of strain, which can be unintentionally present due to heteroepitaxial growth or can be intentionally introduced. The strains cause changes to the band dispersion and band gaps of the materials, which can alter device performance. Previous studies have focused on the effects of strain on the band gap of AlN and GaN, but relatively little work has been devoted to investigating the effects on the effective mass. Using first principles calculations based on density functional theory (DFT), we have conducted a systematic study of the effects of biaxial and hydrostatic stress, and the resulting strain, on the band properties of AlN and GaN. In particular we analyze the changes in band gap and electron effective masses with strain. Electron effective masses were determined both parallel and perpendicular to the *c* direction in hydrostatic and biaxial stress configurations. We find that for small strains ($\epsilon_{xx} = \epsilon_{yy} = \pm 0.01$), the band gap and effective mass generally decrease linearly with tensile strain, as expected from nondegenerate k.p theory. A notable exception occurs in AlN in the direction parallel to the *c* direction; in this case, we observe a linear increase in effective mass with tensile strain, which can be explained by a four-band Kane model analysis using k.p theory. This work was supported by NSF and by the UCSB Solid State Lighting and Energy Center.

2:50 PM Student

W5, Quasi Equilibrium Crystal Shapes and Kinetic Wulff Plots of Gallium Nitride Grown by Hydride Vapor Phase Epitaxy: *Benjamin Bryant*¹; Asako Hirai¹; Shuji Nakamura¹; James Speck¹; ¹University of California, Santa Barbara

In this presentation we demonstrate work on developing the kinetic Wulff plots and quasi equilibrium crystal shapes of GaN by hydride vapor phase epitaxy. The pursuit of these was to explore the stable semi polar planes that emerge naturally from the GaN crystals and to also examine the non-polar *a* and *m* plane stability. The kinetic Wulff plots and quasi equilibrium crystal shapes reveal the stable growth planes and features for differing growth conditions. This work is differentiated from previous work of Han et al and Hirai et al by the use of stacking fault free high quality bulk GaN substrates, thus avoiding any constrained features due to stacking fault generation from heteroepitaxy. The difference in these growths can be seen where the numerous stacking faults appear in the slate like morphology of the defective material but smooth facets emerge in the defect free material. These growths were performed by a conventional three zone horizontal growth system on high quality bulk *m*-plane GaN substrates. HVPE was employed due to the growths being closer to equilibrium than MOCVD, thus allowing for truer representation of the plots and equilibrium shapes. A dielectric mask of 140 nm thick SiN_x was employed for the selective area growths. Circular openings of 5 μm diameter, with fill factors ranging from 0.1, 0.2, 0.3, and 0.4 were used to reveal the shapes of the growths. The QECS was shown to have clear *m*-plane facets and a sharp and flat *c*-face. The *c*+ face became faceted with (10-11) planes emerging. This work sheds light on the stable facets of the GaN crystal shape.

3:10 PM Break

3:30 PM Student

W6, In Situ Stress Measurements during GaN Growth on Ion Implanted AlN/Si Substrates: *Jarod Gagnon*¹; Mihir Tungare²; Xiaojun Weng³; Fatemeh (Shadi) Shahedipour-Sandvik²; Joan Redwing¹; ¹Pennsylvania State University; ²The College of Nanoscale Science and Engineering, University at Albany; ³The Materials Research Institute

Ion implantation of AlN/Si substrates has been shown as a viable pathway to reduce the crack density of GaN thin films grown on Si. These substrates consist

of a thin AlN buffer layer grown by metalorganic chemical vapor deposition (MOCVD) on (111) Si followed by N⁺ implantation to form a defective layer at the AlN/Si interface. While the use of this approach reduces residual stress and dislocation density in the GaN films, the mechanism of stress relaxation is not clear. In this study, *in situ* wafer curvature measurements were used to investigate the effect of thermal annealing and GaN growth on substrate curvature and film stress. Post-growth transmission electron microscopy (TEM) was used to study the structural properties of the layers. The starting substrates used for this study consisted of 34nm AlN/Si(111). One substrate was implanted with N⁺ ions at a dose of 2×10^{16} cm⁻² and a range of 105 nm below the AlN/Si interface while the other served as a control and was not implanted. The substrates were annealed for 10 minutes at 1100°C in N₂ at 50 Torr followed by growth of a 1 μm thick GaN film using trimethylgallium, NH₃ (V/III=13,000) and H₂ as the carrier gas. *In situ* stress measurements revealed that for the unimplanted sample, the GaN initiated growth under a compressive stress of 1.35 GPa which arises due to lattice mismatch with the AlN buffer layer. In contrast, GaN growth on the ion implanted sample begins at a lower compressive stress of 0.7 GPa which suggests a reduction in epitaxial stress. In both cases, the compressive growth stress is fully relaxed after ~0.7 μm of growth. During post-growth cooling, tensile stress is introduced in the GaN layer of both samples due to thermal expansion mismatch. Post-growth optical microscopy characterization, however, demonstrated that the ion implanted sample had a lower density of channeling cracks compared to the unimplanted sample. Cross-sectional TEM images revealed the formation of horizontal cracks in the ion implanted region beneath the AlN buffer layer which may provide an additional mechanism of stress relief. The effects of annealing conditions, AlN buffer layer thickness and ion implantation dose on the film stress and structural properties of the GaN layers will also be discussed.

3:50 PM Student

W7, Effect of Indium Surfactant on N-Polar GaN Epilayers Grown by Metalorganic Chemical Vapor Deposition: *Dongjin Won*¹; Xiaojun Weng¹; Joan Redwing¹; ¹The Pennsylvania State University

N-polar GaN has been attracting much attention since it allows for novel design in optoelectronic and high power electronic devices because of opposite polarity to Ga-polar GaN. However, N-polar GaN films grown by metalorganic chemical vapor deposition (MOCVD) generally show hexagonal hillocks which can be reduced through the use of vicinal sapphire or SiC substrates. Although the density of hexagonal hillocks can be greatly reduced by vicinal substrates misoriented from the *c*-axis, MOCVD-grown N-polar GaN films typically exhibit a higher surface roughness than Ga-polar GaN due to macrosteps arising from the substrate misorientation. In an effort to improve the surface morphology and optical properties, the use of indium as a surfactant during N-polar GaN growth was investigated. The GaN layers were grown by MOCVD at 950 °C on C-face SiC substrates miscut by 3.57 degrees towards <11-20>. A 90 nm thick AlN buffer layer was initially deposited on the SiC at 1100 °C. Convergent beam electron diffraction in transmission electron microscopy confirmed that the polarity of the GaN film grown on C-face SiC is N-polar. Atomic force microscopy (AFM) images obtained over a 20×20 μm² area of N-polar GaN grown at 950 °C without indium showed interlaced triangular hillocks pointing towards the <11-20> direction. Due to these triangular features, the root-mean-square (RMS) surface roughness in AFM measurements was as high as 18.1 nm over 20×20 μm² and 6.1 nm in 2×2 μm² areas. When the indium surfactant was introduced during N-polar GaN growth, the triangular hillocks disappeared due to enhanced step-flow growth promoted by indium, thus markedly reducing RMS surface roughness down to 3.5 nm in 20×20 μm² and 0.5 nm in 2×2 μm² AFM images, respectively. Secondary ion mass spectroscopy (SIMS) analysis revealed that growth with an indium surfactant reduced the background C concentration from 1.8×10¹⁸ cm⁻³ to 1.1×10¹⁸ cm⁻³ while it increased unintentional Si doping from 3.7×10¹⁶ cm⁻³ to 9.5×10¹⁶ cm⁻³. Also, the SIMS results indicated that N-polar GaN films were unintentionally doped with oxygen at the level of 1.2×10¹⁹ cm⁻³ regardless of indium surfactant, leading to n-type GaN films. High O background concentrations are commonly reported in MOCVD-grown N-polar GaN films and are considered to originate from the atomic configuration of

the highly reactive N-face GaN. Differences in residual impurity levels result in a modification of the photoluminescence spectra of N-polar GaN grown with indium, enhancing the near-band-edge emission around 364 nm by a factor of 4 and decreasing the yellow luminescence by a factor of 3.8. The results demonstrate that indium is a useful surfactant in improving the surface morphology and optical properties of N-polar GaN films.

4:10 PM Student

W8, Schottky Barrier Height and Interface Chemistry for Metals Contacted to Low Dislocation Density AlGaIn Grown on C-Oriented AlN Wafers: James Tweedie¹; Anthony Rice¹; Ramon Collazo¹; Seiji Mita²; Jinqiao Xie²; Zlatko Sitar¹; ¹North Carolina State University; ²Hexatech, Inc.

Devices based on III-nitrides and their alloys have attracted interest for high temperature and high power applications. In this paper we investigate the Schottky barrier heights and interface chemistry for a collection of representative unannealed metals (Au, Ni, Al, Ti) on high Al mole fraction AlGaIn films. Metal work functions range from 4.3 to 5.1 eV. The low dislocation density 300 nm Si doped n-type AlGaIn films were grown on bulk c-oriented AlN single crystal wafers by low pressure metal organic chemical vapor deposition (MOCVD) in a reactor with a shower-head configuration. Samples were mounted on a Mo puck and top contacted with In to a metal clip to establish an electrical ground through the sample holder. The mounted samples were then transferred ex situ directly to an ultra high vacuum (UHV) system where the surfaces were studied using x-ray photoelectron spectroscopy (XPS). The samples were transferred within the UHV system to an electron beam evaporation chamber where the contact metals were deposited. The samples were then returned to the XPS chamber for further characterization. Using a method developed by Waldrop and Grant, Schottky barrier heights were measured directly by measuring shifts relative to the valence band maximum (VBM) of reference photoelectron lines corresponding to the AlGaIn film at the interface after metal deposition. A series of thicknesses (1 - 15 nm) for each of the contact metals was used to monitor the evolution of the Schottky barrier height. For Au contacts thicker than 6 nm back bending was observed, while for the other metals the reference photoelectron line was extinguished before significant back bending was observed. The Schottky barriers measured by XPS were compared with barriers derived from I-V measurements and were shown to be in good agreement. Samples were characterized ex situ by high resolution x-ray diffraction (HRXRD) to determine the AlGaIn composition and strain state. Fitting the Schottky Barrier height as a function of the work function of the metal, the electron affinity of Al(0.75)Ga(0.25)N was shown to be approximately 3 eV. Furthermore, the Schottky Mott model holds for the metal-AlGaIn interfaces when surface oxidation is limited.

4:30 PM Student

W9, Generation Mechanism of Threading Dislocations in Heteroepitaxial Growth of 2H-AlN on 6H-SiC (0001) Substrates: Hironori Okumura¹; Tsunenobu Kimoto¹; Jun Suda¹; ¹Kyoto University

AlN is one of the most promising materials for deep-ultraviolet LEDs and high-temperature electronics devices. For AlN growth, SiC is one of the most suitable substrates because of the small lattice mismatch (1%) between AlN and SiC. However, for high-quality AlN growth on SiC, issues originating from the polytype difference (2H-AlN on 4H- or 6H-SiC) and initial nucleation must be solved. We have successfully reduced extended defects generated at AlN/SiC interface by controlling the step heights of the SiC substrates to full-unit-cell and introducing Ga pre-deposition for enhancement of initial layer-by-layer growth. The threading dislocation density (TDD) reduced from 10^{10} cm⁻² to 4×10^8 cm⁻². For further reduction of TDD, we must clarify the generation mechanism of the extended defects formed at the AlN/SiC interface. In this study, we investigated the defects in 2H-AlN layers on 6H-SiC substrates in detail. 6H-SiC (0001) Si-face (vicinal angle 0.15°) substrates were treated by high-temperature H₂ gas etching to control the SiC step height to be 6 bilayers (1.5 nm). Just before AlN growth, the SiC surface was exposed to a 2ML-Ga beam as soon as nitrogen plasma ignited. The 300-nm-thick AlN growth immediately started at the growth temperature of 650°C by rf-MBE. Defects in AlN layers were observed by TEM. Most of threading dislocations (TDs) were

arranged in rows. The separation of the TD rows was 500 nm, corresponding to the terrace width of SiC surfaces with 6-bilayer-height steps. TD rows are thought to be generated at the step edges of SiC substrates. The density of TDs generated on the terrace of SiC surfaces was very low, 8×10^7 cm⁻². We believe that the initial layer-by-layer growth by our optimized growth procedure resulted in the dramatic reduction of TDs on the terrace of SiC surfaces. In the tilted view of plan-view TEM, two TDs on terrace drew V-shape structure. This means that TDs form a half loop. When adjacent TDs have oppositional Burgers vectors each other, the twist component of AlN layers can reduce. It was confirmed by very small FWHMs of (01-12) omega-scan, 41 arcsec in XRD. Meanwhile, TD rows at step edges seem to form dislocation networks via step edges. We suppose that the network was generated by coalescence of AlN layers grown on adjacent terrace of SiC surfaces. For further reduction of TDD, it is important to control the coalescence process of AlN over step edges.

4:50 PM

W10, Impact of AlN Wetting Layer on the Strain Development in GaN Layer Grown on Chemical Mechanical Polished 4H - SiC Substrates:

Eunjung Cho¹; Frank Brunner¹; Markus Weyers¹; ¹Ferdinand-Braun-Institut

SiC is the substrate of choice for nitride based microwave or power transistors due to its high thermal conductivity compared to sapphire or Si. However, lattice mismatch and thermal expansion mismatch with nitride materials cause crystalline defects and epiwafer bow. In this study, the wafer bow is focused on. Specifically, the strain development of GaN layers was investigated depending on the MOCVD growth process. 1.5 μm thick uid GaN layers were grown on an AlN wetting layer using 3 inch chemical-mechanical polished semi-insulating 4H-SiC substrates. Growth temperature and thickness of the AlN layer and growth temperature for GaN were varied. During growth, the wafer curvature and surface reflectance were monitored using an EpicurveTT-AR sensor. The effect of the GaN growth temperature on the strain is relatively negligible. Strain was reduced by increasing the AlN wetting layer thickness from 80 nm to 200 nm. It was also found that the AlN growth temperatures significantly impact on the strain in the GaN layer. The comparison was made between 80 nm AlN wetting layers grown at 1300°C (sample 1), 1250°C (sample 2) and with a two-step growth method (sample 3). In the latter method, the growth temperature is initially 1250°C and then ramps to 1300°C. Sample 1 shows the strongest compressive strain, followed by sample 2. Sample 3 has the least compressive strain. The in-situ surface-sensitive reflectance data (405 nm) shows that strain development in the GaN layer is correlated with the surface morphology at the initial stage of GaN growth on an AlN layer. For sample 3, the surface reflectance slowly increases while the reflectance of sample 1 and 2 reaches the maximum value immediately. 50 x 50 μm AFM images of the initial GaN surface (after three minutes GaN growth) confirmed that the surface of sample 3 is rougher than sample 1 and 2 as expected from the reflectance data. Its RMS roughness (σ_{rms}) is 23 nm and the coalescence of GaN was still in progress. On the contrary, the GaN surface of sample 1 is almost closed and flatter ($\sigma_{\text{rms}} = 11$ nm). It indicates that the growth of GaN proceeds longer in the island growth mode on the two-step method grown AlN layer (sample 3) and consequently, the GaN layer is more relaxed with less compressive strain incorporation during the growth. FWHM rocking curve values for the (0002) and (30-32) GaN reflection plane show that the GaN crystalline quality of sample 3 is better compared to the other samples. In summary, strain of GaN layers was engineered by controlling the AlN wetting layer. Compressive strain was reduced and the crystalline quality of GaN was improved by employing a two-step AlN growth method.

Session X: Oxide Thin Films

Thursday PM
June 23, 2011

Room: Corwin West
Location: Univ. of California-Santa Barbara

Session Chairs: John Conley, Oregon State University; Patrick Lenahan, Pennsylvania State University

1:30 PM Student

X1, Gate First $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{Al}_2\text{O}_3$ MOSFETs with In-Situ Channel Surface Cleaning: *Andrew Carter*¹; Jeremy Law¹; William Mitchell¹; Gregory Burek¹; Brian Thibeault¹; Arthur Gossard¹; Mark Rodwell¹; ¹UC Santa Barbara

As scaling of critical dimensions in VLSI becomes difficult, alternatives to silicon are being examined. III-V MOSFETs may provide larger drive currents than silicon at the same equivalent dielectric thickness [1], absent dielectric interfacial defect densities, D_{it} , which degrade subthreshold slope and drive current. While low D_{it} for HfO_2 on InGaAs has been reported [2], this result used an arsenic cap to protect the semiconductor surface from oxidation during the transfer between the wafer growth system and the dielectric deposition tool. We have demonstrated D_{it} similar to [2] cleaning the InGaAs surface with hydrogen and trimethylaluminum (TMA) before Al_2O_3 deposition [3]. This could eliminate the need for an arsenic cap. Here we report first MOSFET results using such channel surface cleaning techniques. An ~ 5.5 nm Al_2O_3 film was grown in an FlexAL ALD at 300 °C using TMA and deionized water as reactants. We performed an in-situ surface preparation on air exposed samples with iterative cycles of hydrogen plasma and TMA. Hydrogen removes native oxides on the channel surface [4]. Interface quality was measured by capacitance-voltage (CV) on 300 nm, $1\text{E}17\text{ cm}^{-3}$ Si-doped n-type InGaAs surfaces. Gate stack deposition may degrade semiconductor-oxide interface properties [5]. Measurements were done on not annealed and annealed tungsten CV dots to determine damage done by gate metal and SiO_2 deposition. Transistor material was grown lattice matched on InP by MBE with the following layer structure: semi-insulating InP substrate, 400 nm undoped InAlAs, 3 nm InAlAs ($1\text{E}19\text{ cm}^{-3}$ and $3\text{E}19\text{ cm}^{-3}$ Si doped n-type), and 10 nm undoped InGaAs. Blanket depositions of W/Cr/ SiO_2 /Cr and subsequent photolithography define a gate stack that is etched by RIE, followed by PECVD SiN_x sidewall deposition and quasi-MEE InAs source-drain regrowth [6]. Finally, devices were metallized using lifted-off Ti/Pd/Au and wet etch mesa isolated. The performance of the depletion mode device ($3\text{E}19\text{ cm}^{-3}$ doping) was comparable to the previous enhancement mode result [6] which utilized arsenic capped material to prevent surface oxidation. The enhancement mode device ($1\text{E}19\text{ cm}^{-3}$ doping) has a reduced current density and transconductance which are due to large series access resistance underneath the sidewalls. For the depletion mode device, series access resistance to the channel does not explain the poor extrinsic transconductance. Future work will include smaller gate lengths and thinner sidewalls.

1:50 PM Student

X2, Structure of Electronic Defects near the SiC/ SiO_2 Interface: *Corey Cochrane*¹; Patrick Lenahan¹; Aivars Lelis²; ¹Pennsylvania State University; ²Army Research Lab

The silicon /silicon carbide system is a compound semiconductor/oxide system which yields reasonably good metal oxide silicon field effect transistors (MOSFETs). It may be useful as a model system in exploring challenges inherent among all compound semiconductor/oxide interfaces. The interface/near interface defects in compound semiconductors are poorly understood. For several years, with several coworkers, we have explored silicon carbide based MOSFETs with electrically detected magnetic resonance (EDMR), [1-4] establishing a connection between a near featureless isotropic EDMR spectrum with $g=2.003$ and deep level defects in the interface/near interface region of SiC MOSFETs. We tentatively linked the spectrum to a silicon vacancy or closely related defect. Through multiple improvements in EDMR hardware

and data acquisition software, we have achieved a very large improvement in sensitivity and resolution in EDMR, which allows us to detect side peak features in the EDMR spectra caused by electron nuclear hyperfine interactions. This improved resolution allows far more definitive conclusions to be drawn about defect structure. We have made high resolution ESMR measurements on a series of SiC transistors prepared under very different processing conditions. The EDMR results show nearly identical side peak structure in all cases, strongly suggesting that the side peaks and central line are associated with the same defect and also strongly suggesting that this defect is widely important in SiC MOSFETs. The high resolution EDMR traces also show a slight but real anisotropy in the spectra. The high resolution EDMR measurements show a strong central line, two comparatively strong near side peaks, and a second pair of much weaker side peaks located twice as far from the central line as the inner side peaks. The conventional EPR literature on large volume SiC samples consistently links a five line spectrum a strong central line, two comparatively strong near side peaks, and a second pair of much weaker side peaks located twice as far from the central line as the inner side peaks to silicon vacancy centers. The SiC MOSFET EDMR interface spectrum follows this pattern, but only qualitatively. Conventional EPR measurements made on large volume samples indicate a spacing between the lines which is less than half of what we observe and also indicate relative amplitudes of the five lines of about 0.04, 0.26, 1, 0.26, 0.04. Our EDMR measurements indicate a center line to inner side peak ratio significantly larger. The discrepancies between our EDMR results and the conventional large volume EPR results could plausibly be interpreted in terms of a rather gross level of disorder near the interface.

2:10 PM

X3, Interface State Density for Positive Band Offset Dielectrics (Al_2O_3 , SiO_2) on GaN: *Ramya Yeluri*¹; Jing Lu¹; Xiang Liu¹; Brian Swenson¹; Umesh Mishra¹; Guangle Zhou²; Huili Xing²; ¹University of California Santa Barbara; ²University of Notre Dame

Dielectric passivation is important to improve the stability and reliability of semiconductor devices and we need to characterize various dielectrics and their interfaces to nitrides accurately to be able to exploit their benefits efficiently. Earlier, Swenson et al [1] have detailed a Photo-Assisted High Frequency CV Characterization Technique for the Ga-polar SiN/GaN interface that gives an accurate value of interface state density (D_{it}) across the bandgap of the dielectric. This technique was later extended to study the interface states at the SiN/AlGaN interface on GaN for Ga and N polar material [2]. This method works very well for dielectrics with negative band offset with respect to GaN, but it needs to be modified for positive band offset materials like SiO_2 , Al_2O_3 , HfO_2 . For positive band offset materials, we observe a small interface state ledge in the CV curve even without shining any light. After exposure to UV, there is a large flatband shift and an enhanced interface state ledge. This is due to the holes generated in bulk GaN accumulating at the dielectric/GaN interface in the presence of a valence band barrier. It is hard to differentiate the positive charge from the excess holes and the positive charge from the interface states. In order to obtain an accurate interface state measurement, we need to remove the excess holes from the interface first. Previously [3], a Schottky (Ni/Au) stack was used as a gate contact at the dielectric/GaN interface to extract the holes accumulated at the interface. The hole contact is biased negative with respect to the other terminals of the capacitor in order to extract the holes. This caused large electric fields in the device leading to high currents through the third contact and eventually, breakdown of the contact. In this work we use a negative band offset dielectric, MOCVD-grown SiN, under the third contact. The SiN allows the excess holes to flow out and prevents high currents flowing through the gate contact. The dielectrics that were studied are Al_2O_3 and high temperature SiO_2 . After UV exposure and hole extraction, we see that the peak measured D_{it} decreases from $2\text{e}13\text{ cm}^{-2}\text{eV}^{-1}$ to $6\text{e}12\text{ cm}^{-2}\text{eV}^{-1}$ with increasing time of hole extraction and saturates at $6\text{e}12\text{ cm}^{-2}\text{eV}^{-1}$. Once all the excess holes are removed, the measured D_{it} saturates and this is the estimated interface state density value. Further studies are under way to optimize the hole extraction and to analyse the flatband shift in the CV curves corresponding to fixed charges in the dielectric.

2:30 PM Student

X4, Comparison of Metal Deposition Methods by CV Analysis of ALD Al_2O_3 on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$: Gregory Burek¹; Andrew Carter¹; Jeremy Law¹; Brian Thibeault¹; William Mitchell¹; Mark Rodwell¹; ¹Electrical Engineering Department UCSB

Alternative channel MOSFET devices show great promise for delivering next generation devices with highly scaled physical areas, operation frequencies and drive currents. A great deal of work has been done to deposit scaled, high-k dielectrics upon alternative channel materials with low densities of interface traps (D_{it}), however, deposition of metal on the films may damage the films, masking the true D_{it} . Specifically, RF magnetron sputtering and electron beam evaporation may lead to radiation damage by exposing the high-k films to ions and high energy photons. In this work, electron beam evaporation, RF magnetron sputtering and thermal evaporation are experimentally compared to examine the role of metallization damage on capacitance-voltage (CV) measurements of a high-k/metal MOSCAP, as deposited and after a Forming Gas Anneal (FGA). Different methods were used to deposit 50 nm of nickel, through a shadow mask, upon 5nm of Al_2O_3 , grown by atomic layer deposition (ALD), on $1 \times 10^{17} \text{ cm}^{-3}$ Si doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, on a commercially available n-InP substrate, with a backside Ti/Pt/Au contact. CV measurements were taken before and after a 1.5 hour, 400 C FGA and are used to evaluate each deposition method. Substantial differences were seen in the frequency dispersion of CV curves in accumulation, depletion and inversion regions, as well as in the slope of the high frequency CV curve, with thermal evaporation giving the best overall result. In addition, an alternative hearth design was examined that allowed for a focused electron beam to be used during the deposition of Ni. A more focused electron beam yielded an order of magnitude faster deposition rate at the same electron current as the previous experiment, minimizing the time of deposition and potentially the radiation absorbed by the sample. CV measurements showed improvement over the traditional electron beam evaporation method in depletion and inversion regions, while frequency dispersion in accumulation and the slope of the high frequency CV curve was comparable. Further experiments were performed in an effort to isolate the damage mechanisms of the deposition methods. High-k films were exposed to deposition processes while covered with commercially available, optical quality lithium fluoride, which allows partial transmission of VUV photons, while blocking soft x-rays, energetic particles and metal deposition. Ni was then thermally evaporated through a shadow mask on the irradiated high-k samples to form MOSCAP structures. CV measurements yielded minimal differences between samples, showing that VUV photons are not responsible for the majority of damage seen in earlier experiments. More research will be necessary to arrive at optimal deposition conditions for scaled devices.

2:50 PM Student

X5, Passivation Effects of ALD Oxides on Self-Aligned $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ /InAs/InP Vertical Tunnel FETs: Guangle Zhou¹; Yeqing Lu¹; Rui Li¹; Tim Vasen¹; Qingmin Liu¹; Wan Sik Hwang¹; Qin Zhang¹; Haijun Zhu²; Jenn-Ming Kuo²; Siyuranga Koswatta³; Mark Wistey¹; Tom Kosel¹; Patrick Fay¹; Alan Seabaugh¹; Huili Xing¹; ¹University of Notre Dame; ²IntelliEPI; ³IBM T. J. Watson Research Center

Tunnel field-effect transistors (TFETs) are under intense investigation for low-power applications because of their potential for extremely low subthreshold swing and low off-state leakage. III-V semiconductors with small effective mass and broken band lineup are considered to be ideal for TFETs in that they promise high on-current and I_{on}/I_{off} ratios. In this paper, we investigate the passivation effects of atomic layer deposition (ALD) oxides on vertical TFETs fabricated using an optical-lithography-only and self-aligned process. This new and simple fabrication approach has been demonstrated for the first time using an $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ /InAs/InP pocket vertical heterojunction. The TFET operation critically depends on the access region from the drain contact as well as the exposed tunnel junction sidewall. As one may speculate, surface oxidation of the thin access region (2 nm InAs and 13 nm InGaAs) when exposed to air can increase the drain contact resistance and access resistance; surface oxidation of the tunnel junction sidewall may also introduce mid-gap states. Indeed, it was observed that without any passivation the drain

current of an $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ /InP TFET at $V_{DS} = 0.5\text{V}$ dropped by three order magnitudes, when measured several days after it was fabricated, compared to that measured immediately after the undercut mesa was formed. On the other hand, devices passivated with ALD oxides were found to be stable. Prior to passivation, these VTFETs showed an on-current at $V_{GS} = 1\text{V}$ of 14 – 22 $\mu\text{A}/\mu\text{m}$, among the highest demonstrated for this material system. A minimum subthreshold swing of about 130 mV/dec was achieved. The drain current on/off ratio was about 10^4 , while the gate leakage was at least two orders of magnitude smaller than the device channel current. After the devices were passivated by 7 nm of Al_2O_3 and 3 nm of HfO_2 deposited using ALD at 300 °C, it was observed that the on current of the VTFET at $V_{GS} = 1\text{V}$ decreased to 3 – 4.8 $\mu\text{A}/\mu\text{m}$ while SS_{MIN} increased to 240 mV/dec and 220 mV/dec at $V_{GS} = 0.5\text{V}$ and 1 V, respectively. It was also observed that the device performance showed no detectable changes after several days, which means that the ALD oxide passivation can indeed prevent surface oxidation of InGaAs effectively. In conclusion, it has been found that the ALD oxide passivation on self-aligned vertical TFETs can effectively prevent InGaAs surface oxidation thus prevent degradation of drain current over time. However, passivation needs to be optimized to minimize device performance degradation. This work is supported by the Nanoelectronics Research Initiative (NRI) through the Midwest Institute for Nanoelectronics Discovery (MIND).

3:10 PM Break

3:30 PM Student

X6, Influence of Trimethylaluminum (TMA) Exposure on the Growth and Electrical Characteristics of $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ Gate Stacks: Yontae Hwang¹; Varistha Chobpattana¹; Roman Engel-Herbert²; Susanne Stemmer¹; ¹University of California, Santa Barbara; ²Pennsylvania State University

Achieving low interface trap densities and low equivalent oxide thicknesses are still considered major challenges in the development of III-V MOSFETs. Numerous studies have investigated the influence of surface treatment prior to high-k deposition on these parameters. Here we investigate the influence $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surfaces exhibiting different surface reconstructions with trimethylaluminum (TMA) prior to HfO_2 gate dielectric deposition using chemical beam epitaxy. Interface trap densities and Fermi level efficiency of the gate stacks were analyzed using the conductance and Terman methods. Surfaces of As-decapped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layers on (001) InP were exposed to TMA for short times at substrate temperatures between 200 and 300 °C. The growth surfaces were monitored using reflection high-energy electron diffraction (RHEED). It is shown that the TMA dose, exposure time and substrate temperature critically influence the electrical properties of the gate stack, despite that fact that the TMA exposure was sufficiently short to have no apparent influence on the surface reconstructions seen in RHEED. For (2x4) reconstructed $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surfaces TMA acted as surfactant, allowing for the growth of thin, coalesced HfO_2 films using hafnium tert-butoxide as the source. These stacks could be scaled to equivalent oxide thicknesses of less than 1 nm. Without prior TMA exposure the HfO_2 films grew columnar and were not coalesced up to 30 nm in thickness. For low TMA doses and in combination with post-deposition anneals in forming gas, interfaces with an unpinned Fermi level were obtained, showing a band bending corresponding to more than half of the band gap of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ [1]. For higher substrate temperatures and longer TMA exposure times, a much more pronounced midgap interface trap response was observed. For these stacks, the Fermi level was pinned near midgap even after forming gas anneals. For the group-III-rich, (4x2) reconstructed $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surfaces, TMA had no effect on the growth of HfO_2 films and did not act as a surfactant. We will discuss the mechanisms by which TMA and forming gas control the interface trap densities and Fermi level (un) pinning. [1] Y. Hwang, R. Engel-Herbert, N. G. Rudawski, S. Stemmer, *Effect of post-deposition anneals on the Fermi level response of $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ gate stacks*, *J. Appl. Phys.* 108, 034111 (2010).

3:50 PM Student

X7, Investigation of Electrode Roughness and High-K Dielectric Barrier on Metal-Insulator-Metal Tunnel Diode Operation: *Nasir Alimardani*¹; E. Cowell¹; John Wager¹; John Conley¹; ¹Oregon State University

Metal-insulator-metal (MIM) based tunneling devices have been proposed as an alternate approach to high-speed hot electron transistors [1], infrared (IR) detection [2], liquid-crystal display (LCD) backplanes, optical rectennas for IR energy harvesting, and general macroelectronic applications [3]. The operation of a MIM diode is based on quantum mechanical tunneling through a thin dielectric barrier positioned between two metal electrodes. Since tunneling probability depends exponentially on the thickness of the barrier and the uniformity of the electric field, the performance of a MIM tunnel diode should depend strongly on the roughness and uniformity of the MIM interfaces. Despite investigation by many groups over the years, progress towards commercialization of MIM electronics appears to have been hindered by inattention to electrode roughness and the lack of available highly uniform deposited oxides. Most previous experimental work has been performed on native dielectrics produced by oxidation or nitridation of crystalline metals. Recently, we showed that use of the amorphous metal ZrCuAlNi as an ultra-smooth bottom electrode in combination with high quality dielectrics deposited via atomic layer deposition (ALD) enabled the fabrication of high quality MIM tunnel diodes [4]. In this work, we investigate the impact of bottom electrode roughness and various high-k dielectric tunnel barriers on MIM tunnel diode performance. Atomic force microscopy (AFM) revealed a wide variation in roughness between bottom electrodes made from blanket films of ZrCuAlNi (sputtered, RMS ~0.3 nm), Pt (sputtered, RMS ~ 2 nm), Pt (evaporated, RMS ~ 5 nm), and Ir (evaporated, RMS ~11 nm). Current density versus electric field (J - ξ) measurements were made on a series of MIM devices with Al top electrodes, 10 nm Al₂O₃, and grounded ZrCuAlNi, Pt, or Ir bottom electrodes. Theoretically [5], the magnitude of the Fowler-Nordheim tunneling current at large positive fields ($V_{app} > \phi M_2$) should be in reverse order of increasing bottom metal electrode workfunction (ZrCuAlNi: $\phi M = 4.7$ eV; Ir: 5.1 eV; Pt: 5.3 eV). Instead, it was found that the Ir diode achieved significant measured current density at the lowest field, followed by Pt, and then ZrCuAlNi, in order of decreasing electrode roughness. In addition, we found that the percentage of working devices trended lower and J - ξ hysteresis trended higher with increasing roughness. Taken together, these results strongly suggest that bottom electrode roughness can dominate the electrical properties of MIM tunnel diodes. While rough bottom electrodes make it extremely difficult to obtain working devices, high-quality MIM tunnel diodes were obtained using smooth bottom metal electrodes in combination with thin Al₂O₃, ZrO₂, and Ta₂O₅ dielectrics deposited via ALD – using ZrCuAlNi we were able to make uniform and repeatable devices down to 12 ALD Al₂O₃ cycles, ~ 1 nm thick.

4:10 PM

X8, Co-Sputtering of Barium Strontium Titanate (BST) and Barium Oxide-Boron Oxide Flux (BaO-B₂O₃) for Thin Film Applications: *Peter Lam*¹; David Harris¹; Jon-Paul Maria¹; ¹North Carolina State University

Barium strontium titanate (BST) thin films have been widely used for thin film capacitor applications. For example, in RF devices, the strong non-linear response of the permittivity with an applied external bias allow for a direct tuning of the frequency response of an LCR circuit. It has been shown that the dielectric response of the BST is directly correlated to the quality of the crystal, and for conventional ceramic processing high thermal budget is generally required to approach bulk-like properties. For thin film applications the set of substrates compatible with high thermal processing are limited due to chemical, i.e. formation of secondary phases, and mechanical instabilities such as cracking and delamination. Potential enhancement of the crystal structure at a lower temperature can be achieved by addition of a flux with a lower melting point than the sintering temperature of the ceramic. When melted, the flux serves as a medium for enhancing the crystal growth of the matrix ceramic providing lower thermal pathways for crystal densification. For this study we investigate a flux composed of 58% wt B₂O₃ and 42% wt BaO. This composition exhibits a melting temperature of about 869°C, the lowest for this baria-boria system. The films were grown on sapphire via co-

deposition in a dual magnetron gun system in an argon atmosphere at room temperature. The flux content was controlled by adjusting the deposition rates of both guns in order to obtain the target concentration. Several flux contents were tested and the resulting films were annealed in air atmosphere at 900°C for 1 hr. The films were characterized using AFM and X-ray diffraction. Electric properties were measured using interdigitated capacitors fabricated on top of the films and measured with an impedance analyzer. Preliminary results show a substantial increase of the grain size in the flux modified BST films up to certain concentration. Grain growth is generally correlated with enhanced crystal structure and dielectric properties [1]. Moderate grain growth can be observed with increased flux content. With 5% wt flux content the films exhibited large grain growth up to 2 micron. However the grain size was non-homogeneous. More optimizations are required to achieve homogeneous grain sizes across the films. Barium Titanate films grown in PLD by our group have shown enhanced electric performance directly correlated to homogeneous grain growth. Our experiments will aim to reproduce the same results in BST films using co-sputtering.

4:30 PM Student

X9, Solution-Processed Zirconium Oxide and Integration with Zinc-Tin Oxide Thin-Film Transistors: *Chen-Guan Lee*¹; Ananth Dodabalapur¹; ¹University of Texas at Austin

High-k dielectrics have been widely employed in field-effect transistors (FETs) to realize low power consumption. Material deposition with solution-based approaches has been studied to achieve low fabrication cost and high throughput. Here, we present the effect of annealing temperature on the properties of solution-processed ZrO₂ dielectric. Material deposition on glass and flexible substrate are demonstrated. An ultralow subthreshold slope (74 mV/decade) is observed when employing a thin ZrO₂ dielectric in a zinc-tin oxide (ZTO) thin-film transistor (TFT). To study the property of the solution-processed ZrO₂ dielectric, a metal-insulator-metal structure was employed. The substrate was glass coated with 40 nm of Au_{0.6}Pd_{0.4} and the ZrO₂ precursors were deposited in a nitrogen environment followed by thermal annealing in the ambient air. The ZrO₂ precursor solution was synthesized with a sol-gel method by dissolving zirconium chloride [ZrCl₄] and zirconium isopropoxide isopropanol complex {Zr[OCH(CH₃)₂]₄•(CH₃)₂CHOH} powders (0.25 M each) in 2 methoxyethanol. Prepared precursor solution was spin-coated at 2000 rpm for 1 min and converted to ZrO₂ by thermal annealing in air for 1 hr. Three annealing temperatures, 500°C, 400°C and 300°C, were studied. The deposition process was repeated once to form a dual-layer structure. 100 nm of Al was deposited as top metal electrodes. The resulted capacitance values for devices with annealing temperatures of 500°C, 400°C and 300°C are 250, 225 and 150 nF/cm² at a measuring frequency of 1MHz. The tunneling current density depends on the annealing temperature and is less than 100 nA/cm² at 10 V for devices with annealing temperatures of 500°C and 400°C. XPS spectra of the films with different annealing temperatures are almost identical, for which the elements of zirconium and oxygen have an atomic molar ratio close to 1:2 and no chloride element was detected. This indicates the precursors were fully converted to the oxide form and suggests that the ZrO₂ films can be processed at a temperature equal or less than 300°C, which makes it possible for depositing ZrO₂ on flexible substrates, such as Kapton films. AFM images of the ZrO₂ surface shows all the films have a root-mean-square average roughness (R_q) less than 1 nm, which is very smooth for solution-processed dielectrics. A smooth dielectric surface is critical for a well behaved FET since the dielectric/semiconductor interface can affect the interfacial trap density and related FET behaviors, including stability and subthreshold slope. By employing the solution-processed ZrO₂ in a field effect transistor, the operation voltage and subthreshold slope can be significantly improved. We demonstrate a ZTO TFT with a 35 nm ZrO₂ dielectric having an operation voltage of 2 V and a subthreshold slope of 74 mV/decade.

4:50 PM

X10, Epitaxial LaAlO₃/SrTiO₃ Heterostructures by Atomic Layer

Deposition: Nick Sbrockey¹; Michael Luong¹; Eric Gallo²; Jennifer Sloppy²; Guannan Chen²; Christopher Winkler²; Stephanie Johnson²; Mitra Taheri²; Jonathan Spanier²; Gary Tompa¹; ¹Structured Materials Industries, Inc.; ²Drexel University

Oxide heterostructures, consisting of a polar oxide such as LaAlO₃ and a non-polar oxide such as SrTiO₃, offer a novel route to fabricating high speed, nano dimension devices. At a critical film thickness for the polar oxide, a 2-dimensional electron gas (2DEG) can form at the interface, which can be switched from a metallic state to an insulating state. This opens the possibility of building nanoscale devices, for memory and logic applications, based on oxide heterostructures. Prior research on LaAlO₃/SrTiO₃ heterostructures was done using films deposited by pulsed laser deposition (PLD). In this work, Atomic Layer Deposition (ALD) is used to deposit the active materials. ALD has several advantages for fabricating these structures, including excellent control of film thickness, uniformity and stoichiometry. This paper describes the development of ALD processes for LaAlO₃ films on both silicon and TiO₂ terminated (100) SrTiO₃ single crystal substrates, using trimethyl aluminum and lanthanum i-propylcyclopentadienyl for the metal precursors, and water as the oxidizer. Excellent control of film thickness and uniformity is demonstrated at a substrate temperature of 300 C. Control of the La/Al stoichiometry in the film was achieved by adjusting the relative number of La to Al vapor source pulses. The LaAlO₃ films were amorphous in the as-deposited state, as evidence by the lack of x-ray diffraction peaks. The films recrystallize on annealing to form epitaxial LaAlO₃/SrTiO₃ heterostructures, as evidenced by high resolution TEM and electron diffraction. The epitaxial LaAlO₃/SrTiO₃ heterostructures showed electrical conductivity, which turns-on at a thickness of around 3 unit cells for the LaAlO₃ film, in agreement with results reported for similar structures prepared by pulsed laser deposition. The atomic layer deposition process is shown to provide a simple, reliable and flexible means to fabricate epitaxial LaAlO₃/SrTiO₃ heterostructures, and should ultimately be valuable for eventual production of oxide based nanodevices.

Session Y:

Point, Defects, Doping and Extended Defects

Thursday PM
June 23, 2011

Room: Flying A
Location: Univ. of California-Santa Barbara

Session Chairs: Andrew Armstrong, Sandia National Laboratories; Emre Gur, Ohio State University

1:30 PM

Y1, The Influence of Al Composition on AlGa_N Point Defect Incorporation:

Tania Henry¹; Andrew Armstrong¹; Andrew Allerman¹; Mary Crawford¹; ¹Sandia National Laboratories

Successful use of AlGa_N alloys for ultraviolet (UV) optoelectronics involves understanding and mitigating the impact of point defects. We studied defects that dominate unintentionally-doped (UID), coherently-strained Al_xGa_{1-x}N (x=0-0.33) films grown under conditions applicable to laser diode (LD) quantum wells, barriers and wave-guides. The evolution of deep level defect energy (E_o) and defect density (N_t) were quantitatively tracked versus x using deep level optical spectroscopy (DLOS). To maintain coherently-strained heterolayers, nanoscopic UID-Al_xGa_{1-x}N/n-GaN [x= 0.08 (30 nm), 0.22 (25 nm), 0.33 (15 nm)] films were grown on GaN:Si by metal-organic chemical vapor deposition, and Schottky diodes fabricated for DLOS analysis. The combined effect of polarization charge and doping strictly limited DLOS sensitivity to defects in the AlGa_N capping layers. DLOS was performed at 300K with a Xe lamp source coupled to a monochromator. The photocapacitance transient due to optical excitation of deep levels determined E_o, and steady-state photocapacitance determined N_t. Defects in n-GaN:Si films were characterized to verify differentiation between AlGa_N and GaN-

related defects in the heterostructures. Ga_N deep levels at E_c-<2.3 eV, 2.5 eV and 3.31 eV were observed. Conversely, emergent defect levels identified in the Al alloys were E_c-2.2-2.8 eV (L1), E_c-2.8-3.17 eV (L2), and a near-valence band (E_v) level, E_c- 3.31-3.74 eV (L3). N_t increased with x for L1, L2 and L3. L2 is suspected to be related to the cation-vacancy (V(cation)), and its N_t shows the strongest dependence on x (7.5E15 to 1.8E16/cm³). The V(Al) is likely to form in Al_xGa_{1-x}N as its formation energy decreases with x. Additionally, oxygen-related V(cation) are shown to have reduced formation energies in Ga_N, and are expected to show similar behavior in AlGa_N, where excess oxygen incorporation with Al is likely. Regarding the evolution of E_o with x, the suspected V(cation) appears to track the vacuum level, while L3 seems to deepen with respect to E_v. Increased N_t and a greater mid-gap defect concentration with increasing x in Al_xGa_{1-x}N have implications for reduced radiative efficiency in the active region of LDs, whereby increased carrier compensation in the cladding layers can divert carriers away from the active region of the device. This work was supported by Sandia's Solid-State Lighting Science Energy Frontier Research Center, sponsored by the Department of Energy Office of Science. Sandia National Laboratories is a multi-program laboratory operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under Contract DE-AC04-94AL85000.

1:50 PM Student

Y2, Hybrid Functional Calculations of DX Centers in AlN, GaN and

AlGa_N: Luke Gordon¹; John L. Lyons¹; Anderson Janotti¹; Chris G. Van de Walle¹; ¹University of California, Santa Barbara

The group-III nitride semiconductors have many important commercial applications in optoelectronic devices. They are also candidates for fabricating ultraviolet light-emitting devices (LEDs), which could replace gas lasers and mercury lamps for applications such as air and water purification, disinfection and high-resolution photolithography. To achieve high-efficiency UV lasers and diodes, bulk AlN substrates and high Al-content AlGa_N alloys will likely be required, along with a better understanding of the role of defects and impurities in AlN. Several theoretical studies on AlN have been published; however, the majority of these used traditional density functional theory (DFT) functionals, such as the local density approximation (LDA) or the generalized gradient approximation (GGA). These methods severely underestimate the band gaps of semiconductors, which leads to large uncertainties in the position of defect transition levels and formation energies. In this work, we employ a state-of-the-art hybrid functional, developed by Heyd, Scuseria, and Ernzerhof (HSE), which includes a portion of Hartree-Fock exchange. This method gives accurate band gaps and lattice parameters, and allows for much more accurate calculations of defect transition levels, albeit at a significantly greater computational cost. One of the outstanding problems in the study of AlN and high Al-content AlGa_N is the formation of so-called DX centers, also encountered in GaAs and AlGaAs, which consist of donor impurities that self-compensate by turning to acceptors as the Fermi level approaches the conduction band. We use the HSE functional to analyze the electrical properties of oxygen, silicon and germanium donors in AlN and Ga_N, and evaluate the possibility of DX center formation. For the oxygen impurity, we find a stable DX center in AlN and a metastable center in Ga_N, in agreement with previous theoretical and experimental results. However, the structure of the defect differs from previous GGA calculations. By using linear interpolation, we predict at what Al concentration oxygen transitions from shallow donor to DX behavior in Al_xGa_{1-x}N alloys. In the case of the Si and Ge donors, a stable DX center is found for both impurities in AlN. As before, transition concentrations are determined, and the structure of the defect is studied. This work was supported by NSF, by the UCSB Solid State Lighting and Energy Center and by the Institute for Energy Efficiency.

2:10 PM Student

Y3, Deep Traps in M-Plane GaN Grown by Ammonia MBE: Zeng Zhang¹; Christophe Hurni²; Aaron Arehart¹; James Speck²; Steven Ringel¹; ¹The Ohio State University; ²University of California Santa Barbara

III-Nitrides grown along non-polar orientations, e.g. m-plane [10-10] and a-plane [11-20], are attracting great attention, due largely to mitigation of the Quantum Confinement Stark Effect, leading to increased internal quantum efficiency. However, due to differences in growth surface structure, the change in crystal growth orientation could also affect intrinsic and extrinsic defect formation, which can impact device properties. To date, information on traps in non-polar nitrides is relatively sparse. Hence, here we are exploring the influence of crystal orientation on trap incorporation within m-plane GaN grown by ammonia-based molecular beam epitaxy (MBE) utilizing Deep Level Optical Spectroscopy (DLOS) and Deep Level Transient Spectroscopy (DLTS). To isolate the impact of crystal orientation, c-plane and m-plane GaN substrates, with dislocation densities of $\sim 1 \times 10^6 \text{ cm}^{-2}$ and $\sim 1 \times 10^9 \text{ cm}^{-2}$, respectively, were "co-loaded" in the MBE chamber followed by identical epitaxial growth. P⁺-n structures were grown to support capacitance-based DLOS/DLTS, with Mg doping of $1 \times 10^{20} \text{ cm}^{-3}$ and Si doping of $1 \times 10^{17} \text{ cm}^{-3}$, to provide sensitivity to the n-side of the junction. However, C-V revealed that the Si-doped layer of the m-plane sample possessed a higher effective doping concentration of $\sim 1 \times 10^{18} \text{ cm}^{-3}$, which was correlated with SIMS data that revealed a higher oxygen incorporation, which act as residual donors, as has been observed in earlier work on m-plane GaN.^[1] By fitting the DLOS optical cross sections, three traps were revealed in both samples at Ec-1.3eV, Ec-2.6eV and Ec-3.3eV. These levels closely match earlier reports for point defects associated with interstitial carbon, gallium vacancies, and C_N substitutionals, respectively.^[2] Steady state photo-capacitance showed that the traps at Ec-2.6eV and Ec-3.3eV possess nearly two orders of magnitude higher concentration in m-plane ($3.2 \times 10^{16} \text{ cm}^{-3}$ and $2.3 \times 10^{16} \text{ cm}^{-3}$) GaN versus c-plane ($6.5 \times 10^{14} \text{ cm}^{-3}$ and $9.0 \times 10^{14} \text{ cm}^{-3}$) GaN. Similarly, DLTS results also suggest that the m-plane n-GaN layer has a higher concentration of Ec-2.6eV state, which for DLTS appears as a hole trap at Ev+0.8eV, and was observed only in the m-plane sample. Since the dislocation density of the m-plane substrate is \sim two orders of magnitude lower than that of the c-plane substrate, this trend cannot be ascribed to dislocation density. The likely source for the increased defect incorporation may be related to differences in surface growth dynamics for these crystal orientations, although due to the higher oxygen donor concentration for the m-plane sample, the influence of the Fermi level on defect formation energy cannot be discounted. We are currently exploring this in greater detail with respect to systematically varied growth parameters, especially ammonia flux, and this will be reported in a comparative fashion for both crystal orientations.

2:30 PM

Y4, Intrinsic Surface States and Dislocations at GaN(10-10) Surfaces Investigated by Scanning Tunneling Microscopy: Holger Eisele¹; Lena Ivanova¹; Svetlana Borisova²; Mario Dähne¹; Philipp Ebert²; ¹Technische Universität Berlin; ²Forschungszentrum Jülich GmbH

Group-III nitrides are the materials of choice for optoelectronic devices in the green to ultraviolet wavelength range. Recently, the question arose, whether the growth of GaN based devices could be improved by switching from the polar (0001) growth surface to the non-polar ones. For non-polar GaN surfaces only little is known about the exact energetic positions of surface states, and thus their possible influence on the Fermi level. Furthermore, GaN still suffers from high dislocation densities, far above that of zincblende type III-V semiconductor crystals. Dislocations are detrimental for optoelectronic applications of GaN, because dislocations act as non-radiative recombination centers. Therefore we investigated the GaN(10-10) cleavage surface by cross-sectional scanning tunneling microscopy (XSTM) and spectroscopy (XSTS). We were able to identify the energetic positions of the intrinsic surface states and the Fermi level. We found that both, the filled N-derived and empty Ga-derived dangling bond states are outside the fundamental band gap, the latter one being 0.1 – 0.2 eV above the conduction band minimum. The observed band gap is 3.4 ± 0.2 eV, in agreement with the nominal bulk value. The observed Fermi level pinning of about 1.0 eV below the conduction band edge

is attributed to a high defect density at the surface, but not to intrinsic surface states. It is concluded that for defect free GaN(10-10) surfaces the Fermi level is unpinned and determined by the bulk doping. Furthermore, at large scan range XSTM images we were able to identify dislocations, forming localized bunches of entangled non-parallel dislocation lines. Within these bunches the dislocation density reached values of $1.2 \times 10^8 \text{ cm}^{-2}$. Two different dislocation types were found, uncharged perfect dislocations with $a/3 \langle 11-20 \rangle$ Burgers vectors and negatively charged Shockley partials with $a/3 \langle 10-10 \rangle$ Burgers vectors and a related intrinsic type-2 stacking fault. This stacking fault could be identified as ...ABABCACA... stacking sequence, thus inserting one monolayer of cubic GaN within the wurtzite crystal. These measurements show that GaN epitaxial structures can be well investigated by cross-sectional scanning tunneling microscopy.

2:50 PM

Y5, Defect Characterization of InGaN Layer by Deep Level Transient and Optical Spectroscopies: Emre Gur¹; Sriram Krishnamoorthy¹; Zeng Zhang¹; Siddharth Rajan¹; Steven Ringel¹; ¹Ohio State University

There has been great interest in GaN and related alloys due to their superior properties compared to many semiconductors, such as high breakdown field, good thermal conductivity and high electron saturation velocity. While Al_xGa_{1-x}N is important for power devices and deep ultraviolet emitters, In_xGa_{1-x}N alloys with band-gaps ranging from 0.7-3.4 eV covering the entire visible spectrum are of interest for many future optoelectronic and energy applications. In addition, high In composition In_xGa_{1-x}N alloys also possess significant potential for high speed device applications due to small effective mass and high mobility. For all such device applications, device characteristics and performance are greatly impacted, and degraded, by the presence of variety of growth related defects. This study focuses on the presence and electronic properties of deep levels in InGaN materials grown by nitrogen plasma-assisted molecular beam epitaxy (PAMBE). PAMBE was used to grow 300 nm thick, undoped In_{0.2}Ga_{0.8}N layer on an n-type GaN template. The In_{0.2}Ga_{0.8}N composition was confirmed by high resolution triple-axis X-ray diffraction measurements. Schottky diode (SD) properties of semitransparent Pt(8nm) and Au(4nm)/Ag(4nm) metals on In_{0.2}Ga_{0.8}N were investigated and defect characterization was performed using capacitance deep level transient spectroscopy (DLTS) and deep level optical spectroscopy (DLOS), which together make possible deep levels detection throughout In_{0.2}Ga_{0.8}N band-gap. From I-V characterization of the SDs, it is shown that Au/Ag/In_{0.2}Ga_{0.8}N SDs have lower reverse current density, higher barrier height ($\phi_b = 0.67 \text{ eV}$), and lower ideality factor ($n=2$), compared to Pt diode produced in this study and Pt SDs in the literature[1]. C-V measurements show that the In_{0.2}Ga_{0.8}N layer has an n-type background doping concentration of $6 \times 10^{17} \text{ cm}^{-3}$. DLTS measurements displays two electron traps (E_{t1} and E_{t2}) peaking at 227 K and 384 K for 10 s^{-1} rate window, respectively. Defect energies and capture cross section values of the E_{t1} and E_{t2} levels were determined to be Ec-0.39eV, $1.24 \times 10^{-16} \text{ cm}^{-2}$ and Ec-0.91eV, $6.28 \times 10^{-14} \text{ cm}^{-2}$, respectively, with nearly identical concentrations of $1.2 \times 10^{15} \text{ cm}^{-3}$. In order to probe the defect states located in the lower half of the band-gap, DLOS measurements were performed using a monochromatized Xe lamp with photon energies between 1.2-3.6 eV. Analysis of the DLOS optical cross sections revealed three additional defect levels, with energies of at 1.4, 1.76 and 2.5 eV below the conduction band. The concentrations of those deep levels are 1.33×10^{15} , 3.15×10^{15} and $6.13 \times 10^{16} \text{ cm}^{-3}$, respectively. In this work, we have demonstrated Au/Ag/In_{0.2}Ga_{0.8}N SDs and used it for studying the deep levels throughout In_{0.2}Ga_{0.8}N band-gap. Five deep levels were observed throughout the band-gap of the In_{0.2}Ga_{0.8}N. Full details of these 5 traps in InGaN, their possible role in carrier compensation, and their relation to possible physical sources, will be further described.

3:10 PM Break

3:30 PM Student

Y6, Misfit Dislocation Formation in Partially Strain-Relaxed (11-22) Semipolar InGa_N: *Po Shan Hsu*¹; Erin Young¹; Alexey Romanov¹; Kenji Fujito¹; James Speck¹; Shuji Nakamura¹; ¹Materials Department, University of California, Santa Barbara

Semipolar orientations of wurtzite GaN are promising for long wavelength, high performance laser diodes (LDs) because of their reduced QCSE and higher theoretical gain. However, design of LD epitaxial structure on semipolar planes is unique in comparison to nonpolar and polar planes due to the possibility of forming stress-relieving misfit dislocations (MDs) at highly strained hetero-interface(s). The on-set of strain-relaxation in zinc-blende semiconductors occur via lateral glide of pre-existing threading dislocations (TDs). Such TD glide can occur similarly in semipolar wurtzite GaN as a result of the nonzero resolved shear stress on the inclined basal plane. The magnitude of the resolved shear stress is a function of the semipolar plane inclination angle with respect to the basal plane—which is a maximum for basal planes inclined ~45 degrees and decreases with increasing inclination angle. As a consequence, critical thicknesses for MD formation have been observed to vary for different semipolar orientations. In particular, the semipolar (11-22) plane (*c*-plane inclination ~58°) has been observed to have very low critical thickness in comparison to other semipolar planes such as the (20-21) plane (*c*-plane inclination ~75°) [1]. This is likely the key limiting factor in achieving stimulated emission in electrically-injected green (11-22) LDs. However, a better understanding of MD formation in semipolar GaN may provide lucrative opportunities in device design through proper dislocation control. In this work, we investigate strain-relaxation of (11-22) InGa_N on GaN as a function of indium composition (fully coherent to partially relaxed). The samples were grown by metal-organic chemical vapor deposition (MOCVD) on nominally on-axis semipolar (11-22) free-standing GaN substrates. All samples were characterized by cathodoluminescence (CL) and X-ray diffraction (XRD). Partially strain-relaxed (11-22) samples exhibited one-dimensional arrays of MDs along the crystallographic [1-100] direction when analyzed under panchromatic CL. The on-set of strain-relaxation detected by CL correlates well with Matthews Blakeslee's criterion for critical thickness—suggesting MDs are formed via TD glide. Further analysis under monochromatic CL at the substrate (365 nm) and InGa_N peak, showed a single substrate TD associated with every MD. Symmetric reciprocal space maps (RSMs) along the [11-2-3] direction exhibited minimal detectable epi-layer tilt. This indicates a lower detection limit for strain-relaxation using X-ray diffraction, and is likely among the reasons why reported critical thicknesses for MD formation are higher than that calculated using Matthews Blakeslee's equilibrium criterion.

3:50 PM Student

Y7, Observation of *m*-Plane Slip and Relaxation Orthogonal to the Projected *c*-Direction in (20-21) InGa_N/GaN Partially Relaxed Layers: *Matthew Hardy*¹; Feng Wu¹; Po Shan Hsu¹; Ingrid Koslow¹; Erin Young¹; James Speck¹; Steven DenBaars¹; ¹UC Santa Barbara

Despite recent progress, the performance of green light emitting diodes (LEDs) and laser diodes (LDs) is much lower than equivalent devices emitting in blue or violet regimes. Green emitting active regions are grown under very high strain – 3% for In_{0.3}Ga_{0.7}N, degrading crystal quality and leading to large piezoelectric induced electric fields in the quantum wells. Stress relaxation also limits the composition and thickness of InGa_N waveguiding layers in LDs. *c*-plane slip has been observed on (11-22) and (20-21) semipolar orientations, which have significant resolved shear stress on the *c*-plane. An available stress relaxation mechanism which preserves the crystal quality of overlying layers opens up the possibility of growing relaxed InGa_N buffers to reduce the strain in overlying InGa_N layers. However, successful growth of such layers requires understanding the stress relaxation mechanism orthogonal to *c*-plane slip. A series of samples was grown by atmospheric MOCVD on free standing (20-21) GaN substrates. The layer composition was held constant at In_{0.076}Ga_{0.924}N and thickness was varied among 60, 90 110 and 150 nm. The samples were characterized by cathodoluminescence (CL), reciprocal space mapping (RSM)

and TEM. CL images show the onset of *c*-plane slip in the 60 nm sample, in the form of short, low density misfit segments. At 90 nm the onset of formation of dark lines inclined relative to the projected *c*-direction is observed. These dark lines become more dense in the 110 nm sample and fully dense in the 150 nm sample. RSM measurements for the 150 nm sample were taken for 201 symmetric, 203 and 3-21 asymmetric reflections. The 201 RSM indicated a layer tilt of 0.51°, corresponding to a degree of relaxation of 0.33 assuming only *c*-plane slip. The 203 and 3-21 RSMs showed in-plane relaxation of $\Delta q_{||}/q_{||} = 0.018$ and 0.013, respectively. Plan view TEM showed misfit lines parallel to *a* and inclined with respect to the projected *c*-direction. Cross sectional analysis confirmed the presence of misfit dislocations, all with a Burger's vector of $1/3 \langle 11-20 \rangle$. The inclined lines observed in CL and plan view TEM appear to be parallel to $[-2116]$. This corresponds to the intersection of (20-21) and inclined *m*-planes, suggesting these lines are misfit dislocations generated by slip on inclined *m*-planes. As confirmed by the RSM measurements, such a system can relax stress in both orthogonal directions and appears to dominate once the Peierls force opposing slip on *m*-plane relative to *c*-plane is overcome by the lack of any alternative stress relaxation mechanism in the orthogonal direction. We have observed the progression of stress relaxation by slip on the *c*-plane to slip on the *m*-planes and shown that this new slip geometry is effective in relaxing stress orthogonal to *c*-plane slip.

4:10 PM Student

Y8, Stress Mapping Analysis by Ray Tracing (SMART): A New Technique for Residual Strain/Stress Measurement of Single Crystal Material Using Synchrotron White Beam: *Vishwanath Sarkar*¹; Balaji Raghothamachar¹; Michael Dudley¹; ¹SUNY at Stony Brook

Synchrotron X-ray topography is a well established characterization tool for analyzing defect structures and strain in single crystal materials. We have further extended this method to quantitatively measure the residual strain and stress in any single crystal material. This is achieved by the modified technique of synchrotron X-ray topography, where a grid made out of X-ray absorbing material is placed in the path of incident or diffracted beam. By applying the principal of ray tracing to the recorded topographs, all the six components of strain and stress tensor has been calculated and mapped over the entire area of the crystal. This novel non-destructive method of stress measurement can prove to be an invaluable tool for both single crystal manufacturers and users. Single crystal substrates are subjected to a series of processes including cutting, polishing, thermal treatment, brazing, soldering and finally encapsulation in a package during device fabrication. These processes introduce internal or residual strain/stress in the crystal which are not only detrimental to the performance of the device but also can ultimately lead to device failure. Synchrotron X-ray topography method is a powerful non destructive characterization tool for imaging 1-D, 2-D or 3-D defects in nearly perfect single crystals. In our current research we have attempted to measure residual strain and stress in single crystal silicon or in general any single crystal material and mapped it over the entire crystal surface area. For this purpose we used the principle of X-ray reticulography along with the ray tracing technique. In the experimental setup, single crystal material is placed on a goniometer and is aligned such that the surface of the crystal is perpendicular to the incident X-ray beam. A fine grid made out of X-ray absorbing material is placed in the path of incoming X-ray beam, which effectively splits the beam into multiple micro-beams. Diffraction pattern of the entire crystal is recorded at a specific specimen film distance. Each of the microbeam after interacting with the particular region in the crystal is diffracted by a specific plane(s). Combination of all the diffracted microbeams constitute a topograph called reticulograph. Distortion recorded on the reticulographs represents strain or the distortion in the crystal lattice plane. A non-destructive method to calculate residual stress level within the crystal is an invaluable tool for single crystal device manufacturers. We have devised a non-destructive, non-invasive method using X-ray diffraction imaging technique, Stress Mapping Analysis by Ray Tracing (SMART), to fully determine the state of stress and strain within the crystal. Strain and stress maps generated from different single crystals will be presented and discussed.

4:30 PM Student

Y9, Charged Basal Stacking Fault (BSF) Scattering in Wide Band-Gap Semiconductors: Aniruddha Konar¹; Tian Fang¹; Nan Sun¹; Debdeep Jena¹; ¹University of Notre Dame

GaN-heterojunction based high-electron mobility transistors (HEMT) has paved the way towards high speed, high power electronics. Though the built-in polarization field in polar-GaN polarization field plays a negative role due to quantum confined Stark effect. GaN grown in polar direction cannot be used in bipolar devices due to unavailability of hole doping. Moreover, polar GaN-based MOSFET suffers from low threshold voltage. So the recent trend is to explore optical and transport properties of GaN grown in non-polar (m or a plane) direction. However, hetero-epitaxial, non-polar and semi-polar nitrides films grown on lattice-mismatched substrates contain a large number of basal stacking faults (BSFs) parallel to the [0001] direction. In this work we developed a theory of charge transport in bulk nitride semiconductor in the presence of BSFs. Recent density functional theory based calculation and transmission microscope imaging (TEM) revealed that BSFs in wurtzite (WZ) nitrides is of the II-type requiring lowest energy of formation and a BSF can be thought as a thin zincblende (ZB) layer (up to three monolayers thick) perfectly inserted in the WZ matrix without broken bonds as shown in Fig 1a). The built-in polarization difference between ZB and WZ structures will result in bound sheet charges $\pm sp$ at each interface of the BSF layer. Band bending in the BSF region results in a thin barrier and a quantum well (QW due to band-gap difference between WZ and ZB structure) as shown in Fig. 1. For charge transport perpendicular to the BSF layer the carriers has to tunnel through this barrier and QW and then diffuses in the intermediate region between two BSFs. Assuming this barrier and QW are of delta-function like, we developed a tunneling based theory in conjunction with diffusive Boltzmann transport formalism for charge transport in the presence of BSFs. The theory is applied to p-doped m-plane GaN thin films. For the diffusive part of the transport formalism, we included i) ionized impurity scattering, ii) neutral impurity scattering and iii) polar optical phonon scattering. The transport anisotropy predicted by our theory is in agreement with recent experiments as shown in Fig 2. We also discussed two critical limits of carrier concentration, one where transport across a basal stacking fault ceases and another, where the presence of basal stacking faults can be ignored in the context of charge transport.

4:50 PM Student

Y10, Hydrogen-Related Cathodoluminescence in Mg-Doped GaN: Reid Juday¹; Kewei Sun¹; Alec Fischer¹; Fernando Ponce¹; Hee Jin Kim²; Suk Choi²; Jeomoh Kim²; Mi-Hee Ji²; Jae-Hyun Ryou²; Russell Dupuis²; ¹Arizona State University; ²Georgia Institute of Technology

We have observed that low-energy electron beam irradiation (LEEBI) generates strong luminescence in the near-bandgap region in Mg-doped GaN annealed in a hydrogen-containing ambient. This emission resembles that of basal plane and prismatic faults in GaN. The samples used for this study were grown by metalorganic chemical vapor deposition (MOCVD) and consist of a 1 μm -thick Mg-doped GaN film on a 2.5 μm -thick undoped GaN epilayer on sapphire. As is required for hole conductivity in MOCVD-grown Mg-doped GaN, a post-growth thermal anneal was performed to activate the Mg acceptors. A single wafer was grown, cut into pieces, and annealed under different conditions: one in N_2 and one in $\text{N}_2(95\%)/\text{H}_2(5\%)$ ambients. Both samples were annealed for 3 minutes at 850 $^\circ\text{C}$. Secondary ion mass spectrometry gives a Mg concentration of $3\text{-}4 \times 10^{19} \text{ cm}^{-3}$. The room temperature CL shows that the difference in luminescence between the samples is a low-energy, blue band. This band is evident in the N_2 annealed sample at around 2.74 eV with a FWHM of 450 meV. As multiple spectra are taken at the same location, this band undergoes a large blue-shift as well as almost complete quenching of the intensity. Two common explanations for large blue-shifts in luminescence experiments are large-scale potential fluctuations and the commonly observed donor-acceptor pair (DAP) power-dependent blue-shift. Both of these can be safely eliminated as there is no change in the electron beam power during this experiment. The sample annealed in N_2/H_2 does not exhibit this band under the same experimental conditions. Low power CL at 4.5 K shows both samples exhibit nearly identical spectra; both an acceptor-bound exciton at 3.455 eV

and the well-established DAP at 3.289 eV are evident. However, after an electron dose of $1.2 \times 10^8 \text{ e}^-/\mu\text{m}^2$, two additional recombination pathways appear in the sample annealed with hydrogen present. These are attributed to excitons bound to defects in the sample. Their CL energies, 3.41 and 3.38 eV, are similar to energies seen emitted from non-polar a-plane GaN and are attributed to basal plane and prismatic plane stacking faults, respectively. While it may be unlikely that the electron beam is creating stacking faults, it is possible that the defects are already present, yet not initially luminescent; or, these centers are caused by the migration of intrinsic or extrinsic defects through the N_2/H_2 annealed sample.

Session Z: Epitaxial Materials and Devices I

Thursday PM
June 23, 2011

Room: Lobero
Location: Univ. of California-Santa Barbara

Session Chairs: Christine Wang, Massachusetts Institute of Technology, Lincoln Laboratory; Charles Lutz, Kopin Corporation

1:30 PM Student

Z1, Growth of Epitaxially-Embedded ErAs Films in GaAs: Adam Crook¹; Hari Nair¹; Domingo Ferrer¹; Seth Bank¹; ¹University of Texas at Austin

We present a new method for growing heterostructures of semimetallic ErAs in GaAs that appears to avoid the formation of antiphase domains which have historically plagued the ErAs/GaAs material system. With traditional epitaxial growth, antiphase domains nucleate in the GaAs overgrowth of ErAs films, due to the mismatch in rotational symmetry between the rocksalt ErAs and zincblende GaAs. We leverage the recent discovery that, below a critical areal density during growth, surface erbium adatoms will preferentially incorporate into subsurface ErAs nanoparticles. As compared to traditional layered heterostructure growth, this method offers the advantage that a thin layer of GaAs floats on the surface and remains registered to the substrate, preventing antiphase domain formation during subsequent III-V growth. Samples were grown by solid-source molecular beam epitaxy in a Varian Gen II system. The growth method consisted of: (a) growth of an ErAs nanoparticle layer which was overgrown with GaAs. (b) The substrate was heated to 600 $^\circ\text{C}$ and an erbium flux was initiated; the erbium diffused through the GaAs capping layer to the underlying ErAs nanoparticles, displacing gallium and growing the ErAs into a full film. (c) The ErAs film continued to grow vertically through the GaAs cap layer, which was used to seed the subsequent growth of III-V layers, mitigating antiphase domain formation. To verify this growth mechanism, ErAs films were grown with varying GaAs cap thickness and characterized with in situ reflection high energy electron diffraction (RHEED) and ex situ transmission electron microscopy (TEM). Imaging was performed with a 200 kV FEI Tecnai TF20 instrument, equipped with a Schottky field emitter (zirconium oxide coated tungsten tip), and X-twin objective lens. TEM analysis was obtained with the sample aligned to the nearest $\langle 110 \rangle$ zone axis of the substrate. Spherical Aberration (Cs) free high angle annular dark (HAADF) field and bright field (BF) Scanning-TEM (STEM) images were acquired using a JEOL JEM-ARM200F attaining information transfer to $<0.1 \text{ nm}$. TEM images of ErAs films grown with conventional MBE are compared with ErAs films grown by nanoparticle-seeded growth. The conventionally grown films exhibited antiphase domains in TEM images and severely degraded RHEED during GaAs overgrowth. By contrast, the films grown by nanoparticle-seeded growth did not exhibit antiphase domains in the overgrown GaAs. These results demonstrate the ability to suppress antiphase domain formation by growing ErAs films through a GaAs cap that remains registered to the underlying substrate. We will discuss critical growth parameters, particularly the importance of the GaAs cap thickness, on the film and overgrowth quality. This provides a potential path towards epitaxial plasmonic devices containing multiple metallic layers.

1:50 PM Student

Z2, Improved Conductivity of GaAs-Based Tunnel Junctions Containing ErAs Nanostructures via Compositional Grading: *Rodolfo Salas*¹; Erica Krivoy¹; Adam Crook¹; Hari Nair¹; Seth Bank¹; ¹University of Texas at Austin

Low-loss tunnel junctions are essential components of a number of optoelectronic devices and are particularly important for serially connecting the junctions of multijunction solar cells and minimizing electrical/optical losses in vertical-cavity surface-emitting lasers. The tunneling barrier in band-to-band tunnel junctions depends on the bandgap of the materials and the depletion layer thickness. Decreasing the bandgap reduces the tunneling barrier, enhancing the conductivity; however, the resulting increase in optical absorption can degrade device performance. On the other hand, reducing the tunneling distance by increasing the doping concentration shortens the depletion region and improves the conductivity; however, this approach is limited by dopant activation. Placing semimetallic ErAs nanoparticles at the pn junction greatly enhances tunneling currents by breaking the band-to-band tunneling process into two smaller back-to-back Schottky tunneling barriers. Modifying the ErAs nanoparticle size and density provides a route to further enhance conductivity. Additionally, the Schottky barrier height between ErAs and III-V's has been found to be tunable by varying the III-V composition, which provides the motivation for this work. Here, we investigate the combined benefits of compositional grading of the n-side Schottky barrier and ErAs nanoparticle-enhancement to produce an optimized Schottky barrier configuration, while only modestly increasing undesirable optical absorption. Samples were grown in a Varian Gen II molecular beam epitaxy (MBE) system on n-type GaAs (100) substrates, under identical conditions to the best devices reported. Abrupt junctions with and without nanoparticles at the interface were grown and compared to graded junctions. For the graded structures, GaAs was digitally graded to In_{0.5}Ga_{0.5}As on the n-type side in five steps of 2 nm each. The p-side of the tunnel junction was not modified. It is important to note that although the InGaAs graded region has a smaller bandgap than GaAs, these layers are quite small as compared to the absorption depth of InGaAs and do not increase the loss significantly. Through compositional grading, we observed an improvement in the conductivity, as compared to the abrupt ErAs junction. The enhancement was as much as 7x in the forward bias, but was more modest under reverse bias. Experiments are currently underway to better understand the dichotomy between the performance under forward and reverse bias. This work is a proof-of-concept that tunnel junction conductivity can be further enhanced with band engineering. Future work could include the use of lattice-matched dilute-nitrides for grading the n-type side and mixed arsenide-antimonide-nitrides for the p-type side. These combined enhancements in ErAs tunnel junctions have the potential to further improve photonic device performance.

2:10 PM Student

Z3, Photoluminescence from the Direct Bandgap of Ge_{1-x}Sn_x Alloys Grown by Molecular Beam Epitaxy: *Robert Chen*¹; Hai Lin¹; Yijie Huo¹; Suyog Gupta¹; Krishna Saraswat¹; Ted Kamins¹; James Harris¹; ¹Stanford

Recent advances in synthesizing high-quality Ge_{1-x}Sn_x alloys have generated much interest due to the ability to highly engineer a column-IV alloy with favorable predicted properties, including high carrier mobility (>10⁵ cm²/V·s) [1], tunable lattice constant (for straining subsequent epitaxial layers, such as MOSFET channels and Ge layers) [2-4], and a direct-bandgap crossover point [2,5,6]. However, many of these properties require a Sn composition that is many times larger than the ~1% solid solubility in Ge. Sn alloying also increases the lattice constant of the alloy, making growth on a fixed lattice increasingly difficult with higher Sn percentages. In order to overcome these issues, we grow our Ge_{1-x}Sn_x alloys on GaAs (100) wafers with lattice-relaxed InGaAs buffer layers using low-temperature molecular beam epitaxy to control the degree of strain. While the main applications of these alloys are in CMOS-compatible devices on Si, our InGaAs buffers provide us with an incredible amount of freedom in both controlling the epitaxial lattice constant while maintaining high distinguishability in optical measurements due to its large bandgap difference with Ge_{1-x}Sn_x. InGaAs buffers of up to 20% In are mostly relaxed and have been shown to effectively control the strain of epitaxial layers

[7]. Our Ge_{1-x}Sn_x layers are grown at low temperatures of around 200°C and with thicknesses of ~300nm. After growth, we perform an oxide strip using both HCl and HF immediately followed by a rapid thermal annealing at 550°C - 650°C for 30s under a forming gas ambient with the goal of passivating surface states and reducing point defects. After annealing, our samples show Sn compositions of up to ~4.5% Sn as determined by x-ray photoemission measurements. Room-temperature photoluminescence spectra were taken on our samples using a doubled Nd:YAG laser at 532nm using a standard lock-in technique. Due to the predicted shrinking of the bandgap with Sn alloying, we use a thermoelectrically-cooled extended InGaAs detector with a 3dB rolloff at 2.5µm. Our samples show that as we increase the Sn percentage, the direct bandgap of Ge shifts from 0.8eV down to around 0.55eV with the addition of Sn, nearing the predictions of the direct-gap crossover point (which can be as low as around 6.5% Sn). In our presentation, we will further discuss these results and also show how tensile strain can be used to further achieve direct bandgap.

2:30 PM

Z4, Fabrication and Characterization of Whispering Gallery Mode (WGM) Microdisk Resonator Based on Epitaxially Grown GeSn: *Seongjae Cho*¹; Robert Chen¹; Hai Lin¹; Yijie Huo¹; Gary Shambat¹; Jelena Vuckovic¹; Theodore Kamins¹; Byung-Gook Park¹; James Harris¹; ¹Stanford University

Whispering gallery mode (WGM) resonators are superior to conventional dielectric resonators in advanced RF circuits, optical communication systems, and biosensing technologies by virtue of their high Q-factor and its invariance at high frequency and both TE and TM mode operation. There have been intensive research efforts on novel materials and processing for silicon-based integrated photonics and optoelectronics. GeSn is considered one of attractive approaches due to its higher carrier mobility, energy bandgap tunability, and integrability on silicon via proper buffer materials. In this work, a WGM microdisk resonator based on epitaxially grown GeSn was successfully fabricated and its optical characteristics were investigated. An In_{0.16}Ga_{0.84}As buffer layer and Ge_{0.96}Sn_{0.04} were grown on a GaAs substrate by molecular beam epitaxy (MBE) in sequence without exposure to air. Thicknesses were 350 nm and 220 nm, respectively. The 350 nm buffer layer was grown in two segments: first, a 250 nm layer of In_{0.16}Ga_{0.84}As was grown, followed by an anneal at 540 °C for 20 min to minimize the defects caused by lattice mismatch. This was followed by growing an additional 100 nm of In_{0.16}Ga_{0.84}As. The growth temperature for Ge_{0.96}Sn_{0.04} alloy was 175°C. The device active region was defined by Cr lift-off process and dry etch. Subsequently, the GaAs was chemically etched by H₂O:H₂O₂:H₂SO₄ = 8:1:1 solution for 20 s at room temperature without stirring. This undercut etch process provides confinement for the optical modes to the disk perimeter and minimizing coupling to the substrate. Light signals were transmitted through a polished optical fiber tapered down to have a diameter of 1 µm in a contact with the fabricated devices. Transmission loss was defined as the difference between intensities of input and output signals at the source and the analyzer, respectively. Three local minima were observed at λ₁ = 1430 nm, λ₂ = 1560 nm, and λ₃ = 1680 nm. Confinement of an optical mode by total internal reflection (TIR) begins at λ₁ = 1430 nm but the absorptions at λ₁ and λ₂ are weak due to material loss. The bandgap edge is predicted to be near 1600 nm judging from a drastic decrease in the curve. The characteristics wavelengths reveal the consecutive integer numbers at which TIRs in the fabricated device occur: 14, 15, and 16 by recursive calculations with effective diameters.

2:50 PM Student

Z5, Raman Study of Strained Ge_{1-x}Sn_x Alloys: *Hai Lin*¹; Robert Chen²; Yijie Huo²; Theodore Kamins²; James Harris²; ¹Materials Science and Engineering; ²Electrical Engineering

Ge_{1-x}Sn_x alloys have been of growing interest, because it is a possible route to develop totally group IV based optoelectronic materials systems. Unstrained Ge_{1-x}Sn_x alloy is predicted to exhibit a direct band gap, starting with x around 10%. Moreover, the presence of tensile strain is expected to decrease the Sn composition needed than unstrained alloys. Therefore, the ability to determine the strain ϵ and the Sn composition x , is of crucial importance. Raman

spectroscopy is a very powerful technique for this purpose because the optical phonon modes of the alloys are strongly affected by x and e . However, the strain and composition contributions are not decoupled. Other research groups published the composition dependence of Raman frequency of $\text{Ge}_{1-x}\text{Sn}_x$ alloys, but they corrected the strain contribution using coefficients for Ge. In our work, the strain of $\text{Ge}_{1-x}\text{Sn}_x$ alloys is controlled by growing on top of InGaAs buffer layers, whose lattice constants could be changed by In composition. XRD reciprocal space mapping of symmetric (004) and asymmetric (224) diffraction peaks of $\text{Ge}_{1-x}\text{Sn}_x$ alloys were carried out to determine the in plane and out of plane lattice constants. From the measured lattice constants, the $\text{Ge}_{1-x}\text{Sn}_x$ alloy composition and strain can be obtained applying a self-iterative simulation based on the elastic constants, which is assumed to change linearly with composition in the same manner as the lattice constant. From XRD data, we conclude that the strain of the $\text{Ge}_{1-x}\text{Sn}_x$ alloys ranges from -0.2% to 0.8%, and the Sn composition x ranges from 1% to 10%. Raman scattering experiments were performed at room temperature in the backscattering directions using 532 nm green Laser for the same set of samples. The Raman spectra of $\text{Ge}_{1-x}\text{Sn}_x$ alloys consist of one strong peak corresponding to Ge-Ge Longitudinal Optical (LO) mode. For $\text{Ge}_{1-x}\text{Sn}_x$ alloys of the same Sn concentration, this peak progressively shifts toward lower energy and broadens with increasing strain. The frequency shift with respect to the value for bulk Ge, $\omega_{\text{Ge}}=300\text{cm}^{-1}$, follows the linear relationship $\Delta\omega=\omega-\omega_{\text{Ge}}=be$, where e is the in plane strain. By comparing the Raman shift and the strain data from XRD, the coefficient b is determined as $-(570\pm 7)\text{cm}^{-1}$. This coefficient is purely for strain contribution. After deducting the strain contribution from total Raman peak shift using this coefficient, the coefficient of the composition dependence of Raman frequency of $\text{Ge}_{1-x}\text{Sn}_x$ alloys is calculated. The value is $-(80\pm 5)\text{cm}^{-1}$. This value is closed to the value from literature, $-(75.4\pm 4.5)\text{cm}^{-1}$.

3:10 PM Break

3:30 PM

Z6, Study of Molecular Beam Epitaxial Grown HgCdSe for Infrared Applications: *Gregory Brill*¹; Yuanping Chen¹; Priyalal Wijewarnasuriya¹; ¹U.S. Army Research Laboratory

The Army Research Laboratory has recently initiated research on the growth and characterization of HgCdSe material by molecular beam epitaxy (MBE). HgCdSe is an infrared material that can be engineered to detect any wavelength of infrared (IR) light by controlling the Cd composition within the alloy. This compound is completely analogous to the much more common II-VI IR material HgCdTe, except that large area, scalable, and lattice matched substrates are commercially available for HgCdSe, specifically, GaSb and InAs substrates. This is a potential advantage over HgCdTe material as current and future infrared focal plane array (IRFPA) sizes and formats are currently outpacing the physical size of bulk CdZnTe substrates used for HgCdTe material growth, severely limiting next generation IR technology. Initial work on the HgCdSe material system was conducted 30 years ago and focused on bulk grown material and electrical properties. A decade later, MBE growth of HgCdSe was first investigated, but did not address the use of scalable III-V substrates for growth. At this time, there is very little in the literature regarding HgCdSe material by MBE and nothing related to the use of a lattice matched III-V substrates. In this work, we will report on the first ever growth of HgCdSe on GaSb substrates by MBE and compare results to HgCdSe grown on ZnTe/Si, which was also conducted in this study. A systematic study of MBE growth temperature and material flux ratios were varied to ascertain the best growth conditions. HgCdSe defect structures were examined as a function of growth temperature with smooth, defect-free HgCdSe surface morphologies obtained using a growth temperature much lower than HgCdTe for comparable material fluxes. X-ray rocking curve measurements were also made to ascertain the overall crystalline quality of the material. To date, the best HgCdSe/GaSb double crystal rocking curve measurements resulted in a full width at half maximum of 180 arcsec. Transmission electron microscopy (TEM) was used to investigate the epilayer - substrate interface with electron diffraction showing aligned crystal structures between the HgCdSe epilayer and the substrate, as expected. FTIR data shows a linear relationship between the Se/Cd flux ratio

and cut-off wavelength and indicates the easily tunable nature of the alloy. Additionally, an investigation into the electrical properties of HgCdSe will be discussed with an emphasis on Hg saturation conditions during the annealing process.

3:50 PM Student

Z7, XMCD Measurement of Molecular Beam Epitaxy γ' -Fe₄N Thin Films on LaAlO₃(100) and MgO(100) Substrates: *Keita Ito*¹; GeunHyong Lee¹; Kazunori Harada¹; Mao Ye²; Yukiharu Takeda³; Yuji Saitoh³; Takashi Suemasu¹; Akio Kimura²; Hiro Akinaga⁴; ¹University of Tsukuba; ²Hiroshima University; ³JAEA; ⁴AIST

Ferromagnetic γ' -Fe₄N has potential interest for application to spintronics devices because the spin polarization of electrical conductivity at the Fermi level was calculated to be -1.0. In addition, γ' -Fe₄N has a relatively small lattice mismatch of 1.3% to Si(100). Thus, γ' -Fe₄N is considered an appropriate material for application in spin injection electrodes to Si(100). However, the magnetic moments of γ' -Fe₄N remain unclear from an experimental point of view. The saturation magnetization per volume (M_s) in γ' -Fe₄N on LAO(100), STO(100) and MgO(100) substrates by sputtering was reported to increase with decreasing lattice mismatch between γ' -Fe₄N and the substrate used, that is 0, 3, and 11%, respectively. It is also still under discussion whether the M_s value of γ' -Fe₄N is really larger than that of α -Fe, that is approximately 2.2 μ_B per Fe atom. In order to get the accurate M_s value of γ' -Fe₄N, we think high-quality γ' -Fe₄N epitaxial films should be employed, and the M_s value should be evaluated by x-ray magnetic circular dichroism (XMCD), because the M_s value can be obtained free from its volume with XMCD. There have been several reports on XMCD measurements of γ' -Fe₄N. However, M_s values were not systematically evaluated for γ' -Fe₄N epitaxial films grown on different substrates. We prepared 10-nm-thick γ' -Fe₄N films epitaxially by molecular beam epitaxy (MBE) using solid Fe and a radio-frequency NH₃ plasma on LAO(100) (sample A) and MgO(100) (sample B) substrates. After the growth of γ' -Fe₄N layers, 3-nm-thick Au capping layers were subsequently deposited at RT in the same MBE chamber to prevent oxidation of the surfaces. X-ray diffraction patterns showed that the γ' -Fe₄N films were not strained. The magnetic moments were deduced from XMCD measurements at 300 K. Circularly polarized x-rays were incident perpendicular to the sample surface with an external H of ± 3 T, applied perpendicular to the sample surface. We confirmed that the magnetic moments of samples were saturated under $H = 3$ T. The total magnetic moments of γ' -Fe₄N in samples A and B were calculated to be $2.44 \pm 0.06 \mu_B$ and $2.47 \pm 0.06 \mu_B$ per Fe atom, respectively. These are almost the same, and are much closer to the theoretically predicted value of $2.59 \mu_B$. Therefore, we conclude that the M_s value in γ' -Fe₄N does not change depending on lattice mismatch between γ' -Fe₄N and the substrate used as long as γ' -Fe₄N is not strained. We should also note that the M_s value of γ' -Fe₄N is significantly larger than that of α -Fe.

4:10 PM

Z8, Sb Surfactant Use during GaInP and GaInAs Strain Relaxation: *Ryan France*¹; William McMahon¹; John Geisz¹; Aaron Ptak¹; Myles Steiner¹; Bobby To¹; Manuel Romero¹; Waldo Olavarria¹; ¹National Renewable Energy Laboratory

The semiconductor surface plays a large role in the determination of strain relaxation behavior. Surface roughness can both lower the dislocation nucleation energy and limit dislocation glide. We investigate the use of Sb surfactant on the strain relaxation of compressive GaInP and GaInAs on (001) GaAs grown using OMVPE. Sb is known to disrupt the ordering of GaInP, and has also been shown to smooth the surface of GaInAs. We grow compositionally graded buffers of GaInP and GaInAs with varied amounts of Sb surfactant and characterize the relaxation with cathodoluminescence, high resolution x-ray diffraction, atomic force microscopy, and an in situ multi-beam optical stress sensor. The last layer of the compositional grade is thickened for characterization, and has the relaxed in-plane lattice constant necessary for growth of a strain-free 1eV GaInAs solar cell. On GaInAs compositionally graded buffers, Sb reduces the final roughness, lowers the residual strain, and lowers the final threading defect density from 3 to 1×10^6

THURSDAY PM

cm⁻². After relaxation, lower residual strain with fewer threading dislocations indicates a longer average glide length. Thus, by reducing the surface roughness through the addition of Sb during growth, we reduce the barrier to glide in GaInAs. Sb surfactant drastically alters the relaxation characteristics of GaInP buffers. It raises the final threading defect density by over an order of magnitude and changes the direction of the epilayer tilt. These results indicate major differences in strain relaxation between ordered (without Sb) and disordered (with Sb) GaInP. The compositional grades in this study are grown on (001) GaAs substrates which are miscut 2° towards (-111). In the absence of ordering, substrate miscut results in a preferential glide plane for misfit relief. Relaxation of compressive GaInP or GaInAs on this substrate should result in tilt around [110] in a direction opposite the miscut. This is due to an imbalance between the misfits with (-111) or (1-11) slip planes. Disordered GaInP relaxes in this manner and has a similar tilt to the GaInAs buffers. However, ordered GaInP tilts in a direction contrary to the expected direction. Based on the degree of tilt, the vast majority of β dislocations must have glided on the (1-11) slip plane, indicating a large preference for this glide plane even with the reduced glide force due to the miscut. Glide along the planes associated with this tilt introduces anti-phase boundaries into the GaInP, bringing it closer to its disordered ground state. Therefore, glide may be enhanced in ordered GaInP due to this effect.

4:30 PM Student

Z9, Sensitivity of Strained and Unstrained Structure Growth on GaAs (111)B: *Denzil Roberts*¹; David Mueller¹; Gregory Triplett¹; ¹University of Missouri

The growth window for achieving high-quality photonic device structures on (111) GaAs by conventional molecular beam epitaxy (MBE) is very narrow. For this reason, the vast majority of fabricated GaAs-based photonic devices are synthesized on (100)-oriented substrates. However, strained and unstrained structures produced on (111) substrates offer a new class of electronic and optoelectronic devices that benefit from the piezoelectric effect- a feature that is not accessible on symmetric (100) orientations. In this work, we report on a series of investigations of strained and unstrained structures that include GaAs, AlGaAs/GaAs, and InGaAs/AlGaAs multi-quantum wells deposited on epi-ready GaAs (111)B 2° [21 1 -] Si-doped substrates by conventional molecular beam epitaxy. The difficulty with high-quality thin film deposition on (111)-oriented surfaces stems from its sensitivity to V-III ratio and substrate temperature, specifically the nucleation of adsorbed species and adatom migration lengths, which differ significantly from deposition on (100) GaAs surfaces. During this study, we reference the identification of the four temperature related surface reconstructions: (1x1)HT, (v19 x v19), (1x1)LT and (2x2), that are associated with the (111)B GaAs surface via in-situ reflection high energy electron diffraction (RHEED). In an effort to adequately examine the surface morphology for various strained and unstrained quantum well structures, a parameter space that includes surface reconstruction, substrate temperature, and a beam equivalent pressure (BEP) is explored. Under identical deposition conditions, direct comparisons are accomplished for strained and unstrained quantum well structures on GaAs (100) and GaAs (111) surfaces. A statistical experimental design is also employed, where the V/III ratio and substrate temperature are selected within the (v19 x v19) surface reconstruction phase. Using a scanning electron microscope (SEM) and an atomic force microscope (AFM), surface morphology was studied and demonstrates a strong correlation with V/III BEP ratio and substrate temperature. For smooth samples, AFM and SEM results show surface roughness of ~0.24nm across a 1x1 μ m² area and a significant decrease in the pyramidal hillock density across the wafer. As the growth parameters are optimized, strained and unstrained structures that take advantage of the piezoelectric properties can be produced.

4:50 PM

Z10, Ternary In_xGa_{1-x}As Nanowires on Silicon Substrates: 1D Heterogeneous Epitaxy, Bandgap Engineering, and Photovoltaics: Jae Cheol Shin¹; *Xiuling Li*¹; ¹University of Illinois

We report on the one-dimensional (1D) heteroepitaxial growth of high aspect ratio In_xGa_{1-x}As (x=0.15 – 1) nanowires (NWs) on silicon (Si) substrates

in almost the entire composition range without catalysts or masks using metalorganic chemical vapor deposition (MOCVD). NW diameter (~30 – 250 nm) is inversely proportional to the lattice mismatch between In_xGa_{1-x}As and Si (~4 – 11%), and can be further tuned by MOCVD growth condition. However, in contrast to self-assembled S-K quantum dots, the 1D heteroepitaxy in this case appears to be grown through the Volmer-Weber mode. Remarkably, no dislocations have been found in all composition In_xGa_{1-x}As NWs, even though massive stacking faults and twin planes are present. Indium rich NWs show more zinc-blende structure and Ga-rich ones show dominantly wurtzite polytypes, as confirmed by transmission electron microscopy (TEM) and photoluminescence peaks. Small degree of phase separation is observed from all ternary In_xGa_{1-x}As using both X-ray diffraction (XRD) rocking curves and Z-contrast TEMs. Solar cells fabricated using an n-type In_{0.3}Ga_{0.7}As NW array on p-type Si (111) substrate operates, with a mere ~2-3% area coverage, at Voc and Isc at 0.37 V and 12.9 mA/cm², respectively, with 2.4% efficiency. The direct 1D heteroepitaxy of ternary In_xGa_{1-x}As NWs in a wide composition/energy range reported here could enable monolithic tandem solar cells on silicon substrate with high absorption efficiency attributed to the direct bandgap, nanowire enhanced light trapping, as well as better bandgap and current matching.

Session AA: Four Dots and a Dash

Thursday PM
June 23, 2011

Room: Lotte Lehman
Location: Univ. of California-Santa Barbara

Session Chair: Akio Sasaki, Kyoto University; Baolai Liang, CNSI, UCLA

1:30 PM

AA1, Self-Assembled, Tensile-Strained III-V Islands on (110) and (111)A Substrates: *Paul Simmonds*¹; Minjoo Larry Lee¹; ¹Yale University

Traditionally, research into self-assembled quantum dots (SAQDs) has focused on compressively strained materials on (001) substrates. Nevertheless, SAQDs on other low-index surfaces may have attractive properties; long spin-lifetimes and a lack of fine-structure splitting are associated with heterostructures on (110) and (111) substrates respectively. SAQDs on (110) and (111) surfaces could therefore be useful for spintronics and quantum optics. However, compressively strained materials typically form relaxed 2D layers on (110) and (111) surfaces, due to the preferential glide of 90° partial dislocations.[1,2] By focusing instead on tensile strained materials, we demonstrate that it is possible to grow self-assembled GaP islands on both GaAs(110) and (111)A surfaces. Our results are consistent with the Kvam-Hull strain relaxation model[1] in which the combination of tensile strain *and* (110) or (111) surfaces prohibits the glide of 90° partial dislocations.[2] Moreover, nucleation of allowed 60° dislocations is kinetically limited; strain relief thus occurs by the observed self-assembly of dislocation-free, 3D islands. We have previously reported the spontaneous formation of 3D GaP islands at step-edges on GaAs(110) buffers.[3] Island growth proceeds without a wetting layer, consistent with the Volmer-Weber (VW) mechanism. These dislocation-free GaP islands exhibit monomodal size distributions, which are tunable with GaP thickness. Adatom diffusion length on GaAs(110) is large and equivalent to buffer terrace widths. As a result, GaAs(110) step-edges mediate island nucleation, even at deposition thicknesses << 1 ML. This presentation focuses on results obtained for tensile growth on (111) surfaces. MBE of GaP/GaAs(111)A leads to uniform self-assembled 3D islands, albeit with many differences from those formed on (110) surfaces. Given the relative surface energies of GaP(111)A and GaAs(111)A we predicted VW growth, and this was confirmed by submonolayer island nucleation. We demonstrate that island size and density are controllable as a function of both growth temperature and GaP thickness. Cross-sectional and plan-view transmission electron microscopy show that tensile GaP/GaAs(111)A islands are dislocation-free. We speculate that some of the differences in growth behavior between GaP/GaAs(110) and GaP/GaAs(111)A may result

from the shorter adatom diffusion length on GaAs(111)A. GaP/GaAs(111)A island size scales for GaP deposition between 0.17 and 1.73 ML. Fitting our scaled island size distributions with functions of the form derived by Amar and Family,[4] we obtain a critical island size for GaP/GaAs(111)A of 1–3 adatoms. By applying our understanding of GaP/GaAs island formation to tensile systems offering quantum confinement, we hope in the future to realize SAQDs on (110) and (111)A surfaces.

1:50 PM

AA2, Atomic Structure of InAs/InGaAsP/InP(001) Quantum Dashes and Decomposition of the InGaAsP Matrix Material: *Andrea Lenz*¹; Holger Eisele¹; Florian Genz¹; Lena Ivanova¹; Rainer Timm¹; Dieter Franke²; Harald Künzel²; Udo Pohl¹; Mario Dähne¹; ¹Technische Universität Berlin; ²Fraunhofer Heinrich Hertz Institut

Semiconductor nanostructures based on InP are interesting for various applications in opto-electronics at datacom emission wavelengths around 1.55 μm . In contrast to InAs deposition on GaAs, self-organized growth of InAs on InGaAsP/InP leads to more elongated structures, referred to as quantum dashes (QDashes). Here we study the structural properties of stacked InAs/InGaAsP QDashes buried in a heterostructure pin-diode, using cross-sectional scanning tunneling microscopy (XSTM). Samples with InAs layers embedded in an In_{0.78}Ga_{0.22}As_{0.47}P_{0.53} matrix were grown lattice-matched on InP(001) using metal-organic vapor phase epitaxy. XSTM images scanned at both the (-110) and (110) cleavage surfaces show ~ 2 nm high InAs QDashes, extending to about 15 nm along the [110] and to about 60 nm along the [110] direction. They are characterized by an almost pure binary InAs stoichiometry and cover almost the entire surface with typical center-to-center distances of 20 nm along the [110] direction and of 70 nm along the [-110] direction, corresponding to a QDash density of $7 \times 10^{10} \text{ cm}^{-2}$. The InGaAsP material between the InAs QDash layers appears inhomogeneous with bright regions separated by darker areas. From similar observations at filled-state and empty-state images we conclude that the quaternary material partly decomposes into columns of InAs-rich regions, which appear bright, and darker GaP-rich regions. The corresponding stoichiometry variation could be determined by a quantitative analysis of the strain-induced outward relaxation of the cleavage surface, amounting to about $\pm 10\%$ for both sublattices or up to $\pm 20\%$ if the decomposition occurs only at one sublattice. Images taken at both orthogonal cleavage planes show evidence for a spatial correlation of the InAs QDashes with the decomposition of the InGaAsP matrix material. Furthermore, a vertical stacking is found for the QDashes in the different InAs layers even being separated by the unusually large distance of 40 nm. It is demonstrated that InAs QDash formation on InGaAsP occurs by nucleation on initially slightly decomposed InAs-rich regions. This effect is intensified on top of an InAs QDash layer, leading to a column-like modulation of the InGaAsP composition, and hence a preferential vertical alignment of the QDashes in subsequently grown InAs layers.

2:10 PM Student

AA3, Photoluminescence and Thermal Carrier Activation in Type-II ZnTe/ZnSe Quantum Dots: *Bor-Chau Juang*¹; Weiming Wang¹; Jamie Phillips¹; ¹University of Michigan, Ann Arbor

Semiconductor nanostructures with type-II band alignment result in spatially separated electron and hole wavefunctions, resulting in reduced oscillator strength and corresponding reduction in optical absorption, spontaneous radiative recombination rate, and increased radiative carrier lifetime. The reduced optical response, however, provides a tradeoff with carrier lifetime that may be useful in applications where materials with longer radiative lifetime are desired in order to match coupled generation-recombination or transport processes. Furthermore, the optical characteristics of type-II structures may be tuned by varying structural dimensions rather than limited by intrinsic material properties. ZnTe/ZnSe quantum structures provide such a type-II band alignment, along with favorable energy transitions for efficient solar energy conversion. In this work, the epitaxial growth and photoluminescence properties of ZnTe quantum dots grown on ZnSe will be presented. Materials are grown by solid source molecular beam epitaxy

on GaAs (001) substrates. Strained layer growth of ZnTe on ZnSe results in the spontaneous formation of 3-D islands in the Stranski-Krastanow growth mode as observed by in-situ reflection high energy electron diffraction. Low temperature photoluminescence (PL) spectra demonstrate optical transitions for ZnTe/ZnSe in the range of 1.7-2.8eV. Emission near 2.8eV corresponds to bandedge emission of the ZnSe, while emission below 2.1eV is attributed to a defect band observed in ZnSe control samples without ZnTe. Emission peaks are observed near 2.6eV and 2.7eV corresponding to Te substitutional impurities in ZnSe. Broadband emission in the range of 2.1-2.4eV is attributed to ZnTe/ZnSe quantum dots, is both below the ZnSe and ZnTe bandedge, and is evidence that this emission corresponds to the type-II band lineup in the material. Temperature dependent PL indicates that the emission peak energy for ZnSe follows the Varshni relation. The emission from the ZnTe/ZnSe quantum dots demonstrates a sharp transition from 2.24eV to 2.1 eV near 100K, implying a thermal activation process that is attributed to carrier transfer between quantum dots of varying size. The temperature dependent integrated PL intensity of the ZnTe/ZnSe quantum dots follows an Arrhenius relation with activation energy of 54meV. Further details of the ZnTe/ZnSe quantum dot structural properties, electronic structure, and temperature dependent carrier transfer and emission properties observed in PL studies will be presented.

2:30 PM Student

AA4, Temperature Dependent Photoluminescence of Ensemble and Single InAs/InGaAlAs Quantum Dots: *Nahid Jahan*¹; Claus Hermannstädter¹; Jae-Hoon Huh¹; Hirotaka Sasakura¹; K. Akahane²; M Sasaki²; Pankaj Ahirwar³; Thomas J Rotter³; Ganesh Balakrishnan³; Hidekazu Kumano¹; Ikuo Suemune¹; ¹Laboratory of Nano-photonics; ²National Institute of Information and Communication Technology; ³Center for High Technology Materials

Understanding the quantum nature of photons as messenger qubits and the ability to prepare, manipulate and process them is indispensable. Recent microscopic-spectroscopy studies of individual semiconductor quantum dots (QDs) have shown that single quantum dots (SQDs) have excellent potential for high speed quantum computation and quantum key distribution. However, operation of SQDs at elevated temperature is a challenge for practical applications. While to-date most studies focus on InAs QDs grown on GaAs substrates, InAs QDs grown on InP substrates are gaining more attention for applications in the near-infrared wavelength range (1.3-1.55 μm) because of their suitability with silica based single fiber networks. However, accessing SQD is limited by the high density of QDs ($\sim 10^{11} \text{ cm}^{-2}$) due to the smaller lattice-mismatch compared to InAs QDs grown on GaAs. Motivated by the aforementioned circumstances we studied the temperature dependent photoluminescence (PL) of ensembles of QDs and SQDs from different aspects, e.g., state filling, quenching mechanism at high temperature, and the influence of inter-dot coupling on photon emission processes. We measured temperature dependent macroscopic PL from high density InAs/InGaAlAs QDs grown on InP(311)B substrates by molecular beam epitaxy. By varying the nominal thickness of the optically active layer from 3 to 6 monolayers (MLs), photon emission from QDs is achieved between 1.2 and 1.6 μm . Fitting the temperature dependent integrated PL of 4ML QDs with Arrhenius equation results in a thermal quenching energy of 150 meV, which is close to the energy difference between the InAlGaAs barrier and the high energy edge of the QD ensemble. Because the integrated intensity is constant upto 71 K, these QDs are assumed to exhibit high quantum efficiency at low temperatures. To access SQDs, electron beam lithography and etching were performed to fabricate tapered nanostructures with 300nm height and diameters of 250-450 nm of the QD plane. The micro-PL spectra of SQDs were recorded using a double monochromator with 300 gr/mm gratings and an InGaAs photodiode array detector. We observed clearly separable SQD emission lines in the wavelength range around 1.46 μm which is comparable to the long wavelength side of the QD ensemble. Such SQD emission can be temperature tuned in a range of ~ 10 nm between 3 and 82 K; especially, clear SQD emission can be obtained at the technically relevant liquid nitrogen temperature of 77 K. In this work we present a suitable way to use high density QDs as an attractive wavelength-tunable source of single photons around 1.45 to 1.5 μm . The longer wavelength of 1.55 μm can be reached by varying the thickness of QDs up to 6ML.

Considering the high QD density, inter-dot coupling and charge carrier transfer will be studied as a continuation of this work.

2:50 PM

AA5, Atomic Structure and Optical Properties of Submonolayer InAs/GaAs Depositions: Andrea Lenz¹; Holger Eisele¹; Jonas Becker¹; Jan-Hindrick Schulze¹; Tim Germann¹; Franziska Luckert¹; Konstantin Pötschket¹; Ernst Lenz²; Lena Ivanova¹; Andre Strittmatter¹; Udo Pohl¹; Mario Dähne¹; Dieter Bimberg¹; ¹Technische Universität Berlin

Quantum dots formed from submonolayer (SML) depositions are an interesting alternative to quantum dots grown using the Stranski-Krastanov mode. SML depositions are expected to yield exceedingly high dot densities above 10^{11} cm⁻² and therefore bear the potential to produce high optical gain for laser devices. Indeed, vertical emitting lasers based on InAs/GaAs SML quantum dots recently demonstrated high-speed error-free operation at 20 Gb/s up to 120°C. However, there is a lack of structural information in order to develop a model for ultrafast relaxation dynamics in this system. SML quantum dots are formed by a cycled deposition of the dot material with a thickness well below one monolayer (ML) and several MLs of matrix material. Structural correlation, both vertically as in-plane is coupled to strain originating from the dot material. Segregation and diffusion acting vertically and laterally during growth are counteracting for the intended SML formation. Cross-sectional scanning tunneling microscopy (XSTM) is used to determine the spatial structure and the stoichiometry with atomic resolution. The investigated sample was grown by metalorganic vapor phase epitaxy at 500 °C and contains two fivefold stacks of 0.5 ML InAs with either 1.5 ML, 4 ML, or 16 ML separation layers. XSTM measurements demonstrate clearly that there is an island formation instead of a layer-like structure. The InAs is not assembled within a single atomic plane, but segregated along growth direction. The center-to-center distance between the islands is only about 7 nm, resulting in a high density in the 10^{12} cm⁻² range. The height of the islands is about 4–5 ML, and the width is approximately 5 nm. Islands of this size lead to localization of charge carriers and hence act as quantum dots. The vertical segregation is determined in detail by the analysis of the local lattice parameter. At each layer where 0.5 ML InAs was deposited, the measured lattice parameter jumps up to a value corresponding to an InAs concentration of $x_{In} = 15\text{--}20\%$, followed by an exponential decrease. For the 4 ML and 16 ML thick GaAs spacer layer samples a segregation coefficient of about 0.73 was determined. The segregation becomes even more important, when the spacing between the InAs SML is reduced to about 2–4 ML GaAs. The In segregates into the subsequently deposited SML, thereby enhancing the local In concentration. Furthermore, the stacked InAs islands are stronger coupled, comparable to the case of stacked Stranski-Krastanov quantum dots with thin spacer layers. These structural observations are correlated with optical photoluminescence measurement, in which the peak energy shifts with spacer thickness toward the blue spectral range.

3:10 PM Break

Session BB:

Fundamentals of Low-Dimensional Structures

Thursday PM
June 23, 2011

Room: Lotte Lehman
Location: Univ. of California-Santa Barbara

Session Chair: Seth Bank, University of Texas

3:30 PM Student

BB1, Local Density of States and Semimetallic Behavior of Rare Earth-V Nanoparticles Embedded in a III-V Semiconductor Matrix: Jason Kawasaki¹; Rainer Timm²; Trevor Buehl¹; Edvin Lundgren²; Arthur Gossard¹; Anders Mikkelsen²; Chris Palmstrom¹; ¹University of California Santa Barbara; ²Lund University

The atomic and electronic structure of molecular beam epitaxy (MBE)-grown ErAs nanostructures embedded within a GaAs matrix are examined

via cross-sectional scanning tunneling microscopy (STM) and spectroscopy (STS). Tunneling current $I(V)$ and differential conductance dI/dV spectra show that for both ErAs nanoparticles and nanorods the local density of states (LDOS) exhibits a sharp but finite minimum at the Fermi level, demonstrating that both the particles and rods are semimetallic and not semiconducting. This observation lies in contrast to previous models of quantum confinement in ErAs. We also use STS to measure changes local in the density of states across the ErAs/GaAs interface and discuss the formation of interface states and band bending at the interface.

3:50 PM Student

BB2, A Simple Thermodynamic Model for the Doping and Alloying of Nanoparticles: John Petropoulos¹; Thomas Cristiani¹; Pernell Dongmo¹; Joshua Zide¹; ¹University of Delaware

We present a simple thermodynamic model to explain the doping of nanoparticles through minimization of Gibbs free energy. Over the last decade, nanoparticle-related research has become increasingly prominent, and researchers have found that the properties of nanoparticles differ significantly from that of bulk materials. Accordingly, there has been considerable work done on the doping of nanoparticles and nanostructures, with varying levels of success. While it is possible to dope nanoparticles, as their size decreases, the ability to incorporate impurities into the core of the structure becomes increasingly difficult [1]. There are two models commonly used to explain this phenomenon, kinetics and thermodynamics, the former of which requires many assumptions and complex calculations. We propose that thermodynamics on its own is generally sufficient to explain the doping properties of nanoparticles. Gibbs free energy is minimized, with both the enthalpy and entropy terms playing prominent roles on such small scales. We are primarily concerned with electrically-active dopants and therefore differentiate between surface and core atoms, calculating differential Gibbs free energy for each as a function of nanoparticle size. We define the enthalpic term as a difference (generally increase) in bond energy for dopants and consider configurational entropy for both the surface and core. We show that the free energy of surface impurities in very small nanoparticles is lower than that of core impurities; as particle size decreases, competition between the enthalpic and entropic terms becomes more prominent, surface doping therefore occurs preferentially. A critical size for core doping is identified, below which impurity incorporation in the core is thermodynamically limited. In all cases, core impurity concentration is reduced as particle size decreases. However, we confirm that larger-than-bulk impurity concentrations (which have been reported experimentally as increased alloying [2]) are possible, but are confined to surface doping. We also present data which confirms that this simple model is capable of handling real world systems and is in good agreement with experimental results. This model can easily be extended to one- and two-dimensional structures, such as nanowires and quantum wells, and can be applied to material systems with different particle shapes and coordinations. It is also not restricted to bond energy as the dominant enthalpic term, but can be modified to model any other first order effect such as strain.

4:10 PM Student

BB3, Band Structure and Thermal Escape Processes of Strained InGaSb/AlGaSb Quantum Wells: Nahid Jahan¹; Hitoshi Iijima¹; Claus Hermannstädter¹; Thomas Rotter²; Pankaj Ahirwar²; Ganesh Balakrishnan²; Hidekazu Kumano¹; Ikuo Suemune¹; ¹Hokkaido University; ²University of New Mexico

The optical behavior of InGaSb/GaSb QWs has recently attracted attention due to the narrow band-gap properties, high carrier mobility and applications in the infrared spectral region. As a result of the low temperature GaSb band gap of 0.81 meV (1.53 μ m), ternary InGaSb/AlGaSb heterostructures lattice matched on GaSb substrates are suitable to tailor wavelengths around 1.55 μ m for usage in silica based fibre communication. Although wavelength-tunable quantum well long wavelength lasers are applicable in gas sensing, phase shifting interferometry, optical detectors, etc., reports on fundamental optical properties of InGaSb/AlGaSb heterostructures are not yet found prolific in number. Considering these aspects, the band structure of strained InGaSb/AlGaSb

QWs, as well as optical properties and quantum confinement was examined in this work. The temperature dependent photoluminescence (PL) was measured to study the optical properties of In_xGa_{1-x}Sb QWs for two different Indium concentrations. From the PL temperature dependence, the thermal quenching energy was found to be around 45 meV by fitting the measurement data with the Arrhenius equation. Based on the measured low temperature exciton recombination energies, the band structure and confinement were calculated by solving the Schrodinger equation for a finite potential well with a small valance band (VB) offset. The theoretical treatment of the strained QWs resulted in a strain contribution of -72 meV to the VB (heavy-holes), measured relative to the VB maximum at zero-strain. Including this band deformation potential and the measured 45 meV activation energy as input parameters, the confinement energy calculation results in a weak hole confinement energy and a thin InGaSb well of around 3 nm width along with a small VB offset. The emphasis on the assumption of a small VB offset comes with the key issue of the small activation energy which is suitably explained by the thermal escape of the single carrier holes from the QW to the barrier. To approve the composition and the calculated well thickness, X-ray diffraction measurements were carried out to precisely characterize the epitaxial layer structure. Both In_xGa_{1-x}Sb QWs of 32% and 36% indium concentration exhibit a thin well width of around 3nm, which is in excellent agreement with the calculations. The InGaSb QW exhibits 1.52 μm photon emission at 10 K, which is desirable for fiber optical communication, and has the ability to be tuned to longer wavelengths by increasing the temperature. We demonstrated a small thickness of the QWs and a small activation energy of 45 meV which is explained by the hole carrier escape because of weak confinement and small VB offset. The next target is to analyze the efficiency of InGaSb/AlGaSb QWs using time resolved spectroscopy.

4:30 PM Student

BB4, Formation and Templating of III-V Semiconductor Nanospikes by Focused Ion Beams: Kevin Grossklaus¹; Joanna Millunchick¹; ¹University of Michigan

Serial methods for nanowire creation allow careful placement of nanostructures in arrays, but often have the downside of low throughput. Bottom-up self-assembly based methods for nanowire production allow for the creation of nanowires rapidly over a large area, but often with limited ability to accurately place nanowires at desired locations. We have developed a focused ion beam (FIB) based hybrid method for III-V nanostructure creation that provides a compromise between these two extremes. By using a FIB to erode InAs films grown on InP substrates we have been able to create high aspect ratio heterostructure spikes, or “nanospikes,” with average heights of 300 nm and maximum heights greater than 800 nm. Nanospike formation proceeds via an ion-produced droplet masking process. Initially, metallic droplets form on the surface due to preferential sputtering of the group V material. These droplets initially move randomly across the surface but as film erosion proceeds they become stationary and act to shield the underlying material. In this way the droplets act as etch-masks that allow nanospikes to form under them as the surrounding material recedes due to FIB erosion. Characterization of the nanospike structure by transmission electron microscopy has revealed that they contain a single crystalline core that maintains the structure of the original film and is free of extended defects such as twin boundaries. We have found that the InAs/InP film heterostructure is necessary for nanospike formation, as nanospikes will not form on InAs or InP alone upon FIB irradiation. We have also found that the placement of nanospikes is strongly dependent on the initial InAs film morphology and the recession of the InAs/InP interface as erosion proceeds. Pre-patterning the InAs/InP heterostructure leads to well ordered arrays of nanospikes, and the location and spacing of nanospikes may be directly controlled by pre-patterning the surface. Using this hybrid pre-patterning and FIB erosion approach, it is possible to create ordered arrays of nanospikes in arbitrary patterns.

4:50 PM Student

BB5, A Detailed Temperature-Dependent Photoluminescence Investigation into the Growth Pause Induced Ripening of InAs/GaAs Quantum Dot Heterostructures: Rahul Makhijani¹; Saumya Sengupta²; Subhananda Chakrabarti²; ¹Dept. of Electrical Engineering, Center for Nanoelectronics, Indian Institute of Technology Bombay; ²Indian Institute of Technology Bombay

In recent years InAs/GaAs self organized quantum dots (QDs) system grown by S-K mode have attracted considerable research interest. A less investigated but important growth condition which was studied for the first time is the introduction of growth pause. Growth pause (GP) is the time interval between the end of deposition of quantum dots and subsequent deposition of a capping/barrier layer. We investigated the effect of GP on structural and optical properties of single layer InAs/GaAs QDs system. Six samples with different growth pauses(0,25,50s) and two growth rates(0.187 ML/s and 0.032 ML/s), were grown by solid source MBE on (100)oriented GaAs substrate. We performed STEM, AFM and temperature-dependent PL study of the samples. TEM images show the shape of the dots in all the samples is trapezoidal. Average height and lateral size is measured in the range of 3-4 nm and 13-18 nm, respectively. Though the height of the dots remained almost constant, an increment in lateral size (and hence aspect ratio) of dots is observed as GP is increased. The average density of dots measured is (0.6-1.5)*10¹⁰ dots per cm² and (2.3-2.8)*10¹⁰ dots per cm² for slow growth rate (SGR) and fast growth rate (FGR) respectively. The density of dots is decreasing with increasing GP for both the growth rates. We believe that for longer GP the dots are getting longer duration to interact with neighboring dots under strained condition which coalesce to produce larger ones and hence their corresponding decrease in number. Faster deposition rate helps to produce higher density of dots. This is due to the competition between nucleation rate and nucleation probability. For SGR the growth process is dominated by nucleation probability. The nucleation rate increases with the increment of growth rate, resulting in a higher dot density. In FGR nucleation rate and nucleation probability reach a dynamic equilibrium, resulting in dot density saturation. PL measurements depict a shift of ground state peak from 1.082 eV to 1.071 eV with an increase in GP for SGR confirming our previous claims. A decrease in integrated photoluminescence is observed as the GP increases. Since integrated PL is proportional to number of dots, it is evident that dot density decreases gradually. We observed that integrated area of QDs increases with aspect ratio at 283 K. The activation energy in general is found to increase with the increase in dot size (i.e. width) as expected from k.p model. Experimentally it decreases from 412.7 meV to 306.8 meV for SGR and 496 meV to 419 meV for FGR. There is an increase in activation energy for 25 sec growth pause sample for SGR. These contradictions are attributed to lattice and interface defects generated in the QD structures due to In out diffusion. Larger the QD, larger the strain, and so are the barrier interface defects, i.e. non-radiative centers through which PL emission quenching takes place.

Session CC: Graphene Characterization and Applications

Thursday PM Room: MCC Theatre
June 23, 2011 Location: Univ. of California-Santa Barbara

Session Chairs: Huili Grace Xing, University of Notre Dame; M.V.S. Chandrashekar, University of South Carolina

1:30 PM

CC1, In Situ High-Temperature Scanning Tunneling Microscopy Studies of Graphene Growth on 6H-SiC(0001): Suneel Kodambaka¹; Yuya Murata¹; Vania Petrova²; Ivan Petrov²; ¹University of California, Los Angeles (UCLA); ²Frederick Seitz Materials Research Laboratory, University of Illinois Urbana-Champaign

Using high-temperature (~1400 K), ultra-high vacuum scanning tunneling microscopy (UHV-STM), we investigated the graphene growth on single-

crystalline 6H-SiC(0001) surface. STM images are acquired during annealing as a function of time. We observed the growth of graphene at the expense of SiC. From the STM images, we measured time-dependent variations in areal coverages of SiC terraces and graphene. We find that the rate of decomposition of SiC is $3.13 \times$ higher than the rate of growth of graphene. That is, 3.13 layers of SiC is consumed for every one layer of graphene formation, consistent with the expected number of carbon atoms required to form graphene from SiC. Interestingly, STM images indicate that the second layer graphene nucleates at the SiC surface step edges and grows inward at the expense of the SiC terraces. This result is strikingly different from the growth of the first layer graphene. Our results provide new atomic-scale insights into the growth of graphene on SiC.

1:50 PM

CC2, Electrical Characterization of Graphene-Semiconductor Heterojunctions: *Travis Anderson*¹; Karl Hobart¹; Luke Nyakiti¹; Virginia Wheeler¹; Rachel Myers-Ward¹; Boris Feigelson¹; Joshua Caldwell¹; Francisco Bezares¹; Jennifer Hite¹; Michael Mastro¹; D Gaskill¹; Charles Eddy¹; Francis Kub¹; Glenn Jernigan¹; ¹Naval Research Laboratory

Graphene is a 2D material, and as such it only has chemical bonds in the plane parallel to its molecular plane. Those bonds are conjugated leading to molecular orbital overlap and produce the unique physical and electrical properties typically associated with graphene. However, when graphene is grown on SiC or transferred to other substrates from Ni or Cu catalyzed growths, there is only van der Waals bonding between the graphene and the underlying surface. To date there has been few attempts to understand the properties of electron or hole transport through the graphene sheet into the underlying substrate. It has been shown in the literature however that, based on a graphene work function of 4.5-5.0 eV, a Schottky contact is formed when graphene sheets are transferred to various semiconductors, such as Si, GaAs, and SiC [1,2]. Furthermore, diamond has also been shown to form a Schottky contact when grown directly on SiC [3]. In this work, we present the electrical characterization and analysis of the vertical junction formed between graphene and various semiconductors. Epitaxial graphene grown directly on n- or p-type SiC exhibits excellent rectifying behavior and low off-state leakage, <1 nA at -20V. The devices, however, display a large voltage turn-on offset of >2V and virtually no temperature dependence in the turn-on region. These properties are more characteristic of a tunneling junction rather than a Schottky contact. To further study this phenomena, investigations of the vertical transport properties of epitaxial and CVD graphene transferred to Si, GaN, and SiC, as well as graphene formed directly on these semiconductors via precipitation from Ni, will also be presented.

2:10 PM Student

CC3, Correlated Conductivity and Work Function in Epitaxial Graphene: *Mohammad Nomani*¹; Amol Singh¹; Goutam Koley¹; Virgil Shields²; Mike Spencer²; Gary Tompa³; Nick Sbrockey³; ¹University of South Carolina; ²Cornell University; ³Structured Materials Industries, Inc.

A correlation between conductance change and corresponding surface work function (SWF) change due to molecular adsorption on epitaxial graphene grown on both C and Si-faces of 6H-SiC has been demonstrated based on Fermi level shifts, type of carrier, and density of states D(E) of the graphene film. Graphene samples were grown epitaxially on CMP polished Si and C-faces of semi-insulating on-axis 6H-SiC substrates by annealing them at 1300-1600°C for one hour under high vacuum (<10⁻⁵ Torr) in a cold-wall resistively heated SiC sublimation reactor. From Raman spectroscopy, thickness of Si-face graphene was found to be 1-3 MLs, while that of C-face was 8-10 MLs. The low I_D/I_G ('D' peak to 'G' peak) ratio (<0.02) confirmed quality graphene. In amperometric experiments, p-type doping with electron accepting NO₂ caused the conductance to decrease by 9% for Si-face few layer graphene (FLG) and to increase by 3.25% for C-face multilayer graphene (MLG). Adsorption of electron donating NH₃ increased the conductance of Si-face FLG by 8% and decreased that of C-face MLG by 3.5%. Therefore, p-type (n-type) doping by NO₂ (NH₃) should decrease (increase) the conductivity of an n-type graphene layer, and increase (decrease) the conductivity of p-type graphene

layer. As per our observation, this infers that in C-face MLG p-type charge carriers are dominant and in Si-face FLG charge carriers are mostly n-type. Lin et al. supports our observation. To support our amperometric results, and to examine in more detail, we performed the potentiometric experiments, and found a strong correlation between them. Adsorption of NO₂ (NH₃) caused the SWF of graphene on both the faces to increase (decrease) by 120-140 meV (85-100 meV) implying a downward (an upward) shift of the Fermi level by that amount. If the Fermi level of Si-face FLG, E_{F-Si}, goes down, D(E) for n-type carriers decreases, suggesting a decrease in the conductance. Again, if the Fermi level of C-face MLG, E_{F-C}, goes down, D(E) for p-type carriers increases implying an increase in the conductance. If NH₃ adsorption pulls E_{F-Si} up, D(E) for n-type carriers increases which causes the conductance of Si-face FLG to increase. Again if E_{F-C} is pulled up, D(E) for p-type carriers decreases resulting in a decrease in the conductance of C-face MLG. Flow rate dependence of SWF change of an adsorption system has also been observed for Si-face FLG. The observed differences in SWF changes can be explained by considering the change in electron affinity of 6H-SiC due to the formation of a dipole moment between the polar molecules (NO₂, NH₃) and the substrate inferring that at higher flow pressure gas molecules can diffuse through the graphene film to the substrate.

2:30 PM

CC4, Response of Graphene-Based Field Effect Devices Exposed to Gamma and Neutron Irradiation: *Mark Fanton*¹; Joshua Robinson¹; Michael LaBella¹; Randal Cavalero¹; Brenden Heidrich¹; Matthew Hollander¹; Zachery Hughes¹; Kathleen Trumbull¹; ¹Penn State University

The Department of Defense supports development of graphene-based electronic technology for various applications, including space-based platforms. When placed on an insulating substrate it resembles an extreme case of silicon-on-insulator (SOI) technology. While the capture cross section for particles and photons is expected to be low, the impact of atomic displacement on a truly 2D structure could be quite large since displacement of even a single C atom creates a significant discontinuity in the lattice. Similarly, displacement of material into the graphene film from the surrounding substrate, dielectric, or metallization could create a significant disruption of the material properties and performance. In addition, charge generation and trapping at the interfaces with the nano material could create virtual gates to carrier movement. This work focuses on the real time interactions between graphene field effect transistors and ionizing radiation in the form of gamma rays and neutrons. The fundamental electrical, structural, and chemical responses of graphene test structures were characterized after irradiation with gamma rays and neutrons at the Penn State University Breazeale nuclear reactor. Gamma exposure was conducted via a Co60 source with an energy at maximum yield of 1.3 MeV, and a maximum photon energy of 2.16 MeV. The total dose ranged from 2 MRad to 100 MRad. Neutron exposure was conducted at Penn State's Breazeale nuclear reactor. Samples were exposed to thermal neutrons with the total dose ranging from 108/cm² to 1012/cm² and to fast neutrons with the total dose ranging from 1010/cm² to 1014/cm². Field effect transistors (FETs) and gated Van der Pauw structures were examined. Gate dielectrics consisted of SiO₂ and HfO₂. Hall effect mobility was evaluated after irradiation, while the response of FET's was evaluated in real time during irradiation. For gamma irradiation the average carrier mobility remained near 800 cm²/V-s after irradiation. Raman spectroscopy showed no significant change in the D/G peak ratio indicating no measureable structural damage was created. In contrast, neutron irradiation appears to induce some degradation at exposures above 1010/cm². Raman spectroscopy data will be reported as an assessment of increased defect density. Additional experiments using fast neutrons are being performed to understand this. The effect of irradiation on device characteristics in real time during irradiation will be discussed with an emphasis on the saturation current and source-drain current in field effect transistors. This will provide baseline information for charge trapping in simple structures as a function of the gate dielectric. The use of alternate gate materials to mitigate charge trapping will also be discussed.

2:50 PM Student

CC5, Surface Adsorption and Charge Transport in Epitaxial Graphene on 6H-SiC: *Shamaita Shetu*¹; MWK Nomani¹; Goutam Koley¹; MVS Chandrashekar¹; ¹University of South Carolina

Graphene has captured the attention of researchers as a prospective candidate for gas and vapor sensors with its remarkable properties including high electron mobility, high thermal conductivity and stiffness, room temperature quantum hall effect and ballistic transport. Our goal here is to obtain an understanding of charge carrier transport in sensing and reconcile the discrepancy between earlier measurements in [1]. Surface work function (SWF) change and conductance(%) change was observed due to adsorption of NO₂ and NH₃ in graphene layers on 6-H SiC. A reduction in SWF for NO₂ implies NO₂ dopant behaving as n-type while an increment in SWF implies NH₃ as p-type. This was opposite to the previous observations made on graphene on SiO₂ and free-standing graphite layers on SiO₂ indicating that the electron transfer behavior upon adsorption depends on the substrate. Another inconsistency was that conductance(%) change decreased with impurity concentration, even with increasing carrier concentration for NO₂ while it was opposite for NH₃. These inconsistencies were reconciled using Boltzmann transport, by accounting for the influence of scattering from the adsorbed impurities. Graphene conductivity has been influenced by long range coulomb scattering from the screening of charged impurities on the surface of graphene and short range scattering arising due to electron-electron interaction and defects or dislocations [2]. Experimentally, it has been observed that long-range coulomb scattering from surface impurities dominates. We have interpreted total impurity density as $n_{imp} = n(NO_2 \text{ or } NH_3) + K$ where $n(NO_2 \text{ or } NH_3)$ is the impurity concentration due to adsorption and K is the residual impurity density. Conductivity is calculated by considering both scattering mechanisms using the formulas in [2]. The carrier concentration was calculated from the measured SWF. We found excellent agreement with the experimental results approximating a residual impurity density $\sim 4.5 \times 10^{12}/\text{cm}^2$ and thickness of about 8-10ML. This is higher than that observed in exfoliated graphene $\sim 10^{11}/\text{cm}^2$ without intentional impurities introduced. This discrepancy is currently not understood and is being investigated. For NO₂ adsorption SWF reduction implies electron donation by NO₂ to graphene layer and conductivity is reduced and the opposite for NH₃ adsorption. Finally, only the top ML of graphene was assumed to be modulated by the adsorbate impurities. This is due to 2 reasons: a) the electrostatic screening length in graphene is $\sim 1\text{ML}$ and b) due to graphene's small lattice constant, no molecules can diffuse through the layers. Thus, for a 10ML film, the effective %change in conductance is reduced by 10x compared to that for a single ML. In summary, residual impurity density and the thickness of layers play a significant role in charge carrier transport in graphene.

3:30 PM Student

CC6, Graphene Reinforced Composites as Efficient Thermal Interface Materials: *Khan Shahil*¹; Samia Subrina¹; Alexander Balandin¹; ¹University of California, Riverside (UCR)

The power dissipated in computer chips has been growing with each new technology node reaching unsustainable levels. In such a situation, the search for materials that conducts heat well and fast became essential for design of the next generations of integrated circuits (ICs) and three-dimensional (3D) electronics [1]. Efficient thermal management of electronics, optoelectronics and photonic devices require better thermal interface materials (TIMs). Current TIMs are based on polymers or greases filled with thermally conductive particles such as silver or silica, which require high volume fractions of filler (up to 70%) to achieve K of $\sim 1\text{-}5 \text{ W/mK}$ of the composite. Carbon materials such as carbon nanotubes (CNTs) have been studied as possible fillers in TIMs. Theoretical and cost considerations suggest that chemically derived graphene and few-layer graphene (FLG) flakes can perform better than other carbon materials in TIMs. It was discovered that the intrinsic thermal conductivity of graphene is extremely high [2]. At the same time, thermal properties of graphene flakes in the composites will be determined by the flake size, thickness, and coupling to the matrix material. We report the results of the experimental investigation of thermal properties of the graphene reinforced composite materials. The TIM samples were produced using the chemically

derived graphene and FLG flakes. The number of atomic planes in FLG flakes was determined with the micro-Raman spectroscopy [3]. Thermal properties of the resulting graphene-epoxy composites were measured with the "laser flash" and "hot disk" thermal conductivity techniques. The thermal conductivity enhancement factor exceeded $\sim 2300\%$ at 10% of the volume loading fraction. To achieve such strong enhancement with the conventional filler materials one would need a loading fraction of $\sim 70\%$. The computer simulations of thermal properties of TIM composites carried out using the modified effective medium approximation, which included the thermal boundary resistance effects, were in agreement with our experimental data. Our results suggest that graphene and FLG flakes can become excellent filler materials in the next generation of TIMs. The work at UCR was supported, in part, by the Office of Naval Research (ONR) award on Graphene Quilts for Thermal Management of High-Power Density Electronics and DARPA - SRC through the FCRP Center on Functional Engineered Nano Architectonics (FENA).

3:10 PM Break

3:50 PM Student

CC7, Frequency Domain THz Characterization of Graphene: *Berardi Sensale-Rodriguez*¹; Rusen Yan¹; Michelle Kelly¹; Tian Fang¹; Kristof Tahy¹; Debdeep Jena¹; Lei Liu¹; Huili Grace Xing¹; ¹University of Notre Dame

Graphene has been intensely investigated for various electronic applications such as flexible electronics, RF amplifiers, transparent conductors, and potential replacement of Si channel in high performance MOSFETs. There are also a few reports and proposals on THz lasers and photodetectors based on graphene. However, to date only photodetectors and mode-locked ultrafast lasers have been demonstrated in the lab. In this work we present frequency domain characterization of large area graphene (single-layer and double-layer) over the THz range and demonstrate that THz absorption by graphene can be electrically tuned. Based on this observation, broadband and tunable attenuators for THz quasi-optical systems can be designed and fabricated. In this study we aim to discover applications for graphene in THz communication systems. Single-layer graphene was grown using the copper-catalyzed chemical vapor deposition (CVD) approach recently developed by Li et al in a quartz tube furnace using CH₄ and H₂. Following the growth, graphene sheets of over 1 cm² are transferred to the host substrates (in this study quartz or SiO₂/p+silicon) using PMMA and wet etch methods; double-layer graphene sheets were obtained by transferring twice the single-layer CVD graphene. For the single-layer graphene sample transferred onto SiO₂/Si substrate, top and bottom ring contacts were fabricated to contact graphene and p+Si respectively. Transmission was measured in frequency domain using a VDI (Virginia Diodes, Inc.) THz source that produces CW radiation in the 570-630 GHz frequency band. THz radiation was coupled by a four off-axis parabolic mirror setup into a zero bias Schottky diode broadband detector. Samples were scanned by a 2D positioning stage, and then a 2D transmission attenuation image was generated. Using this technique, graphene on quartz substrate samples were imaged. It was found a single layer graphene introduces an attenuation of 0.5 - 1.0 dB while the double-layer graphene leads to another 0.5 dB of attenuation. Though not yet tested, we expect a linear increase in attenuation with respect to the number of graphene layers. From the relation between graphene sheet conductivity and transmission ratio of the graphene/substrate sample to that of the substrate, local sheet conductivity of a single layer graphene was found to range between 0.4 - 0.9 mS. THz attenuation can be tuned by tuning the graphene conductivity. To this end, we applied DC voltage across the single layer CVD graphene and SiO₂/Si substrate while monitoring the THz transmission as a function of this voltage. It was found that the transmission clearly changes with the applied voltage (by sweeping it from -35 to +35 V at 600 GHz, attenuation changes by 0.25 dB). The above observations indicate graphene can be potentially used to fabricate precision and tunable THz attenuators.

4:10 PM

CC8, Charge Carrier Dynamics in Graphene: Suspended vs. Supported: Bo Gao¹; Libai Huang¹; Gregory Hartland¹; Michelle Kelly¹; Huili Xing¹; Debdeep Jena¹; ¹University of Notre Dame

Charge carrier dynamics is important to electron transport, and understanding this process will be vital for the realization of future graphene-based electronics. Since graphene is an all-surface material, the environment, especially the substrate which graphene sits on, may play a key role in the process. Here we use transient absorption microscopy to characterize suspended and supported graphene and to interrogate the charge carrier dynamics. This technique has the ability to directly image carrier dynamics with a diffraction-limited spatial resolution and a time resolution of ~ 200 fs. In our experiment graphene was grown by chemical vapor deposition (CVD), and was subsequently transferred onto glass with micro-trenches to get suspended and supported graphene. For supported graphene, transient absorption signal decays very fast and vanishes within 1.5 ps at low pump fluence (< 3.4 mJ/cm²). As increasing the pump fluence, the decay becomes slow, and constant at high pump fluence (~ 13 mJ/cm²). For suspended graphene, transient absorption signal needs a decay time of 4.0 ps at very low pump fluence (~ 0.3 mJ/cm²) and becomes constant at low pump fluence (~ 5 mJ/cm²). When constant, the slow decay time of suspended graphene is longer than that of supported graphene. It is known [1] that the fast and slow decay is assigned to coupling between the electrons and optical phonons in graphene and the hot phonon effect respectively. Therefore, the remarkable differences in the dynamics of supported and suspended graphene are attributed to the coupling between the graphene and the substrate, which could greatly facilitate the cooling of hot electrons and hot phonons. For suspended graphene lack of the coupling, charge carriers need a longer time to decay and become constant at higher pump fluence. Laser power dependent Raman spectra collected in both supported and suspended graphene also confirmed the existence of hot phonons in suspended graphene at low laser fluence. This observation provide a possibility of tuning the charge carrier dynamics in graphene by different substrates. [1] Libai Huang, Gregory V. Hartland, Li-Qiang Chu, Luxmi, Randall M. Feenstra, Chuanxin Lian, Kristof Tahy, and Huili Xing, Nano Letters, 10, 1308(2010).

4:30 PM Student

CC9, Polariton Enhanced IR-Reflectivity of Epitaxial Graphene on SiC: Biplob Daas¹; KM Daniels¹; S. Shetu¹; W.K Nomani¹; Goutam Koley¹; TS Sudarshan¹; MVS Chandrashekar¹; ¹University of South Carolina

Graphene is a two-dimensional form of sp² carbon in a honeycomb structure exhibits unusual electronic, optical and mechanical properties, being a promising candidate for nanoelectronics, advanced nanoelectromechanical systems (NEMS), etc. Because of graphene's high optical absorption, transmission/reflection spectra are a convenient characterization tool, a challenge for ultrathin layers (~ 2 nm). The IR-transmission of EG on semi-insulating SiC was studied by Dawlaty et. al(2008)[1], Thickness in monolayers(N in ML), momentum scattering time(τ) and Fermi level position(E_f) were extracted on semi-insulating substrate only because conductive SiC absorbs strongly in the IR. EG-induced optical responses in reflection are larger than for transmission [2], yielding greater measurement precision. The presence of a phonon-induced singularity in the dielectric function in SiC's reststrahlen band predicts the formation of a polariton at the EG/SiC interface, leading to enhanced reflectivity. We present polariton-enhanced reflectivity of EG grown on N+ substrates for accurate extraction of N, τ and E_f . IR-reflectivity was measured in the 2.5-25 μ m range with an N+ SiC reference. Our developed mathematical model fitted to the experiment to extract N, τ and E_f . Increasing N gives higher conductivity, leading to enhanced interaction with the incoming light, increasing reflectivity similar to the Drude model [3]. Thickness measurements by FTIR were correlated with X-ray photoelectron spectroscopy (XPS) confirming the accuracy of our model. Raman spectra show the presence of G, D and 2D peaks, while D/G ratio < 0.2 , confirming the presence of EG. In reflectivity measurements, 2ML EG, reflectivity increases by 20% in the Reststrahlen band, much higher than the $\sim 2\%$ observed outside the band. This behavior of the electromagnetic field at the SiC/EG interface constitutes the polariton. The model we used fit both Si-face EG and C-face EG equally well,

As layer thickness increased from 2-38ML's, τ increased from 4-20fs, while IEFI decreased from 105meV to ~ 20 meV, indicating that carrier scattering at the SiC/graphene interface is strong. By showing that $\tau \approx 1/\nu$ ns, the carrier concentration/ML, we argue that scattering is likely dominated by short-range interactions [4]. Polariton formation finds application in near field optical plasmon-polariton devices such as an efficient plasmonic waveguide, near-field superlenses. This characteristic was also used as gas sensor where adsorption doping occurs, changing IEFI, resulting in a change of reflectivity.

4:50 PM Student

CC10, CVD Graphene Metrology with Fluorescence: Jennifer Reiber Kyle¹; Ali Guvenc¹; Wei Wang¹; Jian Lin¹; Maziar Ghazinejad¹; Cengiz Ozkan¹; Mihrimah Ozkan¹; ¹University of California Riverside

In this work, we demonstrate a high-throughput metrology method for measuring the thickness and uniformity of entire large-area chemical-vapor deposition (CVD) grown graphene sheets on arbitrary substrates. This method utilizes fluorescence quenching microscopy (FQM), a novel technique for visualizing graphene that is based on the discovery that graphene quenches fluorescence via resonant energy transfer. Fluorescence quenching is visualized by spin-coating a solution of polymer mixed with fluorescent dye onto the graphene then viewing the sample under a fluorescence microscope. Graphene regions are identified by dark regions in the fluorescence image of the sample. The contrast between graphene and the substrate can be customized by controlling the thickness of the dye layer. Currently, FQM has only been used to visualize graphene-oxide and exfoliated graphene samples and has been unable to achieve quantitative characterization of the graphene samples. In this work, we calibrate the fluorescent quenching by the graphene layers, measuring the contrast between graphene and the substrate for different graphene layer thicknesses and dye layer thicknesses. Using the results from our fluorescence quenching calibration, we quantify the thickness and uniformity of entire CVD-grown samples. This is achieved by creating a large-scale, high-resolution fluorescence montage image of the entire graphene sample using a microscope with a motorized stage. Next, we identify graphene layers by histogram-based segmentation of the image based on contrast relative to the substrate. This work introduces a new method for graphene quantification that can quickly and easily identify the graphene layer thickness throughout the entire graphene sample.

Session DD: Nano-Magnetic, Magnetic Memory and Spintronic Materials

Thursday PM
June 23, 2011

Room: Santa Barbara Harbor
Location: Univ. of California-Santa Barbara

Session Chairs: Michael Flatte, University of Iowa; Xinyu Liu, University of Notre Dame

1:30 PM Student

DD1, Enhanced Spin Injection and Spin Lifetimes in Graphene: Wei Han¹; Roland Kawakami¹; ¹University of California, Riverside

Graphene is an attractive material for spintronics due to the low intrinsic spin-orbit and hyperfine coupling, which should lead to excellent spin transport properties, such as long spin lifetimes and spin transport lengths. Gate tunable spin transport and spin precession in non-local single layer graphene (SLG) spin valves at room temperature (RT) were demonstrated in 2007. This work and subsequent results identified two critical challenges which need to be overcome in order to realize the full potential of graphene for spintronics. The first important challenge is to enhance the spin injection efficiency, which is low due to the conductance mismatch between the ferromagnetic metal electrodes and graphene. The second important challenge is to enhance the spin lifetimes (50-200 ps), which are orders of magnitude shorter than expected from the intrinsic spin-orbit couplings ($\sim \mu$ s). To achieve high spin injection efficiency,

we demonstrated tunneling spin injection by inserting a thin insulating film (MgO/TiO₂) between Co and SLG. Utilizing sub-monolayer TiO₂ as the adhesion layer, we are able to grow smooth MgO film on top of graphene. With the tunneling contacts, we observe a non-local MR of 130 Ω at RT for a SLG spin valve with 2.1 μm spacing between the injector and detector with enhanced the spin injection efficiency of 26-30%. This compares favorably with the tunneling spin polarization of 35% measured by spin-dependent tunneling from Co into a superconductor across polycrystalline Al₂O₃ barriers. Gate tunable spin transport with tunneling contacts shows that the nonlocal MR (black squares) varies inversely with SLG conductivity (red line), which is consistent with theoretical predictions. Furthermore, tunnel barriers reduce the contact-induced spin relaxation and enhanced spin lifetimes are observed. For SLG spin valves with transparent contacts, and pinhole contacts, the spin lifetimes are in the range of 50-200 ps, which are consistent with previous studies. With tunnel barrier, which decrease the contact-induced spin relaxation, the spin lifetimes increased to ~450 ps at room temperature. For SLG, at room temperature, there is no obvious correlation between τ_s and D . Interestingly, when the device is cooled to $T = 4$ K, τ_s and D exhibit a strong correlation, with both quantities increasing with carrier concentration. Finally, we observe spin lifetimes as long as ~6 ns in bilayer graphene with tunneling contacts, which is the highest reported value in a graphene spin valve. In conclusion, we achieve tunneling spin injection and observe large MR with enhanced spin injection efficiency of 26-30%. Also, long spin lifetimes are observed both in SLG and bilayer graphene. These results are important advances for graphene to be used for spin computing or spin logic applications

1:50 PM Student

DD2, Enhancement of Spin Torque by Proximity to Other Domain Walls: *Elizabeth Golovatski*¹; Michael Flatte¹; ¹University of Iowa

The motion of domain walls due to the spin torque generated by coherent carrier transport [1] is of considerable interest for the development of spintronic devices [2]. We model two π Neel walls [3] separated by a variable distance, and calculate transport characteristics and spin torque through the system [4]. We model a realistic magnetization profile[5] for each π wall as a piecewise linear function, where the wavefunctions in each linearly varying segment can be solved analytically[6], and use transfer matrices to connect the segments. We find that for large separations, the domain walls show the resonant transmission behavior of a spin-dependent double barrier; for smaller separations, the transmission spectrum approaches that of a 2π wall of the same size as the double wall system. Similarly, the spin torque as a function of incident carrier energy shows several resonance peaks for larger separations between the two domain walls, and behavior more consistent with the 2π wall for smaller separations. The total spin torque across the system as a function of the separation between the π walls exhibits nonlinear behavior, with a peak at a particular separation, and then saturating for larger separations at a slightly lower value than at the peak. We find that the magnitude of this saturation spin torque is larger than both the equivalent torque for a 2π wall and the torque for two non-interacting π walls. This work is supported by an ARO MURI.

2:10 PM Student

DD3, Spin Seebeck Effect in MnAs/GaMnAs Bilayers: *Kurtis Wickey*¹; Christopher Jaworski²; Jing Yang³; Shawn Mack⁴; David Awschalom⁴; Joseph Heremans²; Roberto Myers³; Ezekiel Johnston-Halperin¹; ¹Physics Department, The Ohio State University; ²Mechanical Engineering Department, The Ohio State University; ³Materials Science and Engineering Department, The Ohio State University; ⁴Center for Spintronics and Quantum Computation, UCSB

A recently discovered thermo-transport phenomenon is the spin-Seebeck effect, which analogous to the charge Seebeck effect is a thermal redistribution of spin instead of electrons. First discovered by Uchida et al. in permalloy[1], subsequently in the ferromagnetic semiconductor GaMnAs [2], and the ferromagnetic insulator YIG [3], we observe it in the metallic ferromagnet MnAs and bilayer systems consisting of MnAs grown epitaxially on GaMnAs which results in an exchange bias of the GaMnAs layer[4]. A flux of spin-polarized particles induced by the temperature gradient enters the Pt strips

deposited on the samples, where the inverse spin Hall effect converts it to a voltage signal that we measure. The voltage, and thus the spin polarization, are proportional to the temperature gradient. The temperature dependence of this voltage is studied above and below the Curie temperatures of GaMnAs and compared with SQUID measurements. MnAs and GaMnAs exhibit different coercivities and we are able to isolate and measure the spin-Seebeck signal due to each ferromagnetic layer. Their spin-Seebeck coefficients also have opposite polarities. We study the temperature dependence of the spin-Seebeck signal in MnAs and GaMnAs with a goal of better understanding the mechanism of the spin-Seebeck effect in these materials. This work was supported by the NSF and the ONR.

2:30 PM

DD4, Universal Valence-Band Picture of the Ferromagnetic Semiconductor GaMnAs Obtained by the Resonant Tunneling Spectroscopy: *Shinobu Ohya*¹; Kenta Takata¹; Yufei Xin¹; Masaaki Tanaka¹; ¹The University of Tokyo

Extensive studies on the ferromagnetic semiconductor GaMnAs in the last decade have revealed a variety of unique features induced by the combination of its magnetic and semiconducting properties. However, complete understanding of the band structure of GaMnAs has not been achieved yet. Especially, there has been a hot dispute on the Fermi level (E_F) position of GaMnAs. Resonant tunneling spectroscopy is a very powerful method for investigating the band structure, because the observed resonant levels contain a lot of information, such as the effective mass, band offset, and E_F [1,2]. Here, using a precise etching technique and resonant tunneling spectroscopy, applied to a variety of surface GaMnAs layers, we show the universal valence-band (VB) picture of GaMnAs. We find that E_F exists in the bandgap for any of the GaMnAs samples with Mn concentrations ranging from 6 to 15%, and that the VB structure of GaAs is almost perfectly maintained and does not merge with the impurity band. Furthermore, the exchange splitting of the VB, which has been generally thought to be important for the appearance of ferromagnetism, is found to be very small (only several meV), even in GaMnAs with a high Curie temperature (154 K). Our new findings are largely different from the conventional understanding of the ferromagnetic semiconductors [3]. To investigate the VB structure, we used heterostructures comprising Ga_{1-x}Mn_xAs (4-20 nm)/ AlAs (5 nm)/ GaAs:Be (Be: 1×10^{18} cm⁻³) / p⁺GaAs(001). After the growth, we fabricated mesa diodes with various GaMnAs thicknesses ($d = 0-20$ nm) in the same sample wafer by carefully controlling the etching time for the GaMnAs layer. Since the Schottky barrier is formed at the surface of the GaMnAs layer due to the E_F pinning, the VB holes are confined by the Schottky barrier and the AlAs barrier. Thus, resonant levels are formed in the GaMnAs layer. With increasing d , the resonant energies approach the VB top in the bulk GaMnAs. In all the samples examined here, clear oscillations of the d^2I/dV^2 - V characteristics due to resonant tunneling were observed. The resonant levels were converged at a certain negative bias voltage with increasing d , which indicates that E_F exists in the bandgap. We found that these resonant levels are well reproduced by the calculated ones when assuming the same effective masses of holes as those in GaAs. This work was partly supported by Grant-in-Aids for Scientific Research, the Special Coordination Programs for Promoting Science and Technology, and FIRST Program of JSPS.

2:50 PM Student

DD5, Fe₃O₄/GaAs Hybrid Ferromagnet/Semiconductor Nanostructures: *Paul Reichers*¹; Jun Chen²; Christopher Murray²; Richard Kiehl¹; ¹UC Davis; ²University of Pennsylvania

A technology for creating hybrid ferromagnet/semiconductor nanostructures could enable the development of ultra-high-density non-volatile memories, low-power spintronic logic circuitry, and powerful quantum computing systems. The magnetic interaction between the two materials is the key that can open a door to electrical control of spin states, which could be highly exploited for design flexibility and device scalability. The injection of electrons into GaAs through ferromagnetic contacts could provide the spin-polarized current needed for various spintronic transistor, memory and logic proposals [1]. The modification of electron spin dynamics in GaAs by adjacent ferromagnetic regions via ferromagnetic proximity polarization [2] could allow control of the

quantum states of selected electron spins, as needed for quantum computing. Ultimately these hybrid structures must reach nanometer scale dimensions in order to exploit single domains and superparamagnetic properties and to allow ultimate scaling of circuitry. The nanoscale could be reached by using a bottom-up approach like DNA scaffolding [3] to self-assemble ferromagnetic nanoparticles into precise geometries. However, the assembly of nanostructures from solution introduces serious problems for attaining high-quality interfaces with suitable mechanical and electronic properties due to unwanted oxides and organics created during the process. Here we report a technique for bonding self-assembled arrays of oleic acid-coated Fe_3O_4 nanoparticles to a GaAs substrate, a technologically important pair of materials. Our protocol involves separate oxide and organic removal steps together with an optimized thermal annealing cycle. SEM and AFM images provide dramatic topographical evidence for strong bonding between the two materials. Solution phase synthesized 20-nm Fe_3O_4 nanoparticles suspended in hexane [4] were drop cast or adsorbed onto a (100) GaAs surface precleaned in NH_4OH . The samples were then exposed to a gentle oxygen plasma step to remove organics and subjected to various rapid thermal annealing cycles in the range of 200 to 400°C. The integrity of the adhesion between the nanoparticles and surface was evaluated by scraping the edge of a glass slide across the substrate and performing comparative analysis of the interface by SEM and AFM. Certain combinations of precleaning, oxygen plasma treatment and thermal annealing parameters were found to produce SEM images consistent with strong bonding between the nanoparticles and the substrate. Topographical AFM images add convincing evidence for a physical restructuring or intermixing at the interface. Further study will be needed to evaluate the chemical and electronic nature of the interface in these and other hybrid ferromagnet/semiconductor nanostructures. We believe that the techniques described here will be highly valuable for future studies.

3:10 PM Break

3:30 PM Student

DD6, Magnetic Depth Profile of Mn-Graded (Ga,Mn)As: *J. Leiner*¹; B. Kirby²; K. Tivakornsasithorn¹; Xinyu Liu¹; J. Furdyna¹; M. Dobrowolska¹; ¹University of Notre Dame; ²National Institute of Standards & Technology

In order to increase the storage density of magnetic memory while maintaining the requirements of magnetic recording technology – high signal to noise ratio, robust thermal stability, and low switching field (or current) – new types of recording media and technologies have been proposed. Graded media is one such approach, where thin films have a gradually changing anisotropy strength from top to bottom.[1,2] In such systems the thermal stability is maintained by the high anisotropy region, while the write field is reduced by the low anisotropy region. Although (Ga,Mn)As is not ideal for magnetic data storage due to its low Curie Temperature T_c (below 200 K), the ability to read and write using (Ga,Mn)As nanostructures through tunneling anisotropic magnetoresistance (TAMR) and spin-orbital coupling [3] make it a very interesting model system for studying the graded media approach, provided that the magnetic anisotropy of (Ga,Mn)As depends strongly on Mn concentration. In this work we have successfully fabricated (Ga,Mn)As films with vertically graded Mn concentration, and studied them with x-ray diffraction (XRD), superconducting quantum interference device (SQUID) magnetometry, and polarized neutron reflectometry (PNR). To achieve directional control of magnetic anisotropy, the films were grown either directly on a GaAs substrate (in-plane anisotropy), or on top of an (In,Ga)As buffer layer (perpendicular anisotropy). XRD clearly shows a wide shoulder on the left or right side of GaAs (400) peak, indicating the variation of Mn concentration in the films (see Fig. 1). SQUID results in Fig. 2 show the cubic anisotropy to be dominant for both in-plane and perpendicular anisotropy films at low temperature. The hard axis hysteresis loops feature a convex profile, suggesting a non-uniform anisotropy profile. At higher temperature, an unusual linear temperature dependence of magnetization is observed, suggesting a depth variation of T_c . PNR measurements are sensitive to the nuclear and magnetic depth profiles of thin films and multilayers. Figure 3a shows model-fitted spin-down and spin-up reflectivity data plotted as spin asymmetry (spin-

up – spin-down / spin-up + spin-down) for a 200 nm thick Mn-graded film on an (In,Ga)As buffer layer, at 6 K in a 100 mT (saturating) in-plane field. The solid (dashed) line in Fig. 3a is a best (constrained) fit corresponding to a non-uniform (uniform) magnetization depth profile shown in Fig. 3b. While this result confirms an inhomogeneous saturation magnetization profile, more detailed PNR measurements are planned to characterize the anisotropy and T_c profiles. The results will be compared with the Mn concentration profile determined by secondary ion mass spectroscopy measurements.

3:50 PM

DD7, Manganese-Doping of Group IV Semiconductor Surfaces and Nanostructures: Christopher Nolph¹; Kiril Simov¹; Catherine Jenkins²; Anders Glans²; Petra Reinke¹; ¹University of Virginia; ²Lawrence Berkeley National Laboratory

The magnetic doping of semiconductor materials is a critical contribution to the development of novel spintronics device structures. Mn-doping of group IV semiconductor materials is highly desirable for seamless combination of spin- and charge driven electronics. One of the critical limiters is currently the development of a suitable material, where Mn is placed in the correct bonding state, and not in germanide or silicide compounds. The main goal of our research is to develop a fundamental understanding of the relation between atomic-level bonding and the magnetic signature of the system. We combine STM (scanning tunneling microscopy) observations of material synthesis with measurement of the integral magnetic properties with magnetometry and XMCD (x-ray magnetic circular dichroism, Advanced Light Source). We studied the following systems: (A1) Mn-nanowires on Si(100) and their response to annealing, (A2) delta-doped Mn as Si-Mn-Si and Si-Mn-Ge synthesized from (A1), (B1) Ge-quantum dots (QD) doped by surface-deposition of Mn, and (B2) co-deposition of Mn during Ge QD growth. All growth processes were analyzed by STM, and we therefore possess atomic level information about the structure of Mn and the semiconductor matrix. Monoatomic Mn-wires (A1) form on the reconstructed Si(100) surface and are always oriented perpendicular to the dimer rows of the Si-surface. They are therefore an ideal vehicle for the fabrication of delta-doped Mn-layers, which are embedded within a semiconductor matrix (A2). The quality of Mn-wires is controlled by the density of defects on the surface. A phase diagram for wire growth has been established, and Monte-Carlo simulations are used to unravel the role of surface defects. The subsequent growth of the Si and Ge caps does not modify the Mn-wires. Mn-doping of Ge QDs has recently attracted considerable attention, and we will discuss the growth processes for (B1) and (B2) with special attention to the role of temperature, and bonding configuration with Mn. The development of the wetting layer and QD growth is only marginally influenced by the presence of Mn. Deposition of Mn on the QDs leads to roughening of the wetting layer surface, and formation of Mn-islands on the QD facets. The magnetic signature of structures (A2), (B1) and (B2) show either superparamagnetic behavior or a very narrow ferromagnetic loop. We will compare the magnetic data (saturation magnetization, spin and orbital moments, bonding configuration) across all nanostructures. C. Nolph and K. Simov performed the work in equal parts, and we collaborated with C. Jenkins and P. Glans for the XMCD measurements. The authors gratefully acknowledge the support by NSF awards CHE-0828318 and DMR-0907234. The Advanced Light Source is supported by the Director, Office of Science, Office of Basic Energy Sciences, of the U.S. Department of Energy under Contract No. DE-AC02-05CH11231.

4:10 PM

DD8, Unexpected Exchange-Bias Effect at Paramagnetic/Ferromagnetic Interfaces in Oxide-Based Structures: *Laura Steren*¹; Juan Rojas Sanchez²; Brittany Nelson-Cheeseman³; Mara Granada⁴; E. Arenholz⁵; ¹Centro Atomico Constituyentes; ²Centro Atomico Bariloche; ³University of California;; ⁴Laboratoire de Photonique et Nanostructures- CNRS; ⁵Lawrence Berkeley National Laboratory

Manganese oxides of the type A1-xBxMnO_3 (A: La; B: Sr, Ca, Ba) present a rich phase-diagram with a wide variety of magnetic and transport behaviours, whereas most of the compounds have a pseudo-cubic crystalline

structure. The most relevant properties of these materials are the high Curie temperatures of some ferromagnetic compounds of the family and the almost full spin-polarization of the electron bands at the Fermi level. For these reasons, manganite compounds are excellent candidates for spintronics devices and have been successfully integrated in room temperature tunnel junctions and spin-filter devices, among others. Another phenomenon useful for spintronic applications is the so-called exchange-bias effect (EBE). This phenomenon was first observed in Co-CoO particulate systems and is generally described as a uniaxial unidirectional anisotropy produced at a ferromagnet/antiferromagnet (F/AF) interface. In spite of the fact that there are still many open questions to solve, the exchange-bias effect is already applied in spin-valves as a way of artificially pinning ferromagnetic electrodes. The exchange-bias effect has been observed in oxide-based F/AF multilayers more recently. In this work we present the first evidences of exchange-bias in La_{0.75}R_{0.25}MnO₃/LaNiO₃ (LSMO/LNO) multilayers. The constituents of the bilayers are a ferromagnet (LSMO) and a Pauli paramagnet (LNO), respectively. The observation of the EB phenomenon is revealed by magnetization measurements performed at different thermo-magnetic conditions, measured in multilayers with different LSMO and LNO thicknesses. The temperature dependence of the EBE indicates that the effect is suppressed well-below the Curie temperature of the LSMO layers. The effect is enhanced in multilayers with multiple LSMO/LNO interfaces, indicating that the effect occurs in a few layers close to the interface. The mechanism underlying the exchange-bias effect in these structures is discussed in terms of charge reaccommodation in the atomic layers close to interfaces.

4:30 PM Student

DD9, Formation of Half-Metallic Ferromagnet Tunnel Junctions of Co₂FeSi/SiO_xN_y/Si Using Radical Oxynitridation Technique: Yota Takamura¹; Kengo Hayashi¹; Yusuke Shuto²; Satoshi Sugahara²; ¹Dept. of Electronics and Appl. Phys., Tokyo Inst. of Tech.; ²ISEL, Tokyo Inst. of Tech., and CREST, JST

Half-metallic ferromagnet(HMF) tunnel contacts using a full-Heusler alloy thin film are promising for the spin injector of spin-functional semiconductor devices, since the contacts enable them highly efficient spin-injection and can simultaneously solve the conductivity mismatch problem. Recently we reported that full-Heusler Co₂FeSi(CFS) alloy thin films were successfully formed by rapid-thermal-annealing(RTA)-induced silicidation technique using a single crystalline Si-on-insulator(SOI) film or an amorphous Si(a-Si) layer deposited on a thick SiO₂ film. Although CFS films were also formed by this technique on ultrathin tunnel barrier layer (thermally grown SiO₂ and ECR-sputtered SiO_xN_y films), a slight (nonnegligible) amount of Co and Fe atoms were found to diffuse into the substrate through the ultrathin barrier layers during the silicidation process.¹ In this study, we showed that the diffusion was dramatically suppressed using an ultrathin SiO_xN_y film formed by radical oxynitridation of a silicon surface, and demonstrated that a high quality L₂₁-CFS/SiO_xN_y/Si junction was successfully formed by the RTA-induced silicidation. The sample preparation was carried out using our multi-chamber system equipped with radical oxynitridation and molecular-beam deposition (MBD) chambers. First, thermal cleaning (800 °C) of a Si substrate was done in the ultrahigh vacuum oxynitridation chamber. Then, radical oxynitridation was performed using a commercially available radical source at a substrate temperature of 500 °C with an RF power of 300 W and an N₂ pressure of 2.7×10⁻³ Pa, in which radical oxygen was involuntarily produced from the quartz radical source. The resulting film was SiO_xN_y that was confirmed by XPS measurements. After the sample transferred to the MBD chamber without breaking ultrahigh vacuum, Si, Co, and Fe films were deposited on the sample in this order. Subsequently, RTA was performed at 800 °C for 4 min in N₂ atmosphere. When an ECR-sputtered SiO_xN_y thin film was used as a tunnel barrier, the diffusion of Co was observed in the substrate¹, as described above. On the other hand, SIMS profiles for the CFS/oxynitridation-SiO_xN_y sample revealed that the diffusion of Co and Fe was completely blocked by the SiO_xN_y layer. From XRD analysis, the CFS film on the SiO_xN_y layer was found to exhibit a highly (110)-oriented texture structure without any precipitation. Furthermore, strong superlattice CFS(200) and CFS(111) diffraction peaks

were also observed, indicating that the CFS layer was the L₂₁ structure with a high degree of L₂₁-order. Cross-sectional TEM images showed that the interfaces of the CFS/SiO_xN_y/Si junction were atomically flat without any interfacial layer, and the lattice image of the CFS grains was consistent with the highly oriented film structure. We will also discuss electrical characteristics of CFS/SiO_xN_y/Si junctions at the conference. The authors would like to thank Dr. R. Nakane of University of Tokyo.

4:50 PM Student

DD10, Characterization of L₂₁-Ordered Full-Heusler Co₂FeSi_{1-x}Al_x Alloy Thin Films Formed by Silicidation Technique Employing Silicon-on-Insulator Substrate: Mitsuhiro Satoh¹; Yota Takamura¹; Satoshi Sugahara²; ¹Dept. of Electronics and Appl. Phys., Tokyo Inst. of Tech.; ²ISEL, Tokyo Inst. of Tech., and CREST, JST

Full-Heusler Co₂FeSi_{1-x}Al_x (CFSA) alloy films are suitable for a high efficiency spin injector, since their Fermi-energy is theoretically predicted to lie near the center of the minority spin gap for x=0.25-0.5. Recently, we reported that full-Heusler Co₂FeSi (CFS) alloy thin films with a very high degree of L₂₁ order were successfully formed by the silicidation of an Fe/Co/silicon-on-insulator (SOI) multilayer, which reaction was induced by rapid thermal annealing (RTA)¹. In this study, we applied this technique to the formation of CFSA. Crystallographic features of CFSA alloy thin films strongly depended on the multilayer structures before RTA-induced silicidation. Firstly, the quality of CFSA films was investigated when the CFSA films were directly formed on SiO₂/Si substrates by sputtering with a stoichiometric Co₂FeSi_{0.5}Al_{0.5} target and successive RTA treatment (at T_A=350-800°C). In this case, the CFSA films exhibited only the disordered A2 structure even for higher annealing temperatures over 700°C. In a manner analogous to the RTA technique for CFS films, we examined the silicidation of an Al/Fe/Co/SOI multilayer, in which the RTA-induced silicidation was performed at T_A=600-800°C. The film thickness of each layer was set so that the resulting CFSA film had the stoichiometric composition. X-ray diffraction (XRD) for the CFSA film formed at 800°C showed the (111) superlattice diffraction, indicating the L₂₁-order structure. However, it co-existed with unidentified precipitates, and the surface was notably roughened. The silicidation of other layered structures, such as Fe/Al/Co/SOI and Fe/Co/Al/SOI, had no effect on quality improvement.
A high quality CFSA film was obtained using a Co₂FeAl_{0.5}-alloy/SOI layered structure. The Co₂FeAl_{0.5} alloy layer was deposited on a SOI layer by sputtering with a Co-Fe-Al alloy target, and then the RTA-induced silicidation was performed at T_A=600-800°C for 4min. From SIMS measurements, it was found that the Co, Fe, Si and Al atoms were almost uniformly distributed in the film for the sample annealed at 800°C and nearly stoichiometric composition was achieved. XRD for the CFSA film showed a strong CFSA (220) diffraction peak with narrow half maximum full-width, indicating that the film was highly (110)-oriented. The film was confirmed to be a (110)-oriented texture structure from pole figure analysis. These crystallographic features were the same as RTA-formed CFS films¹. The lattice constant of the CFSA film varied according to the Vegard's law, implying that the Al atoms preferentially occupied a part of the Si sites in the L₂₁ structure. Strong (111) and (200) superlattice diffraction lines were clearly observed, indicating a highly ordered L₂₁ structure. The above-described results indicate that the silicidation process of Co₂FeAl_x/SOI is essential to obtain high quality L₂₁-order CFSA films.

Session EE: Organic Thin Film and Crystalline Transistors: Devices and Materials

Thursday PM
June 23, 2011
Barbara

Room: State Street
Location: Univ. of California-Santa

Session Chairs: Alberto Salleo, Stanford University; David Gundlach, National Institute of Standards and Technology

1:30 PM Student

EE1, Quantitative Analysis of Lattice Disorder and Crystallite Size in Organic Semiconductor Thin Films, and Implications for Charge Transport: *Jonathan Rivnay*¹; Rodrigo Noriega¹; Michael Toney²; John Northrup³; R. Kline⁴; Alberto Salleo¹; ¹Stanford University; ²Stanford Synchrotron Radiation Lightsource; ³Palo Alto Research Center; ⁴NIST

Rational design of organic semiconductors, as well as thorough modeling of structure and charge transport in devices requires a detailed understanding of molecular packing and structural imperfections. It is often assumed that charge transport in films of both small molecule and polymer semiconductors is limited by defects at grain boundaries and by inter-grain morphology. While chemically the intra-grain packing motif can be tuned, it is still assumed that transport within a grain is much more efficient than between grains. Thus, little attention is paid to the degree of ordering in the crystalline regions. To this end, we measure the intra-crystalline order in high performance organic semiconductors. We utilize an X-ray peak shape analysis method developed by Warren and Averbach (1950), and incorporate a rigorous error propagation routine to establish confidence bounds in the results. This analysis yields information on grain size, and static, cumulative disorder called paracrystalline disorder. With this tool we investigate three prototypical organic semiconductors: the high performing n-type polymer P(NDI2OD-T2) (Polyera ActivInkN220), p-type polythiophene PBTTT, and p-type small molecule TIPS-Pentacene. By analyzing the paracrystalline disorder of three different materials in a variety of crystallographic directions, new insight is gained regarding the nature of molecular packing and transport in this class of materials. For the first time, we quantify the degree of paracrystalline disorder in a charge transport relevant (crystallographic) direction. We find that PBTTT π -stacking has a large, 7.3% paracrystalline disorder (where <1% is considered highly crystalline, and 15% is considered amorphous). For a high performing (up to 1 cm²/Vs) polymer that is so often regarded as highly ordered due to its terraced topography and strongly diffracting lamellar stacks, the π -stacking direction is surprisingly disordered. We find that such high disorder dominates peak broadening, and we formulate a disorder-induced correlation length. Furthermore, by modeling the band structure of a collection of π -stacked PBTTT segments with different degrees of paracrystalline disorder, we show that, compared to the ideal completely ordered microstructure, the experimentally determined disorder introduces a tail of localized states which can act as traps for charge transport. These calculations provide physical justification for the mobility edge model.

1:50 PM Student

EE2, Following Charge-Trapping Chemical Reactions in Pentacene Films by Selective Chemical Doping and Wavelength-Resolved Electric Force Microscopy: *Louisa Brown*¹; Vladimir Pozdin¹; Justin Luria¹; Chad Lewis¹; John Marohn¹; ¹Cornell University

Despite continued study, the nature of charge traps in pentacene and related polyacenes remains poorly understood. Numerous products of pentacene degradation have been identified in solution, in the solid post sublimation, and in thin films. Which, if any, of these chemical defects is responsible for charge trapping remains unclear. It has been demonstrated in a bulk current-voltage measurement that trapped charge in pentacene can be rapidly cleared under illumination and that the activation energy and prefactor for charge trap formation is consistent with a chemical reaction. Trap clearing rates have recently been measured in a scanned probe microscope experiment as a function

of illuminating wavelength to obtain a (localized) trap clearing action *spectrum* for the first time. In this recent work, a large peak in the pentacene trap-clearing spectrum was observed at an energy well above the peak absorbance of pentacene, which was explained in terms of chemical charge trapping and a new trap-clearing mechanism involving an internal photoexcitation of the charged trap species. Based on quantum-mechanical calculations of the charged trap species' absorbance spectra, pentacene-6(13*H*)-one and 6,13-dihydropentacene were identified as likely charge trap precursors. These precursors are proposed to react with pentacene cation radicals to form charged trap molecules. To provide even more definitive evidence that charge trapping in polyacenes is the result of chemical reactions of pentacene cations with chemical defects, we have chemically synthesized two proposed pentacene defect molecules and have developed a method for co-depositing these defect molecules in thin films with pentacene. We have studied these films by electric force microscopy with *in situ* variable-wavelength illumination. We find that doping with pentacene-6(13*H*)-one gives a transistor whose localized trap-clearing spectrum is in quantitative agreement with that observed in aged pentacene thin-film transistors. Studies of localized trap-clearing spectra for 6,13-dihydropentacene as a dopant are underway. Our work suggests that acquiring localized trap-clearing spectra and comparing spectra of nascent and intentionally doped films is a powerful approach to identifying the chemical reactions leading to charge-trap formation in polyacene films.

2:10 PM Student

EE3, Molecular Contact Doping for Organic n-Channel TFTs and Fast Complementary Circuits: *Frederik Antel*¹; Tobias Canzler²; Jan Blochwitz-Nimoth²; Florian Letzkus³; Joachim Burghartz³; Ute Zschieschang¹; Hagen Klauk¹; ¹Max Planck Institute for Solid State Research; ²Novald AG; ³IMS CHIPS

The charge-carrier mobility in most organic semiconductors that are useful for air-stable n-channel thin-film transistors (TFTs) is approximately one order of magnitude smaller than that in state-of-the-art p-channel TFTs [*Chem. Soc. Rev.* 39, 2643, 2010]. Therefore, the dynamic performance of air-stable organic complementary circuits is usually limited by the performance of the n-channel TFTs. To improve the dynamic characteristics of organic circuits, a common approach is to reduce the TFT channel length in order to increase the transconductance and reduce the gate capacitance. However, the drain current in short-channel organic TFTs and hence the speed of aggressively scaled circuits is often limited by the energy barrier at the interface between the semiconductor and the contacts. To some extent, this energy barrier can be reduced by choosing a contact metal with a work function matching the frontier orbital energy of the semiconductor [*J. Appl. Phys.* 96, 7312, 2004]. Further improvements are possible by contact doping, in the case of n-channel TFTs either with alkali metals, reduced semiconductor analogs, cationic dyes, or molecules with high-lying HOMO [*App. Phys. Lett.* 97, 243305, 2010]. Here we utilize the molecular dopant NDN-44 (Novald) to reduce the contact resistance in air-stable hexadecafluorocopperphthalocyanine (F₁₆CuPc) n-channel TFTs. The HOMO of the dopant is sufficiently high (-4.4 eV) to allow electron transfer to the LUMO of the semiconductor (-4.5 eV). Transistors with channel lengths between 1 and 60 μ m were fabricated by vacuum deposition in combination with high-resolution silicon stencil masks [*IEDM*, 21.6, 2010]. The TFTs consist of Al gates, an AlOx/SAM gate dielectric (5.7 nm thick), the organic semiconductor (30 nm), and a thin dopant layer (~2.5 nm) deposited only underneath the Au top contacts. The linear-region mobilities of F₁₆CuPc TFTs without doping (contact resistance: 48 k Ω -cm) range from 0.002 cm²/Vs (L = 1 μ m) to 0.03 cm²/Vs (L = 60 μ m). For TFTs with contact doping (contact resistance: 9 k Ω -cm) the mobilities are between 0.01 cm²/Vs (L = 1 μ m) and 0.06 cm²/Vs (L = 60 μ m). Since the off-state drain current (~1 pA) is not affected by the contact doping, the TFTs have an on/off current ratio as large as 10⁷. The contact doping greatly improves the linearity of the I_D/V_{DS} curves for small V_{DS}. We also combined n-channel F₁₆CuPc TFTs with p-channel dinaphtho[2,3-b:2',3'-f]thieno[3,2-b] TFTs and realized air-stable organic complementary ring oscillators operating with low supply voltages (< 5 V). Incorporating NDN-44 as a contact dopant into the n-channel TFTs leads to a reduction in signal delay per stage from 30 μ s to 20 μ s (for a supply

voltage of 3 V), confirming the potential of area-selective contact doping to improve the dynamic performance of organic n-channel TFTs and organic complementary circuits.

2:30 PM Student

EE4, Charge Trapping and Localization Due to Paracrystalline Disorder in High Performance Polymeric Semiconductors: *Rodrigo Noriega*¹; Jonathan Rivnay¹; John Northrup²; R. Joseph Kline³; Michael Toney⁴; Alberto Salleo¹; ¹Stanford University; ²Palo Alto Research Center; ³NIST; ⁴Stanford Synchrotron Radiation Lightsource

Disorder within crystallites of organic semiconducting materials has been shown to be strongly linked with electronic processes. One type of disorder is positional fluctuations within the crystalline regions of semicrystalline polymers. The positional fluctuations of monomer units in these materials are described by the paracrystallinity model developed by Hosemann et al. An experimental, quantitative measure of the disorder parameters inside polymer crystallites is performed using the X-ray diffraction lineshape analysis of Warren and Averbach. The use of synchrotron radiation and a variety of diffraction geometries allows us to study disorder in the different crystallographic directions even for weakly scattering materials like semicrystalline semiconducting polymers. The usual assumption of 3D ordering in crystalline domains is disputed, since one of the most ordered materials in the lamellar direction, the high performance p-type polymer PBTTT, is strongly disordered in the π -stacking direction. This highly disordered character in a direction which is closely related to charge transport is present in a variety of materials reported in the literature. The implications of such a disordered behavior are studied with a tight binding model using density functional theory calculations to determine the intersite transfer integral. Localized tails in the DOS due to disorder can have a significant effect on electronic and optical properties of these materials. A closed-form expression for the DOS of an ensemble of paracrystalline 1D chains, as well as for a localization length of states in the tail is obtained. Increasing the paracrystalline disorder has the double effect of creating a tail of localized states, but also decreasing the delocalization length of states in the band. For extremely large values of paracrystallinity, the band disappears and we are left with a single population of localized states. Thus, the validity of different charge transport models such as the mobility edge or hopping in a localized DOS can be verified by quantitatively measuring lattice disorder in the crystallographic directions related to charge transport in organic semiconductors.

2:50 PM Student

EE5, Probing the Microstructure of Buried Polymer-Polymer Interfaces with Thin Film Transistors: *Justin Cochran*¹; Michael Chabinye¹; ¹University of California Santa Barbara

Improvement in the performance of polymeric thin film transistors (TFTs) require a better understanding of how the dielectric interface impacts the formation of the semiconducting polymer interfacial microstructure. The charge carrier mobility of thiophene-based polymers strongly depends on the nature of the molecular orientation at the semiconductor/dielectric interface. The nature of the surface of the dielectric layer has been widely reported to have a significant impact on mobility and overall device behavior but the connection between morphology and electrical performance is not well understood. Furthermore, gate voltage-dependent mobility, variations in threshold voltages, and bias stress have been attributed to dielectric interface effects. To better understand these issues, a dry lamination method utilizing poly(dimethyl siloxane) (PDMS) was used to fabricate polymer-polymer TFTs to avoid any interactions of the dielectric with the solvent used to cast the semiconducting polymer. This dry lamination process enabled the fabrication of a wide variety of semiconducting-dielectric polymeric devices, enabling a direct comparison of how devices performed as a function of the target polymer dielectric and an indirect measure of the interface microstructure as a function of their current-voltage characteristics. Films of two thiophene based semiconducting polymers are formed initially on a known dielectric, octyltrichlorosilane (OTS) modified 150 nm thermal oxide (SiO₂). Using the PDMS lamination process, films are transferred to the target polymer dielectric

in their two states, as cast and annealed above the first liquid crystal transition. The carrier mobility in films on OTS/ SiO₂ before and after lamination was determined for comparison with results measured on the polymeric dielectrics. These results are then compared with films annealed at the semiconductor's T_{lc}¹ on the target polymer dielectric in order to quantify the effects on the interface microstructure. The electrical characteristics of the TFTs were compared to the bulk morphology determined by grazing incidence wide angle x-ray scattering (GIWAX). TFTs thermally processed, annealing at the semiconductor's T_{lc}¹, on polystyrene (PS) exhibit a factor of 10 decrease in field effect mobility and an increase in bias stressed threshold voltage, $> |V|$, as a function of processing on the polymer dielectric. Observed GIWAX results show an increase in crystallite size and orientation distribution for films annealed on the polymer dielectric but do not give a direct measurement of the interface nor show any change in p-p spacing. This combined data suggests that the semiconducting polymer's interfacial microstructure has undergone a significant change directly attributed to interactions with the polymeric dielectric.

3:10 PM Break

3:30 PM EE6, Late News

3:50 PM Invited

EE7, Materials Requirements for Low-Voltage Flexible Organic Transistors and Circuits: *Hagen Klauk*¹; ¹Max Planck Institute for Solid State Research

Organic thin-film transistors (TFTs) are of interest for applications that require electronic functionality with low or medium complexity distributed over large areas on unconventional substrates, such as flexible plastics or paper. Generally these are applications in which the use of silicon devices and circuits is technically or economically not feasible, such as rollable flat-panel displays and large-area conformable sensor arrays. Active-matrix displays based on high-efficiency organic light-emitting diodes (OLEDs) require TFTs that can be operated with voltages of about 3 V. A promising approach to organic TFTs that can be operated with such low voltages are gate dielectrics based on a thin, plasma-grown AlO_x layer in combination with an alkylphosphonic acid self-assembled monolayer (SAM); these hybrid gate dielectrics have a thickness of about 5 nm and a capacitance close to 1 $\mu\text{F}/\text{cm}^2$. The static and dynamic performance of low-voltage organic p channel TFTs with AlO_x/SAM gate dielectrics and relaxed lateral dimensions is already sufficient for flexible OLED displays with VGA resolution, where the TFTs operate with frequencies of a few tens of kilohertz. Increasing the performance of organic TFTs into the Megahertz regime requires scaling of the lateral TFT dimensions to 1 μm and below, which can be achieved, for example, by high-resolution inkjet-printing or stencil-mask techniques, ideally in combination with stable contact doping. Further advances are also required in the environmental stability of organic TFTs and in the development of high-mobility organic n channel TFTs to enable low-voltage, low power organic complementary circuits.

4:30 PM

EE8, Organic Transistor-Based Memory: *Martin Burkhardt*¹; Abdesselam Jedaa²; Michael Novak²; Marcus Halik²; ¹Materials Department, University of California Santa Barbara, Santa Barbara, United States; ²Institute of Polymer Materials, University Erlangen-Nürnberg

Basic organic electronics such as capacitors, transistors, and memory devices focus on novel organic materials and concepts for future applications. Processability at low temperatures from solution ($T < 150^\circ\text{C}$) is the key feature of organic electronics, allowing the use of low-cost flexible polymeric substrates (Polyethylene naphthalate, Polyethylene terephthalate). Solution processes enable large area fabrication of organic electronics using printing techniques and molecular self-assembly, respectively. The presented work will focus on a hybrid dielectrics formed by an aluminum/aluminum oxide layer (Al/AlO_x) in combination with a self-assembled monolayer (SAM; here: alkyl phosphonic acids). The key benefit of this hybrid dielectric is low-voltage operation in organic electronics due to reduced dielectric layer thicknesses (7nm). Low-voltage operation and processability on flexible substrates are crucial for low energy consumption and adaption to mobile devices. Recent results show

the impact of nano-scale variations on molecular lengths in the formation of alkyl phosphonic acid monolayers (C6-, C10-, C14-, C18-alkyl phosphonic acids). The alkyl chain length is correlated with device performance and leakage currents in organic electronics, specifically capacitors and transistors. Non-linear behavior of leakage current versus alkyl chain length is observed in experiments and correlated with Molecular Dynamics (MD) Simulations. MD Simulations display an increasing gap formation within the monolayer – without displaying pinholes – resulting in a reduced effective monolayer thickness. The theoretical calculations link the nonlinear correlation of the alkyl chain length and the leakage currents to the experimental results. Subsequently, hybrid gate dielectrics with alkyl phosphonic acids on Al/AIO_x were used to develop flexible memory cells (bottom electrode/SAM/Al/AIO_x/SAM/top electrode). A hybrid dielectric stack is used in a floating gate memory transistor geometry, integrating the functionality of a capacitor and transistor in a single device. Devices which are processed, stored, and characterized in air (without encapsulation) display high retention times on the order of 2 hours at low-programming voltages ($\pm 2V$). Utilizing these results a novel memory approach based upon hybrid gate dielectrics incorporating a new molecular design was developed. The new molecular design unites the previously discussed insulation behavior of a monolayer (alkyl phosphonic acid as SAMs anchor group and spacer) and the redox activity of a fullerene (SAM's head group). Low-voltage programming behavior is obtained ($\pm 2V$) at retention times higher than 2 hours. The programming effect is based upon the fullerene moiety. In addition, studies demonstrate a highly controlled deposition of mixed monolayer at different molecular ratios. The film formation is studied by amplitude modified atomic force microscopy. Electronic characterization shows that the memory behavior of programmable thin film memory transistors strongly correlates with the amount of fullerene-based molecules within the monolayer. The retention time and the programming ratios are controlled by the quantity of fullerene alkyl phosphonic acids within the monolayer.

4:50 PM Student

EE9, From Nano- to Micro-Scale Control of Crystalline Order in Soluble Small-Molecule Organic Semiconductors: *Jeremy Ward*¹; *Marsha Loth*²; *John Anthony*²; *Oana Jurchescu*¹; ¹Wake Forest University; ²University of Kentucky

A major challenge with organic thin-film transistors (OTFTs) rests in the ability to judiciously control the magnitude of the field-effect mobility, as this is critically affected by thin-film microstructure. Often, a higher degree of order in the molecular arrangement within the organic semiconductor film results in increased mobilities. In this work we describe our efforts towards tuning this order over a broad distribution of length scales in fluorinated Anthradithiophenes (ADTs). At nano-scale level, the solid state order can be tuned during the synthesis process, through chemical modifications, i.e. the choice of the substituent to the ADT backbone. Through the use of various functional groups, such as methyl (TMS), ethyl (TES), n-propyl (TPS), isopropyl (TIPS), and tri-sec-butylsilyl ethynyl (TSBS) to 2,8 difluoro- anthradithiophene (ADT) backbone, we show that we are able to obtain very different molecular packings. Correspondingly, the mobility varies from $10^{-3} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for a 1D-p stacking motif, to $1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for a 2D-p stacking motif. Furthermore, we show that we can modify the solid state order over tens of micrometers by controlling processing parameters during the fabrication of OTFTs. For example, for the case of 2,8-difluoro-5,11-bis(triethylsilylethynyl) anthradithiophene (diF-TESADT), through the use of fluorinated self-assembled monolayers (SAMs) on the transistor contacts, the film presents a high degree of order, with organic molecules being co-facially packed, (001) preferred orientation, in the regions where interactions between organic semiconductor and SAM are present. Therefore, the transistor has superior electrical characteristics: devices having PFBT (pentafluorobenzenethiol) treated contacts exhibit mobilities on the order of $0.1 - 0.5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. For untreated surfaces, a mixture of fine film regions with (001) and (111) oriented crystals are present, yielding mobilities on the order of $0.01 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. The latter morphology obtained in diF-TESADT during device processing is similar to that present in diF-TSBSADT single crystals, and we show that the two types of devices exhibit similar electrical properties. Thus, by combining the two aforementioned methods, we show that we are able to

fine tune molecular packing in organic thin-films on various surfaces, and that the degree of order dictates electronic properties in the transistor channel.

Session FF: Epitaxy Material and Devices II

Friday AM
June 24, 2011

Room: Corwin East
Location: Univ. of California-Santa Barbara

Session Chairs: Seth Bank, University of Texas at Austin; Archie Holmes, University of Virginia

8:20 AM

FF1, n+GaAs Sheet Resistance Saturation and Implications to BiHEMT Growth: Kevin Stevens¹; Nuvée Kunathai¹; Tom Nunes¹; Charles Lutz¹; Wayne Johnson¹; ¹Kopin Corporation

A processing challenge of BiHEMT (HBT + pHEMT) epi structures is the relatively large depth of field over which a stepper must focus and expose both the HBT and pHEMT patterns. Any reduction in this height differential would be beneficial to help alleviate this processing challenge. The collector layers are the obvious choice to focus these efforts as they make up a large percentage of the height differential. Thinning the collector layer tends to reduce collector and transistor breakdown voltages and degrades device robustness. Thinning the subcollector layer increases the collector sheet resistance. Since most state-of-the-art production subcollector layers are already doped near an upper limit commonly referred to as "saturation," increasing doping is not an option. In this work, we explore these maximum doping and minimum sheet resistance limits in order to better understand and push beyond them. As-grown Si-doped n+GaAs bulk layers, grown to calibrate the subcollector layers, exhibit sheet resistances which reach minimum values of $\sim 120/\text{sq}$ (layer thickness $\sim 5000 \text{ \AA}$). In real world BiHEMT growth however the subcollector is subjected to further annealing as the rest of the HBT layers are grown on top of the pHEMT. We observe that thick Si-doped n+GaAs layers, when subjected to additional annealing mimicking the temperature cycle of typical HBT growth, exhibit $\sim 20\%$ increase in sheet resistance. This higher resistance is a consequence of a lower active doping limit as compared with the unannealed bulk samples. These data indicate the dominant factor limiting minimum attainable sheet resistances in n+GaAs:Si HBT layers is the thermal treatment the layers receive during additional growth as would be the case in a BiHEMT device. These results can be explained via the interaction of three phenomena: a) an increasing equilibrium concentration of gallium vacancies with Fermi level, b) the tendency of gallium vacancies to form complexes with silicon donor atoms thereby rendering the dopant atom inactive, and c) the influence of growth conditions on the non-equilibrium state under which GaAs is grown [1]. The treatment in Fushimi et al. [1] focused on these mechanisms in the context of Si-doped n+GaAs layers. To our knowledge, no significant study has been conducted which examines this phenomenon for other dopant species. We show that GaAs doped with Te exhibits substantially different behavior upon annealing than that for Si-doped samples. More specifically, no reduction in the free carrier electron density is observed upon annealing. In this presentation we will discuss these results as well as additional studies investigating Sn as the n-type dopant in order to further explore mitigations for the sheet resistance limits evident with Si doping.

8:40 AM Student

FF2, Metamorphic p-i-n InGaAs Photodetectors Grown by MOCVD: Yan Gao¹; Zhenyu Zhong¹; Hu Liang¹; Yu Geng¹; Shaoqi Feng¹; Kei May Lau¹; Andrew W. Poon¹; ¹HKUST

High performance and high speed optoelectronic components grown and fabricated on InP substrates are widely used in today's fiber-optic communication systems operating at $1.55\mu\text{m}$. Due to the limited wafer size, high cost, and the fragile property of InP, metamorphic devices grown on either GaAs or Si substrates are more desirable for low cost and high yield products. Metamorphic devices grown on Si substrates also have the potential to integrate with silicon photonics. In our group, InP/GaAsSb/InP mHBTs with a composite buffer on GaAs substrates by Metalorganic chemical vapor deposition (MOCVD) has

been successfully demonstrated [1]. In this work, p-i-n InGaAs photodetectors (PDs) lattice-matched to InP were grown on GaAs substrates in an Aixtron AIX-200/4 MOCVD system using the same buffer techniques. The p-i-n structure includes 120nm p+ InGaAs , $850\text{nm undoped InGaAs}$ and 150nm n+ InP layers. Top illuminated, circular devices with a different diameter ($60\mu\text{m}$, $40\mu\text{m}$, $30\mu\text{m}$, $20\mu\text{m}$) were fabricated for speed performance evaluation. Pt/Ti/Pt/Au and Ni/Ge/Au were deposited as the p-type and n-type ohmic contact metal, respectively. Polybenzobisoxazole (PBO) was coated as passivation layer to help suppress dark current and minimize parasitic capacitance between the substrate and the ground-signal-ground (GSG) pads. No anti-reflection layer was used in our devices. DC and RF response measurements were carried out. The dark current of a $40\mu\text{m}$ device was measured to be 27nA at a reverse bias of 5V , corresponding to a current density of about 2mA/cm^2 , which is comparable to the results reported by Dentai et al. [2]. This is also somewhat larger than the best reported devices grown by MBE [3]. $60\mu\text{m}$ diameter devices showed a high responsivity of about 0.5A/W at $1.55\mu\text{m}$ corresponding to a quantum efficiency of 40% . The frequency responses were measured with a vector network analyzer. A 3dB bandwidth of 5GHz was achieved in $60\mu\text{m}$ devices at -5V while smaller devices, $40\mu\text{m}$, $30\mu\text{m}$ and $20\mu\text{m}$ PDs obtained a 3dB bandwidth exceeding 10GHz , which was the frequency upper limit of our present measurement system. It is believed that higher bandwidth could be achieved by further reduction of the parasitic capacitance. Based on the devices grown on GaAs substrates, the same p-i-n structure was grown on a Si substrate using previously reported buffer techniques [4]. A responsivity of about 0.45A/W and a 3dB bandwidth of 1.3GHz at -5V bias were obtained in $60\mu\text{m}$ devices. The dark current was relatively large due to the large dislocation density propagated to the InGaAs layer. Further optimization on the growth and fabrication process is in progress.

9:00 AM Student

FF3, Optimized Growth Condition and Dot Geometry in InAs/InGaAs Sub-Monolayer Quantum Dot Infrared Photodetector: Jiayi Shao¹; ¹CHTM at University of New Mexico

We report the optimized growth of the InAs/InGaAs Sub-Monolayer (SML) Quantum Dot Infrared Photodetector (QDIP) with the small dot base diameter as 7 nm by molecular beam epitaxial (MBE). In a previous study I we optimized the dot geometry and quantum confinement of Stranski-Krastnov (SK) QDs QDIP by using InAlGaAs capping material. The results indicate that the engineering SK QDs with small base diameter (12 nm) and high height (8 nm) have better 3-D quantum confinement, behave more close to the "artificial atom" and have enhanced normal incidence absorption. Recently, several groups have reported growth of InAs/InGaAs SML QDs on GaAs without wetting layer 2-3. Contrast to "dome-shaped" SK QDs, the "cylinder-shaped" SML QDs has advantages including small base diameter, better 3-D quantum confinement, high dot density, adjustable height of the dot geometry, and no wetting layer needed. In this work, we designed and grow InAs/InGaAs SML QDs infrared photodetector on (100) S. I. GaAs substrate using VG-80 solid-source molecular beam epitaxy (MBE) system with a cracked As₂ source. The diagram of the growth structure and the TEM image are shown as Fig. 1 (a) and (b). The InAs/InGaAs SML QDs were formed as 2 layers of 0.5 ML InAs evenly embedded in 5.1 nm GaAs . The active region consisted of 10 periods of SML QDs separated by $50\text{ nm Al}_{0.16}\text{Ga}_{0.84}\text{As}$ barrier is sandwiched by 1000 nm bottom and 200 nm top N+ GaAs contact layer. The growth conditions were optimized in several factors. The photoluminescence measured at room temperature indicates the SML QDs with the V/III flux rate ratio as 30, growth temperature as 540°C , growth rate as InAs- 0.159 ML/s and GaAs- 0.787 ML/s , and 10 sec interruption both before and after InAs deposition have the highest intensity. High resolution Scanning TEM image of the SML QDs in Fig. 2 reveals that the two layers of InAs/InGaAs SML QDs is confined evenly in the 5.1 nm GaAs and they are vertically self-aligned to each other. The dots have InAs core surrounded by InxGaAs alloy with $7\text{-}8\text{ nm}$ base diameter and total $5\text{-}6\text{ nm}$ height. There is no wetting layer observed. After the standard fabrication, the SML QD infrared photodetector shows photoresponsivity of 0.4 A/W and photodetectivity of $0.5 \times 10^{10}\text{ cmHz}^{1/2}/\text{W}$ at 77K -1.8V for a peak wavelength of 10.1 micron (Fig. 3 and Fig. 4). The experimental set up of

polarized spectral response measurements is shown in Fig. 5 (a) and (b). The results in Fig. 5 (c) indicate that the ratio of the s/p polarized spectral response of the SML QDs QDIP at 77K is ~17%, which is comparable to the ratio of conventional SK QDs QDIP.

9:20 AM

FF4, Epitaxial Growth of InGaAs/InAlAs/InP Quantum Cascade Lasers by Metalorganic Chemical Vapor Deposition: Yong Huang¹; Jae-Hyun Ryou¹; Russell Dupuis¹; Christian Pflugl²; Federico Capasso²; Kewei Sun³; Alec Fischer³; Fernando Ponce³; ¹Georgia Institute of Technology; ²Harvard University; ³Arizona State University

We report on the systematic study of growth conditions in relation to structural, optical, and morphological properties of lattice-matched $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{InP}$ heterostructures and quantum cascade lasers (QCLs) grown by metalorganic chemical vapor deposition (MOCVD). The growth parameters in this study include the substrate misorientation, growth temperature, and V/III ratios for each layer and epitaxial structures. For microscopic surface morphology, while the InGaAs growth undergoes a step-flow mode regardless of the substrate misorientation, the surface of InP layer has different features depending on the misorientation. At a small off-cut angle of 0.02° , the surface is very rough characterized by high-density hillocks. At a relatively large off-cut angle of 0.25° , a step-bunched surface is observed. Using InP substrates with a misorientation of $0.07^\circ \pm 0.02^\circ$ from (100), the effects of growth temperature and V/III ratio on epitaxial materials are studied to find the optimized growth parameters for the QCL structures. InGaAs/InAlAs superlattice (SL) structures exhibit a stable step-flow growth at the temperature of 720°C and V/III ratios of 116 for InGaAs and 21 for InAlAs. According to secondary-ion mass spectrometry, the O and C concentration in InAlAs layers is only 2×10^{16} and $7 \times 10^{15} \text{ cm}^{-3}$, respectively. When applying these optimized conditions to the QCL growth, step-flow surface, abrupt interfaces, low strain, and precise periodicity are obtained, indicating an excellent capability of MOCVD in controlling the interface, thickness, composition, and morphology of the QCL structures. The active region of the QCLs consists of 35 stages of the InGaAs/InAlAs SL: **34/14/33/13/32/15/31/19/30/23/29/25/29/40/19/7/58/9/57/9/50/22 Å**, where InAlAs layers thicknesses are in bold and the underlined layers are doped with $n \sim 6 \times 10^{16} \text{ cm}^{-3}$. The active region is sandwiched symmetrically by $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ waveguide layers, InP cladding layers, and InP plasmon-confinement layers. The total thickness of the epitaxial structure is 11.3 μm . Atomic-force microscopy (AFM) image of the QCL structure shows excellent surface morphology with a root-mean-square (RMS) roughness of only $\sim 0.09 \text{ nm}$ for $10 \times 10 \mu\text{m}^2$ scanning area. Bright-field transmission electron microscopy (TEM) images of the core active region show abrupt interfaces and uniform SL thickness along the growth direction. The wafer is processed into 27.5- μm -wide 2-mm-long ridge structure lasers. The devices exhibit a threshold current density of $J_{\text{th}} \sim 2.0 \text{ kA/cm}^2$ and a threshold voltage of $\sim 9.1 \text{ V}$. The slope efficiency is $\sim 550 \text{ mW/A}$ and the maximum peak power is 480 mW. The emission wavelength of the laser is $\lambda \sim 9.2 \mu\text{m}$, close to the designed 9.3 μm .

9:40 AM Student

FF5, GaInNAsSb Quantum Wells with Strain-Compensating GaAsP Layers for GaAs-Based 1.55 μm Lasers: Tomas Sarmiento¹; James Harris¹; ¹Stanford University

GaInNAsSb alloys enable the realization of long-wavelength lasers on GaAs substrates. Despite challenges in material growth relatively low threshold 1.55 μm edge-emitting lasers have been demonstrated. These lasers employ tensile-strained GaNAs barriers to compensate the high compressive strain of the GaInNAsSb quantum well (QW). This is indispensable to avoid degradation of the optical quality of the QW. Unfortunately, the small conduction and valence band offsets between GaInNAsSb and GaNAs allow the carriers to escape thermoinically from the QW into the barriers, where they recombine non-radiatively due to the poor optical quality of GaNAs. These processes result in higher thresholds and a degradation of the temperature sensitivity (T_0) of the lasers. Therefore, to improve the performance of the lasers it is necessary to optimize the thickness of the GaNAs barriers or alternatively use GaAsP

layers, which are also tensile strained on GaAs, to compensate the strain in the quantum well. In this work, we investigate the effects of barrier and well thicknesses on the luminescence efficiency of GaInNAsSb/GaNAs quantum wells and present the growth and characterization of GaInNAsSb quantum wells with GaAsP strain compensating layers. The quantum well structures were grown by molecular beam epitaxy and consist of a 300 nm GaAs buffer layer, a GaInNAsSb QW surrounded by either GaNAs or GaAs/GaAsP barriers, and a 50 nm GaAs cap layer. Photoluminescence (PL) measurements of GaInNAsSb SQWs with different GaNAs barrier thickness indicate that the optical quality of the QW degrades considerably if the strain in the well is not fully compensated by the strain in the barriers. On the other hand, over compensation of the strain does not result in a significant improvement of the luminescence efficiency as confirmed by PL measurements of QWs with different well thicknesses. To investigate the use of GaAsP strain compensating layers GaInNAsSb QWs were surrounded by a 10 nm GaAs spacer and a 20 nm GaAsP layer. The nominal P concentration in the GaAsP layer was 20%, which yields approximately the same strain as the GaNAs barriers. The structural quality of the QW is excellent as indicated by the Pendellosung fringes in the x-ray diffraction (XRD) scans. The PL intensity of the sample was lower than the structure with GaNAs barriers, which can be attributed, at least in part, to the reduced injection efficiency of the structure with GaAs-GaAsP barriers. The peak PL wavelength was blueshifted by $\sim 50 \text{ nm}$ compared to the structure with GaNAs barriers. It is thus necessary to increase the In and/or N concentration in the QW to achieve emission at 1550 nm.

10:00 AM Break

Session GG:

III-Nitrides: Non-Polar and Semi-Polar Devices

Friday AM

June 24, 2011

Room: Corwin East

Location: Univ. of California-Santa Barbara

Session Chairs: Russell Dupuis, Georgia Institute of Technology; Jae-Hyun Ryou, Georgia Institute of Technology

10:20 AM Student

GG1, Highly Polarized Spontaneous Emission from Semipolar (20-2-1) InGaN/GaN Light-Emitting Diodes: Yuji Zhao¹; Shinichi Tanaka²; Roy Chung²; Chih-Chien Pan²; Kenji Fujito³; Daniel Feezell²; James Speck²; Steven Denbaars¹; Shuji Nakamura¹; ¹Electrical and Computer Engineering Department, University of California, Santa Barbara; ²Materials Department, University of California, Santa Barbara; ³Optoelectronics Laboratory, Mitsubishi Chemical Corporation

Semipolar and nonpolar orientations of group III-Nitrides have attracted considerable attention for realizing high-efficiency light-emitting diodes (LEDs) and laser diodes (LDs). Several advantages over commercially available *c*-plane structures have been highlighted, including reduced polarization-induced electric fields in the quantum wells (QWs), increased indium uptake, and polarized light emission. The former characteristics are promising for achieving high-performance green emitters, while the latter characteristic contributes to anisotropic optical gain in LDs fabricated on these planes. For example, on nonpolar (*m*-plane) the emission components polarized along the *a*- and *c*- axes involve the highest and second highest valence bands, respectively. Due to the higher emission intensity along the *a*-axis, stripes oriented along the *c*-axis are preferred for *m*-plane LDs. The relative magnitude of the intensity parallel to and perpendicular to the *c*-axis is described by the polarization ratio and high values are preferred for improved LD performance. While high polarization ratios have been reported for *m*-plane devices, long wavelength emission is difficult to achieve on this plane due to the generation of defects at high indium compositions. On the other hand, the semipolar (20-21) orientation has shown promising performance at long wavelengths but the reported polarization ratios are relatively low. In this work, we report increased

polarization ratios using the semipolar (20-2-1) plane, which is inclined at 15° and 30° toward the [000-1] direction from *m*-plane and (20-21), respectively. Using integrated electroluminescence measurements the polarization ratio was 0.7 at 480 nm for 490×292 μm² (20-2-1) devices at 20 mA. Comparable devices of a similar wavelength on (20-21) showed a polarization ratio of 0.3. A high-performance blue LED was also fabricated on the (20-2-1) plane utilizing backside roughening and a transparent packaging technique. At a drive current of 20 mA, the LED showed an output power of 30 mW and an external quantum efficiency (EQE) of 55%, which is comparable to best reported data on the semipolar (10-1-1) plane. The Matthews-Blakeslee equilibrium critical thickness also reveals that (20-2-1) has a larger critical thickness than (10-1-1) and (11-22) planes, which is favorable for higher indium content devices. Our results indicate that devices fabricated on the (20-2-1) plane have the potential to achieve high performance, such as high optical gain, low threshold current and possible high indium uptakes. Green LEDs and LDs on (20-2-1) plane are currently under investigation.

10:40 AM Student

GG2, Characterization of Green Semipolar (20-21) GaInN/GaN Multiple Quantum Well Light-Emitting Diodes Grown on Freestanding GaN Substrate: *Liang Zhao*¹; Shi You¹; Christopher Stark¹; Wenting Hou¹; Theeradetch Detchprohm¹; Edward Preble²; Tanya Paskova²; Christian Wetzel¹; ¹Rensselaer Polytechnic Institute; ²Kyma Technologies, Inc.

The heteroepitaxial growth of GaInN/GaN quantum wells (QWs) on *c*-plane sapphire has long been a commercially favored approach for high power green light emitting diodes (LEDs). However, the strong electric fields in the QWs lead to the quantum-confined Stark effect and cause the rapid drop of quantum efficiency at high working power. In order to reduce or avoid the role of piezoelectric polarization in this performance droop, we investigate the properties of semipolar (20-21) green LEDs. We report on the growth and characterization of such LEDs as prepared on freestanding GaN substrate. The samples are grown by metal-organic vapor phase epitaxy on semipolar (20-21) bulk GaN substrate. The structure consists of eight pairs of 3 nm-thick quantum wells and 12 nm-thick barriers grown on top of Si doped *n*-GaN layer, and capped by a 20 nm of electron blocking layer and a 200 nm of *p*-GaN layer. The electroluminescence (EL) spectra were measured in scratch diode geometry using indium dots of 1 mm in diameter as *p*-type and *n*-type contacts and driving the device with current varying from 0.513 mA to 247 mA. The EL peak wavelengths are at about 508 nm and the variation is within 2 nm. This EL data shows significantly reduced wavelength shift compared with commercially available *c*-plane LEDs, which could make the semipolar (20-21) LEDs very promising for color stable displays. Further characterizations such as surface morphology, external quantum efficiency, emission polarization are currently under investigation and will be presented at the conference. This work was supported by a DOE/NETL Solid-State Lighting Contract of Directed Research under DE-EE0000627. This work was also supported by the National Science Foundation (NSF) Smart Lighting Engineering Research Center (# EEC-0812056).

11:00 AM Student

GG3, Optical Emission Patterns in Semipolar (11-22) GaN Light Emitting Diodes on Planar *m*-Plane and Etched *r*-Plane Sapphire: *Benjamin Leung*¹; Yu Zhang¹; Christopher Yerino¹; Jung Han¹; Bo Kong²; Hyung Cho²; Qian Sun³; Zhen Chen³; Steve Lester³; Kuan Liao⁴; Yun Li⁴; ¹Yale University; ²Sungkyunkwan University; ³Bridgelux, Inc.; ⁴Genesis Photonics Inc.

Semipolar orientations of GaN have recently been proven to be attractive alternatives to standard *c*-plane growth, especially with respect to long wavelength light emitters and laser diodes. However, given the very limited supply of even small-area bulk GaN substrates, heteroepitaxial growth on foreign substrates will still be the practical approach for LEDs in the foreseeable future. The semipolar (11-22) orientation has promising material characteristics for long wavelength emission, and heteroepitaxial material has been demonstrated using *m*-plane sapphire. GaN templates grown this contain a large number of defects, in particular a large density of stacking faults of the order 10⁵ cm⁻¹ and associated partial dislocations. Several

semipolar (11-22) LEDs on sapphire substrates have been reported previously, with performance limitations attributed to material quality. However, with the possibility of a low defect and stacking fault density template grown on stripe etched *r*-plane sapphire (as we have reported elsewhere), heteroepitaxial (11-22) LED device performance can be analyzed critically. In this paper, we present optical device analysis on LEDs grown on *m*-sapphire, and by an alternative method on stripe etched *r*-sapphire. The GaN template is grown in two methods – 1) a two-step islanding-coalescence growth on *m*-plane sapphire using a LT-GaN or HT-AlN buffer. By TEM, we see a stacking fault density of low 10⁵ cm⁻¹. 2) by use of an etched *r*-plane sapphire substrate, selective growth on exposed *c*-plane sapphire sidewalls result in a flat semipolar (11-22) surface. TEM shows a much reduced stacking fault density, achieved by decreased heterogeneous *N*-polar growth area and coalescence blocking of stacking faults. Optical characterization of the standard semipolar (11-22) GaN LED structure (designed for blue ~450nm emission) on *m*-plane sapphire shows a dual wavelength emission, similar to previous reports. Signatures of this behavior include a broad long wavelength emission dominating at sub-mA injection, with a narrower band-edge emission increasing in intensity with injection current. This has previously been attributed to uniformity of the InGaN wells and localized states, and limits the spectral purity and output power of the devices. However, comparison with semipolar (11-22) grown on etched *r*-plane sapphire shows a much reduced long wavelength emission, resulting in a spectrally narrow emission. Magnified EL images shows that the long wavelength emission is spatially localized, and corresponding with surface features found on the as-grown GaN. The dual wavelength emissions in each case are analyzed by monomolecular and bimolecular rate equations, and it is hypothesized that trap assisted tunneling occurs producing the unwanted green emission. The correspondence of emission patterns, surface features, and growth methodology is clarified, which will suggest ways to achieve high efficiency long wavelength LEDs using heteroepitaxial semipolar GaN.

11:20 AM Student

GG4, Microscopic Optical Properties of Semi-/Nonpolar GaN with InGaN SQWs on Top Grown Directly on Patterned Si Substrate: *Sebastian Metzner*¹; Frank Bertram¹; Christopher Karbaum¹; Jürgen Christen¹; Shujian Liu²; Natalia Izyumskaya²; Vitaliy Avrutin²; Ümit Özgür²; Hadis Morkoç²; ¹Institute of Experimental Physics, Otto-von-Guericke-University Magdeburg; ²Department of Electrical and Computer Engineering, Virginia Commonwealth University

Quantum structures for optoelectronic applications grown in the conventional *c*-direction are dramatically affected by the large spontaneous and piezoelectric polarization of the wurtzite crystal structure. Due to these built-in electric fields the electron and hole wave functions are locally separated inside the quantum well (QW) significantly reducing the overlap integral and hence the efficient radiative recombination in the QW known as quantum-confined Stark effect. One approach to overcome these impacts is the growth in semi- and nonpolar directions using patterned Si substrates and epitaxial lateral overgrowth as the usual semi/nonpolar heteroepitaxy leads to an insufficient crystal quality due to the lack of appropriate substrates apart from expensive and small bulk material. We have investigated semi- and nonpolar GaN templates and InGaN/GaN quantum structures which were grown by metal organic chemical vapor deposition directly on pre-patterned Si substrates using highly spatially and spectrally resolved cathodoluminescence (CL) at liquid He-temperature. The general idea is to initially grow (0001)GaN at {111} side facets of the grooved surfaces of Si substrates. For Si(112) substrates the trenches consist of vertical (-1-11) Si sidewalls and inclined (111) Si facets separated by terraces of residual Si(112). Except for the (-1-11) sidewall all other Si facets have been masked using SiO₂, hence, the final GaN crystal orientation forms a planar *m*-plane surface. Additionally, a saw tooth-like semipolar (10-11) GaN surface was grown on the patterned Si(112) substrate. For Si(001) substrates the (1-1-1) Si sidewall is inclined and single GaN stripes with semipolar (1-101) facets form the surface. All sample structures were finally used as a template for an InGaN/GaN SQW. Using Si(112), the +*c*-wing of the GaN structure with a semipolar surface shows a homogeneous and slightly red-shifted (D⁰,X) emission at 3.463 eV (358 nm) with a FWHM of about 8 meV. In local spectra

from the $-c$ -wing two strong luminescence contributions from basal plane stacking faults (BSF) at 3.418 eV and 3.410 eV can be observed which can be directly attributed to the emission from short and elongated BSFs, respectively. The CL intensities of (D^0 ,X) and BSF are locally perfectly anticorrelated. The partially coalesced m -plane GaN structure with an InGaN SQW atop exhibits an intense quantum well luminescence which is centered at about 3.2 eV, having a FWHM of 98 meV. Strong and homogeneous CL from the SQW is emitted from nearly the entire m -plane surface. Just above the $-c$ -wing the InGaN luminescence is reduced due to the presence of stacking faults and defects. In absolute contrast no BSF luminescence is found at the $+c$ -wing where (D^0 ,X) GaN and the InGaN QW dominate.

11:40 AM Student

GG5, Strain Relaxation in Semipolar Nitrides for Optoelectronic Device Applications: *Ingrid Koslow*¹; Matthew Hardy¹; Po-Shan Hsu¹; Erin Young¹; Shuji Nakamura¹; James Speck¹; Steven Denbaars¹; ¹UCSB Materials

Performance of devices grown on partially strain-relaxed InGaN layers is reported. The (In)(Al)GaN material system is highly attractive for many devices, including light emitters from the UV to the visible regions, photovoltaics, power electronics, and thermoelectrics. In particular, $\text{In}_x\text{Ga}_{1-x}\text{N}$ layers with $x > 0.2$ are necessary for emitters and absorbers in the longer-wavelength visible region, while $\text{Al}_y\text{Ga}_{1-y}\text{N}$ layers with $y > 0.4$ are desired for deep ultraviolet (UV) emitters. However, strain in such layers can lead to significant defect generation, as well as high piezoelectric fields, which can be detrimental to device performance. Partial strain relaxation via misfit dislocation (MD) formation was recently reported for the first time in semipolar InGaN and AlGaN films, on both (11-22) and (20-21) orientations[1,2], where the basal c -plane acts as the primary slip system. Given the high lattice mismatch of the (Al,In)GaN material system, the availability of a slip system for dislocation glide has significant consequences for semipolar III-nitride devices. However, thus far the critical thickness for relaxation of $\text{In}_x\text{Ga}_{1-x}\text{N}$ layers has not been investigated in the literature beyond $x \sim 0.05$. In this report, strain relaxed $\text{In}_x\text{Ga}_{1-x}\text{N}$ layers with $0.05 < x < 0.25$ have been grown on (11-22) bulk GaN substrates by MOCVD, and characterized by x-ray diffraction, atomic force microscopy, cathodoluminescence, and transmission electron microscopy. We report here for the first time on devices grown on strain-relaxed layers. Long-wavelength light emitting diode (LED) structures were grown on top of partially relaxed InGaN layers, resulting in reduced strain in the active region, which shows promising performance.

observed carrier densities at elevated temperatures and the O-deficient non-stoichiometry in bulk In_2O_3 . However, the thin-film conductivities, which under comparable conditions ($T, p\text{O}_2$) exceed the bulk conductivities by several orders of magnitude, lie outside the thermodynamic bounds of a bulk-defect mechanism. Utilizing complementary experimental and theoretical approaches, we performed surface calculations and thickness-dependent Hall measurements in epitaxial In_2O_3 films to unearth the puzzling cause of conductivity in undoped In_2O_3 thin films. From the electronic structure calculations for the particularly stable (111) surface, we find that the formation energies of electron-producing intrinsic surface donors (surface O vacancies and In adatoms) are much reduced compared to their bulk counterparts, and the shallow donor levels of the surface defects can release electrons into both the surface and the bulk conduction band. Thus, intrinsic surface defects are a likely source of the recently observed electron accumulation in In_2O_3 films [2]. The film thickness-dependent transport measurements allow decomposition of the total sheet carrier density of the film into a bulk-like component in the film interior and into a surface component. We find that the conductivity of the epitaxial films is dominated by the surface contribution up to a thickness of about 150 nm, and therefore conclude that the conductivity of In_2O_3 thin-films is decisively controlled by surface defects. The generation of carriers via surface defects is therefore a viable route for the design of highly conductive transparent thin films.

8:40 AM Student

HH2, The Role of Native Point Defects in Highly n-Type Degenerate (Zn,Ga)O Films: *Daniel Doutt*¹; Snjezana Balaz¹; Louis Isabella¹; Leonard Brillson¹; ¹The Ohio State University

We have used a complement of depth-resolved cathodoluminescence spectroscopy (DRCLS), x-ray photoemission spectroscopy (XPS), and Hall effect measurements to determine the role that native point defects play in the electrical properties of highly conductive degenerate Ga-doped ZnO (GZO) films. Transparent conducting oxides (TCO) have found applications in many opto- and microelectronic applications such as transparent electrodes for flat-panel and flexible displays, photovoltaic cells, and LEDs. Of late, the demand for these applications and devices has grown, leading researchers to explore alternative materials for TCO applications. GZO has emerged as a strong TCO candidate due to its low cost and environmental safety. Until now, it has been unclear what kind of role native defects play in the resistivity, mobility, and carrier concentrations of these GZO films. GZO films were grown on Al₂O₃ using PLD at 200°C in Ar. DRCLS studies reveal a dominant peak at 3.7 eV-3.85 eV for all GZO films due to degenerate conduction band-valence band recombination. XPS confirms this degeneracy, displaying Fermi level (EF) positions well above the known conduction band minimum (CBM) of ZnO (3.4 @ RT) for all GZO films. Furthermore, reduced VB spectra reveals a Ga-induced gap state extending > 0.2 eV above EC, consistent with additional states forming above EC due to band filling. By using small probe energy increments we are able to plot the changes in Fermi level position with depth for these GZO films. We propose that the energy at which the 3.85 eV peak decreases to 50% above this peak on linear scale be used as an estimate of EF above the conduction band edge. We can extract the charge density (n) from the shift in Fermi level position due to degenerate doping and observe how the carrier densities vary with depth and with sample. DRCLS of GZO films show emission from 1.7- 2.1 eV isolated or clustered VZn as well as ~ 2.4 eV oxygen vacancy related (VO-R) emission. Our studies reveal large variations in EF and VZn emission with samples and with depth. Plotting the normalized peak intensities of native defects versus Hall concentration for all GZO samples shows that higher doping correlates weakly with higher intensities of the 2.4 eV VO-R emission but strongly with lower densities of the 1.7 – 2.1-eV VZn feature, underscoring the important role VZn defects play in highly conducting GZO films.

Session HH:

Oxide Semiconductors: Growth, Doping and Defects

Friday AM
June 24, 2011

Room: Corwin West
Location: Univ. of California-Santa Barbara

Session Chairs: Yicheng Lu, Rutgers University; Patrick Kung, University of Alabama

8:20 AM

HH1, Surface Donors Dominate the Conductivity of In_2O_3 Thin Films: *Stephan Lany*¹; Andriy Zakytayev¹; Thomas Mason²; John Wager³; John Perkins¹; Joseph Berry¹; David Ginley¹; Alex Zunger¹; ¹National Renewable Energy Laboratory; ²Northwestern University; ³Oregon State University

The underlying mechanism for conductivity in transparent conducting oxides (TCO) has so far been discussed mostly in terms of bulk-defect models, involving traditional doping with donor impurities, intrinsic defects, or unintentional impurities like hydrogen. In the technologically important thin-film form of pure (undoped) In_2O_3 one observes often mysteriously high carrier densities, which can rival that achieved in bulk specimens only through heavy doping by Sn_m donor impurities. Based on first-principles electronic structure calculations for bulk defects [1], we show that the formation of oxygen vacancies in thermal equilibrium can explain the experimentally

9:00 AM

HH3, High Resolution Photoluminescence Spectroscopy of Donors in Undoped and Indium-Doped ZnO Grown by Metalorganic Vapor Phase Epitaxy: Zhiwei Deng¹; Dichen Li¹; He Huang¹; *Simon Watkins*¹; ¹Simon Fraser University

There have been very few reports of spectroscopic identification of donors in ZnO grown by metalorganic vapor phase epitaxy (MOVPE). In this work we report the observation of extremely narrow photoluminescence (PL) transitions in ZnO epilayers grown using dimethylzinc and nitrous oxide at 800°C which allow us to unambiguously identify shallow donors in these materials. PL linewidths as low as 0.2 eV at 4.2K have been observed for films grown on C-plane sapphire substrates. Temperature dependent Hall effect analysis of undoped layers indicates a residual shallow donor concentration of $5 \times 10^{17} \text{ cm}^{-3}$ with an activation energy of 28 meV. Undoped layers exhibit very strong excitonic and very weak deep level luminescence. A dominant donor bound exciton (D⁰X) peak at 3361 meV is observed in all undoped samples together with the corresponding ionized donor bound exciton (D⁺X) peak at 3373 meV. Exciton linewidths as narrow as 0.2 meV are observed in undoped samples. Because of the possibility of residual strain due to growth on sapphire substrates, it is difficult to make unambiguous chemical assignments based on single D⁰X transition energies. The addition of In dopant using trimethylindium (TMIn) results in the appearance of the I9 transition at 3358 meV, which has been previously attributed to In D⁰X transitions, based on In-diffusion experiments. [1] An additional transition at 3369 meV is observed due to In D⁺X transitions. Based on a comparison with accepted values of the I9 transition energy in homoepitaxial ZnO samples, we deduce a strain induced blue shift of +1.5 meV. This is consistent with residual compressive strain induced in the ZnO films upon cooling, due to the much larger in plane thermal expansion coefficient of sapphire. By intentionally doping the epilayers with In we are able to identify the D⁰X transition at 3361 meV as being due to Ga donors. The In and Ga identifications are also confirmed by the observation of two electron satellites. Surprisingly no evidence of Al donors is observed despite the use of sapphire substrates. The addition of increasing amounts of TMIn results in an increasing ratio of In to Ga D⁰X PL, however the crystal quality degrades substantially with increasing TMIn flow based on X-ray rocking curve measurements. Temperature dependent PL measurements above 4K show additional lines due to well resolved D⁰X (B) transitions separated by 4.5 meV for both Ga and In donors due to the A/B crystal field splitting of the valence band. PL measurement at lower energies show only zone center phonon replicas of the D⁰X emission, with no evidence of donor-acceptor pair luminescence. This indicates that the films have very low residual acceptor compensation.

9:20 AM Student

HH4, Trap-Limited Li Diffusion in Melt Grown ZnO: *Knut Erik Knutsen*¹; Pekka Tapio Neuvonen¹; Klaus Magnus Johansen¹; Bengt Gunnar Svensson¹; Andrej Kuznetsov¹; ¹University of Oslo

ZnO is a wide bandgap semiconductor (~3.4eV) with high excitonic binding energy (~60meV). ZnO has great potential as a material for effective blue/UV light emitting diodes and for room temperature excitonic lasing. However, the lack of stable, high quality p-type material prevents the use of ZnO for these applications. Group I and V elements are commonly suggested as acceptor dopants, e.g. Li on Zn site (Li_{Zn}). Since Li is also a residual impurity in hydrothermal ZnO, its properties is a hot topic in the ZnO community. We use secondary ion mass spectrometry to study the diffusion behavior of Li in ZnO. In the present experiments, Li is introduced into melt grown ZnO wafers submerged in a mixture of ZnO and Li₂O powders and heated at 450 - 600°C in a sealed quartz ampoule for 10 minutes. After heat treatment at 450°C the Li concentration versus depth profile obeys the solution of the infinite source model (erfc) up to a depth of ~1.3µm where the Li concentration has fallen from the surface value of $\sim 5 \times 10^{18} \text{ Li/cm}^3$ to a value of $\sim 2 \times 10^{17} \text{ Li/cm}^3$. However, this is followed by a sharp drop in the experimentally obtained Li concentration, which cannot be described by this simple model. Similar profiles, having longer erfc-function parts, yet still exhibiting the same sharp drop at $\sim 2 \times 10^{17} \text{ Li/cm}^3$, are observed after treatments up to 600°C. Moreover, four point probe measurements indicate that high/low cooling rates result in

low/high resistive samples, respectively. Li is widely believed to diffuse via Li interstitials (Li_i), acting as donors in ZnO. The low resistivity observed in the rapidly cooled samples support this view. The sharp drop in Li concentration at the end of the depth profiles is consistent with a trap limited diffusion mechanism for Li_i. Simulation performed on the basis of this model, using a trap capture cross section radius of 2.5nm, yield good agreement with all the experimental profiles in the studied temperature range of 450-600°C. From the obtained data, we extract an activation energy of $1.35 \pm 0.1 \text{ eV}$, and a pre-factor of $1 \times 10^{-2} \text{ cm}^2/\text{s}$ for the diffusion coefficient of Li_i. Further, the trap occurs with a uniform concentration of $\sim 2 \times 10^{17} \text{ cm}^{-3}$ in melt grown ZnO, whereas the trap concentration is found to be higher in hydrothermal ZnO, indicating that the trapping may be impurity related since impurity concentrations are indeed higher in hydrothermal material.

9:40 AM Student

HH5, Identification of Acceptor States in Li Doped ZnO Using Nanoscale Depth-Resolved Cathodoluminescence Spectroscopy: *Zhichun Zhang*¹; K-E. Knutsen²; Andrej Kuznetsov²; Bengt Svensson²; Leonard Brillson¹; ¹Ohio State University; ²University of Oslo

We used nanoscale depth-resolved cathodoluminescence spectroscopy (DRCLS) coupled with surface science techniques to explore the relationship between the electrical properties and energies of native defects in Li doped hydrothermal (HT) ZnO. As a leading candidate for next generation opto- and microelectronics, ZnO has attracted tremendous interest. However, despite extensive research in the past decades, some fundamental issues remain unsolved, such as the control of amphoteric electrical behavior of Li in HT-ZnO. Li is unintentionally incorporated during HT-ZnO synthesis. And HT-ZnO wafers are usually highly resistive as a result of the Fermi-level dependent and low energy barrier to switch between interstitial Li (Li_i) and substitutional Li on Zn-site (Li_{Zn}). [1] Our previous work showed mastering of Li concentration by high temperature treatment. [1] And the 1.9-2.1eV and 2.3-2.5eV luminescence emissions have been correlated with Zinc vacancy (V_{Zn}) and Oxygen vacancy (V_O) related defects, respectively. [2] In this work, two HT-ZnO samples were firstly annealed in 10% Li₂O and ZnO at 600°C for one hour. Then Li-1Q was quenched in DI water, while Li-2S was slow cooled in air. The third melting grown Li-d6 was annealed the same way and also slow cooled in air. From the DRCL spectra of these samples, the Li_{Zn} acceptor is identified with an energy level located 3.0eV below Ec. DRCLS provided the energy level of Li_{Zn} acceptor in ZnO bandgap, different Li configurations under different annealing process, enabling identification of defects in ZnO and methods to control them. Monte Carlo simulation of ZnO illustrates electron-hole pair generation versus incident electron beam energy E_b and excitation depth. DRCLS spectra of these samples showed the V_{Zn}-related 2.1eV, V_O-related 2.5eV, and new 3.0eV peak, which is assigned to Li_{Zn} acceptor state. The Li acts as interstitial donor in quenched Li-1Q, which makes it having low resistivity in 4-point probe measurement and low surface potential in Kelvin Probe Force Microscopy results. However, after slow cooling in air, the Li_i donor passivates V_{Zn} and becomes substitutional Li_{Zn}, which decreases 2.1eV (V_{Zn}) peak intensity and increases 3.0eV (Li_{Zn}), in another way, increasing the relative intensity of $I_{3.0 \text{ eV}}/I_{2.1 \text{ eV}}$. It's clear that after slow cooling, the relative intensity of $I_{2.1 \text{ eV}}/I_{\text{NBE}}$ in Li-2S decreases about one order of magnitude and $I_{3.0 \text{ eV}}/I_{2.1 \text{ eV}}$ increases about one order of magnitude. Low Li_i and high Li_{Zn} lead to low electron concentration, which is validated by high resistivity and high surface potential in slow cooled samples. In summary, quenching leads to low concentration of Li_{Zn}, as well as low resistivity and surface potential. These studies identify the Li_{Zn} acceptor energy level in ZnO band gap, reveal different Li configurations in ZnO under different annealing process, and provide guidance to produce low resistivity in-situ auto-doped ZnO bulk.

10:00 AM Break

10:20 AM

HH6, Zn(Mg,Cd)O Epitaxy for Optoelectronic Applications: *Jizhi Zhang*¹; Jin Joo Song²; ¹ZN Technology, Inc.; ²ZN Technology & UCSD

ZnO-based, wurtzitic Zn(Mg,Cd)O material system has recently drawn significant attentions for optoelectronic applications. As ZnO has an

exceptionally high exciton binding energy, 60meV, one expects many Zn(Mg,Cd)O alloys could also have high exciton binding energies and be used for ultra-high efficiency light emission and detection. By varying the Mg and Cd compositions, energy band gap tuning is achievable with the alloys, covering uses in a wide spectral range from UV to visible. High efficiency light emitters and detectors may be made with advanced heterostructures using the Zn(Mg,Cd)O alloys for applications in the same spectral range. Zn(Mg,Cd)O films were grown using both MOCVD and MBE methods, with more emphasis given on the MOCVD method for high throughput purpose. Both hetero- and homo-epitaxial techniques were employed for the film growth. Improvements in these techniques have resulted in the growth of high crystalline ZnO films with FWHMs of X-ray rocking curves as low as 57"; ternary films of various Mg/Cd compositions, showing light emission from green to UVA; and high quality Zn(Mg,Cd)O quantum well structures. Significant efforts were put on p-doping on our way towards the fabrication of Zn(Mg,Cd)O pn junction devices. P-Type doping has been successful in the ZnO films. Utilizing the p-type ZnO films, p-i-n type, ZnO homojunction LEDs have been fabricated with rectifying IV characteristics, turn-on voltages at ~3V, and RT electroluminescence single-peaked in the near UV. Our most recent p-doping effort was on development of p-type ZnMgO films that have high Mg compositions. These p-type ZnMgO films are the key components to be used in Zn(Mg,Cd)O heterostructures for the high efficiency light emitters and detectors. ZnMgO films with Mg composition of about 0.22 were grown and intentionally doped for p-type conduction using MOCVD. Most of these doped ZnMgO films were not conductive electrically at room temperature. However, some interesting results were shown from a low temperature (LT) photoluminescence (PL) study, carried out using the 325nm line of a CW He-Cd laser as the excitation source. Measurements at 10K from the films consistently yielded spectra with a dominant emission peak at ~347nm. This intense peak, having several orders of phonon replicas, most likely resulted from donor to acceptor pair (DAP) emission, suggesting existence of acceptor levels introduced by our doping effort. In addition, a less intense emission peak was observed at ~341nm in the spectra, probably caused by emission from neutral acceptor bound excitons (AX0). More results of the doping and other Zn(Mg,Cd)O related efforts will be given in the presentation.

10:40 AM Student

HH7, ZnO and Al₂O₃ Thin Films Deposited by Plasma Enhanced Atomic Layer Deposition and Plasma Enhanced Chemical Vapor Deposition: *Yuanyuan Li¹; J. Ramirez¹; Thomas Jackson¹; ¹Penn State University*

Oxide thin film electronics has gained interest in recent years due to low-temperature film deposition, ease of scale-up to large-area applications, and suitability for transparent electronics. We have demonstrated high quality thin film transistors and fast circuits using aluminum oxide and zinc oxide films deposited by plasma-enhanced atomic layer deposition (PEALD).[1] For applications that require thicker films the low deposition rate of PEALD or conventional ALD can be problematic. In this work, we studied ZnO and Al₂O₃ deposited by ALD, PEALD, fast mode PEALD, and plasma enhanced chemical vapor deposition (PECVD). A rectangular reactor (about 28 cm x 30 cm) was used for the film depositions described here. The gas input is through a slit at one end of the reactor and the system is pumped through a slot at the other end, resulting in a pseudo-laminar gas flow. Films were deposited at 200C using trimethylaluminum (TMA) for Al₂O₃, and diethyl zinc (DEZ) for ZnO, as metal organic precursors. For Al₂O₃ ALD, CO₂ is used as a purge gas and H₂O as a reactant. For Al₂O₃ PEALD and PECVD, CO₂ is used as both a purge gas and, with plasma activation, as a reactant. For ZnO PEALD and PECVD, N₂O is used as both a purge gas and, with plasma activation, as a reactant. Films were deposited on SiO₂ and characterized by spectroscopic ellipsometry. Al₂O₃ deposited by ALD or PEALD at ~4 nm/min have similar refractive index (~1.67 at 630 nm). The reactor pseudo-laminar gas flow combined with the simplified process of PEALD (only one reactant needs to be purged) allows a fast deposition mode. Al₂O₃ deposited by PEALD at ~1.25 nm/min has index very similar to films deposited at lower rate by ALD or PEALD. Increasing the deposition rate to ~2.5 nmAl₂O₃ results in a slightly lower refractive index (~1.63 at 630 nm). Al₂O₃ film deposited by PECVD allows very fast uniform film

deposition, ~40 nm/min, but with significantly lower refractive index (~1.57 at 630 nm), likely due to reduced film density or increased carbon incorporation. ZnO thin films deposited by ALD typically have substantially lower refractive index than films deposited by normal PEALD (1.9 compared to 2.02, at 630 nm). ZnO thin films deposited by fast mode PEALD have refractive index similar to films deposited by ALD (~1.83 at 630 nm), again significantly lower than that of films deposited by normal mode PEALD.

11:00 AM Student

HH8, Thin Films of ZnO Prepared by Reactive Pulsed Arc Molecular Beam Deposition: *David Eno¹; Juhyung Yun²; Tingfang Yen²; Robert DeLeon¹; James Garvey¹; Wayne Anderson²; ¹Dept of Chemistry, University at Buffalo; ²Dept of Electrical Engineering, University at Buffalo*

ZnO is a promising material for optoelectronic applications such as solar cells, ultraviolet light detectors, and light emitting diodes because of its highly transparent and electrically conductive characteristics. Moreover, ZnO is inexpensive, relatively abundant, and a non-toxic material, unlike Indium Tin Oxide (ITO) which is widely used in the electronic industry. Nevertheless, high quality ZnO thin films are not yet easy to grow especially at low temperature. Low temperature process is necessarily required for low cost processing and flexible electronics. Herein, highly crystalline ZnO thin films were deposited by reactive Pulsed Arc Molecular Beam deposition (PAMBD) at room temperature. High temperature plasma was generated by arc discharge under oxygen, nitrogen, and ammonia backing gases. With a base vacuum between 10⁻⁶ to 10⁻⁷ Torr, a molecular beam arc was triggered and maintained in the region of 10⁻¹ to 10⁻² Torr with 1 Hz duty cycle. Overall deposition rate ranged between 10 and 250 nm/hr based on source-substrate distance, backing gas, backing gas pressure, deposition time, and cathode condition. XRD analysis shows a single diffraction peak of (101) orientation corresponding to 36.334° of 2θ with 0.082 of FWHM. Interestingly, by tuning oxygen backing gas, structural properties were changed toward (002) orientation corresponding to 34.318° of 2θ with 0.375 of FWHM. Nano-crystalline ZnO thin films have been deposited on Si substrates by PAMBD method to make ZnO/p-Si heterostructures. Using as deposited heterostructure, Metal-Semiconductor-Metal (MSM) photodiodes were fabricated and characterized under dark & light condition. As a low work function metal (2.6 eV), ytterbium was utilized to form the Schottky contact with n-type ZnO film and it efficiently suppresses dark current due to a large Schottky barrier height. At a bias of -0.25 V, highly sensitive photocurrent was has been measured showing photo to dark current ratio of 2526 and responsivity of 24.5 A/W. Such a high photo-response is attributed to not only a low defect crystal structure of the as-grown ZnO film and but also efficiently suppressed interface defects at the hetero-interface.

11:20 AM

HH9, Atom Probe Tomography of ZnO Nanowires: *Nabil Dawahre¹; Joseph Brewer¹; Gang Shen¹; Nicholas Harris¹; Soner Balci¹; William Baughman¹; Lee Butler¹; Shawn Wilbert¹; Richard Martens¹; Seongsin Kim¹; Patrick Kung¹; ¹University of Alabama*

Zinc oxide (ZnO) has become an important wide bandgap semiconductor material because of its wide range of optical and electrical properties, including a large bandgap ~3.3 eV and exciton binding energy ~60 meV, its piezoelectricity, room temperature ferromagnetism and magneto-optic effects. ZnO nanostructures ranging from nanowires to nanobelts and nanoribbons have dramatically expanded the range of applications of this material, including light emitting diodes, lasers, solar cells, transparent electronics, chemical sensors, and mechanical energy harvesting devices. Atom probe tomography (APT) is an analytical technique that has the unique ability to identify and map the positions of individual atoms from a nanostructure with three-dimensional atomic resolution. This capability is becoming essential when trying to understand defect distribution (e.g. composition fluctuations or doping) in semiconductor materials, as they can significantly affect device characteristics. In this study, we present the first APT compositional analysis of individual ZnO nanowires and the challenges encountered in developing this new technique for ZnO. We have grown ZnO nanowires by thermal chemical vapor deposition on sapphire substrates. To promote the orientation and

alignment of the nanowires, ZnO seeds were prepared by oxidizing zinc acetate in suspension in an alcohol solution. The synthesis was carried out at 900 °C. A mixture of ZnO and graphite in powder form was used as precursor, with the carbon acting as a reducing agent for the oxide. Various molar ratios of the ZnO to carbon were investigated. The resulting nanowires were characterized using scanning electron microscopy (SEM), transmission electron microscopy (TEM), x-ray diffraction, photoluminescence (PL), Raman spectroscopy, atom probe tomography, and Terahertz time domain spectroscopy (THz-TDS). THz-TDS is an emerging technique that is capable of probing the electrical conductivity of nanostructures in a non-destructive manner because it does not require making an electrical contact. SEM and x-ray diffraction showed the nanowire were 500 to 3000 nm long, with a diameter range from 50 to 150 nm, and were crystallographically orientated with their c-axis perpendicular to the substrate. Their density was on the order of 108 cm⁻². TEM was used to analyze the atomistic structure of the nanowires. Raman spectroscopy revealed the expected phonon modes of wurtzite ZnO while photoluminescence exhibited near band edge emission near 380 nm and allowed the probing of the visible defect-related emission near 500 nm as a function of the growth parameters. These nanowires were subsequently prepared for APT. Measurements under various voltage and laser pulse conditions were investigated and the resulting data will be presented.

11:40 AM

HH10, Strain: A New Strategy of Tuning Doping Site and Type in Semiconductors: *Junyi Zhu*¹; Su-huai Wei¹; ¹National Renewable Energy Lab

Controlled doping is one of the most important and challenging problems in semiconductor physics. For a specific application it is often desirable to introduce a specific dopant at a particular site to generate required carriers. For example, ZnO is easy to be doped n-type but is difficult to be doped p-type. In principle, p-type doping in ZnO can be achieved by using group-I elements such as Li substituting at Zn site. However, for small dopant such as Li, they often favor interstitial positions, which makes it a donor and passivate p-type dopants such as Li Zn. This is especially true when the Fermi energy is close to the valence band maximum (VBM) in p-type material. Using first-principles method, we show that the preference of substitutional and interstitial doping can be tuned through external strain, either hydrostatic or epitaxial, because doping induces a local volume change around the dopants. When the external strain is applied in the same direction as the dopant induced volume change, the solubility of that type of dopant is enhanced. As an example, we show that Li substitution on Zn sites in ZnO can be enhanced against the Li interstitial doping by applying a compressive strain. We suggest that this simple and general strategy should be very useful to control doping and electronic properties of many semiconductor materials.

under debate. The intrinsic energetic position of the Fermi level is unclear, i.e., whether the Fermi level is located within the fundamental band gap or shifted slightly into the conduction band. The latter case induces electron accumulation at the surfaces of the crystal. Such an electron accumulation is typically observed at InN surfaces upon air contact, raising the question whether it is an intrinsic material property or not? In order to probe intrinsic bulk properties by STM and not only contamination or surface effects, a clean and stoichiometric surface is necessary. This can be achieved by cleaving InN along non-polar planes. To analyze the origin of the different electronic states in detail, we investigated the clean non-polar (11-20) cleavage surface using cross-sectional scanning tunneling microscopy (XSTM) and spectroscopy (XSTS). Using combined XSTM and XSTS we were able to locate an InN layer grown on an AlN buffer layer on top of a Si(111) substrate. XSTS spectroscopy on the InN(11-20) cleavage surface yield normalized conductivity spectra, where three contributions to the tunneling current can be observed: (i) the contribution from the conduction band density of states for biases above the conduction band minimum at +0.3 V, (ii) a defect induced current, dominating the spectra between biases of 0 and -0.4 V, and (iii) a valence band related tunneling current rising at a bias of about -0.4 V and dominating the spectrum for biases below. The defect induced current arises from semi-filled defect states being present at the surface steps, and probably also from other (point) defects at the surface. Within the bulk band gap of EG = 0.7 eV no intrinsic surface states could be observed. Furthermore, the Fermi level pinning at about 0.3 eV below the conduction band minimum indicates the absence of an electron accumulation layer. The results illustrate that electron accumulation at InN surfaces is not a universal property on InN. For clean stoichiometric cleavage surfaces no electron accumulation is observed. Thus, electron accumulation results primarily from the details of the surface structure and is hence not an intrinsic property of the bulk InN material.

8:40 AM Student

I12, MBE Growth Study of AlInN and AlInN/GaN Heterostructures for Intersubband Device Applications: *Liang Tang*¹; Geoff Gardner¹; Bob Colby¹; Rich Molnar²; Colin Edmunds¹; Michael Manfra¹; Oana Malis¹; ¹Purdue University; ²MIT Lincoln Laboratory

Nitride semiconductors are promising candidates for high-speed intersubband optoelectronic devices due to the existence of large conduction band offsets (exceeding 1 eV) and sub-picosecond upper-level lifetimes. However heterostructures with high mole fraction AlGaIn are difficult to grow due to the large lattice mismatch between AlN and GaN. Al_{0.82}In_{0.18}N lattice-matched to GaN presents an alternative barrier material that provides high conduction band offset and significant reduction in strain in thick device structures. Nevertheless, the growth of high quality AlInN is hampered by several factors including the vastly different optimal growth temperatures for AlN and InN and the tendency for phase segregation during growth. We present a systematic study of the growth of AlInN films and AlInN/GaN superlattices by MBE on [0001] GaN templates. Using RF-plasma conditions known to produce a nitrogen-limited growth rate of 6.5nm/min for GaN, we studied the impact of varying growth rate, III/N ratio, and doping on the structural and optical properties of thick AlInN layers and AlInN/GaN superlattices. Initial studies focused on lattice-matched samples grown in the nitrogen-rich regime at a substrate temperature of 530°C. It was found the growth rate increases linearly with increasing total metal (Al+In) flux up to a growth rate of 3.8nm/min. Here high quality films can be realized. However, when the metal flux was increased further, film quality deteriorated as measured by x-ray diffraction, suggesting the onset of large scale segregation. The origin of this abrupt change is currently under investigation. Our films are characterized by atomic force microscopy (AFM), high resolution x-ray diffraction (HRXRD), high resolution transmission electron microscopy (HRTEM) and optical absorption measurements of doped superlattices. Thick AlInN films (~200nm) display high quality ω -2 θ x-ray data. Si-doped AlInN/GaN superlattices display relatively smooth surface morphology with an RMS roughness of 0.9nm over a 4micron x 4micron area and strong satellite peaks in x-ray diffraction. Interestingly, even in films that do not display evidence of large scale segregation in x-ray data, high angle annular dark field STEM imaging

**Session II:
Intersubband Devices: AlInN and InGaIn
Materials Characterization**

Friday AM Room: Flying A
June 24, 2011 Location: Univ. of California-Santa Barbara

Session Chairs: Oana Malis, Purdue University; Michael Manfra, Purdue University

8:20 AM

III, Absence of Electron Accumulation at InN(11-20) Cleavage Surfaces: *Philipp Ebert*¹; Sarah Schaaflhausen¹; Andrea Lenz²; Aizhan Sabitova¹; Lena Ivanova²; Mario Dähne²; Y.-L. Hong³; Shangjr Gwo³; Holger Eisele²; ¹Forschungszentrum Jülich GmbH; ²Technische Universität Berlin; ³National Tsing Hua University

InN in principle opens up the possibility of using only one ternary III-V semiconductor alloy (InGaIn) in optoelectronic devices to cover the whole visible spectral range. Despite this, key material properties of InN are still

indicates phase contrast consistent with small length scale segregation. The length scale of the fluctuations is a few nanometers. This observation is further corroborated by plan view images which are also sensitive to fluctuations in Z . This data indicate that our MBE-grown AlInN layers are not completely homogeneous. Finally we present data of the Silicon doping dependence of intersubband absorption in AlInN/GaN superlattices. While it is generally known that high Si-doping ($\sim 10^{19}$ - 10^{20} cm $^{-3}$) is required to measure significant intersubband absorption in Nitride structures, a systematic study of impact of Si doping levels on absorption in AlInN/GaN heterostructures is still lacking. We vary the Si doping levels over several orders of magnitude (10^{18} cm $^{-3}$ to high 10^{20} cm $^{-3}$) and correlate doping with strength and linewidth of intersubband absorption.

9:00 AM

II3, Room Temperature near-Infrared AlInN/GaN and AlGaIn/GaN Quantum Well Photodetectors Grown by Molecular Beam Epitaxy: *Colin Edmunds*¹; *Donghui Li*¹; *Liang Tang*¹; *Richard Molnar*²; *Michael Manfra*¹; *Oana Malis*¹; ¹Purdue University; ²MIT Lincoln Laboratories

Nitride semiconductors are promising candidates for high-speed intersubband optoelectronic devices operating in the 1.5-3 micron range due to the large conduction band offset (exceeding 1 eV) between GaN and high-Al composition alloys, and sub-picosecond upper-level lifetimes. We have demonstrated AlInN/GaN and AlGaIn/GaN quantum well infrared photodetectors (QWIPs) operating in this technologically important near-infrared range. The detector structures were grown by plasma-assisted molecular beam epitaxy on approx. 100 μ m thick GaN templates grown by hydride vapor-phase epitaxy (dislocation density less than 1×10^8 cm $^{-2}$). A typical detector consists of a 15 period superlattice of 21 \AA GaN quantum wells separated by 21 \AA thick barriers ($\text{Al}_{0.75}\text{Ga}_{0.25}\text{N}$ or $\text{Al}_{0.2}\text{In}_{0.8}\text{N}$). The contact layers consisted of highly doped GaN layers. The structure of the superlattices was characterized with high resolution x-ray diffraction. In order to determine the superlattice's optical properties the samples were first polished into standard multipass waveguides and characterized using Fourier-transform infrared absorption spectroscopy. In some cases a metal film was deposited on the sample surface to enhance the electromagnetic field near the quantum wells. The measurements were carried out in both the s- and p-polarizations in order to isolate the absorption due to intersubband transitions. The AlGaIn/GaN detector exhibited intersubband absorption at 2.1 microns (591 meV) with a FWHM of 57 meV. The QWIP devices were processed using reactive Cl_2 plasma to define 1 mm by 1/2 mm mesas. Light was coupled into the QWIP through a 45 degree polished facet. The photocurrent spectral measurements were performed at room temperature using a Nicolet Fourier-transform infrared spectrometer, a current amplifier, and a lock-in amplifier. An optical chopper was used to modulate the amplitude of the incoming radiation. Polarization sensitive measurements were employed to confirm the intersubband nature of the photocurrent. The intersubband photocurrent peak was located at 2.02 microns (614 meV) and had a FWHM of 92 meV. A peak responsivity of 195 $\mu\text{A/W}$ was measured at zero bias using a calibrated blackbody source. This value is consistent with previous results reported in the literature for AlGaIn/GaN QWIPs.

9:20 AM Student

II4, Characterization of Lateral and Vertical Inhomogeneities in InAlN Grown by Plasma-Assisted Molecular Beam Epitaxy: *Wei Kong*¹; *Wenyuan Jiao*¹; *Tongho Kim*¹; *Maria Losurdo*²; *Giovanni Bruno*²; *April Brown*¹; ¹Duke University; ²Institute of Inorganic Methodologies and of Plasmas

Lattice-matched In $_{0.17}$ Al $_{0.83}$ N/GaN is of substantial interest for III-N device applications. For electronic devices, the high spontaneous polarization of InAlN enables high electron concentrations. However, the growth of device-quality InAlN by molecular beam epitaxy (MBE) is still challenging because of the inability to achieve high growth temperature due to In desorption and consequent low mobility of Al on the evolving surface at the limited growth temperatures. Recent TEM studies have identified the presence of a nanoscale columnar structure in InAlN grown by MBE resulting from a platelet coalescence layer-by-layer growth mode. MOCVD-grown InAlN films, in comparison, are laterally uniform. Therefore, the characterization of both the

vertical and lateral compositional uniformity in PAMBE grown InAlN films is critical in order to ultimately understand and control the relationships between growth conditions and optical and electrical properties. In this report, we present our investigation on the lateral and vertical inhomogeneities observed in InAlN grown by PAMBE near the lattice-matched composition to GaN. A series of InAlN films were grown on GaN templates at the temperature from 400 $^\circ$ to 540 $^\circ$ under N-rich and stoichiometric conditions. These films show a smooth micron-scale morphology (RMS of 0.3nm as determined by atomic force microscopy (AFM)). Reciprocal space map (RSM) characterization indicates that all samples are pseudomorphic with In content from 14%~17%. However, x-ray diffraction rocking curve fitting indicates that several samples possess two compositional regions with an In-poor layer nearest to the surface. The thickness of the In-poor layers varies from 2nm~5nm with In content of 5%~10%. The vertical inhomogeneity is to be compared to that observed for InGaIn heterostructures which are widely reported to be capped by an In-rich layer. In addition, we investigated the characterization of the lateral inhomogeneity of InAlN layers by observing the variation of RSM intensities for a given sample. The ratio for the layer peak to the substrate peak decreases from that for the (002) plane to the (105) plane, which indicates an anisotropic deterioration of crystalline quality. Compared to the same characterization applied to InGaIn samples, the effect is much less significant. Such inhomogeneities in InAlN can be introduced by the presence of V-defects penetrating from the substrate to the InAlN surface as identified by AFM and scanning electron microscopy (SEM). In addition, the nanoscale columnar structure will also introduce such asymmetry.

9:40 AM Student

II5, Electrical Tuning of InGaIn Quantum Dots in GaN Photonic Crystal Cavities: *Alexander Woolf*¹; *Kasey Russell*¹; *Fabian Rol*¹; *Evelyn Hu*¹; *H.A.R. El-Ella*²; *M.J. Kappers*²; *R.A. Oliver*²; ¹Harvard; ²Department of Materials Science and Metallurgy, University of Cambridge

Semiconductor optical cavities offer a unique platform for the study of light-matter interactions. The ability to precisely control these interactions offers promising possibilities toward quantum computing, cavity quantum electrodynamics, and the creation of exotic states of matter like quantum dot exciton-polaritons. The large band gap and high exciton binding energy of gallium nitride (GaN) make it a candidate for such studies at room temperature. Significant challenges still remain, due to the strong piezoelectric fields in GaN and the material's chemical inertness. Here we demonstrate the fabrication of photonic crystal cavity structures in a thin, suspended, electrically active GaN p-n junction membrane consisting of InGaIn quantum dots. Historically, the lack of a selective wet chemical etch in GaN has been an obstacle in the fabrication of suspended membranes. But by utilizing a novel etch technique known as photo-electrochemical (PEC) etching, our group has recently demonstrated microdisk resonators with quality factors as high as 6,000 [1]. In spite of clear evidence of modes in the cavity, we have not been able to measure a change in the lifetimes of the InGaIn quantum dots, one signature of coupling between the emitters and the cavity. This coupling critically depends on both the resonance of the quantum dot emission and the frequency of the cavity mode as well as the strategic placement of the quantum dot at the mode's maximum field intensity. Thus the spectral tuning of the quantum dot and the cavity mode have been essential components of achieving quantum dot-cavity resonance. In the past, spectral tuning has been achieved by a variety of techniques including temperature tuning of quantum dots and cavity deformation via oxide etching or monolayer deposition of inert gases. However, these approaches have limitations such as irreversibility or performance degradation. The internal electrical fields of GaN allow for a unique associated tunability of InGaIn quantum dot emissions up to 80 meV under an applied bias of a few volts [2]. Furthermore, such tuning is reversible and does not adversely affect device performance. Initial measurements using this technique show the feasibility of tuning quantum dots in a cavity structure. We intend to present those tuning results for a cavity. Thus we have carried out the first studies demonstrating electrical tuning of InGaIn quantum dots in a material structure designed uniquely to allow the fabrication of cavities. This work should be the critical missing piece to demonstrate coupling between

InGaN quantum dots and a nanoscale GaN cavity structure. These results could be pivotal in bringing fundamental science out of the lab and into the next generation of integrateable and robust solid-state devices.

10:00 AM Break

10:20 AM Student

II6, Investigation of Indium and Impurity Incorporation of InGaN Films on Polar, Nonpolar, and Semipolar GaN Orientations Grown by Ammonia

MBE: David Browne¹; Erin Young¹; James Speck¹; ¹UCSB

The band gap of In_xGa_(1-x)N spans the entire visible spectrum. Progress in understanding the growth of this material has resulted in the production of blue LEDs and laser diodes. Increasing the composition of indium is necessary in order to produce devices that emit in the green spectral region, as well as for the development of high efficiency solar cells. Ammonia molecular beam epitaxy (MBE) provides an attractive method of growth due to ultra high vacuum (UHV) growth conditions as well as high purity group III elemental source materials. Growth on orientations of GaN other than the conventional c-plane (0001) are also of interest due to the reduction (semipolar) or elimination (nonpolar) of spontaneous and piezoelectric polarization in the growth direction, as well as increased indium uptake on certain orientations. Presented in this work is a growth study of InGaN films on nonpolar m-plane GaN (10-10), semipolar GaN((11-22) and (20-21)), as well as on conventional c-plane GaN templates on sapphire. Indium incorporation, impurity incorporation, and surface morphology were studied for the growth of InGaN on all 4 orientations. Growths were performed coloaded so that direct comparisons between orientations could be made as growth conditions were systematically varied. Growths consisted of 100nm of a high temperature GaN buffer (750°C) followed by a low temperature (560-630°C) InGaN growth (50-200nm), and finally a thin (3nm) GaN cap to protect the films. Various substrate temperatures, growth rates, and thicknesses were examined to investigate the effect of each on the properties of the films. Indium composition was analyzed using high resolution x-ray diffraction measurements (HRXRD), while surface morphology was characterized with atomic force microscopy (AFM) images. Secondary ion mass spectrometry (SIMS) was performed to determine impurity concentration levels. It was observed that the (20-21) orientation had the greatest propensity for indium incorporation into the films, whereas (11-22) had the least for identical growth conditions. It was also observed that indium incorporation was strongly affected by substrate temperature during growth, as higher temperatures resulted in less indium for all orientations. For instance, the indium composition on (20-21) decreased from 13.9% to 6.4% when the growth temperature was increased from 575°C to 630°C. Finally SIMS analysis indicates higher impurity (O, C, H) incorporation for non-basal plane than for c-plane similar to MOCVD growth of GaN.

10:40 AM Student

II7, Piezoresponse Force Microscopy of InGaN/GaN Quantum Dots:

Adrian Bayraktaroglu¹; Meng Zhang¹; Pallab Bhattacharya¹; Jamie Phillips¹; ¹University of Michigan

The polar nature of III-N compound semiconductors results in piezoelectric effects that determine built-in electric fields and induced charge at heterojunction interfaces. Strong piezoelectric effects are evident in InGaN/GaN heterojunctions due to the strain associated with lattice mismatch and determine optical properties that are critical for light emitting devices. Light emitting diodes based on InGaN/GaN quantum dots have shown outstanding performance with 500-520nm photoluminescence peaks and a reduced efficiency droop¹ in comparison to quantum well structures. The improved performance is attributed to reduced piezoelectric fields in the quantum dots. However, this conclusion is based on experimental observation of emission energies without definitive knowledge of piezoelectric response. Furthermore, an enhancement in piezoelectric response is predicted for nanoscale systems², which opposes the current conclusion that the observed efficiency improvement is based on reduced piezoelectric contributions for InGaN/GaN quantum dots. In this work, piezoresponse force microscopy (PFM) is utilized to measure piezoelectric response of InGaN/GaN quantum dots at the nanoscale. PFM provides a technique of directly measuring the spatial dependence of the

piezoelectric response that is orthogonal to more conventional techniques that infer piezoelectric response from electronic and optical properties. PFM images of an exposed single layer of InGaN/GaN quantum dots grown by molecular beam epitaxy will be presented and compared to surface topology. Results of the PFM measurements will be compared to previous models on the dependence on quantum dot shape³ and relation to quantum wells⁴. Piezoelectric response is found to correlate with quantum dot morphology with enhanced response in quantum dot regions and a weak dependence on quantum dot size.

11:00 AM Student

II8, InGaN/GaN Core-Shell Nanorod Arrays Grown by Selective Area Growth for InGaN-Based Light Emitting Diodes:

Ting-Wei Yeh¹; Lawrence Stewart¹; Hyung-Joon Chu¹; Yen-Ting Lin¹; P. Dapkus¹; Byungmin Ahn²; Steven Nutt²; ¹Center for Energy Nanoscience, University of Southern California; ²Department of Chemical Engineering and Materials Science, University of Southern California

Ordered GaN nanorod arrays were successfully grown by selective area growth by metalorganic vapor phase deposition (MOCVD). The nanorods are formed by patterning the substrate with a dielectric film containing a dot array of nanoscale openings prepared by electron beam lithography and reactive ion etching. Hexagonal GaN nanorods with six non-polar planes were grown on the patterned c-plane GaN bulk material using a pulsed MOCVD growth mode. GaN nanorods with the diameters of 150nm or less were grown on dot arrays with 250-500nm center-to-center spacing. A wurtzite crystal structure in the rods was confirmed by high-resolution transmission electron microscope analysis. In some studies, GaAs or InAs nanowires grown either by vapor-liquid-solid (VLS) or selective area growth exhibit very dense stacking faults along the growth directions. Unlike the general III-V nanowires, no stacking faults were found in the GaN nanorods. Therefore, the possible influence of the stacking faults on the electrical conductivity along the nanorods can be eliminated in the GaN nanorods. As compared to the GaN nanorods prepared by etching planar GaN bulks through a mask, the MOCVD-grown GaN nanorods can avoid the surface damage from the dry etching process and the grown surfaces are expected to be high quality templates for the subsequent structures. The nanometer-scale sizes of the GaN nanorods release the strain at the growth hetero-interfaces allowing the rods to be grown without dislocations. Finally, the nanorod geometry may be beneficial for improving the light coupling from these structures. InGaN/GaN multiple quantum wells (MQWs) were grown on GaN nanorod arrays. Photoluminescence measurements were performed to confirm the light emission from the MQWs. Strong emission peaks were observed from the nanostructures. We believe the dominant emission peak results from the large exposed surface area of the sidewalls of GaN nanorods. The exposed sidewalls of nonpolar {1-100} planes are potential candidates for the growth of heterostructures of InGaN-based materials to reduce the piezoelectric fields and increase the radiative recombination efficiency for the LED applications. This work was funded in part by support in the early phases from NSF through Award Numbers ECS-0501634 and ECS-0507270. Later phases were supported as part of the Center for Energy Nanoscience, an Energy Frontier Research Center funded by the U.S. Department of Energy, Office of Basic Energy Sciences under Award Number DE-SC0001013.

11:20 AM

II9, Molecular Beam Epitaxial Growth and Characterization of InN Nanocolumns on GaN Templates:

Ke Wang¹; Tomohiro Yamaguchi¹; Tsutomu Araki¹; Euijoon Yoon²; Yasushi Nanishi¹; ¹Ritsumeikan University; ²Seoul National University

InN nanocolumns (NCs) have attracted much attention recently as they are not only suitable for studying fundamental physical properties, but also able to be applied as building blocks for a range of nanoscale devices, including infrared emitters, transistors, biosensors, and solar cells [1-6]. In this work, we investigate InN NCs grown on MOCVD GaN templates using radio frequency plasma assisted molecular beam epitaxy (RF-MBE). We have also grown InN NCs on sapphire substrate as comparison. All InN NCs were grown under very nitrogen rich conditions. The III/V ratio to achieve nanocolumns is estimated to be ~1/6 for N-polar InN on sapphire substrates and ~1/9 for In-polar InN on

GaN templates. In the case of sapphire substrates, the diameter of NCs is in the range from 30 to 70 nm with density of $\sim 2 \times 10^{10}/\text{cm}^2$. The optimized growth temperature is around 450 °C if we adopt the low temperature nitridation and In nucleation [2]. The XRD (0002) rocking curve of InN NCs grown at optimized conditions is only 1.3 arcmin, indicating the growth direction of NCs is well aligned to c-axis. In contrast, for InN NCs grown on GaN templates, the density of NCs is about two orders of magnitude lower, $\sim 1.0 \times 10^8/\text{cm}^2$, than that on sapphire. The diameter is estimated to be from ~ 300 to ~ 600 nm. InN NCs show clear hexagonal shape with faceted top surface and very smooth sidewalls. More important, they are highly homogeneous in their height (~ 1.2 μm) and exhibit no change in their diameter along the column after the initial ~ 250 nm. The growth rate is estimated to be 0.51 $\mu\text{m}/\text{h}$ vertically and about 0.12–0.25 $\mu\text{m}/\text{h}$ in the lateral direction. Strong photoluminescence (PL), comparable to InN films, has been observed for both kinds of NCs at 77 K. The PL peak of In-polar InN NCs on GaN is at a lower energy, with a narrower linewidth and also stronger integrated intensity (~ 2.5 times), compared to that of N-polar InN NCs on sapphire. The influence of various growth parameters, such as growth temperature, III/V ratio, nucleation layers, on the morphological, structural, and optical properties of such InN NCs is under investigation.

11:40 AM

III10, Vertical Transport in GaN/AlGaIn Resonant Tunneling Diodes and Superlattices: *Elias Wardel*¹; *Salam Sakr*¹; *Maria Tchernycheva*¹; *François Julien*¹; ¹Département Photis, Institut d'Electronique Fondamentale, UMR 8622 CNRS, Université Paris-Sud XI

Fabrication and operation of many optoelectronic devices need good understanding as well as precise control of the vertical transport. This is particularly true for GaN/AlGaIn devices such as the GaN/AlGaIn THz quantum cascade lasers or quantum cascade detectors. However, the numerous experimental attempts to study the vertical transport in the III-Nitride thin film resonant tunneling diodes (RTD) haven't been convincing so far. In particular, the experimentally observed negative differential resistance (NDR) in the I-V measurements tentatively attributed to quantum effects were found to be irreproducible^{1, 2, 3, 4} because of the carrier trapping in material defects and leakage current through dislocations. These difficulties to observe experimentally an NDR effect have been recently solved in the case of GaN/AlGaIn nanowires⁵ thanks to the improved material quality. Using the transfer matrix method⁶, we theoretically study the vertical ballistic transport in GaN/AlGaIn RTDs and superlattices with a small number of periods. Details on the numerical method are given in reference [7]. We have calculated the transmission probability, T , vs. the longitudinal electron energy and the current density-voltage characteristics J - V . In the case of a simple RTD, systematic calculations of both T - E and J - V characteristics have been performed for different Al contents in the barriers, as well as for the variable barrier and well widths. Applied to the RTD structure, our calculations demonstrate: a) the increase of the peak to valley ratio (PVR) of the NDR with increasing Al content in the barriers, b) the dependence of the J - V resonances values on the current direction, c) the asymmetry of the NDR with respect to the current direction due to the huge internal electric field in the structure. Furthermore, an optimized RTD structure operating symmetrically whatever the direction of the applied voltage is proposed. Finally, in the case of short period superlattices, the calculations show the validity of the used model and of the numerical method to study GaN/AlGaIn devices based on multiple heterostructures.

Session JJ: Compound Semiconductor Growth on Silicon Substrates

Friday AM
June 24, 2011

Room: Lobero
Location: Univ. of California-Santa Barbara

Session Chairs: Thomas Rotter, UNM; Gregory Triplett, University of Missouri-Columbia

8:20 AM Invited

JJ1, Growth Investigations of Lattice-Matched III/V Compound Materials on (001) Si Substrate for Optoelectronics: *Bernardette Kunert*¹; *Sven Liebich*²; *Martin Zimprich*²; *Andreas Beyer*²; *Stefan Ziegler*¹; *Kerstin Volz*²; *Wolfgang Stolz*²; ¹NAsP III/V GmbH; ²Material Sciences Center and Department of Physics

The monolithic integration of III/V compound materials on Silicon (Si) substrates moves back into focus of interests after a long history of research. In particular the application for high-mobility n-channel materials in Si-based CMOS transistors as well as for optoelectronic devices is of rising importance. In the latter case the realization of III/V laser diodes on Si substrate with sufficient life time could finally allow for the monolithic combination of optical data processing with the mature Si microelectronic technology and therefore open up a completely new field of micro-chip functionalities. One of the major obstacles in the hetero-epitaxy is the large lattice-mismatch between most common III/V compound semiconductor materials and Si, which leads inevitably to the formation of misfit- and threading dislocations, which is most critical for any device performance. In contrast, the lattice-mismatch between GaP and Si is very small and offers the immense advantage in dislocation-free monolithic growth of GaP on Si substrate by the incorporation of a few percentages of Nitrogen (N) or Boron (B). However, because of the indirect band gap of GaP this approach has been mainly ignored in the past. The novel dilute nitride Ga(NAsP) based on GaP has been especially developed for the lattice-matched and defect-free integration of a direct band gap material on Si. The high As concentration of the quaternary compound material guarantees the direct band gap formation whereas the incorporation of N enables the adjustment of the lattice constant of Ga(NAsP) towards the one of Si. Optical gain measurements of Ga(NAsP) quantum well (QW) structures reveal excellent optical properties comparable to standard III/V laser materials. Therefore, the novel Ga(NAsP) laser material offers an entire new approach for the defect-free integration of optoelectronic devices on Si substrate. In this paper we discuss growth investigations using metal organic vapour phase epitaxy (MOVPE) for the deposition of Ga(NAsP) QW laser structures lattice-matched on (001) Si substrate. Electrical current injection involves the growth of p- and n-doped cladding layers based on (BGa)P. The quaternary barrier material (BGa)(AsP) ensures a better carrier and light field confinement in the Ga(NAsP)/(BGa)(AsP) based separate confinement hetero-structure (SCH) of the laser diode. Due to the difference in the thermal expansion coefficients of III/V compound semiconductors and Si, each device layer requires a precise strain-management at growth temperature. High-resolution X-ray diffraction (XRD) analysis in line with transmission electron microscopy (TEM) studies did not show any indication for dislocation formation in the several micrometers thick III/V laser device grown on (001) Si substrate. Structural and optical properties of these first electrical pumped laser devices will be introduced and discussed in detail.

9:00 AM Student

JJ2, Coalescence Phenomena in Narrow-Angle Stripe Epitaxial Lateral Overgrown InP by MOCVD: *Nicholas Julian*¹; *Philip Mages*¹; *Steven DenBaars*¹; *Larry Coldren*¹; *Pierre Petroff*¹; *John Bowers*¹; ¹University of California, Santa Barbara

The primary goals in Epitaxial Lateral Overgrowth (ELO) of one material over another are a) defect reduction and b) maximizing the amount of lateral growth vs. vertical growth. However, unless the material is very insensitive to

defect concentrations, the usable size of even the largest field of ELO material will be cut in half by a coalescence front that creates defects when the two lateral growth wings converge. Work by Olsson et al. has shown promising Photoluminescence (PL) results where HVPE-grown ELO InP on Si appears to have coalesced with a reduced number of recombination center defects¹. One aspect of their approach involves using the so-called zipper effect² which relies on the idea that the coalescence defects can be eliminated if the convergence of two lateral growth fronts can be arranged to occur at certain optimal angles. This is intended to avoid simultaneous convergence at multiple points along the convergence front, as experienced by parallel lines. We have investigated the zipper effect in ELO InP by MOCVD using various growth conditions on paired ELO stripes with very narrow opening angles of 5.6° along 32 different stripe directions ranging from [-110] to [1-10]. This is in contrast to the usual approach of using large opening angles that maximize the amount of lateral ELO material per length of coalescence front. We observe multipoint coalescence as forming dimples or voids along the coalescence front and find that their formation occurs most often in the orientations with the highest overall coalescence rate. Our results illustrate the balance between mixed-plane sidewall formation and lateral sidewall growth rate, allowing optimization of multipoint coalescence and the resultant dimples. We present SEM images showing that slight deviations from high rate/high void orientations and tuning of growth parameters, especially Phosphorus overpressure, allow for the elimination of these voids by changing the sidewall faceting at the moment of coalescence. Further information from ongoing Atomic Force Microscopy, Luminescence and Transmission Electron Microscopy characterization of the resulting coalescence fronts will be presented as well.

9:20 AM

JJ3, Growth Habit Control of Epitaxial Lateral Overgrown InP on Si Substrates by MOCVD: *Phil Mages¹; Nick Julian¹; Chong Zhang¹; Larry Coldren¹; Steve DenBaars¹; John Bowers¹;* ¹Univ. of California Santa Barbara

In this work we revisited the oft-attempted idea of Epitaxial Lateral Overgrowth (ELO) of InP on Si. Owing to the large number of failed attempts at this goal in the past, we have refocused our efforts on a few key growth and geometric relationships that seem to be held in common between InP-on-Si and the more successful c-plane III-Nitrides on sapphire ELO system. In contrast to most past attempts we do not focus initially on the all-important lateral/vertical growth ratio. Instead we consider the creation of an ELO film from the perspective of four key phases: Nucleation within the windows; Cresting of the III-V to the height of the dielectric; steady-state Lateral Propagation; and Film Coalescence. Each phase has different requirements for the sake of reducing defects, propagating laterally and producing a smooth film. Throughout this whole process we focus most closely on the detailed crystal habit of the growing films. We do this because in the past it has been found that lateral growth is easily stalled at some point during attempts to extend growth laterally until coalescence[1]. It has been found that the growth habit or cross-sectional faceting of the ELO material is strongly correlated to the orientation of the stripe opening [2]. We find that both of these results are due to the tendency of certain growth-limiting facets to form and have located parameter windows in which we can control the growth habits of the films during each phase of the ELO process. Namely, we present the results of varying stripe/mask geometry and orientation and discuss the most significant growth condition effects on the morphology of the films prior to and during coalescence. The result is the controllable production of stripes having sidewall geometries ranging from linear and smooth through strongly faceted and weakly roughened. We control profiles showing variation between the natural preference for (111)A and B planes and mixed plane circumstances of differing value for continued lateral propagation and coalescence. Primarily we show that the cross-sectional growth habit of the ELO material is extremely sensitive to stripe orientation with misalignments as small as 5° being very significant. Secondly we demonstrate that the effective local overpressure of Phosphorous (TBP) at the lateral growth front is most important to the sidewall formation and faceting at any growth rate or mask geometry.

9:40 AM

JJ4, Integration of InAs/GaAs Nano/Micro Structures with Silicon by Selective Area Epitaxy: *Guan Huang¹; Faxian Xiu¹; Liang He¹; Yong Wang²; Xufeng Kou¹; Xinxin Yu¹; Kang Wang¹;* ¹University of California at Los Angeles; ²University of Queensland

III-V compound semiconductor epitaxially grown on silicon has attracted interest due to its applications in integration of optoelectronic devices with silicon-based microelectronics. In the present study, we have investigated the formation and optical properties of InAs/GaAs nano/micro structures grown on silicon by selective area epitaxy. The starting wafers are (001) and (111) oriented silicon substrates. First, a 60nm thick SiO₂ layer is thermally grown as mask. Arrays of holes with diameters ranging from 400nm to 1µm are then patterned on these substrates by stepper and subsequent dry etching. After proper cleaning procedures, growth is performed in Molecular Beam Epitaxy (MBE) chamber. Substrate temperature is shown to strongly affect the morphology and selectivity of GaAs grown on the patterned silicon substrates. In the silicon (111) case, at 550°C, almost no selectivity is observed and the deposited GaAs shows an amorphous or polycrystalline feature. At 600°C, hexagonal shape crystals are formed at the patterned nanohole sites, showing enhanced material quality. However, the selectivity is not perfect as GaAs can be seen on SiO₂ surface. Complete selective growth is achieved at 630°C with very evident faceting, indicating single crystalline growth, although defects can be observed on some of the crystals. Above 670°C, desorption dominates under the applied arsenic overpressure and therefore no material is deposited. At optimal growth temperature, dimension of the selectively grown GaAs crystal can be as large as ~1µm with clear {011} facets as top surface and side walls. Samples grown with different deposition time reveal the time evolution picture of growth. At the beginning stage, GaAs nucleates at the edge of the circular patterns. These nanocrystals then incorporate more material and expand to fill the patterned holes as growth proceeds both vertically and laterally. Transmission Electron Microscopic (TEM) image shows that misfit dislocations and stacking faults exist in the patterned hole area. However, the laterally grown material on top of SiO₂ is almost dislocation free. Based on the selectively grown GaAs structure, GaAs/InAs/GaAs structure is realized with 2 monolayers' deposition of InAs. The growth mode of InAs on GaAs base material is not clear. One possible structure formation mechanism could be patterned quantum dots. Photoluminescence measurement shows a strong peak centered at ~1200nm at 80K. The relatively broad linewidth is probably due to non-uniform growth of InAs layer. Work supported by KACST.

10:00 AM Break

10:20 AM

JJ5, The Electrical Nature of Structural Defects in InSb Synthesized by Molecular Beam Epitaxy on Si (100) and GaAs (100): *Madhavi Edirisooriya¹; Tong-Ho Kim¹; Aruna Dedigama¹; Yang Yang¹; April Brown¹;* ¹Duke University

InSb has the narrowest band gap (0.18eV at 300K), smallest effective mass (0.0136m₀) and the highest room temperature electron mobility (78,000cm²/Vs) of the III-V semiconductors. Because of its high electron mobility, InSb has extensively studied for magnetic-field sensing applications and high-speed electronic devices. The mobility of InSb quantum wells and thin films grown by molecular beam epitaxy (MBE) on GaAs is partly limited by scattering resulting from the high concentration of crystalline defects such as threading dislocations and micro-twins that arise from the large lattice mismatch (14.6%) between the film and the GaAs substrate. Synthesis of InSb on Si substrates is even more challenging due to larger film-substrate lattice mismatch (19.4%) and the fact that the growth of non-polar materials such as InSb on a polar substrate (Si) creates anti-phase domains. The structural properties of these defects and their impact on electron mobility have been widely studied. However the electrical nature of these defects and their relationship to the film's electrical properties, specifically the electron density, has not been extensively studied. We report the results of a characterization study that enables articulation of the electrical nature of anti-phase domain boundaries and micro-twins in InSb epilayers grown on Si (100) and GaAs (100). Our

scanning capacitance microscope (SCM) imaging and Hall measurements show that the density of anti-phase domains and micro-twins influences the electron density of InSb epitaxial films grown on both GaAs and Si. Variations in the buffer layers enabled modifications of the densities of the defect types present in InSb. The SCM images show that both the micro-twin defects and anti-phase boundaries are electrically active, while the threading dislocations, revealed by wet etching in the films as etch-pit contrast, are not. Hall measurements show that an InSb layer on GaAs with a micro-twin density of $5.6 \times 10^6 \text{ cm}^{-2}$ shows a 10% increase (or $2.5 \times 10^{11} \text{ cm}^{-2}$ higher) in the electron density (at 300K) compared to the same structure synthesized without micro-twins. A similar behavior in electron density with anti-phase boundary density and micro-twin density is observed for InSb epilayers grown on Si (100). We conjecture that filled traps within the energy gap of InSb act as donors. From SCM imaging, micro-twin defects and anti-phase boundaries show a higher n-type nature compared to that for a depleted InSb surface, indicating the presence of filled energy states below the conduction band. Further characterization of dislocation-related electronic states in InSb is under investigation.

10:40 AM

JJ6, Low Leakage Current AlGaN/GaN HEMTs on Si Substrates with Partially Mg-Doped GaN Buffer Layer by MOCVD: *Li Ming*¹; ¹The Hong Kong University of Science and Technology

AlGaN/GaN HEMTs are excellent candidates for power electronics and Radio Frequency (RF) devices due to their superior properties [1], [2]. Although sapphire and SiC are commonly used substrates for the growth of AlGaN/GaN HEMTs, silicon is emerging as a promising alternative because of its low cost, large size as well as potential integration with advanced Si electronics. However, the growth of GaN on Si is more challenging than that on sapphire or SiC because of the larger mismatches in lattice and thermal expansion coefficient, resulting in a higher density of dislocations and cracks. Moreover, during the growth of GaN films on Si substrates at temperatures over 1000 °C, auto-doping of silicon from the substrate into the GaN buffer layers may occur, leading to a low resistivity buffer layer and large buffer leakage. To avoid or minimize this problem and increase device breakdowns, many groups chose to grow a fairly thick buffer with multiple interlayers for strain management. In this study, we used a $< 2 \mu\text{m}$ thick buffer, with a partially Mg-doped 1.0- μm GaN portion to increase the resistivity of the buffer layer. After the first set of interlayer, 125-nm lightly Mg-doped GaN was used to compensate the residual donors, followed by an 875-nm unintentionally doped GaN layer to decrease the scattering from the Mg dopants (Fig.1). It is very difficult to determine the exact doping level of the Mg in the thin structure. The AlGaN/GaN HEMTs were grown on Si (111) substrates by MOCVD in an Aixtron 2000HT system. The electron mobility of the HEMTs structure was over $1200 \text{ cm}^2/\text{V}\cdot\text{s}$ at room temperature. Transistors with device dimensions of LG/LGS/LGD/WG = 1/1/1/10 μm were fabricated without any post-process to block the leakage current. The devices exhibited a maximum drain current density (IDSS) of 1.14 A/mm at VGS = 2 V and the maximum transconductance (gm) was about 300 mS/mm. A minimum OFF-state drain leakage current of $8.3 \times 10^{-8} \text{ A/mm}$ (VGS = - 8 V) was achieved, and a gate leakage current density of $7.9 \times 10^{-6} \text{ A/mm}$ (VGS = -35 V and VDS = 0 V) was obtained. The ON/OFF current ratio was up to 2×10^7 , and the OFF-state breakdown voltage (VGS = - 5 V) was 104 V. Compared to recently reported AlGaN/GaN HEMTs on Si [3], [4], performance of these devices on Si is very favorable, which indicated that the partially Mg-doped GaN buffer layer is an effective way to reduce the leakage current of transistor. The small signal characterizations were also investigated with 0.25- μm gate length T-shaped gate devices, the current gain cutoff frequency fT and maximum oscillation frequency fMAX were measured to be 31.3 GHz and 22.3 GHz, respectively.

11:00 AM Student

JJ7, Effect of Growth Temperature on Composition of InAlN Alloy Grown by GSMBE on Si (111): *Md Rakib Uddin*¹; Mahesh Pandikunta¹; Vladimir Mansurov¹; Sandeep Sohal²; Georgiy Guryanov³; Mark Holtz²; Sergey Nikishin¹; ¹Nano Tech Center/Department of Electrical and Computer Engineering, Texas Tech University; ²Nano Tech Center/Department of Physics, Texas Tech University; ³Corning Inc.

$\text{In}_x\text{Al}_{1-x}\text{N}$ alloy spans the range of III-Nitride bandgap energies from InN (0.7eV) to AlN (6.2eV), covering the infrared to deep-UV region of electromagnetic spectrum.¹ Several papers described growth and characterization of InAlN alloy on GaN or AlN template using various processes.¹⁻⁵ However, very few papers described the growth of InAlN using Gas-Source Molecular Beam Epitaxy (GSMBE).⁴ In this work, we report results on the growth and characterization of $\text{In}_x\text{Al}_{1-x}\text{N}$ alloys in the low In composition regime ($0.02 < x < 0.08$) using GSMBE with NH_3 . Two-inch Sb doped n-type Si (111) wafers were used as substrates. Epitaxial growth of InAlN consists of four-steps: substrate preparation by wet chemical etching, thermal cleaning of the substrate surface in the growth chamber, epitaxial AlN buffer layer growth at 900 °C with Al and NH_3 precursors, and InAlN alloy growth at temperatures ranging from 550 to 650 °C with Al, In and NH_3 precursors. The Al and In were evaporated from effusion cells. For all samples, the effusion cell temperatures and NH_3 flux were kept constant. Typical growth rate was 0.2 $\mu\text{m/h}$ for both AlN and InAlN. Film thicknesses were $\sim 100 \text{ nm}$ for AlN and $\sim 500 \text{ nm}$ for InAlN. We also grew AlN/InAlN short period superlattices (SPSLs) for deep-UV emitter applications. Crystal structure, layer composition and surface morphology have been studied by High Resolution X-Ray Diffraction (HRXRD), Secondary Ion Mass Spectroscopy (SIMS), and Scanning Electron Microscopy (SEM). Symmetric (0002) 2-theta-omega XRD rocking curves show high-intensity distinct peaks for AlN and InAlN layers. Long-range 2-theta scans have confirmed that there are no other phases in the alloys. Asymmetric (101-1) XRD scans around the axis perpendicular to the surface also show peaks at every 60° phi angles which affirm single crystal structure of the InAlN layers. All samples were crack-free as observed by SEM. The SEM cross-sections also confirmed a sharp interface between AlN and InAlN layers. Both Optical Reflectance and Spectroscopic Ellipsometric (SE) measurements were used to determine the bandgap of InAlN. Bandgap energies and InN molar fractions have been calculated from SE and XRD, respectively. The SIMS results were in good agreement with these calculations. We found that concentration of InN in InAlN alloy linearly decreases from ~ 8 to $\sim 3 \text{ mol.}\%$ when growth temperature increases from 560 to 640 °C. The bandgap of InAlN decreases from ~ 5.8 to 5.1 eV when InN concentration increases from ~ 3 to $\sim 8 \text{ mol.}\%$. We will discuss the luminescence efficiency of InAlN alloys and their electrical properties. The optical and electrical properties of AlN/InAlN SPSLs will be reported.

11:20 AM Student

JJ8, Vapor Phase Epitaxial Growth of (211)B CdTe on Nanopatterned Si for HgCdTe Based Infrared Device Applications: *Shashidhar Shintri*¹; Sunil Rao¹; Charles Schaper²; Ishwara Bhat¹; ¹Rensselaer Polytechnic Institute; ²Transfer Devices

There is a crucial need to grow high quality epitaxial CdTe on (211)Si, which is used as a buffer layer for subsequent growth of HgCdTe, presently the material of choice in the USA for fabricating IR based focal planar arrays (IR-FPAs). With the progress made so far, CdTe films with threading dislocation (TD) density as low as mid- 10^5 cm^{-2} are routinely obtained by MBE. The TD density needs to be further reduced by at least an order of magnitude for the devices to work in the LWIR region. Epitaxial CdTe growth on nanopatterned Si offers a promise, since the confinement obtained due to nanopatterning provides new pathways for defect annihilation. The goal of the present work is to study the feasibility of using nanopatterned Si for the CVD growth of epitaxial (211)B CdTe. At the 2010 EMC conference, we had presented epitaxial growth of CdTe on nanopatterned Ge/(211)Si, but the initial Ge growth and the nanopatterning of Ge/(211)Si needed improvement possibly due to poorer Ge surface morphology. Here, we present the direct growth of Ge and CdTe on nanopatterned SiO_2 /(211)Si substrates since patterning of SiO_2 on Si is

presumably easier. Patterning of 3" SiO₂/Si wafers was carried out at Transfer Devices Inc using nanotransfer lithography with water soluble templates to produce circular holes of ~400 nm and a pitch of ~540 nm. The oxide thickness was ~60 nm. Selective Ge and CdTe growth was carried out on these SiO₂/Si substrates using custom-built CVD reactor equipped with precursors for the growth of Ge, ZnTe and CdTe. Epitaxial CdTe directly on Si is challenging, hence selective Ge was first grown by As passivation of exposed Si. As passivation helped in preventing Si surface contamination by the residual Te present in the reactor and also promoted layer-by-layer evolution of selective Ge. Selectivity was achieved in the temperature range of 575-675°C. Selective CdTe was then grown inside the holes. Pressure and temperature were invariably varied between 25-100 torr and 350-495°C respectively to achieve CdTe selectivity. In addition, in-situ annealing was carried out to improve the crystal quality. Once the islands merged, the conditions were changed to get higher growth rates. The films were characterized by SEM, AFM, XRD and TEM. A comparison of the CdTe films grown on nanopatterned and non-patterned (211) Si showed an improvement in the crystal quality due to patterning. However, the surface was rougher compared to the best blanket CdTe/Si. Further growth studies are being carried out to improve both the surface roughness as well as crystal quality that will be presented at the conference. This work was partially supported by US Army STTR contract W911NF-08-C-0071 through Brimrose Corporation. We thank Dr. William Clark of ARO for all the encouragement.

11:40 AM Student

JJ9, Synthesis and Characterization of ZnTe Grown by VLS Method: *Jih-hong Peng*¹; *Ebraheem Azhar*¹; *Ronald Roedel*¹; *Sandwip Dey*¹; *Hongbin Yu*¹; ¹Arizona State University

Over the last few years, the materials of wide bandgap II–VI semiconductors has been widely studied because of the interests in their fundamental structural, electrical and optical properties. Among them, Zinc telluride (ZnTe) is one of the attractive and important II–VI compound semiconductor with a direct bandgap of 2.3 eV that is used in many applications in optoelectronic devices. The intrinsic ZnTe usually has p-type conductivity, and this character can be further enhanced by appropriate doping allowing the formation of p-n junctions by combining ZnTe with other n-type semiconductors. ZnTe thin films can be prepared by several techniques, such as molecular beam epitaxy (MBE), electrodeposition, metal-organic chemical vapor deposition (MOCVD), thermal evaporation, etc. In this work, we present the study of ZnTe thin films and nano-structures, for example nanowires (NWs), that are synthesized through a simple vapor–liquid–solid (VLS) method. The growth of ZnTe was performed on Si substrate with or without Au catalysts deposited by sputtering technique. Half of the Si substrates have the Au catalysts on them and the other half substrates have no Au catalysts, and they are placed alternatively in the growth furnace along different temperature zones. Argon is introduced as carrier gas. ZnTe power (99.99%) is loaded into a ceramic boat as the source material. The ceramic boat is placed at the center of the tube furnace with highest temperature about 750 °C. By controlling the presence or the absence of Au catalysts and controlling the growth parameters such as growth temperature, we can obtain different morphologies of ZnTe, such as thin films and NWs at the same run. The characterization of the ZnTe NWs was performed using scanning electron microscope (SEM), X-ray diffraction (XRD), Photoluminescence (PL), Energy-dispersive X-ray spectroscopy (EDX), etc. The morphology of ZnTe can be checked through SEM analysis. The ZnTe NWs can be grown with the aid of Au catalysts, while without Au catalysts ZnTe polycrystalline thin films are prevalent instead. The X-ray diffraction (XRD) data demonstrates that ZnTe NWs has the crystal orientation of (111), (220), and (311). The content of tellurium is higher than zinc from the EDX spectrum revealing a nonstoichiometry of the ZnTe NWs. Because the saturated vapor pressure of zinc is higher than that of tellurium, the films deposited from nominally stoichiometric source will be Zn deficient. The PL measurements exhibits that the photons emission in ZnTe NWs at wavelength 552 nm. The broad peak between 600-800 nm can be attributed to oxygen impurities in ZnTe film. The light scattering measurement from ZnTe also confirms photons absorption at wavelength around 540 nm.

Session KK: Nanowire Growth and Applications

Friday AM
June 24, 2011

Room: Lotte Lehman
Location: Univ. of California-Santa Barbara

Session Chairs: William Wong, University of Waterloo; Suzanne Mohnhey, Pennsylvania State University

8:20 AM Student

KK1, Size Effects in Ni Catalyzed Germanium Nanowire Growth: *Shruti Thombare*¹; *Ann Marshall*¹; *Paul McIntyre*¹; ¹Stanford University

The great majority of literature studies of Ge nanowire growth have used Au as a catalyst. In most cases, growth is said to have occurred by the VLS mechanism. Gold has been a popular choice as a catalyst in part because of its ability to form a eutectic with Ge, allowing nanowire growth at a temperature below 400 C. However, Au induces trap levels deep in the Si and Ge bandgaps. In order to make deposited Ge nanowires compatible with silicon-based electronics and useful for photovoltaic applications, an electronically benign metal catalyst may be required. We report an investigation of low temperature Ge nanowire growth using Ni, which is electronically more benign than Au. Ni nanoparticles in colloidal solution were drop-cast on Ge (111) substrates. Ge nanowires were grown at temperatures as low as 375°C in a cold-wall CVD reactor with hydrogen diluted Germane as reactive precursor. Nanowire growth is expected to occur by the vapor-solid-solid (VSS) mechanism with a germanide of Ni as the catalyst phase, because the growth temperature is depressed by greater than 300° C relative to the lowest eutectic temperature in the Ni-Ge binary system. We observed a great difference in the morphology of the nanowires as a function of their diameter. Their length and preferred crystallographic orientation were strongly dependent on nanowire diameter. Nanowires with diameter greater than 25-35 nm are <111>-oriented and have a high density of grown-in defects such as twins and stacking faults and exhibit frequent kinking. Transmission electron microscopy showed that nanowires with diameter smaller than 25-35 nm, which grow preferentially in the <110> direction, appear to have no kinks despite having a substantial density of crystal defects. The observed size-dependence of Ge wire morphology will be discussed in terms of wire surface energies and the structure of the catalyst/nanowire growth facet interface.

8:40 AM Student

KK2, Effects of Annealing on Sub-Eutectic Heteroepitaxial Growth of Germanium Nanowire on Si (111) Substrate: *Sung Hwan Chung*¹; *Se Jun Park*¹; *Bong Joong Kim*¹; *Minghao Qi*¹; *Xianfan Xu*¹; *Eric Stach*¹; *Chen Yang*¹; ¹Purdue University

Germanium Nanowire (GeNW) has drawn the interest for electronic device material since it has high intrinsic hole and electron mobilities compared to silicon, low growth temperature through Vapor-Liquid-Solid growth, and its compatibility with the current silicon VLSI technology. Heteroepitaxial growth of GeNW on the Si substrate is the key for a direct bottom-up self-assembly of three-dimensional device applications. In this study, we examined the effect of the annealing condition prior to the introduction of the precursor. Annealing below the Au-Si eutectic temperature (T_e) leads to the formation of a single, well oriented interface that templates heteroepitaxial nucleation, whereas annealing above Au-Si T_e leads the formation of multiple nucleation sites and randomly oriented growth. The Si substrate was treated under buffered hydrofluoric. A mixed solution of 40nm Au colloidal nanoparticles and 10% HF/H₂O was dispersed on the substrate. The substrate was then loaded into hot-wall tube furnace, and annealed between 280°C to 400°C for 5 min in 100 Torr with H₂ flow. After annealing, GeNWs were grown using GeH₄ (diluted in H₂) at 280°C. The results are observed by using scanning electron microscopy (SEM). The substrate underwent growth step without annealing step (GeH₄ is flown right after reaching the growth temperature) shows poor growth. Therefore, certain stabilization time for annealing is required for reproducible

epitaxial growth of GeNW. The GeNW growth results are compared between different annealing temperatures. The GeNWs grown on Si (111) after annealing temperature of 280°C and 320°C have uniform diameters of ~50nm without significant tapering along an average length of ~2.2µm. Most of the NW is grown perpendicular to the (111) substrate and the others are also along with the other <111> direction. Transmission electron microscopy (TEM) of the GeNWs confirms the crystalline nanowires are grown along [111] direction. In comparison, when the substrate is annealed at 400°C for 5 min prior to GeH₄ flow, there is no successfully grown GeNW. The results suggests that the substrate annealing below the eutectic temperature (T_e) of the substrate (Si) and catalyst (Au), 363°C, is critical for the heteroepitaxial growth of GeNWs on Si(111). When Au is annealed at below T_e of Au-Si, a well-defined interface between Au and Si(111) is formed. However, when the substrate is annealed at above Au-Si T_e, an Au-Si eutectic liquid alloy develops facets below the substrate. When the temperature is lowered into the growth temperature 280°C, some amount of Si from Au-Si alloy is rejected. Subsequent provision of Ge via GeH₄ to the solidified Au-Si alloy will result in non-epitaxial growth. This study shows that the annealing below T_e of the substrate and catalyst is necessary for the heteroepitaxial GeNW growth, and it can be applied for a direct assembly of applications.

9:00 AM Student

KK3, Catalyzed Vapor-Liquid-Solid Oxidation: Germanium Oxide Nanowires: Marika Gunji¹; Shruti Thombare¹; Paul McIntyre¹; ¹Stanford University

Germanium oxide (GeO_x) nanowires (NW) may find application in future optical communication devices. Photoluminescence (PL) study of GeO_x nanocrystals has shown that GeO_x can exhibit blue or green luminescence. Several synthesis methods for crystalline GeO_x nanowires have been reported including laser ablation, thermal deposition of germanium dioxide (GeO₂) powders, and metal catalyzed growth in a germanium- and oxygen- containing ambient. Here we report a novel method for directed synthesis of GeO₂ wires by thermal oxidation of gold (Au) catalyst-tipped Ge <111> single crystal nanowires. During oxidation at temperatures greater than the Au-Ge binary eutectic temperature (T > 361 °C), one-dimensional oxidation of as-grown Ge NWs occurs by Ge diffusion through Au-Ge catalyst droplet driven by the free energy of oxidation of Ge dissolved in the droplet in the presence of oxygen. Elongated GeO₂ wires form at the catalyst tip, consuming the adjoining Ge nanowire as they grow. The oxide nanowire diameter is dictated by the catalyst diameter, and their alignment generally parallels that of the initial Ge nanowires, although some viscous flow of the oxide, causing GeO₂ wire bending, is evident. Transmission electron microscopy and scanning electron microscopy were used to investigate the kinetics of VLS oxidation induced GeO₂ nanowire growth.

9:20 AM

KK4, Catalyst Proximity Effects on the Synthesis of Si Nanowires for In Situ Scanning Electron Microscope Li Intercalation Experiments: Steven Boles¹; Andreas Sedlmayer¹; Charles Ho²; Di Chen¹; Oliver Kraft¹; Eugene Fitzgerald²; Reiner Mönig¹; Carl Thompson²; ¹Karlsruhe Institute of Technology; ²Massachusetts Institute of Technology

Silicon nanowires have been actively pursued for potential use in numerous electronic applications, including solar cells to batteries to transistors. Controlled wire synthesis is critical to fabricating nanowire-based devices and is found to be dependent on many factors in the vapor-liquid-solid (VLS) growth process including chemical vapor deposition (CVD) conditions, substrate geometries and catalyst configurations. In some cases, varying the catalyst deposition conditions or catalyst density on the substrate surface can have a tremendous impact on wire growth despite fixed CVD conditions. Understanding and manipulating these conditions is essential to creating ideal wire geometries for applications such as solar cells or lithium-ion batteries. In this work we present high aspect-ratio Si nanowires grown by the VLS mechanism for in situ scanning electron microscope (SEM) lithiation studies. Silicon nanowires were fabricated using Au-catalyst nanoparticles and silane (SiH₄) gas in a commercial CVD system. Au was deposited on the substrate

surface by electron-beam evaporation and Au-colloid deposition. Both kinking defects and vertical nanowire epitaxy on Si <111> substrates were found to be directly related to SiH₄ flow rate. A correlation between Au-colloid dilution and nanowire growth rate was found to be in good agreement with a SiH₄ reaction model which predicted an increasing growth rate of Si nanowires with increasing concentration of Au-catalyst particles. A method of enhancing SiH₄ decomposition was employed to fabricate high aspect ratio Si nanowires with relatively low Au-colloid dilutions. These nanowires preferably grow parallel to the surface of the substrate making them ideal for harvesting with nano-manipulator probes. After growth the nanowires were loaded into an SEM for intercalation experiments with Li metal. A nano-manipulator probe was used to pick individual wires off of the substrate and to position the wire for testing. An ionic liquid electrolyte was used to facilitate the lithiation and delithiation process in the Si nanowires. The high aspect-ratio of the wires was found to be critical to both the harvesting procedure, as well as the lithium intercalation process as it allows for in situ SEM investigations of the pristine Si nanowire with minimal charging of the nearby electrolyte. Implications towards potential Si nanowire batteries are also discussed.

9:40 AM

KK5, A-Si / Si Nanowire Hybrid Photovoltaics: Surobh Raychaudhuri¹; Rene Lujan¹; Katherine Song¹; Chris Paulson¹; Robert Street¹; ¹Palo Alto Research Center

The trade-off between solar cell thickness and carrier collection efficiency places a practical limitation on planar amorphous Si (a-Si) photovoltaic devices which prevents them from efficiently absorbing light in the longer wavelengths. To address this issue we have devised a scheme where a thin a-Si cell is deposited over a disordered Si nanowire (NW) mat. The disordered geometry of the NW mat scatters light causing a photon to interact with multiple nanowires increasing the probability that it will be absorbed. The NW mat makes it possible to improve the absorption efficiency of the cell without increasing the cell thickness and thus results in enhanced absorption at the longer wavelengths. We fabricated and studied these a-Si / Si Nanowire hybrid structures. The NW mats are grown using the VLS technique with nanowire lengths of 5-10 microns. The nanowires are coated with 100-400 nm a-Si PIN solar cell structures. Top contact is achieved by using a transparent conducting oxide. We are able to grow disordered mats on a variety of substrates including silicon, glass and flexible stainless steel foil which allow for a variety of novel designs. We present electrical and optical characterization data for our NW hybrid photovoltaics. We will examine how disordered mat geometries can be optimized to impact cell performance. Our current device designs show a 10 fold increase in the absorption of red/infrared light (>700 nm) over comparable planar devices. We will also discuss the challenges in fabricating and optimizing these devices for efficient operation. Our experiments focus on device geometries that can be fabricated using techniques that are compatible with a-Si processing technologies.

10:00 AM Break

10:20 AM

KK6, Internal Quantum Efficiency in Nanorod LED Arrays Created by Top-Down Techniques: Qiming Li¹; George Wang¹; Karl Westlake¹; Mary Crawford¹; Stephen Lee¹; Daniel Koleske¹; Jeffery Figiel¹; Karen Cross¹; Saeed Fatholouloumi²; Zetian Mi²; ¹Sandia National Laboratories; ²McGill University

The external quantum efficiency of light-emitting diodes (LEDs) is determined by its internal quantum efficiency (IQE) and light extraction efficiency. The improvement of light extraction efficiency can be dramatically improved by creating additional optical escape routes through texturing the surface of planar LEDs. However, it is not clear that the texturing process, such as plasma etches, will negatively impact the IQE of the devices or not. In this paper, we developed a top-down process for creating nanorod LED arrays from planar LED epitaxial wafers. The IQE of these nanorods was studied and compared to planar LEDs. In the top-down process, we first use a self-assembled monolayer of silica colloids as mask during the plasma etching of MOCVD grown planar LED wafers. We then use a novel anisotropic wet etch technique to remove the plasma etch damage on the sidewall of the nanorod LEDs, which may

potentially reduce IQE of the nanorods LEDs. The anisotropic wet etch also allows precise control of the diameter and aspect ratio of the nanorod LEDs. The morphology of the nanorod LEDs was characterized by scanning electron microscopy and transmission electron microscopy. The optical performance of nanorod LEDs and planar LEDs was compared using photoluminescence (PL) studies. We observed that as the diameter of the nanorod LEDs decrease below 200 nm, the PL intensity increases dramatically and shows a total enhancement factor of 15 as compared with the planar LED samples. The IQE extracted from the temperature dependent PL studies revealed that IQE of the nanorod LEDs remains constant as compared with planar LEDs. Therefore, this top-down technique may be feasible for creating LEDs with high light extraction efficiency. In addition, the dislocation morphology in the nanorods LEDs were studied by TEM. We observed that the percentage of dislocation-free nanorod increases as their diameter decreases. This results suggest that the life time and reliability of the nanorod LEDs may be improved due to the fact of majority of the nanorods are free of dislocations. Sandia National Laboratories is a multiprogram laboratory operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under Contract No. DE-AC04-94AL85000.

10:40 AM Student

KK7, Electrochemically Deposited Branched Indium Antimonide (InSb) Nanowire Arrays as "In-Situ" Anti-Reflective Structures: *Asaduzzaman Mohammad¹; Suprem Das¹; Mohammad Khan¹; Muhammad Alam¹; David Janes¹; ¹Purdue University*

Semiconductor nanowire arrays, as opposed to their bulk counterparts, exhibit properties that may be of interest for next-generation photovoltaics and optoelectronic applications. For detectors and photovoltaic applications, vertical arrays of nanowires offer the potential to de-couple the two relevant length scales, i.e. the optical absorption length and the distance a photo-generated carrier must travel to be collected. Nanowire arrays also offer the possibility to change the overall electromagnetic environment, basically through tapering that causes the transition between air and the absorbing semiconductor region [1]. Bulk Indium Antimonide (InSb) is an interesting material for infrared detectors due to its low and direct bandgap ($E_g = 0.17\text{eV}$ at 300K). However, a semi-infinite InSb slab would have $\sim 40\%$ optical reflectance due to the significant impedance mismatch with air; thereby almost half of the incident light does not contribute to any device performance. In this work, we developed branched InSb nanowire arrays by electrochemical deposition into the partially branched pores of a porous anodic alumina (PAA) template. The branched nanowires exhibited a diameter of around 20 nm on the top branches and widened to a diameter of about 100 to 150 nm at the stems of the wires. Following etching of the alumina matrix to expose several microns of the branched wires ($\sim 20/956\text{m}$ from the top surface), the structure exhibited a very low reflectance (less than 5%) in the near infrared range ($0.75\ \mu\text{m} = \lambda = 2\ \mu\text{m}$). The branched structures provide a unique tapered transition between air and the body of the InSb nanowires. A detailed theoretical model considering the various length dimensions of the tapered region was developed to interpret our observed experimental data and explore the potential of such structure for optoelectronic applications.

11:00 AM

KK8, Aligned Assembly of Nanowire Arrays with Intrinsic Control: *Kyeong-Sik Shin¹; Chi On Chui¹; ¹UCLA*

As the emerging research materials candidates, semiconductor nanowires possess many superior characteristics over their bulk counterparts. For practical applications with flexible device design or scalable performance, a controllable number of nanowires should however be assembled in predefined locations, orientations, and morphologies to yield scalable, predictable, and repeatable device characteristics. The state-of-the-art aligned semiconductor nanowire array formation techniques can be broadly classified into three categories including in-situ aligned growth, ex-situ aligned assembly, and nanolithography-based patterning and etching. The ideal technique to form aligned 1-D nanowire arrays should guarantee an intrinsic and concurrent

control over the three key parameters benchmarking the array: (i) number of nanowires, (ii) inter-nanowire pitch, and (iii) nanowire diameter. Moreover, a viable nanomanufacturing technology should also be VLSI-compatible and scalable to any substrate size. This is a stringent yet essential requirement not only from the manufacturing throughput and robustness consideration. It also constitutes a good leverage of the infrastructural investment made by the industry during the past few decades. To enable genuine and agile heterogeneous device integrations, our approach to manufacture aligned 1-D nanostructures is primarily based on the ex-situ assembly route owing to its flexibility in material selection, ultra-low processing thermal budget, and low level of contamination during fabrication. In contrast to the existing techniques, we propose and demonstrate a novel concept to combine top-down lithography and crystallographic etching for aligned 1-D nanostructures manufacturing. The baseline strategy comprises three major steps: 1. Creation of an intrinsically controlled nanoscale periodic line array above the substrate surface. 2. Selective conjugation of 1-D nanostructures only onto the lines within the array. 3. Transfer of the aligned nanostructure array to different substrates. The approaches involved are based on the wafer-scale and VLSI-compatible philosophy yet they offer an intrinsic control over the number, pitch, and linewidth of the resultant aligned nanostructure arrays. Nanoscale, sub-lithographic pitch and linewidth are readily accomplished without seeking advanced lithography. The alignment to the pre-existing features on the target substrate is also inherently allowed as a side benefit if needed. Moreover, line edge roughness (LER) free features could be created for the first time that arguably enables an extreme linewidth scaling with suppressed variations. For further manufacturing yield enhancement, a novel nanotrench structure can be considered accompanying the pitch and linewidth reductions.

11:20 AM

KK9, Nanostructure Decorated AlGaIn/GaN HEMTs for Chemical Sensing: *Shrawan Jha¹; Igor Bello¹; ¹City University of Hong Kong*

Inherently n-type conductivity of ZnO has been exploited for sensing applications. The high sensitivity of ZnO, towards the exposure to NH₃, H₂, O₃, CO, NO₂, and ethanol etc., makes it viable for gas sensing applications. Similarly, the same sensors should respond to any oxidizing or reducing chemical environment when it is placed in a solution or exposed to a vapour or jet containing chemical analytes. We report AlGaIn/GaN based HEMT chemical sensors which show a reasonably fast response on exposure to chemical analyte in gas or solution phase. State-of-the-art GaN-HEMT process was used to fabricate bare-gated FET-like sensor structures, which was later covered by a dense layer of nanorods. While the most of the reported studies on similar topics exploit the conductance modulation in ZnO nanostructures, this work exploits surface and interface effects at the ZnO/GaN heterointerface coupled with signal modulation capabilities of HEMT structure. A two step growth process was used to grow ZnO nanorod arrays using a solution method that resulted in a matrix of nanorods over the entire exposed gate of proposed sensor structure. Typically, nanorods possess micrometer-scale length and submicrometer-scale width, and act as integrated nanoscale gate arrays of the GaN HEMT. Hall measurements revealed a noticeable decay of charge density in the AlGaIn/GaN heterostructure after the nanorod growth. Low-frequency noise measurements revealed the role of interface traps at the ZnO/GaN heterointerface. Analytical techniques indicated a high crystalline quality of the nanorods. A dense array of nanorods over the gate area played important role in the presented devices by means of facilitating quick absorption of chemical analytes, and in a much larger volume in comparison to a control device with no ZnO decoration on the gate area. A very large surface-to-volume ratio offered by the ZnO nanorod arrays could facilitate quick adsorption of large volume of chemical analyte. Sensor devices were installed in a chamber where gasses could be introduced in a controlled environment. Electrical response of the devices was recorded by means of acquiring current-voltage data at a fixed temperature and without any gate-bias. A device with dimensions identical to test devices and without any surface modification was used as control. Sensor response to Hydrogen gas was recorded at different temperatures. Further, transient response of the sensor was also recorded when it was exposed to human breath and it showed a significant and quick response. Sensing results suggest the potential of studied

structure for chemical sensing. This work was supported by the City University of Hong Kong Strategic Research Grant (Project No. 7008102).

11:40 AM

KK10, Environmental Stabilization and Functionalization of ZnO Nanobridge Sensors Fabricated Using Carbonized Photoresist: Ashley Mason¹; Chien-Chih Huang¹; Chris Heist¹; Myra Koesdjojo¹; Nate Stephon¹; Vincent Remcho¹; *John Conley*¹; ¹Oregon State University

Two of the major challenges to the application of nanowires as bio-sensors are the integration of nanowires into electrically accessible devices and functionalization for selectivity [1]. Recently, we demonstrated a method for the directed integration of nanowires that avoids the use of metal catalysts, seed layers, and additional patterning processes [2]. This method exploits the use of carbonized photoresist (C-PR) to direct the growth of ZnO nanowires [3]. Using lithographically patterned carbonized photoresist pads as electrodes, growth and electrical connection of nanowire bridges takes place simultaneously for many devices. Electrical measurements on three-terminal C-PR/ZnO nanobridge/C-PR devices show field effect modulation of the conductivity of the ZnO channel via a back gate. Nanobridge devices were found to perform well as gas (O₂ and H₂O) sensors and show excellent sensitivity to UV exposure (> 104 increase in current). In addition, the response of the three-terminal nanobridge sensors to UV and oxygen could be enhanced by the application of a negative bottom gate voltage. The use ZnO nanowires as selective sensors in vapor phase or aqueous environments requires protection and functionalization of the ZnO surface. In this work, we investigate the use of parylene, a common moisture barrier, as a protective coating and general platform for selective functionalization [4]. Whereas a chemical vapor deposition (CVD) process for parylene-C is fairly well established, the amine group on parylene-A can be used for anchoring functional groups, such as aptamers, that can be used to selectively sense a target species. A CVD process for parylene-A was developed. It was demonstrated that parylene-A coated ZnO NWs show increased water contact angle ($140 \pm 5^\circ$ for coated vs. $22 \pm 5^\circ$ for unmodified nanowires) and no signs of dissolution after 24 hours in an aqueous solution. The impact of the parylene-A coating on the electrical performance and environmental sensitivity of ZnO nanobridge devices was investigated. A comparison of H₂O and O₂ sensitivity for coated and uncoated devices revealed that a thin coating of parylene-A attenuated both the H₂O and O₂ response as compared to uncoated devices, suggesting the ability to modulate environmental sensitivity using this non-covalently bound polymer passivation layer. It has recently been demonstrated by others the amine group on parylene-A can bind to the carboxylate groups on bovine serum albumin (BSA) by utilizing a crosslinker, such as glutaraldehyde, to form a covalent bond [5]. Thus, in addition to protecting ZnO NWs from dissolution in liquid and vapor-phase sensing applications, parylene-A may also serve as an activation layer for further functionalization. This work demonstrates the novel use of parylene-A coating as a potential starting platform for the functionalization of ZnO NW devices for selective sensing in the liquid or vapor phase.

Session LL:

Materials Integration: Wafer Bonding and Engineered Substrates

Friday AM
June 24, 2011

Room: MCC Theatre
Location: Univ. of California-Santa Barbara

Session Chairs: Mark Goorsky, University of California, Los Angeles; Cindy Colinge, Tyndall National Institute

8:20 AM Student

LL1, Electrochemical Etched InP Porous Layer Formation for Layer Transfer: *Xiaolu Kou*¹; Mark Goorsky¹; ¹UCLA

Porous InP layer was fabricated on InP substrates to promote the transfer of subsequently grown epitaxial device layers to an alternate substrate. After epitaxial growth of InP on top of the porous surface, the mechanically weak

porous layer would facilitate transferring overlaying epitaxial layer onto any substrate, either flexible or lattice mismatched, enabling innovative device applications¹. Moreover, since the original substrate – except for the porous layer – remains intact after cracking through the porous layer, this technique allows the expensive seed material to be reused. Electrochemical etching was applied to fabricate the porous layer. Heavily doped n-type InP wafer was subjected to anodic current using a diluted HCl electrolyte to produce a low density porous layers of a few micron thickness. The porosity was modified by adjusting the current density or HCl concentration. The microstructure of the porous layers was confirmed by scanning electron microscope (SEM). Two morphologies of pores were identified, current line oriented and crystallographically oriented². The latter one was obtained when the current density was lower than 100 mA/cm² and was found to be more applicable because of its smoother surface for epitaxial growth. The RMS roughness of the porous surface was about 10 nm characterized by atomic force microscope (AFM) and chemical mechanical polishing (CMP) was applied to further reduce the roughness. High resolution triple axis X-ray diffraction was used to determine the strain condition within the porous layer. From reciprocal space mapping, the reciprocal points of the substrate and the porous layer got separated, and the porous layer exhibited compression, similar to the case of porous silicon formation under certain conditions. Furthermore, it was determined that the strain increased with increasing porosity. Young's modulus of the porous layer was calculated through nano-indentation measurements, and it was found that the modulus of porous layer can be controlled to be significantly lower than bulk InP. By adjusting the etching conditions, the porous layer can be made weak enough to guarantee easy splitting while sufficiently strong to withstand CMP and thermal treatment. This concept of controlled reduction in mechanical strength is promising to be applied to other compound semiconductors.

8:40 AM Student

LL2, Ion-cut Transfer of InP-Based High Electron Mobility Transistors Using Adhesive Bonding: *Wayne Chen*¹; Christopher Doran¹; Thomas Kuech²; S Lau¹; ¹UCSD; ²University of Wisconsin, Madison

In ion-cutting, a donor wafer is implanted with hydrogen ions and bonded to an acceptor substrate. Annealing allows for the hydrogen trapped in the implantation-induced damage to nucleate into gas bubbles and results in layer exfoliation. The advantages of ion-cutting include control over the transferred thickness as well as possible recycling of high-cost donors such as III-V semiconductors. Direct wafer bonding without adhesives require extremely flat wafer surfaces, with surface roughness rms values typically less than 0.5nm. Adhesive bonding overcomes these requirements and allows integration of donor substrates with alternative substrates such as sapphire, glass, or flexible plastics. Despite these advantages, one of the key drawbacks of ion-cutting is that the transferred films typically suffer from hydrogen implantation damage, which can be difficult to remove in III-V semiconductors, even with high temperature treatment. Compounding these issues is the fact that most adhesive agents have fairly low temperature tolerances, far below the temperatures needed for partial restoration. Recent work in ion-cutting and integration of InP with alternative substrates focus on the integration of optoelectronic components, such as lasers or photodetectors. These devices suffer from higher dark/noise current levels due to defects introduced by proton implantation. In this work, we investigate the ion-cut transfer of a majority carrier device: an InP-based modulation doped field effect transistor (MODFET). InP-based MODFETs utilize band offsets in epitaxial materials to place majority carriers into an undoped, narrow bandgap InGaAs channel, which results in exceptionally high carrier mobility. Lattice-matched InAlAs/InGaAs MODFET epilayers are grown by MOCVD. The device layers are implanted with hydrogen ions at high dose and low temperature, and then bonded onto sapphire using SU-8 adhesive. Mesa and gate recess are created using selective etch, and contacts are deposited by ebeam evaporation. The entire process is done at temperatures less than 150°C. The MODFETs were characterized by I-V measurements and shown to be nonfunctional due to the defects introduced by hydrogen implantation, particularly in regards to the Schottky-based gate. To transfer functional transistors, we discuss our experiments in patterned ion-cut transfer, where areas of interest are shielded from implantation but still

transferred by surrounding implanted regions. We show that patterned ion-cut transfer is strongly dependent upon crystal orientation and that using cleavage-plane oriented donors can be beneficial in transferring large areas of high quality semiconductor material.

9:00 AM

LL3, Investigation of PECVD Silicon Nitride Deposition on Porous Si: *Caroline Moulet¹; Mark Goorsky¹; ¹UCLA*

Porous semiconductor materials have presented a special interest since the invention of the ELTRAN® process leading to the transfer of epitaxial thin films. Because of the high qualities of the transferred layer, this process allowed the development of the first SOI substrates. However, the ELTRAN® process or similar methods are limited to the transfer of silicon homoepitaxial or pseudomorphic layers. Therefore, alternative processes including porous materials have been recently developed. In this study, we focused on a process suggested by Joshi et al. using porous semiconductor materials and direct wafer bonding in conjunction with hydrogen exfoliation process. The main steps consist in the direct bonding of an implanted wafer to a porous silicon wafer. Then, through an annealing treatment, there is exfoliation of the implanted substrate leading to the layer transfer on the Si handle wafer. Thus, various semiconductor materials can be transferred and used as a thin layer. The porous substrate can be chosen depending on the application, recycled and substrates with different orientations can be integrated. One of the key steps is the direct wafer bonding. Direct wafer bonding refers to a process by which two wafers are put into contact and held together at room temperature by adhesive forces, without any additional materials. The conditions to obtain a successful bonding are contaminant-free surfaces and smooth enough to allow an intimate contact. Therefore, before bonding the porous layer is generally coated with another material to produce defect-free and high strength bonding interface. Because of its properties and the possibility to be deposited at low temperature, silicon nitride (SiN) is often used as a “bondable” layer. This work presents an investigation of the SiN deposition on porous Si in preparation for wafer bonding. For that, porous silicon has been made by electrochemical etching and coated with different thicknesses of SiN layers. The SiN has been deposited by plasma enhanced chemical vapor deposition with a deposition rate of 120 Å/min. AFM measurements were performed on both porous Si and flat Si samples covered with the SiN corresponding to the same deposition times. In the case of porous Si, for short deposition times, the roughness increases and becomes compatible with wafer bonding again after 100 seconds of deposition. This is in agreement with SEM observations showing deposition mechanism of SiN through small, sub-micron size areas first, explaining an increase of surface roughness, and then the formation of a homogeneous and uniform layer. These analyses were complemented by EDX and TEM observations which brought more details about SiN deposition mechanisms. In contrast to SiN deposition on flat Si, a minimum thickness or deposition time is required to form a stoichiometric and uniform SiN layer on porous Si compatible with direct wafer bonding.

9:20 AM Student

LL4, Double Layer Transfer Made by the Smart Cut™ Technology and Embedded Porous Silicon Layer: *Anne-Sophie Stragier¹; Thomas Signamarcheix¹; Patrice Gergaud¹; Thierry Salvetat¹; Chrystel Deguet¹; Mustapha Lemiti¹; ¹CEA-LETI*

Double transfer of thin single crystalline processed layer can be very interesting for 3D integration and back side imager fabrication that require front and back side engineering of the Si active films. To fulfill such requirements, a recent alternative technology was developed at the CEA-LETI, based on the use of porous Si substrates. We previously reported on the first transfer of a non-porous/porous Si bilayer by the Smart Cut™ technology followed by a second layer transfer after low temperature bonding via a benzocyclobutene interlayer and mechanical separation in the porous layer. In this paper, a first single layer was transferred onto a porous Si layer by the Smart Cut™ technology and a second transfer was achieved by direct Si/SiO₂ bonding and mechanical separation. For this technology, 200mm p+ type Si substrates are superficially porosified by electrochemical anodization in a HF based

solution. Typical porous Si substrate was fabricated presenting homogeneous characteristics: a mean porosity value of 65% and an effective thickness value of 540nm. Such porosification step combined with the application of the Smart Cut™ technology lead to the perfect transfer of a 200mm Si layer onto a handling Si substrate (picture). Here the SOPL structure is composed by a top Si/SiO₂ bilayer transferred onto a superficially SiO₂-capped porosified substrate. Here the SiO₂ layer was included in between the non-porous and porous Si layers. The crystalline quality and the strain induced in the different layers were accurately determined by High-resolution X-Ray Diffraction (HRXRD) using Reciprocal Space Mapping (RSM) measurements. After chemical and mechanical polishing, the surface roughness of SOPL substrate was reduced to 0.1 nm (5*5µm² scan area), allowing a second hydrophilic direct bonding of SOPL structure onto another host substrate. The rupture energy needed to induce the mechanical separation in the buried porous layer was characterized by the method of Maszara. Complete mechanical separation in the weak porous layer was used to obtain a 200mm DT (Double-Transferred) Si substrate (picture). The superficial porous Si residues and the oxide layer protecting the active Si layer can be removed selectively by chemical etching. This paper demonstrates the stability of the SOPL structure with high thermal treatments for instance as involved in device integration, and its compatibility with double-sided layer processing. This technology offers many advantages such as substrates reuse, good doping characteristics of the active transferred Si layer and easy final post processing steps.

9:40 AM

LL5, LiNbO₃ Thin Single Crystal Layer Transfer by Smart Cut™ Technology: *Bruno Imbert¹; Francois de Guerville²; Nicolay Cherkashin²; Vincent Paillard²; Alain Claverie²; Frederic Mazen¹; Chrystel Deguet¹; ¹CEA; ²CEMES*

Transfer of single crystalline layer by Smart Cut™ technology has been improved over the last decades by substrate developments for various applications. From the best-seller SOI wafers to thin silicon layer on glass or sapphire, this technology has been developed to answer to specific material needs. With the increasing demands for telecommunications services, RF manufacturers require more and more ultra wide band filters. Most used applications are typically Surface Acoustic Wave (SAW) and Bulk Acoustic Wave (BAW) filters, based on piezoelectric materials. The transfer of thin single crystalline piezoelectric layers on specific receiver substrates could be an innovative, efficient and industrial engineered substrate solution. Lithium niobate oxide (LiNbO₃) strong piezoelectric coupling properties drive its choice in such an engineered substrate. This kind of substrate could open new ways for high quality factor solutions. The Smart Cut™ technology applied to LiNbO₃ thin film transfer has imposed development of dedicated process steps. This paper highlights the material behavior during the transfer process. First, a cleaning process has been developed to obtain a particle free surface without any degradation of initial roughness, leaving substrates compatible with direct bonding technology. Most of critical process steps have been controlled and characterized by mean of SIMS, XRD, TEM and RBS-c techniques. To achieve the RF structure, metallic electrode was deposited on the LiNbO₃ bulk substrate followed by a PECVD silicon oxide. Low chemical interactions between layers have been observed by SIMS characterization. The capped top structure was then subjected to ion implantation (e.g. He ions) with dose in the mid 10¹⁶ at/cm² and energy about 250 keV. Although implantation step for silicon on insulator wafers is well known, He implantation used for LiNbO₃ transfer process required advanced characterization to understand physical mechanisms. Ion implantation in LiNbO₃ was characterized thanks to quantitative and qualitative analysis. The top wafer surface was specifically prepared, for instance by CMP and wet cleaning processes, for bonding to a receiver substrate at room temperature thanks to a direct hydrophilic bonding. Then, a thermal anneal was performed to initiate nanocracks growth and to transfer the thin film of LiNbO₃ from the “donor” wafer. The final stack was also characterized to demonstrate the conservation of piezoelectric properties of the thin single crystal layer of LiNbO₃. This work is supported by French ANR under “POEM” project.

10:00 AM Break

10:20 AM Student

LL6, InGaAs-InGaN Wafer-Bonded Current Aperture Vertical Transistors: *Shalini Lal*¹; Eric Snow¹; Jing Lu¹; Stacia Keller¹; Umesh K. Mishra¹; ¹Department of Electrical and Computer Engineering, University of California, Santa Barbara

Wafer-bonded heterojunctions is an enabling technology that joins two dissimilar semiconductors which are otherwise difficult to grow epitaxially. This technology can be used to couple a narrow and a wide-bandgap semiconductor to simultaneously accomplish high speed and high breakdown in a transistor. One such transistor is a BAVET- Bonded CAVET (Current Aperture Vertical Electron Transistor). It consists of an $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ heterojunction Field Effect Transistor (FET) wafer bonded to an $\text{In}_{0.1}\text{Ga}_{0.9}\text{N}/\text{GaN}$ epilayer CAVET. The BAVET source lies in high-mobility InGaAs layer and the drain is buried in wide-bandgap GaN layer. The BAVET gate on InAlAs modulates current through a conductive aperture in the InGaN/GaN layer. These vertical apertures are defined by an isolation implant as earlier demonstrated for CAVETs. To achieve a fully functional BAVET, the structural design should meet some key requirements, namely, a strong wafer bonded interface, good current control through both the lateral FET and the vertical BAVET, and a minimal barrier to electron conduction through apertures. This paper reports our progress in achieving the above requirements for the BAVET. In the first demonstration of the BAVET, with implanted GaN layer, reasonable gate modulation and current saturation characteristics are achieved. This illustrates that wafer bonding process does not adversely affect the InGaAs channel. However, this device showed poor pinch-off of channel for both the FET and the BAVET. The pinch-off in FET is prevented by the re-grown InGaN layer acting as a parasitic conduction path underneath the gated region. By implanting the InGaN layer instead, a significant improvement in FET pinch-off is observed. This successfully removes one of the parasitic leakage paths affecting the BAVET characteristics. In Ga-face CAVET template, a thin InGaN interlayer is introduced to reduce the barrier to electron conduction through InGaAs-GaN wafer-bonded junction. The inclusion of InGaN layer, adds another polarization induced barrier to electron flow at InGaN-GaN interface. This barrier sets up a significant turn-on voltage when the device is biased as a BAVET. We are able to mitigate this barrier by intentionally increasing doping in InGaN/GaN layers. And thus, achieve a reduced turn-on voltage in BAVETs. However, high doping in InGaN layer is unfavorable to current blocking properties of implant; consequently affecting BAVET pinch-off. This vertical leakage path through the implanted InGaN layer is in the process of being remedied by optimizing implant and doping at the InGaN-GaN interface. To summarize, we successfully eliminated some of the leakage paths affecting current modulation in BAVETs and reduced the barrier in the apertures. The BAVET characteristics demonstrated in this work have greatly enhanced our understanding of the technology and its design space, enabling a steady progress in achieving bonded heterojunctions for transistor applications. The path to a fully functional BAVET is now clear.

10:40 AM

LL7, Electrical Conductivity of Directly Bonded Silicon/Germanium Hetero-Structures: *Isabelle Ferain*¹; John Hayes¹; Ran Yu¹; Ki Yeol Byun¹; Farzan Gity¹; *Brenda Long*¹; Cindy Colinge¹; ¹Tyndall National Institute

Direct wafer bonding of Silicon (Si) to Germanium (Ge) has already been successfully demonstrated. However, little has been published about the relationship between electrical characteristics of Si/Ge hetero-structures and the quality of their bonded interface. In the present work, the impact of thin buried oxides (BOX) at the bonded interface on the electrical conductivity of bonded p-Si/p-Si/p-Ge stacks is investigated. p-Si/p-Si stacks were directly bonded to p-type Ge wafers. On the Si wafers, silicon dioxide films were used with a thickness range of a few Angstroms to 12nm. Prior to in-situ bonding, wafers were exposed for 10 minutes to free oxygen radicals generated by a remote plasma ring within the bonding chamber. After bonding, the overall thermal budget of the anneal was limited to 300 °C. Slow ramp-up rate ex-situ anneals helped to minimize the formation of thermally generated voids. Cross-

sectional HR-TEM analysis of the bonded interface was used to characterise the BOX thickness. Limited discrepancy was observed between the oxide thicknesses prior to bonding and the subsequent thickness of the bonded interface. Ohmic contacts were fabricated on both sides of the bonded pair after formation of mesa structures. Due to the doping levels of the silicon and germanium, the total net current across the hetero-structure was expected to show a rectifying effect, with the total net current under positive bias (on the Si side) being significantly higher than its counterpart under negative bias. Such rectifying behaviour has been observed experimentally on our bonded Si/Ge samples. At low reverse bias, the electrical conductivity is shown to decrease exponentially as the BOX thickness increases linearly. As compared to an ideal oxide-free interface, bonded pairs with thin native oxides of silicon and germanium at the bonded interface present a dramatic (50 %) reduction of their conductivity in reverse bias. The rectifying behaviour measured on thin BOX samples was successfully matched to results of device simulations involving the same p-Si/p-Si/p-Ge hetero-structures and direct tunnelling across the bonded interface as main conduction mechanism. Electrical properties of SiO₂, GeO and GeO₂ were carefully selected and impact ionisation was neglected to a first approximation. These simulations helped to predict that the conductivity vs. BOX thickness trend remains valid at higher biases. They confirmed the substantial conductivity loss caused by native oxides. Our results stress the importance of an aggressive BOX scaling to enable the direct bonding approach for the fabrication of photodiodes for instance. This may pose some challenges in terms of bond strength, interface uniformity and yield.

11:00 AM Student

LL8, Interface Barrier Height Reduction in Wafer Bonded n-GaAs / n-GaAs by Sulfur Passivation Methods: *Michael Jackson*¹; Mark Goorsky¹; ¹UCLA Materials Science & Engineering

Sulfur passivation methods are examined for application to III-V wafer bonding where high interface conductivity is desirable for optoelectronic devices such as multijunction solar cells. Passivation methods have been utilized in the past to lower the grain-boundary potential barrier in polycrystalline silicon by hydrogenation¹, and HF acid treatment in hydrophobic Si bonding serves to passivate charges at the interface². For III-V surfaces, sulfide solutions are utilized to improve the electronic properties for Schottky contacts and HBTs, yet the use of passivation at III-V wafer bonded interfaces have not been fully examined. In this study, sulfide solution processing and a dry sulfur treatment method utilizing elemental sulfur vapor activated by ultraviolet light are demonstrated to produce large area bonding for GaAs/GaAs at 400°C without large compressive forces. The vacuum UV-sulfur method allows the role of sulfur at the interface to be investigated separately from the etching of the oxide. Electrical measurements of bonded GaAs/GaAs samples treated with UV-S, aqueous (NH₄)₂S, or NH₄OH, and annealed 2hrs at 400°C reveal the large barrier to conduction common for low temperature bonding of III-V materials, with (NH₄)₂S showing the highest conductivity and the UV-S sample the largest barrier to conduction. Transmission Electron Microscope imaging shows an interfacial layer of a few nanometers, where the thicknesses correlate with the electrical responses. Further annealing for 1-2 minutes at 600°C causes the conductivity of sulfur treated samples to dramatically increase to near ohmic behavior; while NH₄OH treated samples remain non-ohmic with only small increase in conductivity. Examination after annealing by TEM shows redistribution of the interfacial layer into fused regions separated by inclusions occurring to a similar level for sulfur and NH₄OH samples. This indicates that improvements to conductivity are not solely related to the fractional area of fused regions, but are strongly determined by the degree of electronic passivation. By measuring the temperature dependence of the current-voltage of the sulfur and NH₄OH samples, it is found that the sulfur at the interface lowers the interface potential barrier between GaAs layers by 0.2 eV. This barrier height reduction highlights the importance of incorporating passivation methods along with oxide removal steps into III-V wafer bonding techniques as a means of increasing the interface conductivity without having to subject samples to extended times at high temperature. Further study into the role of sulfur on III-V surfaces and interfaces will aid in developing a low-cost efficient procedure for materials integration for devices such as lattice mismatched multijunction solar cells.

11:20 AM Student

LL9, Comprehensive Investigation of Ge-Si Bonded Interfaces Using Surface Activation: *Ki Yeol Byun*¹; Isabelle Ferain¹; Brenda Long¹; Susan Holl²; Cindy Colinge¹; ¹Tyndall National Institute; ²California State University

Germanium (Ge) has been considered as a promising candidate to overcome the limitation of silicon (Si) for next generation CMOS devices and optoelectronics due to higher mobility and smaller absorption coefficient. Epitaxial crystal growth is a well-known method for integration of heterostructures between dissimilar materials. However, conventional epitaxial Ge growth on Si requires careful processing and device design to minimize the impact of the dislocations caused by the lattice mismatch and large thermal expansion coefficient difference between Ge and Si. Low temperature wafer bonding is a simple and easy alternative method for forming heterostructures without these limitations. In this work, our chemical and structural investigations of bonded interface show that successful low temperature Ge-Si hetero integration can be achieved utilizing wafer bonding. In the experiment, 4-inch <100> oriented p-type Ge (Ga doped, resistivity = 0.016 Ω.cm) were selected for bonding. Prior to bonding, the Ge and Si wafers were cleaned in an SC1-equivalent solution with ozone for Si and without ozone for Ge. Wafers were then loaded into bonder and vacuum was applied. The wafers were then exposed for 10 minutes to either oxygen or nitrogen free radicals (chamber pressure was 1 mbar at 100 W) generated by a remote plasma ring. After exposure the wafers were bonded in-situ under a pressure of 1kN applied for 5 minutes at a chamber pressure of 10-5 mbar. The wafers were annealed in-situ at 100°C for 1 hour with an applied pressure of 500N in vacuum followed by an ex-situ anneal at 200°C for 24 hours in order to enhance bond strength. The same wafers were then annealed again at 300°C for 24 hours. The ramp-up rate was set to 0.5°C/min in both cases. After anneal Ge-Si bonded pairs remained intact due to a slow ramp-up rate. X-ray Photoelectron Spectroscopy (XPS) data is presented which provides the chemical composition of the Ge surfaces as a function of the hydrophilic bonding reaction at the interface. Additionally, the hetero interfaces were characterized by Atomic Force Microscopy (AFM), High Resolution Transmission Electron Microscopy (HR-TEM), and synchrotron x-ray topography. The reaction product at Ge-Si bonded interfaces has been investigated comprehensively. It is demonstrated that radical exposure prior to bonding can achieve less defective and a lower strained interface by means of a conversion of the bulk Ge to GeO₂. The stable passive film contributes to a reduction of bubbles ("voids") caused by Ge desorption. This conclusion is very useful for high quality hetero-structure integration of thermally mismatched materials such as those used for photonic devices. In particular, we have found that to achieve void-free, strain free Ge-Si interface it is necessary to "passivate" the Ge surface prior to bonding. This is accomplished using oxygen free radical exposure.

11:40 AM

LL10, 3C-Silicon Carbide Epitaxy by Means of Silicon Carbide-on-Silicon Wafer Bonding: *Michael Jennings*¹; Tony Rogers²; Amador Pérez-Tomas³; Nick Aitken²; Peter Ward⁴; Andrea Severino³; Craig Fisher¹; Peter Gammon¹; Philip Mawby¹; ¹University of Warwick; ²Applied Microengineering Limited; ³Centro Nacional de Microelectronica; ⁴PWC; ⁵CNR-IMM

Silicon Carbide (SiC) is widely accepted to be the material of choice for the next generation of power semiconductor devices, due to its superior material properties such as high critical electric field strength, high thermal conductivity and low intrinsic carrier concentration at room temperature. Although Cree inc. have recently commercialised a SiC power MOSFET, there are still key technological drawbacks associated with this device that are hampering its widespread uptake. The cubic form of SiC has many advantageous properties that should allow an increased MOSFET channel mobility and simplified processing with respect to its 4H-SiC counterpart. In this paper, we present a novel wafer bonding technique in an attempt to overcome the wafer bowing problem of 3C-SiC growth on silicon (Si). This involves the fabrication of wafer bonded polycrystalline SiC wafers onto crystalline Si <111> wafers. Wafer bonding was performed on polycrystalline 4⁺ SiC (poly-SiC) carriers supplied by PocoGraphite. The fabrication of the SiC carrier wafers is based on utilising graphite as a precursor. The wafer is then machined from this graphite

material, purified and subjected to a proprietary process that converts the graphite to high purity polycrystalline SiC. In order to achieve an acceptable bond, the poly-SiC carrier wafers were polished at NovaSiC. This is the first time a polishing process has been attempted on such polycrystalline SiC carrier wafers. It is presumed that for high quality wafer bonding to be successful, a root mean square (rms) roughness of less than 0.5 nm is required. Due to the novel nature of the poly-SiC carrier wafer polishing process, this proved to be difficult. Atomic force microscopy (AFM), total thickness variation (TTV) and bearing area ratio calculations were performed by Applied Microengineering Limited (AML). Here we consider the two smoothest poly-SiC carrier wafers, coined poly-SiC wafers 1 and 2. Poly-SiC carrier wafers 1 and 2 revealed rms roughness values of 3.96 and 8.24 nm respectively. A typical Si wafer rms roughness was ~0.3 nm. The total thickness variation (TTV) for both wafers was in the range of 60-80 μm. The predicted Abbott-Firestone curve based primarily on the rms roughness of the wafers to be bonded was calculated. Bearing ratios of 0.3% and 0.05% at a depth of 1.4 nm were calculated for wafers 1 and 2 respectively. The process for bonding the Si to poly-SiC carrier was as follows; firstly the wafers were subjected to a SC1 (NH₄OH : H₂O₂ : DI water) chemical clean followed by an in-situ plasma clean in an oxygen ambient for the purpose of activating the bonds. Secondly the wafers were mechanically bonded at room temperature and thirdly, the bonded wafers were annealed at 500 °C for sufficient bond strengthening to occur.

Session MM:

Semiconductor Processing: Oxidation, Passivation, Etching and Contacts

Friday AM
June 24, 2011

Room: Santa Barbara Harbor
Location: Univ. of California-Santa Barbara

Session Chairs: Douglas Hall, University of Notre Dame; Thomas Jackson, Pennsylvania State University

8:20 AM Student

MM1, Surface Preparation of GaP for Regrowth on Epitaxially-Inverted Structures on Silicon: *Angie Lin*¹; Martin Fejer¹; James Harris¹; ¹Stanford University

GaP and its ternary relatives such as AlGaP and InGaP, are commonly used in devices ranging from LEDs to solar cells. The development of these materials for nonlinear optical devices, however, is more recent. Growth and processing of GaP need to be specifically tailored for orientation-patterning, which is a process by which one can control the two crystallographic orientations of a polar, III-V material on a nonpolar, Si substrate. This technique involves growth by molecular beam epitaxy (MBE), lithography and etching, and regrowth. For epitaxial regrowth, the GaP surface after etching and photoresist removal is extremely important. In this study, we investigated the surface preparation of GaP for MBE regrowth by AFM to study surface morphology, XPS to detect the presence of remaining oxide or contaminants on the surface, and cross-section TEM to study the film regrowth quality. 200-nm GaP films on GaP substrates were used. By using standard films for these studies, we could isolate any processing and regrowth issues to these steps, rather than problems related to GaP on Si growth. The samples underwent various times of surface cleaning by O₂ plasma etching: 0, 1, 5, and 10 min. AFM images before and after O₂ cleaning revealed smooth surfaces with rms roughness values of ~0.2 nm. The XPS scans before and after the surface cleaning steps revealed several differences in the oxide created by the O₂ plasma clean and native oxide including different ratios of the P2p and O1s peak areas and a 1-eV chemical shift in the Ga3d peak. Regrowth on a 30-sec plasma-cleaned sample resulted in areas of poor crystalline quality as seen by cross-section TEM. This is likely due to residual plasma-induced oxide that could not be completely thermally desorbed in the MBE chamber. The need for an additional surface cleaning step prior to regrowth was necessary to ensure that the plasma-induced oxide was fully removed and replaced by the native oxide to protect the surface yet

could be thermally desorbed under UHV. O₂ plasma-cleaned samples were etched with either dilute hydrofluoric acid (HF) or hydrochloric acid (HCl). A rough surface resulting from the HF etch and smooth surface from the HCl etch was seen by AFM, yet no difference between the surfaces was detected by XPS. GaP and GaP/Si samples were processed and prepared for regrowth by a 1-min O₂ plasma clean and HCl etching, then regrown by MBE. Cross-section TEM will be presented to show the regrowth quality. Using a combination of AFM, XPS, and TEM, surface preparation steps were optimized to ensure high-quality regrowth by MBE.

8:40 AM Student

MM2, Oxide Surface Passivation of Ge for Optoelectronic Applications: William O'Brien¹; Bin Wu¹; Chad Stephenson¹; Christina Arisio¹; Marya Lieberman¹; Mark Wistey¹; ¹University of Notre Dame

Ge has made an impact on electronic applications. However, surface passivation is still a critical element in realizing high performance devices. Though a range of passivation techniques have proven adequate for electronics applications, optical applications can be more demanding. Here, we investigate thermal oxidation because it is a relatively simple, low temperature process that has been reported to yield interfacial trap densities in the range of $1\text{E}11\text{ eV}^{-1}\text{cm}^{-2}$. We report a simple surface passivation technique via dry thermal oxidation that is shown to improve the radiative recombination efficiency in Ge, as determined by relative photoluminescence (PL) intensity. For this study, undoped Ge wafers were cleaned by solvents and stripped of native oxide using a dilute HF-based solution to realize a bare Ge surface. Samples were then oxidized in a tube furnace at 500°C for one hour in an O₂ ambient. To test this passivation technique on processed surfaces, a different set of samples was intentionally damaged by reactive ion etching (RIE) before oxidation. X-ray photoelectron spectroscopy (XPS) was used to confirm the Ge oxide. PL was performed on all samples. Oxidizing an as-received sample resulted in 50% higher peak emission. The improvement in PL suggests a strong reduction in nonradiative recombination. We infer that thermal oxidation produced a higher quality oxide interface, with fewer dangling bonds than native oxide interfaces formed in ambient air. RIE reduced PL intensity to about 40% of the as-received intensity, indicating significant surface damage and formation of recombination sites. These samples were then oxidized, which increased peak PL intensity by 4.5x, equal to or higher than bare oxidized wafers. Although we expected RIE samples to be permanently degraded, several etched wafers had even higher PL after oxidation than the corresponding bare, thermally oxidized wafers. We suspect this may be due to two effects, arising from surface roughening. Either transmission of the 534 nm pump beam into the sample was increased by a graded effective index, or facets of the roughened surface enabled multiple reflections, increasing total absorption. Finally, this low temperature thermal process is post-diffusion CMOS compatible, which satisfies a major prerequisite for materials integration on Si. Thermal oxidation thus appears to be a successful technique to repair highly defective surfaces, observed from improvements in RIE-damaged Ge.

9:00 AM Student

MM3, Oxygen-Enhanced Wet Thermal Oxidation of In_{0.53}Ga_{0.47}As: Christopher Seibert¹; Jinyang Li¹; Wangqing Yuan¹; Douglas Hall¹; ¹University of Notre Dame

The recent discovery of oxygen-enhanced wet thermal oxidation has allowed for the oxidation of various low aluminum content and aluminum-free compound semiconductor alloys that are traditionally difficult to thermally oxidize, including those latticed matched to InP, which are of great importance for telecommunications and other applications. In this work we show that it is possible to form thick insulating oxides on InGaAs layers latticed matched to InP by adding trace amounts (<1%) of oxygen relative to the traditional nitrogen carrier gas used in wet oxidation. Oxidations at various relative oxygen/nitrogen ratios up to 0.7% show that at process temperatures below 500°C the oxidation rate of In_{0.53}Ga_{0.47}As saturates between 0.3 and 0.5% O₂/N₂. This is due to the balance of the thermodynamically favorable oxidation reaction involving dry O₂, which forms a dense As oxide, and the removal of volatile As from the oxide by the H₂ byproduct of the less thermodynamically

favorable wet oxidation reaction. At higher process temperatures, above 500°C, this saturation in the growth rate with increasing oxygen content is not seen up to 0.7%, which is likely due to increased As dissociation at higher temperatures reducing the need for the As removal reactions critical at lower temperatures. For all temperatures studied the oxidation reaction is linear, 34 nm/hr and 120 nm/hr for 475°C and 510°C respectively, after an initial time delay before oxide growth. Without added O₂ there is no measurable oxide growth. AFM measurements of the oxide surface reveal a decrease in the RMS roughness of the oxide surface from 2.97 nm (475°C) to 2.14 nm (525°C) as the temperature was increased. To increase the growth rate and overall uniformity of the oxide an unpolished silicon cover piece in direct contact with the surface to be oxidized was used. This cover piece provides an overpressure of the volatile species during oxidation in the small volume between the sample surface and the cover piece, greatly increasing the uniformity of the oxide (determined via visual inspection) and growth rate. A sample which had only half its surface covered during oxidation was considerably more uniform, with a 2 order of magnitude lower leakage current in the portion covered during oxidation. This is due in part to the increased thickness (350 nm vs. 210 nm), a direct result of the increased oxidation rate caused by the cover piece. While these oxides are not of sufficient quality for use as a gate oxide in field effect devices, they do show promise for use in isolating and passivating devices. A 350 nm oxide reduces the leakage current density beneath a Au:Ti contact by 4.6 orders of magnitude (to $<2 \times 10^{-2}\text{ A/cm}^2$ at a bias of 1 V) relative to directly metalized InGaAs.

9:20 AM Student

MM4, Wet Etching Technique for Fabrication of GaSb Based Mid Infrared Single Lateral Mode Lasers: Seungyong Jung¹; Sergey Suchalkin²; Leon Shterengas¹; Gela Kipshidze¹; Gregory Belenky¹; ¹Stony Brook University; ²Power Photonics Corporation

GaSb based mid infrared (IR) light sources and detectors are in high interests due to applications including gas sensing, medical diagnosis, and infrared imaging. Etching is a necessary step in the fabrication procedure of single lateral mode ridge lasers, LED arrays, and detectors. Most of the narrow ridges for laser structures have been formed using dry etching since it can provide precise control of etching depth and the mesa wall steepness. Simplicity of the implementation and low cost are among the advantages of the wet etching. One of the main problems of a wet etching technique is precise control over the etching depth and mesa width, the parameters which are crucial for fabrication of single lateral mode ridge lasers. Fabrication of narrow mesas using wet etching is especially difficult due to the etching undercut and material selectivity of most of the etching solutions. We suggest a wet etching procedure based on two etching solutions with complementary selectivity. Hydrochloric acid (HCl) based solution works well on aluminum containing layers, while sodium hydrogen-tartrate based etchant etches faster the materials without aluminum. Introducing an AlInGaAsSb etch-stopping layer with reduced Al content into the Al-rich cladding layer of the laser structure makes possible to control the etching depth with high accuracy. The ridge lasers were fabricated from GaSb-based type-I quantum well laser structure emitting near 2 μm. For this wavelength, the laser mesa width less than 8 μm is required to ensure single lateral mode operation. The 50 nm thick AlInGaAsSb etch-stopping layer was placed 200 nm over the waveguide. Tartrate etchant was applied to remove the GaSb cap and part of the upper cladding layer. HCl etchant was subsequently used to control the width of the ridge. The 6-μm wide ridge laser with nearly vertical sidewall was obtained using the above etching technique. The laser generated the continuous wave power of 67 mW at 20°C and the threshold current density was 416A/cm² (50 mA). Full width at half maximum of slow axis angle distribution was 10 degrees, which exhibited diffraction limited output beam.

9:40 AM Student

MM5, Fabrication of GaAs Micromechanical Resonator Arrays for Single Molecule Detection: *Andrew Hollowell*¹; Christopher Hains¹; Vakhtang Putkaradze²; Mario Marconi²; Larry Dawson¹; Ganesh Balakrishnan¹; ¹University of New Mexico; ²Colorado State University

Arrayed micro and nano-scale cantilevers in crystalline materials give rise to a new technology of highly sensitive, field-deployable, and cost-effective detectors capable of single molecule/atom recognition. This new technology detects changes in the dynamics and collective oscillation behaviors of micro-cantilever arrays (or nano-pillars) defined as Inherent Localized Modes (ILMs). This novel technique is developed for the intent of early detection and counter-measure of warfare agents used in Weapons Mass Destruction (WMD). ILMs are coherent oscillations set in stable and localized patterns in an array of nanometer size pillars. If one oscillation from a pillar is different from others due to a variation in mass, caused from a defect or the presence of a molecule attached to it, coherence of the resonator is affected and extreme changes in the ILMs pattern are induced, leading to the detection of a molecule. A process is described for the fabrication, and imaging using extreme ultraviolet (EUV) holography, of micromechanical resonator arrays with submicron GaAs, InP, and GaSb cantilevers constructed from epilayers grown using molecular beam epitaxy (MBE). To construct extremely thin arrays of InP, GaAs, and GaSb cantilevers, MBE is used to grow stacks of epilayers on GaAs substrates. Aluminum-rich epilayers are used as etch stop layers between the GaAs substrate and the cantilever material. The rectangular dimensions (length and width) of the cantilevers are defined using photolithography techniques while the material growth is used to define the lateral thickness of the cantilevers. Uniformity of the cantilevers is crucial as variations in dimensions will affect the ILMs. An etch study is performed and characterized with various cantilever dimensions as well as different dry and wet etch process in order to develop a process for the fabrication of uniform pillars with straight and consistent side wall profiles. Material characteristics such as resonant frequencies, quality factors, spring constants and young's modulus are analyzed in order to accurately analyze the ILM behaviors. The ILMs make use of a "defect or anchor-pillars" with different dimensions introduced periodically to achieve more sensitive mass detection. Two different methods of fabricating such inherent "defects" into the cantilevers are performed through variations in the lithography mask as well as utilization of a focused ion beam (FIB) to change the mass and dimensions of the pillars. The fabrication of InP, GaAs, and GaSb arrayed cantilevers are described in detail through use of photolithography, thin film metal deposition, Cl₂ reactive ion etching, and selective wet etch processes. The implementation of EUV holography for real time, simultaneous imaging of the resonators is also described in order to explain the experimental visualization of the collective ILM dynamics.

10:00 AM Break

10:20 AM Student

MM6, Hydrogenated Amorphous Silicon-Carbon Alloy Thin Films for Uncooled Microbolometers: *Hang-Beum Shin*¹; David John¹; MyungYoon Lee¹; Nikolas Podraza¹; Thomas Jackson¹; ¹The Penn State University

The majority of commercially produced uncooled infrared microbolometer imagers use either vanadium oxide or hydrogenated amorphous silicon (a-Si:H) as the infrared sensing material. Undoped a-Si:H has relatively high temperature coefficient of resistance (TCR), a desirable quality for infrared sensing microbolometer devices.[1] Unfortunately, the high TCR is accompanied by high material resistivity which makes undoped a-Si:H unsuitable for device integration. Doping reduces a-Si:H resistivity, but also results in lower activation energy.[2] Recently, high TCR in moderate resistivity materials have been reported including a TCR of -5.2 %/K for 400 Ω-cm a-Si_xGe_{1-x}:H prepared by low frequency plasma enhanced chemical vapor deposition (PECVD) and TCR values of -2.7 %/K and -4.86 %/K at resistivity of 100 Ω-cm and 245 Ω-cm from magnetron sputtered silicon germanium oxide (SiGe_xO_y) [3]. In this work, amorphous silicon carbon alloy (a-Si_{1-x}C_x:H) films were deposited by PECVD monitored by real time spectroscopic ellipsometry (RTSE). RTSE is used to quantify film thicknesses and detect changes in the complex dielectric

function spectra ($\epsilon = \epsilon_1 + i\epsilon_2$) over a spectral range from 1.5 to 4.2 eV. The RTSE tracks changes in material arising from deposition parameter variations or changes in the film microstructure, for example nucleation and evolution of microcrystallites in the amorphous matrix, as a function of deposition time. Titanium top contacts are used to measure film resistivity using a transmission line method, and TCR is measured from room temperature to 55°C. 1/f noise is measured using resistors with varying sample volume and with varying bias current to extract the normalized Hooge parameter (normalized by carrier concentration). Resistivity, TCR, and 1/f noise were investigated for a-Si_{1-x}C_x:H films prepared under a variety of deposition conditions including hydrogen dilution $R = [H_2] / \{[SiH_4] + [CH_4]\}$, to control the relative degree of order and crystallinity in the material, doping concentration $D = [PH_3] / \{[SiH_4] + [CH_4]\}$, to control resistivity, and carbon incorporation $C = [CH_4] / \{[SiH_4] + [CH_4]\}$. Adding carbon to a-Si:H increases the material optical bandgap and suppresses the formation of microcrystallites for hydrogen-diluted film growth. Adding carbon to a-Si:H result in films with TCR near -3%/K for resistivity near 1500 Ω-cm and reduced noise compared to films without carbon. Research was sponsored by the U.S. Army Research Office and U.S. Army Research Laboratory under Cooperative Agreement Number W911NF-0-2-0026.

10:40 AM

MM7, Metal and Semiconductor Contacts (Si, V, Au) to Organic Molecules: The Fullerene Model System: *Harmonie Sahalov*¹; *Hui Liu*¹; *Petra Reinke*¹; ¹University of Virginia

Thin films made from organic molecules are currently used in organic photovoltaics, molecular electronics and organic light emitting diodes (OLED). An important part of their functionality is determined by the local interaction with the contact material. This includes the electronic interaction in terms of charge transfer and band bending, and the geometric distribution of the contact material within the organic layer. We present here an extensive study of the interaction of Si, Au, and V with the surface and bulk of ultrathin C60 layers. The fullerenes are used in organic photovoltaics as acceptor materials, and are a highly reproducible model system. These materials systems are studied with scanning tunneling microscopy (STM) and photoelectron spectroscopy (PES) of the core level and valence band. All experiments were performed under ultrahigh vacuum conditions, and with sequential deposition of the material. The C60 layer consists of large hexagonal islands, and inter-molecular grooves and interstices provide an environment with higher coordination number. The Si deposition and evolution of cluster size and bonding state was observed with PES. Bonding to C60 molecules is preferred for Si clusters with 5 or fewer atoms and this drives the filling of the high coordination sites on the surface. The Si-clusters merge and form an a-Si overlayer. The valence band-offset is about 1.2 eV, and band bending is limited to the fullerene layer. The interaction of the C60 surface with Au shows the formation of metal clusters on the surface, which coexist with an inventory of highly mobile Au-atoms within the surface grooves likely stabilized by the interaction with the fullerene matrix. In contrast to Si, ultrasmall clusters are not observed. A charge transfer occurs from the Au-clusters to the fullerene, and shifts EF into the LUMO states of C60. If C60 and Au are co-deposited the fullerenes will arrange around Au-clusters in a self-assembly process. The behavior of V, however, is quite different: while Si and Au interact predominantly with the C60 surface, V ad-atoms diffuse rapidly into the fullerene layer. The electronic interaction of the sub-surface V-inventory modifies the surrounding C60 matrix. The modulation of the local electronic structure is clearly seen in the STM images, and will be discussed in detail in my presentation. None of these elements reacts chemically with the fullerene molecules at room temperature, and SiC is formed around 500° C, while V-carbide formation begins around 250° C. The considerable differences we observed in this fundamental study on the interaction of C60 surfaces with different elements will impact the design of contacts especially for ultrathin molecular films and complex electrode geometries. This research was supported by start-up funding from the University of Virginia, and NSF-DMR-1005809.

11:00 AM Student

MM8, Silicide/Silicon/Silicide Heterostructures with Ultra-Thin Silicon Gap and Realization of FET Device: *Wei Tang*¹; Shadi Dayeh²; Tom Picraux²; King-Ning Tu¹; ¹UCLA; ²Los Alamos National Lab

The in-situ transmission electron microscopy (TEM) observation of solid-state reactions and direct correlation with transport behavior in semiconductors is a unique tool for uncovering the evolution of detailed material-device inter-relations and for engineering materials and/or devices for optimum performances. This is uniquely fitted for one-dimensional nanostructures where no sample cleaving or damage is required for the experiment allowing simultaneous TEM and multiple transport experiments. We present here an experimental investigation and discussion for controlled formation of nanometer-scaled Si gaps within Si nanowires (NWs) grown in different crystallographic orientations, and the fabrication and characterization of sub-100 nm (down to several nanometers is possible) Si NW field-effect transistors (FETs) with excellent transport properties, and subsequently introduce new techniques for further optimizing their performances. Our platform consists of a 50 nm nitride membrane suspended over an window in a TEM-compatible Si sample. Vapor-Liquid-Solid (VLS) grown Si NWs are transferred to the nitride membranes from solution and photolithography is used to define Ni electrodes to the Si NWs. The metal-Si reaction forms inward into the channel in a process that is precisely controlled on an in-situ TEM hot stage. The reactions are generally formed at 400 °C resulting in Ni₂Si silicide. Our experiments show that the silicidation path is preferred over (111) planes. [211] oriented NWs have three {111} slanted planes with respect to the NW growth axis sometimes resulting with a rough silicide-Si interface. This is detrimental for FETs where source-drain fields are maximized at the rough edges of the interface leading to short-channel effects. Spreading of the silicidation reaction on the (111) plane perpendicular to the growth axis of [111] Si NWs results in a smooth silicide-Si interface, which is better controlled and well suited for deeply scaled Si NW FETs. The Ni₂Si-Si interface provides a hole barrier height of ~ 0.37-0.4 eV for holes. For low doping densities in Si NWs (n or p) or undoped wires, the transport is dominated by thermo-ionic emission over the hole barrier leading to higher transconductances at negative gate voltages. Therefore, our NW FETs show ~ 106 Ion/Ioff ratios at VSD=1V and in the negative gate voltage quadrant. Positive gate voltages result in a smaller current transport over the higher electron barrier.

11:20 AM

MM9, Improved Electrical Properties of N-Contacts to N-face GaN for Vertical Light-Emitting Diodes by Laser-Annealing: Joon Woo Jeon¹; Sang Youl Lee²; June-O Song²; *Tae-Yeon Seong*¹; ¹Korea University; ²LG Innotek

High-power GaN-based vertical light-emitting diodes (VLEDs) are considerably important for solid state lighting application. One of the main barriers to the realization of solid-state light is the formation of high-quality ohmic contacts having low-resistance and excellent reliability. For conventional lateral LEDs, n-type ohmic contacts are easily formed on Ga-face n-GaN using either Ti- or V-based schemes. However, for n-type side-up VLEDs (where the n-GaN has N-polarity), n-type ohmic contacts were shown to be difficult to form. For example, when Ti/Al contacts to n-GaN were annealed at temperatures exceeding 500°C, Ga-face n-type contact showed ohmic behaviours with a contact resistivity of ~10⁻⁵ Ωcm². However, N-face n-contacts produced non-ohmic behaviours. Furthermore, Ti/Al contacts to N-face n-GaN thin films prepared by a laser lift-off process yielded significantly degraded electrical properties when annealed at temperatures above 300°C. The degradation was attributed to the absence of polarization-induced two-dimensional electron gas caused by the formation of interfacial AlN on p-GaN. In particular, unlike lateral LEDs, the fabrication of vertical LED structures requires relatively low processing temperatures not to damage host substrates formed by wafer bonding or electroplating. Thus, in this work, in order to develop high-quality n-contacts to N-face n-GaN for high-performance vertical LEDs by avoiding damaging the host substrates, we introduced a laser-annealing process. Ti/Al/Pt contacts were first laser-annealed at 400 – 600 mJ/cm² in air by means of KrF excimer laser (248nm) prior to rapid-thermal annealing at 250°C. The electrical properties of the Ti/Al/Pt contacts to N-face n-type GaN were investigated. It is

shown that all the Ti/Al/Pt contacts exhibit ohmic behaviors before annealing. Unlike the contacts without laser annealing, the laser-treated samples produce ohmic behavior after annealing at 250°C for 1 – 2 min. It is further shown that the laser-treated samples give almost constant total resistance although annealed at 300°C for 60 min in an oven. However, the untreated samples become gradually degraded with increasing annealing time. To understand the ohmic formation mechanisms, X-ray photoemission spectroscopy examination were performed on the samples before and after laser-annealing. For untreated samples, the Ga 2p core level shifts toward the lower binding energy side upon annealing at 250°C. For the laser-annealed samples followed by rapid-thermal annealing at 250°C, however, the Ga 2p core level remains almost unchanged after annealing. Furthermore, measurements showed that the normalized N/Ga atomic ratios are 1.04± 0.02 and 1.00± 0.01 for the samples without and with laser annealing, respectively. Based on the x-ray photoemission spectroscopy, Auger electron spectroscopy, and TEM results, the laser-annealing effect on the electrical characteristics of n-contacts to N-face n-type GaN layers are described and discussed.

11:40 AM Student

MM10, Resistance and Transparency Study of Contacts to p-Type GaN: *Wenting Hou*¹; Christoph Stark¹; Theeradetch Detchprohm¹; Christian Wetzel¹; ¹Rensselaer Polytechnic Institute

Low-resistance Ohmic contacts critically contribute to the energy efficiency of III-nitride-based light emitting diodes (LEDs). In particular, the challenge of identifying a low-resistance contact to p-GaN is compounded by the high variability of high Mg doping in GaN. For planar injection LEDs the ideal p-contact would also need to be highly transparent. While, contact resistance and current spreading are known to improve with increasing thickness of the metal stack, the transmittance decreases. Here we analyze Ni/ITO, NiZn/ITO, AgCu/ITO, Ag/ITO, and Cr/ITO in comparison with the bare Ni/Au and ITO contacts to p-GaN. Semi-transparent Ni/Au contacts have commonly been used on p-type GaN. We here employ 5nm of Ni and 5nm of Au as deposited by an e-beam evaporator and followed by rapid thermal anneal in oxygen ambient at 500°C for 1 minute. With this anneal, the specific resistance reduces from 1×10⁻²Ω·cm² to 4×10⁻³Ω·cm². The voltage range of Ohmic behavior however is very limited. With the anneal, the transmittance of Ni/Au on glass at a wavelength of 500nm increases from 40% to 75%. An improvement in Ohmic behavior and contact resistance can be achieved with NiZn/Ag contacts. We achieve low-resistance Ohmic contacts with 5nm/200nm NiZn/Ag after anneal in oxygen ambient at 550°C for 1 minute. The specific contact resistance reduces from 2×10⁻²Ω·cm² to 8×10⁻⁴Ω·cm² with annealing. The contact is non-transparent, limiting its application to vertical LED structures. In an attempt to increase transparency the layer thickness was reduced, resulting, however, in much higher contact resistance. Indium-tin-oxide is a well known transparent conducting film that has widely been employed as contact to p-GaN. We find that a 200nm ITO film can achieve very high transparency after annealing in oxygen ambient at 550°C for 1 minute. For ITO on glass, we find a transmittance above 80% across the whole visible spectrum. However, with annealing the contact resistance only reduces from 1×10⁻¹Ω·cm² to 2×10⁻²Ω·cm². These results are worse than for the Ni/Au contact. A compromise between low contact resistance and high transmittance has been reported by the combination of metal-ITO contacts. For 3nm Ni and 130nm ITO on glass annealed in oxygen ambient at 550°C for 1 minute, we achieve over 95% transmittance at 520nm. By adjusting the thickness of ITO, we improve the transmittance to over 95% at the desired wavelength. With this insertion of a thin metal layer before the ITO, the contact resistance is significantly reduced, without any apparent problems in current spreading or losses of transmittance. Several metal-ITO schemes show a better Ohmic behavior than Ni/Au. This work was supported by a DOE/NETL Solid-State Lighting Contract of Directed Research under DE-EE0000627. This work was also supported by the National Science Foundation (NSF) Smart Lighting Engineering Research Center (#EEC-0812056).

Session NN:

Molecular Electronics / Sensor / Ionic Conductors

Friday AM
June 24, 2011

Room: State Street
Location: Univ. of California-Santa Barbara

Session Chairs: David Janes, Purdue University; Theresa Mayer, Pennsylvania State University

8:20 AM Student

NN1, Au-Molecule-GaAs Devices with Graphene Barrier Layer: *Patrick Carpenter*¹; Ting-Fung Chung¹; David Janes¹; Yong Chen¹; ¹Purdue University

Molecular electronics has offered many solutions to current semiconductor fabrication issues. The atomic size and versatile functionality of the molecules allow for the fabrication of electric switching devices, high-density memory devices, or chemical/biological sensors. These interesting properties have been realized through the fabrication of molecular devices in metal-molecule-metal (MMM) and metal-molecule-semiconductor (MMS) configurations. While these devices have proven to be interesting test beds for molecular devices, there are still issues associated with top contact metallization of the molecular layer. Electrical characteristics can be greatly affected by evaporated metal, creating metal shorts in the molecular devices or dislodging the molecules from the substrate. A previous study was conducted to determine the most effective metal deposition technique to prevent metal penetration [4]. A low energy, thermal metal deposition method was determined as the most effective method; however there was still indication that there remained a relatively small amount of metal penetration. In this study, a single layer of graphene was inserted between the top metal contact and the molecular layer in a MMS device. The graphene layer was grown by chemical vapor deposition and transferred to the device substrate. Metal-graphene-molecule-GaAs devices were fabricated for spectroscopic analysis and electrical characterization. Fourier transform infrared spectroscopy (FTIR) was used to determine survivability of the molecules from the chemical processing and the top layer metallization. Sharp peaks in the IR spectra, both before and after metallization of the molecule-GaAs samples, indicate that a well ordered monolayer is present. A slight deformation of the molecular layer after metallization is apparent, indicated by shifts and tail broadening of the molecular peaks. Current-voltage (*I-V*) data shows that there is a 10x increase in the conductance of the metal-graphene-GaAs device versus a comparable metal-GaAs device, indicating a change in the electrostatic barrier height due to the addition of the graphene layer. The metal-graphene-molecule-GaAs devices display another order of magnitude increase in conductivity. This increase in conductivity is consistent with prior results for MMS devices fabricated using low-penetration metallization techniques. Based on these results graphene appears to be an effective interlayer for blocking metal penetration in molecular devices.

8:40 AM Student

NN2, Gap Mode Plasmonic Cavity with Coupled Organic Gain Medium: *Shanying Cui*¹; Kasey Russell¹; Evelyn Hu¹; ¹Harvard University

In recent years there has been considerable interest in nanoscale metal devices that take advantage of surface plasmon polaritons (SPPs) and localized surface plasmons to concentrate optical energy to sub-wavelength length scales. Of particular interest for investigations into quantum electrodynamics are metal-based cavities that concentrate optical energy in the vicinity of optical emitters. Although metal losses limit the maximum cavity quality (*Q*) factors attainable in metal-based cavities, the much smaller mode volumes (*V*) achievable in these structures provide a *Q/V* that can be commensurate with those characteristic of dielectric cavities. An important advantage of these metal cavities is the wide choice of optically active layers that may be incorporated into the device. Our group has recently demonstrated a metal-based plasmonic cavity containing coupled colloidal PbS nanocrystal optical emitters that showed strong modification of the nanocrystal luminescence spectrum. In the work described here, a similar plasmonic nanocavity design

is used, consisting of a silver nanowire lying parallel to a silver substrate. In this case, however, the coupled gain medium is a self-assembled monolayer of organic dye in the gap between the nanowire and the substrate. Surface plasmon modes of the nanowire and substrate hybridize across the gap, yielding gap-mode states of long wave-vector confined in the region under the nanowire. The sub-nm roughness of the Ag substrate is formed through a 'template stripping' technique, using metal deposition onto an atomically-smooth Si wafer. The surface of the silver is then covered with a monolayer of bidentate thiol molecules (pentaerythritol tetrakis (3-mercaptopropionate)), which acts as a bifunctionalized linker between the silver substrate and the thiol-reacting organic dye (Alexa Fluor 532 maleimide). The result is a smooth and covalently bound monolayer of the emitter. Cavity fabrication is completed by depositing silver nanowires onto the sample. Fluorescence from dye molecules within the gap couples to the modes of the cavity, resulting in clear modifications of the dye emission spectrum. Polarization measurements indicate that the emission is highly polarized along the axis of the cavity, in agreement with the behavior of nanocrystal-based cavities. The gap size between the silver substrate and the nanowire is an essential variable to understanding the limits of our system. Placing the dye too close to the metal surface quenches its fluorescence, but placing it too far prevents it from coupling its emission into the cavity modes. Organic dyes give us the capability to explore these limits by controlling the gap thicknesses with layer-by-layer growth or by binding it to molecules self-assembled on thickness controlled atomic layer deposition of dielectrics.

9:00 AM

NN3, Conductance Statistics of Molecular Junctions Fabricated with a Large Array of Sub-10 nm Single-Grain Au Nanodots Electrodes: Nicolas Clement¹; Kacem Smaali¹; Gilles Patriarche²; *Dominique Vuillaume*¹; ¹IEMN-CNRS; ²LPN-CNRS

An unexplored gap exists between electronic transport through a single molecule and a large ensemble of molecules. The results cannot be obviously transposed between both types of molecular junctions. Here we show, by using an array of nanometric gold dots as electrodes, that we can easily get statistics on the conductance of thousands of molecular junctions composed of self-assembled monolayers with less than two hundred molecules. We demonstrate the formation of sub-10 nm single-grain Au dots (down to 5-8 nm) with small dispersion in size and perfect alignment by using e-beam lithography process. An annealing process converts dots from amorphous to single crystals. These nanodots are successfully used as electrodes for chemical and electrical characterization of organic self-assembled monolayers (SAMs) made of less than 200 molecules. The structure of these nanodots are revealed by physical measurements, such as atomic force microscope (AFM), atomic resolution scanning transmission electron microscopy (corrected-STEM) and by chemical techniques using energy dispersive x-ray spectroscopy (EDX). These Au nanodots are used for the fabrication of a large number of a metal-molecule-metal (MMM) nano-junctions. We formed SAMs of alkylthiols ($C_nH_{2n+1}-SH$, with $n = 8, 12, 18$) on these nanodots, and we measured current-voltage characteristics by C-AFM. We analyze conductance characteristics statistically over thousands of junctions using only a single C-AFM image, and this approach gives very significant and valuable statistical data on the electronic transport properties of these molecular devices, in a quicker and easier way compared to other approaches. On the amorphous nanodots, we observe two peaks of conductance whatever the chain length. The two peaks are observed at all applied voltages, but the peak separation is reduced at $V > 0.7$ V. The two peaks become closer when the chain length increases. On perfect single crystal nanodots, only a single peak is observed, except for small molecules ($n=8$). By stopping the tip over a nanodot, we recorded the *I-V* curves for representative dots belonging to each conductance peak family. The *I-V* curves are dominated by a tunneling behavior as usually observed in the MMM junctions of alkyl chains. The TVS (transient voltage spectroscopy) analysis shows lower transient voltages (-0.6 V and 0.7 V, e.g. for C_{12}) for the "high" conductance peak than for the "low" conductance peak (-1.2 V and 1.4 V). These results are discussed and related to differences in the molecular organization of the SAMs as function of the chain length and structure of the underlying nanodot. In conclusion, we have demonstrated that these arrays of Au single crystal nanodots are very efficient test-beds for molecular electronics.

9:20 AM Student

NN4, Surface Functionalization of Si Nanowires on SOI Substrates for Biosensing Applications: *Paul Bertani¹; Xuejin Wen¹; Wu Lu¹; ¹The Ohio State University*

Silicon nanowire-type devices have demonstrated great potential for label-free bio-detection with selectivity and high sensitivity. However, these devices, generally functionalized through a silane self-assembly chemistry on an oxide layer, suffer from current drift with time due to ion diffusion into the oxide layer. In this paper, we present a surface functionalization process through a H-terminated Si surface on SOI substrated for detection of DNA hybridization. XPS and fluorescence are used to confirm the presence of molecules and check the surface coverage. A H-passivated surface is used in beginning stages in order to protect surface Si from oxidation. This is done by removing native oxide then using NH₄ to bind hydrogen to dangling Si Bonds. The functionalized silicon nanowires are obtained by creating an amine terminated sequence using a thin layer of t-BOC (10-N-BOC-Amino-dec-1-ene) protected amine. Once the t-BOC is applied the devices are sealed in a nitrogen rich environment and exposed to 254 nm UV light, during which the double carbon bonds break and re-bond with the dangling surface silicon bonds. This is followed by a deprotection step to leave exposed amine groups on the surface. DNA Oligonucleotides modified by a thiol group can then be covalently linked to the exposed amine groups after a cross-linking step using SSMCC (sulfo-succinimidyl 4-(N=maleimidomethyl) cyclohexane-1-carboxylate). The resulting DNA-modified surface has been demonstrated to produce high selectivity for complementary DNA sequences in solution. XPS data is used to verify surface functionalization at five significant stages throughout the modification process. Specifically they are: (1) the bare Si surface with native oxide, (2) hydrogen-terminated surface, (3) protected amine linked to surface (t-BOC), (4) de-protected amine group linked, and (5) the cross-linking SSMCC applied. Specific attention is paid to oxygen (1s), nitrogen (1s), carbon (1s), and silicon (2p) peaks. The results show reasonable levels of nitrogen (1s) on the surface (3%) compared to reference (control) procedure samples (4.3%) during the protected amine phase. After successful functionalization procedures, the DNA hybridization quality is evaluated by fluorescence intensities. Four trials of interest are used for evaluation: (1) background sample for instrumental calibration and reference, (2) probe DNA only, (3) target DNA only, and finally a sample exposed to probe and then target DNA. Probe DNA referring to DNA Oligonucleotides modified by a thiol group linked to the surface and target DNA referring to DNA desired to hybridize with the probe to verify successful detection. Cy5 (green) is used as the fluorescence marker for probe DNA and Cy3 (red) is used for target DNA. Current efforts are being directed to fabricate Si nanowire biosensors using this functionalization approach for detection of DNA and miRNA hybridization.

9:40 AM Student

NN5, Switching Characteristics of Nonvolatile Organic Resistive Memory Devices with Interfacial Oxide Layers Tuned by O₂ Plasma Treatment: *Byungjin Cho¹; Sunghoon Song¹; Yongsung Ji¹; Takhee Lee¹; ¹Gwangju Institute of Science and Technology*

Organic resistive memory, based on the resistance change of organic materials, has attracted a significant attention due to its attractive features such as low-cost processing, printability, and flexibility. Meanwhile, the interface engineering has been considered as one of the essential strategies for obtaining high-performance memory devices. We note that naturally formed native oxides on an Al surface strongly influences the switching characteristics and reproducible switching in organic memory can be realized through an intentional introduction of the additional oxide film. However, there have been few detailed studies on the effects of the interfacial oxide on the switching parameters and performance. We herein demonstrated organic resistive memory devices with interfacial oxide layers, the thickness of which depended on O₂ plasma treatment time. The memory consisted of a composite material of polyimide and [6,6]-phenyl-C61 butyric acid methyl ester (PCBM) sandwiched between Al electrodes in an 8x8 cross-bar array structure. The different interfacial oxide thicknesses sequentially changed the ON and OFF states of the fabricated memory devices. We observed that the memory devices

treated with the additional plasma showed higher ON/OFF ratios than devices without the treatment, which was due to the relatively large OFF resistance values. However, a long oxidation process widened the threshold voltage distribution and degraded the switching reproducibility. It implies that the oxidation process should be carefully optimized with consideration of essential memory parameters.

10:00 AM Break

10:20 AM Student

NN6, Synthesis and Lithium Battery Applications of Nitrogen Doped Graphene Films: *Leela Mohana Reddy Arava¹; Anchal Srevestava¹; Sanketh Gowda¹; Hemtej Gullapalli¹; Madan Dubey²; Pulickel Ajayan¹; ¹Rice University; ²U.S. Army Research Laboratory*

Graphene, due to its superior electrical conductivities than that of graphitic carbon, high surface areas and a broad electrochemical window, has been considered as potential electrode material for Li-ion battery application. Further nitrogen and boron doped graphene structure has got considerable interest in the field of electronics. Reports on synthesis of nitrogen doped graphene is very remote and hence developing a simple method to synthesis N-doped graphene is noteworthy. Like other carbon forms, there is a high possibility to have enhanced Li-battery properties of graphene when it is doped with nitrogen. Hence, it of fundamental interest to investigate how N-doping affects Li interaction properties when compared to its parent graphene. With this motivation, we have prepared graphene and N-doped graphene over large copper foils by liquid phase chemical vapor deposition technique and studied its Li intercalation properties. Continuous single and few layers of graphene and nitrogen doped graphene films were grown on Cu foils by chemical vapor deposition technique using liquid precursor. As-grown nitrogen doped graphene films on the Cu foil were then used for all electrochemical studies. For structural and morphological characterization studies, nitrogen doped graphene films were removed from the Cu foil and transferred to other desired substrates such as SiO₂/Si or ITO substrate. Ranging from single to multiple layered nitrogen doped graphene films were well characterized by Raman spectroscopy, transmission electron microscopy and X-ray photoemission spectroscopy. Nitrogen doped graphene films showed improved reversible Li storage properties when compared to undoped graphene films prepared by similar technique.

10:40 AM Student

NN7, Conformal Coating of Thin Polymer Electrolyte Layer on Nanostructured Electrode Materials for 3D Battery Applications: *Sanketh Gowda¹; Leela Mohana Reddy Arava¹; Pulickel Ajayan¹; ¹Rice University*

Various 3D battery architectures have been proposed to address effective power delivery in micro/nano-scale devices and for increasing the stored energy per electrode footprint area. One step towards obtaining 3D configurations in batteries is the formation of core-shell nanowires that combines electrode and electrolyte materials. One of the major challenges however in creating such architectures has been the coating of conformal thin nanolayers of polymer electrolytes around nanostructured electrodes. Here we show conformal coatings of 25-30 nanometer Polymethylmethacralate (PMMA) electrolyte layers around individual Ni-Sn nanowires used as anodes for Li ion battery. This configuration shows high discharge capacity and excellent capacity retention even at high rates over extended cycling, allowing for scalable increase in areal capacity with electrode thickness. Our results demonstrate conformal nanoscale anode-electrolyte architectures for efficient Li-ion battery system.

11:00 AM Student

NN8, Nanostructured Co₃O₄ Supercapacitors via Solution Precursor Plasma Spray: *Raghavender Tummala¹; Ramesh K. Guduru¹; Pravansu Mohanty¹; ¹Univ of Michigan*

The metal oxide based supercapacitors have attracted enormous attention recently, and especially Co₃O₄ material has the potential of superior electrochemical characteristics with relatively low cost. There have been powder based, sol-gel process, hydrothermal and vapor deposition based

techniques in use to develop Co_3O_4 electrodes. Almost all of these techniques require multi-step procedures and longer processing times to develop the electrodes. Therefore an inexpensive and rapid processing route which is also capable of producing nanostructures is of technological importance. Here, for the first time, we report the synthesis and characterization of Co_3O_4 electrodes developed by a novel liquid precursor plasma spray process that is inexpensive as well as faster compared to the above mentioned techniques. The solution precursor for the spray process was prepared from a mixture of Cobalt Acetate and water. An axial plasma spray system was employed to create nanostructured films of the desired compound. X-ray studies confirmed the phase of porous Co_3O_4 coatings and their microstructural analysis showed fine grain size below 100 nm. The electrochemical performances of these coatings have been evaluated in KOH electrolyte in two electrode and three electrode configurations. Electrochemical specific capacitance of Co_3O_4 coatings along with their electrical characteristics will be reported.

11:20 AM Student

NN9, Performance of MnO_2 Crystallographic Phases in Rechargeable Lithium-Air Oxygen Cathode: Olubukun Oloniyo¹; ¹Newcastle University

The need to reduce dependence on depleting resources for energy generation has drawn attention to lithium air rechargeable cells which has the potential to significantly increase the energy density of current lithium ion rechargeable cells¹. Manganese dioxide (MnO_2) has been shown to be effective for improving the efficiency of cathodes in lithium air cells. The different crystallographic phases (α , β and γ) of MnO_2 nanowires, α nanospheres and α - MnO_2 nanowires on carbon were synthesized using the hydrothermal method. Electrochemical properties of the synthesized catalyst particles were investigated by fabricating cathodes and testing them in a lithium air cell with LiPF_6/PC and $\text{LiTFSi}/\text{TEGDME}$ electrolytes. α - MnO_2 had the highest discharge capacity in the $\text{LiTFSi}/\text{TEGDME}$ electrolyte with 2500 mAh/g while α - $\text{MnO}_2/\text{Carbon}$ in LiPF_6/PC showed a significantly higher discharge capacity of 11,000 mAh/g based on total mass of catalytic. The samples were characterised using different techniques including X-ray diffraction, Scanning electron microscopy (SEM), Transmission electron microscopy (TEM) and Brunauer, Emmett and Teller (BET) surface area measurements. The morphologies of the sample particles were observed by SEM while TEM was used to measure the particle sizes. Powder X-ray diffraction was conducted to confirm the identities of the catalyst while the specific surface area was determined through the BET method. The sample with catalyst based on carbon (MnO_2/C) had the highest capacity of 11,000 mAh/g in LiPF_6/PC electrolyte. The other samples pale in comparison to this and tend to be only around 2500 mAh/g. Using the same catalyst in a different electrolyte ($\text{LiTFSi}/\text{TEGDME}$), β - MnO_2 nanowire was found to be the best catalyst but only at about 2600 mAh/g which is comparable to the least effective catalysts in LiPF_6/PC electrolyte. This difference can only be attributed to the difference in electrolytes since all other factors remained the same. LiPF_6 salt appears to have a higher effect than LiTFSi on discharge capacity as already demonstrated in literature². α - MnO_2/C with the highest discharge capacity of 11,000mAh/g showed the least cycling properties and a sudden upward spike in discharge capacity to 7000 mAh/g on the 5th cycle while the other catalyst types rather maintained good capacity retention on cycling. In the $\text{LiTFSi}/\text{TEGDME}$ electrolyte, β - MnO_2 nanowire catalyst therefore had the highest discharge capacity of about 2800mAh/g and least capacity retention. The α - MnO_2 however maintained the best capacity retention for 15 cycles although at poor discharge capacities. Optimising the air cathode as shown is imperative for influencing the performance of lithium air rechargeable cell. ¹K.M. Abraham, Z.J. Jiang, Electrochemical Society 143 (1), 1 (1996); ²M.Minakshi, S.Thurgate, Surf. Interface Anal. 2009, 41, 56-60.

11:40 AM

NN10, Investigation on Activated Charcoal-Carbon Fabrics Composite Electrode Materials for Supercapacitor Application: Amrita Jain¹; Ashish Gupta¹; Manju Mishra²; S.K. Tripathi¹; ¹Jaypee University of Engineering and Technology; ²Viva Institute of Technology,

Composite electrodes comprising of activated charcoal and carbon fabrics were prepared and used as electrode materials for supercapacitor applications

in combination with PMMA-EC-PC- NaClO_4 based polymeric gel electrolytes. Supercapacitor cells were characterized using a.c. impedance spectroscopy, linear sweep cyclic voltammetry and galvanostatic charge-discharge tests. Overall capacitance of the capacitor cells have been observed to be in the range of 260 mF/cm² which is equivalent to the single electrode specific capacitance of 127 F/gm. These values corresponds to the energy density of 18 Wh/kg and power density of 0.1 kW/kg. Capacitance of the capacitor cell has been observed to be quite stable for about 5000 cycles and even more.

Index

A		
Adachi, H	35	
Adhyaksa, G	74	
Agarwal, A	40, 41	
Agrawal, A	63	
Ahirwar, P	28, 64, 88, 89	
Ahiwar, P	64	
Ahn, B	108	
Aidam, R	34	
Aifer, E	23	
Aitken, N	118	
Ajayan, P	123	
Akahane, K	88	
Akinaga, H	86	
Akyol, F	53	
Alam, M	114	
Alberi, K	50	
Albrecht, A	28, 64	
Alexandrov, D	20	
Alfaro-Mantinez, A	64	
Alford, T	26	
Ali, A	63	
Alimardani, N	80	
Allerman, A	45, 47, 81	
Ambacher, O	34	
Anderson, T	91	
Anderson, W	105	
Ante, F	97	
Anthony, J	99	
Araki, T	108	
Arava, L	123	
Arehart, A	31, 53, 82	
Arenholz, E	95	
Arisio, C	119	
Armstrong, A	45, 46, 81	
Asbeck, P	31, 63	
Atwater, H	29, 30	
Avrutin, V	102	
Awschalom, D	94	
Azhar, E	67, 112	
B		
Bakalova, S	42	
Baker, D	73	
Balakrishnan, G	28, 61, 63, 64, 88, 89, 120	
Balandin, A	92	
Balasubramanian, V	38	
Balaz, S	103	
Balci, S	105	
Bandaru, P	22, 71	
Banerjee, A	54	
Bank, S	84, 85, 89, 100	
Barquinha, P	56	
Baughman, W	105	
Bayraktaroglu, A	108	
Bayraktaroglu, B	56	
Bazan, G	73	
Beam, E	59	
Becker, J	89	
Belenky, G	62, 71, 119	
Bello, I	52, 114	
Bennett, B	63	
Berry, J	103	
Bertani, P	123	
Bertness, K	32, 38, 65, 66	
Bertram, F	102	
Beyer, A	109	
Bezares, F	91	
Bharatan, S	70	
Bhaskar, U	24	
Bhat, I	111	
Bhatia, A	70	
Bhattacharya, P	54, 108	
Billingsley, D	60	
Bimberg, D	89	
Blanchard, P	32, 38	
Blochwitz-Nimoth, J	97	
Bo, L	51	
Boettcher, J	30	
Bolen, M	67	
Boles, S	113	
Bommena, R	36	
Boos, B	63	
Borghetti, J	55	
Borisova, S	82	
Bornstein, J	50	
Bosco, J	29	
Bowers, J	35, 37, 109, 110	
Branz, H	50	
Breitenstein, O	56	
Brenner, T	73	
Brewer, J	105	
Brill, G	86	
Brillson, L	103, 104	
Brivio, J	43	
Brongersma, M	24	
Brown, A	20, 107, 110	
Brown, D	33, 58, 60	
Browne, D	108	
Brown, L	97	
Brückner, P	34	
Brunner, F	77	
Bruno, G	107	
Bryant, B	76	
Buehl, T	35, 49, 65, 89	
Burek, G	78, 79	
Burghard, M	30	
Burghartz, J	97	
Burk, A	40	
Burke, P	21, 35	
Burkhardt, M	98	
Burmistrova, P	36	
Butcher, K	20	
Butler, L	105	
Byrappa, S	42	
Byun, K	117, 118	
C		
Caldwell, J	40, 91	
Calizo, I	45	
Campbell, J	54	
Campbell, P	43	
Cantoni, C	50	
Canzler, T	97	
Cao, Y	59, 73	
Capano, M	67	
Capasso, F	101	
Carnevale, S	65	
Carpenter, P	37, 122	
Carter, A	58, 78, 79	
Cassels, L	35, 36	
Cavalero, R	44, 67, 91	
Chabinyc, M	98	
Chakrabarti, S	90	
Chandrashekhar, M	42, 68, 69, 90, 92, 93	
Chandy, J	28	
Chang, C	32	
Chang, W	25	
Chauveau, J	52	
Chen, D	113	
Chen, G	81	
Cheng, G	45	
Cheng, L	41	
Chen, H	42	
Chen, J	94	
Chen, R	85	
Chen, W	26, 115	
Chen, Y	39, 73, 86, 122	
Chen, Z	102	
Cherkashin, N	116	
Cheun, H	57	
Chi, C	29	
Chidsey, C	73	
Cho, B	123	
Chobpattana, V	79	
Cho, E	77	
Choe, M	38	
Cho, H	102	
Choi, G	42	
Choi, S	34, 46, 47, 84	
Cho, S	85	
Chowdhury, I	42	
Chow, W	45	
Christen, J	102	
Chuang, S	62	
Chu, H	108	
Chui, C	114	
Chung, R	46, 101	
Chung, S	112	
Chung, T	122	
Chu, S	38, 52	
Chvala, A	60	
Clark, B	47	
Clark, S	28, 63, 64	
Claverie, A	116	
Clement, N	122	
Cloutier, S	65	
Cochrane, C	78	
Cochran, J	98	
Cohen, D	46	
Colby, B	67, 106	
Coldren, L	29, 109, 110	
Cole Jr., E	55	
Coleman, E	36	
Colinge, C	115, 117, 118	
Collazo, R	53, 77	
Collins, P	23	
Collins, R	73	
Conley, J	78, 80, 115	
Coronel, N	30	
Corso, B	23	
Cowell, E	80	
Crawford, M	45, 46, 47, 81, 113	
Cristiani, T	89	
Crook, A	84, 85	
Cross, K	47, 113	
Cruz, S	49, 50	
Cui, S	122	

Index

Curtin, B 37

D

Daas, B 68, 69, 93
 Dähne, M 70, 82, 88, 89, 106
 Dalmau, R 53
 Dang, X 23, 73
 Daniels, K 68, 69, 93
 Dapkus, P 29, 108
 Dasgupta, S 33, 34
 Das, M 40
 Das, N 25
 Das, S 39, 114
 Datta, S 63
 Dawahre, N 105
 Dawson, L 28, 61, 64, 120
 Dawson, R 61
 Dayeh, S 121
 Dedigama, A 110
 de Guerville, F 116
 Deguet, C 116
 DeLeon, R 105
 Delker, C 39
 Demchenko, I 71
 Demeo, D 62
 Denbaars, S 37, 49, 101, 103
 DenBaars, S 46, 58, 83, 109, 110
 Deng, J 60
 Deng, Z 104
 Denlinger, J 71
 Denninghoff, D 33, 54
 Deparis, C 52
 Detchprohm, T 48, 75, 102, 121
 Dey, S 67, 112
 Dhar, S 41
 Dinolfo, P 74
 Dobrowolska, M 95
 Dodabalapur, A 80
 Donetsky, D 62
 Dongmo, P 72, 89
 Donoval, D 60
 Doolittle, W 20
 Doran, C 26, 115
 Dorfmueller, J 30
 dos Reis, R 72
 Douglas, E 32
 Doutt, D 103
 Drachev, R 42
 Dreyer, C 76
 D. Sands, T 36
 Duan, Z 57
 Dubey, M 123
 Dubon, O 71
 Duda, J 63
 Dudley, M 42, 83
 Dufaux, T 30
 Duong, D 73
 Dupuis, R 34, 45, 46, 47, 53, 58, 62, 84, 101

E

Ebert, P 82, 106
 Eddy, C 91
 Eddy Jr., C 42, 43
 Edgar, J 42
 Edirisooriya, M 110

Edmunds, C 106, 107
 Eisele, H 70, 82, 88, 89, 106
 El-Ella, H 107
 Enck, R 47, 54
 Engel-Herbert, R 79
 Engelken, R 30
 Eno, D 105
 Escobedo-Cousin, E 24
 Esposto, M 53, 60

F

Fang, T 84, 92
 Fan, J 62
 Fanning, T 50
 Fanton, M 44, 67, 68, 91
 Fastenau, J 62
 Fatholoulumi, S 113
 Favaloro, T 36
 Fay, P 79
 Feenstra, R 67
 Feezell, D 101
 Feigelson, B 91
 Fejer, M 118
 Felizco, F 30
 Feng, S 100
 Ferain, I 117, 118
 Ferrer, D 84
 Figiel, J 113
 Fischer, A 46, 47, 48, 84, 101
 Fisher, C 118
 Fitzgerald, E 113
 Flage-Larsen, E 22
 Flatte, M 93, 94
 Fortunato, E 56
 Foxon, T 71
 France, R 72, 86
 Franke, D 88
 Frenzel, H 56
 Freundlich, A 50
 Fuentes-Hernandez, C 27, 57
 Fujito, K 83, 101
 Fuller, E 23
 Furdyna, J 95
 Furtak, T 73

G

Gagnon, J 76
 Gallinat, C 47, 54
 Gallo, E 81
 Gammon, P 118
 Ganguly, S 58
 Gao, B 93
 Gao, X 59
 Gao, Y 100
 Garcia, T 64
 Gardner, G 106
 Garrett, G 53
 Garvey, J 105
 Gaska, R 60
 Gaskill, D 42, 43, 91
 Gautam, N 61
 Geisz, J 86
 Geng, Y 100
 Genz, F 88
 Gergaud, P 116

Germann, T 89
 Ghazinejad, M 66, 68, 93
 Ghosh, A 43, 44
 Ginley, D 103
 Gity, F 117
 Glans, A 95
 Gmachl, C 64
 Goldman, R 25, 28, 70
 Goldthorpe, I 24
 Golovatski, E 94
 Gong, Y 42
 Goorsky, M 49, 115, 116, 117
 Gordon, L 81
 Gossard, A 35, 49, 65, 78, 89
 Gowda, S 123
 Granada, M 95
 Granstrom, J 73
 Greenberg, K 57
 Grossklaus, K 90
 Gross, M 29
 Grundmann, M 56
 Guduru, R 123
 Gue, S 68
 Gullapalli, H 123
 Gundlach, D 73, 97
 Gunji, M 73, 113
 Gunning, B 20
 Guo, J 59
 Guo, S 59
 Gupta, A 124
 Gupta, S 85
 Gur, E 81, 82
 Guryanov, G 111
 Gu, S 63
 Gutacker, A 73
 Gutsche, C 39
 Guvenc, A 93
 Gwo, S 106

H

Haberstroh, J 37
 Hacker, C 45
 Hackman, N 35
 Hader, J 64
 Haeger, D 46
 Hains, C 28, 63, 64, 120
 Halik, M 98
 Hall, D 118, 119
 Haller, E 72
 Hall, J 30
 Hamaguchi, S 49
 Han, J 75, 102
 Hansen, D 42
 Han, W 93
 Haque, M 27
 Harada, K 86
 Hardy, M 83, 103
 Harris, D 80
 Harris, J 85, 101, 118
 Harris, N 105
 Hartland, G 93
 Harvey, T 66
 Hayashi, K 96
 Hayes, J 117
 Heatherly, L 50
 Heeger, A 73

Index

Heidrich, B.....	91	J	Ketterson, A.....	59
Heist, C.....	115	Jackson, M.....	Khan, M.....	114
He, L.....	110	Jackson, P.....	Kiefer, R.....	34
Henry, T.....	46, 81	Jackson, T.....	Kiehl, R.....	94
Henttinen, K.....	26	Jahan, N.....	Kim, B.....	112
Heremans, J.....	94	Jain, A.....	Kimball, G.....	29
Her, J.....	27	Jain, F.....	Kim, C.....	73
Hermannstädter, C.....	88, 89	Jakubiak, R.....	Kim, H.....	34, 38, 46, 53, 59, 60, 84
Herrero, A.....	66	Jandieri, K.....	Kim, J.....	27, 44, 46, 47, 57, 84
Hicks, R.....	66	Janes, D.....	Kim, K.....	50, 62
Hierro, A.....	52	Jang, J.....	Kimoto, T.....	77
Hirai, A.....	76	Janotti, A.....	Kim, S.....	37, 105
Hite, J.....	91	Jaworski, C.....	Kim, T.....	20, 107, 110
Hlaing Oo, W.....	70	Jean, R.....	Kimura, A.....	86
Hobart, K.....	42, 91	Jedaa, A.....	Kim, Y.....	27
Ho, C.....	113	Jena, D.....	Kippelen, B.....	27, 57
Hoffmann, A.....	53	Jenkins, C.....	Kipshidze, G.....	119
Hollander, M.....	44, 67, 91	Jennings, M.....	Kirby, B.....	95
Hollowell, A.....	120	Jeon, J.....	Kirk, B.....	36
Holl, S.....	118	Jernigan, G.....	Kirste, L.....	34
Holmes, A.....	100	Jha, P.....	Kirste, R.....	53
Holtz, M.....	111	Jha, S.....	Kis, A.....	43
Hong, W.....	38	Jiao, W.....	Kitai, A.....	51
Hong, Y.....	106	Ji, M.....	Kitano, M.....	26
Hopkins, P.....	63	Ji, Y.....	Klauk, H.....	97, 98
Hou, W.....	102, 121	Jo, G.....	Klein, P.....	41
Howsare, C.....	68	Johansen, K.....	Kline, R.....	97, 98
Hsu, C.....	65	John, D.....	Knutsen, K.....	104
Hsu, P.....	83, 103	Johnson, S.....	Kobayashi, M.....	49
Huang, C.....	115	Johnson, W.....	Kobayashi, N.....	36
Huang, F.....	73	Johnston-Halperin, E.....	Ko, D.....	40
Huang, G.....	110	Jo, M.....	Kodambaka, S.....	23, 66, 90
Huang, H.....	104	Joo, J.....	Koesdjojo, M.....	115
Huang, K.....	24	Juang, B.....	Koike, J.....	41
Huang, L.....	93	Juday, R.....	Koleske, D.....	46, 113
Huang, S.....	28	Julian, N.....	Koley, G.....	32, 91, 92, 93
Huang, Y.....	48, 62, 101	Julien, F.....	Kolluri, S.....	58
Hu, E.....	25, 57, 107, 122	Jung, K.....	Konar, A.....	84
Huffaker, D.....	28, 39, 40, 49, 65	Jung, S.....	Kondo, D.....	69
Hughes, Z.....	44, 91	Jung, Y.....	Kong, B.....	102
Hu, H.....	62	Jurchescu, O.....	Kong, J.....	38, 52
Huh, J.....	88	Ju, S.....	Kong, W.....	20, 107
Hull, B.....	40, 41	K	Kordos, P.....	60
Hunt, H.....	73	Kamimura, T.....	Kosel, T.....	79
Hunt, S.....	23	Kamins, T.....	Koslow, I.....	83, 103
Huo, Y.....	85	Kanazawa, T.....	Koswatta, S.....	79
Hurni, C.....	21, 50, 82	Kang, J.....	Kou, X.....	110, 115
Hu, S.....	24	Kanno, T.....	Kovac, J.....	60
Hu, X.....	60	Kappers, M.....	Kraft, O.....	113
Hwang, D.....	27, 57	Karbaum, C.....	Krishna, L.....	22, 35
Hwang, H.....	38, 56	Kargar, A.....	Krishnamoorthy, S.....	33, 53
Hwang, W.....	43, 79	Karmakar, S.....	Krishnamoorty, S.....	82
Hwang, Y.....	79	Kasarda, R.....	Krishna, S.....	61
I		Kato, R.....	Krivoy, E.....	85
Iijima, H.....	89	Kaun, S.....	Kuang, Y.....	71
Imbert, B.....	116	Kawabata, S.....	Kuball, M.....	42
Imhoff, E.....	42	Kawakami, R.....	Kub, F.....	42, 91
Inaguma, M.....	49	Kawamura, Y.....	Ku, C.....	57
Isabella, L.....	103	Kawasaki, J.....	Kuech, T.....	115
Isik, D.....	27	Keller, S.....	Kumano, H.....	88, 89
Ito, K.....	86	Kelly, M.....	Kunathai, N.....	100
Ivanova, L.....	70, 82, 88, 89, 106	Kern, K.....	Kunert, B.....	109
Iwai, T.....	69	Kesler, B.....	Kung, P.....	103, 105
Iyer, S.....	70		Künzel, H.....	88
Izyumskaya, N.....	102		Kuo, J.....	79
			Kutsay, O.....	52
			Kuznetsov, A.....	104

Index

Kwon, J	27	Li, X	87	Mishra, M	124
L		Li, Y	102, 105	Mishra, U	21, 31, 33, 34, 49, 50, 54, 58, 60, 78, 117
LaBella, M	44, 67, 68, 91	Lochner, Z	34, 53	Misra, R	63
Laboda, M	42	Long, B	117, 118	Mita, S	53, 77
Lahourcade, L	30	Lorenz, M	56	Mitchell, W	78, 79
Lajn, A	56	Losurdo, M	107	Mi, Z	113
LaLonde, A	22	Loth, M	99	Mizuta, S	31
Lal, S	117	Lowder, J	20	Modine, N	45
Lam, P	80	Lubyshev, D	62	Moe, C	21
Lang, J	21, 50	Luckert, F	71, 89	Mohammad, A	114
Lany, S	103	Lu, H	22, 35	Mohanty, P	123
Lau, K	100	Lu, J	33, 78, 117	Mohney, S	112
Laurent, M	54	Lujan, R	113	Molnar, R	106, 107
Lau, S	26, 115	Lukco, D	40	Moloney, J	64
Law, J	78, 79	Lundgren, E	89	Mönig, R	113
Lee, C	27, 44, 80	Luong, M	81	Moody, B	53
Lee, D	56	Luria, J	97	Moran, P	22
Leedy, K	56	Lutz, C	84, 100	Morhain, C	52
Lee, G	74, 86	Lu, W	38, 59, 60, 123	Morkoç, H	102
Lee, M	28, 75, 87, 120	Lu, Y	57, 62, 79, 103	Moseley, M	20
Lee, S	26, 47, 52, 113, 121	Lyons, J	81	Moug, R	64
Lee, T	38, 123	Lysov, A	39	Moulet, C	116
Lee, V	31	M		Mueller, D	87
Lee, Y	34	Mack, S	94	Mueller, S	42
Leiner, J	95	Madaria, A	29	Mughal, M	30
Lelis, A	78	Mages, P	109, 110	Müller, S	56
Lemiti, M	116	Mahadik, N	23, 42	Murata, Y	23, 90
Lenahan, P	78	Makhijani, R	90	Murphy, N	25, 26
Lenz, A	70, 88, 89, 106	Malis, O	106, 107	Murray, C	94
Lenz, E	89	Mandl, M	62	Myers, R	65, 94
Lenzner, J	56	Manfra, M	20, 31, 106, 107	Myers, S	61
Lester, S	102	Mansurov, V	111	Myers-Ward, R	42, 43, 91
Letzkus, F	97	Mao, S	72	N	
Leung, B	75, 102	Marconi, M	120	Nagel, J	51
Levander, A	71	Maria, J	80	Nair, H	84, 85
Lewis, C	97	Mariani, G	49	Nakamura, S	37, 75, 76, 83, 101, 103
Liang, B	87	Marohn, J	97	Nakanishi, T	26
Liang, H	39, 40, 100	Marshall, A	24, 112	Nanishi, Y	108
Liang, X	45	Martens, R	105	Narayanan Kutty, M	61
Liao, K	102	Martin, R	71	Nath, D	33, 53, 60
Li, D	104, 107	Martins, R	56	Naydenkov, M	61
Lieberman, M	119	Mason, A	115	Nelson-Cheeseman, B	95
Liebich, S	109	Mason, T	103	Neufeld, C	49, 50
Li, G	21, 48, 58	Mastro, M	91	Neuvonen, P	104
Li, H	71	Matioli, E	50	Newell, J	30
Li, J	70, 119	Matney, K	23	Newman, S	47
Li, L	38	Matsumoto, K	44	Ngo, C	66
Liliental-Weber, Z	71, 72	Mawby, P	118	Nguyen, T	23, 73
Lim, T	34	Mayer, M	72	Nikishin, S	111
Lin, A	118	Mayer, T	122	Nolph, C	95
Lin, C	29	Mazen, F	116	Nomani, M	32, 91, 92
Lindemuth, J	31	McIntosh, D	54	Nomani, W	93
Lin, H	85	McIntyre, P	24, 73, 112, 113	Noriega, R	97, 98
Lin, J	45, 66, 73, 93	McMahon, W	86	Northrup, J	97, 98
Lin, Y	108	McSkimming, B	21	Novak, M	98
Lindemuth, J	31	Mecklenburg, M	66	Novikov, S	71
Lin, H	85	Medeiros-Ribeiro, G	55	Nunes, T	100
Lin, J	45, 66, 73, 93	Mehrotra, A	50	Nutt, S	108
Lin, Y	108	Metzner, S	102	Nyakiti, L	91
Li, Q	45, 113	Mikhailovsky, A	23	O	
Li, R	29, 79	Mikkelsen, A	89	Obeng, Y	45
List, F	50	Miller, M	47, 55	O'Brien, W	119
Liu, A	62	Mills, M	65		
Liu, H	120	Millunchick, J	90		
Liu, J	38, 52, 55	Ming, L	111		
Liu, L	32, 92				
Liu, Q	79				
Liu, S	102				
Liu, X	78, 93, 95				

Index

Ohno, T.....	73	Pimputkar, S.....	75	Rol, F.....	107
Ohoka, A.....	31	Piner, E.....	31, 59, 75	Romanov, A.....	83
Oh, S.....	56	Pipe, K.....	36	Romero, M.....	86
Ohta, H.....	37	Plis, E.....	61	Roshko, A.....	66
Ohya, S.....	94	Podraza, N.....	120	Rotella, P.....	54
Okumura, H.....	77	Pohl, U.....	88, 89	Rotter, T.....	28, 63, 64, 88, 89, 109
Olavarria, W.....	86	Ponce, F.....	46, 47, 48, 84, 101	Rourke, D.....	32, 66
Oliver, R.....	107	Poon, A.....	100	Rowe, M.....	32
Olmedo, M.....	52, 55	Potscavage, W.....	27	Russell, K.....	25, 107, 122
Oloniyo, O.....	124	Pötschket, K.....	89	Ryou, J.....	34, 46, 47, 53, 62, 84, 101
O'Loughlin, M.....	40	Pozdin, V.....	97	Ryu, S.....	40, 41
Olsen, S.....	24	Pozuelo, M.....	66		
Olson, D.....	73	Prange, J.....	73	S	
Omar, S.....	42	Preble, E.....	48, 102	Sabitova, A.....	106
Omote, A.....	35	Prost, W.....	39	Sahalov, H.....	120
Onishi, T.....	36	Protasenko, V.....	48	Saitoh, Y.....	86
Ooi, B.....	54	Ptak, A.....	72, 86	Sakai, A.....	35
Oswald, N.....	70	Puls, C.....	68	Sakr, S.....	109
Özgür, Ü.....	102	Putkaradze, V.....	120	Salagaj, T.....	69
Ozkan, C.....	45, 66, 68, 93			Salahuddin, S.....	43
Ozkan, M.....	45, 66, 68, 93	Q		Salas, R.....	85
		Qadri, S.....	23	Salehzadeh, O.....	66
P		Qazi, M.....	32	Salleo, A.....	97, 98
Padture, N.....	40	Qi, J.....	55	Salvetat, T.....	116
Paillard, V.....	116	Qi, M.....	112	Sambandam, S.....	50
Palefsky, S.....	65	Quay, R.....	34	Sampath, A.....	21, 47, 54
Palmour, J.....	40, 41			Sanchez, E.....	42
Palmstrom, C.....	89	R		Sanders, A.....	32, 66
Palmstrøm, C.....	35, 65	Radenovic, A.....	43	Sands, T.....	39
Pan, C.....	101	Radisavljevic, B.....	43	Sanford, N.....	32, 38, 66
Pandikunta, M.....	111	Raghothamachar, B.....	42, 83	Santato, C.....	27
Paranthaman, M.....	50	Rajan, S.....	33, 53, 60, 82	Saraswat, K.....	85
Park, B.....	85	Raman, A.....	54	Sarkar, V.....	83
Park, J.....	74	Ramirez, J.....	105	Sarmiento, T.....	101
Park, P.....	33, 53, 60	Ramu, A.....	35	Sasaki, A.....	26, 87
Park, S.....	27, 112	Rao, S.....	111	Sasaki, M.....	88
Park, W.....	38	Raskin, J.....	24	Sasakura, H.....	88
Paskova, T.....	48, 102	Raychaudhuri, S.....	113	Sasikumar, A.....	31
Patel, C.....	71	Rearick, D.....	44	Satka, A.....	60
Patel, V.....	28, 64	Reddy, K.....	40	Satoh, M.....	96
Patra, N.....	70	Redwing, J.....	76	Sattu, A.....	60
Patriarche, G.....	122	Reed, M.....	47	Saunier, P.....	59
Paul, R.....	68	Regan, C.....	66	Sbrockey, N.....	69, 81, 91
Paulson, C.....	113	Regolin, I.....	39	Scarpulla, M.....	49, 51, 70
Pearton, S.....	32	Reiber Kyle, J.....	93	Schaafhausen, S.....	106
Pei, Y.....	22	Reinke, P.....	95, 120	Schaper, C.....	111
Penchev, M.....	45, 66	Reissmann, S.....	28, 64	Scherf, U.....	73
Peng, H.....	45	Remcho, V.....	115	Schiffer, P.....	63
Peng, J.....	67, 112	Ren, F.....	32	Schlager, J.....	38, 66
Peng, L.....	64	Ren, J.....	38, 52, 55	Schlesser, R.....	53
Pérez-Tomas, A.....	118	Restrepo, O.....	40	Schowalter, L.....	52
Perkins, J.....	103	Reuters, B.....	61	Schroeter, P.....	50
Pernot, G.....	35	Rice, A.....	53, 77	Schuette, M.....	59
Petroff, P.....	109	Richter, C.....	45	Schulze, J.....	89
Petropoulos, J.....	72, 89	Riechers, P.....	94	Seabaugh, A.....	43, 79
Petrova, V.....	23, 90	Ringel, S.....	31, 53, 82	Sedlmayer, A.....	113
Petrov, I.....	23, 90	Rivnay, J.....	97, 98	Seibert, C.....	119
Petschke, A.....	62	Roberts, D.....	87	Selvamanickam, V.....	50
Pflugl, C.....	101	Roberts, J.....	59	Sengupta, S.....	90
Phillips, J.....	55, 56, 61, 88, 108	Robins, L.....	38	Sensale-Rodriguez, B.....	92
Phillips, P.....	65	Robinson, J.....	44, 67, 68, 91	Seo, J.....	73
Phinney, L.....	63	Rodwell, M.....	78, 79	Seong, T.....	121
Picard, Y.....	64	Roedel, R.....	112	Severino, A.....	118
Pichanusakorn, P.....	22, 71	Rogers, T.....	118	Shahedipour-Sandvik, F.....	76
Pickett, M.....	55	Rojas Sanchez, J.....	95	Shahil, K.....	92
Picraux, T.....	121			Shakouri, A.....	35, 36

Index

Shambat, G.....	85	Steren, L.....	95	Triplett, G.....	87, 109
Shao, J.....	100	Stevens, K.....	100	Trivedi, N.....	40
Shao, L.....	36	Stewart, L.....	108	Trumbull, K.....	44, 67, 68, 91
Shao, Y.....	38	Stitt, J.....	68	Tseng, A.....	71
Shapiro, J.....	39, 40, 49, 65	Stolz, W.....	109	Tseng, F.....	44
Shatalov, M.....	60	Stone, P.....	70	Tsui, R.....	37
Shea, P.....	55	Stragier, A.....	116	Tu, C.....	71
Shemelya, C.....	62	Street, R.....	113	Tu, K.....	121
Shen, A.....	64	Strittmatter, A.....	89	Tummala, R.....	123
Shen, G.....	105	Subramanian, G.....	39, 67	Tungare, M.....	76
Shen, H.....	47, 51, 53	Subrina, S.....	92	Tweedie, J.....	53, 77
Shen, P.....	54	Suchalkin, S.....	62, 119		
Shen, S.....	34	Su, D.....	42	U	
Shetu, S.....	68, 92, 93	Suda, J.....	77	Uddin, M.....	111
Shields, V.....	69, 91	Sudarshan, T.....	41, 42, 68, 69, 93	Ureña, F.....	24
Shin, H.....	120	Suemasu, T.....	86		
Shin, J.....	87	Suemune, I.....	88, 89	V	
Shin, K.....	114	Sugahara, S.....	96	Vandervelde, T.....	62
Shintri, S.....	111	Sullivan, G.....	63	Van de Walle, C.....	76, 81
Shrivastava, A.....	41	Sultana, H.....	64	Vangilder, J.....	30
Shterengas, L.....	71, 119	Sundaram, A.....	50	Vasen, T.....	79
Shur, M.....	60	Sun, K.....	46, 47, 48, 74, 84, 101	Velicu, S.....	36
Shuto, Y.....	96	Sun, L.....	25, 26	Verma, J.....	21, 48, 58, 59
Siddiqui, J.....	56	Sun, N.....	84	Vogelgesang, R.....	30
Siegel, G.....	70	Sun, Q.....	75, 102	Volz, K.....	70, 109
Signamarcheix, T.....	116	Sun, S.....	42	von Wenckstern, H.....	56
Siller, L.....	24	Sun, Y.....	73	Voßbürger, V.....	70
Simin, G.....	60	Sutou, Y.....	41	Vuckovic, J.....	85
Simmonds, P.....	28, 87	Svensson, B.....	104	Vuillaume, D.....	122
Simon, J.....	75	Svensson, S.....	62, 71		
Simov, K.....	95	Swenson, B.....	78	W	
Singh, A.....	91	Sztein, A.....	37	Wager, J.....	80, 103
Sitar, Z.....	53, 77			Waite, A.....	25, 26
Skriniarova, J.....	60	T		Walker, B.....	73
Sloppy, J.....	81	Tabares, G.....	52	Waltereit, P.....	34
Smaali, K.....	122	Taheri, M.....	81	Walukiewicz, W.....	20, 71, 72
Smolev, S.....	61	Tahy, K.....	43, 92	Wang, C.....	84
Snow, E.....	117	Takahashi, K.....	35	Wang, D.....	62, 71, 74
Snyder, D.....	44, 67, 68	Takamura, Y.....	96	Wang, G.....	38, 113
Snyder, G.....	22	Takata, K.....	94	Wang, H.....	42
Snyder, J.....	22	Takeda, Y.....	86	Wang, K.....	108, 110
Soga, I.....	69	Tamargo, M.....	64	Wang, L.....	31, 63
Sohal, S.....	111	Tamayama, Y.....	26	Wang, P.....	39
Sohn, J.....	38	Tamayo, A.....	73	Wang, W.....	61, 88, 93
Soltz, W.....	70	Tanaka, M.....	94	Wang, Y.....	110
Song, H.....	42	Tanaka, S.....	101	Warde, E.....	109
Song, J.....	104, 121	Tang, L.....	106, 107	Ward, J.....	99
Song, K.....	123	Tang, W.....	121	Ward, P.....	118
Song, S.....	123	Tangyunyong, P.....	55	Watkins, S.....	66, 104
Song, Y.....	28	Tchernycheva, M.....	109	Weidner, J.....	69
Spanier, J.....	81	Tedesco, J.....	43	Weiland, B.....	68
Speaks, D.....	72	Tegude, F.....	39	Wei, Q.....	48
Speck, J.....	21, 31, 33, 34, 46, 49, 50, 75, 76, 82, 83, 101, 103, 108	Teplin, C.....	50	Wei, S.....	106
Spencer, M.....	67, 69, 91	Terziyska, P.....	20	Welland, M.....	38
Sperling, B.....	45	Thibeault, B.....	78, 79	Weng, X.....	76
Spry, D.....	40	Thombare, S.....	112, 113	Wen, X.....	123
Sramaty, R.....	60	Thompson, C.....	113	Westlake, K.....	113
Srevastava, A.....	123	Timm, R.....	88, 89	Wetherington, M.....	67
Stach, E.....	67, 112	Tivakornsasithorn, K.....	95	Wetzel, C.....	48, 49, 102, 121
Stahlbush, R.....	40, 42	Tiwari, S.....	57	Weyers, M.....	77
Stark, C.....	48, 102, 121	To, B.....	86	Wheeler, V.....	91
Steenbergen, E.....	62	Toberer, E.....	22	Wickey, K.....	94
Steiner, M.....	86	Toledo, N.....	49	Wierer, J.....	47
Stemmer, S.....	79	Tompa, G.....	36, 69, 81, 91	Wijewarnasuriya, P.....	86
Stephenson, C.....	119	Toney, M.....	97, 98	Wilbert, S.....	105
Stephon, N.....	115	Tripathi, S.....	124		

Index

Williams, C	69
Williams, R	55
Willner, B	69
Windl, W	40
Winkler, C	81
Wistey, M	59, 79, 119
Won, D	76
Wong, M	31, 34
Wong, P	40, 49
Wong, W	26, 112
Woodall, J	29
Wolf, A	107
Wraback, M	21, 47, 52, 53, 54
Wright, J	21, 47
Wu, B	119
Wu, F	42, 83
Wu, H	39, 40, 73
Wu, J	28, 71

X

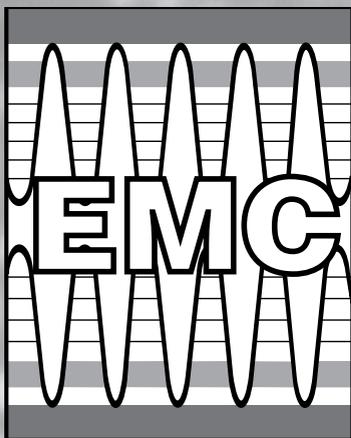
Xie, J	53, 77
Xing, H	43, 48, 58, 59, 78, 79, 90, 92, 93
Xin, Y	94
Xiu, F	110
Xu, H	28, 64
Xu, J	65
Xu, X	36, 112

Y

Yadav, A	36
Yagi, A	49
Yagishita, Y	69
Yakes, M	23
Yamada, Y	35
Yamaguchi, T	108
Yang, C	65, 112
Yang, F	40
Yang, J	55, 60, 65, 94
Yang, Y	110
Yan, K	45
Yan, R	92
Yao, M	29
Yao, Y	64
Yeh, T	108
Yeluri, R	78
Ye, M	86
Yen, T	105
Yerino, C	75, 102
Yeung, Y	25
Yi, C	23
Yocom, A	73
Yoder, P	46
Yokogawa, T	48
Yoon, E	108
Yoon, J	38
Yoon, Y	43
Young, D	50
Young, E	21, 46, 83, 103, 108
You, S	48, 102
Yuan, W	119
Yu, H	39, 40, 67, 112
Yu, K	70, 71, 72
Yun, J	105
Yu, R	117
Yu, X	110

Z

Zakharov, D	39
Zakytayev, A	103
Zeier, W	22
Zevalkink, A	22
Zhang, C	110
Zhang, J	40, 104
Zhang, K	36
Zhang, L	42
Zhang, M	54, 108
Zhang, Q	45, 79
Zhang, R	69
Zhang, Y	34, 42, 62, 75, 102
Zhang, Z	82, 104
Zhan, N	55
Zhao, J	36, 38, 55
Zhao, L	48, 102
Zhao, X	40
Zhao, Y	101
Zheng, Y	29
Zhong, J	45, 66
Zhong, Y	72
Zhong, Z	100
Zhou, C	29
Zhou, G	78, 79
Zhou, H	66
Zhou, Q	54
Zhu, H	79
Zhu, J	106
Zhu, M	67
Zhu, X	45
Zhu, Y	42
Zide, J	35, 36, 70, 72, 89
Ziegler, S	109
Zimprich, M	109
Zscheschang, U	97
Zunger, A	103
Zuo, D	62
Zuo, J	62
Zuo, Z	52



2 0 1 1

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Corwin East			Session O: III-Nitrides: UV Emitters and Detectors	Session W: III-Nitride: Bulk Growth and Epitaxy	Session FF: III-Nitrides: Epitaxy Material and Devices II Session GG: Non-Polar and Semi-Polar III-Nitrides Devices
Corwin West			Session P: Oxide Semiconductors and Devices	Session X: Oxide Thin Films	Session HH: Oxide Semiconductors: Growth and Doping
Flying A	Session A: III-Nitrides: MBE Growth	Session H: III-Nitrides: Electronics I	Session Q: III-Nitrides: Electronics II	Session Y: Point, Defects, Doping and Extended Defects	Session II: Intersubband Devices: AlInN and InGAN Materials Characterization
Lobero	Session B: Thermoelectrics and Thermionics I	Session I: Thermoelectrics and Thermionics II	Session R: Narrow Bandgap Materials and Devices	Session Z: Epitaxial Materials and Devices I	Session JJ: Compound Semiconductor Growth on Silica Substrates
Lotte Lehman	Session C: Nanoscale Characterization	Session J: Nanowire Transport and Devices	Session S: Nanowire Synthesis and Characterization	Session AA: Four Dots and a Dash Session BB: Fundamentals of Low-Dimensional Structures	Session KK: Nanowire Growth and Applications
MCC Lounge	Session D: Plasmonics and Metamaterials	Session K: Silicon Carbide Growth, Characterization and Devices			
MCC Theatre	Session E: Organic, Printed and Flexible Electronics	Session L: Graphene Fabrication and Devices	Session T: Growth of Graphene and Carbon Nanotubes	Session CC: Graphene Characterization and Applications	Session LL: Materials Integration: Wafer Bonding and Engineered Substrates
Santa Barbara Harbor	Session F: Devices Utilizing Low Dimensional Structures	Session M: III-Nitrides: Defects and LEDs	Session U: Highly Mismatched Alloys	Session DD: Nano-Magnetic, Magnetic Memory and Spintronic Materials	Session MM: Semiconductor Processing: Oxidation, Passivation, Etching and Contacts
State Street	Session G: Photovoltaics: New Materials and Characterization	Session N: Next Generation Solar Cell Materials and Devices	Session EE: Organic Thin Film and Crystalline Transistors: Devices and Materials	Session V: Organic Photovoltaics and Photoelectrochemical Cells	Session NN: Molecular Electronics / Sensor / Ionic Conductors