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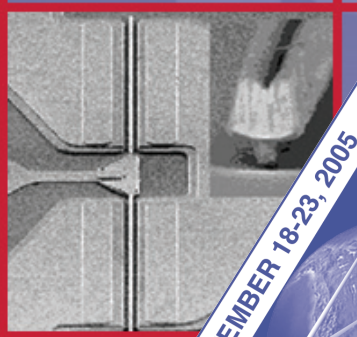

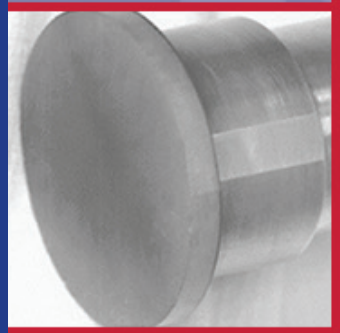

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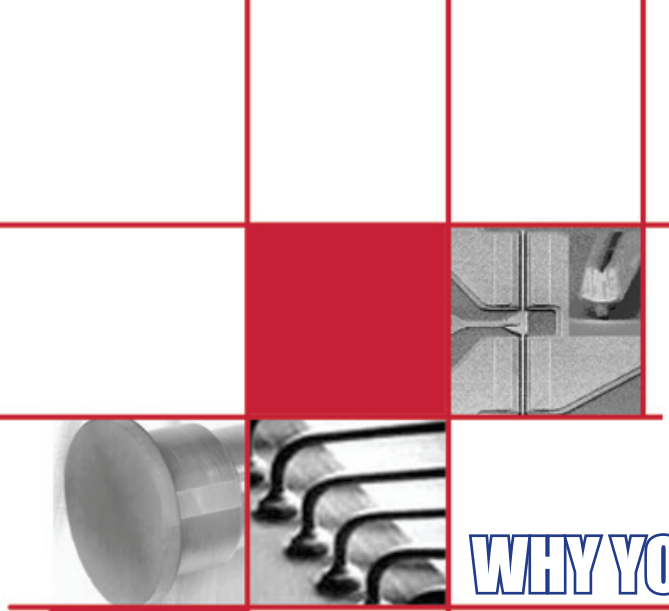

WHY YOU SHOULD ATTEND

The International Conference on Silicon Carbide and Related Materials (ICSCRM) has become the pre-eminent forum to discuss new research results and assess the true "state of the art" for SiC, gallium nitride (GaN) and other related wide bandgap semiconductors. Semiconductor materials science and technology have provided a solid foundation for the remarkable performance of current electronic and optical device technology. Wide bandgap semiconductors, typically defined as materials exhibiting an electronic bandgap greater than 2.9 eV, are emerging as materials capable of driving continued device performance enhancements for many years to come. SiC has been studied for decades, but recent developments have firmly established commercial products in optical, RF and power components. Continued research in the field will assure that the rapid developmental timeline for SiC-based device technology can proceed.

Conference Topics

Materials Growth (Bulk and Epitaxial)

Materials Characterization and Theory

Device Processing

Device Optimization/Performance

WHY YOU SHOULD ATTEND

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About TMS

The Minerals, Metals & Materials Society (TMS) is a professional organization encompassing the entire range of materials and engineering, from minerals processing and primary metals production to basic research and the advanced applications of materials. Included among its professional and student members are metallurgical and materials engineers, scientists, researchers, educators, and administrators from more than 70 countries on six continents. TMS' mission is to promote the global science and engineering professions concerned with minerals, metals, and materials.

The Electronic, Magnetic & Photonic Materials Division (EMPMD) of TMS actively promotes technical exchange and assists in professional development through programming, publications, and continuing education. To further these objectives, the division structures programs to maximize the following: intercommittee, interdivisional, and intersocietal content; interaction among industrial, academic, and governmental personnel; and interaction among science, engineering, and business. To become involved, apply online at www.tms.org/society/membership.html or call (800) 759-4867.

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Topics & Invited Speakers

BULK GROWTH

- Dislocation Reduction in Bulk SiC, D. Nakamura (plenary)
- Advances in Halide-CVD Bulk Growth, A. Polyakov
- Advances and Challenges in Numerical Simulation of Bulk Growth, Y. Makarov
- Defect Reduction in Bulk SiC Growth, H.J. Rost

EPITAXIAL GROWTH

- Large Area, Multi-Wafer Epitaxy, B. Thomas
- Hot Wall, Fast Growth Rate SiC Epitaxy, S. Nishizawa
- Epitaxial Films With Low Basal Plane Dislocations, J. Sumakeris
- Reduction of Defects in GaN Films on SiC, C. Eddy

CHARACTERIZATION AND THEORY

- Theory of SiC Insulator Interfaces, S. Pantelides (plenary)
- Theory of Dislocations in SiC, A. Blumenau
- Optical Studies of Deep Centers in S. I. SiC, B. Magnussen
- Theory of Magnetic Properties of Transition Elements in SiC, M. Miao
- Applications of BEEM to SiC, J. Pelz
- Inelastic Neutron and X-ray Scattering Studies of Phonons in SiC, D. Strauch

DEVICE PROCESSING

- Ion Implantation Effects in SiC, B. Svensson (plenary)
- ONO Gate Dielectrics and Impact on Dislocations in SiC MOS Devices, S. Tanimoto
- Contacts to P-type 4H-SiC, M. Murakami
- Nanochemistry and H-induces Metallization of SiC Surfaces, G. Soukiassian
- High Channel Mobility and Reliability of SiC MOSFETs, E. Sveinbjornsson
- Whole Wafer PL Characterization of Defects in SiC Substrates, M. Tajima

DEVICES

- SiC RF and Power Devices, J. Palmour (plenary)
- SiC Device Applications, J. Hancock
- SiC Power MOSFETs, D. Peters
- Drift Free SiC Pin Junction Rectifiers, M. Das
- SiC GTOs, Y. Sugawara

Registration

Attendees, including authors, presenters, and session chairs are required to register. Authors are expected to present their papers in person at the conference. If an author must withdraw a paper, the technical program chair must be notified well in advance.

REGISTER BEFORE AUGUST 29 AND SAVE $100!

Advance Rate Full Conference: $725
On-site Rate Full Conference: $825
Includes technical sessions, welcoming reception, coffee breaks, continental breakfast, conference banquet, luncheons, poster session breaks, copy of post-conference proceedings*

Advance Student Rate: $250
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*Badges must be worn to gain access to technical sessions and social functions.

TWO CONVENIENT WAYS TO REGISTER

Register online at www.tms.org/Meetings/Specialty/ICSCRM2005/home.html. Or complete the enclosed registration form and return to TMS Meeting Services, 184 Thorn Hill Road, Warrendale, PA 15086, USA; Fax (724) 776-3770; E-mail mtgserv@tms.org.

Full payment in U.S. dollars must accompany the completed registration form.

REFUND POLICY

Written requests for refunds must arrive at TMS Meeting Services, 184 Thorn Hill Road, Warrendale, PA 15086, USA no later than Monday, August 29. A $75 processing fee is charged for all cancellations.

Accommodations

The Westin Convention Center Pittsburgh

Located in the heart of the city's business and cultural districts, The Westin Convention Center Pittsburgh is adjacent to the new David L. Lawrence Convention Center. Guests appreciate meeting rooms with high-speed Internet access and a self-service business center, not to mention the 8,000 square foot Executive Fitness Center. It offers free weights, aerobic equipment, Nautilus training, indoor lap pool, steam, sauna, massage therapy, and aerobic classes.

The hotel is connected to one of Pittsburgh's premier destination restaurants, The Original Fish Market, serving dinner until 1 a.m. daily. Complimentary transportation is available Monday through Friday within the central business district and to local attractions such as the Heinz History Center, Andy Warhol Museum, PNC Park and Mellon Arena.

RESERVATIONS

Reservations must be made and guaranteed by Friday, August 19 or the conference rate and rooms may not be available.

Guests can access a special Westin ICSCRM 2005 site to learn more about the hotel and to book, modify, or cancel reservations until September 25, 2005. Access to the site is organized by guest type and can be obtained by visiting **www.starwoodmeeting.com/Book/ICSCRM2005.**

Mail or fax the housing form in this mailer as early as possible to:
The Westin Convention Center Pittsburgh
ATTN: Terri Eberle, Group Coordinator
1000 Penn Avenue, Pittsburgh, Pennsylvania 15222
Fax: (412) 560-6480

For inquiries and cancellations, call the Westin Hotel at (412) 281-3700.

Social Events

Welcoming Reception - Sunday, September 18, 6 to 8:30 p.m.

Continental Breakfast – daily; coffee, juice, breakfast pastries and fruit served before technical sessions

Session Breaks – mid-morning and afternoon; beverages and snacks outside the technical session rooms

Luncheon - Monday, Tuesday, Wednesday, Thursday, 12:15 to 1:30 p.m.

Poster Session/Breaks – Monday, Tuesday, Wednesday, Thursday, 1:50 to 4:10 p.m.; posters conveniently displayed outside the luncheon room at the convention center

BANQUET DINNER

Free to full conference attendees, this gala event on Tuesday, September 20 begins with a reception of cocktails and hors d'oeuvres at the Carnegie Museum of Natural History. The museum was founded in 1895 by Andrew Carnegie. It conducts scientific inquiry that creates knowledge and promotes stewardship of the Earth and its life. Areas of the museum open to conference attendees include the Gems & Minerals and the Hall of Architecture Exhibits.

Transportation

AIRPORT SHUTTLE

Transportation to and from the airport is available via Express Shuttle USA. The cost is $17 one-way and $32 round-trip. Tickets can be purchased at the Express Shuttle ticket booth in the airport lower level baggage claim area. Ticket holders board from door #4. Shuttles leave hourly, Sunday through Friday from 7 a.m. to 11:30 p.m., and on Saturday from 8 a.m. to 5 p.m. For more information, call (412) 321-4990 or (800) 991-9890.

TAXI

Taxis are available from the airport at the lower level baggage claim area. Cost is approximately $40 one-way.

DRIVING DIRECTIONS

From Pittsburgh International Airport

Take Route 60 towards Pittsburgh through the Fort Pitt Tunnel and exit at Liberty Avenue. Follow Liberty Avenue to 10th Street. Turn left; hotel is on the right.

From East

Take the Pennsylvania Turnpike to Exit 57 to 376 West. Take 376 West to Exit 1C (Grant Street). Take Grant Street to 11th Street and turn left. Drive one block to Pennsylvania Avenue. Turn left and drive one block to 10th Street. Turn left onto 10th Street; hotel entrance is on the left.

From North

Take Interstate 79 South to Interstate 279 South. Follow the signs to Interstate 579 South and cross over Veterans Bridge. Take the 7th Avenue Exit. Proceed to the second light and turn right. Pass the next light; hotel driveway is on the right.

From South

Take I-79 North to the Pittsburgh Exit. Take I-279 North across Fort Pitt Bridge into the city. Follow the signs to Liberty Avenue. Take Liberty Avenue to 10th Street and turn left; hotel entrance is on the right.

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Meeting attendees from countries that require a visa to enter the United States are reminded that the process of obtaining a visa may take several months. Those attendees should begin the application process early. The U.S. State Department Web site, www.state.gov, includes Visa information.

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PROCEEDINGS

ICSCRM 2005 proceedings are scheduled for publication in January 2006. One copy is shipped to each full conference registrant. Additional copies may be purchased on the registration form for $110 each.

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Schedule of Events

Sunday, September 18

Registration	2 to 7:30 p.m.	Allegheny Ballroom Foyer
Exhibit Grand Opening	7 to 9 p.m.	Allegheny Ballroom Foyer
Welcoming Reception	7 to 9 p.m.	Allegheny Ballroom I /Foyer

Monday, September 19

Registration	7 a.m. to 5 p.m.	Allegheny Ballroom Foyer
Exhibit	7:30 to 10:30 a.m.	Allegheny Ballroom Foyer
Plenary Session	8:30 to 10:15 a.m.	Allegheny Ballroom
Break	10:15 to 10:45 a.m.	Allegheny Ballroom Foyer
Sessions	10:45 a.m. to 12:30 p.m.	Allegheny Ballroom I / II & III
Lunch	12:40 to 1:50 p.m.	Spirit of Pittsburgh Ballroom B/C
Posters	1:50 to 4:10 p.m.	Spirit of Pittsburgh Ballroom Foyer
Exhibit	2:30 to 5:15 p.m.	Allegheny Ballroom Foyer
Break	4:10 to 4:30 p.m.	Allegheny Ballroom Foyer
Sessions	4:30 to 5:15 p.m.	Allegheny Ballroom I / II & III

Tuesday, September 20

Registration	7 a.m. to 5 p.m.	Allegheny Ballroom Foyer
Exhibit	7:30 to 10:30 a.m.	Allegheny Ballroom Foyer
Sessions	8:30 to 10:15 a.m.	Allegheny Ballroom I / II & III
Break	10:15 to 10:45 a.m.	Allegheny Ballroom Foyer
Sessions	10:45 a.m. to 12:30 p.m.	Allegheny Ballroom I / II & III
Lunch	12:40 to 1:50 p.m.	Spirit of Pittsburgh Ballroom B/C
Posters	1:50 to 4:10 p.m.	Spirit of Pittsburgh Ballroom Foyer
Exhibit	2:30 to 5:15 p.m.	Allegheny Ballroom Foyer
Break	4:10 to 4:30 p.m.	Allegheny Ballroom Foyer
Sessions	4:30 to 5:15 p.m.	Allegheny Ballroom I / II & III
Conference Banquet	6 to 9:30 p.m.	Carnegie Museum of Natural History

Wednesday, September 21

Registration	7 a.m. to 5 p.m.	Allegheny Ballroom Foyer
Exhibit	7:30 to 10:30 a.m.	Allegheny Ballroom Foyer
Sessions	8:30 to 10:15 a.m.	Allegheny Ballroom I / II & III
Break	10:15 to 10:45 a.m.	Allegheny Ballroom Foyer
Sessions	10:45 a.m. to 12:30 p.m.	Allegheny Ballroom I / II & III
Lunch	12:40 to 1:50 p.m.	Spirit of Pittsburgh Ballroom B/C
Posters	1:50 to 4:10 p.m.	Spirit of Pittsburgh Ballroom Foyer
Break	4:10 to 4:30 p.m.	Allegheny Ballroom Foyer
Sessions	4:30 to 5:15 p.m.	Allegheny Ballroom I / II & III

Thursday, September 22

Registration	7 a.m. to 5 p.m.	Allegheny Ballroom Foyer
Sessions	8:30 to 10:15 a.m.	Ballroom I
Break	10:15 to 10:45 a.m.	Allegheny Ballroom Foyer
Sessions	10:45 a.m. to 12:30 p.m.	Allegheny Ballroom I / II & III
Lunch	12:40 to 1:50 p.m.	Spirit of Pittsburgh Ballroom B/C
Posters	1:50 to 4:10 p.m.	Spirit of Pittsburgh Ballroom Foyer
Break	4:10 to 4:30 p.m.	Allegheny Ballroom Foyer
Sessions	4:30 to 5:15 p.m.	Allegheny Ballroom I / II & III

Friday, September 23

Registration	7 a.m. to 5 p.m.	Allegheny Ballroom Foyer
Plenary Session	8:30 to 10:15 a.m.	Ballroom I
Break	10:15 to 10:45 a.m.	Allegheny Ballroom Foyer
Sessions	10:45 a.m. to 12:30 p.m.	Ballroom II & III

MAP. Plenary Session I

Monday, 8:30-10:10am
September 19, 2005

Room: Allegheny Ballroom I
Location: Westin Pittsburgh

Session Chairs: W. R.L. Lambrecht, Case Western Reserve University; H. McD. Hobgood, Cree, Inc.

8:30 AM Welcome and Introductory Remarks by Laura Rea

8:50 AM Plenary
Reduction of Dislocations in the Bulk Growth of SiC Crystals: *Daisuke Nakamura*[1]; [1]Toyota Central R&D Laboratories, Inc.

Recently, the macroscopic defects such as micropipes, polytype inclusions and small angle boundaries in SiC substrates have been reduced gradually. However, there are still more than a few macroscopic defects (1~10 cm^{-2}) and a high density of elementary dislocations (~10^4 cm^{-2}) such as threading edge dislocations, basal plane dislocations and screw dislocations in SiC substrates. I believe that our goal of developing the SiC substrates for high-performance and high-reliability devices should be to reduce the elementary dislocations to virtually zero as well as the macroscopic defects. We proposed novel method for elimination of the dislocations, composed of two or more times growth perpendicular to c-axis (a-face growth) and final growth along c-axis (c-face growth). We call this method as Repeated A-Face (RAF) growth process. Averaged EPDs of the RAF substrates are less by two to three orders magnitude than conventional substrates, and there is no micropipe in the observed area of the substrate. Moreover, the synchrotron X-ray topography shows that crystal quality of the RAF substrate is very homogeneous, and there are very few macroscopic defects and dislocations. Thus, the RAF growth process is very effective to eliminate dislocations and other defects.

9:30 AM Plenary
Ion Implantation Processing and Related Effects in SiC: *B. G. Svensson*[1]; A. Hallén[2]; J. Wong-Leung[3]; M. S. Janson[2]; M. K. Linnarsson[2]; H. K. Nielsen[2]; A. Yu Kuznetsov[1]; G. Alfieri[1]; U. Grossner[1]; E. V. Monakhov[1]; C. Jagadish[3]; J. Grillenberger[1]; [1]University of Oslo; [2]Royal Institute of Technology; [3]Australian National University

In order to realize SiC-devices for commercial use a processing technology compatible with large-scale production needs to be established. In this context, different key research areas have been identified; one being selective area doping which is a prerequisite for genuine implementation of a planar device technology. Ion implantation is, in principle, ideally suited for selective area doping of SiC but suffers from the inherent limitation of damage formation destroying the crystalline structure of the implanted layer. Indeed, it constitutes a major scientific challenge to accomplish a highly doped layer with complete electrical activation, shallow dopant levels, and a minimum of defects; this holds, in particular, for p-type doping of SiC. In this contribution, we intend to give a survey of the current status of ion implantation processing of SiC and issues like range profiles (an accurate and fast empirical profile simulator based on more than 150 experimental profiles has recently been established), flux and implant temperature, post-implant annealing/activation and surface morphology, co-implantation and nitrogen donor deactivation, effect of substrate orientation on defect evolution, long distance defect migration, and the use of implanted transition metals (e.g., Pt) to obtain semi-insulating layers and to control carrier lifetime, will be discussed.

10:10 AM Coffee Break

MB1. Bulk Growth I

Monday, 10:45am-12:25pm
September 19, 2005

Room: Allegheny Ballroom I
Location: Westin Pittsburgh

Session Chairs: C. H. Carter, Jr., Cree, Inc.; R. Madar, INPG/CNRS

10:45 AM Invited
The Spatial Distribution of Defects in Dependence on the Seed Polarity and Off-Orientation During the Growth of 4H – SiC Single Crystals: *Hans-Joachim Rost*[1]; Martin Schmidbauer[1]; Dietmar Siche[1]; [1]Institute for Crystal Growth

Defect distribution in dependence on the polarity and off-orientation during the growth of 4H – SiC single crystals was investigated. Micropipe density (MPD), stacking fault density (SFD) and dislocation density (DD) were determined for 2" 4H - SiC single crystals grown in <000-1> direction 0 - 7° off to <11-20> respectively for crystals up to 1" in diameter grown in <11-20> (a) and <1-100> (m) directions and using repeated a – face growth. KOH- etching, optical microscopy and X-ray topography were used for the characterization. It is shown that the MPD and DD decrease with increasing off-orientation of the seed for the growth in polar directions. A similar behaviour was found for the SFD and DD in non-polar directions with off- orientation to c-direction. Nevertheless, while the DD could be reduced up to three orders of magnitude for the growth along non-polar directions compared with that in c-direction where the DD remains nearly constant, the SFD was continuously increasing. Additionally, there are differences in the average level of these defects. The observed defect distribution will be discussed in terms of growth related and kinetic aspects.

11:15 AM
Micropipe-Free Single Crystal Silicon Carbide (SiC) Ingots via Physical Vapor Transport (PVT): *Cem Basceri*[1]; Igor Khlebnikov[1]; Yuri Khlebnikov[1]; Monica Sharma[1]; Peter Muzykov[1]; George Stratiy[1]; Murat Silan[1]; Cengiz Balkas[1]; [1]INTRINSIC Semiconductor Corp.

The move towards commercialization of SiC based devices places increasing demands on the quality of the substrate material. While the industry has steadily decreased the micropipe (MP) levels in commercial SiC wafers over the past years, achievement of wafers that are entirely free of MPs marks an important milestone in commercialization of SiC based devices. We present the results of a fundamental study into mechanisms controlling the nucleation and propagation of MP defects in SiC ingots via PVT. We illustrate how polytype instability, can be suppressed to reduce and eliminate MP generation. Our studies confirm that during SiC bulk growth, foreign polytype nucleation such as 3C-polytype generally occurs at the initial stages of growth (nucleation period) and/or during subsequent growth in the presence of facets. Centered on this key concept, an innovative MP annihilation process was developed and tested in our conducting 4H-SiC wafer production line. Statistical analysis from over 50 runs lead to a fine-tuned growth process condition that resulted in MP-free (zero MP density) conducting 4H-SiC ingots. We believe that the results presented here correspond to the first report of micropipe free SiC ingots via a commercially viable PVT process.

11:30 AM
Basal Plane Dislocation Dynamics in Highly p-Type Doped Versus Highly n-Type Doped SiC: *Peter J. Wellmann*[1]; Désirée Queren[1]; Ralf Müller[1]; Sakwe Aloysius Sakwe[1]; Ulrike Künecke[1]; [1]Materials Department 6

Stacking fault generation is known to be one of the most severe lifetime limiting and performance killing defects in SiC bipolar electronic devices. In this paper we report for the first time on the comparison of generation and annihilation dynamics of basal plane dislocations in highly p-type doped versus highly n-type doped SiC. Slip of basal plane dislocations is known to be one of the major causes for stacking fault propagation in SiC. Using KOH defect etching we have observed that basal plane dislocations are absent or at least appear significantly less pronounced in p-type SiC. In a systematic study to address dislocation dynamics we have performed crystal growth experiments with an alternating doping sequence using the M-PVT technique: initial 1/3 of the crystal p-type / middle 1/3 of the crystal n-type / final 1/3 of the crystal again p-type. We found that the dislocation density with pronounced basal plane component dramatically increases in the n-type doped region and considerably decreases again in the subsequent p-type doped area, indicating that thermo-elastic strain relaxation takes place using different dislocation types and slip systems in n-type and p-type SiC. From these experimental result an electronically driven dislocation dynamics in SiC is derived.

11:45 AM
Growth of Micropipe Free SiC Crystals on 4H-SiC {03-38} Seed: *Tomoaki Furusho*[1]; [1]SiXON Ltd.

We have developed the crystal growth on 4H-SiC {03-38} to achieve micropipe and stacking fault free crystals. 4H-SiC {03-38} is obtained by inclining the c-plane to <01-10> at a 54.7º angle and semi-equivalent to 3C-SiC {100}. When a wafer cut from an ingot grown on the 4H-SiC {03-38} seed crystal was characterized by molten KOH etching, no etch pits originated

from micropipes were observed. It was reported that even if there were micropipes in the 4H-SiC {03-38} wafer, all micropipes were dissociated to screw dislocations during the epitaxial growth. The 4H-SiC {03-38} crystal has many advantages in the crystal growth. Moreover, since the 4H-SiC {03-38} crystal is semi-equivalent to 3C-SiC {100}, inerface state density of MOS structure on the 4H-SiC {03-38} crystal is lower than that on the conventional c-plane. We will characterize devices fabricated on micropipe free crystals grown on the 4H-SiC {03-38} seed.

12:00 PM
Enhanced Carrier Lifetime in Bulk-Grown 4H-SiC Substrates: *Jason Jenny*[1]; Dave P. Malta[1]; Valeri T. Tsvetkov[1]; Mrinal Das[1]; H. McD. Hobgood[1]; Calvin H. Carter[1]; [1]Cree Inc

To devise a means of circumventing the cost of thick SiC epitaxy to generate drift layers in PIN diodes for >10kV operation, we have endeavored to enhance the minority carrier lifetimes in bulk-grown substrates. In this report, we discuss the results of a process that has been developed to enhance minority carrier lifetimes to in excess of 30 µs in bulk-grown 4H-SiC substrates. Measurement of lifetimes was principally conducted by microwave-photoconductive decay (m-PCD). Confirmation of the m-PCD lifetime result was obtained by electron beam induced current (EBIC) measurements. Additionally, deep level transient spectroscopic analysis of samples subjected to this process suggests that a significant reduction of deep level defects in general and of Z1/Z2, specifically, may account for the significantly enhanced lifetimes. Finally, a study of operational performance in devices employing drift layers fabricated from substrates produced by this process confirmed ambipolar lifetimes in the microsecond range.

12:15 PM Introduction to Invited Poster (Extended Defects I)
Structure of Carrot Defects in 4H-SiC Epilayers: Xuan Zhang[1]; S. Ha[1]; M. Benamara[1]; M. Skowronski[1]; J. J. Sumakeris[2]; M. J. Paisley[2]; M. J. O' Loughlin[2]; [1]Carnegie Mellon University; [2]Cree Inc.

12:20 PM Introduction to Invited Poster (EPI I)
4H-SiC Epitaxial Growth on Carbon-Face Substrates with Reduced Surface Roughness: *Takashi Aigo*[1]; Mitsuru Sawamura[1]; Tatsuo Fujimoto[1]; Masakazu Katsuno[1]; Hirokatsu Yashiro[1]; Hiroshi Tsuge[1]; Masashi Nakabayashi[1]; Taizo Hoshino[1]; Noboru Ohtani[1]; [1]Nippon Steel

MB2.Unipolar Devices & Detectors

Monday, 10:45am-12:25pm
September 19, 2005

Room: Allegheny Ballroom II & III
Location: Westin Pittsburgh

Session Chair: S. Dimitrijev, Griffith University

10:45 AM Invited
SiC Device Applications: Identifying and Developing Commercial Applications: *Jon Mark Hancock*[1]; [1]Infineon Technologies NA

Silicon carbide brings well known highly desirable physical and electrical properties to components for power conversion applications. While many esoteric low volume applications are being explored in the aerospace and specialized industries, more widespread commercial success will be dependent on several factors, including the development of devices ideally suited for targeted high volume applications for which existing semiconductor solutions fall short of the achievement of system performance targets. The challenge in accomplishing this is addressing both the immediate application technical issues, addressing commercial cost viability, and also surmounting market perceptions regarding the suitability of high voltage semiconductors in high reliability applications as diverse as computing server and telecom power supplies, or automotive hybrid vehicle power conversion. Clear cut advantages are achieved with SiC for power conversion in the 400-600V area, resulting in the ability to drastically scale power density and thermal density in "consumer" grade systems. Details of the component requirements and the affect on system configuration and performance will be discussed for power conversion applications in both offline AC power and automotive applications, and industry inputs regarding component reliability and de-rating will be presented.

11:15 AM
10kV, 106 mΩcm² Normally-Off 4H-SiC Vertical Junction Field-Effect Transistor: Yuzhu Li[1]; Petre Alexandrov[2]; Jianhui Zhang[2]; Larry X. Li[2]; *Jian H. Zhao*[1]; Ming Su[1]; [1]Rutgers, State University of New Jersey; [2]United Silicon Carbide, Inc.

SiC JFET, compared with SiC MOSFET, is attractive for high power, high temperature applications because it is free of oxide reliability issue. Trenched-and-Implanted Vertical Junction Field-Effect Transistor (TI-VJFET) does not require epi-regrowth and is capable of high current density. High voltage (=10kV) normally-off TIVJFET has been reported before based on 120um, 4.9x1014cm-3 doped drift layer. In this paper, we present a TI-VJFET with a thinner and more heavily doped (100um, 6x1014cm-3) drift layer, resulting in a blocking voltage VB in excess of 10kV and a forward current density of 23A/cm² at a drain voltage of 2V, corresponding to an apparent specific on-resistance RSP_ON equal to 87 mOcm². By correcting the current spreading outside of the active area of the device with the help of computer simulations, the corrected RSP_ON is 106 mOcm² and corresponds to a ratio of VB2/RSP_ON equal to 943 MW/cm², which is believed to be the highest value for any type of SiC field-effect transistors reported to date.

11:30 AM
Correlation Between Leakage Current and Defects Induced by Ion Irradiation in 4H-SiC Schottky Diodes: *Vito Raineri*[1]; Fabrizio Roccaforte[1]; Lucia Calcagno[2]; [1]CNR-IMM; [2]Dipartimento di Fisica

Schottky diodes are the most rife devices currently developed on SiC. Their performances are nearly ideal while their reliability is high. Therefore, they can be used as a reliable instrument to investigate properties of material trying to correlate them with device characteristics. In particular, ion irradiation of SiC devices can be of high interest due both the fundamental implications and the need of information when applying them to hostile environment or directly as detectors.We fabricated Schottky diodes of several areas up to 1 mm² and we irradiated them. Several diodes were fully characterised by I-V from room temperature up to 300°C. In spite of the large variety of defects introduced the leakage current behaviour reported in an Arrhenious plot shows a quite well defined value of 0.64 eV. DLTS on the same diodes allowed us to demonstrate the presence of several generation centres, including a 0.69 eV that seems the only responsible of the leakage current in the devices. This centre (Z1/Z2) has been associated in literature to a couple Si and C vacancies. The forward curves behaviour was associated to the formation of an intrinsic layer (measured by SCM) in the epitaxial region enlarging with increasing the irradiated dose.

11:45 AM
Fabrication of 4H-SiC p-Channel MOSFETs with High Channel Mobility: *Mitsuo Okamoto*[1]; Mieko Tanaka[1]; Tsutomu Yatsuo[1]; Kenji Fukuda[1]; [1]National Institute of Advanced Industrial Science and Technology

We have fabricated 4H-SiC p-channel MOSFETs and characterized their electronic properties aiming for SiC CMOS application. In this study, the influence of the gate oxidation process was investigated. MOS gate oxide was formed under three conditions: (i) dry oxidation at 1200°C, (ii) dry oxidation 1200°C following wet re-oxidation at 950°C, and (iii) wet oxidation at 1200°C. The peak value of the channel mobility (μ_{FE}) of the fabricated 4H-SiC p-channel MOSFETs was 10.3cm²/Vs for a dry oxidation, 12.5cm²/Vs for a dry oxidation following wet re-oxidation and 15.6cm²/Vs for a wet oxidation, respectively. P-type 4H-SiC MOS capacitors were also fabricated using p-type 4H-SiC substrate in order to investigate the MOS interface states around the valence band. The D_{it} obtained from CV curves on the p-type MOS capacitors by hi-lo technique was largest for dry oxidation and smallest for wet oxidation. From these results, it is supposed that the MOS interface with lower D_{it} near the valence band has higher μ_{FE}. The μ_{FE} of 15.6cm²/Vs for a wet oxidation is the highest value among previous reports on SiC p-channel MOSFETs, to my knowledge.

12:00 PM
Demonstration of a 4H SiC Betavoltaic Cell: *MVS Chandrashekhar*[1]; Christopher Ian Thomas[1]; Hui Li[1]; Michael Gregg Spencer[1]; Amit Lal[1]; [1]Cornell University

A betavoltaic cell in 4H SiC is demonstrated. An abrubpt p-n diode structure was used to collect the charge from a 1mCi Ni-63 source. An open circuit voltage of 0.95V and a short circuit current density of 8.8 nA/cm2 were measured in a single p-n junction. An efficiency of 3.7% was obtained. A simple photovoltaic type model was used to explain the results. Good correspondence with the model was obtained. Fill factor and backscattering effects were included as well. Efficiency was mainly limited by edge and surface recombination.

Lunch

Monday, 12:40-1:50pm
September 19, 2005

Room: Spirit of Pittsburgh
Location: Convention Center

MP.Monday Poster Session

Monday, 1:50-4:10pm
September 19, 2005

Room: Spirit of Pittsburgh Foyer
Location: Convention Center

MPG1.Bulk Growth I

Resistivity Distribution in Undoped 6H-SiC Boules and Wafers: *Qiang Li*[1]; Alexander Y. Polyakov[1]; Marek Skowronski[1]; Edward K. Sanchez[2]; Mark J. Loboda[2]; Mark A. Fanton[3]; Timothy Bogart[3]; Richard D. Gamble[3]; N. B. Smirnov[4]; Yu Makarov[5]; [1]Carnegie Mellon University; [2]Dow Corning Compound Semiconductor; [3]Pennsylvania State University; [4]Institute of Rare Metals, Russia; [5]Semiconductor Technology Research, Inc.

SIMS, Hall measurements, contactless resistivity mapping (COREMA), deep level transient spectroscopy (DLTS) and optical DLTS (ODLTS) measurements were performed on undoped semi-insulating (SI) and lightly nitrogen doped conducting 6H-SiC crystals grown by physical vapor transport (PVT) method. The concentration of all electron and hole traps, as well as nitrogen concentration strongly decrease when moving from the seed to the tail and from the center to the periphery of SiC boules. Radial distribution of resistivity in commercial SI-SiC wafers show several types of non-uniformities, the two most frequently observed ones being the U-shape and the inverted U-shape distributions. Possible reasons for the observed variation include systematic stoichiometry shift from Si-rich toward stoichiometric composition along the growth axis, increase of growth temperature from seed to tail and from center to periphery of the boule, and orientation dependent incorporation of nitrogen. The results of growth modeling using "Virtual Reactor" software package indicate the major role played by the stoichiometry change during growth.

Characterization of Bulk <111> 3C-SiC Single Crystal Grown by the CF-PVT Method: *Laurence Latu-Romain*[1]; Didier Chaussende[1]; Carole Balloud[2]; Jean Camassel[2]; Laetitia Rapenne[1]; Etienne Pernot[1]; Michel Pons[1]; Roland Madar[1]; [1]INPGrenoble - CNRS; [2]Université des Sciences et Techniques du Languedoc

According to its excellent intrinsic properties, the 3C-SiC polytype should be more and more considered in the forthcoming years. 3C-SiC single crystals have never been reported up to now because of the formation of DPB (Double Positioning Boundary) when starting from a hexagonal <0001> seed. With adapted nucleation conditions, we have been able to grow by the CF-PVT method a 0.4 mm thick 3C-SiC single crystal almost free of DPB on a 30 mm diameter seed. The as-grown morphology observed by AFM presents a step-and-terrace structure, which reveals a 2D growth mode. Large EBSD maps confirm that the surface is free of DPB and free of hexagonal inclusions. Cross-sections of the sample are observed by cross-polarized optical microscopy both close to the interface and close to the surface. These observations clearly evidence an improvement of the structural quality vs thickness. The LTPL spectrum collected at 5K presents a nice resolution of near band edge features (with phonon replicas) which evidence the high (electronic) quality of the material. A comparison of this CF-PVT material with state of the art 3C-SiC will be given. Then, the possibility to improve the CF-PVT process will be discussed.

The Reduction of Defects by Thermal and Surface Control in Initial Growth Stage for Large Diameter (> 2.5 inches) SiC Crystal Growth: *Soo-Hyung Seo*[1]; Joon-Suk Song[1]; Tae-Sung Kim[1]; Myung-Hwan Oh[1]; [1]Neosemitech Corporation

We present the novel method for the control of growth behavior by thermal control in initial growth stage in order to reduce the growth-induced defects of micropipes and planar cavity. And we demonstrate the availability for improving the crystal quality as the polishing process is applied. 6H-SiC crystals of above 2.5 inches in diameter were grown on 2 inches seeds manufactured by using mechanical polishing and chemo-mechanical polishing. The effect of applying intermediate disk between graphite lid and seed was investigated for management of radial temperature gradient. The different growth behaviors reveal as applying mechanical(M)-polished seed and chemo-mechanical(CM)-polished seed, respectively. While the smooth surface exhibited on a CM-polished seed, many plateaus with 5 mm in diameter were formed on the M-polished seed. These plateaus enlarged from undesirable nuclei should be coalescenced during the growth, and then the planar cavity and micropipe should be generated in the united plateau. In addition, the macrodefects were reduced by adopting the intermediate disk because this disk acts as a role in regulation of radial temperature gradient and prevents the reverse sublimation from seed surface. For future works, we demonstrate the novel results of applying the intermediate disk as the disk thickness and disk materials.

Processing of Poly-SiC Substrates with Large Grains for Wafer-Bonding: *Guy Chichignoud*[1]; Laurent Auvray[1]; Elisabeth Blanquet[1]; Mikhail Anikin[1]; Etienne Pernot[1]; Jean-Marie Bluet[2]; Michel Mermoux[1]; Catherine Moissan[3]; Fabrice Letertre[4]; Michel Pons[1]; Roland Madar[1]; [1]INPGrenoble; [2]INSA-Lyon; [3]NOVASiC; [4]SOITEC

The transfer by wafer-bonding of single-crystalline SiC thin films to a polycrystalline SiC support to obtain a "quasi-wafer" is an attractive alternative source. The generic nature of the Smart-Cut process (SOITEC Company), based on ion implantation and wafer bonding is now recognized through successful demonstrations of Si, III-V and SiC thin film transfers. Currently, 3C-SiC CVD wafers, with a fine grain structure (grain size around 5µm) and highly textured, are used. However, it is difficult to use the Chemical – Mechanical – Polishing technique (Epi-Ready process of NOVASiC) to obtain surfaces with a very low roughness as for single crystals. In the literature, there is no systematic study of high temperature and high growth rate (> 100 µm/h) processing of polycrystalline SiC by vapor deposition. In this paper, the evaluation and polishing of large poly-SiC grains processed by the classical PVT technique and the CF-PVT one at high growth rate were investigated with the aim to fabricate low roughness (< 5 nm) and low bow (> 3 µm) substrates able to fulfill the constraints of wafer bounding. For this preliminary research study, 2" substrates were processed.

The Effect of Aluminum Nitride-Silicon Carbide Alloy Buffer Layer on the Sublimation Growth of Aluminum Nitride on SiC (0001) Substrates: *Zheng Gu*[1]; Peng Lu[1]; James H. Edgar[1]; [1]Kansas State University

The benefits of depositing an AlN-SiC alloy transition layer on SiC substrates for the seeded growth of bulk AlN crystals were examined. The presence of the AlN-SiC alloy crystal layer helped to suppress the SiC decomposition by providing vapor sources of silicon and carbon. It enabled a higher growth temperature, and hence a higher growth rate and better quality crystals. In addition, cracks in the final AlN crystals can be avoided because AlN-SiC alloys have intermediate lattice constants and thermal expansion coefficient. AlN-SiC alloys were firstly grown on different polytypes of SiC substrate by the sublimation-recondensation method. Then pure AlN crystals were grown upon those at 1850-2000°C. For comparison, AlN crystals were directly grown on SiC substrates under the same conditions. X-ray diffraction (XRD) confirmed the formation of pure single crystalline AlN layer upon AlN-SiC alloy on SiC substrate, and established the orientational relationship between them. The substrate misorientation ensured that the alloy crystals grew two dimensionally with obvious cracks, as identified by scanning electron microscopy (SEM). Its presence effectively inhibited the appearance of cracks in the resultant AlN crystals. Defect selective etching in molten KOH demonstrated the high quality of the final AlN crystals.

High Quality SiC Crystal Grown by Physical Vapor Transport Method with New Crucible Design: *Byoung-Chul Shin*[1]; Jung-Kyu Kim[1]; Kap-Ryeol Ku[1]; Jung-Doo Seo[1]; Chi-Kwon Park[1]; Won-Jae Lee[1]; Geun-Hyoung Lee[1]; Il-Soo Kim[1]; [1]Dongeui University

The present research was aimed to systematically investigate the dependence of SiC crystal quality and yield during PVT growth on various crucible designs modified with graphite materials and tantalum-foils. Before the actual experiment, we carried out simulations using a specialized software tool, Virtual Reactor, for SiC crystal boules resulted from the modification of crucible and insulation felt structure with graphite materials and tantalum-foils. According to simulation result, we prepared SiC crystal with using sublimation PVT technique and then systematically investigated the SiC crystal quality controlled by new crucible designs. The growth rate of 2-inch SiC crystal grown in this study was about 0.3~0.5mm/hr. Typical absorption spectrum of SiC crystal indicated that the SiC polytype exhibited n-type 6H-SiC, the fundamental absorption energy and below-bandgap absorption energy of this SiC crystal were 3.02 and 1.97 eV, respectively. The doping concentration level of below ~10^{17}/cm^3 was extracted from the absorption spectrum and Hall measurement. The defect density such as micropipe and inclusion in SiC crystal boules with crucible design was systematically investigated. Finally, we observed the improvement of crystal quality through the introduction of new designs into the crucible.

The Obtaining (SiC) 1-X (AlN) X Semiconductor Solid Solutions Layers by Magnetron Sputtering Method: *Malik Kurbanov*[1]; [1]Daghestan State University

The results of obtaining of (SiC)1-x (AlN)x solid solutions layers by magnetron sputtering method are submitted. The study of layers composition, structure and optical transmission are carried out. The opportunity of monocrystal (SiC)1-x(AlN)x, layers obtaining on 6H-SiC substrates at T≥1000°C is shown. The edge of optical absorption is displaced in ultraviolet area with AlN content increasing in the solid solution.

The Influence of SiC Powder Source in 6H-SiC Single Crystals Grown by the Sublimation Method: *Jae Woo Kim*[1]; Soo-Hyung Seo[1]; Joon-Suk Song[1]; Myung-Hwan Oh[1]; Tae-Sung Kim[1]; [1]NeosemiTech Corporation

We examined the influence of heat treatment for high-purity SiC powder in 6H-SiC crystal growth. All of 6H-SiC crystals grown under four different

baking conditions were single crystals. And it was found that the doping concentration was decreased as either to increase baking temperature or time. It was also found that the micropipes were extended as the increase of baking time, because the surface of SiC powder was significantly graphitized. A 6H-SiC crystal grown by using SiC source treated under 2100°C for 6 hours revealed the best result of relatively low micropipes. For the effects of baked sources on the enhancement of single crystal growth, it could be explained that both the formation of alpha phase (Si/C ratio ~ 1) transformed from high-purity beta-SiC powder and the elimination of free metallic silicon in SiC powder had an influence on the removing silicon droplets resulting in random orientation at initial growth stage.

Growth and Characterization of AlN Single Crystals: *Shaoping Wang*[1]; Michael Dudley[2]; Andy Timmerman[1]; [1]Fairfield Crystal Technology; [2]SUNY at Stony Brook

AlN single crystal is a substrate material suitable for high quality III-V nitride epitaxy for a wide range of semiconductor devices, including blue lasers, high frequency devices and UV detectors. Physical vapor transport technique is a promising technique for growing large diameter AlN single crystals. AlN bulk crystal growth experiments are carried out and preliminary results from these experiments will be presented. The AlN crystals are grown using a sublimation physical vapor transport technique. The morphology of the AlN single crystals grown under various growth conditions is studied using optical microscopy and scanning electron microscopy. Selected AlN single crystals are studied using an X-ray double-crystal diffraction technique and Synchrotron White Beam X-ray Diffraction Topography technique. Defects identified in the AlN crystals in this study include dislocations, grain boundaries and inclusions.

Polytype Control in 6H-SiC Grown via Sublimation Method: *Xianxiang Li*[1]; Shouzhen Jiang[1]; Xiaobo Hu[1]; Xiangang Xu[1]; Minhua Jiang[1]; [1]Shandong University

15R-SiC is often parasitic with 6H-SiC grown via sublimation method. Its occurrence mainly depends on the solid-vapor interface shape and the crystal growth rate when the seed temperature was fixed at 2250°C. In order to interpret the relationship between occurrences of 15R-SiC and the solid-vapor interface shape in the growth of 6H-SiC, a model of the step flow mechanism has been proposed in this study. In addition, the effect of different growth rate on 15R-SiC parasite was studied in the experiment. The results show that the 15R-SiC occurs more easily on the convex and concave interface than on the slight convex interface at a low growth rate. But when the growth rate exceeds 300μm/h, 15R-SiC occurs at random even if the crystal was grown with slight convex interface.

PVT Growth at High Temperature; Novel Tunable Widebandgap Materials: *Narsingh Bahadur Singh*[1]; Brian Wagner[1]; David Knuteson[1]; Darren Thomson[1]; Michael Aumer[1]; Andre Berghmans[1]; Jack Hawkins[1]; [1]Northrop Grumman, ES

Aluminum nitride (AlN) and Gallium nitride (GaN) have become important wide bandgap semiconductors because of their excellent properties for high power microwave devices, competing with GaAs and Si in terms of gain, power output and efficiency at low frequency, and promising even better performance at the higher frequencies. In particular, efficient, broad-band power RF transmitters are needed with high efficiency and high linearity, as well as low noise rugged receivers for T/R modules. These nitrides are very difficult to grow as bulk single crystals because of decomposition into their elemental components at high growth temperature. The success of various systems depends on the availability of large diameter, low defect, and high quality nitride substrates at affordable prices. Single crystals of aluminium nitride were grown by physical vapor transport (PVT) method. Evaluation of transport conditions was carried out during bulk growth of pure and doped aluminium nitride in a vertical, cylindrical geometry. Experiments were carried out for the conditions in which we varied thermal gradients (TH - TC = 30 to 90ºC). Crystals grown at low thermal gradients and lower source temperature (below 2100ºC) showed dominantly needle morphology. As we increased the source temperature hexagonal morphology became dominant. These results along with preliminary results on pure and doped AlN will be presented.

Growth and Surface Morphologies of 6H SiC Bulk and Epitaxial Crystals: *Govindhan Dhanaraj*[1]; Yi Chen[1]; Michael Dudley[1]; Hui Zhang[1]; [1]Stony Brook University

Silicon carbide (SiC) is a potential semiconductor material to replace the conventionally used silicon crystal in certain critical device applications. Epitaxial growth based on chemical vapor deposition (CVD) is commonly used in fabricating these device structures. However the defects nucleated during the growth as well as the propagating micropipe dislocations from substrate to the epitaxial film need to be studied thoroughly and contained. We have developed a sophisticated PVT system and upgraded it as a CVD system with the aim to understand SiC growth kinetics and defect nucleation mechanisms during SiC deposition. As-grown surfaces of PVT crystal as well as epitaxial films deposited on SiC as well Si substrates using propane and silane/silicon tetrachloride as precursor gases have been studied using Nomarski Optical Microscopy, AFM and X-ray diffraction techniques. Interesting morphological features such as step flow pattern and their pinning at microppipes, spirals and hillocks have been observed. The details of the investigation and results will be presented.

MPG2.EPI I

Invited

4H-SiC Epitaxial Growth on Carbon-Face Substrates with Reduced Surface Roughness: *Takashi Aigo*[1]; Mitsuru Sawamura[1]; Tatsuo Fujimoto[1]; Masakazu Katsuno[1]; Hirokatsu Yashiro[1]; Hiroshi Tsuge[1]; Masashi Nakabayashi[1]; Taizo Hoshino[1]; Noboru Ohtani[1]; [1]Nippon Steel

Recently, the application of a site-competition technique to epitaxial growth on 4H-SiC Carbon-face (C-face) has been developed. It is difficult for the epitaxial growth, however, to achieve both the low residual donor concentration and the specular surface morphology because high C/Si ratio for the low residual donor concentration leads to crystal defects such as hillocks and pits. In this study, we report on the C-face epitaxial growth using 4H-SiC substrates with reduced surface roughness by mechanical polishing and in-situ HCl etching. The surface roughness (Rms) of the substrate in a 10×10 μm^2 area was 0.27nm after polishing and in-situ etching. The use of the smooth substrates made it possible to decrease the substrate temperature below 1550°C because the surface migration length became large. Consequently, the residual donor concentration could be kept below 1×10^{15} cm^{-3} even for low C/Si ratio, which was needed to suppress the generation of the crystal defects. It was demonstrated for the C-face epitaxial layer grown at the substrate temperature of 1550°C and at the C/Si ratio of 1.5 that the specular surface morphology with Rms of 0.26nm was obtained and the residual donor concentration was 6.7×10^{14} cm^{-3}.

Origin of Surface Morphological Defects in 4H-SiC Homoepitaxial Films: *Tatsuya Okada*[1]; Kouichi Okamoto[1]; Kengo Ochi[1]; Kouichi Higashimine[2]; Tsunenobu Kimoto[3]; [1]Tokushima University; [2]JAIST; [3]Kyoto University

Plan-view transmission electron microscopy (TEM) was applied to investigate the origin of morphological defects on the surface of homoepitaxial films that were grown on 4H-SiC (0001) crystals off-cut towards the [11-20] direction by 8°. From the elongated shape of the surface defects and their length along the off-cut direction, it was presumed that their origin existed at the substrate/epi-film interface. Hence, almost entire thickness of the epi-film was first removed by plasma etching and then the epi-crystal was thinned from the substrate side so that the electron transparent region of the plan-view TEM sample included the substrate/epi-film interface. Morphological features of the surface of epi-films remained unchanged even after the plasma etching process. Hence, one-to-one correspondence between surface defects and crystallographic defects was confirmed by comparing optical micrographs and TEM images. Defect structure associated with “carrot defects” was found. It was composed of stacking faults on the (0001) plane and partial dislocations bounding them. These defects originated from foreign particles at the interface. From X-ray energy-dispersive spectrometry, it was confirmed that particles contained zirconium (Zr). Selected area diffraction patterns showed that the particles were crystalline.

Simulation of Threading Edge Dislocation Images in X-Ray Topographs of Silicon Carbide Homo-Epilayers: *William M. Vetter*[1]; Hidekazu Tsuchida[2]; Isaho Kamata[2]; Michael Dudley[1]; [1]SUNY at Stony Brook; [2]Central Research Institute of Electric Power Industry

Among the types of dislocation seen in homo-epilayers of SiC grown upon 4H-SiC wafers with an 8° surface offcut are basal plane dislocations propagated into the epilayer at an 8° inclination, and threading edge dislocations. These types may be imaged by monochromatic synchrotron x-ray topography in the grazing-incidence reflection geometry using the 11-28 reflection. Equations needed to apply the ray-tracing method of computer simulating x-ray topographic defect images in this experimental geometry were derived and used to simulate images of the threading edge dislocations. Simulations of the threading edge dislocations showed 4 μm wide white ovals with narrow arcs of dark contrast at their ends, inclined relative to the g-vector of the topograph according to the sign of their Burgers vector. These resembled the experimental topographs, inasmuch as was possible at the maximum resolution of x-ray topographs.

Studies on the Selective Growth and In-Situ Etching of 4H-SiC Using TaC Mask: *Canhua Li*[1]; Ishwara Bhat[1]; Paul Chow[1]; [1]Rensselaer Polytechnic Institute

We have previously reported on the selective growth of 4H-SiC epitaxial layers on 4H-SiC substrates using TaC mask. Here, we present more systematic studies on the selective growth and in-situ selective etching of 4H-SiC using TaC masks. Epitaxial growth of SiC was carried out in a conventional, horizontal cold wall reactor. Bulk 4H-SiC with 8o miscut (0001) Si-face wafers were coated with Ta and patterned using standard photolithography. Ta was then converted to TaC by exposing Ta in propane/hydrogen ambient at 1300°C for 15 minutes. The morphological evolution during selective epitaxy

as a function of crystallographic orientation, growth temperature and C/Si ratio is analyzed. It was found that the growth window for selective growth was a function of the surface area covered by the TaC mask as well as the mask width between windows. We speculate that selective etching is related to the incomplete conversion of Ta to TaC, and evolution of atomic hydrogen at the Ta/SiC interface. Additional experiments with various Ta metal thickness, TaC conversion time, temperatures and growth conditions are being carried out to develop a robust process for selective growth. This will be an enabling process for the development of advanced power semiconductor devices in SiC.

CVD Epitaxial Growth of 4H-SiC on Porous SiC Substrates: *Y. Shishkin*[1]; Yue Ke[2]; Fei Yan[2]; R. P. Devaty[2]; W. J. Choyke[2]; S. E. Saddow[1]; [1]University of South Florida; [2]University of Pittsburgh

We report on the growth of CVD homoepitaxial SiC films on substrates with 5 µm and 10 µm thick porous layers on their surface. A part of each substrate was left unetched to be used as a control. The growth was conducted in a horizontal hot-wall CVD reactor at 1580°C with the process pressure set to 150 Torr. The precursor chemistry is silane-propane-hydrogen. The precursor flow rate was varied (Si/C ratio is maintained constant for all the experiments) to obtain growth rates from 12 to 30 µm/h. We will describe in detail the technique of growing on porous SiC substrates leading to epitaxial films of specular and microscopically smooth morphology. The structural quality of the films was analyzed by secondary electron microscopy (SEM) and X-ray diffraction (XRD). Low temperature photoluminescence (LTPL) was used to study the presence of point defects. We show that the epitaxial layer quality was improved when growing on porous vs. non-porous substrates regardless of the thickness of the porous layer and the epi growth rate.

Stability of Thick Layers Grown on (1100) and (1120) Orientations of 4H-SiC: *Mikael Syväjärvi*[1]; Rositza Yakimova[1]; A. Arjunan[2]; E. Toupitsyn[2]; T. Sudarhsan[2]; [1]Linköping University; [2]University of South Carolina

In (0001) epitaxy threading defects cause difficulties in devices. These may be reduced by growth on (1100) and (1120) orientations of SiC. Smooth surfaces have been obtained in (1120) epitaxy while (1100) epitaxy is difficult due to an increased sensitivity to growth stability. We have grown thick layers up to 90 µm with growth rate up to 180 µm/h by sublimation epitaxy. The growth rate dependence for (1120) and (1100) epitaxy are compared with (0001) epitaxy, the slopes in the Arrhenius plot are similar, thus the rate limiting mechanism would be sublimation of the source material. Therefore the surface kinetics may support stable (1100) growth. The surfaces on (1100) layers with thickness 35, 60 and 90 µm are smooth and typical elongated defects having a length of hundreds of µm, observed in CVD layers grown on (1100) substrates are not observed, even though the thicknesses are much greater than the ones in the CVD layers (5 µm). The details on the surfaces are obtained from AFM measurements and these are used to discuss the stability and growth mechanisms related to sublimation epitaxy conditions on (1120) and (1100) orientations, even in thick layers grown at high growth rate.

High-Speed Homoepitaxy of SiC from Methyltrichlorosilane by CVD: *Peng Lu*[1]; James H. Edgar[1]; Orest J. Glembocki[2]; Paul B. Klein[2]; Evan R. Glaser[2]; Jesse Perrin[3]; Jharna Chaudhuri[4]; [1]Kansas State University; [2]Naval Research Laboratory; [3]Wichita State University; [4]Texas Tech University

Silicon carbide was deposited homoepitaxily at high growth rates (up to 90 µm/hr) with methyltrichlorosilane (MTS) as the precursor in chemical vapor deposition. The substrates were 6H- and 4H-SiC (0001) wafers with different misorientation tilts toward (1120). As the growth temperature increased from 1400°C to 1600°C, the deposited films' morphologies changed from rough, faceted grains to a smooth, mirror-like surface. Raman spectroscopy showed that the polytypes of the resulting films were affected by the substrate misorientation. When the 6H-SiC substrates were well-oriented, i.e. with the offset angle of less than 0.5°, 3C-SiC was deposited with numerous triangular stacking faults (TSFs). When the offset angle of substrates was 3.5°, mixtures of 3C- and 6H-SiC polytypes were deposited. When the offset angle was 8°, the epitaxial growth perfectly replicated the substrates' polytypes, i.e. high quality 6H- and 4H-SiC epilayers were generated on the 6H- and 4H-SiC substrates, respectively. The Full-Width Half-Maximum (FWHM) of x-ray diffraction rocking curves for the *c*-plane of pure smooth 6H- and 4H-SiC layers was in the range of 15 to 20 arcsecs. Photoluminescence (PL) confirmed that the 6H- and 4H-SiC layers were of good quality.

High Epitaxial Growth Rate of 4H-SiC using Horizontal Hot-Wall CVD: *R. L. Myers*[1]; Y. Shishkin[1]; O. Kordina[2]; I. Haselbarth[1]; S. E. Saddow[1]; [1]University of South Florida; [2]Caracal Inc.

A horizontal hot-wall CVD reactor with a growth rate of nearly 40 µm/h, capable of growth on whole wafers (50mm), has been established. The process consists of silane/propane/hydrogen chemistry operating at 150Torr and a growth temperature of 1560°C. The growth rate, as a function of process flow and pressure, was studied and is reported. 4H-SiC films were grown for up to two hours resulting in a thickness of 65 µm. The morphology of the thick films was specular with the presence of a few carrot type defects, as is typically encountered for thick epitaxial layers. The Si/C ratio, which produced the net carrier concentration for our process of approximately 2x10[15] cm^{-3}, was found to be 1.2. X-ray diffraction was used to confirm the high structural quality of the thick films. The FWHM of a rocking curve of the (0004) peak for the 65 µm thick film is approximately 11arcsec. Preliminary low temperature photoluminescence was conducted on some of the thinner films and the quality found to be comparable to the quality of films generally grown at lower growth speeds. Further details for the process described here as well as the photoluminescence results on thick films will be reported.

Effect of the Crystallization Conditions on the Epitaxial Relationship of Si Deposited on 3C-SiC(100): *Gabriel Ferro*[1]; E. K. Polychroniadis[2]; Dieter Panknin[3]; Wolfgang Skorupa[3]; John Stoemenos[2]; Yves Monteil[1]; [1]Laboratoire des Multimatériaux et Interfaces; [2]Aristotle University of Thessaloniki; [3]Forschungszentrum Rossendorf

The epitaxial relationship of Si deposit on 3C-SiC was studied using both free standing 3C-SiC(100) material from Hoya and 3C-SiC thin layers deposited on Si(100) as substrates. The conditions of Si growth were varied depending on the substrate. When Si is deposited at 1000°C on (001) 3C-SiC, it is in perfect epitaxial relation with the SiC layer [100]Si//[100]SiC and [001]Si//[001]SiC. After 20 ms flash lamp pulse on the same sample, which has the effect of fast melting of the Si top layer only, the defects in the Si are eliminated. Using free standing 3C-SiC, the deposition temperature was not limited by the Si melting point so that it was fixed at 1500°C in order to form a set of Si liquid droplets on the surface with diameter ranging from 5 to 20 µm. Surprisingly more than 60% of the Si droplets exhibit the epitaxial relation [110]Si//[001]SiC and [111]Si//[110]SiC. The occurrence of this new epitaxial relationship can be understood in terms of lattice mismatch reduction from 20% to 18.3%. The conditions of crystallization, most probably the cooling rate, seem to have a strong effect on Si orientation.

Transmission Electron Microscopy Investigation of the Role of Surface Steps in the Generation of Misfit Dislocations during MOCVD Growth of GaN on 4H-SiC: *Nabil D. Bassim*[1]; Mark E. Twigg[1]; Michael A. Mastro[1]; Charles R. Eddy[1]; Philip Neudeck[2]; Richard L. Henry[1]; Ronald N. Holm[1]; J. Anthony Powell[2]; Andrew Trunek[2]; [1]U.S. Naval Research Laboratory; [2]NASA Glenn Research Center

The development of GaN-based vertical devices with low-leakage currents deposited on SiC represents an important technological challenge for power applications. Threading dislocations have been identified as defects that contribute to such leakage. Through the use of patterned SiC substrates that have regions that are free of surface steps, we have previously reported the growth of high-quality GaN heteroepitaxial films with threading dislocation densities on the order of 107/cm2. In addition to the low-defect densities, we have observed a defect substructure in which lateral a-type dislocations annihilate early in the GaN growth. This study will focus further on the role of substrate surface steps in the generation of misfit, a-type, and threading dislocations at the heteroepitaxial interface. By using weak-beam imaging from plan-view TEM samples of stepped and unstepped mesas, we show dislocations generated on hillocks and flat surfaces and compare their geometries, showing that flat surfaces are confined to one set of a-type Burgers vectors and thus much more likely to annihilate. Dislocations from a hillock have more options for plastic flow and are thus more likely to generate barriers to dislocation glide. We suggest an annihilation mechanism based on step-geometry and step prevalence.

Surface Morphology of GaN Films Grown by RF-Plasma MBE using Lateral Overgrowth and Low-Temperature Ga-Rich Condition: *Hiroshi Chonan*[1]; Mitsuaki Shimizu[2]; Guanxi Piao[2]; Hajime Okumura[2]; Mutsumi Sugiyama[1]; Hisayuki Nakanishi[1]; [1]Tokyo University of Science; [2]National Institute of Advanced Industrial Science and Technology

By employing the high temperature growth, we enhanced the lateral overgrowth in RF–plasma MBE, and improved the crystal quality grown on the sapphire substrate. Due to the lateral overgrowth we observed the enlargement of the grain size. Grains of GaN in the film are enlarged up to 2 µm in diameter, which indicates the density decrease of the threading dislocations. We measured FWHM of the peak in asymmetry refection XRC as a function of the epilayer and found the reduction of the FWHM even though the epilayer is thin. The shortest value was 394 arcsec that is comparable value with that of MOCVD-grown wafers. Further, to planarize the surface the low temperature Ga-rich growth process was employed at the end of the growth procedure, and the good flat surface morphology was obtained. We also found the surface morphology depends not only on the growth conditions but also on the background carrier density.

Homoepitaxial Growth of 4H-SiC Using a Chlorosilane Silicon Precursor: *Michael F. MacMillan*[1]; Mark Loboda[1]; Eric Carlson[1]; Gilyong Chung[1]; [1]Dow Corning Compound Semiconductor Solutions

Silicon carbide homoepitaxy using a chlorosilane-based silicon precursor and a hot wall CVD system has been investigated. A design of experiments approach has been employed to optimize the CVD epitaxy process for the growth of low-doped (<5E14/cm^3), uniform films suitable for fabrication of power devices. Temperature, pressure and gas composition were controlled in the study. In the process space examined, a range of SiC film morphology

was observed – from diffuse to specular – with the optimal conditions evidencing wafer crystal defect overgrowth. Using a chlorosilanes/propane chemistry high growth rates (approaching 20 um/hr) and very high resistivity layers (net doping<3E14/cm^3) have been produced with uniformity in line with device fabrication targets. Characterization of the epitaxial layers using simple Schottky devices has been used to further define the preferred process conditions for growth of device structures, with optimal conditions leading to 75%+ yields on 2 mm diameter diodes. Failure analysis of the Schottky devices indicates the best epitaxy process conditions are capable to convert basal plane wafer defects to threading dislocations in the epitaxial layer.

N-Doping of Polycrystalline 3C-SiC Films Deposited by LPCVD: *Xiaoan A. Fu*[1]; Jacob Trevino[1]; Mehran Mehregany[1]; Christian A. Zorman[1]; [1]Case Western Reserve University

This paper reports the effect of deposition temperature on the deposition rate, residual stress, and resistivity of nitrogen-doped (N-doped) poly-SiC films deposited by LPCVD. N-doped poly-SiC films were deposited in a high-throughput, resistively-heated, horizontal LPCVD furnace capable of holding up to 100, 150 mm-diameter substrates using SiH2Cl2 (100%) and C2H2 (5% in H2) precursors, with NH3 (5% in H2) as the dopant gas. The deposition rate increased, while the residual stress decreased significantly as the deposition temperature increased from 825 to 900ºC. The resistivity of the films decreased significantly from 825°C to 850°C. Above 850ºC, although the resistivity still decreased, the change was much smaller. XRD patterns indicated a polycrystalline (111) 3C-SiC texture for the films deposited in the temperature range studied. SIMS depth profiles indicated a constant nitrogen atom concentration of 2.6 x 1020/cm^3 in the intentionally doped films deposited at 900°C. The nitrogen concentration of unintentionally doped films (i.e., when NH3 gas flow was zero) deposited at 900°C was on the order of 1017/cm^3. Films deposited at 900°C exhibited a resistivity of 0.0172 Ω-cm and a tensile residual stress of 59 MPa, making them very suitable for use as a mechanical material supporting MEMS device development.

Growth Acceleration in FLASiC Assisted Short Time Liquid Phase Epitaxy by Melt Modification: *Jörg Pezoldt*[1]; Fransisco Morales[1]; Thomas Stauden[1]; Christian Förster[1]; Elias Polychroniadis[2]; Jon Stoemenos[2]; Dieter Panknin[3]; Wolfgang Skorupa[3]; [1]TU Ilmenau; [2]Aristotele University Thessaloniki; [3]FWHIM, Institute for Ion Beam Physics and Material Science, FZ Rossendorf

The defect density of the SiC on Si results from the high defect density in the seeding layer formed by the carbonization and the thermal mismatch. The defect density can be reduced if the layer is annealed by flash lamps (the FLASiC process). To improve the situation further a multilayer stack of the type SiC/Si(SOL)/SiC can be used. It will be shown that Ge and C additions to the SOL are beneficial in this technique. They lead to an substantial increase of the mass transfer of the upper layer to the lower one observed by transmission electron microscopy investigations. If the Ge content of the SOL and the FLASiC conditions are properly chosen a homogeneous layer with a 3C-SiC thickness between 150 and 200 nm can be achieved corresponding to a growth rate between 7.5 and 10.0 µm/s. The thickening of the lower layer strongly depends on the SOL composition and is caused by the modification of the optical and mass transport properties. Ge and/or C incorporation into the SOL and therefore into the Si melt enhances the mass transport from the upper SiC layer to the lower one.

Improvement of 4H-SiC Selective Epitaxial Growth by VLS Mechanism using Al and Ge Based Melts: *Gabriel Ferro*[1]; Maher Soueidan[1]; Christophe Jacquier[1]; Philippe Godignon[2]; Joerg Pezoldt[3]; Thomas Stauden[3]; Mihai Lazar[4]; J. Monserrat[2]; Yves Monteil[1]; [1]Laboratoire des Multimatériaux et Interfaces; [2]Centro Nacional de Microelectrónica; [3]Zentrum für Mikro- und Nanotechnologien; [4]CEGELY

Al-Si and Ge-Si systems were studied for selective epitaxial growth (SEG) of 4H-SiC by Vapour-Liquid-Solid mechanism. Al-Si and Ge-Si bilayers stackings were deposited on 8° off, Si face, 4H-SiC substrates. After patterning of the layers, the samples were heated up to 1000°C and 1200°C respectively for Al-Si and Ge-Si stackings in order to melt the layers. Propane was introduced either during the initial heating ramp or after reaching the temperature plateau. It was found that introduction of propane during the heating ramp was a key parameter in order to improve the homogeneity of the deposit. In both cases, SEG of SiC was achieved. However, the best results were obtained with Ge-Si system giving smooth and uniform 300 nm thick epitaxial deposit on all the pattern sizes and shapes. On the other hand, with Al-Si system the deposit was less homogeneous and rougher.

6H-SiC Homoepitaxial Growth and Optical Property of Boron-and Nitrogen-Doped Donor Accepter Pair (DAP) States on 1°-Off Substrate by Closed-Space Sublimation Method: *Yohjiro Kawai*[1]; Tomohiko Maeda[1]; Yoshihiro Nakamura[1]; Motoaki Iwaya[1]; Satoshi Kamiyama[1]; Hiroshi Amano[1]; Isamu Akasaki[1]; Masahiro Yoshimoto[2]; Tomoaki Furusyo[3]; Hiroyuki Kinoshita[3]; Hiromu Shiomi[3]; [1]Meijo University; [2]Kyoto Institude of Technology; [3]SiXON Ltd.

DAP emission is promising for use as phosphors in a nitride-based light-emitting diode grown on donor- and acceptor-doped SiC homoepitaxial layers. However, for the growth of doped SiC epitaxial layers, a SiC substrate with a small off angle is preferable, because it is very difficult to obtain nitrides with smooth surfaces if they are grown on SiC with large off angles. We demonstrate high-speed homoepitaxial growth of high quality 6H-SiC epitaxial layer on a 1°-off substrate by a closed-space sublimation method. Under the high growth rate of 60 µm/h, a specular surface was obtained under optimized growth conditions. The crystallinity of the epitaxial layer was found to be improved by XRD measurement, where the FWHMs of the epitaxial layer and the substrate were 38 arcsec and 80 arcsec, respectively. In the photoluminescence spectrum of the boron- and nitrogen-doped SiC epitaxial layer, a visible emission peak at 570 nm was observed. The origin of this peak was DAP recombination between deep boron and nitrogen states. Without any optimization of the impurity concentrations, distinctly bright emission was obtained at room temperature. The DAP emission in the thick and high-quality SiC epitaxial layer seems to be suitable for optical device applications.

Multi-Scale Simulation of MBE-Grown SiC/Si Nanostructures: *Jörg Pezoldt*[1]; Yurii Trushin[2]; Kiril L. Safonov[3]; Alexander Schmidt[2]; Oliver Ambacher[1]; Vladimir Kharlamov[2]; [1]TU Ilmenau; [2]A.F. Ioffe Physico-Technical Institute; [3]St.Petersburg State Polytechnic University

The main obstacle for the implementation of numerical simulations for the prediction of the epitaxial growth is the variety of physical processes with considerable differences in time and spatial scales taking place during epitaxy: deposition of atoms, surface and bulk diffusion, nucleation of two-dimensional and three-dimensional clusters, etc. Thus it is not possible to describe all of them in frame of a single physical model. In the present work a multi-scale simulation of the epitaxial growth of silicon carbide nanostructures on silicon using three numerical methods, namely Molecular Dynamics (MD), kinetic Monte Carlo (KMC), and the Rate Equations (RE) was implemented. MD method was used for the estimation of kinetic parameters of atoms at the surface, which are input parameters for the other simulation methods. The KMC allowed the atomic-scale simulation of the cluster formation, which is the initial stage of the SiC growth, while the RE method gave the ability to study the growth process on a longer time scale. As a result, a full-scale description of the surface evolution during SiC formation on Si substrates was developed.

MPP1.Device Processing

Impurity Concentration Dependence of Recrystallization Process of the Phosphorus Implanted 4H-SiC(112-0): *Masataka Satoh*[1]; Tomoyuki Suzuki[1]; [1]Hosei University

In the present study, we investigated that the impurity concentration dependence of the recrystallization rate of the phosphorus implanted 4H-SiC(112-0). Samples used in the present study were p-type 4H-SiC(112-0). The phosphorus ions were multiply implanted to form the implantation layer with the thickness of 200 nm and the phosphorus concentration of 1 x 10^{20}, 4 x 10^{20}, and 1 x 10^{21} /cm^3, respectively. The isothermal annealing of the implanted samples were performed at the temperature range from 660 to 720°C in Ar gas flow using an infrared image annealer with a black SiC crucible. The recrystallization rate of the P ion implantation-induced amorphous layer in 4H-SiC(112-0) increases with an activation energy of 3.4 eV as well as the case of the Ar ion implantation-induced amorphous layer in 6H-SiC(112-0) and (11-00). As the P concentration is increased from 1 x 10^{20} to 1 x 10^{21} /cm^3, the recrystallization rate is enhanced from 3.5 to about 5nm/min, while the recrystallization rate for Ar implantation-induced amorphous layer was 1.5 nm/min. It is suggested that the recrysallizatioin process is enhanced by the presence of the substitutional impurity at the a/c interface during the recrystallization.

Fabrication of Low Resistive Layer in Diamond Surface by Ni Ion Irradiation at Low Doses using FIB: *Soichi Mejima*[1]; Tatsuya Arai[1]; Kazuyuki Hirama[1]; Hitoshi Umezawa[2]; Ferrer Domingo[1]; Takehiro Shinada[1]; Iwao Ohdimari[1]; Hiroshi Kawarada[1]; [1]Waseda University; [2]National Institute of Advanced Industrial Science and Technology

In this research, single crystalline diamond surface was locally irradiated with Ni, P and Pt ions at an acceleration voltage of 30 kV utilizing focused ion beam (FIB) attached Ni-P-Pt liquid metal ion source (LMIS). Ni ion was chosen in order to induce the phase transition (changing diamond phase to carbide phase) at low temperature because Ni ion has strong interaction with carbon. Irradiation was performed, held at substrate temperature (Ts) of 27°C (room temperature) to 200°C, with doses from 1 × 10^{15} to 1 × 10^{17} ions/cm^2. The sheet resistance and the specific contact resistance were measured by circular transmission line model (c-TLM) method at room temperature. Controlling the substrate temperature at 200°C, The sheet resistance of 0.50kΩ/sq. was obtained at 2×10^{15} ions/cm^{2}doses. At the same substrate temperature, Ohmic characteristics with a minimum specific contact resistance of 8×10^{-6} Ω cm^2 were obtained at 1×10^{16} ions/cm^2 doses.

Formation of Nanovoids Due to Thermal Annealing of MeV C Implanted Si and Their Role in Impurity Gettering: *Satyabrata Mohapatra*[1]; Boby Joseph[1]; Biswarup Satpati[1]; Durga Prasad Mahapatra[1]; [1]Institute of Physics,

Bhubaneswar

Carbon implantation into Si at 1 MeV to a dose of 2 x 10^{16} cm^{-2} followed by 2 h annealing at 1050°C has been found to result in the formation of buried SiC nanoclusters in Si. Cross-sectional transmission electron microscopy revealed the presence of amorphous SiC patches, β-SiC nanocrystals and nanovoids in the C implanted layer. The role of these amorphous SiC patches and the nanovoids formed from their conversion to β-SiC at high temperatures, has been studied regarding metal gettering using Au as an impurity. For this, Si substrates were implanted with 1.5 MeV Au^{2+} ions to a dose of 2.2 x 10^{15} cm^{-2} and annealed for 1 h at 850°C. These were subsequently implanted with C and annealed at different temperatures to look at trapped Au concentration in the C implanted layer using Rutherford backscattering spectrometry. A 2 h anneal at 1050°C has been found to result in Au accumulation in the C implanted layer with an efficiency going beyond 92%. The gettered Au fraction has been found to be thermally stable up to 1050°C beyond which there was a release. Some of these results will be presented and discussed.

Die Bonding Issues on Silicon Carbide Diodes: *Sang-Kwon Lee*[1]; Kyu-Chang Sim[2]; Sang-Gyun Hong[2]; Sung-Yong Choi[2]; Hak-Jong Kim[2]; Ki-Cheol Choi[1]; Seung-Yong Lee[1]; Wook Bahng[3]; Nam-Kyun Kim[3]; [1]Chonbuk National University; [2]SP Semiconductor & Communication Co.; [3]Korea Electrotechnology Research Institute

Die attachment is one of most crucial processes, especially in vertical structure devices, since the primary function of a die attach material is to secure a semiconductor chip to a leadframe or substrate, and to ensure it does not detach or fracture over an operational lifetime that may include many power and temperature cycle excursion. Here, we report the die bonding processes how the surface roughness and metallization schemes affect the process of die bonding in SiC device fabrication using a soldering test and die shear test (DST) with differently prepared SiC samples. One set of samples (FB#1 and FB#2) was capped with sequentially evaporated Ti and Au on annealed Ni layer. The other set of samples (FB#3 and FB#4) was prepared by 4μm-thick Au electroplating on annealed Ni layer. The quality of the soldering, such as the solder coverage, void, and adhesion, was characterized by optical microscope, X-ray microprobe, and DST, respectively. We found that the sample FB#2 had a satisfactory result for the test of solder coverage, void, and DST. But, the rest of samples were failed. The void taken by X-ray microprobe for the sample FB#2 was in the range of 1.2% to 4.7%.

Subsurface Damage Evaluation and Preparation of Damage Free Surfaces on Silicon Carbide: *William Everson*[1]; Volker Heydemann[1]; Rick Gamble[1]; David Snyder[1]; Greg Goda[1]; Marek Skowronski[2]; Josh Grim[2] Joan Redwing[1]; Jeremy Acord[1]; [1]Pennsylvania State University; [2]Carnegie Mellon University

A new chemical mechanical polishing process (ACMP) has been developed by the Penn State University Electro-Optics Center for producing damage free surfaces on silicon carbide substrates. This process is applicable to semi insulating and conductive wafers of 4H or 6H polytype. The process has been optimized to eliminate defect selectivity and to obtain material removal rates of greater than 150nm/hour on two-inch diameter wafers. The wafer surfaces and subsurface damage were evaluated by white light interferometery, Transmission Electron Microscopy (TEM), Atomic Force Microscopy (AFM), and epitaxial layer growth. Parametric studies were conducted using diamond and alternative abrasives and the removal rate and surface finish for each is reported. Residual surface damage induced by the polishing process that propagates into the epitaxial layer has been significantly reduced, if not entirely removed. Total dislocation densities have been measured on the ACMP processed wafers. The dislocation densities measured (<1x106 dislocations/cm2) in the EOC polished substrates are on the order of the densities reported for the best as grown silicon carbide crystals. Characterization of the GaN HEMT layers grown on these substrates indicates that the electrical performance of the devices will meet or exceed current industry requirements.

Post-Implantation Annealing in a Silane Ambient using a Hot Wall CVD Apparatus: *S. P. Rao*[1]; F. Bergamini[2]; R. Nipoti[2]; A. M. Hoff[1]; E. Oborina[1]; S. E. Saddow[1]; [1]University of South Florida; [2]CNR Sezione di Bologna

Post implant annealing of aluminum implanted 4H-SiC in a silane ambient has been conducted in a hot-wall CVD reactor with the resulting annealed surfaces exhibiting a step-bunch free, specular morphology. Two sets of 4H-SiC wafers were implanted with dual doses of $^{27}Al^{+}$ to maximize the damage to the SiC crystal. Anneals were performed from 1600°C to 1750°C. Silane was introduced into the reactor via an argon carrier gas. The silane flow was increased until a sufficient Si partial pressure was maintained over the crystal surface to ensure step-bunch free morphology. A thermodynamic model of the process has been developed in parallel to the experimental effort in order to best optimize the process parameters for other temperatures and will be reported. The annealed surfaces were characterized using plan-view SEM and AFM. For comparison, samples were annealed in an argon ambient at 1650°C in an annealing furnace for 30min. This resulted in a heavily step-bunched surface. AFM data for samples annealed in argon and silane displayed a roughness of 13.4nm and 0.9nm RMS, respectively. Non-contact electrical measurements were performed on these samples throughout processing. Secondary Ion Mass Spectrometry (SIMS) was performed to monitor the doping profile after processing and will be reported.

Application of CMP-D Process on SiC Wafers: *Ian S. Currier*[1]; [1]Engis Corporation

Chemical-mechanical polishing (CMP) has proven a powerful tool for the final polishing of semiconductor and compound semiconductor substrates such as silicon, sapphire, gallium arsenide, and indium phosphide. For these, conventional CMP techniques have been able to produce removal rates of several μm/hr while achieving pristine, epi-ready surfaces with subsurface damage under 10nm. For certain materials of interest in the compound semiconductor community, particularly silicon carbide (SiC) and III-V nitrides, conventional CMP techniques perform poorly. These materials are extremely chemically inert, negating the desired chemical effect leading to removal rates of less than 0.1μm/hr. These materials are also brittle and take damage easily, so a significant amount of material must be removed to ensure little or no subsurface damage for epitaxy. This paper introduces Engis' CMP-D process for preparing SiC wafers and its benefits. It documents the improvements made in final polishing of 4H and 6H SiC by augmenting a chemically enhanced CMP-D slurry. The chemical activity proved most effective on 4H SiC, enhancing the slurry's chemical effect and improving its removal rate. For both polytypes, the addition of diamond greatly enhanced the removal rate and provided sufficient mechanical strain to enable the chemical effect, resulting in low subsurface damage.

Effect of Reactive-Ion Etching on Thermal Oxide Properties on 4H-SiC: *Kevin Matocha*[1]; Chris Cowen[1]; Rich Beaupre[1]; Jesse Tucker[1]; [1]GE Global Research

The effect of SiC reactive-ion etching on thermal oxidation was characterized using MOS capacitors. MOS capacitors were characterized using capacitance-voltage hysteresis with ultraviolet excitation (CV-UV), linear voltage ramp breakdown (VRAMP), and Fowler-Nordheim tunneling analysis. CV-UV hysteresis showed no statistically significant difference between all oxide etching techniques examined. However, VRAMP characterization of the different treatments showed a significant effect of reactive-ion etching on the oxide breakdown field. The critical oxide breakdown field was 10.2 MV/cm with baseline RIE/wet etching and degraded to 9.7 MV/cm with 30% or greater RIE overetch. Overetching beyond 30% does not significantly decrease the oxide breakdown field. The leakage current versus electric field was fitted using a Fowler-Nordheim tunneling model through the oxide showing that progressive RIE etching reduces the barrier height from 2.51 eV to 2.46 eV. Thus, it is important to utilize multiple analysis techniques when characterizing the effect of processing parameters on the reliability of gate dielectrics on 4H-SiC.

Laser Direct Write Metallization and Doping Fabrication of Silicon Carbide PIN Diodes: Nathaniel R. Quick[1]; *Aravinda Kar*[2]; Zhoaxu Tian[2]; [1]AppliCote Associates, LLC; [2]University of Central Florida

A laser direct write metallization and doping technique is used to fabricate prototype SiC PIN diodes on n-type 6H-SiC. The laser doping process is conducted by laser irradiation in a dopant-containing ambient to simultaneously heat the SiC surface and incorporate dopant atoms into the SiC lattice. Trimethyaluminum (TMA) and nitrogen are precursors used to laser dope p-type and n-type regions, respectively, and deep junctions (~ 4 mm for both cases), with less defect generation compared to the conventional ion implantation, can be fabricated in the substrate. Laser metallization is realized by changing the surface stoichiometry forming electrically conductive phases with metal-like behavior. The diodes, fabricated by this laser direct write technique, are composed of an n-type zone in one surface and a p-type zone in the opposite surface, which are separated by the original n-type 6H-SiC medium. The edge termination is fabricated around the p-type region by laser metallization in an argon ambient. The current-voltage and capacitance-voltage characteristics of the PIN diodes were measured as a function of active diode area and annealing conditions. The silicon carbide diodes are intended for high-temperature and high-voltage power electronics applications.

Annealing Behavior of Implantation-Induced Defects in SiC at Low Temperatures: *Masataka Satoh*[1]; Tomoyuki Suzuki[1]; Shingo Miyagawa[1]; [1]Hosei University

The annealing behavior of the implantation-induced defects in highly defective N^{+} ion implanted 4H-SiC(0001) layer has been investigated by means of Rutherford backscattering spectrometry in the annealing temperature ranging from 200 to 1000°C. The samples are multiply implanted by N^{+} ions with energy range from 15 to 120 keV at a total dose of 2.4 x 10^{15} /cm^{2}. Three annealing stages are observed by isochronal annealing; first stage from 200 to 400°C, second stage from 400 to 600°C and third stage from 600 to 1000°C. The 80% of the N^{+} implantation-induced defects are annealed out by annealing stage from 400 to 600°C, which is correlated to that "Hot implantation" is performed at arount 500°C. The annealing mechanism of the defects in each stage is discussed.

MPD1.Diodes

Performance Comparison of 1.5kV 4H-SiC Buried Channel and Lateral Channel JBS Rectifiers: *Lin Zhu*[1]; T. Paul Chow[1]; Kenneth A. Jones[2]; C. Scozzie[2]; Anant Agarwal[3]; [1]Rensselaer Polytechnic Institute; [2]Army Research Lab; [3]Cree Inc.

In this work, we theoretically and experimentally, compare the performance of a new 4H-SiC JBS rectifier structure, the Buried Channel JBS (BC-JBS) rectifier with that of the Lateral Channel JBS (LC-JBS) rectifier with 1.5kV blocking capability. The BC-JBS rectifier employs buried p-type regions to create a vertical JFET region to reduce the surface electric field at Schottky contact during reverse blocking while the LC-JBS rectifier adds a lateral channel together with the vertical JFET region to protect the surface Schottky interface during high-voltage blocking conditions. The LC-JBS rectifier offers low reverse leakage current while the BC-JBS rectifier demonstrates lower on-resistance. The optimized LC-JBS rectifiers show low forward drop (<1.8V) with PiN-like reverse characteristics. The LC-JBS rectifiers also demonstrate a ~50% reduction in switching capacitance when compared to conventional Schottky rectifiers.

Nucleation Sites of Stacking Faults in Silicon Carbide PiN Diodes under Forward Bias: *Zehong Zhang*[1]; Alexander Grekov[1]; Priyamvada Sadagopan[1]; Serguei Maximenko[1]; Tangali Sudarshan[1]; [1]University of South Carolina

The nucleation sites of stacking faults (SFs) in SiC PiN diodes under forward bias were studied by electron beam induced current (EBIC) mode of scanning electron microscopy (SEM). The p+ layer of the test PiN diode structure is formed by epitaxial growth. The degradation test was done at 200 A/cm^2 at room temperature for a certain time (3 minutes to 3 hours). Basal plane dislocations (BPDs) were found to be the primary nucleation sites of SFs, and threading dislocations did not serve as nucleation sites. It was also found that damage on the sample surface introduced during device fabrication and testing can be nucleation sites for SF development. By scratching a sample surface intentionally by a diamond scriber, numerous SFs were found to develop from the scratch. It has been proposed that during the degradation test, the local stress on the diode surface (e.g. surface damage) can be released by the formation of SFs, driven by the electron-hole recombination energy. By paying careful attention to device processing and testing, such kind of surface damage can be avoided. Hence, the elimination of pre-existing BPDs present in the SiC epitaxial layer is critical to solve the problem of SiC PiN degradation.

Non-Degrading Silicon Carbide PiN Diodes Fabricated on Basal Plane Dislocation-Free Epilayer: *Zehong Zhang*[1]; Tangali Sudarshan[1]; [1]University of South Carolina

Molten KOH etching was implemented on SiC substrates before growing epilayers on them. It was found that the existence of basal plane dislocation (BPD) etch pits on the substrates can greatly enhance the conversion of BPDs to threading edge dislocations (TEDs) during epitaxy, and BPD-free SiC epilayers can be obtained if the BPD etch pits on the substrates are deep enough. The epilayers grown by this method have depressions on the surfaces, due to the "shadow" of the etch pits on the substrates. Two approaches were developed to eliminate these depressions. (1) Optimization of the KOH etching conditions. After optimization, BPD etch pits clearly present on the etched substrate surface, while etch pits of threading screw dislocations (TSDs) and TEDs are faint. (2) Polishing the epilayer surface for a few micrometers to remove the depressions. Test PiN diode structure was fabricated using such BPD-free SiC epilayer as the active layer. The degradation test was done at 200A/cm^2 for 1 to 3 hours. No BPDs were observed in these diodes by electron beam induced current (EBIC) mode of scanning electron microscopy (SEM) before degradation test, and no stacking faults (SFs) were observed after the test.

Design and Analysis of a Dual-Step Field-Plate Terminated 4H-SiC Schottky Diodes using SiO_2/High-K Dielectric Stack: *Amit Sudhakar Kumta*[1]; R. Rusli[1]; Chin-Che Tin[2]; [1]Nanyang Technological University; [2]Auburn University

Silicon dioxide (SiO_2), one of the commonly used dielectrics for field plate termination, suffers from high electric field and premature breakdown due to its low dielectric constant of k~3.9. This problem can be addressed by using high-k dielectrics that will reduce the field, increase the breakdown voltage.While the advantages of single step field-plate terminated diodes are well-known, the breakdown voltage can be improved even further using a dual-step field-plate termination.In this work we investigated using numerical simulations using MEDICI, the use of purely SiO_2 as well as high-k dielectrics such as Al_2O_3 and Si_3N_4 in conjunction with SiO_2 as dielectric for the dual-step field-plate terminated diodes. The structure simulated consists of a n-/n+ structure with a 10um 3E15/cm^3 doped epi. As shown in figure 1 our initial results show an improvement in the breakdown voltage by as much 30% from 720V to 980V for SiO_2/SiO_2 dual-step stack. With proper design, breakdown can be increased even further by using high-K dielectrics such that the layer of SiO_2 absorbs the high-electric field close to the surface while layer of high-K electric reduces the intensity of this field by virtue of its high K.

Optimization of SiC Super-SBD Based on Scaling Properties of Power Devices: *Tetsuo Hatakeyama*[1]; [1]Toshiba

A new figure of merit of power devices (HFOM) is derived based on scaling properties of power devices, which can be used for precise evaluation of the performance of a power device instead of the well-known Baliga's figure of merit. The characteristic length of a power device is the depletion layer width at breakdown, which is a function of the doping density and the breakdown field. If the doping density of the drift layer of a power device is changed, the physical structure of a power device is rescaled according to the new characteristic length, and this device shows the rescaled breakdown voltage. HFOM is defined as an invariant of this scale transformation, and is useful for the optimization of a power device, because HFOM describes the "quality" of the optimization of a power device structure. The optimization of a SiC Schottky barrier diode with the floating junction structure (Super-SBD) has been performed using HFOM. The performance of the optimized Super-SBD surpasses the performance limit of 4H-SiC devices with the conventional structure in every range of breakdown voltage.

Charge Induced in 6H-SiC pn Diodes by Irradiation of Oxygen Ion Microbeams: *Takeshi Ohshima*[1]; T. Satoh[1]; M. Oikawa[1]; S. Onoda[1]; T. Hirao[1]; H. Itoh[1]; [1]Japan Atomic Energy Research Institute

In recent year, SiC has received considerable interest in connection with its application to particle detectors with strong radiation tolerance. For the development of particle detectors, it is very important to understand the generation and transportation behavior of charge induced in SiC by a wide variety of particles. In this study, charge induced in 6H-SiC pn diodes by oxygen ion microbeams was examined in an energy range between 6 and 18 MeV. To minimize the influence of damage, single ion hit Transient Ion Beam Induced Current (TIBIC) measurement system, in which the transient current induced by single ion incidence can be measured, was used in this study. The value of charge increases with increasing reverse applied bias, and the saturation of charge is observed when the depletion layer becomes longer than ion range. An increase of collected charge by the funneling effect (the generation of a transient electric filed) is observed in the case of the depletion layer shorter than ion range. The charge collection efficiency is estimated to be 100 % in the saturation region (the depletion layer longer than ion range). It strongly suggests that high quality particle detectors are fabricated using SiC.

Anealing Effect on Cu/, Ni/4H-SiC Schottky Barrier: *Zhengyun Wu*[1]; [1]Xiamen University

Schottky Barriers are formed by magnetron sputtering the metals (Cu and Ni) on the front side of 4H-SiC(Si face) to study the rectifying characteristics of the contacts between the metals and 4H-SiC. The effects on the annealing under different temperatures are also investigated. Schottky Barrier Height (SBH) and ideal factor of metals/4H-SiC are evaluated from the I-V and C-V measurements. After annealing, the SBH of Cu/ SiC and Ni/SiC increase. But when the annealing temperature is higher than 500°C for Cu/ SiC, 700°C for Ni/SiC, the rectifying characteristic of samples degrades. The reverse leaky current is low whether or not annealing. No strong Fermi pining is found and the interface between metal and 4H-SiC is in good quality.

Characteristics and Ionization Coefficient Extraction of 1kV 4H-SiC Implanted Anode PiN Rectifiers with Near Ideal Performance Fabricated Using AlN Capped Annealing: *Lin Zhu*[1]; Peter A. Losee[1]; T. Paul Chow[1]; Kenneth Jones[2]; R. D. Vispute[3]; Anant Agarwal[4]; [1]Rensselaer Polytechnic Institute; [2]Army Research Laboratory; [3]University of Maryland; [4]Cree Inc.

4H-SiC PiN rectifiers with implanted anode and single-zone JTE were fabricated using AlN capped anneal. The surface damage during the high temperature activation anneal is significantly reduced by using AlN capped anneal. The forward drop of the PiN rectifiers at 100A/cm^2 is ~3 V while the leakage current is less than 10^{-7}A/cm^2 at room temperature. With 6µm thick drift layer, the PiN rectifiers can achieve near ideal breakdown voltage up to 1 kV. Hole impact ionization rate was extracted and compared with previous results.

Microwave Limiters Based on 4H-Siliconcarbide Diodes: *Qamar Ul Wahab*[1]; [1]Linkoping University

Simulations of PIN and Schottky diodes in 4H-SiC for high power microwave protection circuits are performed. Results are compared with Si and GaAs limiters by simulation. For microwave limiters, a minimum product of Junction Capacitance at zero bias (Cj0) and On-resistance (Ron) in combination with high thermal conductivity is needed for high power rating and minimum small signal losses. The product (Ron x Cj0) for a 50 x 50 µm2 PIN diode in 4H-SiC was 8.2 x 10-14 ΩF which was quite close to the same product for a Si PIN diode which was 7.4 x 10-14 ΩF. The same product for a GaAs PIN diode (1.7 x 10-14 ΩF) was the lowest, but the thermal conductivity of GaAs is quite low as compare to Si and 4H-SiC. Due to higher thermal conductivity 4H-SiC could enable better power performance for the same size diodes or smaller diodes with the same power rating. The higher turn on voltage of 4H-SiC PIN is a problem, to achieve limiting low signal levels (~20 dBm). Thus 4H-SiC Schottky limiter was studied for low turn on voltage (~1.1 V) and its performance was found best among all the other PiN and Schottky diode based limiters.

Investigation of Packaged Microwave 4H SiC Pin Diodes in the 20-700°C Temperature Range: *Mykola Boltovets*[1]; Volodymyr Basanets[1]; Nicolas Camara[2]; Valentyn Krivutsa[1]; Konstantinos Zekentes[2]; [1]State Enterprise Research Institute "ORION"; [2]Foundation for Research & Technology-Hellas

Packaged microwave 4H SiC pin diodes (with i-region length of 6 µm, mesa diameter of 80 µm and blocking voltage of 1000 V) were investigated. We studied the parameters of diode I-V curve (in particular, diode resistance R_s at forward current)and the process of diode switching from forward current of 50 mA to reverse voltage of 15 V, as well as the C-V curves (at reverse voltages up to 40 V) in the 20-700°C temperature range. At voltage of 300 V, the diode reverse current was 10 (180) µA when temperature was 600 (700)°C. At forward current of 40 mA, diode resistance first decreases smoothly as temperature is increased from 20 up to 300°C and then grows up. As temperature is increased from 20 up to 700°C, the effective lifetime t_{eff} grows from 7 up to 50 ns, while the diode capacitance (in the 0-40 V reverse voltage range) increases smoothly by a factor of 2.5 at reverse voltage of 40 V. The C-V curve variation indicates an increasing of the uncompensated charge carrier concentration in the diode base as temperature grows.

Electrothermal Issues in 4H-SiC 600 V Schottky Diodes in Forward Mode: Experimental Characterization, Numerical Simulations and Analytical Modeling: Andrea Irace[1]; *Vincenzo d'Alessandro*[1]; Giovanni Breglio[1]; Paolo Spirito[1]; Rossano Carta[2]; Diego Raffo[2]; Luigi Merlin[2]; [1]University of Naples "Federico II"; [2]IRCI-International Rectifier Corporation Italia

This contribution is devoted to the analysis of electrothermal issues in 600 V 4H-SiC Schottky diodes in forward mode. Particular emphasis is given to thermally-induced ON voltage surges in transient conditions when current pulses with amplitude above a threshold value are applied to state-of-the-art devices. In order to investigate this behavior we resorted to a twofold approach. First, we have tuned the parameter values of built-in SiC physical models implemented in the commercially available ATLAS software. Second, we have developed a physically-based analytical model, which relates the ON voltage drop to the applied forward current at an assigned temperature. Both the model and numerical ATLAS data have been successfully compared to experimental results obtained under isothermal (pulsed) conditions at various temperatures. Subsequently, a steady-state electrothermal simulation has been performed by means of both approaches. As a main result, it is shown that the negative temperature coefficient of the forward current at high current levels leads to an undesirable flattening of the I-V characteristic. Hence, the aforementioned voltage surges are justified by the absence of a stable equilibrium point at the forced current values. In conclusion, a fast and reliable diagnostics of the electrothermal device behavior is provided.

High-Temperature (up to 800 K) Operation of 6-kV 4H-SiC Junction Diodes: *Michael E. Levinshtein*[1]; Pavel A. Ivanov[1]; Mykola S. Boltovets[2]; Valentyn A. Krivutsa[2]; John W. Palmour[3]; Mrinal K. Das[3]; Brett A. Hull[3]; [1]Ioffe Institute of Russian Academy of Sciences; [2]Enterprise Research Institute "ORION"; [3]Cree Inc.

Steady-state and transient characteristics of packaged 6-kV 4H-SiC junction diodes have been investigated in the temperature range T = 300 – 773 K. Analysis of the forward current-voltage characteristics and reverse current recovery waveforms shows that the lifetimet of non-equilibrium carriers in the base of the diodes steadily increases with temperature across the entire temperature interval. The rise in t and decrease in carrier mobilities and diffusion coefficients with increasing temperature nearly compensate each other as regards their effect on the differential resistance of the diode, Rd. As a result, Rd is virtually temperature independent. An appreciable modulation of the base resistance takes place at room temperature even at a relatively small current density j of 20 A/cm^2. At T = 800 K and j = 20 A/cm^2, a very deep level of the base modulation has been observed. The bulk reverse current is governed by carrier generation in the space-charge region via a trap with activation energy of 1.62 eV. The surface leakage current of packaged structures does not exceed 2×10 ^(-6) A at T = 773 K and a reverse bias of 300 V.

Current Conduction and Process Yield of Ion Implanted p$^+$/n 4H-SiC Junction without JTE: Post–Implantation Annealing in Ar Ambient: *Roberta Nipoti*[1]; Fabio Bergamini[1]; Francesco Moscatelli[2]; Antonella Poggi[1]; Mariaconcetta Canino[3]; Giuseppe Bertuccio[4]; [1]CNR-IMM; [2]Università di Perugia; [3]Università di Bologna; [4]Politecnico di Milano

Ion implantation is often used in the construction of bipolar junction in SiC devices but it is not jet clear which processing steps determine the electrical quality of such junctions. The work here presented shows that process yields and current conduction of ion implanted p+/n diodes can be extremely good even for post–implantation anneals that induce step bunching at the SiC surface. 4H-SiC bipolar diodes without JTE were made by 400°C Al$^+$ ion implantation in a n–type, 3×10^{15} cm^{-3}, 5 µm thick, epitaxial layer and post implantation annealing in Ar ambient at 1600°C for 30 minutes. The sample surface was step–bunched with roughness ≤ 7 nm. The implanted acceptor profile was flat at the sample surface, 6×10^{19} cm^{-3} height and 160 nm large. The wafer was <0001> oriented, 8° off axis, Si face. Statistics of hundreds of diodes having areas in the range 2×10^{-4}–1×10^{-3} cm^{-2} were constructed. The process yield was always ≥75%. In the temperature range 25–290°C the diode forward conduction was describable by the model of abrupt junction within the frame of low-level injection-depletion approximation with ideal factor ≤ 2. In the off status the diode leakage current was dominated by the perimeter conduction and was 10^{-10} A/cm^2 at room temperature while overcame 10^{-9} Acm^{-2} for temperature ≥ 70°C and 500 V reverse bias (i.e. maximum electric field at the junction 1.14×10^6 Vcm^{-1}). At room temperature, 16% of the diodes broke down at the "reach through" reverse bias voltage and 55% at 82% of such a value.

High Temperature Operation of Silicon Carbide Schottky Diodes with Recoverable Avalanche Breakdown: *Konstantin Vassilevski*[1]; Irina Nikitina[1]; Praneet Bhatnagar[1]; Alton Horsfall[1]; Nick Wright[1]; Anthony O'Neil[1]; M. Uren[2]; Keith Hilton[2]; Alison Munday[2]; A. Hydes[2]; Mark Johnson[3]; [1]University of Newcastle; [2]QinetiQ Ltd.; [3]University of Sheffield

4H-SiC Schottky diodes with nickel silicide, titanium and molybdenum Schottky contacts have been fabricated and characterised at temperature up to 400°C. 4H-SiC epitaxial structures designed to have theoretical parallel-plain breakdown voltages of 1900 and 3600 V have been used for this research. Boron implants annealed under Ar flow at temperature of 1500°C were used for junction termination. Fabricated nickel silicide 4H-SiC Schottky diodes revealed soft recoverable avalanche breakdown at voltages above 1450 V and 3400 V respectively, which are about 75% and 95% of ideal values. Location of avalanche breakdown area was defined by electroluminescence observation and it was found to be at the outer edge of the guard ring and clearly separated from the metal contact. The nickel silicide diodes revealed unchangeable barrier heights and ideality factors as well as positive coefficients of breakdown voltage.

MPM1.Doping

Shallow P Donors in 3C-, 4H- and 6H-SiC: *Umeda Takahide*[1]; [1]University of Tsukuba

Electron paramagnetic resonance (EPR), pulsed ENDOR (electron nuclear double resonance) and other pulsed techniques were used to study phosphorus shallow donors in 3C-, 4H- and 6H-SiC doped during chemical vapor deposition growth. The precise determination of 31P hyperfine (hf) tensor has been achieved by pulsed-ENDOR which resolved weak hf hidden underneath the line broadening (P in 3C-SiC) and by ESEEM (electron spin echo envelope modulation) which enabled to assign forbidden transitions (P in 6H-SiC). The accurate determination of g-tensors was achieved by W-band (~95 GHz) experiments, especially for confirming the D2d symmetry of P in 3C-SiC. Our new data in combination with results from supercell calculations allow us to reassign the spectra to the shallow P donor at different cubic sites in hexagonal polytypes. The valley-orbit splitting (VOS) of the shallow P donors in three polytypes were estimated from the temperature dependence of the spin-lattice relaxation time and of the intensity of EPR signals. The VOS values determined from both methods are in the range 4.2-7.0 meV for different P centers. The P-related centers in P-implanted 3C-, 4H- and 6H-SiC were studied and compared to P centers in as-grown material.

Dependence of the Ionization Energy of Phosphorus Donor in 4H-SiC on Doping Concentration: *Sunil Rao*[1]; Paul Chow[1]; Ishwara Bhat[1]; [1]Rensselaer Polytechnic Institute

Recently there have been several reports on the ionization energy of phosphorous in 4H-SiC doped by ion implantations, but most of these reports concentrated on high dose phosphorous implanted SiC since the interest has been in getting heavily doped region for reducing the sheet resistance. It has been shown that 4H-SiC implanted with high dose of phosphorus has lower sheet resistances than that of 4H-SiC implanted with high dose of nitrogen. In this paper, we have implanted various doses (1x1014cm^{-2}, 2x1014cm^{-2}, 1x1015cm^{-2} and 4x1015cm^{-2}) of phosphorous into 4H-SiC in order to extract the ionization energy of phosphorous in 4H-SiC as a function of the doping concentration. Variable temperature Hall effect measurements were performed in the temperature range from 125-500K. Phosphorus in 4H-SiC has been shown to have two donor ionization energies corresponding to the in-equivalent hexagonal and cubic lattice sites. Least squares fits using the charge neutrality equation and two donor levels was used to extract the ionization energies and donor concentrations from the measured data. The ionization energies for both, the hexagonal (52meV, 48meV, 26meV) and the cubic (92meV, 83meV and 63meV) site, showed a decrease as the extracted donor concentration (5x1018cm^{-3}, 9x1018cm^{-3} and 4x1019cm^{-3}) increased.

Theoretical Investigation of Incorporation of Phosphorus during CVD Growth in SiC: *Tamás Hornos*[1]; Ádám Gali[1]; R. P. Devaty[2]; W. J. Choyke[2]; [1]Budapest Univeristy of Technology and Economics; [2]University of Pittsburgh

SiC layers can be doped by phosphorus (P) during chemical vapor deposition (CVD) growth. We used *ab initio* supercell calculations to investigate the

incorporation of P into 4H-SiC for CVD conditions. The calculations show that P_{Si} and P_C bind interstitial H and form electrically inactive stable complexes, i.e., H passivates P donors. However, unlike the case of B, the H does not change the site selection of P. We calculate the concentration of defects under consideration and that of free carriers by simulating the CVD growth. Our results indicate that concentrations of P_{Si}, as well as that of free carriers, change less than one order of magnitude and the maximum is about 3-4× $10^{16}cm^{-3}$. The second most abundant defect after P_{Si} is P_C. Its concentration is at least one order of magnitude less than that of P_{Si}. The relatively low dopant incorporation can be entirely explained by the relatively low value of chemical potential of P in the gas phase. In order to increase the incorporation of P during growth we suggest that one analyze the gas phase compositions under growth conditions: such P related precursors should be used which result in the appropriate chemical potential of P.

New Aspects in n-Type Doping of SiC with Phosphorus: *E. Rauls*[1]; U. Gerstmann[2]; Siegmund Greulich-Weber[2]; K. Semmelroth[3]; G. Pensl[3]; E. E. Haller[4]; [1]University of Aarhus; [2]University of Paderborn; [3]University of Erlangen-Nürnberg; [4]University of California

Phosphorus is a desired n-type dopant of SiC, but doping is very demanding. Doping during growth would be the most self-evident possibility. Phosphorus only hardly diffuses into SiC. Our molecular dynamics (MD) simulations show that not the diffusivity of the dopant is most critical. The P-atoms do not enter the bulk material but gather at the surface of the sample. Since also ion-implantation affects a small region below the surface only, neutron transmutation provides the most promising alternative for volume doping. In MD simulation, beside the experimentally observed donors alternative complexes with intrinsic defects (e.g. P_CC_{Si}) are predicted. Based on these theoretical results doping with neutron transmutation was reexamined. Since one problem of this method is given by the low natural abundancy of the 30Si isotope that gives rise to the transmutation process, a 6H-SiC single crystal enriched with 50% ^{30}Si was grown by the PVT-method. Hall-measurements prove the efficiency of n-type doping. Surprisingly, in EPR-measurements none of the signatures of the known P-related donors can be observed. Instead a new signal is found with large ligand hyperfine splittings in the range of 1GHz. A possible correlation with the theoretically predicted complexes is discussed.

Conditions and Limitations of using Low Temperature Photoluminescence to Determine Residual Nitrogen Levels in Semi-Insulating SiC Substrates: *Evan R. Glaser*[1]; Benjamin V. Shanabrook[1]; William E. Carlos[1]; [1]Naval Research Laboratory

We have employed low-temperature photoluminescence to estimate the total residual N concentration in large-area, semi-insulating 4H-SiC substrates where all N shallow donors are compensated in the dark. This technique was shown previously to be useful for n-type epi and bulk 4H/6H SiC where the concentration of uncompensated N donors could be determined via transport measurements. In this work the ratio of the nitrogen-bound exciton line (Q_o) to the free excitonic emission (I_{77}) as a function of excitation power density ($P_{exc.}$) was tracked for ~ 15 SI 4H-SiC samples with varying residual N concentration (~ $7x10^{14}$ – $5.2x10^{16}$ cm^{-3}) as determined by SIMS. Most notably, a linear relationship was found between Q_o/I_{77} and [N] for [N] < $1x10^{16}$ cm^{-3} under $P_{exc.}$ of ~ 100 W/cm^2. However, a sub-linear behavior was observed for samples with higher N levels under similar $P_{exc.}$ due to incomplete photo-neutralization of the residual N shallow donors. Thus, this technique should be particularly valuable to map non-destructively the residual N concentration in SI SiC substrates for cases where the N levels are driven close to or below the present SIMS Nitrogen detection limit of ~ 5 $x10^{14}$ cm^{-3}. Results obtained for SI 6H-SiC substrates will also be presented.

The Microscopic Structure of the X Center as the Dominant Defect in Semi-Insulating Silicon Carbide: *E. N. Kalabukhova*[1]; S. N. Lukin[1]; D. V. Savchenko[1]; E. N. Mokhov[2]; E. Rauls[3]; H. Overhof[3]; U. Gerstmann[3]; Siegmund Greulich-Weber[3]; [1]Institute of Semiconductor Physics; [2]N-Crystals; [3]University of Paderborn

In this work, multi-frequency EPR between 9 and 140 GHz and Hall measurements have been made on a series of undoped HPSI 4H-SiC samples. The investigations in a temperature interval from 4 K to 300 K are focused on the photosensitive intrinsic X-defect with S=1/2 residing at two inequivalent positions which is responsible for the high resistivity of HPSI 4H-SiC. At 77 K and 9 GHz the EPR spectrum consists of an overlapping central line due to X_h and X_c which characterized by an axially symmetric g-factor and hf satellites. At 40 K and 36 GHz the symmetry of the EPR spectrum changes from axial C_{3v} to a lower symmetry for the X_c defect, while for the X_h defect the axial symmetry of EPR spectrum persists. The hf splitting and angular dependence of the hf satellites are consistent with those observed for the EI6/EI5 centers (V_C^+). However, there are several details of the spectra that are quite different: The observed energy-level, the relative intensities of the inner hf splittings, and the multiplicity of EPR lines at low temperatures. Possible reasons for these discrepancies (e.g. superposition with additional donor) are discussed with the help of molecular dynamic simulations.

Identification of the Triplet State N-V Defect in Neutron Irradiated Silicon Carbide by Electron Paramagnetic Resonance: *Marina Muzafarova*[1]; [1]A.F. Ioffe Physico-Technical Institute RAS

Silicon carbide (SiC) is now facing the challenge of the material of the future for applications in high-frequency, high-temperature, high-power and radiation-resistant electronic devices. We present the results of the EPR study of heavily neutron irradiated (dose of 1021 cm^{-2}) and high-temperature annealed 6H-SiC crystals. After thermal annealing at 2000°C a new triplet center labeled as N-V has been observed. The parameters of this center are similar to that for well-known N-V center in diamond. For the first shell the structure of the N-V defect in 6H-SiC is practically identical with that in diamond. The EPR spectra of N-V defects in the triplet state in 6H-SiC reveal strong temperature dependence. This center has an axial symmetry along c-axis. The charge state of this defect seems to be +1 compare with neutral state for N-V defects with S=1/2. Anisotropic hyperfine splitting due to the 14N nuclei has been observed. Similar to the diamond N-V centers in SiC were produced by neutron irradiation and high-temperature annealing of the crystals containing nitrogen. It seems to consist of silicon vacancy and carbon substitutional nitrogen in the adjacent lattice cites oriented along c-axis.

Kinetic Mechanisms for the Deactivation of Nitrogen in SiC: Michel Georg Bockstedte[1]; *Alexander Mattausch*[1]; Oleg Pankratov[1]; [1]Universitaet Erlangen-Nuremberg

In growth or implantation experiments it was observed that the electrical activation of nitrogen saturates well below the solubility limit. This is attributed to the preferential formation of neutral nitrogen-vacancy complexes above a critical concentration. In co-implantation experiments [Schmid et al., Appl. Phys. Lett. 84 (2004), p. 3064] a reduction of the electrical activation even below the critical concentration was observed for a silicon co-implantation and annealing temperatures above 1500°C. This effect is absent for carbon co-implantation and without co-implantation. We approach the problem by the investigation of the interaction of silicon interstitials with activated nitrogen N_C and by studying the properties of vacancy clusters in conjunction with the mobile nitrogen. We find that silicon interstitials may form $(Si\text{-}N)_C$-complexes. Upon their dissociation they preferentially eject mobile nitrogen interstitials. However, the onset of this process should be below the observed critical annealing temperature. Alternatively, vacancy clusters may form at high temperatures. These may act as traps for mobile nitrogen interstitials and eventually may lead to the formation of neutral defect complexes.

MPM2.Electrical & Optical Properties I

Atomistic Insight into Thermal Conductivity Degradation of Irradiated β-SiC: *Tjacka Bus*[1]; Brian D. Wirth[1]; Yutai Katoh[2]; Lance L. Snead[2]; [1]University of California, Berkeley; [2]Oak Ridge National Laboratory

While most electronic applications of SiC are founded upon its wide bandgap-related properties, many promising future applications are based upon its high break down electric field and its excellent intrinsic thermal conductivity. These properties and especially the latter, strongly depend on the presence of defects resulting from fabrication processes involving dopant implantation, in addition to service environments with irradiation fields. In particular, it has been observed that ß-SiC experiences degradation of both thermal conductivity and dimensional stability (swelling) as a consequence of neutron irradiation at temperatures below ~ 1000°C. We have performed atomistic molecular dynamics (MD) and molecular statics (MS) simulations using the empirical interatomic potentials developed by Tersoff to improve understanding of the thermal conductivity degradation mechanisms, and the characteristics of the responsible defect structures. The results provide insight into the lowest energy defect cluster configurations, in addition to the most common defect structures produced in ion- or neutron-induced displacement cascades, and the contribution of point defects to phonon scattering. The atomistic simulation results are compared to available experimental results, which motivate additional experiments to further understand thermal conductivity degradation in ß-SiC.

Wannier-Stark Ladder and Negative Differential Conductance in 4H-SiC: *Vladimir Ilich Sankin*[1]; [1]A.F. Ioffe Physico-Technical Institute

Establishment of the basic features of impact ionization in 4H-SiC is necessary for assessing marginal parameters for a large variety of devices. The Wannier-Stark localization (WSL) process is realized in natural superlattice of SiC polytypes. Among the most significant consequences of the WSL regime there was a breakdown voltage drop with temperature rise. It should be noted that WSL phenomena are realized at a field F parallel to the axis. WSL effects disappear if the field becomes orthogonal to axis. The moderate technology of 4H-SiC epilayers fabrication prefers the plane with 80 off axis. The principle problem is whether the 8° angle is enough to depress WSL in 4H-SiC. This is what this work deals with. In our experiment we have observed the stark-phonon resonance with acoustic phonons. The NDC is discovered at eFd = 42meV that approximately equals to acoustic Eph in 4H-SiC. This result shows that WSL is not depressed by 8° slope of the field to the axis and with sufficient probability the breakdown voltage will drop with temperature rise.

Quantitative Mobility Spectrum Analysis of AlGaN/GaN Heterostructures Using Variable-Field Hall Measurements: *C. W. Litton*[1]; Necmi Biyikli[2]; J. Xie[2]; Y.-T. Moon[2]; F. Yun[2]; C.-G. Stefanita[2]; S. Bandyopadhyay[2]; H. Morkoc[2]; J. R. Meyer[3]; [1]Air Force Research Laboratory; [2]Virginia Commonwealth University; [3]Naval Research Laboratory

Carrier transport properties of AlGaN/GaN heterostructures have been analyzed with quantitative mobility spectrum analysis (QMSA) technique. The nominally undoped $Al_{0.08}Ga_{0.92}N$/GaN samples investigated were grown by plasma-assisted molecular beam epitaxy on GaN/sapphire templates prepared with hydride vapor phase epitaxy. Variable magnetic field Hall measurements were carried out in the temperature range of 5-300 K and magnetic field range of 0.01-7 T. Employing QMSA analysis on the experimental variable field Hall data, the concentration and mobility associated with the high-mobility 2DEG and the relatively low-mobility bulk electrons have been extracted for the temperature range investigated. The analysis led to 2DEG and bulk electron mobility values of ~10000 cm^2/Vs and 300 cm^2/Vs at 150 K. The results are compared with the standard single-field Hall measurements. Our study represents the multi-carrier analysis of AlGaN/GaN heterostructures using variable-magnetic field Hall measurements and QMSA.

Precise Determination of Thermal Expansion Coefficients Observed in 4H-SiC Single Crystals: *Masashi Nakabayashi*[1]; Tatsuo Fujimoto[1]; Masakatsu Katsuno[1]; Noboru Ohotani[1]; [1]Nippon Steel Corporation

Thermal expansion of SiC single crystals comprising of single 4H polytype was measured from 123K to 473K using laser interferometry method. This method allows us to directly measure the temperature-dependent variation in thermal expansion of the crystal volume, and thus enables us to obtain practical information of coefficients of thermal expansion (CTEs) that are of particular importance for designing device assembly. The CTE obtained for a nitrogen-doped 4H-SiC single crystal increased continuously from 2.0ppm/K to 3.1ppm/K for temperatures of 273K and 423K respectively, and suggested that the CTE is almost independent of the crystal axis directions of 4H-SiC.

MPM3.Extended Defects I

Invited

Structure of Carrot Defects in 4H-SiC Epilayers: *Xuan Zhang*[1]; S. Ha[1]; M. Benamara[1]; M. Skowronski[1]; J. J. Sumakeris[2]; M. J. Paisley[2]; M. J. O' Loughlin[2]; [1]Carnegie Mellon University; [2]Cree Inc.

Structure of the "carrot" defects in 4H-SiC homoepitaxial layers deposited by CVD has been investigated by plan-view and cross-sectional transmission x-ray topography, cross-sectional transmission electron microscopy, atomic force microscopy, and KOH etching. The carrot defects nucleate at the substrate/epilayer interface at the emergence points of threading screw dislocations propagating from the substrate. The typical defect consists of two stacking faults: one in the prismatic plane and the basal plane stacking fault. The faults are connected by a stair-rod dislocation with Burgers vector 1/n [10-10] with n>3 at the crossover. The basal plane fault is of Frank-type and is bounded by a partial dislocation with Burgers vector 1/12 [4-403]. The effect of carrot defects on breakdown characteristics of p-i-n diodes will be discussed.

Raman Scattering Analyses of Stacking Faults in 3C-SiC Crystals: *Takeshi Mitani*[1]; Shin-ichi Nakashima[1]; Hajime Okumura[1]; Hiroyuki Nagasawa[2]; [1]National Institute of Advanced Industrial Science and Technology; [2]HOYA Advanced Semiconductor Technologies Co., Ltd.

Stacking faults (SF) have a great influence on Raman spectra in 3C-SiC. We have investigated relationship between Raman spectral profiles and the stacking structure of faulted regions by Raman measurements with visible (457.9nm), UV (364 nm), and deep-UV (244nm) excitation sources. SF-induced Raman spectra were obtained for samples in which the location of SF was identified by molten KOH etching. SF-activated folded transverse optical (FTO) modes show that α-type stacking arrangements present in the stacking faulted region. The FTO bands also show that faulted stacking arrangements are position dependent. Structure of SFs simulated by one-dimensional lattice dynamics model based on the bond polarizalizability concept will be discussed with the results of Raman measurements. Line-shape analysis of the longitudinal optical (LO) phonon coupled with plasmon band shows the decrease of free carrier density at the place at which SF density is high.

Why Do Some of Basal Plane Dislocations get Converted to Threading Edge Dislocations, while Others Propagate during 4H-SiC Homo-Epitxay?: *Zehong Zhang*[1]; Amitesh Shrivastava[1]; Tangali Sudarshan[1]; [1]University of South Carolina

During conventional SiC epitaxial growth, 70% to 90% of the Basal Plane Dislocations (BPDs) in the substrate are converted to become Threading Edge Dislocations (TEDs) as a result of image force. However, still 10% to 30% of the BPDs in the substrate would propagate into the epilayer. The reason why some of BPDs get converted, while others propagate during SiC epitaxial growth is studied in this work. The sample was a 6.4-μm-thick (0001) 4H-SiC epilayer on a substrate cut off-axis by 8° toward the [11-20] axis. By using a new method based on the combination of molten KOH etching and Reactive Ion etching, the dislocations in the sample were tracked from the epilayer to the substrate. It was found that the BPDs with dislocation lines parallel (or approximately parallel) to the off-cut direction might propagate as BPDs into the epilayer, while those dislocation lines that form large angles (>10°) with the off-cut direction will get converted to TEDs.

Structure and Energy of the 30° Partial Dislocation in Cubic-GaN: *Gianluca Savini*[1]; Malcolm I. Heggie[1]; Alexander Blumenau[2]; [1]University of Sussex; [2]Max-Planck Institute for Iron Research

30° partial dislocations lying in {111} plane in cubic GaN are investigated theoretically. This work is focussed on the electrical properties of Ga and N dislocation cores, and on investigating the electrical fields around these defects. We use AIMPRO, a local-density functional method with norm-conserving pseudopotentials, non-local core corrections and Gaussian basis sets. The band structure analysis shows that both partials present deep states ranging between 0.6-1.0 eV from the top of the valence band. The Ga-core dislocations give rise to a donor level while an acceptor level is localized at the N-core dislocations. In the analysis of the deformation of the bonds in the dislocation cores, it is found that the atomic structure adopted (i.e. symmetric vs. asymmetric reconstructed core) depends on the environment of the dislocations. These dislocations experience a substantial charge polarization with a compressed region which is negatively charged balanced by a tensile region which is positively charged. In addition, we showed these dislocations tend to charge in a stress field. These charges could hinder carrier recombination and explain why GaN devices can tolerate high dislocation density.

MPM4.Novel Characterization and Structures I

Thermal Lens Technique for the Determination of SiC Thermo-Optical Properties: *Virgilio de Carvalho dos Anjos*[1]; Maria Jose Valenzuela Bell[1]; Elder Alpes de Vasconcelos[2]; Eronides Felisberto da Silva Jr.[2]; Acacio Andrade[3]; Roberto Franco[3]; Maria Priscila Castro[3]; Israel Esquef[3]; Roberto Faria Jr.[3]; [1]Universidade Federal de Juiz de Fora; [2]Universidade Federal de Pernambuco; [3]Universidade Estadual do Norte Fluminense

The thermal lens effect occurs in partially transparent solids when an excitation laser beam passes through the sample. The energy absorbed from the excitation laser is converted into heat and changes the optical path length, s=nl, where n is the refractive index and l is the sample length. When a probe beam propagates through the sample it can be spread or focalized, depending on the temperature coefficients of the thermal expansion and electronic polarizability of the sample. By measuring the probe beam on-axis intensity in the far field, one can obtain the thermo-optical properties (thermal diffusivity, thermal conductivity and ds/dT -optical path variation with temperature) and the fraction of absorbed energy radiation converted into heat of the sample. Thermal Lens is a high sensitivity technique with attractive advantages: it is remote, nondestructive, do not require any particular sample treatment and it is faster and simpler than other photothermal techniques. It reduces the heat transfer due to radiation and convection when compared to steady state techniques, since it is a transient method. It has been used to obtain optical and thermal properties of glasses and polymers, but until now it has not been used in semiconductor materials.

Photoacoustic Visualization of Stressed State Spatial Resolution in Silicon Carbide: *Roman M. Burbelo*[1]; Oleksandr M. Alekseev[1]; Mykola K. Zhabitenko[1]; Andryi G. Kuzmich[1]; [1]Kyiv National Taras Shevchenko University

The methods based on photoacoustic (PA) effect became of considerable widely use for investigation of optical, thermalphysic and acoustic properties of solids in last two decades. The idea of these methods is the generation of heat and acoustic waves in solids under modulated electromagnetic or pulsed radiation absorption. The goal of this work is to study the possibility of PA method usage for visualization of spatial distribution of mechanical stress fields in semiconductor silicon carbide plates under harmonic modulation of electromagnetic radiation. SiC samples of hexagonal 6H-symmetry in plate's form in which the regions of residual stresses have been artificially induced were investigated. Samples were irradiated by power laser radiation of continuous and pulsed mode. In case of continuous irradiation mode as a result of non uniform heating and cooling the cracks appeared and in case of pulsed irradiation the burned oval crater arose. This permitted to obtain two groups of samples with various types of defects. Analysis yields that the main contribution to the change of PA response value is made nonlinearity of elastic and thermoelastic properties of the medium.

MPM5.Related Materials I

Strain Relaxation Mechanisms in GaN Films Grown on Vicinal SiC Substrates: *Jie Bai*[1]; Xianrong Huang[1]; Balaji Raghothamachar[1]; Michael Dudley[1]; [1]SUNY at Stony Brook

For GaN films grown on on-axis SiC substrates, the lattice mismatch is partially accommodated by misfit dislocations at the interface with the remainder being accommodated elastically during further growth. The latter leads to gradients of lattice spacing distributions which can affect crystal quality and device performance. High resolution X-ray diffraction studies show that GaN films grown on 3.5° off-cut (towards [11-20]) SiC substrate enable the strain to largely relax at the interface and leads to better crystal quality than those grown on on-axis SiC substrates. High resolution TEM studies of the off-axis films reveal that there are two sets of misfit dislocations at the GaN (AlN)/SiC interface: 60° mixed type perfect dislocations which lie along <11-20> directions; and 60° Shockley partial dislocations which lie along <1-100> directions with Burgers vector 1/3<10-10>. The formation of above mentioned Shockley partials is favored on vicinal substrate surfaces because they can accommodate the difference in stacking sequences either side of a step. These Shockley partials exhibit special features and are referred to as geometrical partial misfit dislocations (GPMD). Much higher densities of such GPMDs at the GaN/vicinal SiC interface leads to improved strain relaxation during the initial stages of GaN film growth and hence better GaN crystal quality compared to films grown on on-axis SiC substrates.

Structural Characterization of Bulk AlN Single Crystals Grown from Self-Seeding and Seeding by SiC Substrates: *Balaji Raghothamachar*[1]; Rafael Dalmau[2]; Michael Dudley[1]; Raoul Schlesser[2]; Dejin Zhuang[2]; Ziad Herro[2]; Zlatko Sitar[2]; [1]SUNY at Stony Brook; [2]North Carolina State University

Sublimation growth is the most promising technique for the growth of large high quality, single crystal AlN boules required as substrates for nitride-based devices. Boules can be grown using self-seeding methods or using AlN or other appropriate materials as seed. Using a combination of synchrotron white beam x-ray topography (SWBXT) and high resolution x-ray diffraction (HRXRD), along with optical microscopy and SEM, the structural quality of AlN crystals grown by various sublimation-based techniques have been non-destructively analyzed. This set of characterization tools facilitates identification of defect types and mapping their distribution over the entire range of defect densities. Spontaneously nucleated AlN crystals are characterized by very low defect densities but their size is limited. Self-seeding results in nucleation of multiple grains of different orientations, a few of which are of good quality while most are highly strained. Using readily available commercial 4H and 6H-SiC substrates, several growth runs have been conducted using different growth conditions to obtain thick AlN layers, either attached to the seed or free-standing. While attached layers are typically cracked and highly strained, crack-free free-standing layers can be obtained by delamination or SiC decomposition. X-ray characterization reveals these crystals have good purity but moderately high defect densities.

Improved Structural Quality and Carrier Decay Times in GaN Epitaxy on SiN and TiN Porous Network Templates: Cole W. Litton[1]; *Umit Ozgur*[2]; Yi Fu[2]; Yong-Tae Moon[2]; Feng Yun[2]; Henry O. Everitt[3]; Hadis Morkoç[2]; [1]Air Force Research Laboratory; [2]Virginia Commonwealth University; [3]Duke University

Improved structural quality and radiative efficiency were observed in GaN thin films grown by metalorganic chemical vapor deposition (MOCVD) on in situ-formed SiN and TiN porous network templates. The room temperature decay times obtained from biexponential fits to time-resolved photoluminescence data are increased significantly with the inclusion of SiN and TiN layers. The decay time of 1.86 ns measured for a TiN network sample is slightly longer than that for a 200 µm-thick high quality freestanding GaN (1.73 ns). The linewidth of the asymmetric X-Ray diffraction (XRD) peak decreases considerably with the use of SiN and TiN layers, indicating the reduction in threading dislocation density. However, no direct correlation is yet found between the decay times and the XRD linewidths, suggesting that point defect and impurity related nonradiative centers are the main parameters affecting the lifetime.

MPM6.Surfaces and Interfaces I

Low Energy Ion Modification 3C-SiC Surfaces: Jörg Pezoldt[1]; *Christian Förster*[1]; Rastislav Kosiba[1]; Gernot Ecke[1]; Volker Cimalla[1]; Oliver Ambacher[1]; [1]TU Ilmenau

Plasma processing is the basis of different etching and deposition techniques. Furthermore they can be used for surface modification and passivation. These applications are connected with the interaction of low energy ions with solid surfaces. Nevertheless, this interaction lar-gly effects the properties of the surface and interfaces. Unfortunately, up to now less attention is drawn on the defect formation and the change in the surface composition. In the present investigation the effect of argon and nitrogen with 3C-SiC surfaces at accelaration voltages below 2 keV were studied by stylus profilometry, reflectometry, atomic force microscopy, reflection high energy electron diffraction and Auger electron spectroscopy (AES). The ero-sion rate of the silicon carbide surface was determined. AES measurements revealed Ar and N incorporation at a depth of a few nanometers as well as stoichiometric changes at the same depth scale. In the case of N interaction with the 3C-SiC surface the formation of a SiCN-alloy was detected.

A Comparison of Various Surface Finishes and the Effects on the Early Stages of Pore Formation During High Field Etching of SiC: Y. Ke[1]; C. Moisson[2]; R. Feenstra[3]; R. P. Devaty[1]; *W. J. Choyke*[1]; [1]University of Pittsburgh; [2]NOVASIC Savoie Technolac; [3]Carnegie Mellon University

The effects of initial surface morphology on the early stages of porous SiC formation under highly biased photoelectrochemical etching conditions are discussed. We etched both Si and C-face polished n-type 6H SiC with different surface finishes prepared by either mechanical polishing or by chemical mechanical polishing at NOVASIC. For both Si-face and C-face porous SiC samples, different surface and cross sectional porous morphologies due to different surface finishes are observed. We propose corresponding explanations due to the spatial distribution of holes inside the semiconductor. This understanding of surface nucleation and its effects on the resulting porous structure formation will help us fabricate a variety of useful porous morphologies.

Temperature Induced Phase Transformation on the 4H-SiC (11-20) Surface: Wai Y. Lee[1]; Serguei Soubatch[2]; *Ulrich Starke*[1]; [1]Max-Planck-Institut für Festkörperforschung; [2]International University Bremen

The demand for better SiC devices has initiated an interest in the non-polar 4H-SiC (11-20) surface due to its lower defect density properties as compared to the basal-plane surfaces. In this work, we have studied the hydrogen etched (11-20) surface as a function of temperature and after Si deposition using XPS, LEED, AES and AFM. Results show that despite having a smooth, featureless surface (as observed by AFM), the 'just-loaded' hydrogen etched surface exhibits a (1x1) LEED pattern, although weak. Chemically, the surface has a C-rich composition, indicated by XPS spectra and an Auger Si/C peak ratio of 0.5 with an additional small amount of oxygen present. The oxygen peak vanishes upon heating to about 1150°C. A well ordered surface can be obtained by Si deposition and subsequent annealing. The LEED pattern remains (1x1). However, the LEED intensities show a sharp change around 1000°C indicating a structural phase transformation. The chemical composition also changes during annealing, however in a more gradual manner. The surface is still carbon rich. The results will be discussed in detail, focusing on the chemical and structural properties of the two distinct phases observed.

Effect of Surface Orientation and Off-Angle on Surface Roughness and Electrical Properties of p-Type Impurity Implanted 4H-SiC Substrate After High Temperature Annealing: *Akimasa Kinoshita*[1]; Makoto Katou[1]; Miwa Kawasaki[1]; Kazutoshi Kojima[1]; Kenji Fukuda[1]; Kazuo Arai[1]; Fukuyoshi Morigasa[1]; Tomoyoshi Endou[1]; Takuo Isii[1]; Teruyuki Yashima[1]; [1]Advanced Industrial Science and Technology

High temperature above 1600º is useful to fabricate p-type region with low resistance for low contact resistance of SiC DMOS. Many researchers have studied the activation technique or the surface roughness for Si-face 4H-SiC annealed at high temperature. However, there is a little work reported on the effect of surface orientation and off-angle on the p-type activation or surface roughness. We investigated the effect of surface orientation and off-angle on surface roughness, sheet resistance, free carrier concentration and Hall mobility of 4H-SiC after high temperature annealing. The samples were obtained from 4H-SiC (0001) substrate 8 degree off-angled and (000-1) substrate 8º, 4º, less than 1º off-angled with an n-type epitaxial layer. High temperature annealing was performed in an Ar ambient at 1600 ~ 1800º for 60s using hybrid super RTA system. In this study, it is shown that surface roughness after high temperature annealing at 1800º decrease with decreasing off-angle for C-face 4H-SiC. Using C-face 4H-SiC with low off angle is expected to suppress any problems caused by increase of surface roughness after high temperature annealing.

4:10 PM Coffee Break

MC1.Extended Defects I

Monday, 4:30-6:15pm
September 19, 2005

Room: Allegheny Ballroom I
Location: Westin Pittsburgh

Session Chair: P. Pirouz, Case Western Reserve University

4:30 PM Invited
Theory of Dislocations in SiC: *Alexander T. Blumenau*[1]; [1]Max-Planck-Institut f. Eisenforschung GmbH

Under forward bias bipolar 4H- and 6H-SiC devices are known to degrade rapidly through stacking fault formation and expansion in the basal plane. These stacking faults are bordered by 30° and 90° Shockley partial dislocations and it has been suggested that a recombination-enhanced dislocation glide mechanism allows them to overcome their barrier to glide motion and thus results in stacking fault growth. To gain deeper insight into this mechanism requires a better understanding of the atomistic and electronic structure of the dislocations involved. Fortunately, nowadays advances in computing power and in theoretical methodology allow the *ab initio* based modelling of some aspects of the problem. This contribution therefore gives a review of recent activities and advances in this field, and further discusses the general problems of *ab initio* based modelling of dislocations in compound semiconductors.

5:00 PM
Recombination Behavior of Stacking Faults in SiC P-I-N Diodes: *Serguei Ivanovich Maximenko*[1]; Pirouz Pirouz[2]; Tangali Sudarshan[1]; [1]University of South Carolina; [2]Case Western Reserve University

Although silicon carbide (SiC) exhibits superior material characteristics as a semiconductor material, its applications for device fabrication is limited due to the presence of various crystallographic defects in the material. Due to improvements in crystal growth technology during the past several years, micropipes, a harmful defect for device performance, have been reduced significantly in high-quality commercial SiC wafers. However, a current problem of significant interest is an increase of voltage drop in forward-biased bipolar devices (degradation phenomenon), even at moderate current densities. It has been found that this degradation phenomenon is associated with the nucleation and development of stacking faults (SFs) in the active region of SiC bipolar diodes under forward carrier injection. In this paper, the electrical activity of the SF areas as well as that of the bounding partial dislocations were investigated using the technique of EBIC on degraded p-i-n diodes. The recombination behavior of C- and Si-core dislocations is discussed. It is proposed that nonradiative recombination significantly exceeds radiative recombination on both the C- and Si-core partial dislocations. At the same time, predominantly radiative recombination takes place in the faulted planes that are presumably acting as quantum wells.

5:15 PM
Observation of Shrinking and Reformation of Shockley Stacking Faults by PL Mapping: *Toshiyuki Miyanagi*[1]; Hidekazu Tsuchida[1]; Isaho Kamata[1]; Tomonori Nakamura[1]; Ryousuke Ishii[1]; Koji Nakayama[2]; Yoshitaka Sugawara[2]; [1]Central Research Institute of Electric Power Industry; [2]Kansai Electric Power Co., Inc.

In this paper, we firstly report the evidence of shrinking of Shockley stacking fault (SSF) in SiC epitaxial layer by high temperature annealing. The high-power laser irradiation in combination with PL mapping makes it possible to investigate the formation of SSFs, which lie between a pair of partial dislocations formed by dissociation of a basal plane dislocation (BPD), without fabrication of pin diodes. Using of this technique, we investigated the annealing effects on SSFs. In comparison with before and after annealing at 600ºC for 10 minutes, it is confirmed that the high-temperature annealing results in shrinking of the faulted area of the SSFs. The SSFs reform into exactly the same features as those before annealing when the high-power laser irradiation is performed again to the same position. This result shows that the SSFs shrink by 600ºC annealing but the nuclei of each SSF (BPDs) do not disappear.

5:30 PM
Overlapping Shockley/Frank Faults in 4H-SiC PiN Diodes: *Mark E. Twigg*[1]; Robert E. Stahlbush[1]; Peter Losee[2]; Canhua Li[2]; Ishwara Bhat[2]; Paul Chow[2]; [1]Naval Research Laboratory; [2]Rensselaer Polytechnic Institute

Using light emission imaging (LEI), we have determined that certain planar defects in 4H-SiC PiN diodes do not expand in response to bias. Accordingly, plan-view transmission electron microscopy (TEM) observations of these diodes indicate that these planar defects are different in structure from the mobile stacking faults (SFs) that have been previously observed in 4H-SiC PiN diodes. Bright and dark field TEM observations reveal that these static planar defects are bounded by partial dislocations that display both Frank and Shockley character. That is, the Burgers vector of such partial dislocations is 1/12<4-403>. For sessile Frank partial dislocations, glide is severely constrained by the need to inject either atoms or vacancies into the expanding faulted layer. Other aspects of these planar defects, however, are observable in plan-view TEM by weak-beam imaging. Because certain regions of these planar defects are only visible by weak-beam TEM, these areas must consist of overlapping SFs configured so as to translate thin layers of 4H-SiC lying in the c-plane. Such thin layers must be bounded top and bottom by stacking faults with equal and opposite translation vectors in order to be visible in weak beam TEM, but invisible in bright field and dark field TEM.

5:45 PM
Development of Non-Destructive In-House Observation Techniques for Dislocations and Stacking Faults in SiC Epilayer: *Isaho Kamata*[1]; Hidekazu Tsuchida[1]; Toshiyuki Miyanagi[1]; Tomonori Nakamura[1]; [1]Central Research Institute of Electric Power Industry

In this paper, we report the non-destructive, in-house observation techniques of dislocations / stacking faults in SiC epilayer using a laboratory X-ray topography system and photoluminescence (PL) mapping. By PL mapping, the grain boundaries in the C-face epilayer, narrow band of Shockley stacking faults with a pair of partial dislocations dissociated from BPDs and In-grown stacking fault were clearly observed. By the laboratory X-ray topography system, screw dislocations and BPDs are also observed. From the measurement datum, we showed that the techniques are a quite beneficial for the routine measurement.

6:00 PM
Transmission Electron Microscopy of Basal Plane Slip Bands in Bulk SiC Crystals: Seoyong Ha[1]; *Jae Won Lee*[1]; Marek Skowronski[1]; M. F. Brady[2]; A. Powell[2]; [1]Carnegie Mellon University; [2]Cree Inc.

Basal plane slip bands in bulk SiC crystals have been studied by molten KOH etching and transmission electron microscopy (TEM). Parallel arrays of oval shaped etch pits extending in the direction perpendicular to the off-cut direction observed after KOH etching have several characteristics of basal plane slip bands. Low magnification TEM analysis determined the Burgers vector of multiple dislocations in one array as b = a/3[11-20]. Contrasts of all dislocations in an array behaved in the same way indicating parallel Burgers vectors and confirming the interpretation of the origin of an array. At high magnification, dislocations were resolved into pairs of partials with b = a/3<1-100>. Cores of partial dislocations were identified as C- or Si-types by oscillating contrast analysis. Pairs of C-core partial dislocations found in the slip bands did not move under electron beam. In contrast, pairs of Si-core partial dislocations were widely dissociated and mobile under electron beam.

MC2.Schottky and Bipolar Devices

Monday, 4:30-6:15pm
September 19, 2005

Room: Allegheny Ballroom I
Location: Westin Pittsburgh

Session Chair: D. Stephani, Siemens

4:30 PM Invited
Advances in SiC GTO Development and Its Applications: *Yoshitaka Sugawara*[1]; [1]Kansai Electric Power Company

SiC has excellent electrical and physical properties and some high voltage SiC FETs have demonstrated superior performances to those of Si devices. However, because of a small chip area caused to crystal defects and a positive temperature dependence of RonS, their current capabilities are small for practical applications. To achieve the large current capability in spite of the small chip area, high current density is essential. In this point, thyristor devices are superior to unipolar devices due to conductivity modulation and negative temperature dependence of on-state voltage, therefore, some SiC GTO (Gate Turn-off) thyristors with current capability of 0.35-60A and blocking voltage of 0.7-12.7 kV have been demonstrated [1,2]. In this presentation, recent progress in SiC GTO performance will be introduced, specially focused on SiCGT (SiC Commutated Gate turn-off Thyristor). Furthermore, modules using SICGTs and inverters using SICGT modules will be introduced. [1]Y.Sugawara :"SiC Devices for High Voltage High Power Applications", Final Program of ICSCRM2003, p.64 (2003); Material Science Forum Vol.457-460, p.963 (2004). [2]Y.Sugawara et al.: "12.7kV Ultra High Voltage SiC Commutated Gate Turn-off Thyristor: SICGT", Proceedings of ISPSD2004, p.365 (2004).

5:00 PM
A Surge Current Stable and Avalanche Rugged SiC Merged pn Schottky Diode Blocking 600V Especially Suited for PFC Applications: *Michael Treu*[1]; [1]Infineon Technologies

Today silicon carbide (SiC) Schottky diodes are mainly used in the power factor control (PFC) unit of high end switched mode power supplies, due to their outstanding switching performance compared to Si pn diodes. To increase the market penetration of SiC Schottky diodes it is very valuable to provide devices satisfying the special needs of this key application. In the case of the PFC it is required that the diodes are capable of handling surge currents up to several times the current of normal operation. Such surge currents occur e.g. during power on or after line cycle drop outs. For the standard Schottky diode this surge current capability is quite limited due to its unipolar nature and the related significant positive temperature coefficient of the resistivity. An improvement of this property will clearly increase the performance/cost

ratio of the device and, therefore, improve the market penetration capability. In order to increase the surge current capability Infineon Technologies and SiCED realized a merged pn Schottky diode where the p-areas are optimized as efficient emitters. During normal operation the diode is behaving like a normal Schottky diode whereas during surge current condition the diode is behaving like a pn diode.

5:15 PM
A 1 cm x 1 cm, 5 kV, 100 A 4H-SiC Thyristor Chip for High Current Modules: *Anant K. Agarwal*[1]; Ben Damsky[2]; James Richmond[1]; Sumi Krishnaswami[1]; Craig Capell[1]; Sei-Hyung Ryu[1]; John W. Palmour[1]; [1]Cree Inc.; [2]Electric Power Research Institute

We report on the development of the first 1 cm x 1 cm SiC Thyristor chip capable of handling 5 kV. This demonstrates the present quality of the SiC substrate and epitaxial material. A forward drop of 4 V at 100 A and 200°C was measured. The turn-on delay is found to be a strong function of the gate current. At a gate current of 1.5 A, the turn-on delay of 72 ns is observed for anode to cathode current, IAK =10 A. The turn-on rise time is a strong function of the anode to cathode voltage, VAK. These devices can turn-on 100 A with a delay of less than 200 ns and a rise time of about 1 microsecond with VAK = 100 V and IG=1 A. The rise time can be even faster (< 100 ns) with higher VAK. The successful paralleling of three 1 cm^2 chips demonstrates that higher current modules can be built with the 1 cm^2 building blocks. In summary, with the successful demonstration of a 1 cm^2 SiC switch, an important milestone has been reached in the development of the SiC Power Device Technology.

5:30 PM
6 kV, 25 A 4H-SiC PiN Diodes for Power Module Switching Applications: *Brett A. Hull*[1]; Mrinal K. Das[1]; James T. Richmond[1]; Bradley Heath[1]; Joseph J. Sumakeris[1]; Bruce Geil[2]; Charles J. Scozzie[2]; [1]Cree, Inc.; [2]Army Research Laboratory

The advances in the technology of 4H-SiC PiN diodes have been rapid over the past few years, with state-of-the-art devices able to block in excess of 20 kV. However, forward voltage (V_F) drift, in which a PiN diode suffers from an irreversible increase in V_F under forward current flow, continues to inhibit commercialization of SiC PiN diodes. Recent progress in 4H-SiC epitaxial growth has allowed for the reduction in the density of basal plane dislocations (BPD) – a main contributor to V_F drift – to as low as 10 cm^{-2}. We are refining BPD reduction epitaxial growth with the aim of developing a commercially viable process that provides the best combination of V_F, blocking, and V_F drift yields. We will present our latest efforts at employing this process to fabricate 4H-SiC PiN diodes designed to carry 25 A and block up to 6 kV. Our best single 3" wafer (108 diodes/wafer) had 100% V_F yield, 49% blocking yield, and 87% V_F drift yield (ΔV_F < 100 mV with a 30 min, 25 A stress), for a 43% total die yield. We will present a comparison of the electrical characteristics of these diodes to similarly rated commercially available Si PiN diodes.

5:45 PM
Improving Switching Characteristics of 4H-SiC Junction Rectifiers using Epitaxial and Implanted Anodes with Epitaxial Refill: *Peter Almern Losee*[1]; Canhua Li[1]; Ravi Kumar[1]; T. Paul Chow[1]; Ishwara Bhat[1]; Ronald Gutmann[1]; [1]Rensselaer Polytechnic Institute

The on-state and switching performance of high voltage 4H-SiC junction rectifiers are compared using numerical simulations and fabricated devices. 4H-SiC Epitaxial anode, implanted anode, and static-shielded-diode (SSD) rectifiers have been fabricated on 110µm thick, lightly doped drift layers. The low forward voltage drop of the epi-anode diodes (~4.2V \@ 100A/cm^2) indicates signifcant conductivity modulation while the superior switching performance of the SSD is demonstrated with device reverse recovery characteristics at various temperatures and forward current densities.

6:00 PM
Current Gain Dependence on Emitter Width in 4H-SiC BJTs: *Martin Domeij*[1]; Hyung-Seok Lee[1]; Carl-Mikael Zetterling[1]; Mikael Östling[1]; Adolf Schöner[2]; [1]KTH Royal Institute of Technology; [2]Acreo AB

In this work, high current gain SiC BJTs with improved epilayer design and a continuous growth of the base-emitter junction have been studied with varying emitter finger widths. Measurements of the common emitter current gain vs. the collector current show a clear emitter size effect indicating that surface recombination has a pronounced effect on the current gain. The results are highly reproducible over the wafer with maximum gain values exceeding 60. Device simulations with interface states along the etched and oxidized (exposed) surfaces show an emitter size effect in qualitative agreement with the measurements. Simulations with a pure bulk recombination, on the other hand, result in current gains that increase with decreasing emitter width in contradiction with the measurements. Improved surface passivation using state-of-the-art thermal oxidation is proposed for improving the current gain of SiC BJTs.

TA1.Advanced Processing

Tuesday, 8:30-10:00am
September 20, 2005

Room: Allegheny Ballroom I
Location: Westin Pittsburgh

Session Chairs: S. E. Saddow, University of South Florida; B. G. Svensson, University of Oslo

8:30 AM Invited
Nanochemistry at Silicon Carbide Surfaces: H-Induced Semiconductor Surface Metallization: *Patrick Gilles Soukiassian*[1]; Hanna Enriquez[1]; Mathieu Silly[1]; Vincent Derycke[1]; Marie D'angelo[1]; Claudio Radtke[1]; Victor Aristov[1]; Fabrice Amy[2]; Yves Chabal[3]; Maddalena Pedio[4]; Paulo Moras[4]; Paulo Perfetti[4]; [1]Commissariat à l'Energie Atomique; [2]Princeton University; [3]Rutgers University; [4]ISM-CNR/Elettra Sincrotrone Trieste

Hydrogen (H) is Mendeleev classification simplest element and is well known to passivate semiconductor surfaces. The first example of semiconductor surface metallization induced by atomic H is presented here. Such a surprising nanochemistry is evidenced using STM/STS, synchrotron radiation-based core level/valence band photoemission, infrared absorption (IRAS), and achieved for Si-rich 3C-SiC(100)3x2[1]. Most interestingly, such H-induced metallization also occurs for pre-oxidized 3C-SiC(100)3x2[2]. H-induced metallization is evidenced through band gap closing, Fermi level built-up, large band-bending, reactive component and large chemical shift at Si 2p, and specific IRAS features. The results indicate H-induced asymmetric attack on sub-surface Si dimers. The metallization process results from competition between H termination of surface dangling bonds and H-generated steric hindrance below surface. The results are compared to recent ab-initio calculations also predicting metallization but providing an alternative interpretation[3]. H-stabilized metallization directly impacts ability to eliminate electronic defects at semiconductor interfaces critical for microelectronics, provides means to develop electrical contacts on high band-gap chemically passive materials, particularly exciting for interfacing e.g. with biological systems. [1]Derycke et al., Nature Materials 2, 253 (2003); [2]Silly et al., Appl. Phys. Lett. 85, 4893 (2004); [3] di Felice et al., Phys. Rev. Lett. 94, 116103 (2005).

9:00 AM
Variations in the Effects of Implanting Al at Different Concentrations into SiC: *Kenneth A. Jones*[1]; [1]Army Research Laboratory - SEDD

SiC samples implanted at 600°C with 1018, 1019, or 1020 cm-3 of Al to a depth of ~ 0.3 µm and annealed with a (BN)AlN cap at temperatures ranging from 1300 – 1700°C were studied. Some of the samples have been co-implanted with C or Si. They are examined using Hall, sheet resistivity, EPR, CL, TEM, and RBS measurements. In all instances the sheet resistance is larger than a comparably doped epitaxial layer, with the difference being larger for samples doped to higher levels. The results suggest that not all of the damage can be annealed out, as stable defects appear to form, and a greater number or more complex defects form at the higher concentrations. Further, the defects affect the properties of the Al acceptor as the CL peak associated with a free electron recombining with a hole bound to an Al acceptor decreases in intensity as the annealing temperature is raised. Also, no EPR peak is detected for implanted Al, and the implanted Al reduces the peak's intensity in bulk SiC. TEM analyses indicate that the defects are stacking faults and/or dislocations.

9:15 AM
High Dose High Temperature Ion Implantation of Ge into 4H-SiC: Jörg Pezoldt[1]; *Thomas Kups*[1]; Petia Weih[1]; Matthias Voelskow[2]; Wolfgang Skorupa[2]; [1]TU Ilmenau; [2]FWHIM, Institute for Ion Beam Physics and Material Science, FZ Rossendorf

$(Si_{1-x}C_{1-y})Ge_{x+y}$ semiconductor solid solutions could be of great interest for the forma-tion of new types of heterostructures for SiC devices. Ion implantation of Ge in SiC is an al-ternative technique that provides the possibility to overcome this obstacles attendant to growth processes in the case of metastable or immiscible material systems. This material syn-thesis method allows the incorporation of Ge with concentrations exceeding the thermody-namical Ge miscibility limit and leads to the formation of $(Si_{1-x}C_{1-y})Ge_{x+y}$ alloys. A box like Ge distribution was formed by ion implantation at 600°C. The Ge concentration was varied from 1 to 20 %. The TEM investigations revealed an increasing damage formation with in-creasing implantation dose. No polytype inclusions were observed in the implanted regions. This agrees well with previous studies were the polytype could be retained during ion beam synthesis of $(SiC)_{1-x}(AlN)_x$ with a composition of 20% AlN in the SiC lattice. A more detailed analysis showed different types of lattice distortion identified as insertion stacking faults. The ALCHEMI analysis revealed that the Ge atoms are mainly located at interstitial positions. These observations will be compared to FTIR-ellipsometric measurements.

9:30 AM
Micromachining of Novel SiC on Si Structures for Device and Sensor Applications: *Christian Förster*[1]; Volker Cimalla[1]; Mike Stubenrauch[1]; Carsten Rockstuhl[2]; Klemens Brückner[1]; Jörg Pezoldt[1]; Oliver Ambacher[1]; [1]Technical University Ilmenau; [2]Friedrich Schiller University Jena

SiC is well known for smart power electronic devices operating at high temperatures as well as at high frequencies. The superior mechanical attributes like the high Young's modulus, the extreme mechanical hardness and stiffness predestines this material for microsensors and microactuators in microelectromechanical systems and nanoelectromechanical systems (MEMS and NEMS) with high frequencies up to the GHz range. The very low oxidation and corrosion rates of SiC connected together with the strong chemical inertness in all kinds in wet etching acid solutions allows the application of silicon carbide based micro- and nanostructures in harsh environments. We will present SiC based MEMS and NEMS resonators actuated under ambient conditions, nanooptics in the form of SiC/Si infrared gratings and applications of silicon carbide for wear protection as well as nanomasking.

9:45 AM
Development of a Microstrip SiC MMIC Process: *Mattias Südow*[1]; Niklas Rorsman[1]; Per-Åke Nilsson[1]; Kristoffer Andersson[1]; Herbert Zirath[1]; [1]Chalmers University of Technology

Since both SiC MESFETs and high performance GaN HEMTs use semi-insulating SiC substrates, the development of a SiC MMIC process is in theory generic. This paper describes the development of the microstrip SiC MMIC process at Chalmers University. The MMIC process is based on the Chalmers SiC MESFET technology. These transistors exhibit power densities of 3W/mm\@3GHz in class AB operation and drain efficiencies of 60%. The passive component technology has been transferred from the InP microstrip MMIC process at Chalmers and adapted to the high power requirements set by the SiC MESFET technology. Circuit models have been developed using the built in models in Agilent ADS®, thereby enabling the construction of a design kit for SiC MMIC fully compatible with a future process for GaN MMIC with the exception of the active elements. MIM capacitors with break down voltages surpassing 100V, air bridged spiral inductors and TaN thin film resistors with sheet resistances of 45Ω/□ have been developed and characterized. One key factor in the development of the microstrip process has been through wafer via-holes.

10:00 AM Coffee Break

TA2.EPI I: Multi-Wafer, Halide Assisted Epitaxy

Tuesday, 8:30-10:00am
September 20, 2005

Room: Allegheny Ballroom II & III
Location: Westin Pittsburgh

Session Chairs: J. A. Powell, Sest, Inc.; R. Yakimova, Linkoping University

8:30 AM Invited
Challenges in Large-Area Multi-Wafer SiC Epitaxy for Production Needs: *Bernd Thomas*[1]; Christian Hecht[1]; [1]SiCED GmbH & Co. KG

In the last years the quality of SiC devices could be enhanced and the costs have been reduced by enlarging the wafer size as well as by a significant progress in epitaxial growth of active layers by using multi-wafer CVD systems. Besides material properties like crystal structure, purity and specular surface morphology it becomes more and more necessary to achieve excellent values in homogeneity of doping and thickness as well as excellent run-to-run and intra-run reproducibility in order to meet the requirements of production needs. Special attention must be paid to the reduced off-orientation for large area substrates which needs to evaluate new process windows. Additionally, equipment parameters, which are not directly related to the properties of epitaxial layers are of great interest to utilize a cost-effective system for large-scale production. In this paper we want to give an overview of SiC multi-wafer systems in the past and presence. We will present recent results of SiC homoepitaxial growth using our multi-wafer hot-wall CVD system. This equipment exhibits a capacity of 5x3"wafers per run and can be upgraded to a 7x3" or 5x4" set-up. Issues like lifetime of components, drift of parameters and system stability over several runs will be discussed.

9:00 AM
SiC Warm-Wall Planetary VPE Growth on Multiple 100-mm Diameter Wafers: *Al Burk*[1]; M. J. O'Loughlin[1]; M. Paisley[1]; A. Powell[1]; M. Brady[1]; R. Leonard[1]; D. McClure[1]; [1]Cree, Inc.

Experimental results are presented for SiC epitaxial layer growths employing large-area, up to 8x100-mm, warm-wall planetary SiC-VPE reactors. These high-throughput reactors have been optimized for the growth of uniform 0.01 to 35-micron thick, specular, device-quality SiC epitaxial layers with background doping concentrations of $<1x10^{14}$ cm^{-3}. Multi-layer device profiles such as Schottkys, MESFETs, SITs, and BJTs with n-type doping from $\sim1x10^{15}$ cm^{-3} to $>1x10^{19}$ cm^{-3}, p-type doping from $\sim3x10^{15}$ cm^{-3} to $>1x10^{20}$ cm^{-3}, and abrupt doping transitions (~1 decade/nm) are regularly grown in continuous growth runs. Intrawafer layer thickness and n-type doping uniformities of <1% and <5% σ/mean have been achieved in the 7x3-inch and ~3% and ~9% in a 6x100-mm configuration. Within a run, wafer-to-wafer thickness and doping variation are ~± 1% and ~± 5% respectively. Long term run-to-run variations while under process control are approximately ~3% σ/mean for thickness and ~5% σ/mean for doping. Latest results from an even higher capacity 8x100-mm reactor are also presented.

9:15 AM
Highly Uniform SiC Epitaxy for MESFET Fabrication: *Jie Zhang*[1]; Janice Mazzola[1]; Carl Hoff[1]; Cristian Rivas[1]; Esteban Romano[1]; Janna Casady[1]; Jeff Casady[1]; [1]SemiSouth Laboratories

This presentation demonstrates our highly uniform SiC CVD epitaxy with abrupt buffer/channel transition for MESFET growth. The epi growth is conducted in a horizontal hot-wall CVD reactor with gas foil rotation. N-doping is obtained with N2 and p-doping with TMAl. This reactor provides exceptionally good uniformity in both thickness and doping. FTIR is used to map thickness over full wafer and the doping is obtained by CV measurements on mercury or Ni Schottky. We have obtained typical thickness uniformity below 2% for 2" and below 1% for 3" wafers. For 3x2" growth, the wafer-to-wafer variation lies below 1%. For instance, a 0.8 um thick 3" epilayer has a thickness uniformity of 0.5%. The n-doping of this epi is 4x1017 cm-3 with a uniformity of 7%. The doping uniformity for both p- and n-doped epilayers lies reproducibly below 10% for a wide doping range of below 5x1015 to above 1x1019 cm-3 for both n- and p-doping. SIMS and SEM examination is under progress to verify the high quality interface and abrupt transition between buffer and channel. In addition, on-wafer electrical measurements will be performed to demonstrate the pinch-off voltage distribution over the full wafer.

9:30 AM
Epitaxial Layers Grown with HCl Addition: A Comparison with the Standard Process.: *Francesco La Via*[1]; Giuseppa Galvagno[1]; Fabrizio Roccaforte[1]; Riccardo Reitano[2]; Lucia Calcagno[2]; Gaetano Foti[2]; Giuseppe Abbondanza[3]; Maurizio Masi[4]; Danilo Crippa[5]; [1]CNR-IMM; [2]Catania University; [3]Epitaxial Tecnology Center; [4]Politecnico di Milano; [5]LPE

In the last ECSCRM in Bologna we presented a new process that overcomes the limitation of the low growth rate and will produce a second breakthrough in the epitaxy process. The growth rate has been increased of a factor 3 (up to 18µm/h) with respect to the standard process with the introduction of HCl in the deposition chamber. In this work, we have characterized the epitaxial layers grown with the addition of HCl by electrical, optical and structural characterization methods. A comparison with an optimized process without the addition of HCl is reported too. On the epitaxial wafers several Schottky diodes with different contact areas have been realized with a boron implanted edge termination and using a nickel silicide (Ni2Si) as Schottky barrier. These diodes were characterized by current-voltage (I-V) and capacitance-voltage (C-V) maps of the entire wafer to obtain statistical information, spatial distribution of defects and doping uniformity. The diodes, realized on the epitaxial layer grown with the addition of HCl at 1600°C, should have electrical characteristics comparable with the standard epitaxial process with the interesting advantage of an epitaxial growth rate a factor three higher.

9:45 AM
Investigation of the Mechanism and Growth Kinetics of Homoepitaxial Growth using CH_3Cl Carbon Precursor.: *Yaroslav Koshka*[1]; Huang-De Lin[1]; Jeffery L. Wyatt[1]; [1]Mississippi State University

The mechanism of the epitaxial growth of 4H SiC using CH_3Cl carbon source was investigated. The experiments were conducted with H_2 carrier gas flow rate reduced in comparison to the standard conditions optimized for device-quality full-wafer C_3H_8 growth. Low-H_2 conditions have been found favorable for investigating the differences between the two gas systems. A non-linear trend of the growth rate dependence on CH_3Cl flow was observed. The increasing of CH_3Cl flow resulted in (1) enhanced rate of homogeneous nucleation at the leading edge of the susceptor and (2) depletion of the precursors downstream of the susceptor. The observation of a quantitatively different pattern of this trend for C_3H_8 growth is an indication of different kinetics of CH_3Cl and C_3H_8 precursor decomposition as well as different influences on Si droplet formation and dissociation. The maximum growth rate that we were able to achieve at

the same temperature and flow conditions was by a factor of two higher for CH_3Cl system than for C_3H_8 system. Growth experiments at temperatures below 1450^{0}C will be presented. The currently observed trend offers a promise of a mirror-like morphology of 4H SiC homoepitaxial growth at temperatures below 1400^{0}C with growth rates of at least 1-2 μm/hr.

10:00 AM Coffee Break

TB1.Point Defects I

Tuesday, 10:45am-12:40pm
September 20, 2005

Room: Allegheny Ballroom I
Location: Westin Pittsburgh

Session Chairs: G. Pensl, University of Erlangen-Nürnberg; A. Gali, Budapest University

10:45 AM Invited
Optical Studies of Deep Centers in Semi-Insulating SiC: *Björn Magnusson*[1]; Erik Janzén[2]; [1]Norstel AB; [2]Linköping University

Deep centers are important defects in semi-insulating SiC wafers and they also act as lifetime limiting defects in bipolar device applications. Today's state of the art growth techniques are able to produce epitaxial layers and wafers with such low levels of impurities that intrinsic defects become more and more important. In this paper we will present our current understanding on deep centers in SiC from optical measurements in the infrared region. The focus will be on the intrinsic and so far unidentified deep centers but also deep centers from impurities will be briefly discussed. The most common defects observed are vanadium, chromium and the silicon vacancy related defect centers together with a number of so far unidentified defect centers labeled I-1, UD-1, UD-2, UD-3 and UD-4. The annealing of the defect centers and their possible origin will be discussed based on optical measurements combined with positron annihilation lifetime, magnetic resonance, and electrical measurements. Results from different perturbation techniques (magnetic field, temperature, polarization, excitation dependence) also give additional information about the deep centers.

11:15 AM
Investigation of the Electronic Structure of the UD4 Defect in 4H-SiC by Optical Techniques: *Aurelie Thuaire*[1]; Anne Henry[2]; Björn Magnusson[3]; Peder Bergman[3]; Erik Janzen[2]; Michel Mermoux[4]; Edwige Bano[5]; [1]LEPMI- IMEP - INPG - France / IFM - Linköping University - Sweden; [2]IFM - Linköping University - Sweden; [3]IFM - Linköping University / Norstel; [4]LEPMI - INPG - France; [5]IMEP - INPG - France

A detailed investigation on the optical and electronic properties of the deep-level defect UD4 is reported. This defect has recently been observed in 4H semi-insulating silicon carbide, but it has hardly been studied yet. Both low temperature and temperature-dependent photoluminescence (PL) were collected from the defect. The PL spectra show three main lines, assigned to no-phonon (NP) lines, at 846nm (Ua1), 888.7nm (Ub2) and 889.3nm (Ub1). Further lines appear when temperature is raised. Zeeman spectroscopy measurements were performed as well as time-resolved photoluminescence. The Zeeman spectroscopy results show that the high and low-temperature lines are splitting and shifting when a magnetic field is applied. Their behavior is however strongly dependent on both the orientation of the magnetic field and the detection polarization. The results indicate that the UD4 defect could be associated with an isoelelectronic center.

11:30 AM
Relationship between IR Photoluminescence and Resistivity in Semi-Insulating 6H SiC: Sashi K. Chanda[1]; *Yaroslav Koshka*[1]; Murugesu Yoganathan[2]; [1]Mississippi State University; [2]Wide Band Gap Materials Group, II-VI, Inc.

A combination of room temperature PL mapping and low-temperature PL spectroscopy was applied to establish the origin of resistivity variation in PVT-grown 6H SiC substrates. A direct correlation between the native defect-related PL and resistivity was found in undoped (V-free) samples, indicating that native point defects are associated with the compensation mechanism in the undoped SI substrates and resistivity distribution across the wafer. In vanadium-doped samples with low vanadium content, both the V-related PL and the native point defect-related PL were observed simultaneously with their relative strength varying from wafer to wafer. There was no clear correlation between the resistivity and the PL intensity measured at either of the two PL peaks. At the same time, the resistivity showed a good correlation with the total PL signal. Thus, the resistivity of these wafers is likely to be due to the contribution of both V-related and native point defect-related deep levels. Analysis of the low temperature spectra will be reported in order to identify specific defects responsible for the observed trends in PL mapping. A complex temperature dependence of the main PL peaks will be investigated in order to reveal various recombination channels influencing PL spectra.

11:45 AM
Defect Level and Defect Relaxation Studies of V_c^+ in Semi-Insulating 4H SiC: *Haiyan Wang*[1]; Mary Ellen Zvanut[1]; [1]University of Alabama at Birmingham

Recently, photo-induced electron paramagnetic resonance (photo-EPR) has been used to study the plus-to-neutral transition of the carbon vacancy in 4H SiC. The present results add new insight into the earlier reports by considering defect relaxation and including time-dependent measurements. We conducted photo-induced electron paramagnetic resonance (photo-EPR) studies of high purity semi-insulating 4H SiC by illuminating the sample with light of selected energy at 4 K. The intensity change of the positively charged carbon vacancy EPR signal enabled us to estimate the defect level for the plus-to-neutral transition. The time-dependent photo-EPR data suggest that when V_c^+ captures an electron from the valence band becoming V_c^0 the optical ionization energy required is about 1.9 eV, and when V_c^0 releases an electron to the conduction band becoming V_c^+ the energy required is 2.3 eV. Initial analysis indicates that lattice relaxation accounts for the energy difference between the plus-to-neutral and neutral-to-plus states. Thus, the average lattice relaxation energy is estimated at about 0.47 eV, within range of preliminary theoretical values. At the presentation, we will consider the influence of other centers and discuss additional support for the defect relaxation model.

12:00 PM
On the Existence of Carbon Split-Interstitials in Electron-Irradiated n-Type 6H-SiC: *M. V.B. Pinheiro*[1]; Siegmund Greulich-Weber[2]; U. Gerstmann[2]; E. Rauls[3]; H. Overhof[2]; J.-M. Spaeth[2]; [1]Universidade Federal de Minas Gerais; [2]University of Paderborn; [3]Institute of Physics and Astronomie

Since the dopant atoms only hardly diffuse into SiC, other methods like ion implantation are necessary, but results in various radiation-induced defects. Technologically high temperature annealing is used to reduce these unwanted by-products, to obtain high free carrier concentrations. However, valuable information can be obtained from the unannealed samples, which provide good insight in the annealing process. Mobile split-interstitials, either intrinsic ones like the carbon split-interstial $(CC)_C$ or those in connection with dopants, e.g. $(NC)_C$, are well known to play a central role in the beginning of the annealing process, but these had not been identified yet. In irradiated p-type SiC, the carbon split-interstitial has been suggested for the EI1/EI1' (S=1/2) as well as for the EI3/EI3' (S=1) centers in C1h symmetry, but so far an unambiguous assignment was not possible. In this work, from electron paramagnetic resonance and theoretical investigations we present strong arguments (e.g. an observed EPR-line with resolved hyperfine splittings due to 2+2 Si-ligands) for the existence of carbon split-interstials within C_{2v} symmetry in unannealed irradiated n-type 6H-SiC.

12:15 PM
Deep Level Near E_C-0.55 eV in Undoped 4H-SiC Substrates: *William C. Mitchel*[1]; William D. Mitchell[1]; Steven R. Smith[1]; Andrew Evwaraye[2]; Zhaoqiang Fang[1]; David Look[1]; Sizelove John[1]; [1]Air Force Research Laboratory; [2]University of Dayton

A variety of developmental undoped 4H-SiC samples from crystals grown by the physical vapor transport technique have been studied by temperature dependent Hall effect, optical and thermal admittance spectroscopy and thermally stimulated current. Free carrier type and activation energies were determined from the Hall effect measurements in samples with a strong Hall voltage. In all cases with a measureable Hall voltage the samples were n-type, indicating that the Fermi level is pinned in the upper half of the band gap. In most samples studied here the activation energies were in the range 0.9 - 1.6 eV expected for commercial grade HPSI 4H-SiC. However, in several samples a previously unreported deep level at EC -0.55 ± 0.01 eV was observed. Thermal admittance spectroscopy detected one level with an energy of about 0.53 eV while optical admittance spectroscopy measurements resolved two levels at 0.56 and 0.64 eV. Thermally stimulated current measurements made to study compensated levels in the material detected several peaks at energies in the range 0.2 to 0.6 eV. The possible role of the 0.55 eV level and other deep levels in the compensation mechanism of HPSI 4H-SiC will be discussed.

12:30 PM Introduction to Invited Poster (Point Defects)
Deep Level Point Defects in Semi-Insulating SiC: Mary Ellen Zvanut[1]; [1]University of Alabama at Birmingham

TB2.EPI II: Defect Reduction Growth Mechanisms

Tuesday, 10:45am-12:40pm
September 20, 2005

Room: Allegheny Ballroom II & III
Location: Westin Pittsburgh

Session Chairs: H. Matsunami, Kyoto University; O. C. Kordina, Caracal, Inc.

10:45 AM Invited
Techniques for Minimizing the Basal Plane Dislocation Density in SiC Epilayers to Reduce Vf Drift in SiC Bipolar Power Devices: *Joseph John Sumakeris*[1]; Mrinal K. Das[1]; Seoyong Ha[2]; Christer Hallin[3]; Brett Hull[1]; Hans Lendenmann[4]; Michael J. Paisley[1]; Marek Skowronski[2]; H. McD. Hobgood[1]; John Palmour[1]; Calvin Carter[1]; [1]Cree, Inc.; [2]Carnegie Mellon University; [3]Linkopings University; [4]ABB AB

Forward voltage instability, or Vf drift, has confounded high voltage SiC device makers for the last several years. The SiC community has recognised that the root cause of Vf drift in bipolar SiC devices is the expansion of basal plane dislocations (BPDs) into Shockley stacking faults within device regions that experience conductivity modulation. In this presentation, we detail relatively simple procedures that reduce the density of Vf drift inducing BPDs in epilayers to < 10 cm^{-2} and permit the fabrication of bipolar SiC devices with very good Vf stability. The first low BPD technique employs a selective etch of the substrate prior to epilayer growth to create a near on-axis surface where BPDs reach the substrate surface. The second low BPD technique employs lithographic patterning of the substrate prior to epilayer growth. Both processes impede the propagation of BPDs into epilayers by preferentially converting BPDs into threading edge dislocations during the initial stages of epilayer growth. With these techniques, we routinely achieve Vf stability yields of up to 90% in devices with active areas from 0.006 to 1 cm^2, implying that the effectiveness of the processes does not vary with device size.

11:15 AM
Comparison of Propagation and Nucleation of Basal Plane Dislocations in 4H-SiC(000-1) and (0001) Epitaxy: *Hidekazu Tsuchida*[1]; Isaho Kamata[1]; Toshiyuki Miyanagi[1]; Tomonori Nakamura[1]; Koji Nakayama[2]; Ryousuke Ishii[1]; Yoshitaka Sugawara[2]; [1]CRIEPI; [2]KEPCO

Propagation and nucleation of basal plane dislocations (BPDs) in 4H-SiC(000-1) and (0001) epitaxy were compared. Synchrotron reflection X-ray topography was performed before and after epitaxial growth to classify the BPDs into those propagated from the substrate into the epilayer and those nucleated in the epilayer. It was revealed that (000-1) epitaxy is significantly advantageous in preventing the propagation of BPDs from the substrate into epilayer compared to (0001) epitaxy. In the case of (000-1) epitaxy, the density of BPDs propagated from the substrate is smaller than that of those nucleated in the epilayer. Growing (000-1) epilayers at a high C/Si ratio of 1.2 achieves a further reduction in BPDs to only 3 cm^{-2} for those propagated from the substrate and 16 cm^{-2} for those nucleated in the epilayer. A dramatic increase was also found in nucleation of BPDs omitting the re-polishing and in-situ H_2 etching procedure.

11:30 AM
'Switch-Back Epitaxy' as a Novel Technique for Reducing Stacking Faults in 3C-SiC: *Kuniaki Yagi*[1]; Takamitsu Kawahara[1]; Naoki Hatta[1]; Hiroyuki Nagasawa[1]; [1]HOYA Advanced Semiconductor Technologies

Previously, we reported a method to reduce planar defects in 3C-SiC (001) by growing it on an undulant Si with counterslopes oriented in the [110] and [-1-10] directions. With 3C-SiC growth, stacking faults exposing the C-face on the surface [SF(C)] vanished, while those exposing the Si face [SF(Si)] gradually decreased by combining with each other. Consequently, only SF(Si) remained on the 3C-SiC (001) surface. To eliminate the residual SF(Si), an additional homoepitaxial layer must be grown on 3C-SiC after converting the SF polarity from the Si face to the C face. The simplest way to accomplish this is to turn the 3C-SiC (001) substrate over after removing the undulant Si. In other words, if an additional homoepitaxial layer is grown on the back of a self-standing 3C-SiC substrate grown on an undulant-Si substrate, the surface polarity of SF is kept as the C-face, and an SF-free 3C-SiC surface is easily obtained. In this paper, we refer to the aforementioned SF-elimination method as switch-back epitaxy (SBE), and the efficacy of SBE is discussed by referring to morphological and electrical observations.

11:45 AM Invited
Reduction of Defects in GaN Epitaxial Films Grown Heteroepitaxially on SiC: *Charles R. Eddy*[1]; Ronald T. Holm[1]; Richard L. Henry[1]; James C. Culbertson[1]; Mark E. Twigg[1]; [1]U.S. Naval Research Laboratory

Silicon carbide (SiC) has become the substrate of choice for III-N epilayers applied to electronic devices due to the lack of a native III-N substrate. This is particularly true for high power applications since the thermal conductivity of the substrate enhances device performance. Although the GaN lattice match is slightly better for SiC than for sapphire, resulting dislocation densities are still very high – generally in the high 10^8 cm^{-2} range. These defects deteriorate device performance. Screw-component dislocations are especially critical since they serve as leakage paths in vertically conducting III-N devices. In this presentation efforts to reduce the extended defect density in III-N films grown on SiC are reviewed. Details on recent efforts to use step-free SiC surfaces are highlighted showing dramatic reductions in extended defect densities and the virtual elimination of critical defects for vertically conducting devices. In these efforts, SiC surfaces that are step-free or of very low step density have been used to grow thin (<3µm) GaN films on a 100nm AlN nucleation layer that possess total dislocation densities two orders of magnitude lower than the previous state-of-the-art with no evidence of screw-component dislocations. Finally, possible future directions will be discussed.

12:15 PM
Composition Effects on Stress Evolution during MOCVD Growth of AlGaN on SiC: *Jeremy Acord*[1]; Srinivasan Raghavan[1]; Xiaojun Weng[1]; Elizabeth C. Dickey[1]; David W. Snyder[2]; Joan M. Redwing[1]; [1]Pennsylvania State University; [2]Applied Research Laboratory

The growth of high Al-fraction (x>0.3) $Al_xGa_{1-x}N$, which is of interest for deep-UV emitter applications, is challenging due to defect formation and film cracking which become more problematic with increasing Al-fraction. Cracking is influenced by epitaxial and thermal expansion mismatches between $Al_xGa_{1-x}N$ films deposited on heteroepitaxial substrates, and also between $Al_xGa_{1-x}N$ layers with different composition within the same structure. Less obvious and equally important are growth-related stresses due to film morphology development such as island coalescence and grain growth. The magnitude and evolution of stress during MOCVD growth of $Al_xGa_{1-x}N$ ($0 \le x \le 0.78$) on SiC substrates using AlN buffer layers was investigated by substrate curvature based in-situ stress measurements. The stress evolution characteristics were found to fall into three distinct regimes based on film composition. Gallium-rich (x<0.1) films initially grew in compression, which relaxed with increasing film thickness. Intermediate Al-fraction samples ($0.16 \le x \le 0.61$) initially grew in compression, which was measured to transition into tension with increasing film thickness. Finally, a sample in the Al-rich regime (x=0.78) exhibited tensile stress from the start of growth, despite a predicted compressive epitaxial mismatch with the AlN buffer layer. The results are interpreted in terms of epitaxial misfit, grain coalescence and morphological evolution during growth.

12:30 PM Introduction to Invited Poster (EPI II)
Investigation of In-Grown Dislocations in 4H-SiC Epitaxial Layer: *Kazutoshi Kojima*[1]; Tomohisa Kato[1]; Satoshi Kuroda[1]; Hajime Okumura[1]; Kazuo Arai[1]; [1]AIST

Lunch

Tuesday, 12:40-1:50pm
September 20, 2005

Room: Spirit of Pittsburgh
Location: Convention Center

TP.Tuesday Poster Sessions

Tuesday, 1:50-4:10pm
September 20, 2005

Room: Spirit of Pittsburgh Foyer
Location: Convention Center

TPG1.EPI II

Invited
Investigation of In-Grown Dislocations in 4H-SiC Epitaxial Layer: *Kazutoshi Kojima*[1]; Tomohisa Kato[1]; Satoshi Kuroda[1]; Hajime Okumura[1]; Kazuo Arai[1]; [1]AIST

We have investigated the generation of new dislocations during the epitaxial growth of 4H-SiC layer. Dislocations were mainly propagated from the substrate into epitaxial layer. However, it was found that some amount of new

threading edge dislocations and basal plane dislocations were generated during the epitaxial growth. On the other hand, screw dislocations were not generated during the epitaxial growth. This results indicate that the etch pit density of the epitaxial layer may be increased compared with that of the substrate. The generation of those dislocations was indicated to depend on in-situ H2 etching condition and not depend on the epitaxial growth condition. It is considered that the roughness of the substrate surface after in-situ H2 etching affects the generation of new dislocations in the epitaxial layer. By optimizing in-situ H2 etching condition, we can well suppress the generation of new dislocations during epitaxial growth, and obtain 4H-SiC epitaxial layers which have the equivalent etch pit density to the substrates.

High Purity SiC Epitaxial Growth by Chemical Vapor Deposition Using CH_3SiH_3 and C_3H_8 Source: *Tomoaki Hatayama*[1]; [1]Nara Institute of Science and Technology

We described the epitaxial growth of SiC by a hot-wall CVD system using monomethylsilane (CH_3SiH_3) as a precursor. In the case of CH_3SiH_3 source only, single-crystalline 4H-SiC can be homoepitaxially grown, and undoped epilayers on the (0001) Si face showed n-type conduction around 10^{16}-$10^{17}cm^{-3}$. Many pits with the density over 10^5cm^{-2} were observed. From these results, it seems to be a Si-rich growth condition. To improve the quality of epilayers, C_3H_8 was simultaneously supplied with the CH_3SiH_3 source during the growth. Though a growth rate was unchanged at about 5μm/h, the pit density can reduce from 10^5 to 10^4cm^{-2} with the additional C_3H_8 supply at 0.78sccm. At the high C_3H_8 flow rate up to 1.4sccm, the pit density could reduce more below 10^3cm^{-2}. The above results suggest that the growth parameter shifts from Si-rich to C-rich conditions with the additional C_3H_8 supply. With the increase of C_3H_8 flow rate, a reduction of donor concentration was observed. A low donor concentration of $1.6\text{-}2.3\times10^{14}cm^{-3}$ was achieved by the simultaneous supply of CH_3SiH_3 and C_3H_8 at 16kPa. The suppression of residual nitrogen incorporation into the epilayer was realized by a C-rich growth condition, indicating the site-competition effect.

Homoepitaxial Growth of Iron-Doped 4H-SiC Using BTMSM and t-Butylferrocene Precursors for Semi-Insulating Property: *Ho Keun Song*[1]; Sang Yong Jung[1]; Hoon Joo Na[1]; Jeong Hyun Moon[1]; Jeong Hyuk Yim[1]; Hyeong Joon Kim[1]; [1]Seoul National University

In this paper, we attempted to grow semi-insulating SiC epitaxial layer by in-situ iron doping. Homoepitaxial growth of iron-doped 4H-SiC layer was performed by MOCVD using organo-silicon precursor, bis-trimethylsilylmethane (BTMSM, [$C_7H_{20}Si_2$]) and metal organic precursor, t-butylferrocene ([$C_{14}H_{17}Fe$]). Doping-induced crystallinity degradation showed different tendency with conducting type of substrate. The crystal quality of epilayer grown on n-type substrate was not degraded significantly despite of the Fe doping but in case of semi-insulating substrate, crystallinity was remarkably degraded as increasing iron contents. For measurement of resistivity of highly resistive iron-doped 4H-SiC epilayer, we used the on-resistance and this technique is firstly attempted for measuring resistivity of epilayer. From on-resistance of epilayer measured by I-V, it is shown that the residual donor concentration of epilayer was decreased as increasing partial pressure of t-butylferrocene. The resistivity of iron-doped 4H-SiC epilayer was about 10^7 Ocm. From this result, it is supposed that Fe could effectively act as a compensation center in the iron-doped 4H-SiC.

Optimization of Epitaxial Layer Growth by Schottky Diodes Electrical Characterization: Francesco La Via[1]; *Giuseppa Galvagno*[1]; Fabrizio Roccaforte[1]; Lucia Calcagno[2]; Gaetano Foti[2]; Giuseppe Abbondanza[3]; Maurizio Masi[4]; Danilo Crippa[5]; [1]CNR-IMM; [2]Catania University; [3]Epitaxial Technology Center; [4]Politecnico di Milano; [5]LPE

The influence of the epitaxial layer growth parameters on the electrical characteristics of Schottky diodes has been studied in detail. The epitaxial layers were characterized using several techniques to measure the defect density and some physical parameters (thickness, uniformity, roughness, dopant concentration…). The diodes were characterized by I-V and C-V maps on the entire wafer to obtain statistical information and spatial distribution of defects. In a first set of experiments several diodes were realized on different epitaxial layers grown with different Si/H2 ratio and then with different growth rate. From the electrical characterization a maximum silicon dilution ratio can be fixed to 0.04 %. This limit fixes also a maximum growth rate that can be obtained in the epitaxial growth, with this process, to about 8 μm/h. Several epitaxial layers have been grown, using this dilution ratio, with different temperatures (1550 ÷ 1650°C). At 1600°C the best compromise between the direct and the reverse characteristics has been found. With this process the yield decreases from 90% for an area of 0.25 mm^2 to reach the 61% for the 2 mm2 diodes.

Using Vapour-Liquid-Solid Mechanism for SiC Homoepitaxial Growth on On-Axis 6H-SiC (0001) at Low Temperature: *Gabriel Ferro*[1]; Maher Soueidan[1]; François Cauwet[1]; Laurent Mollet[1]; Christophe Jacquier[1]; Ghassan Younes[2]; Yves Monteil[1]; [1]Laboratoire des Multimatériaux et Interfaces; [2]Beirut Arab University

Vapour-Liquid-Solid mechanism was used for growing epitaxial SiC layers on on-axis 6H-SiC and 4H-SiC substrate. By feeding Al70Si30 melts with propane, homoepitaxial growth was demonstrated down to 1100°C on both polytypes. The surface morphology is rough and non uniform with spiral growth forming large hillocks at the places where screw dislocation emerges from the substrate. Raman spectroscopy confirms the absence of 3C-SiC polytype and shows the high Al doping of the layers. This growth temperature of 1100°C is the lowest one ever reported for growing homoepitaxial layers on low tilt angle SiC substrates.

Growth of 3C-SiC on Si Molds for MEMS Applications: *M. Reyes*[1]; M. Waits[2]; S. P. Rao[1]; Y. Shishkin[1]; B. Geil[2]; J. T. Wolan[1]; S. E. Saddow[1]; [1]University of South Florida; [2]ARL/SEDD

3C-SiC has been grown on MEMS structures formed by DRIE of (100) Si in a horizontal hot-wall CVD reactor capable of growth on 100mm wafers. The process consists of silane/propane/hydrogen chemistry with HCl used as a growth additive to increase the growth rate. The deposition experiments were carried out using a carbonization step (760Torr, 1170°C) followed by the growth of the 3C-SiC film (200Torr, 1375°C). The preliminary growth rate achieved was 6.6 μm/h, which is approximately double the growth rate achieved without the HCl additive for the same process in the same system. X-ray rocking curve data collected on a 3.3μm thick 3C-SiC film grown at a speed of 6.6 μm/h displayed a FWHM of ~500arcsec which is comparable to values reported in the literature thus confirming the structural integrity of the 3C-SiC film. Cross-sectional SEM analysis after 3C-SiC deposition revealed the film coverage was smooth and uniform at the bottom of ~65μm deep etched trenches. On the trench walls, the film thickness decreased from the top of the trench to the bottom. AFM surface measurements indicated a roughness of ~4nm rms on the top of the trenches. Details of the growth process and film characterization will be presented.

SiC-4H Epitaxial Layer Growth by Trichlorosilane (TCS) as Silicon Precursor: Francesco La Via[1]; *Stefano Leone*[2]; Marco Mauceri[2]; Giuseppe Abbondanza[2]; Maurizio Masi[3]; Danilo Crippa[4]; Riccardo Reitano[5]; Gaetano Foti[6]; [1]CNR-IMM; [2]Epitaxial Technology Center; [3]Politecnico di Milano; [4]LPE; [5]Catania University; [6]Catania University

4H-SiC epitaxial layers have been grown using trichlorosilane (TCS) as silicon precursor source together with ethylene as carbon precursor source. A higher C/Si ratio is necessary to be used compared with the silane/ethylene system. This ratio has to be reduced especially at higher Si/H2 ratio because step-bunching effect occurs. From the comparison with the process that uses silane as silicon precursor, it has been found a 15% higher growth rate using TCS (trichlorosilane) at the same Si/H2 ratio. Furthermore in the TCS process, the presence of chlorine, that reduces the possibility of silicon droplets formation, allows to use high Si/H2 ratio and then to reach high growth rate (16 μm/h). Although the obtained results on the growth rates and the surface roughness are very promising, further optimization of the process is needed to obtain epitaxial layers with good crystal and electrical quality.

Hetero-Epitaxial Growth of 3C-SiC on Silicon Substrates by Plasma-Assisted CVD: Hideki Shimizu[1]; *Yosuke Aoyama*[1]; [1]Aichi University of Education

3C-SiC films grown on carbonized Si (100) by plasma-assisted CVD have been investigated with systematic changing the flow rate of monosilane (SiH4) and propane (C3H8) as source gases. The deposition rate of the films increased monotonously and the microstructures of the films changed from 3C-SiC single crystal to 3C-SiC polycrystal with increasing the flow rate of SiH4. Increasing of C3H8 keep single crystalline structure but results in contamination of α-W2C which is serious problem for the epitaxial growth. To obtain high quality of 3C-SiC films by plasma-assisted CVD, the effects of C3H8 on the microstructures of the films have been investigated by reducing the concentration of C3H8. Good quality 3C-SiC single crystal on Si (100) is grown at low net flow rate of C3H8 and SiH4, while 3C-SiC single crystal on Si (111) is grown at low net flow rate of C3H8 and high net flow rate of SiH4. It is expected that 3C-SiC epitaxial growth on Si (111) is higher deposition rate and lower substrate temperature than that on Si (100). The microstructures and the thickness of the films were investigated by reflection electron diffraction, X-ray diffraction and an ellipsometric measurement respectively.

A Simple Method to Synthesize Nano-Sized 3C-SiC Powder Using Hexamethyldisilane: *Chacko Jacob*[1]; Aparna Gupta[1]; [1]Indian Institute of Technology

In this paper, we report the synthesis of nano-sized cubic silicon carbide (3C-SiC) powder by chemical vapor deposition (CVD) technique in a resistance-heated furnace. The nanoparticles were deposited on the relatively cold region of a hot-wall quartz reactor. Hexamethyldisilane (HMDS) was used as the single source material for both silicon and carbon. The presence of crystalline phase of 3C-SiC was identified using powder X-Ray Diffraction (XRD) technique. From XRD data, the particle size was also estimated in the range of nanometer (nm). The vivid evidence of particle size (~ 10 - 100 nm) was obtained in transmission electron microscopy (TEM) image. Selected area electron diffraction (SAED) was carried out on the nanoparticle assembly showing ring shaped pattern as a clear indication of polycrystalline particle

formation. High resolution TEM (HRTEM) of nanoparticles was performed to study the crystal structure and defects. Finally, the nanoparticles were characterized by Raman study at room temperature.

Selective Epitaxial Growth of 3C-SiC on Si Using Hexamethyldisilane in a Resistance Heated MOCVD Reactor: *Aparna Gupta*[1]; Chacko Jacob[1]; [1]Indian Institute of Technology

3C-SiC epitaxial growth was performed on a patterned Si (100) substrate using Hexamethyldisilane (HMDS) in an inexpensive MOCVD reactor. The reactor has been built around a resistance-heated furnace. HMDS was used as the single source for both Si and C though propane was available for the preliminary carbonization step. Hydrogen was used as the carrier gas and argon was used for purging. It was observed that voids are the major defect in case of heteroepitaxial growth of 3C-SiC on Si. Using selective epitaxial growth (SEG), this problem has been solved. The effect of temperature, window shape and size, precursor concentration, etc. on the SEG of SiC has been studied. After growth, films have been characterized by Nomarski optical microscopy, SEM, Raman spectroscopy and AFM. Faceted growth was observed along (111) planes inside smaller windows. Raman spectroscopy was used to further study the films.

Homoepitaxial Growth and Characterization of 4H-SiC Epilayers by Low-Pressure Hot-Wall Chemical Vapor Deposition: *Guosheng Sun*[1]; Jin Ning[1]; Quancheng Gong[1]; Xin Gao[1]; Lei Wang[1]; Xinfang Liu[1]; Yiping Zeng[1]; Jinmin Li[1]; [1]Institute of Semiconductors, Chinese Academy of Sciences

Horizontal air-cooled low-pressure hot-wall CVD (LP-HWCVD) system is developed to get high quality 4H-SiC epilayers in the authors' group. Homoepitaxial growth of 4H-SiC on off-oriented Si-face (0001) 4H-SiC substrates purchased from Cree is performed at a typical temperature of 1500 degrees with a pressure of 40 Torr by using CH4+C2H4+H2 gas system. The typical growth rate was controlled to be about 1.0 micron/h. The surface morphologies and structural and optical properties of 4H-SiC epilayers are characterized with Nomarski optical microscope, atomic force microscopy (AFM), x-ray diffraction, Raman scattering, and low temperature photoluminescence (LTPL). The background doping has been reduced to 2-5x10^15 cm^-3. The FWHM of the rocking curve was 0.33 nm in 10 micron x□10 micron scale. Intentional N-doped and B-doped 4H-SiC epilayers have been obtained by in-situ doping of NH3 and B2H6, respectively. Schottky barrier diodes with reverse blocking voltage of over 1000 V were achieved preliminarily.

Dependence of Dielectric Properties of (SiC)1-x(AlN)x Alloys on the Concentration of AlN: *Gadjemet Safaraliev*[1]; Bilal Bilalov[1]; Shaban Shabanov[1]; Sadyk Sadykov[1]; Gulnara Kardashova[1]; Suleyman Kallaev[1]; [1]Dagestan State University

In the present work, detailed study of concentration dependence of dielectric properties (effective dielectric constant and dielectric losses (SiC)1-x(AlN)x alloys in the frequency range from 0,1 kHz up to 1 MHz was performed. Our results confirm abnormal high values effective dielectric constant for structures with AlN substance of 30 and 50 % weight, whereas for the structures with AlN substance more than 50 % weight effective dielectric constant coincides to that of AlN ceramics. Possible mechanisms of abnormally high values of dielectric constant of (SiC)1-x(AlN)x alloys and their huge relaxation at high frequencies are discussed.

Growth of Epitaxial Al_2O_3 Thin Films on 4H-SiC: *Carey M. Tanner*[1]; Jane P. Chang[1]; [1]UCLA

Epitaxial oxides on wide bandgap semiconductors such as SiC have the potential to improve the performance of power metal-oxide-semiconductor field effect transistors due to enhanced dielectric strength and stability. The hexagonal α-Al_2O_3 phase can be lattice-matched to the 4H-SiC (0001) surface within 3.4% by considering two Al_2O_3 unit cells for every three SiC unit cells. Epitaxial α-Al_2O_3 growth on 4H-SiC is investigated by atomic layer deposition (ALD) and molecular beam epitaxy (MBE) techniques. The surface structure and compositions are determined by *in-situ* reflection high energy electron diffraction (RHEED) and x-ray photoelectron spectroscopy to assess the effects of substrate temperature and precursor dosage on the film properties. *In-situ* annealing in ultra-high vacuum and O_2 at 600-1000°C is investigated as a method to control the Al_2O_3 film structure. The nature of the interface and the crystalline properties of the film are studied by high-resolution transmission electron microscopy and x-ray diffraction. Band alignment at the Al_2O_3/SiC interface is determined from the XPS analysis and compared with photoconductivity measurements.

Magnetron Sputtering of Thin (SiC)1-X(AlN)X Films of Various Atomic Structure: *Gadjemet Safaraliev*[1]; Bilal Bilalov[1]; Gennadiy Kuznetsov[2]; Sergey Simakin[3]; [1]Dagestan State University; [2]Moscow State Institute of Steel and Alloys; [3]LTD Iontec C

In the present work the opportunity of solid films (SiC)1-X(AlN)X produced with magnetron ionic sputtering is considered. Polycrystalline layers (SiC)1-X(AlN)X produced by hot pressing method were used as a target material. The monocrystalline 6H (0001) silicon carbide polished plates (Lely technique) were used as substrates.The speed of target (SiC)1-X(AlN)X sputtering depending on the discharge power for three structures (x = 0,1; 0,3 and 0,5) was calculated. XRD investigations have shown that a film grown at temperature 500ºC has amorphous structure. At temperature 700-800ºC the structure is polycrystalline, and at 900-1000ºC monocrystal layers are formed. The possibility of making monocrystalline layers of wide bandgap alloys (SiC)1-X(AlN)X (x = 0,1 is shown; 0,3 and 0,5) on substrates 6H-SiC by ionic sputtering of a polycrystalline target of similar structure with the use of magnetron systems.

Low Temperature Growth of Crystallized SiC Thin Films by PECVD: *Wang Rose*[1]; [1]Beihang University

Silicon carbide (SiC) has attracted great interest for the production of devices able to work in extreme conditions due to its excellent properties such as wide band gap, high breakdown voltage, electron mobility, thermal conductivity and good hardness. In the last decade, several routes have been explored to obtain high quality ß-SiC thin films on silicon substrates. However, the preparations of ß-SiC thin films by chemical vapor deposition (CVD) were still carried out in a high-temperature environment. Recently, it has been found that enhancing the activity of the precursors is beneficial to reduce the substrate temperature. In this work, by introducing highly dense of hydrogen into the working gases, crystallized SiC thin films were successfully prepared at low substrate temperature by PECVD on Si (100) substrates. It was found that the thin films deposited at 500°C presented (111), (220), and (311) characteristic diffraction peaks of ß-SiC phase. Our results indicated that crystallized SiC thin films could be obtained at low substrate temperature, which could be resulted from the introduction of the activated hydrogen radical. The underlying mechanisms of hydrogen on the crystallization of the thin films are discussed in details.

Increased Growth Rates of 4H-SiC for Silane-Propane-Hydrogen System in Vertical Cold Wall Reactor using HCl: *Christopher Ian Thomas*[1]; MVS Chandrashekhar[1]; Yuri Makarov[2]; Michael G. Spencer[1]; [1]Cornell University; [2]Widetronics

Growth of SiC epitaxial layers from silane and propane has been analyzed and realized for growth conditions achievable in a resistively heated cold wall rotating disk reactor. In this study, we will show theoretically and experimentally that high growth rates are possible with the addition of chlorine containing species. HCl addition gives rise to significant improvement of the SiC CVD process in a typical cold-wall reactor. For the regime tested, increases from 2.4 to ~ 7-8 microns per hour were observed with a maximum demonstrated growth rate of 15um/hr. Silicon nucleation is suppressed and saturation of the growth rate is not observed, indicating the possibility of even higher growth rates. In addition, we will show that the layer quality is improved and silicon droplets are not observed for a wide range of C/Si ratios.

Investigation of 3C/4H-SiC Polytype Heterojunction: *Christopher Ian Thomas*[1]; M. V.S. Chandrashekhar[1]; Michael Spencer[1]; [1]Cornell University

Unintentionally doped epitaxial layers were grown on both the Silicon and Carbon faces of conductive and semi-insulating (0001) 4H-SiC. The substrates were nominally on axis and CMP polished. The growth rate, C/Si ratio, and growth temperature were varied from .2-2.5um/hr, .5-1.5, 1400-1600°C respectively. The samples were studied using optical and electron microscopy. The morphology of the films grown on both the Si and C faces is consistent with the formation of 3C-SiC. In many of the films boundaries between " growth islands" are clearly visible at the surface. Room temperature and low temperature (liquid nitrogen/liquid helium) capacitance-voltage (C-V) and Hall measurements were used to investigate the electrical property of the material. Hall effect studies on films grown on conducting substrates were performed at liquid helium temperatures in order to eliminate the substrate conductivity. Hall effect measurements on films grown on the semi-insulating substrates were measured at liquid nitrogen temperatures. Initial results have shown that charge is present only on samples grown on the C face. The best sample has shown a persistent mobile charge of ns=2.5x1013 cm^{-2}, with an associated mobility of μ=300 cm^2/Vs. In this presentation we will show additional materials characterization results and details of the growth.

TPP1.MOS Processing

Off-Angle Dependence of Characteristics of 4H-SiC-Oxide Interfaces: *Yasuto Hijikata*[1]; Hiroyuki Yaguchi[1]; Sadafumi Yoshida[1]; Yasutaka Takata[2]; Keisuke Kobayashi[3]; Hiroshi Nohira[4]; Takeo Hattori[4]; [1]Saitama University; [2]RIKEN /SPring-8; [3]JASRI/SPring-8; [4]Musashi Institute of Technology

SiC-Oxide interfaces on 4H-SiC epitaxial substrates of various off-angles have been characterized by C-V measurements, synchrotron radiation excited photoemission spectroscopy and atomic force microscopy. The interface state density (N_{it}) and the amount of sub-oxides (S_i) for small off-angle substrates were smaller than those for large off-angle ones. Furthermore, there is a good correlation between the amount of the interface states and that of sub-oxides. Step-terrace structures were clearly observed in the surface morphology after

the removal of oxide layer, which shows that the interfaces were atomically smooth. These results suggest that the reductions in N_{it} and S_i should relate to the smoothness of the interface and the high performance SiC MOS devices are expected by using small off-angle substrates.

PECVD Deposited TEOS for Field-Effect Mobility Improvement in 4H-SiC MOSFETs on the (0001) and (11-20) Faces: *Amador Perez-Tomas*[1]; [1]Centre Nacional de Microelectronica - CNM-CSIC

Very high field-effect mobilities have been extracted for planar inversion 4H-SiC MOSFETs with deposited SiO_2-TEOS gate oxides. Mobilities of around 216 cm^2/Vs have been extracted for (11-20) 4H-SiC MOSFETs with gate definition using thermal oxidation at 1050ºC during 1h and a subsequent deposition of SiO_2 with TEOS as source material. MOSFET devices have also been fabricated on the (0001) Si face. In this case, depending on the SiO_2 deposition conditions, the mobility improvement (up to 38-45 cm^2/Vs) is also remarkable, when compared with a dry thermal oxidized gate oxide (5 cm^2/Vs) . In the most favorable conditions, the mobility improvement seems to be related with the current leakage more than (or along with) an interface traps reduction of the gate insulator interface. This last statement agrees with the high value of the sub-threshold slope measured in the high mobility devices or with the presence of oxide charges that provokes a shift of the threshold voltage. The exact nature of this very important mobility enhancement is currently under investigation. The real applicability and the reproducibility of these devices seems to be the most critical issues. However, the phenomena observed in our devices could be linked with other previously reported mobility improvements.

Low-Temperature Post-Oxidation Annealing Using Hydrogen Radicals Generated by High-Temperature Catalyzer for an Improvement in Reliability of Thermal Oxides on 4H-SiC: *Junji Senzaki*[1]; Atsushi Shimozato[1]; Kenji Fukuda[1]; [1]National Institute of Advanced Industrial Science and Technology

Low-temperature post-oxidation annealing (POA) process of high-reliability thermal oxides grown on 4H-SiC using new apparatus that generates hydrogen radicals by high-temperature catalyzer has been investigated. Hydrogen radicals were generated by thermal decomposition of H_2 gas at the catalyzer surface heated at high temperature of 1800°C, and then exposed to the sample at 500°C in reactor pressure of 20 Pa. The mode and maximum values of field-to-breakdown (E_{BD}) are 11.0 and 11.2 MV/cm, respectively, for the hydrogen radical exposed sample. In addition, the charge-to-breakdown (Q_{BD}) at 63% cumulative failure of the thermal oxides for hydrogen radical exposed sample was 0.51 C/cm^2, which was higher than that annealed at 800°C in hydrogen atmosphere (0.39 C/cm^2). Consequently, hydrogen radical exposure at 500ºC has remarkably improved the reliability of thermal oxides on 4H-SiC wafer, and is the same effect with high-temperature hydrogen POA at 800°C.

Ellipsometric and XPS Studies of the 4H-SiC / SiO2 Interfaces, and Sacrificial Oxide Stripped 4H-SiC Surfaces: *Owen James Guy*[1]; [1]University of Wales Swansea

The investigation of the silicon carbide surface after a sacrificial silicon oxidation technique is reported. Oxidation of SiC is a necessary step in the fabrication of MOS devices and device termination features such as field plates. Device processing requires the etching of windows through the oxide layer to form features such as metal / SiC contacts. However, this work indicates that a thin interfacial Si-O-C layer is still present after etching the oxide with Hydrofluric acid (HF). Ellipsometry and X-ray photoelectron spectroscopy (XPS) have been used to evaluate this interfacial layer formed after oxide growth and after removal of oxide layers. An XPS analysis of the surface after removal of the oxide revealed that silicon, oxygen and carbon were all present in the remaining layer, which could not be removed by annealing at temperatures up to 1000°C. The Si-O-C layer could be eliminated by altering the oxidation conditions or by using a sacrificial silicon layer oxidation process. Ni Schottky barrier diodes fabricated on the 4H-SiC surface after removal of the oxide displayed slightly higher barrier heights and higher ideality factors to diodes on untreated 4H-SiC samples.

Structural and Morphological Properties of Atomic Layer Deposited HfO_2 on 4H-SiC: *Carey M. Tanner*[1]; Jongwoo P. Choi[1]; Jane P. Chang[1]; [1]University of California, Los Angeles

The material properties of ultra-thin HfO_2 films on 4H-SiC were investigated for their application as gate dielectric materials in SiC power metal-oxide-semiconductor field effect transistors (MOSFETs). The 4H-SiC (0001) surface was prepared by chemical mechanical polishing, yielding a smooth ordered surface characterized by atomic steps. HfO_2 films were grown by atomic layer deposition (ALD) at low substrate temperatures using hafnium *t*-butoxide and oxygen. A phase transition from amorphous to polycrystalline was identified at 280°C by *in-situ* reflection high energy electron diffraction (RHEED) and *ex-situ* x-ray diffraction (XRD) characterization. Below 280°C, amorphous layer-by-layer growth was observed at a rate of 1 Å/cycle as determined by x-ray photoelectron spectroscopy (XPS) and spectroscopic ellipsometry. A smooth film morphology with a root mean square roughness of 2 Å was determined by atomic force microscopy (AFM). No interfacial silicon oxide layer was observed by *in-situ* XPS characterization. Above 280°C, three-dimensional island growth was observed and the film exhibits a polycrystalline structure with monoclinic and tetragonal domains. Angle-resolved and synchrotron XPS, as well as high-resolution transmission electron microscopy, were used to further investigate the HfO_2/SiC interface.

Interfacial Properties of SiO_2 Grown on 4H-SiC: Comparison Between N_2O and Wet O_2 Oxidation Ambient: *Antonella Poggi*[1]; Francesco Moscatelli[2]; Andrea Scorzoni[2]; Giovanni Marino[1]; Roberta Nipoti[1]; Michele Sanmartin[1]; [1]CNR-IMM Sez.BO; [2]DIEI and INFN Università Perugia

The high trap density at silicon carbide (SiC)/oxide interface represents a serious problem for the production of commercial SiC MOSFETs. Many investigations have been conducted on the growth conditions of SiO_2 on SiC to improve the oxide quality and the properties of the silicon carbide-silicon dioxide interface. In this work a comparison between a wet oxidation and an oxidation in N_2O ambient diluted in N_2 is proposed. MOS capacitors were fabricated on a homo-epilayer grown on n-type 4H-SiC wafers (CREE Research Inc). The oxide quality and the SiO_2/SiC interface properties were characterized by capacitance-voltage (C-V) measurements of the MOS capacitors. The interface state density D_{it} near the conduction-band edge of SiC were evaluated from the high frequency and quasi-static C-V measurements obtaining results similar or better than the literature data. Furthermore, we employed the Slow Trap Profiling (STP) technique to study slow trapping phenomena. Preliminary results suggest a correlation between the detected slow traps and the presence of the C-V hysteresis. An accurate analysis of the slow trap measurements is in progress in order to evaluate the traps energy position and to study their influence on the conductance of the MOSFET channel.

TPD1.Reliability & Simulation

The Role of Residual Source/Drain Implant Damage Traps on SiC MESFET Drain I-V Characteristics: *John Adjaye*[1]; Michael S. Mazzola[1]; Andrei V. Los[2]; [1]Mississippi State University; [2]Freescale Semiconductor, Inc.

Experimental characterization of 4H-SiC power MESFETs with n+ implanted source/drain ohmic contact regions, with and without p-buffer layer fabricated on semi-insulating (SI) substrates exhibited hysteresis (looping) in the drain I-V characteristics of both types of devices at 300K and 480K due to traps. However, thermal deep level transient spectroscopy (DLTS), thermal admittance spectroscopy (TAS), and thermal conductance spectroscopy measurements could detect the traps only in the device without the buffer. Device simulation, using the two-dimensional device simulator Medici, also showed hysteresis in both types of devices at 300K and 480K, which is consistent with the experimental results. Simulations further suggest that, in addition to the SI substrate traps which are known to be a major cause of hysteresis in MESFET drain I-V characteristics and surface traps, acceptor traps due to residual implant damage can also be a major contributor to the hysteresis observed in MESFET drain I-V characteristics. Further simulations suggest that much of the hysteresis at low gate voltages and all the hysteresis at high temperatures such as 480K are due to acceptor-type source/drain residual implant damage traps with energy levels distributed in the 4H-SiC band gap.

Optimum Design of Short-Channel 4H-SiC Power DMOSFETs: *Asmita Saha*[1]; James A. Cooper[1]; [1]Purdue University

This paper reports a detailed Taguchi simulation study to determine the optimum design parameters for 4H-SiC power DMOSFETs within a multidimensional parameter space. The aim is to achieve the minimum specific on-resistance RON for a given blocking voltage, with the gate oxide field maintained below 4 MV/cm. At low blocking voltages, the on-resistance of 4H-SiC DMOSFETs is dominated by the MOS channel resistance. To minimize this resistance, a short channel (0.5 µm) design is assumed. Such a device can be fabricated using the self-aligned process recently introduced by the authors. To reduce the JFET resistance and the resistance due to two-dimensional current spreading into the drift layer, the JFET region doping is independently varied, and a novel current spreading layer (CSL) is incorporated into the design. Increasing the JFET region doping reduces the on-resistance, but increases the oxide field. However, narrowing the JFET region reduces the oxide field more than it increases the resistance, leading to an optimal figure-of-merit VB2/RON. We will report the optimum doping and dimensions of each layer (drift region, CSL, and JFET region) to achieve the maximum VB2/RON. Finally, we will extended our study to consider devices with very small feature sizes.

Design Considerations of a New 4H-SiC Enhancement-Mode Lateral Channel Vertical JFET for Low-Loss Switching Operation: *Young Chul Choi*[1]; Ho-Young Cha[1]; Lester F. Eastman[1]; Michael G. Spencer[1]; [1]Cornell University

A new silicon carbide (SiC) enhancement-mode lateral channel vertical junction field-effect transistor (LC-VJFET), namely "source-inserted

double-gate structure (SID-gate) with a supplementary highly doped region (SHDR)", was proposed for achieving extremely low power losses in high power switching applications. The proposed architecture was based on the combination of an additional source electrode inserted between two adjacent surface gate electrodes and a unique SHDR in the vertical channel region. Two-dimensional numerical simulations for the static and resistive switching characteristics were performed to analyze and optimize the SiC LC-VJFET structures for this purpose. Based on the simulation results, the excellent performance of the proposed structure was compared with optimized conventional structures with regard to total power losses. Finally, the proposed structure showed about a 20 % reduction in on-state loss (Pon) compared to the conventional structures, due to the effective suppression of the JFET effect. Furthermore, the switching loss (Psw) of the proposed structure was found to be much lower than the results of the conventional structures, about a 75 % ~ 95 % reduction, by significantly reducing both input capacitance (Ciss) and reverse transfer capacitance (Crss) of the device.

Numerical Investigation of SiC Devices Performance Considering the Incomplete Dopant Ionization: *Andres Udal*[1]; Enn Velmre[1]; [1]Tallinn University of Technology

One drawback of the wide band gap semiconductors what may hinder to achieve their predicted potential, is the deepness of dopant energy levels. In the case of high dopant activation energies Ed,a>>kT cannot be used any more the assumption of full ionization of dopant atoms. High Ed,a values decrease remarkably ionized (i.e. active) doping densities and free carrier densities and also add very abrupt temperature-dependences to those quantities. This, in turn, not only changes remarkably the device characteristics and makes more difficult the simulation tasks but also creates possibilities for thermal instabilities and runaway mechanisms. We have studied those problems applying nonisothermal 1D- and 2D-simulators DYNAMIT-1DT, 2DT in the case of different SiC device structures in wide temperature range 300...2000 K. In general lines the results confirm that the strongly temperature-dependent incomplete doping ionization has noticeable influence on SiC devices performance if impurity activation energies exceed 0.1, 0.2 and 0.3 eV for semiconductor layers with doping concentration of 1E17, 1E18 and 1E19 cm-3, respectively. Results show that in the case of SiC devices the effect of incomplete dopant ionization is one of the most dominating physical mechanisms influencing on the forward I/V curves and their temperature-dependences.

Device Options and Design Considerations for High-Voltage (10 - 20 kV) SiC Power Switching Devices: *Yang Sui*[1]; Xiaokun Wang[1]; Ginger Walden[1]; James A. Cooper[1]; [1]Purdue University

The specific on-resistance of optimally-designed unipolar power devices increases slightly faster than the square of the blocking voltage. For blocking voltages above 10 kV, the rapidly increasing RON and the fixed power dissipation limit of existing packages forces a dramatic reduction in on-state current density. The insulated-gate bipolar transistor (IGBT) presents an attractive alternative at higher blocking voltages. The power dissipation of the IGBT increases less rapidly with blocking voltage, due to conductivity modulation of the drift region, but the advantage is partially offset by the forward-biased diode drop in the main current path. As the blocking voltage increases, the effect of the diode becomes relatively less important, and the advantage of the IGBT increases. In this work we compare three devices: the n-channel MOSFET, n-channel IGBT, and p-channel IGBT at blocking voltages between 10 and 20 kV. Both n-channel and p-channel IGBTs are superior to the MOSFET in this voltage regime, and the advantage becomes more pronounced at elevated temperatures. For the IGBT, we will discuss the optimum drift region doping and the importance of achieving a high ambipolar lifetime in the drift region.

Optimization of 4H-SiC MOSFET Structures for Logic Applications: Peter Tappin[1]; *Alton Horsfall*[1]; [1]University of Newcastle Upon Tyne

Although silicon carbide has become the material of choice for high power applications in a range of extreme environments, the interest in the desire to create active sensor structures requires the development of transistors for operation in amplification circuits. Despite the recent advances in the quality of oxide layers on SiC, the mobility of inversion layers is still low and this will affect the maximum frequency of operation for these devices. We present simulation results which indicate that a delta channel structure is suitable for use with these low level signals. By varying the doping level of the device we have shown that the optimum delta doping for this application is 1.43x1019cm^{-3}, and the investigation of the high temperature behaviour and the frequency dependence will be covered in the final paper.

Dynamic Characteristics of 4H-SiC Pin Diode on (000-1)C-face with Small Forward Degradation: *Koji Nakayama*[1]; Yoshitaka Sugawara[1]; Ryosuke Ishii[1]; Hidekazu Tsuchida[2]; Toshiyuki Miyanagi[2]; Isaho Kamata[2]; Tomonori Nakamura[2]; [1]Kansai Electric Power Co., Inc.; [2]Central Research Institute of Electric Power Industry

The reverse recovery characteristics of pin diode fabricated on the C-face are reported for the first time. The dependence of the reverse recovery characteristics on the V_f degradation for the pin diodes is also introduced. The ΔV_f is 2.72 V for the pin diode on the Si-face. This value is 8 times higher than that on the C-face (0.35 V). The reverse recovery time, the peak reverse recovery current and the recovered charge of the pin diode on C-face are 46.2 ns, 2.52 A and 58.3 nC, respectively. On the Si-face, these parameters are 51.7 ns, 3.55 A and 91.7 nC. The pin diode on the C-face has superior potential to that on the Si-face for all parameters of the reverse recovery characteristics. On the C-face, there is little difference in the reverse recovery characteristics between before and after the current stress test. However, the pin diode on the Si-face after the current stress test exhibits a tendency of a fast turn-off as compared with that before the stress test.

Using a First Principles Coulomb Scattering Mobility Model for 4H-SiC MOSFET Device Simulation: *Siddharth Potbhare*[1]; Gary Pennington[1]; Neil Goldsman[1]; Aivars Lelis[2]; Dan Habersat[2]; F. B. McLean[3]; James McGarrity[3]; [1]University of Maryland; [2]Army Research Laboratory; [3]Berkeley Research Association

We have developed a physics based device simulator for detailed numerical analysis of 4H-SiC MOSFETs. At the core of the simulator is an advanced mobility model that accounts for the effects of surface phonon scattering, surface roughness scattering and Coulomb scattering of mobile carriers by occupied interface states and fixed oxide charges. We have developed a first principles quasi-2D Coulomb scattering mobility model for SiC MOSFETs that takes into account occupied interface traps, fixed oxide charges, distribution of mobile carriers inside the inversion layer, screening by mobile carriers, and temperature dependence. Using this mobility model we have shown that Coulomb scattering plays a dominant role very close to the interface. A few nanometers away from the interface, Coulomb scattering is greatly reduced, and other scattering mechanisms control the total low field mobility. We have extracted the interface trap charge density profile by comparing our simulated IV curves to experimental data for room temperature. Our simulations show that interface trap density of states is low in the midgap region and very high near the conduction band edge in 4H SiC, and it severely limits device performance.

Analytical Modelling of I-V Characteristics for 4H-SiC VJFET: *Praneet Bhatnagar*[1]; [1]University of Newcastle

Physics based Analytical Models are being seen as a constructive way for predicting characteristics of power devices. Circuit designers perceive analytic models as being more accurate since parameters are obtained from data sheets. This paper demonstrates an analytical model for 4H-SiC Enhancement Mode Vertical JFET (VJFET) based on the physics of this device. The results of this model have been compared with that of finite element model provided by SYNOPSYS MEDICI simulator. The paper discusses the results of analytical model's device characteristics between finger widths 1.6µm to 2.5µm at 300K. Both the on and off-state characteristics have a very close agreement with the finite element model.

An Effective Field Plate Termination for SiC Devices Based on High-k Dielectrics: *Mihai Brezeanu*[1]; Marian Badila[2]; Gheorghe Brezeanu[3]; Florin Udrea[1]; Cristian Boianceanu[3]; Gehan Amaratunga[1]; Konstantinos Zekentes[4]; [1]University of Cambridge; [2]Catalyst Semiconductor Inc.; [3]University Politehnica Bucharest; [4]FORTH

A classical implementation of the field plate technique is the oxide ramp termination, widely used for Si and SiC junction barrier diodes (JBDs) and Schottky barrier diodes (SBDs). This method requires the presence of an oxide ramp smaller than 10º, etched around the anode, which assures the smoothness of the electric field at the contact's periphery. This paper presents improvements of the efficiency of this termination for both SiC JBDs and SBDs, obtained by using for the first time high-k dielectrics. Extensive simulations results, for different dielectrics and different ramps, are presented. Two techniques of lowering the maximum electric field in the insulator in order to prevent the dielectric breakdown are also shown. By the increase of either the relative dielectric permittivity or of the insulator thickness, a significant decrease of the maximum electric field and termination efficiencies up to 96.8% are achieved. In the same time, the employment of high-k dielectrics allow the use of ramps with angles up to 10º and thicknesses as low as 1µm, which significantly reduces the cost and the complexity of the technological process.

High Temperature Reliability of SiC n-MOS Devices up to 630°C: *Ruby N. Ghosh*[1]; Reza Loloee[1]; Peter Tobias[1]; Tamara Isaacs-Smith[2]; John R. Williams[2]; [1]Michigan State University; [2]Auburn University

SiC based field-effect devices are attractive for electronic and sensing applications above 250°C. At these temperatures the reliability of the insulating dielectric in metal-oxide-semiconductor (MOS) structures becomes an important parameter in terms of long-term device performance. We report on the reliability of n-MOS SiC capacitors, following thermal stress cycling in the 330 to 630°C range. As the primary mode of oxide breakdown under these conditions is believed to be due to electron injection from the substrate, we have measured the gate leakage current as a function of temperature. The gate dielectric was grown using dry oxidation with an NO anneal. For large area, 1 mm diameter, 6H-SiC capacitors we obtain current densities as low as 10 nA/cm^2 at 630°C. Statistical data on flat band voltages and gate leakage

measurements from the array of 100 to 1000 µm devices on both 4H-SiC and 6H-SiC substrates will be presented. These results are very encouraging in terms of the long-term reliability of SiC field-effect sensors. Our measurement techniques are also relevant for reliability studies of SiC power devices, as they provide a platform for accelerated aging as well as time-dependent dielectric breakdown measurements at high temperature.

Simulations of 10 kV Trench Gate IGBTs on 4H-SiC: *Qingchun Zhang*[1]; Sei-Hyung Ryu[1]; Charlotte Jonas[1]; Anant Agarwal[1]; John Palmour[1]; [1]Cree, Inc.

Numerical simulations were conducted on 10 kV trench gate p-IGBTs on 4H-SiC. A punch through structure was utilized with a p-type buffer layer on the substrate. A p-type conduction layer was incorporated underneath the n-type base layer to mitigate the JFET effect from the trench bottom implants. Simulation results have shown that both the carrier lifetimes and the mesa width are two dominant factors in the device current handling capability. A sufficient drift layer conduction modulation can be achieved with a minority lifetime of >2 µs in the drift layer, and >100 ns in the buffer layer. A mesa width of 2 µm provides a high forward current due to the high channel periphery density. To maintain the device blocking capability, a mesa width narrower than 6 µm is required with 1×10^{16}cm^{-3} doping in the conduction layer. The termination junction needs to be formed on the lightly doped drift region around the device periphery, and sidewall implantation is required to achieve a low leakage current.

Time Domain and Frequency Analysis of Random Telegraph Signal and G-R Centres Contributions to I(V) Instabilities on 4H-SiC MESFETs: M. Trabelsi[1]; *Nabil Sghaier*[1]; Jean-Marie Bluet[2]; Gérard Guillot[2]; N. Yacoubi[1]; Christian Brylinski[3]; [1]IPEIN Nabeul; [2]INSA - LYON; [3]THALES

Our work focus on defects identification responsible of current fluctuations in 4H-SiC MESFETs. Toward this end random telegraphic signals (RTS) was measured and analyzed. We show that devices having instabilities in DC characteristics present random discrete fluctuations on the drain current. The RTS noise parameters analysis (amplitude, high and low state time durations) as a function of temperature and bias voltage allow us to characterize the traps involved. The technique consists in a statistical treatment of the RTS time domain data. Single trap capture cross-sections and activation energy are deduced from an Arrhenius plot. Three levels have been evidenced with activation energies and cross sections E_{c1}-0.32 eV / $\sigma\sim10^{-17}$ cm^2 ; E_{c2}-0.2 eV / $\sigma\sim2.10^{-17}$ cm^2 ; E_{c3}-0.17 eV / $\sigma\sim3.10^{-15}$ cm^2. To extend the RTS analysis, we present the power spectral density of the drain current noise (PSD). From PSD, we extract the cut-off frequency of a single trap even for low frequencies (f_{c1}= 29Hz, f_{c2}= 2Hz and f_{c3}=132Hz respectively for the three levels) and we precise that the noise responsible to RTS fluctuations is a generation-recombination noise. Finally, the nature of these traps (slow or fast traps) is precised using RTS measurements after an electrical stress.

Composite Ohmic Contacts to SiC for High Temperature Applications: *Adetayo Victor Adedeji*[1]; Claude Ahyi[1]; John Williams[1]; Suzanne Mohney[1]; Bangzhi Liu[1]; James Scofield[1]; [1]Auburn University

Composite ohmic contacts for SiC devices operating in air at 350C have been studied. Ohmic contacts to *n*- and *p*-SiC were protected against inter-diffusion and oxidation by Ta-Si-N layer[1] obtained by sputter deposition from a $TaSi_2$ target in a mixture of Ar and N_2. Platinum was sputter-deposited at 250C to promote adhesion between the Ta-Si-N barrier layer and a thick Au cap layer. Platinum also acts as a barrier to the diffusion of Au. The electrical and physical characteristics of the composite contacts are stable after hundreds of hours of cyclic thermal annealing in air at 350C. We report the results of (1) linear transmission line measurements on the composite ohmic contacts and the effect of thermal annealing in air on the specific contact resistance and the sheet resistance of the semiconductor (2) bond pull and shear tests following thermal cycling for stacks (Ta-Si-N / Pt / Au) deposited on both SiO_2 and the ohmic contact layers, and (3) RBS and AES measurements performed to monitor inter-diffusion and oxidation in the composite contacts as a function of annealing time. [1]E. Kolawa, J.S. Chen, J.S. Reid, P.J. Pokela, and M.-A. Nicolet, J. Appl. Phys. 70 (3) (1991) 1369.

Observation of Deep-Level Centers in 4H-Silicon Carbide Metal Oxide Semiconductor Field-Effect Transistors by Spin Dependent Recombination: *Morgen S. Dautrich*[1]; David J. Meyer[1]; Patrick M. Lenahan[1]; Aivars J. Lelis[2]; [1]Pennsylvania State University; [2]Army Research Laboratories

Previously we reported spin-dependent recombination (SDR) results indicating that silicon vacancy centers are important SiC/SiO2 interface trapping defects in 6H-SiC MOSFETs with thermally grown oxides while dangling bond centers are the primary interface/near-interface defect in 4H-SiC MOSFETs with deposited oxides. In this study we examine the more promising 4H-SiC MOS technology, specifically 100µm x 100µm n-channel lateral 4H-SiC MOSFETs on Cree Inc. substrates with thermally grown SiO2 gate dielectrics. We observe quite strong SDR spectra in the thermally grown SiO2 4H-SiC devices. We find that the SDR amplitude is strongly peaked at approximately zero gate potential. This result strongly suggests that we are observing dominating SiC/SiO2 interface traps in these more technologically relevant devices. In some respects, the 4H-SiC SDR spectra closely resemble traces we obtained earlier on thermally grown 6H-SiC devices. This limited result may indicate a similar origin for the defects in these two systems. However, a definitive identification of the 4H-SiC defects will require SDR measurements as a function of magnetic field vector orientation with respect to several SiC crystalline axes. At the present time, we are making these SDR vs. field measurements.

Optimization of the Specifc On-Resistance of 4H-SiC BJTs: *Santhosh Balachandran*[1]; T. Paul Chow[1]; Anant Agarwal[2]; [1]Rensselaer Polytechnic Institute; [2]Cree Inc.

In this paper we investigate the forward conduction characteristics of 4H-SiC epitaxial emitter NPN BJTs with special emphasis on the specific on-resistance ($R_{on\text{-}sp}$) of the device. The effect of factors such as the carrier lifetime in the drift region, surface recombination velocity along the interface and emitter contact resistance on $R_{on\text{-}sp}$ are examined. The reasons for the higher than unipolar value for the specific on-resistance are discussed and methods to improve the on-resistance value are suggested.

TPM1.Point Defects

Invited

Deep Level Point Defects in Semi-Insulating SiC: *Mary Ellen Zvanut*[1]; [1]University of Alabama at Birmingham

The high resistivity of SiC required for many device applications is achieved by compensating residual donors or acceptors with vanadium or intrinsic defects. The presentation will address the structure and defect level of substitutional vanadium and the positively charged carbon vacancy (V_C^+) in semi-insulating (SI) SiC. In addition, the contribution of each to the high resistivity of SI substrates will be discussed. After reviewing the model for (V_C^+) on both symmetry sites, the presentation will focus on photo-induced electron paramagnetic resonance (EPR) experiments used to determine the defect levels for (V_C) and vanadium. In particular, lattice relaxation is invoked to interpret the (V_C^+) photo-EPR data as well as to explain differences between the thermally and optically measured vanadium levels. The last part of the presentation will highlight EPR and Hall measurements that illustrate, on the one hand, the importance of the two vanadium charge states in creating SI SiC, and on the other hand, the limited role of (V_C^+) in compensation. The work of Haiyan Wang and Wonwoo Lee is gratefully acknowledged. Hall measurements and samples were provided by Dr. W. Mitchel and Mr. W. Mitchell, Wright Patterson AFB. The work is supported by Dr. Colin Wood, ONR.

Evidence of the Ground Triplet State of Silicon-Carbon Divacancies (P6, P7 Centers) in SiC: EPR Study: *Ivan Ilyin*[1]; [1]A.F.Ioffe Physico-Technical Institute

The electron paramagnetic resonance (EPR) spectra of the so-called P6, P7 centers were detected in semi-insulating (SI) SiC crystals and were suggested to be responsible for SI properties. These centers have been attributed to the triplet excited state of the Si-C divacancy. Recently they were reassigned to the excited state to the C(Si)-V(C) pair. The spectra have been observed only under light illumination are suggested to belong to an excited triplet state. The effect of optical pumping of ground triplet state and as a result the strong increasing of the EPR spectra intensities had not been taken into account. The aim of this study is to decide whether the observed triplet spectra belong to the ground or to excited state of P6, P7 centers. EPR experiments were performed at very low temperatures and in complete darkness to exclude the possibility of a thermal or optically excited triplet state. Our measurements prove that the ground state of P6, P7 centers corresponds to S=1 and that the zero-field splitting parameter D is positive. A possible energy level scheme and optical pumping process which induces the spin polarization of the ground triplet state of the P6, P7 centers in SiC is presented.

Investigation of the Displacement Threshold of Si in 4H SiC: *Wayne Sullivan*[1]; John Steeds[1]; [1]University of Bristol

The threshold energy needed for the creation of the neutral silicon vacancy in silicon carbide (SiC) has been previously investigated by photoluminescence (PL) techniques. It exhibits a deep PL band which has a no-phonon line existing around 1.44eV in 4H SiC. There has been some disagreement over the irradiation conditions at which the vacancy centres are created and detected by PL. We have attempted to clarify this by electron irradiating 4H SiC samples (from several sources, both n- and p-doped) before performing subsequent analysis by low temperature PL using a 488nm laser. The irradiations were performed in an ion-free transmission electron microscope (TEM) with an electron beam which was approximately circular, diameter 100µm. Four irradiations were performed per sample at 300keV. The electron doses were 10^{19}, 10^{18}, 10^{17} and 10^{16} electrons/cm^2. One sample was also irradiated with electrons from 250keV down to 190keV in steps of 10keV, with all these irradiations having a high electron dosage of 10^{20} e/cm^2. Our results show conclusively that we see the VSi signal at 300keV, even at the lowest dose

given (i.e. 10^{16} electrons/cm^2 although this is sometimes very weak) and for energies below 250keV, we do not detect this signal.

Signature of the Negative Carbon Vacancy-Antisite Complex: Michel Georg Bockstedte[1]; *Adam Gali*[2]; Takahide Umeda[3]; Ngyen Tien Son[4]; J. Isoya[3]; Erik Janzén[4]; [1]Universitaet Erlangen-Nuremberg; [2]Budapest University of Technology and Economics; [3]University of Tsukuba; [4]Linköping University

Direct experimental evidence of the metastability of the silicon vacancy and the more stable V_C-C_{Si} complex is scarce. Although the VC-CSi complex was identified with the P6/P7 center [Th. Lingner et al., Phys. Rev. B 64 (2001), p. 245212], this identification has to be revised [N. T. Son et al., this conference]. In new experiments [T. Umeda et al., this conference] on irradiated n-type 4H-SiC the HEI4-center was found possessing hyperfine (HF) tensors in nice agreement with calculated once of the negative V_C-C_{Si} complex residing on two hexagonal lattice sites. In this paper we report the theoretical identification of the HEI4-center. The small Jahn-Teller-effect of $(V_C\text{-}C_{Si})^-$ explains the temperature dependence of the experimental HF-signal. Measured below 50K or above 60K it originates from the ground state and the motional average of the metastable state, rsp. The analysis of the HF-tensors beyond the nearest neighbor shell allowed for an identification of the complex and its lattice sites. The signal of the HEI4-center is enhanced after excitation. We explain the thresholds observed in the photo-EPR spectra by an direct and indirect ionization of $(V_C\text{-}C_{Si})^{2-}$.

Clustering of Vacancies in Semi-Insulating SiC Observed with Positron Spectroscopy: *Reino Aavikko*[1]; Björn Magnusson[2]; N. T. Son[3]; Erik Janzén[3]; Kimmo Saarinen[1]; [1]HUT; [2]Norstel AB; [3]Linköping University

Semi-insulating (SI) silicon carbide can be produced by co-doping the material with both vanadium to create a mid-gap level and with aluminium to compensate the residual donors. These doped materials have however suffered from e.g. precipitation of the metal dopants degrading the quality of the components grown on these substrates. Another possibility to produce the SI material is to push the concentrations of the residual impurities low enough to allow the pinning of the Fermi-level to the intrinsic defects. A method for producing this kind of material is High-Temperature Chemical Vapor deposition (HTCVD). Positron Annihilation Spectroscopy is a non-destructive method for studying the open-volume defects in the material. We have performed positron annihilation measurements in HTCVD grown SI silicon carbide. Our results show that the material contains vacancy clusters of approximately 5-20 atoms. We also see that the clusters grow in high-temperature (1600°C) annealing. We have applied the positron measurements as a function of temperature and illumination in order to investigate the charge state of the defects.

Deep Traps and Charge Carrier Lifetimes in 4H-SiC Epilayers: *Sung Wook Huh*[1]; J. J. Sumakeris[2]; A. Y. Polyakov[1]; M. Skowronski[1]; P. B. Klein[3]; B. V. Shanabrook[3]; M. J. O'Loughlin[2]; A. V. Govorkov[4]; [1]Carnegie Mellon University; [2]Cree Inc.; [3]Naval Research Laboratory; [4]Institute of Rare Metals

Electron and hole traps and charge carrier lifetimes were investigated in a set of thick (5<d<100 μm) undoped 4H-SiC layers grown by CVD homoepitaxy. Deep trap spectra were measured by DLTS with electrical or optical injection while lifetimes were measured by time resolved PL at room temperature and by electron beam induced current technique (EBIC). The main electron traps detected in all samples were the 0.15-0.17 eV traps due to Ti, 0.65 eV Z1/Z2 centers, and 1.5-1.6 eV EH6/EH7 centers. Two hole traps observed by ODLTS had the activation energy of 0.3 eV (boron acceptors) and 0.6 eV (boron-related D centers). The concentration of electron traps decreased with the thickness of the layers and increased toward the edge of the wafers. The PL lifetimes were in the 200 ns-3400 ns range and correlated with changes in the density of Z1/Z2 and EH6/EH7 electron traps. The lifetimes derived from EBIC were slightly lower than the PL values. DLTS measurements on p-i-n diode structures confirm active participation of Z1/Z2 and EH6/EH7 in the recombination process. Contributions of the surface recombination processes and recombination at extended defects will be discussed.

Low Trap Density Induced in 4H-SiC by High Energy Proton Irradiation: *Alfonso Ruggiero*[1]; [1]Catania University

The effect of high energy irradiation on the electrical characteristics of 4H-SiC Schottky diodes have been investigated by current-voltage measurements and Deep Level Transient Spectroscopy (DLTS). The devices were fabricated by nickel evaporation on a low resistively (concentration ≈ 8×1015 carriers/cm^3) epitaxial layer. The defects are generated uniformly across the epitaxial layer by irradiation of 60 MeV H ions. The ion fluence was in the range 7x10^{10} ions/cm2–1.4x10^{12} ions/cm^2, corresponding to a vacancy concentration in the range 1.8x10^{12} cm^{-3} – 3.6x10^{13} cm^{-3}. Small changes in the electrical characteristics after the highest fluence irradiation were observed, however DLTS investigations show an increase in the intensity of original trap (the well know Z1/Z2 level), whose energy is Ec-0.68 eV and simultaneously the formation of deeper trap at Ec-1.5 eV (RD4) . The concentration of these levels increases linearly with ion fluence and from experimental data we determine a production trap rate of 0.15 trap/vacancy and of 0.11 trap/vacancy for RD4 and Z1/Z2 levels, respectively. These values are lower with respect to the values reported for Si and GaAs material. These devices appear promising for aerospace and terrestrial applications where the radiation hardness is a fundamental requisite.

Deep Traps in High-Purity Semi-Insulating 6H-SiC Substrates: Thermally Stimulated Current Spectroscopy: *Zhaoqiang Fang*[1]; B. Claflin[1]; D. C. Look[1]; L. Polenta[2]; J. Chen[3]; T. Anderson[3]; William C. Mitchel[1]; [1]U.S. Air Force; [2]University of Bologna; [3]II-VI, Inc.

Thermally stimulated current spectroscopy (TSC) has been applied to characterize deep traps in high-purity semi-insulating (HPSI) 6H-SiC substrates, which were grown by the advanced physical vapor transport technique at II-VI, Inc.. The samples had conductivity activation energies of 1.1 – 1.4 eV. By using 360-nm (above bandgap) to 475-nm (sub-bandgap) light for illumination at 83 K and under different biases, at least nine TSC traps in the temperature range of 80 to 400 K can be consistently observed. These traps peak at 95 K, 105 K, 115 K, 155 K, 175 K, 205 K, 265 K, 305 K, and 355 K, respectively. It was found that the low-temperature (T < 130 K) TSC peaks are significantly affected by the applied light and the peak at 175 K is strongly enhanced by the applied bias. The trap activation energies, calculated by using the approximate equation ET=kTm ln (Tm4/β), range from 0.16 eV to 0.74 eV. However, theoretical data fitting of some of the traps gives more accurate trap parameters. Based on temperature-dependent photocurrent spectra and literature results connected with deep traps in conductive 6H-SiC, the impurity and point-defect nature of these TSC traps will be discussed.

TPM2.Electrical & Optical Properties II

Infrared Reflectance Study of 3C-SiC Grown on Si by Chemical Vapor Deposition: Zhe Chuan Feng[1]; W. Y. Chang[2]; Jiangyi Lin[2]; *C. C. Tin*[3]; Weijie Lu[4]; W. E. Collins[4]; [1]National Taiwan University; [2]National University of Singapore; [3]Auburn University; [4]Fisk University

Infrared (IR) reflectance spectra are studied both theoretically and experimentally on 3C–SiC films grown on Si substrate by low pressure chemical vapor deposition (LP-CVD). By the use of transfer matrix method, the spectral features influenced by film thickness, phonon-damping constant and free carrier concentration are systematically studied. Through simulation, film thickness, free carrier concentration and phonon damping constant are determined. However, two typical cases are often observed from some experimental IR reflectance of CVD-grown 3C-SiC on Si, i.e. a damping of the intensity of interference fringes in the region far beyond the lattice phone frequencies and a dip or notch within the "flat top" of the IR reflectance between the transverse optical (TO) and longitudinal optical (LO) phonon frequencies. Both phenomena can not be described by a simple classical lattice dielectric model. Modified effective medium models with consideration of the presence of an "optical transition layer" between film and substrate and of interfacial layer and intergranular pores are, correspondingly, introduced to interpret these interesting features observed experimentally. The simulation results can be well fitted to the experimental IR data, which also lead to penetrating information or quantitative evaluation about the microstructure and crystalline properties of 3C-SiC film on Si.

Non-Equilibrium Carrier Diffusion and Recombination in Semi-Insulating PVT Grown Bulk 6H-SiC Crystals: Ramunas Aleksiejunas[1]; Arunas Kadys[1]; Karolis Neimontas[1]; *Kestutis Jarasiunas*[1]; Gilyong Chung[2]; Edward Sanchez[2]; Mark Loboda[2]; [1]Institute of Materials Science and Applied Research; [2]Dow Corning Corporation

We applied a time-resolved non-degenerate four wave mixing (FWM) technique for investigations of high-density carrier dynamics in two semi-insulating PVT-grown 6H wafers, prepared from one boule. We used 25 ps duration pulses from YAG:Nd^{3+} laser at 355 nm to record a spatially modulated carrier distribution, which then was monitored by diffraction of delayed 1064 nm wavelength probe. We measured the bipolar diffusion coefficient D_a and the carrier lifetime τ_R in the samples at various pump energies. We observed the tendency of both D_a and τ_R to decrease at higher pump energies. We found D_a = 4.4 ± 0.4 cm^2/s at 0.6 mJ/cm^2 and D_a = 2.5 ± 0.3 cm^2/s at 4.8 mJ/cm^2, correspondingly. From low-pump D_a value we estimated the hole mobility μ_h = (88 ± 6) cm^2/Vs. The measured carrier lifetime τ_R in the samples varied from τ_R = 0.9 - 1.1 ns at 0.6 mJ/cm^2 to τ_R = 0.35 - 0.43 ns at 4.8 mJ/cm^2. The higher carrier mobility and the longer lifetime compared to those reported in vanadium doped semi-insulating 6H SiC crystal show the high quality of PVT-grown wafers.

Determination of the Temperature and Field Dependence of the Inversion Conductivity Mobility in 4H-SiC/Si02: *Gary Pennington*[1]; Siddharth Potbhare[1]; Neil Goldsman[1]; Dan Habersat[2]; Aivars Lelis[2]; [1]University of Maryland; [2]Army Research Laboratory

Field-effect mobility (μFE) measurements in 4H-SiC MOSFETs are typically found to be very small (<40 cm^2/Vs). This is believed to be a direct result the large density of traps measured at the 4H-SiC/Si02 interface. Traps may reduce μFE through two mechanisms: charge trapping and coulomb scattering. The importance of each mechanism can be deduced by considering

the conductivity mobility of free inversion channel carriers (μinv), which is independent of charge trapping. Furthermore, μinv gives insight into the importance of phonon and roughness scattering. In this work, a compact device model for determining μinv from experiments is presented. In comparison to Hall measurements, the procedure is advantageous since μinv can be calculated without requiring knowledge of the Hall factor. Results show that μinv is large at room temperature (~200 cm^2/Vs), indicating that μFE is greatly affected by charge trapping. Near threshold, coulomb scattering from fixed and trapped interface charges dominates. The field and temperature-dependent mobility in strong inversion however agrees very well with the results of a surface phonon mobility model. Surface roughness scattering is not found to be important.

TPM3.Extended Defects II

The Synchrotron X-Ray Topographic Analysis of Dislocation Structure in Bulk SiC Single Crystal: *Satoshi Yamaguchi*[1]; Daisuke Nakamura[1]; Itaru Gunjishima[1]; Yoshiharu Hirose[1]; [1]Toyota Central R&D Laboratories., Inc.

Although a rough sketch of dislocation structure in bulk SiC crystals had been reported, a detailed feature was not revealed in bulk sensitive X-ray topograph because of a high density of dislocations. In the meanwhile, we have developed RAF (Repeated A-Face) method to reduce the number of crystal defects in the bulk SiC single crystals. The RAF substrate makes us analyze detailed properties of the dislocations in the SiC crystal by means of bulk sensitive X-ray topography. From this analysis, we can reveal the detailed feature of one type of basal-plane dislocations and two types of threading dislocations. The basal-plane dislocations are screw one, whose Burger's vectors are parallel to the dislocation lines. And one of the threading dislocations is mixed one close to screw dislocation parallel to the growth direction with Burger's vector of 1c+na. Another is the edge dislocation parallel to c-axis, which lie between two basal-plane dislocations. Moreover, these dislocations do not exist independently but do connect with each other, which is the structure of dislocation network.

Stacking Fault and 3C Quantum Well in Hexagonal SiC Polytypes: *Maosheng Miao*[1]; Walter R.L. Lambrecht[1]; [1]Case Western Reserve University

The electronic-stress mechanism for stacking fault growth in 4H SiC is reviewed. The basic effect is that electrons trapped in SF interface-states below the conduction band minimum lower the energy more than it costs to form a SF-unit. The case of n-type annealing must be distinguished from the dynamic situation in devices. In the former, equilibrium conditions dictate the amount of electrons trapped in the interface state. As shown by Kuhr et al. the electrostatic barrier from the charge trapping limits the charge trapped and a net electronic stress only results for double-SF but not for single-SF. However, in the dynamic case, the bias overcomes this electrostatic barrier. Based on results by Sitch et al. we show how the saddlepoint configuration involved in the kink migration may be responsible both for the reduction in activation energy in active devices and their observed luminescence. Previous results on 3C quantum wells in 2H are extended to 3C in 4H and show that effective gaps below the gap of 3C do not occur as a result of the screening of the fields produced by the difference in spontaneous polarization. The possibility of a QW induced increase in excitonic binding energy is pointed out.

First Principles Modelling of Scroll-to-Nanotube Defect: Screw-Type Dislocation: Irene Suarez Martinez[1]; *Gianluca Savini*[1]; Malcolm I. Heggie[1]; [1]University of Sussex

Carbon nanotubes (CNTs) have attracted the attention of carbon scientists for their potential applications especially in nanoelectronics. Their electrical properties are known to be a function of their quirality. Therefore, 1/3 of the CNs are metallic and 2/3 are semiconductors. The band gap for semiconductor CNs is inversely proportional to the diameter. Narrow nanotubes are expected to be wide-band gap semiconductors with forbidden gap up to 2.6 eV. Those narrow nanotubes are found experimentally as inner tubes of multi-wall nanotubes (MWNTs). Several experimental results have shown that the thickness of a MWNT along the axis, can change, while the interlayer spacing remains fairly constant. These observations suggest the coexistence of scroll and multi-wall nested tubes, and therefore the existence of an extended defect responsible for the conversion between these two structures by a 'zipper-like' bond rearrangement. We suggest that this extended defect is a screw dislocation. In this paper, we present a density functional theory study of the structure and electrical properties of screw dislocations, and we discuss their glide motion along MWNTs.

Peierls Barrier and Core Properties of Partial Dislocations in 4H-SiC: *Gianluca Savini*[1]; Malcolm I. Heggie[1]; Sven Öberg[2]; [1]University of Sussex; [2]Luleå University of Technology

Recent studies of p-i-n diodes have reported an increase in the voltage drop under forward bias over a period of few days. Several experimental techniques have revealed that this degradation is due to the expansion of stacking fault along basal plane bounded by Shockley partial dislocations. Under an applied forward bias a band-gap transition at approximately 1.8 eV is observed together with mobile partial dislocations bordering the growing stacking faults. There is also evidence that not all the partials move under forward biasing, but some types move rapidly with an activation energy 0.27 eV, while others are immobile. In this work, energies and structures of the Shockley partial dislocations in 4H-SiC are investigated theoretically. Both partials exhibit asymmetric reconstruction core with no midgap state. The unreconstructed dislocations cores are metastable and present deep levels inside the forbitten gap. We show that the type of reconstruction core is strongly depended on the charge state of these defects. For each charge state, we calculate the Peierls stress barrier. Our results are in agreement with the enhancement of the mobility of partial dislocations under forward bias, and also can explain the luminescence peak at 1.8 eV associated to these extended defects.

Structure of "Star-Pattern" Defect in 4H-SiC Substrates and Epilayers: *Jae Won Lee*[1]; Marek Skowronski[1]; [1]Carnegie Mellon University

Transmission X-ray topography (XRT) and molten potassium hydroxide (KOH) etching followed by optical microscopy have been used to study the structure of a "star" defect in 4H-SiC wafers and its effects on the extended defect structure in the epilayers. High densities of threading dislocations (both screw and edge types) at the center of star defect are bounded by the domain walls along <1-100> directions. Etch pit arrays of threading edge dislocations are aligned along <11-20> directions and are polygonized perpendicular to the direction of each array. The <11-20> arrays indicated that the motion of dislocation was controlled by Peierls mechanism with the morphology consistent with the slip bands generated by the prismatic slip: <11-20>{1-100}. In addition, straight bands of dislocations perpendicular to the off-cut direction were observed in the epilayers deposited on top to the star defect. These correspond to threading dislocation arrays nucleated in epilayers during epitaxial growth. The {11-20} and {1-100} reflections were used to obtain topographic images and determine the Burgers vector, b = a/3[11-20].

TPM4.Novel Characterization and Structures II

Physical and Optical Properties of In-Situ Nitrogenated Amorphous Silicon Carbide Films Prepared by a novel Polymer Source Chemical Vapor Deposition(PS-CVD) Technique: *Yousef Awad*[1]; My Ali El Khakani[2]; Cetin Aktik[3]; Nathalie Camiré[1]; Maxime Lessard[1]; Mihai Scarlete[1]; [1]SiXtron Advanced Materials Inc.; [2]INRS–Énergie, Matériaux et Télécommunications; [3]Université de Sherbrooke

We report on the deposition of nitrogenated amorphous silicon carbide films by means of a newly developed Polymer Source Chemical Vapor deposition (PS-CVD) process. While poly (dimethylsilane) was used as a single-source precursor for the growth of a-SiC films, their nitrogentation was accomplished through the introduction of NH3 in the gas phase during film growth. The chemical bonding, film atomic composition and surface morphology of the deposited films were systematically examined as a function of the [NH3]/[Ar] flow ratio, by means of x-ray photoelectron spectroscopy (XPS), Fourier transform infrared spectroscopy (FTIR) and atomic force microscopy, respectively. On the other hand, mechanical and optical properties of the nitrogenated a-SiC were also investigated by means of nanoindentation, and optical transmission measurements, respectively. The surface of the a-SiC:H films was found to be very smooth (with Ra values in the 0.9-1.8 nm), as deduced from AFM measurements. The photoluminescence (PL), at room temperature was also systematically characterized as a function of the nitrogen doping level. The PL spectra show efficient photoluminescence peaks in the visible part of the spectrum. Not only the intensity but also the position of the PL peaks is shown to vary with the N doping level of the films.

Sol-Gel Silicon Carbide for Photonic Applications: *Siegmund Greulich-Weber*[1]; Bettina Friedel[1]; [1]University of Paderborn

SiC is not only a powerful material for electronic and opto-electronic applications but also for photonics. Due to its excellent properties in particular its hardness, its chemical inertness and its wide bandgap it is a challenge to use SiC also for nano-photonic applications such as for example photonic bandgap materials. We have investigated the growth of SiC, following a modified sol-gel process, which can be used for the fabrication of 3D photonic bandgap materials. This process is, however, useful for several SiC applications. Depending on the sol-gel annealing procedure one obtains macro-porous SiC, amorphous SiC, or micrometer-sized 3C-SiC single crystals. While macro-porous SiC is of interest for e. g. medical applications, amorphous and in particular single crystalline sol-gel-grown SiC are of particular interest for photonic applications. Via the sol-gel annealing procedure we are able to prepare crystal sizes ranging from several nm up to several 100 μm. The resulting polytype depends on the annealing temperature. Doping is possible either during the sol-gel preparation or via the gas phase during the following annealing procedure. We will present details on the sol-gel SiC preparation as well as on doping and we will provide material properties as determined by

EPR and optical spectroscopy.

Mechanical Testing of Flexible Silicon Carbide Interconnect Ribbons: *Radhika Panday*[1]; Xiao-an Fu[1]; Srihari Rajgopal[1]; Torben Lisby[2]; Stefan Nikles[2]; Khalil Najafi[2]; Mehran Mehregany[1]; [1]Case Western Reserve University; [2]University of Michigan

This paper explores polycrystalline 3C-silicon carbide (poly-SiC) deposited by LPCVD for fabricating flexible ribbon cable interconnects for micromachined neural probes. While doped silicon is used currently, we hypothesized that poly-SiC will provide enhanced mechanical robustness due to SiC's superior mechanical properties. Paralleling prior work in silicon, 42 different designs were fabricated from nitrogen-doped poly-SiC films deposited by LPCVD at 900ºC using dichlorosilane and acetylene as precursors. The different designs were then tested in three modes: bending, twisting, and compression. (Ribbon cable interconnects are made up of one or more beams, each being a conductor in the cable.) Curved beams were found to bend nearly 250% more than straight beams before fracture. Longer beams withstood greater bending and twisting due to greater compliance. Longer and narrower beams generally outperformed shorter beams irrespective of design. Also, doped poly-SiC beams had, on average, breaking angles that were greater than those of identical doped silicon beams by ~50% in bending and ~20% in twisting modes. The paper will detail the 42 designs studied, describe the fabrication process for the test structures, and compare/contrast the testing and simulation results related to the different designs to identify best design practices.

TPM5.Related Materials II

Direct Electrical Characteristics of GaN Nanowires Field-Effect Transistor (FET) without Assistant of E-Beam Lithography(EBL): *Sang-Kwon Lee*[1]; Nam-Kyu Cho[1]; Han-Kyu Sung[2]; Heon-Jin Choi[2]; Ki-Suk Nam[1]; [1]Chonbuk National University; [2]Yonsei University

We have investigated a simple technique for extracting the electrical properties of 1D semiconductor nanowires using a standard ultraviolet UV photo-lithography instead of e-beam lithography. For the experiment, the gallium nitride nanowires(GaNNWs) were prepared by a horizontal hot-wall chemical vapor deposition. The substrates, deposited on a 2nm layer of Ni by sputtering, were placed in the region of uniform temperature in the quartz tube reactor. Ga and nitrogen component were supplied to the substrate by using metallic Ga and NH_3 gas. The reactor was heated upto 900ºC under a flow of NH_3 (20 sccm) and maintained for 6 hours, and then cooled down to the room temperature. The GaNNWs have diameters in the range of <100nm and length of several μm. The GaNNWs were dispersed onto the surface of patterned silicon substrate which was prepared by ordinary UV photo-lithography processes for the electrical leads and where the underlying conducting Si wafer was used as the large-area gate in the FET structure.The estimated carrier mobility from the gate-modulation characteristics is on the order of 60-70 cm^2/Vs. The result also shows our GaNNWs have the n-type of dopants.

In-Situ Stress Monitoring by Single Beam Deflectometer: *Mikhail Belousov*[1]; [1]Veeco TurboDisk Operations

It is widely accepted that strain plays a critical role in the performance of compound semiconductor devices. In order to estimate stress level in epilayers during deposition, we have developed a single beam in-situ deflectometer (patent pending). It is based on a laser reflectometer incorporating a Position Sensitive Detector as a sensor that measure the intensity and location of the laser beam reflected from the deformed wafer. Unlike conventional multi-beam deflectometers, the single-beam deflectometer does not require large optical access and can be installed on a small viewport. Its high data acquisition rate allows measurement of deformation of individual wafers located on the carrier spinning up to 1500 RPM. The deflectometer provides the ability to measure wafer curvature changes due to such factors as layer to layer lattice and temperature expansion mismatch, temperature gradient along substrate thickness, layer doping concentration, and nucleation conditions. The deflectometer is sensitive enough to measure stress associated with growth of each layer of GaN LED structure including the extremely thin 25Å InGaN Single Quantum Well. We will discuss application of the in-situ wafer deflection measurements to stress engineering and production of GaN-based LED's.

TPM6.Surfaces and Interfaces II

Effects of Rapid Thermal Annealing Treatment on the Surface Band Bending of n-Type GaN Studied by Surface Potential Electric Force Microscopy: S. Chevtchenko[1]; Q. Fan[1]; F. Yun[1]; C. W. Litton[2]; A. Baski[1]; H. Morkoç[1]; [1]VCU; [2]Air Force Research Laboratory

It is generally accepted that Shottky barrier height is affected by the initial band bending on the bare nGaN surface and by the band bending following metal deposition. The effect of surface treatments during device fabrication on the surface band bending of bare nGaN was studied by surface potential electric force microscopy (SP-EFM). An increase of the initial upward band bending from +1.0±0.1eV for the as-grown GaN to +1.9±0.1eV after RTA treatment in N_2 ambient was observed. There is no significant change in band bending using N_2 or Ar as ambient gas during the RTA treatment. The increase of initial upward band bending was also confirmed by photoluminescence measurements. There is a quenching of PL intensity in the near-band-edge and blue band regions for the GaN sample subjected to RTA treatment at 800°C for 1min in N_2 ambient. We suggest this is due to the enhanced capture of photogenerated carriers by near surface non-radiative centers and or separation of carriers due to the increased near surface electric field. The higher the initial band bending the more photogenerated carriers needed to maintain the equilibrium under illumination. SP-EFM is found to be a useful tool in studying the band bending in GaN.

On Separating Oxide Charges and Interface Charges in 4H:SiC Metal-Oxide-Semiconductor Devices: *Daniel B. Habersat*[1]; Aivars J. Lelis[1]; Gabriel Lopez[1]; James McGarrity[2]; Barry McLean[2]; [1]Army Research Laboratory; [2]Berkeley Associates

We have investigated the distribution of oxide traps and interface traps in Silicon Carbide MOSFETs and capacitors. The density of interface traps, D_{it}, was characterized by two charge pumping methods: base-level charge pumping which gives an average across the midgap region and spectroscopic charge pumping which measures profiles near both band edges. The number of oxide traps, N_{OT} was then calculated by measuring the flatband voltage V_{FB} in p-type capacitors and the threshold voltage V_T in n-channel MOSFETs. The amount of shift in measured voltage from an ideal calculation for the device, minus the contributions due to filled interface traps, gives an estimate for the number of oxide traps present. We also examined the difference in flatband and threshold voltage shifts and then calculated an average interface trap density across the midgap region. There was good correlation between our various measurements. We found D_{it} to be in the low 10^{11} $cm^{-2}eV^{-1}$ range in midgap and approaching 10^{12}-10^{13} $cm^{-2}eV^{-1}$ near the band edges. This data, combined with measurements of V_{FB} and V_T, gives us values of 0.5-2.0 * 10^{12} cm^{-2} for N_{OT}.

Fast Non-Contact Dielectric Characterization for SiC MOS Processing: *Andrew M. Hoff*[1]; Elena Oborina[1]; [1]University of South Florida

This work presents examples of the rapid process knowledge development that may be derived through application of a fast metrology. The approach provides quantitative information regarding dielectric film properties on silicon carbide substrates in only minutes following the film growth process. Known as corona-voltage metrology or C-VM, the method utilizes a determination of the contact potential difference between the material surface and a reference electrode in combination with an application of corona charge to supply a controlled bias to the structure. Contact potential difference maps of as-oxidized 4H n-type SiC wafers were obtained to demonstrate the effects of different growth ambients on dielectric film properties. Examples of such maps show that one process appears to produce a uniform film whereas the other does not. Non-contact capacitance-voltage characteristics were acquired to determine the capacitance equivalent thickness, CET, variation along the vertical axis of each wafer. The CET values corroborate the map information and show variation of less than 1% and up to 8% in the two cases respectively. The combination of both methods represents a fast and powerful tool that may be applied in the development of new MOS process schemes or in the control of established processes.

High Temperature Annealing of Al2O3 Deposited by ALCVD on n-Type 4H-SiC: *Marc Avice*[1]; Ulrike Grossner[1]; Ola Nilsen[1]; Jens Christensen[1]; Helmer Fjellvåg[1]; Bengt Svensson[1]; [1]University of Oslo

Al2O3 has been grown by Atomic Layer Chemical Vapour Deposition (ALCVD) on HF cleaned and RCA cleaned on n-type 4H-SiC and Si using either H2O or O3 as an oxidant. After post-deposition annealing at high temperature (1000°C) in Argon atmosphere for different time periods (1h, 2h, 3h), bulk and interface properties of the films were studied by Capacitance-Voltage, Current-Voltage, X-Ray Diffraction, Secondary Ion Mass Spectrometry (SIMS) measurements and High Resolution Transmission Electron Microscopy. Electrical measurements show a decreasing shift of the flatband voltage indicating a diminution of the negative oxide charges while increasing the annealing time. After annealing at 1000°C for 3h, the flatband voltage shift decreased to 6V. This behaviour may be correlated with crystallization of the Al2O3. SIMS measurements, on as-grown and annealed Al2O3/SiC and Al2O3/Si samples, revealed accumulation of boron, manganese and potassium at the Al2O3/SiC and Al2O3/Si interfaces.

Tunneling Spectroscopy and Transport Studies of Oxidized SiC Surfaces: *Shu Nie*[1]; Randall M. Feenstra[1]; [1]Carnegie Mellon University

We have used scanning tunneling microscopy and spectroscopy to study the spectroscopy and charge transport of electronic states formed at oxide/SiC interfaces. Both 6H c-plane and 4H a-plane orientations have been employed, and we have studied both the natural oxide (formed on as-received wafers, after thermal cleaning) and the oxide formed by annealing in an ultra-high-vacuum chamber at 800°C under 5×10^{-8} Torr pressure of molecular oxygen.

Auger electron spectroscopy performed as a function of oxygen exposure reveals a saturation surface coverage of about 1.2 and 1.6 monolayers for the c-plane and a-plane, respectively. Tunneling spectra reveal qualitatively similar results for all surfaces, revealing a band of donor states located at about -1.0 eV below the Fermi-level and two bands of acceptor states at +0.3 eV and +0.9 eV above the Fermi-level. Transport of charge through these interface states has been studied by observing the variation in tunneling barrier height as a function of tunnel current. A noticeable decrease in barrier height is found for a tunnel current of about 1 nA, corresponding to an estimated surface resistivity of 170 Gohm/square. The spatial variation of this value across the surface is currently being investigated.

4:10 PM Coffee Break

TC1.Extended Defects II

Tuesday, 4:30-6:15pm
September 20, 2005

Room: Allegheny Ballroom I
Location: Westin Pittsburgh

Session Chair: M. E. Twigg, Naval Research Laboratory

4:30 PM Invited
Nm-Resolution Measurement of Individual Planar Inclusions in 4H-SiC using BEEM: Quantum-Well Energy Depth and Local Transport Behavior.: K.-B. Park[1]; Y. Ding[1]; *Jonathan P. Pelz*[1]; J. Grim[2]; M. Skowronski[2]; M. K. Mikhov[3]; Y. Wang[3]; B. J. Skromme[3]; [1]Ohio State University; [2]Carnegie Mellon University; [3]Arizona State University

Thin planar inclusions with local cubic stacking can form in hexagonal SiC during growth, processing, or device operation, and behave as unique "structure only" electron quantum wells (QWs) which strongly impact material and device behavior. A key factor is the QW energy depth E_{QW}, which determines how electrons accumulate and release energy when they "fall" into inclusions. We have measured E_{QW} for several types of inclusions where they intersect a metal/4H-SiC Schottky interface, using nm-resolution Ballistic Electron Emission Microscopy (BEEM). We find $E_{QW} \sim 0.53$ eV for "double stacking fault (SF)" inclusions, ~0.25 eV for "single SF" inclusions, and ~0.39 eV for a third inclusion type formed during epitaxial growth. Using quite different methods, *macroscopic* Schottky diode capacitance-voltage (*C-V*) curves were used to estimate $E_{QW} \sim 0.51$ eV for double SF inclusions, in good agreement with BEEM. We have also observed that inclusions can strongly affect the local Schottky barrier height and electron transport behavior in the surrounding 4H-SiC material, possibly due to strong spontaneous polarization thought to exist in hexagonal SiC. Work Supported by ONR and NSF.

5:00 PM
Observation of Free Carrier Redistribution Resulting from Stacking Fault Formation in Annealed 4H-SiC: *Orest J. Glembocki*[1]; Marek Skowronski[2]; Sharka M. Prokes[1]; David K. Gaskill[1]; [1]Naval Research Laboratory; [2]Carnegie Mellon University

SiC is a unique electronic material because it can be grown in one of a large number of polytypes, which have similar formation energies. This results in a technological problem because under conditions of thermal annealing or electrical stress 4H-SiC has been observed to form stacking faults that locally have 3C stacking order. Because 3C-SiC has a lower band gap than 4H-SiC there is a significant transfer of free carriers into the stacking faults. In this work, we observed the free carrier redistributions in annealed 4H-SiC. The charge density in the 4H-SiC was measured with Raman scattering using the coupled plasmon-LO phonon modes (CP-LO). Bulk n^+-SiC with a carrier density of $n=1\text{-}2\times10^{19}cm^{-3}$ was annealed at 1150°C to produce extended stacking faults. The CP-LO mode was observed to shift in a manner consistent with 10^{18} cm^{-3} doping in the 4H-SiC. Numerical simulations were performed using a self-consistent Poisson-Schroedinger solver and agree well with the experimental observations of carrier transfer from the 4H-SiC into the 3C-SiC stacking faults. In addition, Raman scattering has shown that the 3H stacking faults induce a tensile strain on the surrounding 4H-SiC regions.

5:15 PM
Silicon Carbide: A Playground for 1D-Modulation Electronics?: *Peter Deák*[1]; [1]University of Paderborn

Electronic devices with 1D modulation of the potential through quantum well (QW) or doping superlattices has so far been the privilege of III-V semiconductors, because the large lattice mismatch prevents single crystal heteroepitaxy between silicon and diamond. We will show here, that SiC might provide a unique solution to solve this problem. Since SiC can be grown epitaxially, monolayer by monolayer, with ALE or MBE, and since antiphase boundaries (APB) have been observed in SiC, it is reasonable to assume that APB-s, perpendicular to the growth direction, could be produced by applying a "wrong sequence" of cycles in the homoepitaxial ALE or MBE growth of SiC. This could lead to C–C or Si–Si double layers, orthogonal to the c-axis, or – in other words – to polarity changes, without any strain in the system whatsoever. Using density functional theory with a hybrid functional (to reproduce the band gap correctly), we show here that such a structure in 4H-SiC would have capabilities for 1D-modulated electronics, similar to quantum well and doping superlattices in III-V compounds, opening up the possibility for a large variety of application in nano- and optoelectronics, as well as photonics.

5:30 PM
3-Dimensional Non-Destructive Dislocation Analyses in SiC Measured by Planar Electron-Beam-Induced Current Method: *Yuki Yanagisawa*[1]; Satoshi Nitani[1]; Tomoaki Hatayama[1]; Hiroshi Yano[1]; Yukiharu Uraoka[1]; Takashi Fuyuki[1]; [1]Nara Institute of Science and Technology

High-density defects has been a longstanding problem with SiC epilayers. In this paper, dislocations in SiC are analyzed for the first time by a planar EBIC method with a combination of a mapping technique and a selection of accelerating voltage. To analyze the defects in epilayers, Schottky contact electrode (Ni) with a thickness of 20nm to an all over epitaxial SiC surface. Three types of dark areas were observed in the EBIC image. A large dark area was a micropipe, and small dark area were screw and edge dislocations. It is considered that these dislocations would show a similar electric behavior for the minority carriers. The contrast of a comet-like dark area gradually increased for the down-step [11-20] direction, indicating the basal plane dislocation. Since a large number of minority carrier was generated at a peak depth, the minimum EBIC signal shifted to up-step [-1-120] with the increase of accelerating voltage. In order to characterize the depth information of EBIC signals, we analyzed the peak depth of maximum minority-carrier generation. The peak depth was proportional to the accelerating voltage to the 1.75, and was about 1/3 of the maximum penetration depth.

5:45 PM
Structural Defects and Critical Electric Field in 3C-SiC: *Michael A. Capano*[1]; [1]Purdue University

3C-SiC p-type epilayers were grown to thicknesses of 1.5, 3, 6 and 10 µm on 2.5° off-axis Si(001) substrates. Structural analyses were performed using transmission electron microscopy (TEM), high-resolution x-ray diffractometry (HRXRD), and Raman spectroscopy. TEM showed defect densities (stacking faults, twins and dislocations) decreasing with increasing distance from SiC/Si interface as the lattice mismatch stress is relaxed. This observation was corroborated by a monotonic decrease in HRXRD peak width (FWHM) from 780 arcsecs (1.5 µm epilayer) to 350 arcsecs (10 µm epilayer). Further reduction in x-ray FWHM is expected because the minimum FWHM detected is greater than the theoretical FWHM for SiC (about 12 arcsecs). Raman spectroscopy indicates the residual biaxial in-plane strain decreases with increasing epilayer thickness initially, but becomes essentially constant between 6 and 10 µm. Structural defect density shows the most significant reduction in the first 2 µm. Phosphorus implantation was applied to fabricate n+/p junctions to measure the critical electric field in 3C-SiC. The critical electric field in p-type 3C-SiC with a doping of $2x10^{17}$ cm^{-3} was $1.3x10^6$ V/cm. The implications of having a critical field of this magnitude will be discussed during the presentation.

6:00 PM
Structures of Comets in a Homoepitaxially Grown 4H-SiC Film Studied by DUV Micro-Raman Spectroscopy: *Takuro Tomita*[1]; Shigeki Matsuo[1]; Tatsuya Okada[1]; Tsunenobu Kimoto[2]; Takeshi Mitani[3]; Shin-ichi Nakashima[3]; [1]University of Tokushima; [2]Kyoto University; [3]National Insutitute for Advanced Industrial Science and Technology

The structures of comet defects in a 4H-SiC homoepitaxially grown film are investigated by deep-ultraviolet (DUV) micro-Raman spectroscopy. The light source used in this experiment was an intra-cavity frequency-doubled Ar^+ laser operated at 244 nm (Coherent 300C FreD). The laser beam was guided into the microscope and focused by a Cassegrain objective. The measurements were done in the back-scattering geometry. The sample used in this experiment was a 4H-SiC epitaxially grown film with a thickness of 9 µm. The substrate of this film was a 4H-SiC single crystal wafer off-cut (off-oriented) from the exact (0001) plane by 8°, while keeping projection of the direction. Spatial distribution of the 4H- and 3C-SiC is clearly distinguished both from the intensities of the folded longitudinal acoustic phonon mode and the peak energies of the nonfolded longitudinal optical phonon mode. We have measured the position dependence of Raman spectra for seven comets. It is found that the position dependence of Raman spectra in comets could be classified into two types. The mechanisms of heteropolytypic inclusion in comets will be discussed.

TC2.HF Devices

Tuesday, 4:30-5:45pm
September 20, 2005

Room: Allegheny Ballroom II & III
Location: Westin Pittsburgh

Session Chair: J. W. Palmour, Cree, Inc.

4:30 PM
High Power-Density 4H-SiC RF MOSFETs: *Gudjon Gudjonsson*[1]; Fredrik Allerstam[1]; Halldor O. Olafsson[1]; Per-Ake Nilsson[1]; Hans Hjelmgren[1]; Kristoffer Andersson[1]; Einar O. Sveinbjornsson[1]; Herbert Zirath[1]; Thomas Roedle[2]; Rik Jos[2]; [1]Chalmers University of Technology; [2]Philips Semiconductors

We report on fabrication and characterization of our first normally-off 4H-SiC power MOSFETs for radio frequency (RF) applications. The lateral device contains a buried p-well located underneath the gate serving as a punch-through prevent and a drain extension to improve the drain voltage handling capability. The field effect mobility extracted in long channel devices is 65 cm^2/Vs and the threshold voltage is about 7 V. Devices with a nominal channel length of 0.5 microns and gate oxide thickness of 100 nm exhibit DC drain current of 200 mA/mm at a gate voltage of 20 V, and a drain-source breakdown voltage above 100 V. The transistors have an intrinsic cutoff frequency, fT, of about 12 GHz and the transducer power gain is 8.7 dB at 3 GHz. Wafer level load-pull measurements at 3 GHz, limiting the field across the gate oxide to 2 MV/cm, give an output power of 1.6 W/mm at 3 dB gain compression. To our knowledge this is for the first time that power densities above 1 W/mm at 3 GHz are reported for SiC MOSFETs. The measured devices have a gate width of 0.8 mm.

4:45 PM
Fabrication of 700V SiC-SIT with Ultra-Low on-Resistance of 1.01mΩcm²: *Yasunori Tanaka*[1]; Koji Yano[2]; Mitsuo Okamoto[1]; Akio Takatsuka[1]; Kenji Fukuda[1]; Masanobu Kasuga[2]; Kazuo Arai[1]; Tsutomu Yatsuo[1]; [1]AIST; [2]Yamanashi University

Silicon carbide static induction transistors (SiC-SITs) with submicron buried p^+ gates have been successfully developed through the innovative fabrication process. The submicron buried p^+ gate structure was fabricated by the combination of the submicron trench dry etching process and epitaxial growth process on the trench structure. The gate electrode was formed on the p^+ area exposed by mesa etching outside the active area. As the device performance is mainly determined by the width of the p^+ gate region and the spacing between two adjacent p^+ gate regions, corresponding to the width of n^- channel region, we have optimized these parameters carefully by using ISE-TCAD device simulator. The breakdown voltage V_{BR} and the specific on-resistance R_{onS} of the fabricated SiC-SIT were 700V with the gate voltage V_g of –12V and 1.01mΩcm² at the current density J_D of 200A/cm² with the gate voltage Vg of 2.5V, which is a highest V_g with the unipolar action of SiC-SIT. This R_{onS} value is a lowest on-resistance among 600V-1.2kV class switching devices including the wide-bandgap materials such as SiC and GaN.

5:00 PM
The Improvement of RF Performance for Diamond MISFETs with Miniaturization of Gate Length: *Hidenori Takayanagi*[1]; Kazuyuki Hirama[1]; Mitsuya Satoh[1]; Hiroshi Kawarada[1]; [1]Waseda University

0.15-µm-gate diamond metal-insulator-semiconductor field-effect transistors (MISFETs) are fabricated on Hydrogen-terminated diamond surface. The highest transition frequency (f_T) of 30 GHz and the maximum frequency of oscillation for the maximum available gain (f_{max}) of 48 GHz are realized in this 0.15-µm-gate diamond MISFET. This f_T is the highest characteristics for diamond FETs ever reported.

5:15 PM
Demonstration of the First 4H-SiC Bipolar RF Power Limiter: *Ming Su*[1]; Xiaobin Xin[1]; Larry X. Li[2]; Jian H. Zhao[1]; [1]Rutgers, State University of New Jersey; [2]United Silicon Carbide, Inc.

We present the first RF power limiter fabricated from 4H-silicon carbide. The limiter was based on a SiC RF diode with up to 800V blocking capability with subnano-amper leakage current and packaged into a 50-ohm microstrip transmission line fixture. Small signal s-parameters are simulated and measured in the frequency band from 100MHz to 3GHz. The limiter has insertion loss less than 1.5dB up to 1.6GHz. This is believed to be the highest frequency a SiC based RF power limiter has achieved to date.

5:30 PM
4H-SiC Bipolar Transistors with UHF and L-Band Operation: *Ivan Perez*[1]; [1]Advanced Power Technology

We report for the first time on RF SiC BJTs fabricated on semi-insulating substrates with L-band performance. Small-periphery (4x150µm) devices were tested using on-wafer load pull measurements up to 1.5GHz. Under pulsed conditions, the devices exhibited 10dB of power gain at 1GHz and a peak power density of 2.3W/mm (1.4W) with less than 0.1dB pulse droop for a 100µs pulse width and a 1% duty cycle. The power gain decreased to 8dB at 1GHz under CW conditions at a power density of 1.6W/mm (1W). The load-pull measurements were performed up to 125°C, which resulted in a 1 dB reduction of power gain compared to the room temperature performance. Results at 0.5 and 1.5 GHz will be presented as well.

WA1.Bulk Growth II

Wednesday, 8:30-10:30am
September 21, 2005

Room: Allegheny Ballroom I
Location: Westin Pittsburgh

Session Chairs: D. L. Barrett, II-VI, Inc.; A. Ellison, Norstel AB

8:30 AM Invited
Advances and Challenges in Numerical Simulation of Bulk SiC Growth by PVT and CVD: Yu. Makarov[1]; [1]Semiconductor Technology Research, Inc.

Numerical simulation is a powerful tool used for analysis and optimization of SiC bulk crystals growth by Physical Vapor Transport (PVT) and Chemical Vapor Deposition (CVD). Review of recent progress in this area will be made with the goal to show how modeling can help to solve practical problems. Heat transfer plays crucial role in SiC bulk crystal growth. Modeling of temperature distribution in the whole growth system with accuracy of prediction of temperature gradients in the range of few grads is now possible using advanced commercial software tools on PC. Design of the growth system and hot zone can be supported by modeling analysis, which reduces time of development and modification of the hardware. This is especially effective when scaling of the crystal size has to be done. PVT growth is performed normally from SiC powder in a semi-closed crucible. For prediction of growth rate and interface shape of SiC crystal complex model of mass transport needs to be used to model sublimation of powder, chemical interactions with the crucible, exchange with external environment, formation of deposits and growth of the crystal. Additionally to that, formation of singular facet on the surface of the growing SiC crystal results in some kinetic limitations on the growth. Understanding of mechanisms of PVT growth generated by numerical simulations and experiments will be discussed. CVD growth is very promising technique for growth of bulk SiC which allows better control of species transport and Si/C ratio at the growing surface. But, complex chemical processes in the gas phase during the CVD require better understanding. In particular, formation of clusters in the gas phase results in significant loss of material and lower quality of the growing crystal. Mechanisms of formation of the clusters will be discussed in the paper. One of the possibilities to reduce the cluster formation during CVD growth of bulk SiC crystals is to use Cl-containing precursors. Mechanism of this process will be considered using simulations.

9:00 AM Invited
Halide-CVD Growth of Bulk SiC Crystals: *Alexander Y. Polyakov*[1]; Mark A. Fanton[2]; Marek Skowronski[1]; Hun Jae Chung[1]; Saurav Nigam[1]; Sung Wook Huh[1]; [1]Carnegie Mellon University; [2]Pennsylvania State University

A novel approach to the growth of bulk SiC is described. The Halide Chemical Vapor Deposition (HCVD) method uses $SiCl_4$, C_3H_8, and hydrogen as reactants. The use of halogenated Si source and of separate injection of Si and C precursors allows preheating the source gases without causing premature chemical reactions which is a distinct advantage over approaches employing silane as the Si precursor. The stoichiometry of HCVD crystals can be controlled by changing the C/Si flow ratio and can be kept constant throughout growth, in contrast to the Physical Vapor Transport technique. HCVD allows for growth of high crystalline quality, very high purity 4H- and 6H-SiC crystals with growth rates comparable to other bulk SiC growth techniques. The densities of deep electron and hole traps are determined by growth temperature and C/Si ratio and can be as low as that found in standard CVD epitaxy. At high C/Si flow ratio, the resistivity of HCVD crystals exceeds 10^5 Ωcm. The properties of crystals grown by HCVD make an attractive method for applications in high-frequency and/or high voltage devices.

9:30 AM
In-Situ Observation by X-Ray Imaging of Mass Transfer in the CF-PVT Growth Process: *Didier Chaussende*[1]; Peter Wellmann[2]; Magali Ucar[3]; Michel Pons[1]; Roland Madar[1]; [1]INPGrenoble - CNRS; [2]University of Erlangen; [3]NOVASiC

The development of the Continuous Feed Physical Vapour Transport (CF-PVT) process requires a perfect control of each phenomenon in the growth cell. Along this line, the present paper gives some inputs on the CF-PVT

mass transfer regimes with respect to the process parameters, both from qualitative and quantitative viewpoints. For example, two boundary cases have be evidenced depending on the temperature. At low temperature, the growth is limited by the sublimation step between the source and the seed. In this case, the CF-PVT process can be roughly assimilated to the classical seeded sublimation technique. At high temperature, the process is limited by the feeding step, i.e. the CVD deposition and infiltration on the lower part of the source. Measurements are correlated to in-situ X-ray imaging. The ability of the X-ray imaging to in-situ quantify the mass transfer is discussed.

9:45 AM
Growth and Characterization of Large Diameter 6H and 4H SiC Single Crystals: *Avinash K. Gupta*[1]; Edward Semenas[1]; Ejiro Emorhokpor[1]; John Chen[1]; Ilya Zwieback[1]; Andy Souzis[1]; Tom Anderson[1]; [1]II-VI, Inc.

Single crystals of silicon carbide, 6H and 4H polytypes, are grown using Advanced PVT (APVT) growth process. The process includes measures aimed at the reduction of background impurities, mostly nitrogen and boron. Undoped semi-insulating (SI) 6H-SiC crystals demonstrate residual N and B levels below $2 \cdot 10^{15}$ cm^{-3}. In commercial SI 6H-SiC substrates, stable semi-insulating properties are achieved by precise vanadium compensation. The technique of compensation is optimized to produce controlled and uniform vanadium doping. This resulted in total elimination of vanadium precipitates and high and spatially uniform electrical resistivity throughout the boule reaching 10^{11} Ω-cm or higher. Best quality 3-inch V-doped 6H-SiC substrates demonstrate micropipe densitiy of 3 cm^{-2}. N-type 3-inch 4H-SiC substrates are produced using doping with nitrogen. These substrates show uniform resistivity of 0.020 Ω-cm and micripipe density of 27 cm^{-2}.

10:00AM
Hybrid Physical-Chemical Vapor Transport Growth of SiC Bulk Crystals: *Mark Fanton*[1]; Qiang Li[2]; Alexander Polyakov[2]; Marek Skowronski[2]; Randal Cavalero[1]; Rodney Ray[1]; Brian Weiland[1]; [1]Pennsylvania State University; [2]Carnegie Mellon University

The effects of hydrogen addition to the growth ambient during physical vapor transport (PVT) growth of 6H and 4H SiC were investigated using SIMS, DLTS and Hall effect. Using this hybrid physical-chemical vapor transport (HPVT), boules were grown using Ar-H2 and He-H2 mixtures with H2 concentrations up to 50 at%. Thermodynamic modeling suggests that addition of hydrogen improves the carbon transport in HPVT compared to standard PVT. This should lead to a substantial decrease in the concentration of residual nitrogen donors and the concentration of electron traps. This is confirmed by experimental results. The background nitrogen concentration and the free electron density decrease significantly with increasing hydrogen concentration. The formation of electron traps (activation energies of 0.4 eV, 0.6-0.65 eV, 0.7 eV, 0.9 eV and 1 eV) was also strongly suppressed. These changes were observed for hydrogen concentrations as low as 4 at. %. The decreased nitrogen concentration improves the ability to produce high resistivity SiC material, and for hydrogen concentrations as high as 10-25%, the first wafers cut from the seed end of the boules have a resistivity exceeding 10e6 ohm-cm. Deep levels spectra were studied by Hall effect measurements and by photo-induced current transient spectroscopy PICTS.

10:15 AM Coffee Break

WA2.MOS Processing I

Wednesday, 8:30-10:15am
September 21, 2005

Room: Allegheny Ballroom II & III
Location: Westin Pittsburgh

Session Chairs: P. G. Neudeck, NASA Glenn Research Center; E. O. Sveinbjornsson, Chalmers University of Technology

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8:30 AM Invited
Impact of Dislocations on Gate Oxide in SiC MOS Devices and High Reliability ONO Dielectrics: *Satoshi Tanimoto*[1]; [1]Nissan Motor Co., Ltd.

SiC can be oxidized thermally to grow silicon dioxide (SiO_2), giving it significant advantages over other wide-bandgap materials, especially in power MOSFETs applications. However, thermal SiO_2 is inherently more conductive on SiC than on Si and also contains a certain density of extrinsic defects originating from dislocations on the substrate epilayer. As a result, power MOSFETs on SiC tend to suffer from poor reliability of the thermal gate-oxide. In this paper, a highly reliable $SiO_2/Si_3N_4/SiO_2$ (ONO) dielectric with an equivalent SiO_2 thickness of about 40 nm and a poly-Si gate is demonstrated on commercially available n-type 4H-SiC, which contains a high density of dislocations. Dielectric breakdown strength of BV_{ox} = 22 MV/cm is achieved at room temperature. It is shown that the maximum allowable current density, BJ_{ox}, is in the 30 A/cm^2 range and two to three orders of magnitude higher than that of a single thermal oxide. A time dependent dielectric breakdown (TDDB) test conducted on about 50 capacitors at room temperature under constant current stress reveals charge-to-breakdown, Q_{BD}, of about 50ºC/cm^2 at the 50% failure point and a steep Q_{BD} distribution.

9:00 AM
Nitrogen Implantation - An Alternative Technique to Reduce Traps at SiC/SiO2- Interfaces: Florin Ciobanu[1]; *Gerhard Pensl*[1]; Vateri Afanas'ev[2]; Adolf Schöner[3]; [1]University of Erlangen-Nürnberg; [2]University of Leuven; [3]ACREO AB

In this paper, we report a detailed study on the effect of N implantation, which is conducted prior to the thermal oxidation, on the density of interface states in n- and p-type 4H-/6H-SiC MOS capacitors. For the fabrication of MOS capacitors, we used n/p-type 4H-/6H-SiC epilayers ([N] = (1 to 9) x1016 cm-3 / [Al] = 3x1016 cm-3). The epilayers were deposited on either the Si- or the C-face by the chemical vapor deposition (CVD) technique. The nominally dry oxidation was conducted in pure O2 at 1120°C for 24 h on the Si-face and for 2 h on the C-face; all the samples were exposed to a post oxidation anneal in Ar for 1h. N implantation results in a strong decrease of the interface state density Dit close to the conduction bandedge and an increase of Dit in the lower half of the SiC bandgap. The oxidation of the Si-face leads to lower Dit values compared to the oxidation of the C-face. The observed change in the distribution of interface traps by the N implantation is explained in the framework of the "Carbon-Cluster-Model".

9:15 AM
Improved Dielectric and Interface Properties of 4H-SiC MOS Structures Processed by Oxide Deposition and N2O Annealing: *Tsunenobu Kimoto*[1]; Hiroaki Kawano[1]; Masato Noborio[1]; Jun Suda[1]; Hiroyuki Matsunami[1]; [1]Kyoto University

Since the residual carbon near the SiO2/SiC interface might be inherent to thermal oxidation of SiC, the authors have investigated the potential of deposited oxides for SiC MOSFET fabrication. SiO2 films have been deposited on 4H-SiC{0001} epilayers by plasma CVD at 400ºC. The thickness of deposited oxides is varied in the range from 40 nm to 85 nm. In order to improve the oxide quality, the samples are annealed in Ar or N2O (10% in N2) at 1300ºC for 60-360 minutes. N2O annealing has resulted in significantly improved dielectric properties (resistivity = 1E16 Ohmcm, EB > 10 MV/cm). The Dit values of "CVD + N2O anneal" sample are higher in the energetically deep region but lower near the conduction band edge (Dit = 3E11 cm-2eV-1 \@ EC - 0.2 eV), compared to N2O oxidation. High channel mobililties of 30-34 cm^2/Vs have been attained for 4H-SiC(0001) MOSFETs. MOSFETs fabricated on the 4H-SiC(000-1) face showed even higher mobilities of 46-51 cm^2/Vs. This process has been applied to fabrication of lateral RESURF MOSFETs. The fabricated 4H-SiC(0001) MOSFET exhibits a high breakdown voltage of 1450 V and a low on-resistance of 76 mOhmcm^2.

9:30 AM
Improved 4H-SiC MOS Interfaces Produced via Two Independent Processes: Metal Enhanced Oxidation and 1300°C NO Anneal: *Mrinal K. Das*[1]; Brett A. Hull[1]; Sumi Krishnaswami[1]; Fatima Husna[1]; Sarah Haney[1]; James D. Scofield[2]; Aivars Lelis[3]; Charles J. Scozzie[3]; [1]Cree, Inc.; [2]AFRL; [3]ARL

Two previously reported MOS processes, oxidation in the presence of metallic impurities and annealing in nitric oxide (NO), have both been optimized for compatibility with conventional 4H-SiC DMOSFET process technology. Metallic impurities are introduced by oxidizing in an alumina environment. This Metal Enhanced Oxidation (MEO) yields controlled oxide thickness and robustness against high temperature processing and operation while maintaining high mobility (69 cm^2/Vs) and near ideal NMOS C-V characteristics. Raising the NO anneal temperature from 1175°C to 1300°C results in a 67% increase in the mobility to 49 cm^2/Vs with slight stretch-out in the NMOS C-V. Both processes exhibit a small 30% mobility reduction in MOSFETs fabricated on N_A = 1E18 cm^{-3}/ implanted p-wells. The low field mobility in the MEO MOSFETs is observed to increase dramatically with measurement temperature to 160 cm^2/Vs at 150°C.

9:45 AM Invited
Nitrogen and Hydrogen Induced Trap Passivation at the SiO_2/ 4H-SiC Interface: *Sarit Dhar*[1]; Sokrates T. Pantelides[1]; Leonard C. Feldman[1]; Tamarra Isaacs-Smith[2]; Shurui Wang[2]; John R. Williams[2]; [1]Vanderbilt University; [2]Auburn University

Post-oxidation anneals that introduce nitrogen at the SiO_2/4H-SiC interface are most effective in reducing the large interface trap density (D_{it}) near the 4H-SiC conduction band-edge. Herein, we report the effect of nitridation on interfaces created on the (11-20) a-face and the (000-1) C-face of 4H-SiC. Significant reduction of Dit (from >10^{13}cm^{-2} eV^{-1} to ~10^{12}cm^{-2} eV^{-1} at E_c-E ~0.1 eV) was observed for all faces, indicating the presence of nitrogen susceptible defects in interfaces formed via significantly different oxidation kinetics. Annealing nitridated interfaces in hydrogen results in a further reduction of trap densities (from ~10^{12}cm^{-2} eV^{-1} to ~ 5 x 10^{11}cm^{-2} eV^{-1} at E_c-

E ~0.1 eV). Using sequential anneals in NO and H_2, maximum field effect mobilities of ~55 cm^{-2} $V^{-1}s^{-1}$ and ~100 cm^{-2} $V^{-1}s^{-1}$ have been obtained for lateral MOSFETs fabricated on the (0001) Si-face and (11-20) a-face respectively. These electronic measurements have been correlated to interfacial structure and composition studied by a variety of techniques such as electron energy loss spectroscopy (EELS), surface enhanced Raman spectroscopy (SERS), nuclear reaction analysis (NRA) and secondary ion mass spectrometry (SIMS).

10:15 AM Coffee Break

WB1.Dopants and Impurities

Wednesday, 10:45am-12:40pm Room: Allegheny Ballroom I
September 21, 2005 Location: Westin Pittsburgh

Session Chairs: R. P. Devaty, University of Pittsburgh; J. Steeds, University of Bristol

10:45 AM Invited
Electronic Structure and Magnetic Properties of Transition Metal Doped Silicon Carbide in Different Polytypes: *Maosheng Miao*[1]; Walter R.L. Lambrecht[1]; [1]Case Western Reserve University

We report density functional calculations using the atomic sphere approximation as well as full-potential linearized muffin-tin orbital method on first row transition metal doped Silicon Carbide in both cubic (3C) and hexagonal (4H) polytypes. We found a strong preference for Si site substitution even under C-rich condition. We also found that the early TMs (Ti and V) and late TMs (Fe and Co) are in a low spin configuration. The energy levels in the gap for Ti, V and Cr are in good agreement with the available photoluminescence experiments. Our calculation shows that the Ti impurity is active for 4H but not for 3C, while V and Cr impurities are active for both polytypes. The magnetic interactions are very different for Cr and Mn. Cr shows a very local exchange interaction that decays rapidly after second nearest neighbor, which is similar for different polytypes and different sites. The exchange interaction for Mn is quite long range and is very sensitive to the polytypes and the location of the Mn pairs. However, the magnetic interaction is quite strong, indicating a possible high Curie temperature in such systems.

11:15 AM
Evidence for Phosphorus on Carbon and Silicon Sites in 4H, 6H and 15R SiC: F. Yan[1]; R. P. Devaty[1]; *W. J. Choyke*[1]; A. Gali[2]; I. B. Bhat[3]; D. J. Larkin[4]; [1]University of Pittsburgh; [2]Budapest University of Technology and Economics; [3]Rensselaer Polytechnical Institute; [4]NASA Glenn Research Center

A number of theoretical groups have been studying the doping with phosphorus in 4H SiC and have come to the conclusion that, while phosphorus prefers to substitute for silicon (P_{Si}), there is a finite chance that it also substitutes for carbon (P_C). In this paper we give low temperature photoluminescence results and some theoretical discussion for 4H, 6H and 15R SiC which indicates that contrary to nitrogen, which substitutes only on the carbon sublattice, phosphorus can substitute on both the silicon and carbon sites. Experiments were carried out on epitaxial films grown over a number of years, in two cold wall CVD reactors, at the NASA Glenn Research Center and at the Rensselaer Polytechnical Institute (RPI).

11:30 AM
Photoluminescence of Phosphorus Doped SiC: *Anne Henry*[1]; Erik Janzén[1]; [1]Linköping University

We report the results of a photoluminescence (PL) study from n-type phosphorus-doped SiC epilayers. PL spectra are constituted of a set of sharp lines which are interpreted as excitons bound to the P donor. Depending on the polytype the PL spectrum consists of one or several zero-phonon lines, which have photon energy very close to or similar to the nitrogen-bound excitons and they are followed by their phonon assisted replicas. The intensity of the PL spectrum depends on the concentration of P introduced during the growth of the epilayers but can be reduced by the presence of the nitrogen donor.

11:45 AM
Donor-Acceptor Pair Luminescence of Phosphorus-Aluminum and Nitrogen-Aluminum Pairs in 4H SiC: *Ivan G. Ivanov*[1]; Anne Henry[1]; Erik Janzén[1]; [1]Linköping University

The donor-acceptor pair luminesce due to P-Al pairs in 4H-SiC is investigated. The samples are grown by chemical vapor deposition (CVD) in a horizontal hot-wall reactor and intentionally doped in situ with phosphorus and aluminum simultaneously. The recorded spectra show strong donor-acceptor pair luminescence with no contribution from nitrogen-aluminum pairs. The observed pair luminescence is thus attributed entirely to P-Al pairs. The experimental spectra are fitted with theoretically modeled ones. It is shown that in the case of P-Al pairs the spectra fit to the theoretical model using both P_k-Al_h and P_k-Al_k pairs residing on the Si sublattice (so-called type I spectra), where the subscripts "h" and "k" denote the hexagonal and cubic lattice site, respectively. This makes possible the identification of the shallowest P donor as P_k with ionization energy of 60.7 meV. The difference between the ionization energies of the aluminum acceptors at the two lattice sites is determined, 3.4 meV, and their values are justified, 197.9 and 203.1 meV for aluminum at the hexagonal and cubic sites, respectively. The case of N-Al pair luminescence is revisited as well, and the ionization energy of the deeper nitrogen donor (substitutional for carbon at cubic site) is determined, 125.5 meV.

12:00 PM
Extracting Activation and Compensation Ratio from Aluminum Implanted Layers by Modeling Resistivity Measurements: *Martin Rambach*[1]; [1]University of Erlangen-Nuremberg

Ion implantation is the only practical method to produce laterally structured doped layers in SiC. A subsequent annealing step is performed for activation of implanted atoms. For charac-terization of the annealing step, the measurement of the activation ratio and the degree of compensation is necessary. Usually, this is done by Hall measurements. But, preparation of Hall samples and temperature dependent Hall measurements are rather complex compared to temperature dependent resistivity measurements by 4-point probing, for example. Therefore, a model for extracting relevant electrical parameters from resistivity data only has been devel-oped and will be presented. The model is based on the neutrality equation and a temperature dependent Caughey-Thomas mobility model. The calibration of the developed resistivity model is done by Hall measurements of free carrier concentration and mobility data. Applying the developed metrology on resistivity data measured by 4-point probing shows identical re-sults compared to Hall measurements.

12:15 PM
Co-Doping of Er-Doped SiC with Oxygen - A Promissing Way Towards Efficient 1540 nm Emission at Room Temperature?: *Uwe Gerstmann*[1]; Eva Rauls[2]; Simone Sanna[1]; Harald Overhof[1]; Thomas Frauenheim[1]; [1]University of Paderborn; [2]University of Aarhus

Rare-earth-doped semiconductors can be used as light-emitting diodes or lasers. Of particular interest is Erbium. Its intra 4f-shell transition at 1540 nm coincides with the absorption-minimum of typical silica-based optical fibers. The main problem arises due to rather low luninescence at room temperature. In silicon, this is improved by co-doping with oxygen, otherwise the transition is parity-forbidden. In compound-semiconductors, the ligand-field is expected to be strong enough to break the parity: e.g. in Er-doped SiC an efficient emission assigned to isolated Er-ions is achieved until thermal quenching arises above 240 K. In this work, ab-initio calculations are performed in the framework of density functional theory using self-interaction corrected optimized effective potentials (SIC-OEP) to account for the strong localisation of the f-electrons. Calculated hyperfine splittings for isolated Er ions are in agreement with the experimental data for axial EPR-spectra. Spectra with lower symmetry can be assigned to Er-donor pairs. In comparison with the isolated Er ions, the energy level in case of (Er-O)+ pairs is considerably lowered. Since thermal quenching of the IR-emission is related to the position of the Er-level below the conduction band,co-doping with oxygen would be very desirable also in SiC, providing more intense emission at room temperature.

12:30 PM Introduction to Invited Poster (Extended Defects III)
Characterization of SiC Crystals by Using DUV Excitation Raman Scattering Spectroscopy: *Shin-ichi Nakashima*[1]; Takeshi Mitani[1]; [1]National Institute of Advanced Industrial Science and Technology

12:35 PM Introduction to Invited Poster (Bulk Growth II)
Fundamental Limitations of SiC PVT Growth Reactors with Cylindrical Heaters: *R. Drachev*[1]; E. Deyneka[2]; C. Rhodes[3]; J. Schupp[1]; T. Sudarshan[3]; [1]Schupp Advanced Materials LCC; [2]North Carolina A&T State University; [3]University of South Carolina

WB2.MOS Processing II

Wednesday, 10:45am-12:20pm Room: Allegheny Ballrm II & III
September 21, 2005 Location: Westin Pittsburgh

Session Chairs: T. Kimoto, Kyoto University; M. K. Das, Cree, Inc.

10:45 AM Invited
High Channel Mobility 4H-SiC MOSFETs: *Einar O. Sveinbjornsson*[1]; Gudjon Gudjonsson[1]; Fredrik Allerstam[1]; Halldor O. Olafsson[1]; Per-Ake Nilsson[1]; Herbert Zirath[1]; Thomas Rödle[2]; Rik Jos[2]; [1]Chalmers University of Technology; [2]Philips Semiconductors

We report investigations of MOS and MOSFET devices using a gate oxide grown in the presence of sintered alumina. In contrast to conventionally grown dry or wet oxides these oxides contain orders of magnitude lower density of near-interface traps at the SiO2/SiC interface. The absence of near-interface traps makes possible fabrication of Si face 4H-SiC MOSFETs with field effect mobility of about 150 cm^2/Vs. In addition, a stable operation of such normally-off 4H-SiC MOSFET transistors is observed from room temperature up to 300°C with positive threshold voltage shift less than 2 V. A small decrease in current with temperature up to 150°C is related to a decrease in the field effect mobility due to phonon scattering. We demonstrate a clear correlation between the field effect mobility in n-channel MOSFETs and the density of interface states near the SiC conduction band edge in n-type MOS capacitors. The total trapped charge in near-interface traps is less than 1x1011 cm^{-2} in reference samples to devices with mobility of 150 cm^2/Vs. The interface state passivation is stable up to 300°C. Rapid thermal anneal above 700°C after oxidation results in partial reappearance of the near-interface traps.

11:15 AM
Process Optimisation for <11-20> 4H-SiC MOSFET Applications: *Caroline Blanc*[1]; Dominique Tournier[2]; Phillipe Godignon[2]; D. J. Brink[3]; Jean Camassel[1]; [1]Université Montpellier 2; [2]CNM; [3]University Pretoria

Because of a superior lattice recovery during post-implantation annealing, complemented by a better quality of the layer to oxide interface, non standard <11-20>-oriented p-type 4H-SiC layers possess much potential for SiC power MOSFET applications. However, similar to the well-mastered silicon technology, many steps of the final process remain surface-orientation dependent and have to be separately optimised. In a previous work, we focussed on the growth of low doped p-type epitaxial material. Using SIMS, we could calibrate the deposition conditions and set a non-destructive LTPL (Low Temperature PhotoLuminescence) technique to get a quantitative estimate of the residual doping. In this work we focus on the optimisation of oxidation conditions and show that, using a novel two step procedure, excellent device performances can be reached. From more than 100 different measurements performed on a full 35 mm wafer, we find an average mobility of 147 cm^2/Vs, with a peak value in the range of 320 cm^2/Vs. To the best of our knowledge, this is one of the best results ever reported for 4H-SiC MOSFET devices.

11:30 AM
High Inversion Channel Mobility of 4H-SiC MOSFETs Fabricated on C(000-1) Epitaxial Substrate with Vicinal (Below 1°) Off-Angle: *Kenji Fukuda*[1]; Makoto Kato[1]; Shinsuke Harada[1]; Kazutoshi Kojima[1]; [1]National Institute of Advanced Industrial Science and Technology

SiC power MOSFET is expected to be normally-off type fast switching device. The on-resistance of SiC power MOSFETs is much higher than the value predicted from the physical properties of SiC. This is caused by the low channel mobility due to high interface state density (Dit). Many researchers studied improvement technique of channel mobility. We have already reported that the 4H-SiC MOSFET on the C(000-1) face have higher inversion-channel mobility. However, there is SiO2/SiC interface roughness problem in SiC MOSFETs. There are many steps at SiO2/SiC interface because the high off-angle is necessary for SiC epitaxial growth. These steps make SiO2/SiC interfaces rough, which lead to reduction of channel mobility. In this work, we have investigated the effect of the off-angle on inversion channel mobility of 4H-SiC MOSFETs fabricated on the C(000-1) face. The inversion channel mobility of 4H-SiC MOSFET with the vicinal off-angle(below 1°) is higher than that of 4H-SiC MOSFET with 8° off-angle. The peak value of channel mobility of 4H-SiC MOSFET with the vicinal off-angle is 92.3cm^2/Vs. The reduction of off-angle is very useful for improvement of channel mobility. The C(000-1) epitaxial substrate with vicinal off-angle would be suitable for DMOS type SiC power MOSFETs.

11:45 AM
Characterization of 4H-SiC MOSFETs with NO-Annealed CVD Oxide: *Hiroshi Yano*[1]; Tomoaki Hatayama[1]; Yukiharu Uraoka[1]; Takashi Fuyuki[1]; [1]Nara Institute of Science and Technology

Improvement of channel mobility in 4H-SiC MOSFETs is strongly required to achieve high-performance SiC MOS devices. Deposited oxide is an attractive gate oxide due to absence of carbon at the MOS interface. We fabricated and characterized Si-face 4H-SiC n-MOS capacitors and n-ch MOSFETs with CVD oxide annealed in NO at 1250ºC. Nitrogen and carbon concentration in the oxide was evaluated by SIMS. The CVD/NO sample has lower interface state density near Ec and higher nitrogen concentration at the interface than the Dry/NO sample. Channel mobility of 27.7 cm^2/Vs was obtained for MOSFETs with CVD/NO gate oxide, which is higher than the Dry/NO sample (24.9 cm^2/Vs). As for N2 annealed sample, channel mobility of CVD/N2 and Dry/N2 samples is 6.0 and 3.9 cm^2/Vs, respectively. These results are correlated with the interface state density and nitrogen concentration at the interface. Combination of low carbon concentration of the CVD oxide and nitridation by NO at high temperature results in improved MOS performance.

12:00 PM
Low Temperature Deposition of HfO_2 Gate Insulator on SiC by Metalorganic Chemical Vapor Deposition: *Shiro Hino*[1]; Tomohiro Hatayama[1]; Naruhisa Miura[2]; Tatsuo Ozeki[2]; Eisuke Tokumitsu[1]; [1]Tokyo Institute of Technology; [2]Mitsubishi Electric Corporation

Although SiC MOSFETs are promising for power device applications, the interface quality of the thermally-grown SiO_2/SiC needs drastic improvement. A simple alternative way to obtain the good interface quality is the deposition of the gate-oxide film. In this work, we have deposited HfO_2 gate insulator on 4H-SiC by metalorganic chemical vapor deposition (MOCVD) and interface properties are characterized. To suppress the oxidation of the SiC substrates during the HfO_2 deposition, we deposited HfO_2 films as low as 190°C. We use HfO_2 as a gate insulator because the Hf-precursors easily react with oxidants than Si precursors and we can expect high-quality HfO_2 films even at low deposition temperatures. HfO_2 films were deposited by source-gas-pulse-introduced MOCVD using $Hf[N(C_2H_5)_2]_4$ and H_2O. We first confirmed using HfO_2 films deposited on Si that the Hf-precursor can be effectively decomposed with H_2O supply and high-quality HfO_2 films with low leakage current can be obtained even at a deposition temperature of 190°C. Next, we deposited HfO_2 films at 190°C on HF-etched SiC substrates. It is demonstrated by the capacitance-voltage (C-V) characteristics that the interface state density of the HfO_2/SiC fabricated in this work is lower than that of the thermally-grown SiO_2/SiC.

Lunch

Wednesday, 12:40-1:50pm
September 21, 2005

Room: Spirit of Pittsburgh
Location: Convention Center

WP.Wednesday Poster Sessions

Wednesday, 1:50-4:10pm
September 21, 2005

Room: Spirit of Pittsburgh Foyer
Location: Convention Center

WPG1.Bulk Growth II

Invited
Fundamental Limitations of SiC PVT Growth Reactors with Cylindrical Heaters: *R. Drachev*[1]; E. Deyneka[2]; C. Rhodes[3]; J. Schupp[1]; T. Sudarshan[3]; [1]Schupp Advanced Materials LCC; [2]North Carolina A&T State University; [3]University of South Carolina

Despite the fact that structural quality of PVT grown SiC ingots has been significantly improved in the last decade, the SiC boule size and quality are still far behind those that Si technology features at the present time. As a result, availability, price and nomenclature of SiC electronic devices are yet to reach desirable levels. This situation can be attributed not only to the lack of SiC PVT growth studies, but also to fundamental limitations of the conventional furnace designs utilizing a single cylindrical inductive or resistive heater, which are incapable to provide stable repeatability and control accuracy of SiC PVT growth conditions. In order to overcome these limitations, the alternative furnace design with two plane resistive heaters is suggested. It features two independently controlled heaters and allows controllable variation of the heat dissipation through the crucible side surface, thus offering high flexibility of setting the growth conditions within the furnace. Numerical modeling and simulation of the thermal fields in the growth cells along with shear stress distribution in the basal planes of the growing SiC boules were performed to demonstrate the advantages of proposed furnace design.

Solution Growth of SiC Crystal with High Growth Rate using Accelerated Crucible Rotation Technique: *Kazuhiko Kusunoki*[1]; Kazuhito Kamei[1]; Nobuhiro Okada[1]; Nobuyoshi Yashiro[1]; Akihiro Yauchi[1]; Toru Ujihara[2]; Kazuo Nakajima[3]; [1]Sumitomo Metal Industries, Ltd.; [2]Nagoya University; [3]Tohoku University

We performed solution growth of SiC crystal from Si-Ti-C ternary solution using accelerated crucible rotation technique (ACRT) and conducted numerical analysis of fluid flow during the solution growth. We focused on the effect of forced convection by ACRT on the SiC growth rate. It is clearly found that SiC crystal obtained using ACRT is approximately twice as thick as that obtained without ACRT. It was confirmed that growth rate above 200μm/hr was

achievable by several ACRT sequences. In non-ACRT crystal, we sometimes observed the incorporation of the solution into the grown crystal. On the other hand, we hardly observed this type of defects in the ACRT crystal. It was thought that an increase in the level of solution mixing near the crystal/liquid interface resulted in not only marked increase of SiC growth rate but also a much greater degree of the homogenetiy in the growth morphology. Numerical analysis indicated that the intensity of solution stirring near the crystal/liquid interface increases using ACRT. It concluded that faster stable growth could be possible in the SiC solution growth using ACRT.

Growth Kinetics and Polytype Stability in Halide Chemical Vapor Deposition of SiC: *Saurav Nigam*[1]; Hun Jae Chung[1]; Sung Wook Huh[1]; Alexander Y. Polyakov[1]; Marek Skowronski[1]; Mark A. Fanton[2]; Brian E. Weiland[2]; D. W. Snyder[2]; [1]Carnegie Mellon University; [2]Pennsylvania State University

Dependence of growth rates of 6H- and 4H-SiC on growth conditions was investigated during Chemical Vapor Deposition process using halogenated silicon source (specifically $SiCl_4$), propane, and hydrogen as reactants. Growth experiments were performed in the temperature range of 2000°C-2150°C, C/Si flow ratios between 0.06 and 0.72, and hydrogen flow rate between 0.5 slm and 5 slm. We present a simple thermodynamic model of the chemical processes occurring inside the injectors and the reaction zone, and analyze the growth rate dependence on the input reactants flow and temperature. We conclude that the growth rate and C/Si ratio in the gas phase near the growing crystal can be controlled by the flow of hydrogen or by the flows of Si and C precursors in two different growth regimes referred to as thermodynamic-equilibrium-limited regime and reaction-kinetics-controlled regime Factors facilitating formation of either 6H or 4H polytypes will be discussed.

A Study of Nitrogen Incorporation in the Bulk Growth of n+ 4H SiC by PVT: *Darren M. Hansen*[1]; Mark Loboda[1]; Gil Chung[1]; [1]Dow Corning

A detailed understanding of the incorporation of N2 gas during PVT growth of SiC is required to achieve high performance, low resistivity n+ SiC substrates necessary for power device applications. In this report, nitrogen incorporation is investigated for growth of 4H SiC crystals for both 2" and 3" diameters ranging from unintentionally doped to low resistivity (0.015 Ohm-cm). For a wafer in a particular boule a resistivity uniformity of ± 5% is typical although the uniformity decreases as the wafer orientation is cut off axis from the bulk growth orientation. Within a boule growth, the resistivity is found to increase as wafers are cut further from the seed. These axial and radial gradients are thought to be a function of the changing C/Si ratio during growth. Resistivity and nitrogen incorporation as a function of PVT geometry, N2 partial pressure, and growth temperature are investigated and discussed. Resistivity is found to depend on the crucible size and nitrogen partial pressure, but is not dependent on the absolute growth temperature ranging over 150°C. Trends and N2 gas incorporation behavior will be discussed using resistivity mapping, SIMS, Hall effect data, and modeling of the growth process.

Growth of SiC Single Crystal from Si-C-(Co, Fe) Ternary Solution: *Nobuyoshi Yashiro*[1]; Kazuhiko Kusunoki[1]; Kazuhito Kamei[1]; Akihiro Yauchi[1]; Mitsuhiro Hasebe[1]; Toru Ujihara[1]; Kazuo Nakajima[1]; [1]Sumitomo Metal Industries Ltd/Corporate Research & Development Laboratories

We carried out the growth of single crystalline silicon carbide (SiC) from Si-C-X (X=Co, Fe) ternary solution. These ternary solutions are expected to show a large carbon solubility compared with Si solvent (self flux) by means of CALPHAD (CALculation of PHAse Diagrams) method. We investigated the growth morphology, growth rate and polytype of SiC using the ternary solution. Then we found out that the growth rate from the ternary solution is much larger than that from the self flux. The grown SiC crystal can be classified into 6H which takes over the seed polytype.

Growth of SiC Boules with Low Boron Concentration: *Mark Fanton*[1]; Randal Cavalero[1]; Brian Weiland[1]; Rodney Ray[1]; David Snyder[1]; Richard Gamble[1]; Edward Oslosky[1]; William Everson[1]; [1]Pennsylvania State University

The effects of growth conditions, barrier coatings, and hot zone materials on boron incorporation in SiC crystals grown by physical vapor transport (PVT) were evaluated. Development of high purity source material with a boron concentration less than $1.8e^{15}$ atoms/cm^3 was key to the growth of boules with a boron concentration less than $3.0e^{16}$ atoms/cm^3 and is described in detail. Application of refractory metal carbide coatings to graphite to serve as boron diffusion barriers and the use of high purity pyrolytic graphite components lead to the growth of SiC boules with boron concentrations as low as $2.4e^{15}$ atoms/cm^3 as measured by SIMS. The full range of materials evaluated and their impact on SiC purity will be discussed. The effect of growth temperature and pressure were examined over a range from 2100°C to 2300°C and 5 to 13.5 torr respectively. This range of crystal growth conditions and growth rates had no effect on boron incorporation. Attempts to alter the gas phase stoichiometry through addition of hydrogen gas to the growth environment also had no impact on boron incorporation. These results are explained by considering site competition effects and the ability of boron to diffuse through the graphite growth cell components.

Solution Growth of Cubic Silicon Carbide: *Jean-Louis Santailler*[1]; Jessica Eid[1]; Jean Camassel[2]; Efstathios Polychrionadis[3]; Carole Balloud[2]; Felipe Soares[2]; A. Mantzari[3]; [1]CEA Grenoble; [2]UM2 CNRS GES; [3]University of Thessaloniki

Cubic silicon carbide (3C-SiC) crystals have been grown from solution by using the traveling-zone method. A molten silicon zone heated by induction coils is held between two rods of polycrystalline silicon carbide. A single-crystalline SiC seed is fixed to the lower rod. A temperature gradient between the dissolving and growing interfaces results from a slow downward motion of the system through the heater. The temperature range is kept well around 1600°C to reduce the silicon evaporation and, ensure dissolution of silicon carbide into silicon. Different mass transfer mechanisms are operative : diffusion, marangoni and forced convection. Starting from an a-SiC seed, one obtains crystallization of ß-SiC. The growth experiments have been made on the <0001>-face of 4H-SiC seeds. The seeds were 3mm thick, 12mm diameter, and the growth duration was 20 hours. The resulting samples were 4 mm thick, which corresponds to a growth rate of 0.2 mm/h. As usual for the growth of cubic SiC on hexagonal seeds, the ß-SiC crystals had <111> habits. Identification of the 3C/4H hetero-polytype interface was made by µ-Raman spectroscopy. X rays analysis and LTPL (Low Temperature Photoluminescence) measurements as well as Transmission Electron Microscopy (TEM) observations showed a good crystalline quality.

Modelling and Experimental Verification of SiC M-PVT Bulk Crystal Growth: Peter J. Wellmann[1]; Ralf Müller[1]; Michel Pons[2]; [1]Materials Department 6; [2]INPG

In the Modified-PVT (physical vapor transport) technique an additional gas pipe is used to feed species into the gas room of a conventional seeded sublimation growth setup in order to fine-tune the gas phase composition in front of the crystal growth interface. In the current paper we study the impact of the additional gas flow on the global temperature field, the latter being of importance for growth process stability and high crystal growth quality. We have performed a systematic study using experiments and numerical modelling in order to address the physical and chemical effects responsible for the observed temperature variations during growth runs. In particular we varied the amounts of inert gas helium and/or propane as additional gas flow through the pipe and argon or nitrogen as ambient atmosphere. We found that the experimentally observed temperature variations during change of gas inlet cannot be attributed to physical (heat and mass transfer) or chemical (reactivity) phenomena inside the growth cell. We found that the impact of the varying additional gas flux on the crucible temperature may be attributed to a change of the isolation material heat conductivity by the outlet gas stream which may diffuse into the porous graphite foam isolation.

Active Thermal Interaction of Source and Crystal Surfaces in PVT SiC Crystal Growth: *Krzysztof Grasza*[1]; Emil Tymicki[1]; Jaroslaw Kisielewski[1]; [1]Institute of Electrical Material Technology

Development of flat facet on the growth interface improves crystal quality. A highly convex interface shape allows enlargement of the single-crystalline part of the crystal. Good compromise is strong convex temperature field at the seed/crystallization front edges, which make possible increase of the crystal diameter, and flat temperature field in the middle of the crystallization front, what allows facet growth in central part of the crystal [Z.G.Herro et.al., J.Cryst.Growth 262 (2004) 105]. Changing the temperature field the growth mechanism can be chosen, because extension of facet is possible by flattening of the thermal field [K.Grasza, J.Cryst.Growth 146 (1995) 69]. Silicon carbide crystals were grown from the vapour. Improvement of the quality of the central part of the crystal was achieved by optimization of geometry of the source material. The source was pre-grown in separate growth runs. Temperature field further stimulated shape of the source material during the decent growth runs. The active thermal interaction of the source material free interface and the crystallization front made possible effective stimulation of the shape and morphology of the free surface of the crystal. The repeatability of the optimal growth conditions was considerably increased. The morphological stability of the crystallization front was improved.

The Method for Enhancing Nitrogen Doping in 6H-SiC Single Crystals Grown by Sublimation Process: The Effect of Si Addition in SiC Powder Source: *Kwan-Mo Kim*[1]; Soo-Hyung Seo[1]; Jae-Woo Kim[1]; Myung-Hwan Oh[1]; Wook Bahng[2]; Joon-Suk Song[1]; Eun-Dong Kim[2]; [1]NeosemiTech Corp.; [2]Korea Electrotechnology Research Institute

The variation of nitrogen doping concentration was systematically investigated as the amount of silicon powder added in SiC powder for growing n-type 6H-SiC single crystal by sublimation method. To change intentionally Si/C ratio in SiC powder, a silicon powder was added to first-baked SiC powder by controlling from 0wt% to 2wt% and the mixed powder was treated again for eliminating excess free-metallic silicon at 1800°C for 3 hours. Nitrogen doped 6H-SiC single crystals were grown by using second-baked SiC powder at fixed N2/(Ar + N2) (3%). The nitrogen doping concentration of 6H-SiC crystals were increased with increasing the Si/C ratio in SiC powder. In this work, we could identify that the additional silicon powder in SiC powder plays a role in enhancement for nitrogen doping in 6H-SiC crystals grown by sublimation method.

WPP1.Advanced Processing

RF Characteristics of Fully Ion-Implantated MESFET on a Bulk Semi-Insulating 4H-SiC Substrate: Manabu Arai[1]; *Makoto Ogata*[1]; Shuji Katakami[1]; Shoichi Ono[1]; [1]New Japan Radio Co., Ltd.

Ion implantation is an important process that enables SiC-device manufactures to control doping species and densities in a selected region in a device. In the case of SiC-MESFETs, ion implantation is used to make a highly doped contact region in an epitaxial channel layer as the source and the drain regions. Accordingly, we have applied ion implantation to make a channel region in a bulk semi-insulating substrate for a MESFET. The fabricated fully ion-implanted MESFET shows a typical dc characteristic, though large drain conductance is observed at high drain voltage. Small-signal-characteristics measurement found that a 0.5-µm-gate MESFET with a 100-µm gate width has a cut-off frequency of 7.5 GHz and a maximum oscillation frequency of 22.2 GHz. And this MESFET had an output power of 25 dBm, which is equal to the output-power density of 3.16 W/mm, a power gain of 6.7 dB, and a power-added efficiency of 15.7%. These RF characteristics are almost equivalent to the previous results we obtained from a MESFET fabricated on a typical epitaxial substrate. This is the first report regarding the RF characteristics of a fully ion-implanted MESFET on a bulk semi-insulating SiC substrate.

Deep Reactive Ion Etching (DRIE) of High Aspect Ratio SiC Microstructures using a Time-Multiplexed Etch-Passivate Process: *Laura J. Evans*[1]; Glenn M. Beheim[1]; [1]NASA Glenn Research Center

We report deep (>100 µm) reactive ion etching (DRIE) of SiC microstructures with high aspect ratios (>5). High aspect ratio SiC microstructures are needed for microengines and other power MEMS. Previously, DRIE of low aspect ratio (=1) features to depths >100 µm in SiC has been reported. However, existing processes are not well-suited for high aspect ratio SiC features because they provide insufficient control over sidewall slope and roughness. Therefore, we have investigated the use of a time-multiplexed etch-passivate (TMEP) process which alternates etch and passsivation steps; this provides increased control over sidewall slope and roughness. The TMEP experiments were performed in an inductively coupled plasma (ICP) etcher, using SF_6 for etching and C_4F_8 for passivation. The samples were n-type, off-axis, Si-face 6H-SiC. An etch mask patterned with various width trenches was produced by selective electroplating of nickel. A 2^3 full factorial design was used to optimize the process for maximum etch rate and sidewall slope. Using the optimized TMEP process, trenches with depths >100 µm and aspect ratios >5 were etched. The TMEP process was also used to etch micro-scale turbine blades in 6H-SiC to a depth of 109 µm at a rate of 0.17 µm/min.

Development and Investigation on EBAS-100 of 100 mm Diameter Wafer for 4H-SiC Post Ion Implantation Annealing: *Masami Shibagaki*[1]; Yasumi Kurematsu[1]; Kenji Numajiri[1]; Fumio Watanabe[2]; Shigetaka Haga[2]; Kuniaki Miura[2]; Shingo Miyagawa[3]; Tomoyuki Suzuki[3]; Masataka Satoh[3]; [1]ANELVA Corporation; [2]Sukegawa Electric Co. Ltd.; [3]Hosei University

We developed EBAS-100, in which is available to 100 mm diameter SiC wafer, for post ion implantation annealing in order to realize silicon carbide (SiC) device with large volume production. EBAS-100 is able to perform the rapid thermal process due to the vacuum thermal insulation and small heat capacity of susceptor. Electrical power consumption density was 18.8 Wh/cm^2 for EBAS-100, which is one-third smaller than that of our previous system (EBAS-50). Samples used in this study were p-type epitaxial 4H-SiC (0001) grown on 8°-off SiC substrate. P^+ ions (total dose; 2.0 x 10^{16} /cm^2, thickness; 350 nm) were implanted into SiC samples at 500°C. The root-mean-square (RMS) of surface roughness is estimated to be 1.23 nm for the sample annealed at 1700°C for 5 minutes, which is much smooth than that of the sample annealed by the conventional rf inductive annealing (5.97 nm). Averaged Rs value of 63.3 ohm/sq. is obtained with the excellent non-uniformity of Rs (+/- 1.4 %) for the diameter of 76 mm.

Impact of Annealing Temperature Ramps on the Electrical Activation of N+ and P+ Co-Implanted SiC Layers: *Philippe Godignon*[1]; [1]CNM Barcelona

We have performed nitrogen and phosphorus (N++P+) co-implantation at room temperature to obtain high n-type carrier concentration regions in SiC. An inductive heating RTA furnace (Jipelec) has been used for the activation annealing. The influence of the annealing temperature ramp parameters, such as rise/decrease temperature ramps and intermediate annealing steps on the dopant activation rate and surface morphology, has been investigated. To suppress surface roughening it is important to use a nitrogen atmosphere during the annealing for temperatures below 1650°C. The reduction of the temperature ramp slope reduces the surface roughness by 50%. The inclusion of a pre-activation annealing step at low temperatures (1300°C) is able to further reduce surface roughness. However, the use of slower ramps or intermediate annealing step during ramp up reduces the free carrier concentration. The faster the ramp up, the higher is the activation rate and the resulting doping. On the other hand, we demonstrate that the inclusion of a post-activation annealing at lower temperatures (1150°C) also reduces significantly the surface roughness. In addition, the use of this post-annealing treatment does not degrade the activation rate nor the carrier Hall mobility. Activation rates close to 100% have been then obtained.

Electrical Transport Properties of CVD Grown Silicon Carbide Nanowires (SiCNWs) for High Sensitivity Sensor Applications: *Sang-Kwon Lee*[1]; Hang-Kyu Sung[2]; Heon-Jin Choi[2]; Seung-Yong Lee[1]; Ji-Eun Park[1]; Nam-Kyu Cho[1]; Ki-Suk Nahm[1]; [1]Chonbuk National University; [2]Yonsei University

Here, we demonstrate the fabrication and the electrical transport properties of single crystalline SiCNWs. In addition, we will also introduce the possibility of SiC nanowires as sensors. The growth of SiCNWs was carried out in chemical vapor deposition (CVD) furnace. Methyltrichlorosilane (MTS, CH_3SiCl_3) was chosen as a source precursor SiC NWs had diameter of <100nm and lengths of several micron. For electrical transport measurements, as-grown SiC NWs were prepared on a highly doped silicon wafer, pre-patterned by a photo-lithography process, with a 400nm thick SiO_2 layer. Source and drain electrodes were defined by e-beam lithography. Prior to the metal deposition (Ti/Au, 40nm/70nm) by thermal evaporation, the native oxide on SiC NW was removed by buffered HF. The estimated mobility of carriers is of 15 cm^2/(Vs) for 0.02 V. It is very low compare to that expected in bulk and/or thin film 3C-SiC. The electrical measurements from nanowire-based FET structure illustrate that SiC NWs are intrinsic n-type semiconductor.

Activation Treatment of Impurities using Hybrid Super RTA Equipment: *Akimasa Kinoshita*[1]; Junji Senzaki[1]; Makoto Katou[1]; Shinsuke Harada[1]; Mitsuo Okamato[1]; Shin-Ichi Nishizawa[1]; Kenji Fukuda[1]; Fukuyoshi Morigasa[1]; Tomoyoshi Endou[1]; Takuo Isii[1]; Teruyuki Yashima[1]; [1]Advanced Industrial Science and Technology

High temperature above 1600º is required to fabricate p-type region with low resistance, but surface morphology is degraded due to desorption of Si from surface at high temperature. RTA is useful to activate impurities doped into SiC and suppresses the increase of surface roughness of SiC substrate, but this RTA equipment with infrared lamps is capable to anneal only small area. Therefore, we have developed the hybrid super RTA (HS-RTA) equipment with infrared and RF induction annealing technique to achieve RTA for large area of 2-inch in diameter with good temperature uniformity. Temperature is elevated from room temperature (RT) to peak temperature for 60 s. The temperature at 1565º is ±10º , and the sheet resistance uniformity is below 10%, which are sufficiently small. As a result, exactly rapid thermal annealing, low sheet resistance of n-type region, temperature distributions in a circular area of 2-inch in diameter were shown.

Novel Polycrystalline SiC Films Containing Nanoscale Through-Pores by Selective APCVD: *Li Chen*[1]; Xiao-An Fu[1]; Christian A. Zorman[1]; Mehran Mehregany[1]; [1]Case Western Reserve University

A selective atmospheric pressure chemical vapor deposition (APCVD) process has been developed to deposit polycrystalline silicon carbide (poly-SiC) thin films containing through-pores measuring 50-70 nm in diameter. Such films are enabling in the development of micro/nano systems because they can be used for structural purposes while at the same time the pores allow fluid access through them. For example, they can be used for on-chip encapsulation of micro/nano-mechanical devices prior to release and fabrication of hollow micro/nano-mechanical elements. The process involves selective deposition of poly-SiC films on patterned SiO2/polysilicon regions on Si substrates using a carbonization-based 3C-SiC growth process. This technique capitalizes on significant differences in the nucleation of poly-SiC on SiO2 and polysilicon surfaces in order to form mechanically-durable and chemically-stable structures, thus offering a simple alternative to nanolithographic patterning and electrochemical etching. This paper will detail the process, results of film characterization, and demonstration of hollow micro/nano-mechanical devices.

Ion Implanted p^+/n Diodes: Post–Implantation Annealing in Silane Ambient in a Cold–Wall, Low–Pressure CVD Reactor: *Fabio Bergamini*[1]; Shailaja P. Rao[2]; Anronella Poggi[1]; Fabrizio Tamarri[1]; Stephen E. Saddow[2]; Roberta Nipoti[1]; [1]CNR - IMM; [2]University of South Florida

Post–implantation annealing in a silane rich ambient has been shown to be a viable technology for avoiding step bunching of SiC surfaces. This work reports on 4H-SiC p^+/n diodes fabricated whereby the p^+ anodes were made by hot ion implantation and post–implantation annealing was performed in a silane rich ambient in a cold–wall, low–pressure CVD reactor. The silane partial pressure was varied so as to achieve a step–bunch free surface for annealing in the temperature range of 1600–1700°C. The annealing time was constant and equal to 30 minutes. The sheet resistance of the implanted and electrically activated layers, as well as the diode forward and reverse current conductions, were studied at room temperature versus post–implantation annealing temperature. For increasing annealing temperature, the implanted layer sheet resistance decreased while the diode conduction improved. The ensemble of the results was congruent with the hypothesis that higher electrical activation corresponded to better electrical current conduction of the p^+/n junction. Moreover they showed the used SiC material was very stable

up to 1700°C. Based on this work we conclude that it is possible to perform post–implantation anneals in a silane ambient resulting in both a high–quality surface morphology as well as excellent p^+/n implanted diode performance which is important for SiC electronic devices requiring implanted layers.

Selectivity and Residual Damage of Colloidal Silica Chemi-Mechanical Polishing of Silicon Carbide: *Joshua R. Grim*[1]; M. Skowronski[1]; W. J. Everson[2]; V. D. Heydemann[2]; [1]Carnegie Mellon University; [2]Pennsylvania State University

The selectivity, material removal rate, and the residual subsurface damage of colloidal silica chemi-mechanical polishing (CMP) of silicon carbide substrates was investigated using atomic force microscopy (AFM) and plan view transmission electron microscopy (TEM). Silica CMP process, in most instances, was selective. In the damage region surrounding remnant scratches, the vertical material removal rate exceeded the planar material removal rate, which resulted in an enhancement of the scratches over the duration of the polishing process. The material removal rate was low about 20 nm / hr. In addition, the selectivity leads to a slow removal of residual subsurface damage from mechanical polishing. The silica CMP polished surface exhibits significant subsurface damage observed by plan view TEM even after prolonged polishing of 16 hours.

Hydrogen-Induced Blistering of SiC: The Role of Post-Implant Multi-Step Annealing Sequences: *George E. Malouf*[1]; Ben Poust[1]; Sumiko Hayashi[1]; Ginga Yoshizawa[1]; Mark Goorsky[1]; [1]University of California, Los Angeles

Hydrogen-exfoliation has become a viable approach to transfer SiC thin-layers onto different substrate materials. However, little attention has been paid to the exfoliation-inducing annealing conditions. To investigate these mechanisms a standard splitting dose of $2.5\times10^{15}H_2^+/cm^2$ at 37 KeV was implanted. Furthermore, a dose of $5\times10^{15}H_2^+/cm^2$ was implanted at 37 KeV, and a co-implantation of $5\times10^{14}B^+/cm^2$ at 160 KeV and $2.5\times10^{15}H_2^+/cm^2$ at 37 KeV were also investigated. The crystalline quality of the as-received SiC was studied by Double-Crystal X-ray topography to investigate the effect of crystalline quality on the blistering profile. The implant and defect profile of the implanted wafer were studied for various conditions with Double-axis X-ray diffraction, and Transmission Electron Microscopy; while surface and blister characterization were studied with Atomic Force Microscopy and Nomarski Optical imaging. It was found that the $5\times10^{15}H_2^+/cm^2$ implant deviates from the expected blistering conditions by blistering after longer annealing times than the $2.5\times10^{15}H_2^+/cm^2$ implant. Two-step annealing was also examined since it presents a means to improve interfacial-bond strength during the low temperature regime and promote more efficient layer exfoliation during the high temperature treatment. Exfoliation was facilitated with a two-step annealing process only if the first temperature was sufficient enough to begin strain relaxation.

WPD1.Switches

4H-SiC High-Power Photoconductive Switches with n^+-GaN Subcontact Layer: *Kaigui Zhu*[1]; Guangming Li[1]; Yong-Tae Moon[2]; Yi Fu[2]; Jacob Leach[2]; Feng Yun[2]; Biswa Ganguly[3]; Dan Johnstone[2]; Hadis Morkoç[2]; [1]Tech Explore, LLC; [2]Virginia Commonwealth University; [3]Air Force Research Laboratory

High power photoconductive semiconductor switching devices were fabricated on 4H semi-insulating SiC. An epitaxial layer of n^+-GaN was grown on SiC and acted as a subcontact layer to improve the ohmic contact. In this way, current crowding was greatly alleviated and therefore the electrical contacts were protected from being damaged or degradation. Moreover, This method led to two orders of magnitude reduction in the on-state resistance, which in turn improved the photocurrent efficiency by two orders of magnitude. The GaN in the channel area outside of the contact region was removed by KOH wet etching. Reactive ion etching (RIE) was also used as a test, but was found to bring degradation because of etching induced damage.

Performance Assessment of 4H-SiC Bipolar Junction Transistors and Insulated Gate Bipolar Transistors: *Santhosh Balachandran*[1]; T. Paul Chow[1]; Anant Agarwal[2]; [1]Rensselaer Polytechnic Institute; [2]Cree Inc.

In this paper we compare and contrast the performance of 4H-SiC based NPN BJTs and N-channel IGBTs and evaluate the usable range of device voltage ratings. Performance indicators such as the forward drop, turn-off times and power dissipation at different operating frequencies are used as the figures of merit to quantify the application range for these devices. These performance indicators have also been determined as a function of breakdown voltage, operating current density and carrier lifetime using analytical models

The Characteristics of the MOSFETs Fabricated on the Trench Sidewalls of Various Faces using 4H-SiC (11-20) Substrates: *Hiroyuki Fujisawa*[1]; [1]Fuji Electric Advanced Technology Co., Ltd.

We investigated the channel mobility on the trench sidewalls with different crystal faces including (1-100), (0-33-8), (0001) and (000-1) using 4H-SiC (11-20) substrates. We used highly-doped n-type 4H-SiC (11-20) face substrates with p-type epitaxial layers ($2x10^{17}cm^{-3}$, 2µm). Nitrogen was implanted to form the source regions. Channel length was 1.5µm. Trenches were formed by RIE with ICP. Using several mask pattern with different off angles from orientation flat, various crystal planes were exposed on sidewalls of trench. Deposited poly-Si was oxidized to make gate oxides (160nm by ellipsometry). Post oxidation anneal in N_2O ambient was carried out to improve SiO_2/SiC interfaces. Ni and Al were used source/drain and Gate metals respectively. The order of drain current of MOSFETs were (0-33-8) > (1-100) > (0001) = (000-1), which corresponds to reference[1]. The maximum effective channel mobility was $42cm^2/Vs$ on (0-33-8) plane, and was comparable to those on planar MOSFETs on (11-20) face ($37cm^2/Vs$). Acknowledgement: The authors would like to thank Prof. Kimoto of Kyoto University for N_2O annealing. [1]T.Hirao, et. al., Mat.Sci.Forum, Vols.389-393(2002) pp.1065-1068.

4H-SiC DMOSFETs with Graphite Capped Implant Activation Anneal: *Jeffrey B. Fedison*[1]; [1]GE Global Research Center

This work demonstrates initial results of 4H-SiC DMOSFET process development utilizing a graphite capping procedure to protect the SiC surface during high-temperature implant activation anneal. In this study we are interested in minimizing roughness in order to ensure negligible impact on the MOS interface quality. The graphite cap is formed by spinning on a uniform layer of photoresist and the oxygen and hydrogen in the resist are then baked away leaving only graphite. Initial results comparing AFM scans of capped and uncapped annealed samples indicate a dramatic reduction in surface roughness from 14.1nm (uncapped samples) to 0.8nm (graphite capped sample). A graphite capped, 1650C, 30 minute implant activation anneal was used in the fabrication of these DMOSFET devices and the gate oxide was thermally grown in N2O. The aluminum p-well activation percentage is estimated to be from 70 to 80% from CV measurements. The devices show a specific on-resistance of 70 $mOhmcm^2$ and blocking voltage ranged from 1400V to 1600V. Higher than expected threshold voltage was measured and further work is on-going to investigate the possible influence of the implant anneal process, implant damage or oxidation process on DMOSFET device characteristics.

Rf and DC Characterization of Self-Aligned L-Band 4H-SiC Static Induction Transistors: *Joseph Neil Merrett*[1]; [1]SemiSouth Laboratories Inc.

Trenched, vertical SiC static induction transistors for L-band power amplification were fabricated with p-n junction gates on conducting n-type 4H-SiC substrates using a self-aligned fabrication process. Total channel periphery per device varied from 0.25 to 1 cm. The self-aligned fabrication process required no critical alignments and allowed for high channel packing densities ranging from 2.9x103 to 5x103 cm/cm^2. The vertical structure and high channel packing density produced devices capable of current densities over 650 A/cm^2 at VDS = 1 V for wider channel devices. The narrowest channel devices had somewhat lower current densities, but were able to block higher voltages with much less gate voltage. For example, a device conducting 450 A/cm^2 at VDS of 1 V blocked over 400 V with only -3 V on the gate. Devices were packaged and small-signal and load-pull measurements were taken. Devices having the narrowest channel design had a small-signal power gain of over 9 dB at around 1.3 GHz. Load-pull measurements of packaged SITs yielded a maximum power gain of ~ 8.2 dB at 1 GHz, VDD = 100 V, and VGS = 1.2 V. Drain efficiency and PAE measurements are planned for the full paper.

SiC Smart Power JFET Technology for High-Temperature Applications: *Igor Sankin*[1]; Volodymyr Bondarenko[2]; Robin Kelley[1]; Jeffrey B. Casady[1]; [1]SemiSouth Laboratories, Inc.; [2]Mississippi State University

Wide bandgap semiconductor materials such as SiC or GaN are very attractive for use in high-power, high-temperature, and/or radiation resistant electronics. Monolithic or hybrid integration of a power transistor and control circuitry in a single or multi-chip wide bandgap power semiconductor module is highly desirable for such applications in order to improve the efficiency and reliability. This paper describes a new monolithic SiC JFET IC technology for high-temperature smart power applications that allows for on-chip integration of control circuitry and normally-off power switch. In order to demonstrate the feasibility of this technology, hybrid logic gates with maximum switching frequency >20MHz and normally-off 900V power switch have been fabricated on alumina substrates using discrete enhanced and depletion mode vertical trench JFETs. Monolithic on-chip implementation of SiC JFET IC technology for high-temperature smart power applications will be discussed in the full paper.

High-Frequency SiC MESFETs with Silicon Dioxide/Silicon Nitride Passivation: *Kevin Matocha*[1]; Ed Kaminsky[1]; Alexei Vertiatchikh[1]; Jeff Casady[2]; [1]GE Global Research; [2]SemiSouth Laboratories, Inc.

4H-SiC MESFETs were fabricated using a bilayer dry thermal oxide/low-pressure chemical vapor deposited (LPCVD) silicon nitride for surface passivation]. The passivation dielectric consists of a 15 nm dry thermal oxide covered by a 45 nm thick LPCVD silicon nitride layer. Devices utilize a recessed-channel architecture with 0.6 micron T-gates. Devices with the bilayer SiO2/SiNx passivation achieved an ft=9.3 GHz and fmax=15.5 GHz (Wg=1.5mm). The device transconductance was 35 mS/mm, drain current

density was 250 mA/mm, and pinchoff voltage was –8V. Devices were load-pull characterized at 3 GHz with a 10% duty cycle and 100 ms repetition rate as shown in Figure 1. Large devices with a 9.6 mm gate-periphery deliver an output power of 43.3 dBm (21.4 W=2.2W/mm) with a PAE of 60% at a gain of 7.8 dB with a Class AB quiescent bias of Ids=100 mA/mm, and Vds=30V.

Fast Switching, 300 – 600 V 4H-SiC VJFETs with Low On-Resistance: *Lin Cheng*[1]; Janna R.B. Casady[1]; Michael S. Mazzola[2]; Igor Sankin[1]; Joseph N. Merrett[1]; Volodymyr Bondarenko[2]; Robin L. Kelley[1]; Jeffery B. Casady[1]; [1]SemiSouth Laboratories, Inc.; [2]Mississippi State University

Intensive research in SiC has shown its great potential to realize high-performance power electronics for high-speed switching applications over traditional Si counterpart. In this work we have demonstrated the operation of 300 – 600 V 4H-SiC VJFETs with 6.6-ns rise time, 7.6-ns fall time, 4.8-ns turn-on and 5.4-ns turn-off delay time at 2.5-A drain current (I_{DS}), which corresponds to a maximum switching frequency of 41 MHz – to our knowledge the fastest ever reported switching of SiC JFETs. At I_{DS} of 12 A, a 19.1 MHz maximum switching frequency has been achieved. Specific on-resistance (R_{sp-on}) in the linear region is 5.58 mΩ·cm² at 2-V gate bias (V_{GS}) with some below 2.3 mΩ·cm² at V_{GS} = 3 V. The drain current density is >1310A/cm² at 10V drain voltage. High-temperature operation of the 4H-SiC VJFETs has also been investigated at temperatures from 25°C to 225°C. Changes in the on-resistance with temperatures are in the range of 0.90~1.33%/°C at zero gate bias and I_{DS} = 50 mA. The threshold voltage becomes more negative with a negative shift of 0.096~0.105%/°C with increasing temperature.

SiC MESFET with a Double Gate Recess: *Per-Ake Nilsson*[1]; Niklas Rorsman[1]; Mattias Südow[1]; Kristoffer Andersson[1]; Herbert Zirath[1]; [1]Chalmers University of Technology

In order to increase the output power and drain efficiency, MESFETs in SiC have been made with a double recess technique. Typical device characteristics of the MESFETs are drain currents of 380mA/mm, breakdown voltages of 80V and fT/fmax of 10/20GHz respectively. These transistors exhibit power densities of 3W/mm\@3GHz in class AB operation and drain efficiencies of 60%. SiC MESFETs often suffer from gate-lag effects that reduce the output power density and efficiency of the devices due to charges on the surface. A way to reduce this effect is to move the current path away from the surface of the device. In this work, we have made SIC MESFETs with a double recess etch in the channel layer in order to accomplish this. The RF power characteristics at 3 GHz of devices of this type were compared to standard devices made on the same wafer. At optimized performance, the drain efficiency of a device with a double recess was 60%, while the efficiency of a standard device was 15%. The output power was 3 W/mm and 1.4 W/mm respectively.

Fabrication of 4H-SiC DiMOSFET by High-Temperature (>1400°C) Rapid Thermal Oxidation and Nitridation using Cold-Wall Oxidation Furnace: *Ryoji Kosugi*[1]; Kenji Suzuki[1]; Kazuto Takao[1]; Yusuke Hayashi[1]; Tsutomu Yatsuo[1]; Kenji Fukuda[1]; Hiromichi Ohashi[1]; Kazuo Arai[1]; [1]AIST

4H-SiC power MOSFETs have been investigated as a candidate for high power switching device applications. On-state resistance of 4H-SiC power MOSFETs, however, is limited due to the high channel resistance. A post-oxidation annealing in nitric oxide (NO) ambient has been succeeded in reduction of the interfacial defects of the SiO_2/4H-SiC and has improved the inversion channel mobility of 4H-SiC MOSFETs. Effects of the nitridation in NO become more pronounced by the treatment at high temperatures. In case of a standard hot-wall oxidation furnace, however, the maximum temperature is restricted around 1200°C due to the general application limit of a quartz reaction tube. Meanwhile, by use of a cold-wall oxidation furnace, high temperature and short time thermal processing becomes possible with quartz reaction tube, and the gas decomposition ($2NO \rightarrow N_2+O_2$) is significantly inhibited. In this study, we have developed a high temperature (>1400°C) rapid thermal oxidation and nitridation processing for use in the gate oxidation of 4H-SiC DiMOSFET(Double-implanted MOSFET) fabrication process. Device size and cell pitch of the fabricated DiMOSFET are 0.16-1mm² and 15-19µm, respectively. Specific on-resistance of the DiMOSFET is 12.5mΩcm² (\@Vg=20V, Vd=1.0V) and the blocking voltage is 950V(\@Vg=0V).

Reduction of On-Resistnce in 4H-SiC Multi-RESURF MOSFETs: *Masato Noborio*[1]; Yuki Negoro[1]; Jun Suda[1]; Tsunenobu Kimoto[1]; [1]Kyoto University

SiC lateral RESURF MOSFETs are attractive for high-voltage power ICs in the next generation. In this study, the authors fabricated multi-RESURF MOSFETs which mean double and buried-p RESURF MOSFETs. Double and buried-p RESURF MOSFETs have the p-region which is placed on the top and at the middle of RESURF region, respectively. Since the RESURF region is depleted from top and bottom pn junctions, a higher RESURF dose can be employed than normal RESURF MOSFETs, leading to a lower on-resistance. The on-resistance (\@E_{OX} = 3 MV/cm) dependences of RESURF dose and channel length exhibit a linear relationship. The increase of RESURF dose and/or the decrease of channel length cause the decrease of on-resistance. The on-resistances of double and buried-p RESURF MOSFETs with a RESURF dose of 1.1×10^{13} cm^{-2} were 38 mΩcm² and 118 mΩcm², respectively. The buried-p RESURF MOSFETs have higher on-resistances than double RESURF MOSFETs. The on-resistance of buried-p RESURF MOSFET may be affected by the resistance of JFET region inside RESURF region. Thus, double RESURF structure is more attractive to realize low on-resistance RESURF MOSFETs.

Characterization of 4H-SiC MOSFETs Formed on the Different Trench Sidewalls: *Hiroshi Nakao*[1]; Hidenori Mikami[1]; Hiroshi Yano[1]; Tomoaki Hatayama[1]; Yukiharu Uraoka[1]; Takashi Fuyuki[1]; [1]Nara Institute of Science and Technology

Characterization of MOSFETs formed on trench sidewalls is important to achieve high performance UMOSFETs. In this paper, 4H-SiC MOSFETs formed on trench sidewalls were fabricated to evaluate basic MOSFET performance. The starting materials were n-type 4H-SiC (000-1) C-face substrate with p-type epilayer. The wafer has 8° off toward [11-20] direction. The trench was formed by ICP-RIE using CF_4/O_2 gases. The taper angle of the trench was 85°. 80nm-thick gate oxide was formed by wet oxidation / wet reoxidation anneal / NO anneal. Though (1-100) and (-1100) face MOSFETs had similar channel mobility, a large difference was found between the (11-20) and (-1-120) faces. The highest channel mobility was 43cm²/Vs for (11-20), and lowest channel mobility was 21cm²/Vs for (-1-120). Due to substrate off-angle, the channel plane of (11-20) MOSFETs was 3º inclined from the primary {11-20} face. On the other hand, the channel plane of (-1-120) MOSFETs was 13º inclined from the primary {11-20} face. This deviation from the primary {11-20} face may result in the poorer performance on (-1-120). (1-100) and (-1100) faces have the same deviation (5º) from the primary {1-100} face because of trench taper. Therefore similar characteristics were obtained on (1-100) and (-1100) MOSFETs.

Low On-Resistance in 4H-SiC RESURF JFETs Fabricated with Dry Process for Implantation Metal Mask: *Takeyoshi Masuda*[1]; Kazuhiro Fujikawa[1]; Kaoru Shibata[1]; Hideto Tamaso[1]; Satoshi Hatsukawa[1]; Hitoki Tokuda[1]; Akihiko Saegusa[1]; Yasuo Namikawa[1]; Hideki Hayashi[1]; [1]Sumitomo Electric Industries, Ltd

4H-SiC JFETs are expected to be applied for high power and high temperature devices. Lateral devices can be processed and mounted more easily than vertical ones. We fabricated 4H-SiC lateral JFETs with a reduced surface field (RESURF) structure, which can prevent the concentration of electric field at the edge of the gate metal. A Ti/W layer was used as an ion implantation mask, so as to decrease the thickness of the mask and to improve an accuracy of the device process. The 4H-SiC RESURF JFET with the gate length (L_G) of 3µm was fabricated, and the specific on-resistance of 6.3mΩcm² was obtained. In this paper, the fabrication process and the electric characteristics of the RESURF JFETs are described. This work was supported in part by the New Energy and Industrial Technology Development Organization (NEDO) of Japan.

High Temperature Characterization of 4H-SiC Bipolar Junction Transistors: *Sumi Krishnaswami*[1]; Anant K. Agarwal[1]; James Richmond[1]; Craig Capell[1]; Sei-Hyung Ryu[1]; John Palmour[1]; Bruce Geil[2]; Dimos Katsis[2]; Charles Scozzie[2]; [1]Cree Inc; [2]Army Research Laboratory

In this paper we report the high temperature characterization of 4H-SiC Bipolar Junction Transistors (BJT). The BJT devices with an active area of 0.0225 cm², show an on-current of 5 A at a forward voltage drop of 1.2V. A common-emitter current gain, as high as 48 was observed at 25°C. The output characteristics were measured at elevated temperatures up to 350°C. The gain initially reduces with temperature due to increase in base acceptor ionization, and then increases above 250°C. At 350°C, a collector current of 5 A is observed at V_{CE} = 7.2 V and I_B = 160 mA with a gain of 42. Current gain as a function of collector current at three temperatures was measured. The measurement was done using a 2 µs base current pulse, while V_{CE} was fixed at 400V. The gain shows a gradual rise at low current densities. A gain of 55 is observed at I_C = 10 A. With further increase in I_C, β decreases due to the effect of surface recombination. Breakdown characteristics show a BV_{CEO} of 1600 V and a BV_{CBO} of 1625 V. More high temperature characterization is in progress. Results will be presented at the time of the conference.

Double Gate 180V-128mA/mm SiC-MESFET for Power Switch Applications: Tournier Dominique[1]; Miquel Vellvehi[1]; *Philippe Godignon*[1]; Xavi Jorda[1]; Jose Millan[1]; [1]CNM-IMB

The use of SiC MESFET in high frequency applications has been attracting much interest in recent years. The potential of SiC MESFETs has been demonstrated on several circuits in the 1-10 GHz frequency range. Although MESFET structures are conventionally used for RF applications, in this paper we report a low voltage (180V) power switch and its current limiting application based on a double gate MESFET structure, showing enhanced forward and blocking capabilities. The reported devices use a thin highly doped p-type layer implanted at high energy as buffer layer. The MESFET fabrication compatibility with Vertical Junction FET (VJFET) devices has been already reported allowing monolithic cascode switch associations. Various layouts have been fabricated, varying gate length; with either a single gate (p-buried layer connected to source) or double gate (first Schottky, and second on the Pburied layer). Gate RESURF field-plate variation has been also

included at the gate electrode. The I(V) electrical characterization validates the double gate configuration benefits. This double gate structure shows a higher gate transconductance than the single gate one. High voltage measurements in conducting mode (180V, 160mA/mm, 30W/mm) confirm the operation of the MESFET as a current limiting device, with excellent gate control capabilities.

The Effect of Temperature on Base Current Gain in Power 4H-SiC BJTs (Physical Analysis): *Pavel Ivanov*[1]; Michael Levinshtein[1]; Anant Agarwal[2]; Sumi Krishnaswami[2]; John Palmour[2]; Bruce Geil[3]; [1]Ioffe Institute; [2]Cree Inc; [3]Army Research Laboratory

1-kV, 30-A 4H-SiC epitaxial emitter npn bipolar junction transistors (BJTs) were tested at elevated temperatures with respect to dependence of base current gain β on collector current I_C. Collector current was varied in a wide range from 150 mA to 40 A. The collector-emitter voltage was fixed at 100 V to provide active operation mode at all collector currents. Maximum room temperature current gain β_{max} = 40 was observed at I_C = 10 A (emitter current density j_E = 1600 A/cm^2) while β_{max} = 32 at 250°C. The measured β-I_C dependencies were theoretically fitted by modelling. Calculations were performed in the frame of the model which takes into account all main processes affecting BJT's current gain: i) recombination in the emitter-base depletion layer, ii) surface recombination, iii) crowding of the emitter current, iv) decrease of the emitter injection coefficient at high-level injection, and v) ionization of acceptor atoms (Al) in the base. A very good agreement between simulation and experiment was observed over the whole current range. The hole diffusion length in the n-emitter, electron diffusion length in the p-base, electron lifetime in the p-base, and velocity of surface recombination were derived from simulations.

Design, Fabrication and Application of 4H-SiC Trenched-and-Implanted Vertical JFETs: *Jian H. Zhao*[1]; Petre Alexandrov[2]; Yuzhu Li[1]; Larry X. Li[2]; Kuang Sheng[1]; Ramon Lebron-Velilla[3]; Ming Su[1]; [1]Rutgers, State University of New Jersey; [2]United Silicon Carbide, Inc.; [3]NASA Glenn Research Center

This paper reports recent progress in the development of a vertical JFET, the purely vertical JFET based on trenched-and-implanted vertical JFET (TI-VJFET) approach that eliminates the need of epitaxial regrowth at middle of device fabrication and the need of a merged lateral JFET to control the vertical JFET. Different structures have been designed to target breakdown voltages ranging from 600V to 1.2kV. Vertical channel width uniformity has been studied, showing the feasibility of achieving below 0.1um variation for reasonably flat wafers of good thickness uniformity. Pitch size of the designs has been reduced compared to early report. Gate trench width has been reduced from 3.8um to 2.3um, aimed at increasing the device current capability. Fabricated device cells have been tested and packaged into multi-cell 30A TI-VJFETs which have been characterized of DC and switching characteristics at room and elevated temperatures. PSpice model for TI-VJFET has been developed and applied to the performance prediction of 60kW SiC power inverter, suggesting very high performance efficiency of SiC TI-VJFET based inverters, up to 97.7% at 200°C junction temperature and 590V bus voltage without using soft-switching scheme. Preliminary experimental demonstration of a PWM-controlled three-phase inverter based on SiC TI-VJFET power board will be reported.

1836 V, 4.7 mWcm^2 High Power 4H-SiC Bipolar Junction Transistor: *Jianhui Zhang*[1]; Jian Wu[2]; Petre Alexandrov[1]; Jian H. Zhao[2]; Ming Su[2]; [1]United Silicon Carbide, Inc.; [2]Rutgers, State University of New Jersey

This paper reports recent progresses in the development of high power 4H-SiC BJTs based on improved device design and fabrication scheme. Near theoretical limit high blocking voltage of VCEO=1,836 V has been achieved for 4H-SiC BJTs based on a drift layer of only 12mm, doped to 6.7x1015cm^{-3}. The collector current measured for a single cell BJT with an active area of 0.61 mm^2 is up to IC=9.87 A (JC=1618 A/cm^2). The collector current is 7.64 A (JC=1252 A/cm^2) at VCE=5.9 V in the saturation region, corresponding to an absolute specific on-resistance (RSP_ON) of 4.7 mO.cm^2. From Vce=2.4 V to Vce= 5.8 V, the BJT has a differential RSP_ON of only 3.9 mO.cm^2. The current gain is about 8.8 at Ic=5.3 A (869 A/cm^2). This 4H-SiC BJT shows a V2/Rsp,on of 717 MW/cm^2, which is the highest value reported to date for high-voltage and high-current SiC BJTs. The SiC BJT also represents the first power BJT of any design that results in a specific on-resistance below 5 mOcm^2.

WPM1.Transition Metal, Rare-Earth Dopants

A Study of V^{3+} and the Vanadium Acceptor Level in Semi-Insulating 6H-SiC: *Wonwoo Lee*[1]; Mary E. Zvanut[1]; [1]University of Alabama, Birmingham

The purpose of this study of semi-insulating (SI) vanadium doped 6H-SiC is twofold. First, we address the source of absorption lines that have been attributed to both an isolated defect and defect complex by performing Fourier transform infrared spectroscopy (FTIR) and electron paramagnetic resonance (EPR) measurements on samples taken from the same wafers. Second, we investigate the vanadium acceptor level in SI 6H-SiC using photo-EPR and optical admittance spectroscopy (OAS). The FTIR and EPR spectra are consistent with the assignment of the 0.60 and 0.62 eV IR absorption lines to isolated V^{3+}. Annealing studies up to 1600ºC support the assignment. The photo-induced EPR measurements reveal identical photo-thresholds for V^{3+} and V^{4+} ions. A peak at 0.8 eV, where the data for the V^{3+} and V^{4+} are anti-symmetric, is thought to represent excitation of an electron from V^{3+} to the conduction band edge. Therefore, the 0.8 eV peak is attributed to the V$^{3+/4+}$ level. The difference between the optically measured value reported here and that measured previously using temperature-dependent techniques is attributed lattice relaxation. We will discuss these results as well as the OAS data to test our assertion.

Luminescence and EPR Characterization of Vanadium Doped Semi-Insulating 4H SiC: *Ekaterina Kalabukhova*[1]; Michail Bulanyi[2]; Sergej Omelchenko[2]; Oleg Khmelenko[2]; Andrey Gorban[2]; Evgenij Mokhov[3]; [1]Institute of Semiconductor Physics, NASU; [2]Dnepropetrovsk National University; [3]N-Crystals, Ltd.

To increase semi-insulating yield and homogeneity of electrical properties in vanadium doped and undoped SiC growth, a clear understanding of impurity and dopant corporation is decisive. Semi-insulating properties in SiC can be obtained by incorporating vanadium or deep defects of intrinsic origin making different compensation regime for all shallow donors and acceptors. In this paper, we report on photoluminescence (PL) and EPR study of several s.-i. 4H SiC samples showing the different compensation regimes due to the presence of V4+ and V3+of different concentration. The samples which contain only V3+ indicates the compensation regime NV~=ND-NA>0 with the Fermi level located in the upper half of the band gap. The presence of V4+ along with V3+ in the other two set of samples indicates the semi-insulating behavior of the samples with compensation regime NV>NA-ND>0. Considering that the samples revealed EPR spectrum of vanadium V3+, position of the Fermi level should be also in the upper half of the band gap and mixed conductivity could be expected. The data obtained prove that the PL and EPR are perspective techniques in determination semi-insulating yield in SiC crystal.

Persistent Photoconductivity in Semi-Insulating 4H-SiC Studied with Electron Paramagnetic Resonance and Optical Admittance Spectroscopy: *Ekaterina Kalabukhova*[1]; Sergej Lukin[1]; Darija Savchenko[1]; Alexander Sitnikov[1]; William Mitchel[2]; Steve Smith[2]; Siegmund Greulich-Weber[3]; [1]Institute of Semiconductor Physics, NASU; [2]AFRL/MLPS; [3]Unversity of Paderborn

The decay kinetics of a persistent photoconductivity (PPC) in undoped semi-insulating 4H-SiC and intercenter charge transfer were studied with EPR, photo-EPR and optical admittance spectroscopy (OAS). A thermally activated charge transfer process that occurs in the dark has been observed. The PPC effect was observed directly in changes in the quality factor of the EPR cavity before and after illumination and by the decay of the OAS signal for deep levels, and indirectly by the excitation and decay of the nitrogen and boron EPR lines that were not observed in the dark before illumination. The decay kinetics of the PPC and photo-induced carrier capture by nitrogen and boron levels were found to follow a streched exponential form. The PPC in the temperature range from 77 to 300K was found to be produced by a thermally induced charge transfer process involving deep trap levels.

Radiotracer-Studies of Rare-Earth Related Deep Band Gap States in Hexagonal Silicon Carbide: *Wolfgang Witthuhn*[1]; [1]Friedrich-Schiller-Universitaet

Here we summarize the present status of our investigations on rare earth related deep levels in 4H- and 6H-SiC with the radiotracer deep-level-transient spectroscopy (DLTS). At present band-gap levels of Erbium (Er), Gadolinium (Gd) and Europium (Eu) have been identified. The SiC- samples were doped with radioactive 160Er isotopes. Based on these radiotracer studies two donor like level of Er are identified: in 4H-SiC with an activation-energy of Ev+0.73(2) eV above the valence band and in 6H-SiC with of Ev+0.78(2) eV, respectively. For the Gd-related levels the SiC-samples were doped with radioactive 149Gd isotopes by a heavy ion nuclear reaction. Hereby three deep levels could be assigned to Gd: one level at Ev+0.94(2) eV above the valence band in 4H-SiC and two levels at Ev+0.45(1) eV and Ev+0.95(2) eV in 6H-SiC. The studies on Gd-levels revealed increasing DLTS peaks, indicating the existence of deep levels of the daughter isotope Eu. This was checked by implantation of radioactive 146Eu and 147Eu isotopes as parent activity. From these studies 5 Eu-related deep band-gap levels are established: in 4H-SiC two levels at Ev+0.86(2) eV and Ec-0.47(2) eV, and in 6H-SiC three levels at Ev+0.88(2) eV, Ec-0.29(2) eV and Ec-0.67(2) eV.

Cathodo- and Photoluminescence Measurements and Thermal Activation of Rare Earth Doped (Tm, Tb, Eu) a-SiC Thin Films Prepared by rf-Sputtering: *Roland Weingärtner*[1]; [1]Pontificia Universidad Católica del Perú

We present comprehensive cathodoluminecence and photoluminescence measurements from thin amorphous SiC films doped with rare earths (RE). The a-SiC films where prepared by rf-sputtering using a nominally undoped SiC-wafer as a target in high purity argon atmosphere (6N, pressure ca. 1.3 mbar). The rare earth doping (Tm, Tb or Eu, concentrations vary between 1 and 3%) was preformed by placing respective RE metal pieces of appropriate size onto

the SiC wafer. The rare earth ion emissions cover the colors blue (Tm) green (Tb) and red (Eu). The optical and related structural properties of the films are correlated by means of transmission electron microscopy (TEM) in combination with cathodoluminescence measurements in a scanning electron microscope. In addition, the corresponding compositions are determined by EDS and EELS. The cathodoluminescence and photoluminescence spectra of the RE3+-ions are recorded in the visible for temperatures between 10K and 300K in the as-grown condition and after annealing treatments in the temperature range from 400K to 1000K in steps of 150K. The anneal-related changes in the emission of the cathodoluminescence spectra and in the microstructure of the films at each annealing step are recorded and different activation models are discussed. Conditions for optimal RE emission are derived.

WPM2.Electrical & Optical Properties III

Microwave Loss Dielectric Characterization of Silicon Carbide Wafers: *Timothy E. Bogart*[1]; David Snyder[1]; William Everson[1]; Rick Gamble[1]; Ed Oslosky[1]; Steve Perini[1]; Eugene Furman[1]; Michael T. Lanagan[1]; [1]Pennsylvania State University

Semi-insulating silicon carbide (SiC) wafers have been developed for use as a substrate for high frequency devices. A nondestructive characterization technique to measure the dielectric properties of SiC wafers at the high frequencies the devices will be operating at is being developed as a method to select SiC wafers that produce the highest yield of working devices. The dielectric loss is measured at approximatly16 GHz in a split microwave cavity using a HP 8510C network analyzer. Initial results show a correlation between the dielectric loss and resistivity, where the resistivity was measured using a Contactless Resistivity Mapping (COREMA). The uniformity of dielectric loss across SiC wafers has been looked at using a split post dielectric resonator cavity fixed at 5.5GHz to measure the dielectric loss at five points on a wafer. There is also a correlation between dielectric loss and temperature seen when measuring the loss in a split cavity at temperatures up to 175°C.

Simple, Calibrated Analysis and Mapping of SiC Wafer Defects by Birefringence Imaging: *Seung Ho Park*[1]; Mark J. Loboda[1]; Michael J. Spaulding[1]; [1]Dow Corning Corp

Optical birefringence imaging of SiC wafers is a legacy method for qualitative evaluation of wafer defects. In order to repeatedly predict the device impact of wafer defects that are detected by birefringence imaging, a calibrated and repeatable test method is required. This paper presents a method to obtain repeatable wafer defect maps from a birefringence imaging system with a built-in calibration/reference scale. Digital processing of the image is performed using tabletop optical scanner and commercial image processing software. From the scanned image, a quantitation strategy is applied to normalize the light intensity (and indirectly the degree of optical polarization rotation) in order to scale the magnitude of the defect. The defects are then be binned by intensity and using a threshold approach, the defects known to deteriorate device parameters can be isolated and mapped. Examples of the analysis provided will include PVT growth, wafering and develop wafer/epi/device correlations.

Low Coherence Fiber Optic Interferometry as Probe of SiC and Wide Band Gap Materials: *Wojtek J. Walecki*[1]; Manuel Santos[1]; Alexander Pravdivtsev[1]; Kevin Lai[1]; Talal Azfar[1]; Ann Koo[1]; [1]FSM

The low coherence optical interferometry has been proven to be an effective tool for characterization of thin and ultra-thin semiconductor Si wafers, and deep etched trenches. In this paper we describe extension of this method to characterization of SiC substrate wafers and structures. We discuss in detail practical and theoretical limitation of the measurement technique. We demonstrate that system is capable of measuring thickness and surface topography both polished and ground surfaces, when providing very small edge exclusion (60 microns for standard system and down to 5 microns for system quipped with microscope). System has static repeatability for the thickness measurement of the order of 0.05 micron on 200-400 micron thick wafers with both smooth surfaces. The theoretical limits of measurement system are discussed in greater detail. Finally we discuss compatibility of proposed technique with stress and subsurface damage measurements using FSM high resolution spectroscopy. [1]W. J. Walecki, V. Souchkov, K. Lai, P. Van, M. Santos, A. Pravdivtsev, S. H. Lau, A. Koo "Novel Noncontact Thickness Metrology for Partially Transparent and Nontransparent Wafers for Backend Semiconductor Manufacturing" Mater. Res. Soc. Symp. Proc. Vol. 829, B9.31.1., (2005).

WPM3.Extended Defects III

Invited

Characterization of SiC Crystals by Using DUV Excitation Raman Scattering Spectroscopy: *Shin-Ichi Nakashima*[1]; Takeshi Mitani[1]; [1]National Institute of Advanced Industrial Science and Technology

Deep ultraviolet (DUV) Raman spectroscopy is a powerful tool for characterizing surface layers of wide gap semiconductors. Raman probing using DUV light which penetrates into nanometer-scaled layers of SiC has enabled us to analyze quantitatively processing-induced defects in the thin surface layers. We have measured DUV Raman spectra of ion implanted and post annealed 4H-SiC, and mechanically polished SiC surface layers. Raman spectra of ion implanted and post annealed SiC have been measured as functions of dose level and annealing temperature. The recovery of the crystallinity and electrical activity of dopants have been evaluated. Segregation of phosphorous was found in heavily dosed species. Damaged surface layers of 4H-SiC, which were mechanically polished with various sized abrasives, were also evaluated from DUV micro-Raman measurements. The width and peak frequency of Raman bands varies with abrasive particle size and these quantities vary with position. The Raman analysis indicates that bandwidth, peak frequency and the degree of the scatter in these quantities can be used as monitors of the polish–induced damage. It is found that localized defects reducing free carrier density remain even after polishing with small sized abrasives.

Open Core Dislocations and Surface Energy of SiC: *Serguei Ivanovich Maximenko*[1]; Pirouz Pirouz[2]; Tangali Sudarshan[1]; [1]University of South Carolina; [2]Case Western Reserve University

Since F. C. Frank's proposal that a dislocation with a Burgers vector larger than a critical value would have an open core, there has been a controversy as to whether micropipes in SiC are examples of such open core screw dislocations. In this work open core dislocations in 4H-SiC material are investigated by AFM. The results are interpreted on the basis of Frank's theory and the extracted surface energy is compared with the results of other researches. The surface energy of SiC is discussed based on its estimation from the critical value of Burgers vector when the dislocations form an open-core.

Characterization of Stacking Fault-Induced Behavior in 4H-SiC p-i-n Diodes: *Brian J. Skromme*[1]; Li Chen[1]; Yu Wang[1]; Mikhail Mikhov[1]; Giby Samson[1]; [1]Arizona State University

Formation of I1 Shockley stacking faults by recombination-enhanced defect glide in 4H-SiC p-i-n diodes subject to high forward current stress is known to cause instabilities in forward voltage. Here, we study this process and the resulting faults using variable-temperature photoluminescence (PL), spectroscopic electroluminescence (EL), spectrally-filtered EL imaging, current-voltage and capacitance-voltage (C-V), and electron beam-induced current (EBIC) imaging measurements. The diodes were made on both c-oriented and a-oriented substrates. We observe increases in forward voltage during stressing for both orientations, accompanied by nucleation and expansion of faults visible in EL imaging. Low temperature PL measurements on degraded diodes of both orientations reveal the same set of exciton peaks. The electronic structure of the faults is therefore confirmed to be the same in both cases. The spectroscopic measurements are compared to self-consistent solutions of the Schrodinger and Poisson equations including polarization charge. Changes in C-V profiles after degradation are attributed to modulation doping effects involving the faults. Dislocations nucleating the faults are bright in EL images but dark in EBIC, confirming that they are sites of enhanced radiative recombination. The diodes were provided by Joe Sumakeris of Cree, Inc., and were produced under ONR contract N00014-02-C-0302, monitored by Harry Dietrich.

Giant Burgers Vector Micropipe-Dislocations in Silicon Carbide by Atomic Force Microscopy: *Etienne Pernot*[1]; Juergen Härtwig[2]; Michel Pons[3]; Roland Madar[1]; [1]LMGP-INPG; [2]ESRF; [3]LTPCM

Recently, some micropipes associated with screw dislocation have been observed by X-ray topography and the strain field around them produced images was similar to those of screw dislocations with very large burgers vector (600 nm). The radius of the hole in the centre of the micropipe is less than 20 microns. This value and the theoretical predictions by Frank (about 7.8 mm) using the Burgers vector magnitude show a large discrepancy. In this paper we present Atomic Force Microscopy experiment around this kind of defects. The Burgers vector magnitude of the screw dislocation and the value of the radius have been measured by this technique. Not only one dislocation, but several have been observed around the micropipe. We conclude that it is in better agreement with the Frank theory.

Characterization of SiC Substrates using X-Ray Rocking Curve Mapping: *Murugesu Yoganathan*[1]; Ejiro Emorhokpor[1]; Thomas Kerr[1]; Avi Gupta[1]; Charles D. Tanner[1]; Ilya Zwieback[1]; [1]II-VI, Inc.

SiC substrates produced at II-VI, Inc. have been characterized using x-ray rocking curve mapping. The rocking curves have been measured in the Ω-scan mode for the (0006) reflection of 6H and the (0004) reflection of 4H SiC substrates. Important information extracted from the rocking curves such as rocking curve broadening (FWHM) and local misorientation (dΩ/dx), have been mapped for the test wafers. In the case when wafer-scale lattice distortion is present due to the warp or plastic deformation, the sample angle (Ω) changes gradually upon scanning with dΩ/dx proportional to the lattice curvature. Multi-peak reflections and/or sharp change in the value of Ω indicate the presence of misoriented grains. Mapping of SiC substrates using

the x-ray technique of rocking curves yields excellent measures of crystal quality that contain very important information on the lattice distortion and sub-grain misorientation. Such maps, aided by the conventional maps of micropipe density, can be employed as tools in the development of GaN and SiC epitaxy and devices, as well as in the analysis and correlation of the device performance.

Comparison Between Measurement Techniques Used for Determination of the Micropipe Density in SiC Substrates: *Ejiro T. Emorhokpor*[1]; Eric Carlson[2]; Jianwei Wan[2]; Arnd-Dietrich Weber[3]; Cem Basceri[4]; Rajinder Sandhu[5]; James Oliver[6]; Frank Burkeen[7]; Anoop Somanchi[7]; Vamsi Velidandla[7]; Fred Orazio[8]; Austin Blew[9]; Mark Goorsky[10]; Michael Dudley[11]; W. M. Vetter[11]; [1]II-VI Incorporated; [2]Dow Corning; [3]SiCrystal AG; [4]INTRINSIC Semiconductor; [5]Northrop Grumman Space Technology; [6]Northrop Grumman Corporation - Electronics Systems; [7]GEM Divisin, KLA-Tencor; [8]VTI Incorporated; [9]Lehighton Electronics; [10]UCLA; [11]SUNYSB

Micropipe density (MPD) is a crucial parameter for silicon carbide (SiC) substrates that determines the quality, stability and yield of the semiconductor devices built on these substrates. Several methods used for the MPD counting are known, however, their reliability and applicability to various types of substrates (e.g. semi-insulating, conducting, etc.) has not been systematically studied. The subject of this paper is a comparative study of various techniques used for MPD counting, accompanied by statistical analysis of the results. The study was initiated by several organizations working in the immediate field of silicon carbide or in closely related fields and included SiC substrate manufacturers, substrate consumers, equipment manufacturers and universities. The study represented a round robin experiment in which MPD was measured on twenty-five SiC wafers of various pedigrees. The values of MPD have been determined using both destructive and non-destructive techniques. The repeatability of each technique is analyzed and compared with that of other techniques.

WPM4.Novel Characterization and Structures III

Brillouin Spectra of Porous p-Type 6H-SiC: G. T. Andrews[1]; A. Polomska[1]; *Maynard Clouter*[1]; Y. Ke[2]; R. P. Devaty[2]; W. J. Choyke[2]; [1]Memorial University; [2]University of Pittsburgh

Brillouin spectra have been recorded for a series of supported films of p-type porous 6H-SiC with a branched morphology and porosities in the range from 30% to 58%. Deposited aluminum coatings of 40 nm thickness were employed to enhance the spectra of the surface acoustic waves and the samples were housed in a controlled atmosphere environment. The spectra were obtained in a back-scattering geometry using a tandem Fabry-Perot spectrometer with a probe wavelength of 532 nm. Complex spectra comprising up to 5 identifiable components were observed in some cases and most of these peaks remain unassigned. The features which most closely approximately Rayleigh-wave behavior are consistent with velocities in the range from 3800 to 3900 m/s.

Columnar Pore Growth in n-Type 6H SiC: Y. Ke[1]; F. Yan[1]; R. P. Devaty[1]; *W. J. Choyke*[1]; [1]University of Pittsburgh

A hybrid columnar and dendritic porous structure has been recently developed in n-type 6H SiC using photoelectrochemical etching with proper control of the applied voltage and current density. The diameter of the formed columnar pores is around 200-500 nm. A self supporting film with this morphology is a promising candidate for protein dialysis. Two etching modes are adopted to make this porous structure: potentiostatic and galvanostaic. Under potentiostatic etching conditions, the columnar pore density is found to be proportional to the material doping. Etchings with galvanostatic control give better aligned and more uniform columnar pores. A linear dependence of the surface pore opening diameter on the applied current density is observed on the porous samples fabricated under galvanostatic mode. We also observed pore diameter expansion for the samples made under constant current conditions. A Possible formation mechanism due to the hole distribution and the HF concentration gradient in the pores is proposed. We suggest that optimal etching conditions are required to make a uniform columnar porous structure.

Fabrication of High Resistive Layers of Porous 4H-SiC by Diffusion of Vanadium: *Malika Akhmedova*[1]; [1]Physical Technical Institute

Semi insulated porous silicon carbide was fabricated by thermo diffusion of vanadium at 1100°C. Typical distribution of vanadium is shown on Fig.1. As you can see from this figure vanadium was not diffused into single crystal part of the SiC. The presence of V on surface of the SiC is connected with a breakage of the crystal structure and surface defects. On the porous part of the SiC vanadium penetrated inside up to 400 nanometer. The character of distribution of vanadium is not traditional. The concentration of V at the surface is ~ 1016 cm^{-3} and it goes down up to 1013 cm^{-3} on depth of 450 nm. The resistivity of doped by V porous SiC was investigated in the temperature range from 300°K to 700°K. The temperature dependence of resistivity of porous layer is shown on fig.2(curve1), the activation energy was - 1,45 ev. The resistivity of porous SiC was 5.1011 Ωcm., higher by 2 order at the same temperature.

Formation, Morphology and Optical Properties of 4H-SiC Nanoparticles Obtained from Nano-Grinding of Bulk Porous SiC Nanostructures: Tetyana Nychyporuk[1]; Vladimir Lysenko[1]; Olivier Marty[2]; *Jean-Marie Bluet*[1]; Gérard Guillot[1]; Daniel Barbier; [1]INSA - LYON; [2]University of Lyon 1

The goal of this work is to obtain 4H-SiC nanocrystallites not embedded in a complex matrix and to investigate their structural and optical properties. First, we report in detail on our original technological approach based on nano-grinding of bulk SiC nanostructures allowing formation of laterally separated SiC nanoparticles on a substrate. The initial porous SiC nanostructures were obtained by anodization of 4H-SiC n+ substrate in HF/Ethanol solution under constant UV illumination. SiC nano-powder obtained after nano-grinding of the porous SiC nanostructures can be then dissolved inethanol. The control of nanoparticle dimensions, its size distribution and surface density is performed by appropriate filtering. The structural properties (crystalline nature and chemical composition) of single porous SiC nanoparticle are also reported. The chemical analysis of the formed nanoparticles confirms their SiC nature. For large single porous SiC nanoparticle (~ 30 nm in diameter) a porous fractal structure is clearly visible. On the other hand, small porous SiC nanoparticles (~ 4 nm in diameter) exhibit a crystalline nature. Finally, particular attention will be paid on an optical study of these porous SiC nanoparticles. Micro-photoluminescence experiments using an UV scanning photoluminescence apparatus developed previously in our laboratory will be performed and presented.

Characterization of Low Stress, Undoped LPCVD Polycrystalline SiC Films for MEMS Applications: Jeremy Dunning[1]; Xiao-An Fu[1]; Mehran Mehregany[1]; *Christian Zorman*[1]; [1]Case Western Reserve University

This paper details the characterization of polycrystalline SiC (poly-SiC) thin films deposited by low pressure chemical vapor deposition. Films were deposited on both Si and SiO2-coated substrates using dichlorosilane (SiH2Cl2) and acetylene (C2H2) as precursor gases. Low residual tensile stress films were deposited at 900°C at a pressure of 2 Torr using SiH2Cl2 and C2H2 (5% in H2) flow rates of 35 sccm and 180 sccm, respectively. XRD analysis of these films indicated a strong (111) 3C-SiC orientation regardless of substrate material. Both resistivity and residual stress gradient decreased as a function of increasing film thickness, reaching values of 1.3 Ω–cm and 17 MPa/µm, respectively in films exceeding 1 µm in thickness. Unintentional nitrogen doping is likely to be responsible for the low resistivity measurements and its concentration in the films was about 1.86 x 1016 /cm^3. Poly-SiC films exhibiting near-zero residual tensile stress, low stress gradient and relatively low resistivity exhibit the favorable properties for MEMS devices.

WPM5.Related Materials III

Optical Characterization of ZnO Materials Grown by Modified Melt Growth Technique: *J. W. Yu*[1]; Zhe Chuan Feng[1]; H. C. Lin[1]; R. Varatharajan[2]; J. Nause[2]; I. Ferguson[3]; W. Lu[4]; W. E. Collins[4]; [1]National Taiwan University; [2]Cermet Inc.; [3]Georgia Institute of Technology; [4]Fisk University

ZnO bulk crystal wafers, undoped and doped with impurities of Ga, Er, Co, Ho, Fe, Mn, and co-doped Mg-Li, have been prepared by a modified melt growth method. The method involves melting and crystallizing materials that have volatile components or have thermodynamic instabilities at or near the material' s melting point at atmospheric pressure. Their wurtzite structures were confirmed. Samples were studied by optical techniques of Raman scattering, Photoluminescence (PL), and UV-visible optical transmission (OT) spectroscopy. Computer analysis has helped in obtaining useful information of the optical properties of these ZnO bulk materials. It is observed that for some impurity dopants, for example, Co and Fe, the electronic energy gap is affected much less than the optical absorption gap. From Raman scattering data, the major E2 mode is located at about 438 cm^{-1}. The PL spectrum from the un-doped ZnO exhibits a dominant band near 3.27 eV. PL spectra for doped ZnO show asymmetric characteristics. In order to distinguish and determine precisely their optical gap, Eog, the differential calculation for all OT spectra in the wavelength region near their optical gaps were performed. The detailed analyses on Raman, PL, and OT results are discussed.

Anisotropic Properties of GaN Studied by Raman Scattering: Hung Chiao Lin[1]; Zhe Chuan Feng[1]; W. S. Li[2]; Z. X. Shen[2]; *W. Lu*[3]; W. E. Collins[3]; [1]National Taiwan University; [2]National University of Singapore; [3]Fisk University

In this study, we report the phonon anisotropy using angular dependent Raman spectroscopy on GaN crystal. The c-axis oriented wurtzite GaN thin film used in this study was about 2 micro meter thick grown on c-plane sapphire substrate by low-pressure metal organic chemical vapor deposition. The polarized Raman scattering spectra were recorded from the cross-section of c-axis oriented GaN films as a function of the angle between the polarization direction of the incident laser with three different polarization configurations, the perpendicular, parallel, and the un-polarized configuration. Both theoretical calculations and experiments have been performed. The Raman intensity variations of the A1(TO), E1(TO) and E2 modes have been shown a sinusoidal tendency with the rotating angle. The theoretical fits are weighed in the

susceptibility contribution and the phase differential of the different vibrating elements for these three modes. The intensity of E2 is quite different to the A1 and E1, because the E2 mode has the same vibrating elements but the A1 and E1 have two types of elements and will have the phase differential contributing to the susceptivity of the polarized angle. Therefore, the phonon anisotropy of the wurtzite GaN crystal could be determined.

Asymmetric Interface Densities on n and p Type GaN MOS Capacitors: *Weixiao Huang*[1]; Tahir Khan[1]; T. Paul Chow[1]; [1]Rensselaer Polytechnic Institute

Both n-type & p-type GaN MOS capacitors were demonstrated utilizing SiO_2 as the gate oxide. Both capacitance and conductance techniques were used to estimate the interface state density. An interface state density of 6×10^{11}/cm^2-eV was estimated at 0.2eV near the conduction band and decreases to 9×10^{9}/cm^2-eV as deeper into the bandgap. A 1.2×10^{13}q/cm^2 total oxide charge near the valence band was estimated. Unlike the symmetric interface state density distribution in Si, an asymmetric interface state density distribution with lower density near the conduction band and higher density near the valence band was extracted as compared to asymmetric distribution with higher density near the conduction band, lower density near the valence band in 4H-SiC. The very small interface state density & fixed charge and the decreasing interface-state density deeper into the bandgap shows the potential of high quality GaN inversion-mode MOSFETs for high voltage and current applications.

WPM6.Surfaces and Interfaces III

Experimental Study of the Formation and Oxidation of the Sm/4H-SiC Surface Alloy: *Morten Kildemo*[1]; Ulrike Grossner[2]; M. Juel[1]; B. Samuelsen[1]; Bengt Gunnar Svensson[2]; Steinar Raaen[1]; [1]University of Trondheim; [2]University of Oslo

Searching for a catalytic promoter for possibly enhanced oxidation and improved interface properties between the oxide and the bulk SiC semiconductor, Sm has been deposited onto the Si- and C-face of 4H-SiC. The formation and oxidation of a Sm/SiC alloy after deposition of 2-3 monolayers [ML] of Sm in UHV on clean reconstructed carbon(000-1) and silicon(0001) terminated SiC surfaces is studied by photoemission (XPS and UPS) and low energy electron diffraction (LEED). The oxygen uptake is initially larger on the SmSiC surface alloy, believed to be mainly due to the lower work function of the alloy. The Si3+ oxidation state dominates, but an additional oxidation state at approximately 1 eV higher binding energy is observed particularly on the oxidised C-face SmSiC surface alloy. A higher ratio of the four fold oxygen configuration is observed from the SmSiC alloys, compared to clean Si-face SiC.

Growth and Investigation of n-AlGaN/p-SiC/n-SiC Heterostructures: *Alexander Lebedev*[1]; [1]A.F. Ioffe Physico-Tekhnical Institute, Russian Academy of Science

Investigated GaN epitaxial layer was grown by hydride vapor phase epitaxy (HVPE) on commercial P+ SiC substrate or on N+ SiC Lely substrate with previously grown by sublimation epitaxy p+ SiC layer. To investigate the electrical characteristics of the n-p heterojunction, mesastructures of 100, 200 and 1500 microns in diameter were fabricated by reactive ion etching. Investigation of electrical characteristics shows enough good quality of grown n-GaN/p-SiC heterojunctions. This shows applicability of this technological combination for producing n-GaN/p-SiC bipolar or FET transistors.

Electronic Structure and Band Alignment at the AlN/SiC Interface: *Jongwoo Choi*[1]; Ragesh Puthenkovilakam[1]; Jane P. Chang[1]; [1]University of California, Los Angeles

We investigate the electronic band structures of bulk AlN, SiC and the AlN/SiC interface as well as band alignment at the interface by first-principles calculations and x-ray photoelectron spectroscopy (XPS). Theoretical calculations are made using plane-wave pseudopotential method within the framework of density functional theory (DFT). The conduction- and valence-band offsets at the AlN/SiC heterojunction determined by DFT are 1.3 and 1.7 eV, respectively, which are in excellent agreement with the experimental values obtained by XPS. These relatively large band offsets are sufficient barriers for electron and hole transport, thus AlN is suitable for a gate dielectric or a lattice matched interfacial layer on SiC.

SiC Based Gas Sensors with Aluminum Oxide Grown by ALCVD: *Ulrike Grossner*[1]; Marc Avice[1]; Bengt Gunnar Svensson[1]; Ola Nilsen[1]; Helmer Fjellvåg[1]; Truls Norby[1]; Ingvild Lorentzen[2]; [1]University of Oslo; [2]NorECs Norwegian Electro Ceramics AS

A layered metal-oxide-semiconductor (MOS) device based on platinum, aluminum oxide, and silicon carbide has been characterised as a gas sensor for hydrogen at temperatures up to 800 K. After oxide growth, MOS capacitors were fabricated. The sample was placed in a ProboStatTM measurement cell for studies of electrical properties at high temperatures and in controlled atmospheres. The electrical characteristics of the MOS capacitors have been determined by capacitance-voltage (CV) measurements. At 800 K, a clear difference in the capacitance-voltage behaviour under oxygen and in 10% H2/N2 atmosphere was found. This behaviour could be reproduced and was stable for several cycles of gas environment change, also at temperatures down to at least 523 K. Furthermore, impedance spectroscopy has been used to deconvolute the equivalent circuit for the sensor under varying bias, temperature, and atmosphere conditions.

A Theoretical Study on the Anomalous Field-Effect Mobility Peak of O-Ta_2Si/4H-SiC High-*k* MOSFETs Measured in Strong Inversion: *Amador Perez-Tomas*[1]; [1]Centre Nacional de Microelectronica - CNM-CSIC

Anomalous high field-effect mobility peak (~50 cm^2/Vs) has been extracted in 4H-SiC (0001) Si face MOSFETs with oxidized Ta_2Si (O-Ta_2Si) high-*k* dielectric (ε_r~20) as gate insulator, in the strong inversion regime. The interface states density (D_{it}) has not been particularly reduced in O-Ta_2Si capacitors. This anomalous mobility enhancement is explained in terms of the Coulomb scattering reduction and quantified using a physical model based on the Lombardi mobility model. The anomalous mobility increase is closely related with the leakage current, and also with the gate breakdown mechanism. The observed interfacial SiO_2 tunnel combined with δ-Ta_2O_5 Poole-Frenkel mechanisms at the O-Ta_2Si gate seems to be a sufficiently low abrupt transition in gate breakdown to obtain an effective passivation of the interface traps. Therefore, the increase of free carriers in the inversion layer induced by the gate leakage diminishes the effect of the interface traps Coulomb scattering.

4:10 PM Coffee Break

WC1.Novel Characterization and Structures

Wednesday, 4:30-6:15pm
September 21, 2005

Room: Allegheny Ballroom I
Location: Westin Pittsburgh

Session Chairs: W. C. Mitchel, U.S. Air Force; E. R. Glaser, Naval Research Laboratory

4:30 PM Invited

Characterization of SiC Wafers by Photoluminescence Mapping: *Michio Tajima*[1]; Eikou Higashi[1]; Toshihiko Hayashi[2]; Hiroyuki Kinoshita[2]; Hiromu Shiomi[2]; [1]Institute of Space and Astronautical Science/JAXA; [2]SiXON, Ltd.

The effectiveness of room-temperature photoluminescence (PL) mapping was demonstrated for nondestructive detection of dislocations and micropipes in SiC wafers. We developed a whole-wafer PL mapping system with a capability of microscopic mapping of the area of interest with a spatial resolution as high as 1 µm, and showed that the PL intensity mapping patterns agree surprisingly well with the etch-pit patterns both on a wafer scale and on a microscopic scale. In the case of high-resistivity 6H SiC wafers, PL spectra were dominated by a broad band with a peak at 1.3 eV, which was traceable to the Si vacancy-related lines at 4.2 K. Large dark spots with bright cores, small dark spots, and dark lines appeared in mapping of the 1.3 eV band, and corresponded closely with micropipes, threading screw dislocations, and edge dislocations forming small angle grain boundaries, respectively. We observed the local enhancement of vanadium-related and Ti-related emissions around dislocations in several 4H and 6H wafers. The present findings lead us to propose that the PL mapping technique can be used as quite an effective and practical tool for the characterization of dislocations and micropipes in SiC wafers with the advantages of high-speed, nondestructiveness and noncontact.

5:00 PM

Long Distance Point Defect Migration in Irradiated SiC Observed by Deep Level Transient Spectroscopy: Giovanni Alfieri[1]; E. V. Monakhov[1]; *Ulrike Grossner*[1]; Bengt Gunnar Svensson[1]; J. W. Steeds[2]; W. Sullivan[2]; [1]University of Oslo; [2]University of Bristol

A method has been devised to investigate by DLTS the properties of the long range migrating defects that are created during near-threshold electron irradiation of SiC. The electron irradiations were performed on nitrogen-doped 4H-SiC epitaxial layers using an energy of 300 keV, just above the silicon displacement threshold. The electron beam was focused to a spot of full-width-half-maximum of ~1µm and irradiations were performed to a dose of 10^23 e/cm^2 at the four corners of a square of side ~300-500µm. The dimensions were based on previous PL-work where the so-called alphabet lines, related to carbon interstitials, were detected at distances exceeding 300µm from the place of irradiation. From this work it was also known that the silicon vacancies remained within the irradiated area. DLTS measurements were performed using nickel Schottky contacts deposited at different distances from the square formed by the four irradiated spots. For distances up to at least 400µm, the so-called Z1/2 level and the two S1 and S2 peaks were detected with concentrations above the background level in undamaged areas. In

accordance with the previous PL results, this provides strong evidence that the formation of the Z- and S-centers involve carbon interstitials.

5:15 PM
In-Diffusion, Trapping and Out-Diffusion of Deuterium in 4H-SiC Substrates: *Margareta K. Linnarsson*[1]; M. S. Janson[1]; U. Forsberg[2]; E. Janzen[2]; [1]KTH, Royal Institute of Technology; [2]Linköping University

Various forms of hydrogen are extensively used in SiC processing. When present, hydrogen may get trapped by donors and acceptors, as well as "dangling bonds" in vacancies and other structural defects. Depending on the stability of these complexes, the trapped hydrogen is released at various temperatures and redistribution may occur during subsequent annealing steps. In this investigation we focus on the incorporation of hydrogen/deuterium in n-, p-type, and semi-insulating 4H-SiC substrates during epitaxial growth at 1600ºC, and its subsequent out-diffusion during high temperature anneals. Deuterium is found to have diffused trough-out all of the substrates during the epitaxial growth, but at a different concentration in the different substrates. No obvious correlation to the doping level can be found for n-type and semi-insulating 4H-SiC substrates. An outdiffusion of the incorporated deuterium can be observed after postgrowth anneals at temperatures starting from 1300ºC, but traces of deuterium can still be found even after anneals at 1700ºC. Since the out-diffusion from the n-type substrates is much slower than that from the similarly doped epitaxial material, we conclude that the deuterium trapped in the substrates is not related to complexing with the nitrogen doping atoms. Instead we propose vacancy related trapping centers.

5:30 PM
Columnar Morphology of Porous Silicon Carbide as a Protein-Permeable Membrane for Biosensors and Other Applications: A. J. Rosenbloom[1]; Y. Ke[2]; *R. P. Devaty*[2]; W. J. Choyke[2]; [1]Carnegie Mellon University; [2]University of Pittsburgh

We are investigating the usefulness of a novel columnar morphology of porous SiC as a protein-permeable membrane for biosensors and other applications. This columnar morphology of porous SiC allows the diffusion of proteins up to at least 80 kD in molecular weight (4 nm hydrodynamic radius). In contrast to commercial polymeric semi-permeable membranes, porous SiC membranes appear to suffer little degradation of permeability after prolonged exposure to concentrated protein solutions. We shall also discuss a model for the diffusion of proteins in porous SiC based on effective medium theory.

5:45 PM
Forming Gas Annealing of the Carbon Pb Center in Oxidized Porous 3C- and 4H-SiC: An EPR Study: Hans Jurgen von Bardeleben[1]; *Jean-Louis Cantin*[2]; [1]CNRS; [2]Universite Paris 6

Thermally grown SiC/SiO2 interfaces are characterized by a high density of interface defects with levels close to the band edges as well as deep centers. Whereas electrical measurements can not identify the microscopic structure of these centers we have recently shown for 3C, 4H and 6H-SiC polytypes that the increased surface area of porous SiC single crystals allows electron paramagnetic resonance spectroscopy to identify one of these centers, which we attributed to the carbon dangling bond center PbC[1,2,3]. One of the characteristics of Pb centers is their passivation by forming gas annealing and we investigated this behaviour for the PbC center at the SiC/SiO2 interface. 3C and 4H-SiC porous layers were oxidized at 1000°C and subsequently treated in forming gas at 400°C. For both polytypes we observe a high degree of passivation (>80%) of the PbC centers for typically some hours treatments. We have equally studied their subsequent depassivation under vacuum annealing. Contrary to the depassivation of Si-Pb centers in Si/SiO2 the depassivation takes place at higher temperatures (850°C/ 1h) in agreement with previous results[4]. [1]H.J.von Bardeleben et al,Materials Science Forum 457-460,1457(2004) [2]J.L.Cantin, et al,Phys.Rev.Lett.92,015502(2004) [3]H.J.von Bardeleben et al,Materials Science Forum 483-485,273(2005)[4]P.J.Macfarlane et al,J.Appl.Phys.88,4122(2000).

6:00 PM
Structural and Electrical Characteristics of Carbon Nanotubes Formed on Silicon Carbide Substrates by Surface Decomposition: *John Boeckl*[1]; William C. Mitchel[1]; Weijie Lu[2]; John Rigueur[2]; [1]Air Force Research Lab; [2]Fisk University

Aligned carbon nanotubes (CNT's) are formed on the surface of silicon carbide (SiC) wafers during high temperature anneals. The exposed 4H SiC surface transforms into CNT's for temperatures in the range of 1400-1700°C and under moderate vacuum conditions (10^{-2} – 10^{-5} torr). The rate of formation on the C-face ($000\bar{1}$) is about three times the rate on the Si-face (0001), but both rates increase with anneal temperature. SEM, TEM and Raman scattering measurements have confirmed the presence of both single-wall and multi-wall CNT's. The carbon source is believed to be residual carbon from the SiC left on the surface after preferential evaporation of Si. CNT formation is believed to be catalized by low concentrations of residual oxygen in the chamber. Patterning of both n-type and semi-insulating substrates with Si_3N_4 masks, prior to annealing, results in CNT-free regions. Subsequent I-V measurements provide insight into the electrical characteristics of the CNT's and the SiC/CNT interface.

WC2.MOSFETs

Wednesday, 4:30-6:15pm
September 21, 2005

Room: Allegheny Ballroom II & III
Location: Westin Pittsburgh

Session Chair: J. Scofield, Wright Patterson Air Force Base Laboratories

4:30 PM Invited
SiC Power MOSFETs – Status, Trends and Challenges: *Dethard Peters*[1]; [1]SiCED

SiC power MOSFETs are very attractive electronic power switches able to compete with silicon power transistors. This paper will discuss whether this statement is true and which market segment offers the best chance for commercialisation. Due to well-known difficulties in achieving adequate channel conductivity a lot of SiC-MOSFET publications focus on the channel mobility. However, for a power MOSFET this is only one important parameter affecting the performance. Other characteristics have to be considered too for an honest evaluation: all aspects of transfer characteristics and blocking capability over standard operation temperature range (e.g. -55°C ... 175°C), safe margin of the gate threshold voltage, handling of gate oxide stress and related reliability issues, capability of paralleling, dynamic stability, body diode characteristics, reproducibility of the fabrication process and device size. Various attempts have been made in recent years in order to address these features. Approaches differ in the use of different crystal orientations and polytypes, accumulation or inversion channel, implanted or epitaxially grown channels and novel oxidation techniques, e.g. Worldwide a trend to the planar DIMOS concept can be observed. Present results are reviewed and complemented by results of the static and dynamic behavior of 1200 V SiC MOSFETs fabricated at SiCED.

5:00 PM
Development of 8 mΩ-cm², 1.8 kV 4H-SiC DMOSFETs: *Sei-Hyung Ryu*[1]; Sumi Krishnaswami[1]; Brett Hull[1]; Bradley Heath[1]; Mrinal Das[1]; James Richmond[1]; Anant Agarwal[1]; John Palmour[1]; James Scofield[2]; [1]Cree, Inc; [2]Air Force Research Laboratory

In this paper, we report on a 1.8 kV 4H-SiC DMOSFET with a specific on-resistance ($R_{on,sp}$) of 8 mΩ-cm². The problem of low MOS channel mobility was alleviated by using a short channel structure with an MOS gate length of 0.5 µm. The devices utilized a 12 µm thick n-type epilayer with a doping concentration of 6 x 10^{15} cm^{-3} for the drift layer. The $R_{on,sp}$ increased to 9.4 mΩ-cm² at 150ºC, which represents only an 18% increase in $R_{on,sp}$. This is due to a small negative shift in threshold voltage (V_t) at elevated temperatures, which reduces the MOS channel resistance at a given gate bias. This cancels out, to an extent, the increase in drift resistance due to reduced bulk electron mobility at elevated temperatures, and results in a relatively temperature insensitive $R_{on,sp}$. The switching characteristics of a 4H-SiC DMOSFET were evaluated using a boost converter configuration. A turn-on delay of 50 ns and a fall time of 34 ns were observed during the turn-on transients, and a turn-off delay of 110 ns and a rise time of 44 ns were measured during the turn-off transient.

5:15 PM
4.3 mΩcm², 1100 V 4H-SiC Implantation and Epitaxial MOSFET: *Shinsuke Harada*[1]; Makoto Kato[1]; Mitsuo Okamoto[1]; Tsutomu Yatsuo[1]; Kenji Fukuda[1]; Kazuo Arai[1]; [1]National Institute of Advanced Industrial Science and Technology

The channel mobility in the SiC MOSFET degrades on the rough surface of the p-well formed by ion implantation. Recently, we have developed a double-epitaxial MOSFET (DEMOSFET), in which the p-well comprises stacked two epitaxially grown p-type layers and n-type region between the p-wells is formed by ion implantation. This device exhibited a low on-resistance of 8.5 mΩcm² with a blocking voltage of 600 V. In this study, to further improve the performance, we newly developed a device structure named implantation and epitaxial MOSFET (IEMOSFET). In this device, the p-well is formed by selective high-concentration p+ implantation and following low-concentration p- epitaxial growth. Fabricated IEMOSFET with a buried channel exhibited superior characteristics than DEMOSFET. The extremely low specific on-resistance of 4.3 mΩcm² was achieved with a blocking voltage of 1100 V. This value is the lowest in the normally-off SiC MOSFETs.

5:30 PM
Investigation of SiO2–SiC Interface by High-Resolution Transmission Electron Microscope: *Sima Dimitrijev*[1]; Jisheng Han[1]; Jin Zou[2]; [1]Griffith University; [2]University of Queensland

Although significant progress has been made in terms of minimizing or passivating the electronically active defects at the SiO2–SiC interface,

in particular by the introduction of interface nitridation., the density of electronically active interface defects remains much higher than in Si devices. In this paper, we investigate the SiO2–SiC interface by the HR TEM technique for the case of oxides grown in both NO and dry O2 atmosphere on 4H SiC substrates. In accordance with the widely reported results in recent years, there is a significant difference in electronic properties of these two types of samples. Consistent with the early AFM-based identification of nanometer-sized interface defects, a recent TEM study identified a significant carbon accumulation in localized areas of non-nitrided SiO2–SiC interfaces. We examined interfaces over several micrometers in distance in both nitrided and non-nitrided samples and we could not find any detectable defects (such as clusters). Moreover, we observed almost atomically smooth SiO2–SiC interface in both nitrided and non-nitrided samples. These experimental results, to be disussed in more detail in the paper, suggest that atomic-level defects are responsible for the electronically active interface traps in oxides grown on high-quality 4H SiC substrates.

5:45 PM

Realization of Large Area Vertical 3C-SiC MOSFET Devices: *Adolf Schoner*[1]; Mietek Bakowski[1]; Per Ericsson[1]; Helena Stromberg[1]; Hiroyuki Nagasawa[2]; Masayuki Abe[2]; [1]Acreo AB; [2]Hoya Advanced Semiconductor Technologies Co. LTD.

Vertical DMOSFET devices with varying size from single unit cell to 3x3 mm^2 containing about 12000 hexagonal and about 8000 square unit cells, respectively, have been realized using 3C-SiC substrate material produced by Hoya Advanced Semiconductor Technologies. A 10 µm epitaxial layer was grown at Acreo prior to implanting the 1 µm deep p-body aluminum box profile with concentration of 1e18 cm^{-3}. The source region was implanted with a 0.3 µm deep box profile of either nitrogen or phosphorus with the concentration of 5e19 cm^{-3}. The source and drain contacts were formed by TiW metallization. Single unit cell vertical DMOSFET devices had blocking capability of 250 V and channel mobilities in the range of 30-40 cm^2/Vs. The density of interface states was in the 1e13 $cm^{-2}eV^{-1}$ range. Both the drain current and the leakage current scale linearly with the device size up to the maximum investigated device size of 1 mm^2. The devices with phosphorus implanted source showed a specific on-resistance of 17 $m\Omega cm^2$ and 34 $m\Omega cm^2$ for 2 µm and 4 µm channel width, respectively. The specific on-resistance values are comparable to the best values demonstrated for 4H-SiC vertical DMOSFET devices.

6:00 PM

Fabrication and Performance of 1.2kV, 12.9mΩcm^2 4H-SiC Epilayer Channel MOSFET: *Yoichiro Tarui*[1]; Tomokatsu Watanabe[1]; Keiko Fujihira[1]; Naruhisa Miura[1]; Yukiyasu Nakao[1]; Masayuki Imaizumi[1]; Hiroaki Sumitani[1]; Tetsuya Takami[1]; Tatsuo Ozeki[1]; Tatsuo Oomori[1]; [1]Mitsubishi Electric Corporation

4H-SiC epilayer channel MOSFETs were fabricated. The MOSFETs have an n- channel epilayer which was designed to be depleted at VG=0V. A MOSFET chip consists of 1405 square MOSFET unit cells (25x25 µm) with an active area of 0.88mm^2. The channel length is 2µm and an adjacent p+ base implantation gap is designed to be 3µm to suppress the electric field in the gate oxide. By the optimization of the channel epilayer and the MOSFET cell structure, the ON-resistivity of 12.9mΩcm^2 is obtained at VG=12V (Eox=2.9MV/cm). By the evaluation of the control MOSFETs with n+ implanted channel, the resistivity of the MOS channel was calculated to be 8 $m\Omega cm^2$. It corresponds to an effective channel mobility of about 20cm^2/Vs at the gate voltage. A normally-OFF operation with an ON/OFF ratio > 105 was obtained and stable avalanche breakdown was obtained at VD > 1.2kV. The ON-resistance (VG=12V) and the breakdown voltage were measured as a function of the ambient temperature. Both the ON-resistance and the breakdown voltage increase slightly with an increase in temperature. This behavior is favorable for high power operation.

RA1.Point Defects II

Thursday, 8:30-10:15am
September 22, 2005

Room: Allegheny Ballroom I
Location: Westin Pittsburgh

Session Chair: M. E. Zvanut, University of Alabama, Birmingham

8:30 AM

Divacancy Model for P6/P7 Centers in 4H- and 6H-SiC: *Nguyen Tien Son*[1]; Takahide Umeda[2]; Junichi Isoya[2]; Adam Gali[3]; Michel Bockstedte[4]; Björn Magnusson[1]; Alexandre Ellison[5]; N. Morishita[6]; Takeshi Ohshima[6]; Hisayoshi Itoh[6]; Erik Janzén[1]; [1]Linköping University; [2]University of Tsukuba; [3]Budapest University of Technology and Economics; [4]Universität Erlangen-Nürnberg; [5]Norstel AB; [6]Japan Atomic Research Institute

The P6/P7 centers (electron spin S=1, C_{3v}/C_{1h} symmetry) are known to be common defects in as-grown and irradiated-and-annealed 6H-SiC. The centers were previously identified as pairs of the C vacancy (V_C) and the C antisite (C_{Si}) in the 2+ charge state $(V_C–C_{Si})^{2+}$ [Th. Lingner et al, Phys. Rev. B 64, 245212 (2001)]. In this work, we use electron paramagnetic resonance to study the hyperfine (hf) structure of P6/P7 centers in both 4H- and 6H-SiC. Our results confirm that the hf structure previously assigned to the interaction with one C antisite is indeed due to the hf interaction with three nearest C neighbours of V_{Si} with C_{1h} symmetry. The obtained hf coupling constants of three nearest C and nine next nearest Si neighbours are in good agreement with the values calculated by super-cell calculations for the divacancies in the neutral charge state $(V_C–V_{Si})^0$, suggesting that the P6/P7 centers are the C_{3v}/C_{1h} configurations of the neutral divacancy. Based on the calculated hf coupling constants, the P6b and P6c centers are identified as the divacancy at the hexagonal-hexagonal and cubic-cubic site, respectively. The electronic structure and the mechanism responsible for the annealing behavior of the P6/P7 signals are discussed.

8:45 AM

Divacancy and Its Identification: Theory: *Adam Gali*[1]; Michel Bockstedte[2]; Ngyen Tien Son[3]; Takahide Umeda[4]; J. Isoya[4]; Erik Janzén[3]; [1]Budapest University of Technology and Economics; [2]Universität Erlangen-Nürnberg; [3]Linköping University; [4]University of Tsukuba

Irradiation creates intrinsic defects such as vacancies, interstitials and antisites in SiC. At different annealing temperature these species become mobile and may even form stable aggregates like the divacancies. Divacancy was predicted to be very stable defect [L. Torpo et al., Phys. Rev. B vol. 65, 085202 (2002).], still the positive identification has been missing so far. Recent electron paramagnetic resonance (EPR) measurements have indicated that the so-called P6/P7 centers are originated from the divacancy in 4H and 6H-SiC [N.T. Son et al., this conference]. *Ab initio* supercell calculations have been carried out to investigate the divacancy in detail. Based on the excellent agreement of the number of different configurations, their symmetry, and the calculated hyperfine constants with the experimental results for the P6/P7 centers we identify the P6/P7-centers with the high spin state of the neutral divacancy in its different configurations. The ground state of the neutral divacancy has S=1 state which is stable in slightly doped p-type material. In n-type SiC the divacancy is negatively charged and excitation is needed to produce the neutral charge state in agreement with the experiment. The annealing behavior of this EPR center can also be explained by earlier theoretical studies.

9:00 AM

Electron Paramagnetic Resonance Study of the SI5 Center in 4H-SiC: *Umeda Takahide*[1]; [1]University of Tsukuba

The SI5 center is known as a major defect in high-purity semi-insulating (HPSI) SiC substrates, Despite its important role in controlling of SI-properties of SiC, the origin of SI5 has not been revealed yet. To study this center in detail, we created SI5 defects with a high concentration in n-type SiC substrates by electron irradiation at 800-850°C. Accordingly, we could reveal complete hyperfine (HF) structures of SI5, which enabled us to discuss the origin of the center. In our irradiated samples, several new EPR centers labeled "HEI1-8" were observed earlier. One of them (HEI4) was found to be identical to SI5. The SI5/HEI4 spectrum showed to have new HF structures that were probably too weak to be detected in HPSI samples. With decreasing temperature, the SI5/HEI4 spectrum changed drastically and its symmetry transformed from C3v to C1h below 50 K. This observation indicates that the high-temperature configuration of SI5 (C3v symmetry) corresponds to a thermal average state. The low-temperature C1h state showed a large HF splitting due to the interaction with two Si atoms. Based on the analysis of the observed HF structures, we will construct an atomic model for the SI5 center.

9:15 AM

Thermal Evolution of Defects in Semi-Insulating 4H SiC: *W. E. Carlos*[1]; E. R. Glaser[1]; B. V. Shanabrook[1]; M. A. Fanton[2]; [1]Naval Research Laboratory; [2]Pennsylvania State University

High temperature anneals were used to study the evolution of several native defects in semi-insulating (SI), ultrahigh purity SiC. We obtain insight into defect origins and chemistry that is not only important in the basic identity and physics of defects but also to understanding stability issues for high temperature growth and processing. Our primary probes are electron paramagnetic resonance (EPR), infrared and visible photoluminescence (PL) and COREMA (Contactless Resistivity Mapping) measurements. In EPR we observe isolated vacancies, the divacancy, a V_C-C_{Si} pair and a new defect that we tentatively identify as V_C-C_{Si}-V_C. The EPR intensity of this defect increases significantly with annealing in all samples. This complex was proposed as a metastable configuration of the divacancy; however, our results indicate it may be the more stable configuration. Three sets of sharp lines referred to as UD1-3 are observed in IRPL and the D_1 lines are observed in the visible. We have previously shown that UD2 is due to the V_C-C_{Si} defect and their annealing behavior further confirms this. We observe UD3 decreasing as UD1 increases, suggesting a relationship between them. We will discuss possible origins of these PL lines along with the interaction of the V_C-C_{Si}-V_C complex with the divacancy.

9:30 AM
A Combined Photoluminescence and Electron Paramagentic Resonance Study of Low Energy Electron Irradiated 4H-SiC: *Wayne Sullivan*[1]; John W. Steeds[1]; Hans Jurgen von Bardeleben[2]; Jean-Louis Cantin[3]; [1]University of Bristol; [2]CNRS; [3]Universite Paris 6

The effect of low energy electron irradiation on n-type 4H SiC has been studied by photoluminescence and electron paramagnetic resonance spectroscopy. We have performed the irradiations at 77K with energies of E=250keV and at E=300keV respectively, i.e. around the silicon displacement threshold of 250keV; the total dose was $5x10^{17}cm^{-2}$ and the dose rate was $\sim5x10^{16}/cm^2h$. Contrary to previous studies[1] the irradiation was performed with low fluences and the samples were homogenously irradiated. By using photoluminescence spectroscopy with either 325nm or 488nm excitation sources we have mainly analyzed the energy dependence of the alphabet lines and the silicon vacancy related lines in the 850-920nm range. The dependence of the defect generation on the electron beam orientation has equally been investigated for the two irradiation directions [0001] and [000-1]. Electron paramagnetic resonance studies have been performed on the same samples. The dominant irradiation induced defect observed for both energies is the spin S=1 EI3 center, which has been recently attributed to the [100] carbon split interstitial (C-C)C in the neutral charge state[2]. [1]J.W.Steeds, G.A.Evans, L.R.Danks, S.Furkert, W.Voegli, M.M.Ismail, F.Carosella, Diam.Rel.Mater 11,1923(2002)[2]T.T.Petrenko et al, J.Phys.Condens.Matter 14,12433(2002).

9:45 AM
Deep Electron and Hole Traps in 6H- and 4H-SiC Bulk Crystals Grown by Halide Chemical Vapor Deposition: *Sung Wook Huh*[1]; Alexander Y. Polyakov[1]; Hun Jae Chung[1]; Saurav Nigam[1]; Marek Skowronski[1]; E. R. Glaser[2]; W. E. Carlos[2]; M. A. Fanton[3]; N. B. Smirnov[4]; [1]Carnegie Mellon University; [2]Naval Research Laboratory; [3]Pennsylvania State University; [4]Institute of Rare Metals

Deep electron and hole traps in a series of high purity 6H- and 4H-SiC single crystals grown by Halide Chemical Vapor Deposition (HCVD) method at various C/Si flow ratios and at temperatures between 2000ºC and 2100ºC were characterized by Low Temperature Photoluminescence, Hall effect, Deep Level Transient Spectroscopy, Minority Carrier Transient Spectroscopy, and thermal admittance spectroscopy techniques. Concentrations of all deep traps were shown to strongly decrease with increased C/Si flow ratio and with increased growth temperature. In HCVD crystals grown under optimized conditions, the density of deep traps was on the order of 1013 cm^{-3} and thus comparable to the concentrations encountered in SiC films grown by standard CVD epitaxy. Possible nature of some of the traps detected in HCVD samples is discussed based on dependence of their density on concentration of nitrogen and boron and on changes of crystal stoichiometry.

10:00 AM
Deep Hole Traps in As-Grown 4H-SiC Epilayers Investigated by Deep Level Transient Spectroscopy: *Katsunori Danno*[1]; Tsunenobu Kimoto[1]; [1]Kyoto University

Deep levels detected in p-type SiC epilayers work as minority carrier (hole) traps in most bipolar devices. Little knowledge is, however, available on deep hole traps in SiC. In this work, we have detected deep hole traps in as-grown p-type 4H-SiC epilayers by deep level transient spectroscopy (DLTS). From DLTS measurements from 350 K to 700 K for Al- and B-doped p-type epilayers, three deep levels (named HK2, HK3 and HK4) can be obtained. Their trap concentrations are in the low 10^{12} cm^{-3} range. The traps are energetically located at E_V + 0.86 eV (HK2), E_V + 1.27 eV (HK3) and E_V + 1.44 eV (HK4). By DLTS under various electric field, these three levels are revealed to have a neutral charge state after hole emission, being donor-like (+/0) traps. Thermal stability of these traps is investigated. Trap concentrations of HK3 and HK4 are reduced to below the detection limit (2×10^{11} cm^{-3}) by annealing at 1300°C for 10 min. The trap HK2 is thermally more stable than HK3 and HK4, and become lower than the detection limit by annealing at 1500°C.

10:15 AM Coffee Break

RA2.Novel Devices and Applications

Thursday, 8:30-9:45am
September 22, 2005

Room: Allegheny Ballroom II & III
Location: Westin Pittsburgh

Session Chair: C. Severt, Wright Patterson Air Force Base Laboratories

8:30 AM Invited
Developments in Hybrid Si-SiC Power Modules: G. Skibinski[1]; [1]Rockwell
Abstract not available.

9:00 AM
High Performance Group-III Nitride LEDs on 4H-SiC Substrates: *John Edmond*[1]; Dave Emerson[1]; Mike Bergmann[1]; Kevin Haberer[1]; Chris Hussell[1]; [1]Cree, Inc.

Group III-nitride layers have been grown via metal-organic vapor phase epitaxy (MOVPE) on single crystal 4H silicon carbide (SiC) substrates and fabricated into light emitting diodes (LEDs). To optimize light extraction efficiency, a flip chip design has been developed. This design utilizes a mirrored p-GaN contact followed by a solder layer for susequently die attaching in a p-down configuration using a eutectic melt process. The SiC substrate is then shaped to accommodate the critical Bragg angle. In the blue region of the visible spectrum, an external quantum efficiency (EQE) of ~55% was achieved at 450-455 nm corresponding to a radiant flux of ~30 mW or ~1 lumen (lm) at 20 mA and 2.9 V. This corresponds to a wall plug efficiency and luminous efficiency of ~52% and ~17 lm/W, respectively. When combined with a cerium YAG phosphor, this device exhibits a radiant flux of ~18 mW at a color temperature of ~5000 K and ~6 lumens. This corresponds to a luminous efficiency of ~100 lm/W, which is considerably more efficient than standard incandescent bulbs (~15 lm/W) and is similar to the very best white fluorescent sources. In the green spectrum, an EQE of ~33% was achieved at 525-530 nm corresponding to a radiant flux of ~16 mW or ~7 lumen at 20 mA and 2.9 V. This corresponds to a wall plug efficiency and luminous efficiency of ~28% and ~120 lm/W, respectively. It is believed that 120 lm/W at 20 mA is a record for any wavelength LED ever produced.

9:15 AM
Ethanol Permeation through Nanoporous Free-Standing 6H-SiC Membranes: *Benjamin Alan Grayson*[1]; John T. Wolan[1]; Y. Ke[2]; R. P. Devaty[2]; W. J. Choyke[2]; [1]University of South Florida; [2]University of Pittsburgh

Free-standing nanoporous 6H-SiC membranes, approximately 60 µm in thickness, were evaluated for ethanol permeation. In order to realize efficient on-chip micro-chemical systems utilizing direct ethanol fuel cells, alcohol cross-over must be minimized. PSiC-Nafion® impregnated membranes showed up to a six-fold decrease in ethanol cross-over as compared to as-received Nafion® 117 films. Additionally, the PSiC-Nafion® membranes demonstrate a linear increase in ethanol permeability with temperature whereas Nafion® 117 films exhibited nonlinearities that suggest concentration dependence on permeation. All studies were conducted in temperatures ranging from 30-80°C using a Crown Glass Side-Bi-Side horizontal diffusion cell with PID temperature control. Flux, permeability, and activation energies of these novel membranes are presented and compared to those calculated from an adapted model developed from literature.

9:30 AM
Radiation Hard Devices Based on SiC: *Evgenia Victorovna Kalinina*[1]; Anatolyi Strel'chuk[1]; Alexandr Lebedev[1]; Nikita Strokan[1]; Alexandr Ivanov[1]; Georgii Kholuyanov[1]; [1]Ioffe Physicotekhnical Institute

SiC initial material, Schottky barriers, high power ion implanted diodes and transistor structures were irradiated with protons, alpha-particles, electrons, neutrons, gamma-ray photons, high power pulsed X-ray radiation as well as Al, Kr and Bi ions. The spectrometry of short range ions was produced using alpha-particles (4.8 - 7.0 MeV). It was revealed that diodes degraded after irradiation with fast neutrons and heavy ions, recovered their rectifying properties at the working temperature up to 500ºC. SiC power diode structures recovery time was determined to be equal to 25 ns under 22 ns high power pulsed X-ray radiation indicating hardness of SiC devices to the high dose rate effects. The transistor structures SiC-based detectors were realized with the signal amplification by a factor of tens under irradiation. It is an equivalent to the signal from epitaxial layers of 300-400 mkm thick. The energy resolution of 0.34 % for SiC-based detectors with Schottky barriers was achieved. The detector characteristics at high temperatures of the diode structures based on SiC ion implanted p+-n junctions will be discussed.

9:45 AM
400 Watt Boost Converter Utilizing Silicon Carbide Power Devices and Operating at 200°C Baseplate Temperature: *Jim Richmond*[1]; Sei-Hyung Ryu[1]; Sumi Krishnaswami[1]; Anant Agarwal[1]; John Palmour[1]; [1]Cree

Silicon Carbide (SiC) Schottky diodes have been commercially available for a number of years. While these diodes have been scaled to higher voltage and higher current, the high temperature operational advantage that Silicon Carbide offers will not be realized at the system level until a Silicon Carbide switching device is available. Both SiC MOSFETs and BJTs are in development but at the present time the BJT is likely to be more reliable at junction temperatures above 200°C. This paper reports on a 400 watt boost converter using a SiC BJT as the switch and a SiC Schottky diode as the output rectifier. The converter was operated with an input voltage of 200 volts DC and an output voltage of 400 volts DC. The efficiency was tested with an output load of 50 watts to 400 watts and at baseplate temperatures of 25°C, 100°C,

150°C and 200°C. The results show the converter efficiency was unchanged as a function of temperature. There are two reasons for this result. The switching losses of the SiC devices are unaffected by temperature and the increase in conduction losses in the BJT were offset by the reduction in conduction losses in the highly de-rated Schottky diode.

10:00 AM
Development of Ultra High Sensitivity UV Silicon Carbide Detectors: *Feng Yan*[1]; Xiaobin Xin[2]; Petre Alexandrov[3]; Carl Stahle[4]; Bing Guan[1]; Jian H. Zhao[2]; [1]Code 553, NASA-GSFC/Muniz; [2]Rutgers University; [3]United Silicon Carbide; [4]553, Detector System Branch, NASA-GSFC

A variety of silicon carbide (SiC) detectors have been developed to study the sensitivity of SiC ultraviolet (UV) detectors, including Schottky photodiodes, p-i-n photodiodes, avalanche photodiodes (APDs), and single photon-counting APDs. Due to the very wide bandgap and thus extremely low leakage current, SiC photo-detectors showed excellent sensitivity. The specific detectivity, D*, of SiC photodiodes are orders of magnitude higher than that of their competitors, such as Si photodiodes, and comparable to the D* of photomultiplier tubes (PMTs). To pursue the ultimate detection sensitivity, SiC APDs and single photon-counting avalanche diodes (SPADs) have also been fabricated. By operating the SiC APDs at a linear mode gain over 106, SPADs in UV have been demonstrated. SiC UV detectors have great potential for use in solar blind UV detection and biosensing. Moreover, SiC detectors have excellent radiation hardness and high temperature tolerance which makes them ideal for extreme environment applications such as in space or on the surface of the Moon or Mars.

10:15 AM Coffee Break

RB1.EPI III: Homoepitaxy, Patterned Growth

Thursday, 10:45am-12:25pm
September 22, 2005

Room: Allegheny Ballroom I
Location: Westin Pittsburgh

Session Chair: A. Burk, Cree, Inc.; R. Davis, Carnegie Mellon University

10:45 AM Invited
Recent Progress of SiC Hot-Wall Epitaxy and Its Modeling: *Shin-Ichi Nishizawa*[1]; Michel Pons[2]; [1]National Institute of Advanced Industrial Science and Technology; [2]Institut National Polytechnique de Grenoble

From the engineering point of view, SiC hot-wall epitaxy is very important process in SiC semiconductor processes. There are lots of experimental reports on SiC hot-wall epitaxy. They discussed the growth rate, surface morphology, doping concentration, etc. Recently, the effect of face polarity is also made clear. However, there are problems remain to be solved. Each report mentioned the particular results that strongly depend on the experimental conditions and reactor design. In addition, the discussion with inlet condition such as source gas C/S ratio, not the depositing surface condition, leads to the confusion. In order to understand and try to optimize and design the how-wall CVD reactor, numerical approach attempted. The authors have tried to make it clear that depositing surface condition might be a universal parameter of SiC CVD, and the numerical simulation could predict the growth rate, surface morphology and doping concentration with taking the depositing surface condition. In this presentation, at first, the recent progress of SiC hot-wall epitaxy in experiment is summarized. Then, the present status of its numerical modeling is explained.

11:15 AM
Properties of Thick n- and p-Type Epitaxial Layers Grown by Hot-Wall CVD on Off- and On-Axis Substrates: *Jawad Ul Hassan*[1]; Peder Bergman[1]; Christer Hallin[1]; Erik Janzén[1]; [1]Linköping University

Hot-Wall CVD epitaxy was used to grow thick layers of p- and n-type doping on both off- and on-axis 4H-SiC substrates. The layers have been characterized using electrical, optical and structural techniques to determine the state-of-the-art properties of these layers. The carrier lifetime measured by optical techniques ranged from 0.6 to 1 µsec, strongly related to the substrate quality. P-type epitaxial layers grown on both n-type and p-type substrates showed carrier lifetime close to that for n-type layers. No distinct difference between the lifetime for the layer grown on n-type and p-type substrate was observed. To investigate if the growth conditions and material properties are changing during the long growth time a strip from the wafer was polished at small angle resulting in uniformly varying thickness of 20µm on one side and 90µm on other was investigated by structural, optical, electrical and simulations techniques to obtain depth information on the material properties. The properties of thick layers grown on on-axis C-face substrates are found to have similar electrical and optical properties as for the layers grown on off-axis substrates. The polytype stability and evolution of epitaxial defects as well as the surface morphology is however different.

11:30 AM
Epitaxial Growth of 4H-SiC on 4°Off-Axis (0001) and (000-1) Substrates by Hot-Wall CVD: *Keiji Wada*[1]; Tsunenobu Kimoto[1]; Kimito Nishikawa[2]; Hiroyuki Matsunami[3]; [1]Kyoto University; [2]Ecotron Co., Ltd.; [3]JST Plaza Kyoto

We have investigated homoepitaxial growth on 4°off-axis 4H-SiC(0001) and (000-1) under various growth conditions using horizontal hot-wall CVD. Smooth surface morphology and reduction of background doping concentration have been achieved on 4°off-axis (000-1) by growing at high temperature and at low pressure growth. In comparison with (000-1), epitaxial growth on 4°off-axis (0001) has been difficult because of strong step bunching. A smooth epi-layer with a RMS roughness of 0.46 nm and background doping concentration of $4.4x10^{14}$ cm^{-3} can be grown on 4°off-axis (000-1).

11:45 AM
Experimental Observations of Extended Growth of 4H-SiC Webbed Cantilevers: *Andrew J. Trunek*[1]; Philip G. Neudeck[2]; David J. Spry[1]; [1]NASA-OAI; [2]NASA

We report on recent observations of homoepitaxially grown silicon carbide (SiC) cantilevers on commercial on-axis mesa patterned substrates. This worked focused on closed mesa shapes with hollow interiors. Step flow growth was used to laterally expand the cantilevers emanating from the tops of mesas to increase the useable area of dislocation-free SiC. Mesa shapes were modified to significantly increase the ratio of dislocation-free cantilevers to pregrowth mesa area. The expanded dislocation-free cantilevers represent approximately a six-fold increase in usable area. When cantilevers coalesce to a single point and substrate axial screw dislocations reside within the hollow region of the pregrowth mesa a new step source can form at the coalescence point enabling continued homoepitaxial growth in the <0001> direction. This enabled cantilever thickness to be increased to ~7µm's in thickness without additional dislocations being observed. Molten KOH etching was employed to decorate defects. When growth in the trench region rises to come into contact with the laterally expanding cantilever, defects were observed to form in the contact areas, the remaining portion of the cantilever remains free of dislocations. Eliminating or suppressing trench growth should enable further expansion of the cantilevers with no new dislocations being formed.

12:00 PM
Silicon Carbide Migration Enhanced Embedded Epitaxial (ME3) Growth Technology: *Yuuichi Takeuchi*[1]; Mitsuhiro Kataoka[1]; Tsunenobu Kimoto[2]; Hiroyuki Matsunami[3]; Rajesh Kumar Malhan[1]; [1]Denso Corporation; [2]Kyoto University; [3]Japan Science and Technology Agency

In this work, we have developed an innovative epitaxial growth process and named "Migration Enhanced Embedded Epitaxial" (ME3) growth process. We investigated the growth behavior inside the narrow trenches formed on 4H-SiC. Stripe pattern deep trenches of aspect ratio about 2 (depth: 3.0um; width: 1.5um) were formed by ICP dry etching process. A hot-wall CVD reactor was used in this embedded epitaxial growth study and growth temperature, which is the key parameter of the ME3 process, was varied from 1500 to 1650°C. Non-doped n-type epitaxial layers were grown at C/Si ratio from 0.8 to 2.0. It was found that the epitaxial growth at the bottom of trenches is greatly enhanced compare to growth on the sidewalls under the condition of higher growth temperature of 1650°C and lower C/Si ratio. This is attributed to the large surface diffusion length of reactant species mainly due to the higher growth temperature. In addition, it was found that this high temperature ME3 growth process is not influenced by the crystal-orientation. It seems that the ME3 growth process doesn't follow the basic orthodox step-flow mechanism. The pn junctions formed on either oriented stripe geometry shows good electrical characteristics.

RB2.Device Reliability and Characterisation

Thursday, 10:45am-12:40pm
September 22, 2005

Room: Allegheny Ballrm II & III
Location: Westin Pittsburgh

Session Chair: C. Scozzie, Army Research Laboratory

10:45 AM Invited
Evolution of Drift-Free, High Power 4H-SiC PiN Diodes: *Mrinal K. Das*[1]; [1]Cree, Inc.

The PiN diode is an attractive device to exploit the high power material advantages of 4H-SiC. The combination of high critical field and adequate minority carrier lifetime has enabled up to 20 kV devices with current ratings as high as 50 A. Furthermore, these devices exhibit fast switching with less reverse recovery charge than commercially available Si PiN diodes. The path to commercialization of the 4H-SiC PiN diode technology, however, has been hampered by a fundamental problem with the forward voltage stability resulting from stacking fault growth emanating from basal plane dislocations (BPD). In this contribution, we highlight the progress toward producing stable high power devices with sufficient yield to promote commercial interest. Two independent processes, LBPD1 and LBPD2, have been shown to be effective in reducing the BPD density and enhancing the forward voltage stability while being compatible with conventional power device fabrication. Applying the LBPD1 and LBPD2 processes to 10 kV, 50 A 4H-SiC PiN diode technology has resulted in a dramatic improvement in the total device yield (forward, reverse, and forward drift yields) from 0% to >20%.

11:15 AM
Influence of Basal Plane Dislocation Induced Stacking Faults on the Current Gain in SiC BJTs: *Anant K. Agarwal*[1]; Sumi Krishnaswami[1]; James Richmond[1]; Craig Capell[1]; Sei-Hyung Ryu[1]; John Palmour[1]; Bruce Geil[2]; Dimos Katsis[2]; Charles Scozzie[2]; [1]Cree Inc.; [2]Army Research Laboratory

The reduction in the current gain of SiC BJTs has been observed after operating the devices for a few hours. In addition, the on-resistance of the BJT and the slope of the output characteristics increase after operation. This phenomenon can be explained on the basis of what has been previously observed in SiC pn junction diodes. Basically, an increase in the forward voltage (Vf) of SiC PiN diodes was reported. This Vf increase was explained by the growth of stacking faults from certain basal plane dislocations within the drift layer of the PiN diode. The energy for this expansion of the stacking fault comes from the electron-hole recombination in the conductivity modulated drift layer. It is speculated that a similar phenomenon is taking place in the SiC BJT device. The base of the transistor is flooded with electron-hole pairs during operation. The recombination of electron-hole pairs in the base gives rise to stacking faults which can grow in the base and extend into the collector region. These stacking faults reduce the life-time of the minority carriers locally in the base, which in turn results in reduced current gain.

11:30 AM
A Study on the Reliability and Stability of High Voltage 4H-SiC MOSFET Devices: *Sumi Krishnaswami*[1]; Sei-Hyung Ryu[1]; Mrinal Das[1]; Brett Hull[1]; Bradley Heath[1]; Anant Agarwal[1]; John Palmour[1]; Bruce Geil[2]; Aivars Lelis[2]; Charles Scozzie[2]; [1]Cree Inc; [2]Army Research Laboratory

This paper presents the reliability and stability of MOS-based 4H-SiC devices. In a 4H-SiC vertical MOSFET structure, there is concern about MOS reliability under the following two conditions: (1) on-state of the MOSFET, in which high electric field exists in the oxide overlapping the n+ source regions due to the application of high positive gate bias, and (2) off-state in which the oxide in the JFET region and in the edge-termination regions are stressed under high electric field. Therefore for a reliable operation, the power MOSFET requires a high performance MOS channel and a reliable gate dielectric. Reliability measurements of 4H-SiC DMOSFETs were performed using the Time Dependent Dielectric Breakdown technique at 175°C. The oxide lifetime is plotted as a function of the electric field. The results show the projected oxide lifetime to be >100 years at a operating field of ~3 MV/cm. In addition, reliability of 2kV DMOSFETs were studied by stressing the gate with a constant gate bias of +15 V at a temperature of 175°C, and monitoring the forward I-V characteristics and threshold voltage for device stability. Preliminary measurements show very little variation between the pre-stress and post-stress conditions up to 250 hours of operation at 175°C.

11:45 AM
Measurements of Breakdown Field and Forward Current Stability in 3C-SiC pn Junction Diodes Grown on Step-Free 4H-SiC Mesas: *Philip G. Neudeck*[1]; David J. Spry[2]; Andrew J. Trunek[2]; [1]NASA; [2]OAI

Recent advancements in cubic-SiC crystal growth and MOSFET properties have renewed interest in the 3C polytype for realizing beneficial electronics. Step-free surface heteroepitaxy has enabled dislocation-free layers of 3C-SiC to be realized on top of small device-sized mesas arrayed across on-axis 4H-SiC wafers. This paper reports on fabrication and electrical characterization of 3C-SiC p^+n junction diodes grown on step-free 4H-SiC mesas. Diodes with n-blocking-layer dopings ranging from ~ 2×10^{16} cm^{-3} to ~ 1×10^{18} cm^{-3} were fabricated and tested. No optimization of junction edge termination or ohmic contacts was employed. Room temperature reverse characteristics of the best devices show excellent low-leakage behavior (at or near the measurement noise floor, below previous 3C-SiC devices produced by other growth techniques) until the onset of a sharp (> 50-fold current increase per volt) breakdown knee. The resulting estimated breakdown field of 3C-SiC is at least twice the breakdown field of silicon, but is only around half the breakdown field of <0001> 4H-SiC for the doping range studied. Initial forward current stressing of two diodes at 100 A/cm^2 for over 30 hours yielded less than 50 mV change in forward voltage drop, though much further testing remains to be carried out.

12:00 PM
Advances in Two-Dimensional Dopant Profiling and Imaging of 4H-SiC Devices: *Marco Buzzo*[1]; [1]Infineon Technologies

Dopant profiling and 2D imaging of device cross-sections have a strategic relevance for the development and for the failure analysis of new devices based on silicon carbide. This work gives an insight into the latest advances in dopant profiling and imaging of silicon carbide devices by the use of scanning electron and scanning probe microscopy techniques. A commercial Schottky diode has been characterized by Scanning Capacitance Microscopy and by Secondary Electron potential contrast. Both techniques provided useful contrast information between differently doped regions and allowed to delineate the electrical junction consistently with values obtained by device simulation. Furthermore, a qualitative technique is demonstrated, which enables to image the contrast arising from the different hardness of differently doped regions by the combination of mechanical-chemical etching with Atomic Force Microscopy. Secondary Electron potential contrast emerged as the most powerful and accurate technique for dopant profiling and junction delineation in Silicon Carbide.

12:15 PM
Bias Stress-Induced Threshold-Voltage Instability of SiC MOSFETs: *Aivars Lelis*[1]; Dan Habersat[1]; Gabriel Lopez[1]; James McGarrity[2]; F. Barry McLean[2]; Neil Goldsman[3]; [1]Army Research Laboratory; [2]Berkley Associates; [3]University of Maryland

We have observed instability in the threshold voltage of SiC MOSFETs due to gate-bias stressing. This effect has routinely been observed in all 4H and 6H SiC MOSFETs from three different manufacturers—even at room temperature. A positive-bias stress, applying about a 2-MV/cm field across the gate oxide, for 3 minutes followed by a negative-bias stress for another 3 minutes typically results in a shift of the I_D-V_{GS} characteristic in the range of 0.25 to 0.5 V, and is repeatable. We speculate that this effect is due to the presence of a large number of near-interfacial oxide traps that presumably lie in the oxide transition region that extends several tens of Å in from the SiC interface, caused by the presence of C and strained SiO_2. This effect is consistent with charge tunneling in and out of near-interfacial oxide traps, which in irradiated Si has been attributed to border traps. Also consistent with charge tunneling is the observed linear increase in the magnitude of the SiC V_T instability with log (t).

Lunch

Thursday, 12:40-1:50pm
September 22, 2005

Room: Spirit of Pittsburgh
Location: Convention Center

RP.Thursday Poster Sessions

Thursday, 1:50-4:10pm
September 22, 2005

Room: Spirit of Pittsburgh Foyer
Location: Convention Center

RPP1.Contact Processing

Evaluation of Schottky Barrier Height of Al, Ti, Au, and Ni Contacts to 3C-SiC: *Masataka Satoh*[1]; Hiroshi Matsuo[1]; [1]Hosei University

We investigated that the Schottoky barrier height (SBH) of Al, Ti, Au, and Ni contacts to n- and p-type 3C-SiC. The samples used in the present study were n- and p-type 3C-SiC epitaxial layer grown on n^+-type 3C-SiC substrates, which was provided from Hoya Advanced Semiconductor Technologies. The net donor and acceptor concentration was 1.0 x 10^{16} and 4.0 x 10^{16} /cm^3, respectively. Al, Ti, Au, and Ni electrodes were deposited on the cleaned 3C-SiC using E-gun evaporation in a vacuum of 2 x 10^{-5} Pa. The thickness of Al, Ti, Au, and Ni were 300, 100, 300, 100 nm, respectively. All metal contacts to n- and p-type 3C-SiC show the rectifing I-V characteristics except for Al contact to n-type 3C-SiC. Only Al contact to n-type 3C-SiC shows the ohmic

characteristics. As the work function of metal is increased from 4.3 to 5.2 eV, SBH for n-type 3C-SiC is increased from 0.4 to 0.7 eV and SBH for p-type 3C-SiC is decreased from 2.2 to 1.8 eV. The small change of SBH for 3C-SiC may be correlated to the crystal orientation and the defects on the surface of 3C-SiC.

Fabrication of 4H-SiC Floating Junction Schottky Barrier Diodes (Super-SBDs) and Their Electrical Properties: *Ota Chiharu*[1]; [1]Toshiba Corporation

4H-SiC floating junction Schottky barrier diodes (Super-SBDs) were fabricated for the first time. It was found that their properties were close to the theoretical limitation due to the trade-off between specific on-state resistance and breakdown voltage of 4H SiC-unipolar devices than any other research reported so far. The Super-SBD has a p-type floating layer in an n-type drift layer. The specific on-state resistance of typical Super-SBDs is nearly equal to those of conventional SBDs which have no p-type floating layer, whereas the breakdown voltages of Super-SBDs were higher than those of conventional SBDs. The properties of Super-SBDs in this study improved the trade-off between specific on-state resistance and breakdown voltage significantly.

Ni Graphite Intercalated Compounds in Ohmic Contact Formation on SiC: *Weijie Lu*[1]; J. A. Michel[2]; C. M. Lukehart[2]; W. E. Collins[1]; W. C. Mitchel[3]; [1]Fisk University; [2]Vanderbilt University; [3]Air Force Research Laboratory

Ohmic contacts are a necessary part of every electronic device. Ohmic contacts on SiC have been investigated extensively in the past decade and various materials, including metals, alloys, silicides, carbides, and borides, have been examined. However, the mechanism for ohmic contact formation has been a troublesome issue. The interfacial structures at the atomic scale necessary to form ohmic contacts have not been understood. Our previous results have shown that carbon can form ohmic contacts on SiC after thermal annealing, and that an interfacial carbon layer between Ni and the SiC improves the contacts significantly. In this study, we have investigated the interactions between Ni and carbon, and ohmic contact formation on SiC using x-ray diffraction (XRD) and Raman spectroscopy. After annealing, ohmic behavior was observed and Ni graphite intercalated compounds (GICs) were found on Ni/C/SiC structures. Unlike conventional graphite intercalated compounds, the Ni atoms substitute for carbon atoms in the graphitic networks in these Ni-GICs. XRD peaks at 21.6° due to the Ni graphitic intercalation compound (Ni-GIC) and at 26.3° due to graphite have been observed. The distance between graphitic sheets is 0.403nm in the Ni graphite intercalated compounds, where as it is ~20% larger in the graphite.

Structural Properties of Titanium-Nickel Films on Silicon Carbide Following High Temperature Annealing: *Konstantin Vassilevski*[1]; Irina Nikitina[1]; Alton Horsfall[1]; Nick G. Wright[1]; Mark Johnson[2]; Rajesh Malhan[3]; Takeo Yamamoto[3]; [1]University of Newcastle; [2]University of Sheffield; [3]Denso Corporation

The structural properties of Ni/Ti films deposited on 4H-SiC and annealed at temperatures from 800 to 1040°C have been studied. Samples were prepared by thermal deposition of metals on commercial 4H-SiC wafers followed by high temperature treatment. Films with three different metal deposition sequences were investigated: (a) Ti(100 nm) covered by Ni(50 nm); (b) Ti(4 nm) covered by Ni(50 nm) and Ti(100 nm); and (c) Ti(4 nm) covered by Ni(150 nm). High temperature annealing was performed in vacuum at 800, 925 and 1040°C for a period of 800 seconds. X-ray diffraction, Auger electron spectroscopy and transmission electron microscopy were used for characterization. A distinct spatial separation of nickel silicide and titanium carbide layers was observed in all samples, including sample (c) which had a very thin initial titanium layer. It was discovered that the final distribution of the products of solid state reaction in samples (a) and (b) was independent of the order of deposition of the initial nickel and titanium films. In both samples, a thin nickel layer on the interface between the contact film and the silicon carbide was detected. This thin Ni layer was found to be covered by clearly separated titanium carbide and nickel silicide layers.

Nanoscale Depth-Resolved Spectroscopy of TiAl and NiTiAl Ohmic Contacts to p-Type 4H-SiC: *Min Gao*[1]; S. Tumakha[1]; Leonard Brillson[1]; S. Tsukimoto[2]; M. Murakami[2]; [1]Ohio State University; [2]Kyoto University

We have used depth-resolved cathodoluminescence and Auger electron spectroscopies, DRCLS and AES, respectively, to probe the electronic structure and the composition of TiAl and NiTiAl Ohmic contacts to p-type SiC on a nanometer scale. A continuous Ti-Si-C compound layer with deficient Ti near the interface was observed in the TiAl contact. DRCLS revealed a 1.9 eV sub-band gap transition localized at depths corresponding only to the reaction layer. Another unique sub-band gap emission was present at 2.8 eV in this structure, suggesting the formation of point defects in the near-interface SiC. The NiTiAl contact consisted mainly of Ni silicide and Ti carbide, and considerable amounts of O, Ni and Al were incorporated at the contact region compared to the TiAl contact. DRCLS showed qualitatively a transition at ~ 1.6 eV that persisted beyond the metal-SiC interface. These results show that the different interfacial reactions during the formation of the TiAl and NiTiAl ohmic contacts introduced different interfacial sates in the near-interface SiC. In general, correlation between these interfacial states with the specific local structural/compositional configuration provide strong evidence that both an electrically-active interfacial compound and point defects play a role in Ohmic contact formation.

Ohmic Contact for C-Face N-Type 4H-SiC with Reduced Graphite Precipitation: *Yusuke Maeyama*[1]; [1]Shindengen

Annealed Ni is most conventional as ohmic contact electrode for N-type SiC. However, graphite precipitates by the reaction of Ni and SiC, and it causes electrode peeling because of the brittleness. Almost study was focused on Si-face SiC. The study on C-face 4H-SiC is also important from the view point of vertical devices. We investigated Ni, monel/Si multilayer, Ni/Ti/Ni multilayer and Mo electrodes for C-face N-type 4H-SiC. Although the contact resistivity of Ni is lowest as 2E-5Ocm^2, large amount of graphite precipitates in electrode. Monel/Si achieves a balance between low resistivity (2E-4Ocm^2) and decreasing graphite to C-face as well as Si-Face, because monel/Si electrode forms silicide without reaction between the metal and SiC.

Ohmic Contacts on p-Type SiC Using Al/C Films: *Weijie Lu*[1]; G. R. Landis[2]; W. E. Collins[1]; W. C. Mitchel[3]; [1]Fisk University; [2]University of Dayton Research Institute; [3]Air Force Research Laboratory

It is well known that ohmic contacts on p-type SiC are more difficult to form than on n-type SiC. The maturity of p-type SiC wafers needs to be improved, and the mechanism for ohmic contact formation on p-SiC is still a matter of research. Generally, Al based alloys, such as Al/Ti, are used for ohmic contacts on p-type SiC after annealing at 900-1000°C. Al reacts with SiC and forms Al4C3 and Si during annealing. In this study, we have investigated the roles of Al4C3 in the formation of ohmic contacts on p-SiC. Based on the stoichiometric formation of Al4C3 between Al and SiC at high temperatures, several samples with various Al/C mole ratios in the contact layer were examined after different annealing temperatures. Carbon rich, stoichiometric Al/C films form Al4C3 and ohmic contacts on p-type 4H-SiC (~2.8 x1018 cm^{-3}) after annealing at 800 and 900°C. Al/SiC, as a control sample, does not form ohmic contacts under the same conditions. This study reveals that the interactions between Al and C on SiC are responsible for ohmic contacts on SiC, while the secondary metal, i.e., Ti or Ni, improves electrical conductivity of the film.

Tantalum-Ruthenium Diffusion Barriers for Contacts to SiC: *Sammy H. Wang*[1]; Chad M. Eichfeld[1]; Mary A. Horsey[1]; Bangzhi Liu[1]; Suzanne E. Mohney[1]; Victor Adedeji[2]; John Williams[2]; [1]Pennsylvania State Univeristy; [2]Auburn University

A diffusion barrier is needed to protect contacts to SiC in air at high temperature. For example, failure of Ni and Al/Ni ohmic contacts to p-SiC is observed after aging at 350°C in air for 100 h and 750 h, respectively. We previously reported a Ta-Ru-N diffusion barrier that protects these contacts for at least 2,000 h at 350°C in air. Unfortunately, adhesion of Au layers for wire bonding to the nitride barrier layers still requires improvement. Since Auger depth profiles indicated outdiffusion of nitrogen from aged Ta-Ru-N barriers, we have omitted nitrogen and tested contacts beneath Ta-Ru barriers. The Ta-Ru barriers also protect Ni and Al/Ni ohmic contacts, with specific contact resistances of 4×10^{-5} and 3×10^{-5} Ohm cm^2, respectively, after 2000 h in air at 350°C. Pull tests reveal good adhesion only for the Al/Ni contacts. For the longest time tested (500 h), an average pull strength of 630 g was measured. Encouraging electrical and mechanical results have also been obtained for both ohmic contacts when thin Ta adhesion layers are used between the Ta-Ru barrier and Au. Further aging and materials characterization of the samples is underway.

Diffusion Welding Techniques for Power SiC Schottky Packaging: *Oleg Korolkov*[1]; Toomas Rang[1]; Alexsander Syrkin[1]; Vladimir Dmitriev[1]; [1]Tallinn University of Technology

This paper is devoted to the results of diffusion welding technique applied to solve the problem of packaging for large area SiC Schottky diodes. To supply low defect density substrates for fabrication of 0.3 cm^2 Schottky diodes TDI defect-reducing technology was used. Diodes were fabricated on CVD grown low-doped 4H-SiC epitaxial layer without edge termination. Double layer Ni-Au and triple layer Ti-Ni-Au sputter metallization were used for Schottky contacts fabrication. Non-rectifying bottom contacts were provided by Ni-Au metallization. Diodes were tested on-wafer and delivered for dicing, and packaging. To decrease the parasitic spreading resistance the thickness of initial sputter metallization was increased by diffusion welded 30 µm metal foil. Such combined thick and plane metal layers makes it possible to perform the clamp mode package in the cases usually used in power electronics. This scheme of packaging ensures current takeoff from the whole contact area and increases operating temperature up to 600°C. The forward current-voltage characteristics up to 75 A measured for packaged diodes give 250 A/cm^2 (70A) at 1.9 V forward voltage. Reverse recovery time for packaged diodes was in the range of 29-36 ns.

Investigation of TiW Contacts to 4H-SiC Bipolar Junction Devices: *Hyung-Seok Lee*[1]; Martin Domeij[1]; Carl-Mikael Zetterling[1]; [1]KTH, Royal Institute of Technology

Low–resistivity ohmic contact formation is one important issue of SiC device processing. SiC Bipolar Junction Transistor (BJT) is one of the difficult devices to achieve ohmic contact since the base contact is commonly fabricated on p-type implanted material. During the processing in SiC BJT, the SiC surface experiences harsh conditions like dry etching, oxygen plasma cleaning, ion-implantation and high temperature annealing. In this paper, we have examined ohmic contacts formation in a SiC BJT process with sputter deposition of titanium tungsten contact to both n-type and p-type SiC followed by annealing at 950°C. The contacts were characterized with linear transmission line method (LTLM) structures. To see the change of compound phases, X-ray Diffraction (XRD) θ-2θ scans were performed before and after annealing. The results give at hand that 5 minutes annealing of n+ contact is sufficient whereas the p+ contact undergoes dramatic improvement between 5 and 15 minutes annealing at 950°C. The n+ emitter structure and p+ base structure contact resistivity after 30 minutes annealing was 1.4 x 10-4 Ocm2 and 3.7 x 10-4 Ocm^2, respectively. Roughness measurement using AFM will also be presented.

Ti/AiNi/W and Ti/Ni2Si/W Ohmic Contacts to p-Type SiC: *Bang-Hung Tsao*[1]; Jacob Lawson[1]; James Scofield[2]; [1]University of Dayton Research Institue; [2]AFRL

AlNi and Ni2Si based ohmic contacts to p-type 4H-SiC have been produced using low energy ion implantation, a Ti contact layer, and sequential anneals. Low resistivities were achieved by degenerately (>1020 cm^{-3}) doping the surface region of 4H-SiC epilayers via low energy Al+ implantation. High acceptor activation and improved surface morphology was promoted by capping the samples with pyrolized photoresist and a two-step anneal sequence in Ar. Ti/AlNi/W and Ti/Ni2Si/W stacks were compared by varying the anneal temperature and thickness of the Ti, AlNi, and Ni2Si. AlNi, specific contact resistivities as low as 5.5 x10-5 ohm-cm^2 were achieved after annealing between 700 and 1000°C for 2 minutes in argon. For the Ni2Si samples, resistivities as low 4.5x10-4 ohm-cm^2 were obtained after annealing between 750 and 1100°C. For both metal stacks, the lowest resistivities were realized using thicker (40 nm) Ti layers. I-V analysis reveals a superior linear characteristic for the AlNi system, which also exhibited a more stable microstructure after anneal. SEM and optical microscopy illustrate microstructure evolution with temperature. SIMS and RBS were used to analyze the stability of the stacks subsequent to thermal treatment. AFM analysis illustrates the superiority of photoresist capping over alternatives in minimizing roughness.

Formation and Properties of Schottky Diodes on 4H-SiC after High Temperature Annealing with Graphite Encapsulation: *Brian J. Skromme*[1]; Yu Wang[1]; Mikhail Mikhov[1]; [1]Arizona State University

Annealing SiC at temperature high enough to activate p-type implantations (~1600-1700°C or higher) can cause severe step bunching and roughness if the surface is not adequately protected from loss of Si. The electrical properties of Schottky diodes subsequently formed on such surfaces are particularly sensitive to damage from annealing, which is important when the implants are used for JTE termination of Schottky diodes, for example. Here, we study the impact of annealing using graphite encapsulation (formed by baking photoresist) on the electrical properties of Ni Schottky diodes. The surface morphology is also characterized by atomic force microscopy (AFM). Annealing for 10 min. at temperatures up to 1700°C with graphite encapsulation actually reduces the high-current ideality factor of the diodes while raising the barrier height (linearly extrapolated to n=1) from 1.462 V to 1.68-1.72 V. Excess leakage or excess current at low forward voltage occurs only in a subset of diodes, which are believed to be affected by extended defects. The AFM images show no significant surface roughening, and the graphite can be removed after processing. We conclude that this encapsulation method is highly effective in preserving the electronic properties of the surface during high temperature annealing.

RPD1.Novel Devices and Applications

The Properties of n-ZnO/p-SiC Heterojunctions and Their Potential Applications for Devices: *Cole W. Litton*[1]; Yahya Alivov[2]; Suheyla Sena Akarca-Biyikli[2]; Qian Fan[2]; Daniel Johnstone[2]; Umit Ozgur[2]; Vitaliy Avrutin[2]; Kaigui Zhu[2]; Hadis Morkoç[2]; [1]Air Force Research Laboratory; [2]Virginia Commonwealth University

ZnO with a direct wide band gap (Eg~3.3 eV) is attractive for optoelectronics applications due in part to the availability of ZnO bulk single crystals and a large exciton binding energy (~60 meV). Because reproducible and high quality p-type ZnO films have not yet been achieved, growth of n-type ZnO on other p-type materials could provide an alternative avenue to realize ZnO based p-n heterojunctions. The main factor to be considered, which influences the properties of heterostructures, is the close lattice match of the components employed. In this respect 6H-SiC is a good candidate since it has wurtzite crystalline structure and relatively good lattice matching to ZnO with lattice mismatch of ~4%, and p-6H-SiC substrates are commercially available. Here we report on the growth of n-ZnO/p-6H-SiC heterostructures by plasma-assisted molecular-beam epitaxy and their electrical and optical properties studied by various methods. Their possible applications are also discussed.

Silicon Carbide Power Diodes as Radiation Detectors: *Bernard Phlips*[1]; K. D. Hobart[1]; F. J. Kub[1]; R. E. Stahlbush[1]; M. K. Das[2]; G. De Geronimo[3]; P. O'Connor[3]; [1]Naval Research Laboratory; [2]Cree Inc.; [3]Brookhaven National Laboratory

DARPA has been developing Silicon Carbide (SiC) devices as part of its high power electronics program. These devices consist of 100 micron thick SiC grown epitaxially on SiC substrates. The size and thickness of the devices make them interesting as radiation detectors. We tested 0.25 cm^2 and 0.5 cm^2 devices and obtained X-ray spectra under illumination with an Americium-241 radioactive source. The spectra showed an energy resolution that was consistent with the resolution expected for the large capacitance of the device. Smaller devices with a diameter of 1 mm were therefore tested. When connected to a custom ASIC, these devices produced spectra with a room temperature energy resolution of ~550 eV and no low-energy tails. This is consistent with the electronics limit for the capacitance of the small device. The intrinsic energy resolution is therefore better than 550 eV and the charge collection is therefore complete to within ~28 electrons. This is an excellent performance for a device that was designed for 50 Amperes. Applications for these devices can be found in the fields of particle physics, nuclear physics, nuclear medicine, X-ray fluorescence, X-ray astronomy and X-ray navigation.

Influences of B-Doped Layer under the Channel of H-Terminated Diamond FETs: *Toru Koshiba*[1]; Kazuyuki Hirama[1]; Takeyasu Saito[2]; Masahiko Ogura[2]; Mitsuya Sato[1]; Hitoshi Umezawa[2]; Kyung-Ho Park[2]; Hiroshi Kawarada[1]; [1]Waseda University Kawarada Laboratory; [2]National Institute of Advanced Industrial Science and Technology

Diamond is expected as a next generation semiconductor for high power and high frequency applications. In this study, diamond MISFETs have been fabricated on H-terminated B-doped diamond and evaluated their characteristics. There are expectations for B-doped diamond in the improvement of characteristics such as sheet resistance and mobility. The sheet resistance of 5.4 kΩ/sq and the hole mobility of 124 cm^2/Vs has been measured with the H-terminated B-doped diamond. This time, we have obtained the fT of 18.4 GHz, the fmax of 24.1 GHz and the transconductance of 100 mS/mm with 0.6-μm-gate.

Structural Properties and Electrical Characteristics of Homoepitaxial GaN PiN Diodes: *Xian-An Cao*[1]; S. F. LeBoeuf[1]; H. Lu[1]; C. Cowen[1]; S. D. Arthur[1]; [1]GE Global Research Center

GaN PiN diodes with a 4μm lightly-doped n$^-$-GaN drift layer (n~7x10^{16}16 cm^{-3}) were grown on free-standing GaN and sapphire substrates using metalorganic chemical vapor deposition. The lattice mismatch between the GaN substrate and the homoepitaxial material was found to be ~1x10^{-4}. The full width at half maximum of the (0002) rocking curve was 79 arcsec compared to 230 arcsec for the diode structure grown on sapphire. Secondary ion mass spectrometry measurements showed that the incorporation of C, H, and O impurities in the homoepitaxial drift layer was reduced by a factor of 2 – 4. The diodes on GaN demonstrated rectification to –265 V, which represents a 1.6x improvement over the diodes on sapphire and corresponds to a critical electric field ~2.7x10^6 V/cm. The homoepitaxial diodes also showed two orders of magnitude lower reverse leakage and a smaller negative temperature coefficient for breakdown voltage, consistent with a reduced dislocation density in the drift region.

Inherently Safe Resonant Reset Forward Converter Using a Bias-Enhanced SiC JFET: *Robin Kelley*[1]; Travis Brignac[2]; Michael S. Mazzola[2]; Will Draper[1]; Jeffrey B. Casady[1]; [1]SemiSouth Laboratories, Inc.; [2]CAVS at Mississippi State University

Diverse industries are beginning to look toward SiC to solve problems that Si devices are not capable of addressing. Requirements include reliable performance in high temperature environments as well as innovative solutions resulting in increased efficiency. The power junction FET (JFET) is the second most mature SiC device, after the SiC Schottky diode, and is commonly associated with normally-on functionality; this feature is often viewed as problematic for off-line dc-to-dc converter applications. Two inherently safe, single-switch dc-dc converter designs have been developed that put into practice pure SiC JFET devices (i.e., without cascoded devices) that possess enhancement-mode functionality and bias-enhanced blocking. These 'Quasi-Off' devices block half rated blocking voltage at zero gate bias and achieve full rated blocking capabilities with a modest negative bias, typically -5V. Inherent safety against indefinite short circuits at the output and gate driver failure is provided by utilizing the devices enhancement-mode functionality coupled with appropriate gate driver design. Bias-enhanced blocking matches the dynamic stress encountered by modern high-frequency power supply topologies to the ratings of the device while recognizing that larger dynamic stress is typically encountered only when the power supply (especially the gate driver) is functioning properly. Working prototypes of both circuits are reported.

First Demonstration of 2100 W Output Power at 425 MHz Using 4H-SiC RF Power BJTs: *Anant K. Agarwal*[1]; Jeremy Haley[2]; Howard Bartlow[3]; Bill McCalpin[2]; Sumi Krishnaswami[1]; Craig Capell[1]; Sei-Hyung Ryu[1]; John W. Palmour[1]; [1]Cree Inc.; [2]dBm Engineering, Inc.; [3]HdB Engineering, Inc.

4H-SiC RF Bipolar Junction Transistors (BJTs) have been designed and tested at 425 MHz. Twenty four cells representing approximately 24 inches of emitter periphery were packaged and tested at 425 MHz in common emitter, Class C mode with a 75 V power supply voltage. The pulse width was 2 microseconds and the duty cycle 1%. The total output power was measured to be 2100 W with a power gain of 6.3 dB, collector efficiency of 45% and power added efficiency of 35%. This is the first time, SiC BJTs have been used to produce an output power in excess of 2 kW at 425 MHz. Although the gain and PAE are not very high, the individual cells are capable of producing 50 W with a gain of 9.3 dB and 51% collector efficiency. By further optimization of the device design, cell layout, the input and output match, and by increasing the power supply voltage to 120 V, it is expected that the output power, gain and efficiency can be further improved.

Switching Characteristics of SiC-MOSFET and SBD Power Modules: *Masayuki Imaizumi*[1]; Yoichiro Tarui[1]; Shinichi Kinouchi[1]; Hiroshi Nakatake[1]; Yukiyasu Nakao[1]; Tomokatsu Watanabe[1]; Keiko Fujihira[1]; Naruhisa Miura[1]; Tetsuya Takami[1]; Tatsuo Ozeki[1]; [1]Mitsubishi Electric Corporation

SiC-MOSFETs are promising switching devices for future power converters. A great advantage of SiC-MOSFETs over competitor Si-IGBTs is their low loss switching due to small storage carriers. In this paper, we describe switching characteristics of SiC power modules fabricated using our MOSFETs and SBDs, and discuss their switching losses in comparison with Si-IGBT modules. Prototype SiC devices used for the study are class 10 A, 1.2 kV SiC-MOSFETs and SiC-SBDs. These devices were packaged in a conventional module case to fabricate modules. A double pulse method was used to evaluate switching characteristics. In the SiC module, both overshoot and tail current, which induce power losses, were reduced markedly. Using the measurement, we calculated their switching losses. In Si modules, although the transistor turn-ON loss decreased gradually when RG decreased, the transistor turn-OFF loss saturated and the diode recovery loss increased in low RG range. In contrast, the losses in SiC modules decreased with a decrease in RG and were considerably low especially in the low RG range. The merit of power loss reduction in SiC modules becomes notable at low RG, or high speed switching. Numerical comparison in losses between SiC and Si modules will be given in the paper.

CM-Wave Modulator with High-Voltage 4H SiC Pin Diodes: *Mykola Boltovets*[1]; Volodymyr Basanets[1]; Oleksandr Zorenko[1]; Valentyn Krivutsa[1]; Nicolas Camara[2]; Volodymyr Orechovskij[1]; Vasyl Simonchuk[1]; Konstantinos Zekentes[2]; [1]State Enterprise Research Institute "ORION"; [2]MRG, IESL, Foundation for Research and Technology-Hellas

The results of mathematical simulation, development and investigation of a modulator with 4H SiC pin diodes are presented. For pin diodes (with i-region 6 μm long) we simulated the effect of bias modes on isolation and transmission between the modulator input and output in the 1÷20 GHz frequency range. It was calculated that the isolation in a modulator with three diodes may run to –45 dB and the transmission losses no more than 2 dB. The modulator was made as a hybrid integrated circuit (HIC) on the basis of nonsymmetrical strip lines (characteristic impedance of 50 Ω) incorporating chips of high-voltage 4H SiC pin diodes with i-region 6 μm long, mesa diameter of 60 μm and calculated avalanche breakdown voltage of 1000 V. We studied the experimental parameters of modulator with shielded diodes as a function of forward current and reverse voltage in the 2.4÷12 GHz frequency range, as well as the microwave signal switching behaviour. It was determined that the modulator with shielded diodes provides losses level of 1.0÷2.0 dB and isolation of 27÷34 dB in the 2.4÷7 GHz frequency range. It also provides formation of microwave pulses with leading (trailing) edge of 22 (29) ns.

Electron Injection from GaN to SiC and Fabrication of GaN/SiC Heterojunction Bipolar Transistors: *Jun Suda*[1]; Yuki Nakano[1]; Syouta Shimada[1]; Tsunenobu Kimoto[1]; [1]Kyoto University

SiC is a very attractive material for high-temperature, high-power and high-frequency devices. Heteroepitaxial growth of group-III nitrides on SiC makes it possible to utilize bandgap engineering in SiC-based devices. (Al)GaN/SiC heterojunction bipolar transistors (HBTs) are promising candidates for high-power, high-frequency amplifiers. Control of the n-GaN/p-SiC heterojunction is the most important factor to realize high-performance HBTs. Previously, we have studied n^+-GaN/p^--SiC heterojunctions with GaN layers grown by plasma-assisted molecular-beam epitaxy. From capacitance-voltage measurements it was confirmed that the valence band offset is larger than the conduction band offset, i.e. the potential barrier for electron injection is smaller than that for hole injection. In this study, we present characterization results for n^+-GaN/p^--SiC and n^+-GaN/p^+-SiC heterojunctions as well as fabrication of GaN/SiC HBTs using these heterojunctions. Electroluminescence from n^+-GaN/p^+-SiC heterojunction diodes under forward bias clearly indicated electron injection from n^+-GaN into p^+-SiC. HBT structures consisting of n^+-GaN emitter (0.5μm, 10^{19}cm^{-3})/p^+-SiC base (0.5μm, 5×10^{19}cm^{-3})/n-SiC collector (10μm, 1×10^{16}cm^{-3})/n^+-SiC substrate were fabricated. Clear common-base properties were observed. However, the current gain was as low as 10^{-4}. This is mainly due to low injection efficiency. The HBT fabrication process and improvement of the injection efficiency by controlling the initial growth of GaN on SiC will be discussed.

Minimum Ionizing Particle Detector Based on p^+n Junction SiC Diode: Francesco Moscatelli[1]; *Andrea Scorzoni*[1]; Antonella Poggi[2]; Mara Bruzzi[3]; Silvio Sciortino[3]; Gunter Wagner[4]; Roberta Nipoti[2]; Stefano Lagomarsino[3]; [1]DIEI and INFN Perugia; [2]CNR-IMM sez. BO; [3]INFM and University of Florence; [4]Institut fur Kristallzuchtung Berlin

In this work p^+/n diodes have been used as minimum ionizing particle (MIP) detectors. The diode structure is based on a 0.45 μm deep, $N_A = 4\times10^{19}$ cm^{-3} doped p^+ emitter, ion implanted in an n-type epilayer with thickness equal to 55 μm and nominal donor doping $N_D = 2\times10^{14}$ cm^{-3}. The diode breakdown voltages were above 1000V. At 1000V the leakage current is of the order of 1 nA for all the measured diodes. The depletion voltage is near 220-250 V. The charge collection efficiency to minimum ionising particle has been investigated by a ^{90}Sr β source. The pulse height spectrum was measured as a function of the reverse voltage in the range 0-605V. At each bias point the signal was stable and reproducible, showing the absence of polarisation effects. At 220 V the collected charge was 2970 e^- and saturates at 3150 e^- near 350 V. To our knowledge, this is at the moment the highest collected charge for SiC detectors. At bias voltages over than 100V the spectrum was found to consist of two peaks clearly separated. Around 250 V the signal saturates, in agreement with CV results. The signal noise ratio (SNR) is 6.5.

SiC-Based MOSFETS for Harsh Environment Emissions Measurements: *Peter Sandvik*[1]; Majdeddin Ali[2]; Vinayak Tilak[1]; Kevin Matocha[1]; Thomas Stauden[2]; John Deluca[1]; Oliver Ambacher[2]; [1]GE Global Research; [2]Technical University Ilmenau, Center for Micro and Nanotechnologies

SiC materials are particularly advantageous due to their robust nature, and may be utilized for a number of sensor applications. Gas sensors working at very high temperatures are desired in the monitoring and control of combustion processes, including automotive engines, gas turbines and boiler plants. Gases which are of particular interest include NO, NO2 and O2. Real-time, low-cost sensors measuring those species might be used to tune engines and optimize combustion efficiency while maintaining safe levels of emissions. To date, few sensors have been made available for those gases at high temperatures, typically well in excess of 250ºC. Here, we present SiC FETs fabricated with thin film catalysts deposited in the gate area. These MOSFET devices have been evaluated for their sensitivity to gases at high temperatures with varying bias and current levels. We will describe the device design and fabrication process, and the resulting sensors responses to gases at various temperatures and operating conditions. By choosing the appropriate temperature and catalyst material, devices that are significantly more sensitive to certain gases may be realized. Lastly, we will quantify the devices behavior by showing their confidence and prediction intervals over a variety of conditions.

Current Sensing for SiC Power Devices: Tournier Dominique[1]; *Philippe Godignon*[1]; Josep Montserrat[1]; Jose Millan[1]; Dominique Planson[2]; Franck Sarrus[3]; [1]CNM-IMB; [2]CEGELY - INSA LYON; Ferraz Shawmut

High voltage, high current capabilities of SiC based devices has been already proved, and high current SiC devices working at high temperature are susceptible to be in the market soon. SiC power integration will have to be considered as a further development step to discrete power devices. Packaging remaining the main constrains for high temperature operation and system integration. Up to date, no industrial high temperature package has been reported. In case of short circuit or over current, SiC devices can reach high temperature values, and die might be subjected to high stresses. In order to address such critical requirements, current sensing and real time temperature monitoring are compulsory. The proposed structure provides a protection feature to SiC power devices, to get reliable high temperature electronics. An integrated current sensor has been implemented in a vertical power SiC JFET and its fabrication is reported for the first time in this paper. The current sensor layout and process technology are presented. An experimental current sensing validation is also reported. A current sense-FET device incorporated into a main control system will be analysed in detail in the final paper as well as integration perspectives and the benefits in terms of reliability.

The Limit of SiC Detector Energy Resolution in Ions Spectrometry: Alexandre Lebedev[1]; Alexandre Ivanov[1]; Nikita Strokan[1]; *Rositza Yakimova*[2]; [1]A.F. Ioffe Physicotechnical Institute; [2]Linkoping University

The limit of SiC detector energy resolution is connected with the fluctuations accompanying the transformation of particle (quantum) energy in a nonequilibrium charge. This is incoherence of losses of particle energy in elastic collisions with atoms of "medium" (Si and C), and also fluctuations of the number of electron-holes pairs directly in cascades of impact ionization. By carrying out Monte-Carlo simulation and comparison with real resolution of SiC based detectors it was concluded that the detection limit of a SiC (binary

compound) based detector is comparable to that gained in Si (mono atomic semiconductor) based detectors. The presence of two types of atoms (Si and C) did not lead to significant energy fluctuation in elastic collisions of a-particles. The improved crystal quality of the SiC epilayers enables rather low losses of charge carriers during their transport in the detector. This strongly suggests that SiC can be considered as a "detection medium" similarly to the traditional detector materials Ge, Si, CdTe.

GaN Resistive Gas Sensors for Hydrogen Detection: Feng Yun[1]; S. Chevtchenko[1]; Y.-T. Moon[1]; H. Morkoc[1]; T. J. Fawcett[2]; *John T. Wolan*[2]; [1]Virginia Commonwealth University; [2]University of South Florida

We report on the fabrication and testing of GaN resistive gas sensors for hydrogen detection. The Si-doped n-type GaN was grown by organometalic vapor phase epitaxy (OMVPE) on c-plane sapphire substrates. The device structure is simply a pair of metal contact pads. The sensors are sensitive to H2 gas over a wide range of concentration: the lowest concentration tested being ~0.1% H2 (in Ar), well below the lower combustion limit in air. No saturation of the signal is observed up to 100% H2 flow. In the continuous operation mode with varying H2 concentration, a clear and sharp response was recorded with no memory effects during ramping up and down cycles of H2 concentration. The change in current at a fixed voltage to hydrogen was found to change with sensor geometry, consistent with a surface-adsorption-induced change of conductivity. Possible gas sensing mechanisms will be discussed.

4.5 kV- 8A SiC-Schottky Diodes / Si-IGBT Modules: *Tournier Dominique*[1]; Peter Waind; Philippe Godignon[1]; Jose Millan[1]; Roger Bassett[2]; [1]CNM-IMB; [2]Areva

Silicon has long been the dominant semiconductor for high-voltage power applications. Due to the significant achievements in SiC bulk material growth and in SiC device processing technology, this semiconductor has received a great interest for power devices, concretely for SiC high-voltage rectifiers. The main difference to ultra fast Si pin diodes lies on the absence of reverse recovery charge in SiC SBDs. This paper reports on 4.5kV-8A SiC Schottky diodes / Si-IGBT modules. The Schottky termination design and the fabrication process allow to get a relevant manufacturing yield of 40% for large area devices on standard starting material. Modules have been successfully assembled, containing Si-IGBTs and 4.5kV-SiC Schottky diodes and characterized in static and dynamic regime. The forward dc characteristics of the modules shows an on-resistance of 33mohm.cm2 \@ RT and very a low reverse leakage current density (JR < 10 µA/cm2 \@ 3.5kV). An experimental breakdown voltage higher than 4.7kV has been measured in the air on polyimide passivated devices. This value corresponds to a confirming a termination protection efficiency of at least 80%. These SiC SBDs are well suited for high voltage, medium current, high frequency switching aerospace applications, matching perfectly as freewheeling diodes with Si IGBTs.8A module.

RPM1.SIMS & Electrical Properties of Defects

Electrical Properties of Undoped 6H- and 4H-SiC Bulk Crystals Grown by Halide Chemical Vapor Deposition: *Hun Jae Chung*[1]; Sung Wook Huh[1]; Alexander Y. Polyakov[1]; Saurav Nigam[1]; Qiang Li[1]; Marek Skowronski[1]; Evan R. Glaser[2]; William E. Carlos[2]; Mark A. Fanton[3]; Nikolai B. Smirnov[4]; [1]Carnegie Mellon University; [2]Naval Research Laboratory; [3]Pennsylvania State University; [4]Institute of Rare Metals

Undoped 6H- and 4H-SiC crystals were grown by Halide CVD at growth temperatures of around 2050ºC with C/Si ratio of 0.06 ~ 0.7. SIMS measurements showed nitrogen and boron were the only detectable impurities with concentrations in the 10^{15} cm^{-3} range. With increasing C/Si ratio, the nitrogen concentration decreased while that of boron increased as expected for the site-competition effect. Increasing growth temperature led to decrease of net donor concentration measured by C-V method. This is interpreted as due to enhanced desorption of nitrogen and lower Si surface coverage at higher temperatures. Hall-effect measurements showed the Fermi level was pinned by nitrogen donors in Si-rich (C/Si < 0.1) samples and by the 0.27 eV level in samples with intermediate C/Si ratios. Semi-insulating crystals with room-temperature resistivities between 10^5 and 10^{10}Ωcm were grown with C/Si > 0.36. They are Si-rich, because EPR and low-temperature PL measurements did not detect carbon-antisite complexes, but only carbon-vacancies. Photo-induced current-transient-spectroscopy measurements revealed the presence of multiple deep electron and hole traps. These semi-insulating samples were p-type with the Fermi level located at either the boron acceptor level or the boron-related deep centers. The high resistivities are attributed to close compensation of these centers.

Commercial Optical Scanning Investigations of Doping Density Variations in SiC Substrates: *Joshua David Caldwell*[1]; Orest J. Glembocki[1]; Darren Hansen[2]; Gilyung Chung[2]; Karl Hobart[1]; Frances Kub[1]; [1]Naval Research Lab; [2]Dow Corning Corporation

Here we present the use of commercial optical scanners for mapping the doping density over the surface of a SiC wafer and as a local probe for levels in different regions of the wafer. This method provides a cost effective and fast method for determining homogeneity, defect sites and areas of different polytypes or polycrystalline regions. Local data from the maps have been calibrated using the shift of the LO-phonon mode in µ-Raman spectra as a metric for N_D. It is shown that features present in the transmission maps strongly correlate to those observed in Lehighton resistivity maps. Finally, the complimentary use of these two mapping methods pose the possibility of calculating mobility, therefore providing most electrical parameters required for wafer characterization.

Results of SIMS, Temperature-Dependent Hall Effect and LTPL Measurements Performed on Al-Doped a-SiC Substrates Grown by the M-PVT Method: *Sylvie Contreras*[1]; Marcin Zielinski[1]; Leszek Konczewicz[1]; Caroline Blanc[1]; Sandrine Juillaguet[1]; Ralph Müller[2]; U. Künecke[2]; Peter Wellmann[2]; Jean Camassel[1]; [1]Université Montpellier 2; [2]University of Erlangen

We report an investigation of bulk, p-type doped, SiC wafers grown by the Modified- Physical Vapor Transport (M-PVT) method. Compared to conventional PVT, this technique makes use of an additional gas pipe into the growth cell. This allows improving the growth conditions and doping capabilities. Indeed, SIMS analysis performed with a Cameca IMS 5f mass spectrometer give Al concentrations in the range 1018 to 1020 cm^{-3}. Ti is weak but nitrogen is not. This suggests strong electrical compensation. To determine the wafers resistivity, carrier concentration and mobility, temperature-dependant Hall effect measurements have been performed from 100 K to 850 K using the Van-der-Pauw method. From a comparison between theory and experiments, the degree of compensation, ionisation energy of impurities and scattering mechanisms have been obtained. The active Al concentration is in agreement with the SIMS measurements, but the temperature dependence of the mobility suggests more compensation than previously determined by SIMS. Additional LTPL investigations show no evidence of additional impurities but suggest that the additional compensation may come from an increased concentration of non-radiative centers.

Improved SIMS Methods for Measuring N in SiC: *Howard E. Smith*[1]; Kurt G. Eyink[2]; William C. Mitchel[2]; [1]University of Dayton Research Institute; [2]Air Force Research Laboratory

The background nitrogen concentration in SiC is an important characteristic, with modern wafer manufacturing technology producing levels well below 1 x 1016 atoms/cm^3. Measuring these levels presents a challenging problem for Secondary Ion Mass Spectrometry (SIMS) because of problematic mass interferences, and beam-induced charging which vexes the necessary high resolution work. Thus the SIMS industry standard approach employs simultaneous detection of the combined 12C15N- and 13C14N- minor isotopes at nominal mass 27, requiring only moderate mass resolving power, and providing reasonable counting statistics into the 1015 atoms/cm^3 range. However, these combined ions represent only 1.4% of the total CN- signal. In this work, it is shown that the 12C14N- (98.6% abundance) instead can be analyzed on the typical CAMECA SIMS 4F – 7F class SIMS instrument using careful electron compensation combined with a mass resolving power exceeding 20,000 (10% valley), thus resolving it from the problematic and abundant interference from 13C13C-. This alternative approach, combined with a new method for reducing the nitrogen background in the SIMS instrument, provides improved performance with reasonable counting statistics and a detection limit into the 1014 atom/cm^3 range. This method also establishes the measurement precision and assigns the uncertainty on the measurement.

Accurate SIMS Aluminum Dopant Profiling in SiC: *Howard E. Smith*[1]; Bang-Hung Tsao[1]; James Scofield[2]; [1]University of Dayton Research Institute; [2]Air Force Research Laboratory

Aluminum ion implants into p-type 4H-SiC are used to achieve degenerate doping for AlNi-based ohmic contacts. Detailed knowledge of this total aluminum distribution is important for correlation to the electrically properties, and for authenticating implantation and diffusion models. Secondary Ion Mass Spectrometry (SIMS) was used to evaluate the aluminum concentration profile before and after anneal, and compared to the model. A common SIMS method was employed: sputtering with a Cs+ and following the CsM+ depth profile (here, M = Al). It was observed that the aluminum profile obtained by following the CsAl+ secondary ion differed considerably from that obtained from Al+, with both using a Cs+ primary ion beam. An Al+ profile obtained using an O2+ primary ion beam best matched the Cs+/Al+ profile. This anomaly in the CsAl+ profile was found to be caused by depth-dependent surface charge buildup during the profile, which in turn affects surface work function, the sputtered concentration of Cs0 concentration, and ultimately the CsAl+ signal (produced in the SIMS plasma from the combination of the Cs0 with Al+) in a depth dependent way. This has broad implications for SiC SIMS characterization; experimental conditions to ensure accurate SIMS profiling are described.

RPM2.Electrical & Optical Properties IV

Quenching Photoconductivity and Photoelectric Memory in 6H-SiC: *Marat Duisenbaev*[1]; [1]Karakalpak State University

We investigated high-resistance samples of beryllium doped 6H-SiC which were grown in laboratories of semiconductors and dielectrics of St.-Petersburg Electrotechnical University. The crystals 6H-SiC were polished with sides of parallel mirrored facets [0001] up to a thickness 1.4*10-2-2*10-2 cm. The researched structure was located in cryostat and was irradiated with its own light. A mercury lamp and monochromator were used as a source of its own excitation. The maximum level of excitation ϕmax=2. 6*1014 quantum/cm^2*s and weakening was made with the help of the graduated filters. For illumination an incandescent lamp was used and the light past through monochromator. The maximal intensity of illumination was equal to 1.5 *1015 quantum/ cm^2*s. This is the first time the superlinear dependence in lux–current characteristic, optical and temperature quenching of photocurrent and photoelectric memory in structures made on the basis of compensated 6H-SiC, at room and high temperatures has been discovered. The depth sensivity centre is Ec -1.1eV and the cross section of capture holes on this centre is10-21-10-22 cm^2 is determined.

About Nature of Recombination Current in 4H-SiC pn Structures: *Anatoly Strel'chuk*[1]; Alexander Lebedev[1]; Alexei Mashichev[1]; Anna Volkova[1]; Konstantinos Zekentes[2]; [1]A.F. Ioffe Physico-Technikal Institute Russian Academy of Sciences; [2]Institute of Electronic Structure and Lasers

Device degradation under operation in heavy duty conditions is between the most important problems of the modern SiC based electronics. The particular case of this problem is the surface effects on the diode operation. In this study the forward current J=Joexp(qU/nkT), Jo=Jo*exp(-(Ea/kT)) characterized by n»2 and Ea»Eg/2 was investigated in 4H-SiC pn structures. Such current is usually considered as current due to bulk recombination in the space charge region of pn junction via deep level. However, it was also suggested that this current can be due to surface recombination. The criteria which is performed in this study to differentiate such currents was the investigation of recombination current versus perimeter/area ratio dependence. It was found that no pronounced difference of the parameter Jo for the diodes with different perimeter/area ratio observed, i.e. any noticeable current due to surface recombination did not observed for the hereby 4H-SiC pn structures investigated.

RPM3.Extended Defects IV

Effect of Substrate Defects on Reverse I-V Characteristics of 4H-SiC APD: *Stanislav Soloviev*[1]; Peter Sandvik[1]; Stephen Arthur[1]; Kevin Matocha[1]; Sergei Maximenko[2]; Tangali Sudarshan[2]; [1]GE Global Research; [2]University of South Carolina

Among a various wide bandgap semiconductors, 4H-SiC is a preferable candidate for UV avalanche photodetectors operating at elevated temperatures. In this work, we investigated the effect of substrate defects on reverse I-V characteristics of the avalanche photodiodes using electron-beam induce current mode (EBIC) of SEM. SiC APDs were fabricated using 2 inch p-doped substrates with n-doped epilayers. Areas of the formed diodes were approximately 1mm2. It has been suggested that reverse applied current may induce a change in the EBIC contrast of various types of dislocations. However, no change in the EBIC contrast of dislocations was observed when the diode was subject to a reverse bias. Stability of such a device was tested by applying a short pulse of high voltage (~800V). EBIC images, taken prior to and after the failure test, showed an appearance of new defects in the dislocation free area. Mechanism of the formation of these defects will be discussed.

Point Defects and Basal-Plane Stacking Faults in 4H-SiC: *Naomi Fujita*[1]; Alexander T. Blumenau[2]; Benjamin Hourahine[3]; [1]University of Exeter; [2]Max-Planck-Institut f. Eisenforschung GmbH; [3]University of Strathclyde

The possible role of point defects in nucleating the formation of basal-plane stacking faults in 4H-SiC is investigated using a density-functional based tight-binding method. Such stacking faults are considered to be the major failure mode of p-i-n diodes, and are normally considered to nucleate from pre-existing extended defects, however a recent study strongly suggests a point-like source for at least some faults. To investigate this possibility, the interaction of very small SF regions bounded by Shockley partials is simulated and the roles of both hydrogen and native defects are considered in stabilising these nucleation sites.

Examining Dislocations in SiC Epitaxy by Light Emission from Simple Diode Structures: *Kendrick X. Liu*[1]; [1]U.S. Naval Research Lab

A key component in developing and maintaining low basal plane dislocation (BPD) epitaxial processes is to develop characterization techniques to quickly examine BPDs after each growth. A very reliable and sensitive technique for detecting BPDs is to image the electroluminescence from forward-biased PiN diodes with a metal grid for the anode contact. In this presentation, we describe a simple diode structure that has many of the characteristics of a gridded PiN diode but that can be fabricated much quicker. The only processing steps are to deposit and pattern aluminum (Al) on both sides of a wafer with an epitaxially grown n- drift layer and p+ anode. Three wafers with thick drift layers, 100 – 150 µm, and different concentrations of BPDs are examined. Kelvin contacts compensate for the voltage drop at the Al/SiC interfaces and a guard ring structure confines the current within its boundary. With this simplified diode, it is possible to image BPDs present before stressing, track the growth of stacking faults with electrical stressing, and monitor the resulting forward voltage increase.

A New Method for Counting Micropipes in SiC Wafers: *Jianwei Wan*[1]; Seung-Ho Park[1]; Gilyong Chung[1]; Eric Carlson[1]; Mark Loboda[1]; [1]Dow Corning Corporation

Micropipes are considered to be a major device killer defect in SiC wafers; therefore, micropipe density becomes a figure of merit to characterize SiC wafer quality. However, how to count micropipes accurately has been a challenging and disputable task. In this paper, we present a new method of mapping and counting micropipes in SiC wafers, for both conductive and semi-insulating wafers. Based on molten KOH etching, polishing, and high resolution digital imaging, micropipes can be revealed on the scanned images of etched full wafers and counted by image analysis software. Independent of wafer size and polytype, this method is easy to implement and highly efficient for micropipe counting. It is also discovered that polishing etched wafers is critical to differentiate micropipes from other defects such as dislocations and obtain an optimal contrast on the scanned images to count micropipes accurately. A comparison of the etched SiC wafer scanned image and a Candela reflected light image was performed and a correlation was observed between the micropipe etch pits and features observed in the Candela image.

Identification of Polytypes in Sublimation Grown 4H-SiC Crystals by High Resolution X-Ray Diffractometry: *Dong Jie*[1]; Wang Li[1]; Hu Xiaobo[1]; Li Xianxiang[1]; Xu Xiangang[1]; Jiang Minhua[1]; [1]Shandong University

4H-SiC single crystal with a diameter of 1.5" has been grown by seed sublimation method. Polytypes in 4H-SiC crystal are assessed by high resolution X-ray diffractometry with the asymmetrical diffraction geometry. Multiple reflections are received from the rocking curve measurements of a longitudinal cut 4H-SiC slice. Those reflections are indexed to be 2 1 -3 1 and 2 1 -3 -1 of 4H-SiC,2 1 -3 1,2 1 -3 0,2 1 -3 1, 2 1 -3 -1, 2 1 -3 2 and 2 1 -3 -2 of 6H-SiC, 2 1 -3 1,2 1 -3 -2,2 1 -3 4, 2 1 -3 -5 and 2 1 -3 7 of 15R-SiC respectively based on the lattice constants of different polytypes in SiC crystal. It is believed that the polytypes in 4H-SiC crystal can be identified by high resolution X-ray diffractometry.

RPM4.Novel Characterization and Structures IV

Role of Oxygen in Growth of Carbon Nanotubes on SiC by Sublimation: *Weijie Lu*[1]; John J. Boeckl[2]; William C. Mitchel[2]; J. Rigueur[1]; W. E. Collins[1]; [1]Fisk University; [2]U.S. Air Force

Carbon nanotubes (CNTs) form when SiC decomposes in vacuum at high temperature. The CNTs grown on SiC are metal-free, well-aligned, and with few structural defects. In this study, CNT formation on SiC in both high vacuum (10-5torr) and ultra-high vacuum (10^{-8} torr) is examined. Multi-wall carbon nanotubes and graphitic structures are the main products on the SiC surface after annealing at 1400-1800°C at a pressure of $10,^{-5}$ torr. Raman spectra show that CNT growth is higher in high vacuum than in ultra-high vacuum, and this indicates that SiC decomposes in this process by oxidation. Two oxygen species are found in the CNT films by X-ray photoelectron spectroscopy (XPS). The angle-resolved XPS O_{1s} peak at 530.0 eV from C-O decreases with increasing take-off angle indicating that this oxygen species exists in the bulk of the CNT films. Only oxygen and carbon are found in the spectra, and the binding energy of this oxygen species in the CNT films is close to that of molecular O_2. It is argued that low oxygen pressure not only oxidizes SiC, but also interacts with the CNTs at high temperatures and promotes the formation of graphitic structures on SiC.

Thermodynamic Analysis of Synthetic Potentialities of the SiO_2-SiC Starting System; Synthesis of SiC (Nanowires, Nanotubes), Si, SiO.: *Roman G. Pavelko*[1]; Vladimir G. Sevastyanov[1]; Yurij S. Ezhov[2]; Nikolaj T. Kuznetsov[1]; [1]Kurnakov Institute of General and Inorganic Chemistry RAS; [2]Institute for High Energy Densities

The main goal of our research was to perform thermodynamic analysis of SiO_2-xSiC system (x = 0.1-3), determine its synthetic potential, and use the SiO_2-xSiC starting system for production of different forms of SiC. Thermodynamic scanning of the SiO_2-xSiC starting system was accomplished in wide pressure (1-10^{-8} atm) and temperature (800-2500°K) ranges, and for different component ratios x=0.1-3. For each pressure value we found the temperature intervals, optimal for synthesis of SiO (g) and Si (g). Based on the obtained data, threadlike SiC crystals (nanowhiskers) were synthesized.

Step-by-step thermodynamic modeling of SiC synthesis allowed us to propose the scheme and conditions of crystal growth. It was found that SiC transport, proceeding according to the following reaction, is the governing process for the formation of threadlike crystals: $SiC_{(initial)} + SiO_{(g)} = 2Si_{(g)} + CO_{(g)} = SiC_{(whiskers)} + SiO_{(g)}$ Optimum conditions (T, p) of synthesis of threadlike SiC crystals were determined. Direct synthesis of SiC nanotubes was performed from a gas phase via evaporation of silicon under CO atmosphere according to the following reaction: $2Si_{(g)} + CO_{(g)} = SiC_{(NT)} + SiO_{(g)}$ The obtained samples of SiC were investigated by X-ray, IR methods, atomic force microscopy, scanning and transmission electron microscopy.

RPM5.Related Materials IV

Structural Characteristics of InGaN/GaN Multiple Quantum Wells Grown on Sapphire by Metalorganic Chemical Vapor Deposition: *Hung-Ling Tsai*[1]; Jer-Ren Yang[1]; Zhe Chuan Feng[1]; Alan Gang Li[2]; W. Lu[3]; W. E. Collins[3]; [1]National Taiwan University; [2]ShenZhen Fangda GuoKe Optronics Technical Co. Ltd; [3]Fisk University

InGaN-GaN MQW LED wafers were grown on (0001)-plane sapphire substrates by low pressure (LP) MOCVD using several Emcore systems with the vertical growth configuration and a high speed rotation disk, i.e. the so-called Turbo-disc technology, for a wide range of blue, blue-green and green light emission device application. The compositions and sizes within QWs were designed according to the requirements on the LED performance. Analytical techniques of high-resolution (HR) X-ray diffraction (XRD) and transmission electron microscopy (TEM) have been employed to investigate their structural properties. High quality of MQW wafers have been achieved and evidenced with excellent characteristics. XRD data showed that the GaN peak is very sharp and all satellite bands are narrow. XRD multiple satellite peaks are up to 10th order due to the quantum well superlattice confinements and fine fringe structures among satellite peaks. TEM confirmed the sharp MQW structures and dimensional parameters, and revealed threading dislocation, which were formed from the big lattice misfit between the GaN and sapphire. Threading dislocation would disrupt the InGaN/GaN MQWs and initiate the V-defects which have inverted hexagonal pyramid-shaped {10-11} side walls.

Studies of UV and Blue Light Emitting Diodes Prepared by Metalorganic Chemical Vapor Deposition: J. H. Chen[1]; Zhe Chuan Feng[1]; H. L. Tsai[1]; J. R. Yang[1]; *A. Parekh*[2]; E. Armour[2]; P. Faniano[2]; [1]National Taiwan University; [2]Veeco TurboDisc Operations

InGaN/GaN single and multiple quantum-well (QW) blue and UV light-emitting- diode (LED) structures have been grown on sapphire substrates by metalorganic chemical vapor deposition (MOCVD) TurboDisc technology. The In-composition, layer parameters and the QW-related satellite features of these samples were characterized by high resolution X-ray diffraction measurements. In the photoluminescence spectrum at 9K, the peak of the 4-QWs blue LED structure at 2.702eV is interpreted from the InGaN quantum well and the emission band near 3.284eV from p-type GaN. The full width at half maximum of the main emission peak is about 88meV, indicating the high quality of the sample. From the temperature-dependent photoluminescence measurements, when the temperature was increased from 9 to 300K, the red-shift was about 44meV. From the excitation power dependence photoluminescence measurements of the SQW blue LED structure, when the excitation power was increased from 0.2 to 33.6mW, the emission energy shows a blue-shift (40meV). One refers to the piezoelectric field-induced quantum confined Stark effect, and another is related to the band-tailing effect, due to the self-organized small In-rich regions. The In-rich clustering in nitride-based alloys is favorable for increased luminescence efficiency due to dominating capture of excess carriers to clusters and recombination there.

Material Properties of GaN Films Grown on SiC/SOI Substrate: J. B. Wang[1]; Zhe Chuan Feng[1]; *C. Tran*[1]; J. Zhao[2]; W. Lu[3]; W. E. Collins[3]; [1]National Taiwan University; [2]Tianjin Normal University; [3]Fisk University

Materials investigation of metalorganic chemical vapor deposition (MOCVD)-grown GaN thin films on SiC/SOI substrates is reported. The SiC/SOI substrates were obtained through the conversion of Si/SOI wafer, consisting of a thin Si (111) layer (~100 nm) and a 1 mirco meter SiO2 layer on Si (100) substrate, by carbonization of the thin Si layer using rapid thermal CVD with mixtures of propane (C3H8) and H2 at atmosphere pressure. The top layer was evidenced by X-ray diffraction (XRD) to be the (111) 3C-SiC. The MOCVD growth of GaN on (111) 3C-SiC/SOI was performed by the similar procedure for the GaN growth on sapphire. Raman scattering measurements were performed on a series of MOCVD grown GaN films on SiC/SOI and other comparative substrates of sapphire, 6H-SiC and BaF2/GaAs. Their Raman spectra exhibited a sharp E2 mode at 568 cm^{-1}, characteristic of wurtzite (w-) GaN together with XRD and photoluminescence measurements. It shows also the W-GaN forbidden A1(TO) mode at 532 cm^{-1} and a shoulder at 522 cm^{-1} from Si. More comparison are given on Raman spectra from MOCVD-grown GaN/SiC-SOI samples with different GaN layer thickness and grown on different substrates, the differences of which reveal their material structural features.

RPM6.Surfaces and Interfaces IV

On the Estimation of the Heterostructures Characteristics for 3C-SiC/2H, 4H, 6H, and 8H-SiC: *Alexander Lebedev*[1]; [1]A.F. Ioffe Physico-Tekhnical Institute, Russian Academy of Science

The basic heterostructurs characteristics are the band offsets ΔE_c and ΔE_v for the conduction and valence bands accordingly and the subband center energies ε_0 for the corresponding quantum-wells (energy zero is at the bottom of the well). Here we estimate these parameters for the heterostructures formed by the 3C and NH, where N =2, 4, 6, 8. Within the Shockley-Anderson model value of ΔE_c is determined by the semiconductor electron affinities χ(3C) and χ(NH). Unfortunately, electron affinities are studied rather poorly. Therefore, we put, $\chi(NH) = \chi(3C) - aD$ where $D = n_k/(n_k + n_h)$ is the hexogonality (n_k and n_h are the numbers of the cubic and hexagonal sites), a is a coefficient. Then ΔE_c aD. If we take $\Delta E_c = 0.55$ eV [1], we get □ ≈ 1.67 eV. Calculation shows that for the all polytypes (except 2H) values of $\Delta E_v = E_g(NH) - E_g(3C) - \Delta E_c$ are less than 0.05 eV (E_g is the energy gap). For 2H we have $\Delta E_v = -0.70$ eV. Using for the interface of 3C/6H experimentally determined value of $\varepsilon_0 = 0.060$ eV [1] and estimating the value of the maximum contact potential difference, we find for the triangular quantum-well the values of $\varepsilon_0 = 0.059, 0.062$ □ 0.066 eV for □□□ 8□, 4□, and 2□ correspondingly.

A Study of Inhomogeneous Schottky Diodes on n-Type 4H-SiC: *Daniel J. Ewing*[1]; Lisa M. Porter[1]; Quamar Wahab[2]; Leonard J. Brillson[3]; Sergey Tumakha; Tangali S Sudarshan[4]; Xianyun Ma[5]; [1]Carnegie Mellon University; [2]Linkoping University; [3]Ohio State University; [4]University of South Carolina; [5]MaxMile Technologies, LLC

In this study we performed a statistical analysis of 500 Ni Schottky diodes distributed across a 2-inch, n-type 4H-SiC wafer with epilayer. Nickel diodes were patterned onto the substrate after sacrificial oxidation and LPCVD oxide deposition and patterning. Current-voltage measurements showed dramatic differences among the diodes within this sample. Approximately 10% of the diodes showed a double-barrier characteristic in the room-temperature log I vs. V plot. Modeling reveals that all of the diodes contain a high 'ideal' barrier of ~1.4 eV, whereas the double-barrier diodes also contain a low barrier with an effective $\phi_B = 0.4$ eV and with an area <1% of the total diode area. The source(s) of these variations was investigated using a variety of spectroscopic and imaging techniques. Analyses of X-ray topographic (XRT) and polarized light microscopy (PLM) images revealed no correlations with screw dislocations or micropipes. In contrast, deep level transient spectroscopy (DLTS) and depth resolved cathodoluminescence (DRCLS) indicate that certain point-defect states are associated with the observed electrical variations. Specifically, DRCLS shows specific emissions (2.20 and/or 2.65 eV) that are not present in the near-ideal diodes and that correlate with the degree of non-ideality.

Where Would the Electronic States of a Small Graphite-Like Carbon Island Contribute to the SiC/SiO2 Interface State Density Distribution?: *Peter Deák*[1]; [1]University of Paderborn

A crucial problem for manufacturing SiC-based MOS devices is that thermal oxidation produces a high density of interface traps, Dit(E), in the band gap of SiC. which rises towards both band edges with some distinct features in the gap. In a recent theoretical study, we have shown that isolated C–C and C=C bonds at the interface can explain the observed deep states in the Dit(E). In this paper we investigate whether aromatic carbon bonds, i.e., graphite-like nanoparticles could give rise to the continuous "background" component of Dit(E) rising towards the band edges. Our model of a graphite-like precipitate at the interface consists of 19 carbon atoms, with a diameter of ~7 Å. Such a unit would already be observable experimentally. The electronic structure, calculated by the use of a hybrid functional in density functional theory (correctly reproducing the band gap of SiC), shows only occupied states in the band gap of 4H-SiC, near the valence band edge. Based on this result we believe that – besides the deep states – carbon excess at the interface can only explain the interface hole traps near the valence band edge but not the electron traps near the conduction band.

Real Time Observation of SiC Oxidation using In-Situ Spectroscopic Ellipsometer: *Kouichi Kakubari*[1]; Ryouichi Kuboki[1]; Yasuto Hijikata[1]; Hiroyuki Yaguchi[1]; Sadahumi Yoshida[1]; [1]Saitama University

We have observed in real time the oxidation of SiC using in-situ spectroscopic ellipsometer for the first time. We applied the SiO_2-interface-SiC model to analyze the polarization parameters (Ψ,Δ). Taking into consideration a ~1nm interface layer with a high refractive index, the oxidation time dependence of (Ψ,Δ) was successfully analyzed. The oxide thickness as a function of oxidation time was obtained from the real-time measurements to compare with previous reports using ex-situ measurements. The linear and parabolic rate constants obtained in this study were considerably different from those reported previously based on ex-situ measurements. This is mostly due to the measurement accuracy of the oxide thickness at the initial stage of oxidation. As a result, we can determine more accurately *B/A*, in particular, which corresponds to the initial oxidation rate constant taking advantage of the in-situ

and real-time measurement. We have also derived the activation energies from the temperature dependence of the oxidation rates to discuss the mechanism of SiC oxidation.

Transmission Electron Microscope Observations of 4H-SiC Schottky Barrier Diodes Containing p-Buried Floating Junction: *Johji Nishio*[1]; [1]Corporate R&D Center, Toshiba

The structural analysis by transmission electron microscope (TEM) observation and selected area electron diffraction (SAED) of the 4H-SiC Schottky barrier diode (SBD) with the floating junction structure (Super-SBD) was carried out. It was found that the overgrown layer does not have larger dislocation density or more severe disorder of the lattice spacing than the first epilayer, even where the Al-ion was implanted to form p-buried region below. These results may provide good support for the principal verification of the 4H-SiC Super-SBD, indicating the crystal quality of the overgrown drift layer is acceptable for a high-voltage resisting structure.

4:10 PM Coffee Break

RC1.Vibrational and Optical Properties

Thursday, 4:30-6:00pm
September 22, 2005

Room: Allegheny Ballroom I
Location: Westin Pittsburgh

Session Chairs: W. J. Choyke, University of Pittsburgh; S. Yoshida, Saitama University and AIST

4:30 PM Invited
Phonons in SiC from INS, IXS, and Ab-Initio Calculations: *Dieter Strauch*[1]; [1]Regensburg University

In non-magnetic, non-conducting, non-defective solids the thermal properties stem from phonon excitations. Since a good dozen of years, the old ball-and-spring models have been overcome by rather reliable quantum-mechanical calculations. While the main interest in SiC is in the electronic properties, the aim of this contribution is to spread some familiarity of the recently developped advances in phonon physics and to report some recent experimental determinations of phonon dispersion curves of 3C- and 4H-SiC from inelastic x-ray (IXS) and neutron scattering (INS) experiments.

5:00 PM
High Energy Local Vibrational Modes of Carbon Aggregates in SiC: Experimental and Theoretical Insight: *Alexander Mattausch*[1]; Michel Bockstedte[1]; Oleg Pankratov[1]; John W. Steeds[2]; Suzanne Furkert[2]; Jonathan M. Hayes[2]; Wayne Sullivan[2]; Nick G. Wright[3]; [1]Universität Erlangen-Nürnberg; [2]University of Bristol; [3]University of Newcastle

While it is recognized that clustering of carbon interstitial atoms is a common process occurring during the annealing of irradiation damage of SiC, convincing agreement between theoretical models and experimental results obtained by low temperature photoluminescence (PL) spectroscopy has yet to be achieved. In particular, local vibrational modes (LVMs) have been reported with energies considerably higher than those calculated for likely atomic models. PL experiments performed on ^{13}C enriched 6H-SiC samples have also revealed splittings of these LVMs that are three-fold for the highest energy modes but more complex for lower energy modes. The models that are investigated theoretically are carbon aggregates that span several lattice sites or that consist of a number of carbon atoms substituting for one site. Although it is not evident from the defect configurations, the highest mode of a couple of aggregates corresponds to a stretching vibration of a single carbon pair, as demonstrated for the triangle-shaped tri-carbon antisite $(C_3)_{Si}$. These findings explain the threefold splittings observed in ^{13}C enriched samples. The high thermal stability of these defects indicates their importance for further defect reactions.

5:15 PM
Origin of the Up-Conversion Process in 4H SiC: *John Steeds*[1]; Suzanne Furkert[1]; Wayne Sullivan[1]; Gunter Wagner[2]; [1]University of Bristol; [2]IKZ

It was discovered some time ago[1] that the photoluminescence spectra generated by 488nm excitation extended to much shorter wavelength so that the optical centres produced were as much as 0.5eV more energetic than the incident photons. Moreover, the spectra generated were continuous across the notch filter used to attenuate the back-scattered laser beam indicating that the same excitation processes operating at shorter wavelength were also responsible for the longer wavelength excitation, at least in the vicinity of the notch. We have now made a systematic investigation of this effect, using samples electron-irradiated in an ion-free transmission electron microscope. The electron beam had a circular top-hat profile with a diameter of about 100µm. Spectra obtained both within the irradiated area and outside it have been compared after excitation by the 488nm laser beam and also by a 325nm laser beam (above band-gap). Apparent spatial distributions of some of the centres were quite different. It has been concluded that indirect excitation processes are occurring involving independent deep centres. These centres do not themselves emit photons and once they are removed by high temperature annealing the excitation process changes completely.[1]J. W. Steeds et al, Mater Sci Forum, **353-356** 381 (2001).

5:30 PM
Temperature and Intensity Dependent Carrier Lifetime Measurements on n- and p-Type 4H-SiC Measured by Different Experimental Techniques: *Jawad Ul Hassan*[1]; Karolis Neimontas[1]; Peder Bergman[1]; Erik Janzén[1]; [1]Linköping University

Carrier lifetime is important in SiC both as a parameter in bipolar devices, and as characterization property showing the quality of any epitaxial layer. In this work we have used Hot-Wall CVD epitaxy, to grow thick layers of p- and n-type doping, with doping ranging from low 1013 cm^{-3} to 1018 cm^{-3}. Measurements have been performed as a function of temperature and excitation densities. Different optical experimental techniques have been used. In addition some samples have been processed for devices to be measured using electrical techniques such as reverse recovery measurements, and open voltage circuit decay. For all samples the measured decay using all optical techniques shows an expected exponential decay over several orders of magnitude. The observed carrier lifetime ranges from 0.6 µs to 1.0 µs between the different samples. The temperature dependence of the carrier lifetime shows a continuous increase with increasing temperature. The measured carrier lifetimes shows a slight decrease with increasing excitation density. For n-type samples the FCA measurements shows generally a higher value as compared to the luminescence techniques. In p-type samples no such difference is observed. The PL decay measurements have also been used for high resolution mapping over entire SiC wafers.

5:45 PM Invited
Electronic Raman Studies of Shallow Donors in SiC: *Martin Hundhausen*[1]; R. Püsche[1]; L. Ley[1]; [1]University Erlangen

Electronic Raman scattering from shallow donors in silicon carbide has been studied in the past only for Nitrogen. Polytype dependent Raman peaks with energies between 3meV and 80meV have been assigned to the valley orbit splitting of the 1s ground state of donors occupying inequivalent lattice sites in the crystal, i.e. hexagonal and cubic sites[1,2]. We extend work here to phosphorous doped SiC. 4H-, 6H- and 15R-SiC doped with P (concentration ~ $1018cm^{-3}$) as well as SiC co-doped with P and N were investigated. In our setup, we are able to detect transitions with Raman shifts down to 8 cm^{-1} (1meV). Sample spectra of polytypes co-doped with N and P are shown in the figure with the impurity responsible for the observed signals indicated. The disappearance of the marked peaks due to depletion of the shallow donor states at higher temperature proves the electronic origin of these signals. Spectra taken at higher Raman shift show that electronic transitions around 80meV do exist only for the Nitrogen donor, whereas P-doped samples don't show such higher energy transitions. [1]J. Colwell and M.V. Klein, Phys. Rev. B6, 498 (1972). [2]S. Nakashima and H. Harima, Phys. stat. sol. (a) 162, 39 (1997).

RC2.Contacts

Thursday, 4:30-6:00pm
September 22, 2005

Room: Allegheny Ballroom II & III
Location: Westin Pittsburgh

Session Chairs: M. A. Capano, Purdue University; C. Brylinski, Thales

4:30 PM Invited
Development of Ohmic Contact Materials for p-Type 4H-SiC: *Masanori Murakami*[1]; Susumu Tsukimoto; [1]Kyoto University

Development of thermally stable, low resistance ohmic contacts to p-type 4H-SiC was one of key technical issues to develop high power SiC devices. Since the ohmic contacts to SiC are fabricated by a conventional DA technique (depositing metals and subsequent annealing), metallurgy (i.e. Chemical reaction, diffusion, microstructure) at the contact/SiC interfaces has strong influence on the contact properties such as the contact resistance, thermal stability, surface morphology etc.. However, it was extremely difficult to control the metallurgy at the interfaces to provide the desirable contact properties. This was a main reason why the p-type contacts were fabricated empirically on a trial-and-error basis. In the present talk, we will, first, review the p-type ohmic contact materials developed based on the empirical guideline of selecting the contact elements which reduced the barrier height at the metal/SiC interface or doped heavily in SiC. Then, recent progress of ohmic contact materials developed using transition metals is reviewed. The reason

why the transition metal contacts provided low contact resistance and high thermal stability will be given based on our observation by cross-sectional high-resolution transmission electron microscopy.

5:00 PM
Comparison of Electrical Characteristics of 4H-SiC(0001) and (000-1) Schottky Barrier Diodes: *Tomonori Nakamura*[1]; Toshiyuki Miyanagi[1]; Isaho Kamata[1]; Hidekazu Tsuchida[1]; [1]Central Research Institute of Electric Power Industry

We compared the electrical characteristics of 4H-SiC{0001} Schottky barrier diodes (SBDs) and their annealing dependence. Schottky barrier heights (ϕ_bs) of as-deposited Mo and W contacts on (0001) are 1.07 eV and 1.19 eV, while those of (000-1) are significantly higher at 1.39 eV and 1.32 eV, respectively. After annealing at 700ºC, the ϕ_bs of Mo and W Schottky contacts on (0001) become 1.25 eV and 1.06 eV, and those of (000-1) reach 1.47 eV and 1.40 eV. No degradation of ideality factors was observed after annealing at 700°C. We also tested large as-deposited Mo{0001} SBDs, and the percentages of those with small leakage were compared. The percentages of the (0001) SBDs with a leakage current density below 1 x 10^{-6} cm^2 at 150V (0.52 MV/cm) were 93.3% for 0.25 cm^2, 85.7% for 0.5 cm^2, and 66.7% for 1 cm^2 active area. The percentage of the (000-1) SBDs was 71.1% for 0.25 cm^2. The average densities of catastrophic defects were estimated to be 0.3 cm^{-2} for (0001) and 1.4 cm^{-2} for (000-1). We demonstrated 1 cm^2 Mo(0001) SBDs with no significant excess current in the forward characteristics and a low leakage current below 1 x 10^{-6} A at –300V.

5:15 PM
Nanoscale Deep Level Defect Correlation with Schottky Barriers in 4H-SiC/Metal Diodes: *Sergey Tumakha*[1]; Leonard J. Brillson[1]; Daniel J. Ewing[2]; Lisa Porter[2]; [1]Ohio State University; [2]Carnegie Mellon University

We have used depth-resolved cathodoluminescence spectroscopy (DRCLS) techniques to correlate double barrier current-voltage (I-V) characteristics with deep level emissions across an array of Ni/4H-SiC diodes on the same epitaxial wafer. The results demonstrate not only a correspondence between the localized states near Ni/SiC junctions and measured barrier heights, but they also suggest that such states limit the range of SB heights in general. DRCLS of the near-ideal diode shows a broad deep level emission at 2.45 eV common to all diode areas and associated with either impurities or inclusions. For marginally non-ideal diodes, we observe the presence of additional defect features, primarily at 2.65 eV. For strongly non-ideal diodes, DRCLS reveals the appearance of a third defect emission at 2.2 eV. Polarized light microscopy and X-ray topography characterization of all diodes on the 2" wafer reveal dislocations, micropipes, high stress areas and dislocation walls in the footprints of many contacts. However, there is no correlation between the appearance of such defects and the presence of second barrier in I-V characteristics of individual diodes. The CL observation of defect levels transitions that correlate with the non-ideal SB's suggest that these sub-surface defect features can be used to predict SB behavior.

5:30 PM
An Approach to Improving n-SiC Ohmic Contacts Using Secondary Contacts: *Matthew H. Ervin*[1]; Kenneth A. Jones[1]; Unchul Lee[1]; Mark C. Wood[1]; [1]U.S. Army Research Laboratory

Nickel (Ni) contacts are the most widely used ohmic contacts to n-type silicon carbide. Unfortunately, while these contacts have good electrical properties, the physical contact, and therefore the reliability, can be poor. An approach is described for using the good electrical properties of Ni ohmic contacts while using another metal for its superior mechanical, thermal or chemical properties for the chosen application. In the present work, once the Ni contacts have been annealed forming nickel silicides and achieving low contact resistance, they are etched off. Removal of the primary Ni contacts also removes the poor morphology, voids, and at least some of the excess carbon produced by the Ni/SiC reaction, which may cause poor reliability. The Ni contacts are then replaced by a secondary contact metal chosen for its desired properties. This secondary metal displays low contact resistance as deposited, indicating that the critical feature responsible for the ohmic contact has not been removed by the primary contact etch. Not only does this approach provide more flexibility for optimizing the contact for a given application, it also provides some insight into the ohmic contact formation mechanism.

5:45 PM
Ohmic Contacts to p-Type Epitaxial and Implanted 4H-SiC: *John Crofton*[1]; John R. Williams[2]; Adetayo Victor Adedeji[2]; J. D. Scofield[3]; [1]Murray State University; [2]Auburn University; [3]Air Force Research Laboratory

Ohmic contacts to p-type epitaxial and heavily implanted SiC will be described. Results for Al-Ti contacts to epitaxial material as a function of operating temperature will be presented. Results for Ni contacts to both epitaxial and implanted material will also be presented. Elevated temperature measurements of specific contact resistance for Ni contacts are presented and compared to theoretical calculations. The theoretical calculations require both the acceptor doping concentration and the contact's barrier height. Epitaxial material has a known acceptor value thereby allowing the barrier height to be deduced by requiring agreement between the calculated and measured values of the specific contact resistance. Calculations of specific contact resistance for the implanted material use the barrier height from the epitaxial results along with a variable activated acceptor doping concentration which is adjusted to give agreement with measured room temperature specific contact resistances. Specific contact resistances as low as 8x10-6 ohm-cm2 have been obtained to epitaxial p-type material whereas contacts to implanted material result in much larger contact resistance values of 4x10-5 ohm-cm2. These results give predicted values of activated acceptor doping concentrations in heavily implanted material to be on the order of 2% of the implant concentration.

FA1.Surfaces, Interfaces and Planar Defects

Friday, 8:30-10:15am
September 23, 2005

Room: Allegheny Ballroom I
Location: Westin Pittsburgh

Session Chair: P. Deak, Budapest University of Technology and Economics; U. Gertsmann, University of Paderborn

8:30 AM
The SiO2/SiC Interface: Abruptness, Oxygen and Hydrogen Incorporation: *Fernanda Chiarello Stedile*[1]; Gabriel Vieira Soares[1]; Priscila Schütz[1]; Fabiane Trombetta[1]; Israel Baumvol[2]; Cláudio Radtke[3]; [1]UFRGS; [2]UCS; [3]CEA

We observed previously that dry thermal oxidation of SiC and of Si produced similar SiO2 films in the near surface and bulk regions for both semiconductors. However, the amount of 18O incorporated in the near interface region from a second oxidation performed in 18O enriched O2 gas, following a previous one in 16O2, was always smaller in the case of SiO2/SiC samples as compared to those of SiO2/Si, in which the concentration of 18O was equal to the isotope enrichment of the gas. Now we prepared symmetric samples of SiO2/SiC and SiO2/Si oxidized either in 18O2/16O2 or in 16O2/18O2 gas sequences in order to determine the presence of O from each oxidation in the interfacial region. 18O profiles determined by nuclear reaction techniques were used. Results indicate that, in the case of SiO2/SiC samples, both O isotopes are present in this region. The effect of temperature of the second oxidation step and the role of carbonaceous species formed during oxidation were also investigated, evidencing a more gradual SiO2/SiC interface as compared to the SiO2/Si, and allowing us to propose an oxidation model. Besides, preliminary results of hydrogen incorporation by thermal treatment in D2 at this interface will be also presented.

8:45 AM
Experimental and First-Principles Studies of the Electronic Properties of HfO_2 on 4H-SiC: *Carey M. Tanner*[1]; Jongwoo Choi[1]; Jane P. Chang[1]; [1]University of California, Los Angeles

Ultrathin HfO_2 films were demonstrated to be a viable high-k; gate dielectric alternative to SiO_2 for use in 4H-SiC power MOSFETs. HfO_2 films were deposited on n-type 4H-SiC (0001) by atomic layer deposition. Amorphous and polycrystalline HfO2 films were grown at 275°C and 330°C, respectively. The band alignment at the HfO_2/SiC interface was investigated by x-ray photoelectron spectroscopy and photoconductivity measurements. These results are compared to density functional theory (DFT) calculations of a monoclinic HfO_2/4H-SiC interface, where SiC (0001) was terminated at the interface with either Si or C atoms for comparison. The Si-terminated (C-terminated) structure resulted in valence and conduction band offsets of 2.09 eV (1.47 eV) and 0.35 eV (0.97 eV), respectively. Conductive atomic force microscopy (AFM) measurements were performed to evaluate the leakage current and breakdown voltage of the dielectric. Capacitance-voltage and current voltage measurements were performed on Al/HfO_2/SiC capacitors fabricated by standard lithographic methods. The interface density of states is compared to recent SiO_2/SiC results.

9:00 AM
Investigation of Mechanical Stress Induced-Double Stacking Faults in (11-20) N-Doped 4H-SiC Combining Optical and Transmission Electron Microscopy, Contrast Simulation and Dislocation Core Reconstruction: *Maryse Lancin*[1]; Hosni Idrissi[1]; Gabrielle Regula[1]; Joël Douin[2]; Bernard Pichaud[1]; [1]Paul Cézanne University; [2]CEMES

We study the defects created in highly N-doped 4H SiC by mechanical stresses. They are introduced by scratching the (11-20) sample surface. The samples are annealed at 550°C and 700°C according to two procedures: with or without an additional external stress. For all samples, optical micrographs after chemical etching of the surface immediately reveal that the defects are stacking faults expanding asymmetrically from the sources. A combination of various techniques allows a full characterization of these defects. They consist of double stacking faults (DSFs) dragged by two Sig. The latters were found

to lay in or next to Peierls valleys. Three kinds of DSFs can be categorized by their propagation direction from the scratch, their Burgers'vector and their type of glide plane pair. Their line directions exhibit some differences depending on the procedure. These results sustain the hypothesis of Pirouz et al. on the higher mobility of Sig and 90°Sig as compared to Cg and 30° Sig respectively. By drawing up an inventory of the partial dislocations in each process, we discuss why only some of the possible partial dislocations are observed in terms of electronics, thermodynamics, dislocation dynamics and mechanics.

9:15 AM
Investigation of Basal Plane Dislocations in 4H-SiC Epilayers by X-Ray Topography: *S. Ha*[1]; Y. Hanlumyuang[1]; C. H. Chou[1]; V. Rodriguez[1]; Xuan Zhang[1]; M. Skowronski[1]; J. J Sumakeris[2]; M.J. O'Loughlin[2]; [1]Carnegie Mellon University; [2]Cree Inc.

Plan-view transmission x-ray topography was used to investigate the configuration of basal plane dislocations in thick (*d*~100μm) 4H-SiC CVD epilayers. Four types of basal plane dislocations were distinguished based on their morphologies visible in x-ray topographs. Type I are straight dislocation lines perpendicular to the off-cut direction; Type II are half loops, nucleating in the volume of epilayer and expanding to the epilayer/substrate interface; Type III are circular loops originating around point sources; Type IV are short dislocation segments along the off-cut direction. For each type of the basal plane dislocations, their Burgers vectors and locations in the epilayers were also determined.

9:30 AM
Investigation of Structural Stability in 4H-SiC Structures with a Heavy Ion Implanted Interface: *Augustinas Galeckas*[1]; Anders Hallén[1]; Adolf Schöner[2]; Jan Linnros[1]; Pirouz Pirouz[3]; [1]Royal Institute of Technology; [2]Acreo AB; [3]Case Western Reserve University

Recent studies show that the epilayer-substrate interface region constitutes a major source for nucleation of stacking faults (SFs) and therefore must be considered as a key factor in controlling the structural degradation problem in 4H-SiC. In this work we investigate the possibility of controlling formation of SFs at the interface region by implanting the 4H-SiC substrate with low-energy antimony ions (75 keV Sb+) prior to conventional CVD growth of the homoepitaxial layers. This approach is based on the well-established solid-solution hardening concept, according to which interaction of impurity atoms with dislocations makes the motion of the latter more difficult. PL imaging spectroscopy is employed to investigate incorporation of Sb+ implants at the buried interface and also to assess its impact on structural degradation. Spectral results are analyzed considering both the onset of n-type doping and irradiation damage. The latter factor was estimated separately from supplementary measurements of high-energy (2.5 MeV) proton-irradiated 4H-SiC epilayers. We compare results of optically stimulated SF formation in virgin and Sb implanted regions and provide a comprehensive picture of the defect evolution, including microscopic details of the imminent nucleation sites.

9:45 AM
Ordered Nanofacets on Vicinal SiC Surfaces Induced by Facet-Facet Interactions - An Implication to Substrate Off-Angles: Masahiro Fujii[1]; *Satoru Tanaka*[1]; Hiroyuki Kinoshita[2]; Hiromu Shiomi[2]; Akira Ishii[3]; Ikuo Suemune[1]; [1]Hokkaido University; [2]SiXON Corp.; [3]Tottori University

It has been increasing much attention to surface science in SiC because of its critical roles in determining interfacial trap states in electronic devices. Surface structures, chemistry, and morphology should be studied to elucidate their effects on device characteristics. We have found self-ordering of nanofacets on vicinal SiC surfaces after high temperature H2 etching and discussed the physics behind[1]. In this study, we try to demonstrate optimal vicinal surface structures that may drastically improve device performance. Based upon the periodicity of nanofacets and structural fluctuation observed we obtained a criterion which could predict ideal/perfect nanofacet structures, i.e. the idealistic surface structure is a cross product of a proper off-angle of SiC substrate and a characteristic periodicity simply determined by facet-facet interactions. Those are acting on next neighboring nanofacets due to minimization of surface free energy and uniquely stabilize nanofacet structures with a specific distance, a characteristic periodicity. We will discuss the characteristic periodicity by means of experimental and theoretical approaches and finally suggest idealistic off-angles in both 4H and 6H-SiC substrates, giving rise to perfectly ordered nanofacet surfaces. [1]H. Nakagawa, S. Tanaka, and I. Suemune, Phys. Rev. Lett. 91, 226107 (2003).

10:00 AM
SiC Pore Surfaces: Surface Studies of 4H-SiC(1-102) and 4H-SiC(-110-2): W. Y. Lee[1]; *Ulrich Starke*[1]; S. P. Rao[2]; S. E. Saddow[2]; R. P. Devaty[3]; W. J. Choyke[3]; [1]Max-Planck-Institut für Festkörperforschung; [2]University of South Florida; [3]University of Pittsburgh

Porous SiC has shown intriguing perspectives for a variety of possible applications in electronics, sensors, fuel cells and bio-technology. One important pore type found is a triangular shaped channel with surfaces inclined by about 62° with respect to SiC(0001). The respective single crystal surface, 4H-SiC(-110-2), and its isomorphic opposite, i.e. the 4H-SiC(1-102) surface have been studied in this work using atomic force microscopy (AFM), low-energy electron diffraction (LEED) and Auger electron spectroscopy (AES). The mechanically polished samples were etched in hydrogen flux at about 1500°C which eliminates the polishing damage as monitored by AFM. In addition this yields an ordered surface of bulk-like periodicity as deduced from LEED. An apparent thin oxide layer termination is inferred from AES. For the (1-102)-surface, further annealing in ultra-high vacuum leads to the removal of oxygen after flashing to about 1200°C. Si deposition and subsequent annealing lead to a well ordered surface with the best LEED pattern obtained after about 970ºC heating. Also the Si/C composition ratio increases up to this temperature until it drops at higher temperatures. LEED spot intensity curves clearly indicate a different structure for the UHV treated surface as compared to the "as-etched" surface condition.

10:15 AM Coffee Break

FA2.EPI IV: Heteroepitaxy of Cubic Crystal Structures

Friday, 8:30-9:45am
September 23, 2005

Room: Allegheny Ballroom II & III
Location: Westin Pittsburgh

Session Chairs: E. Janzen, Linkoping University; H. Tsuchida, CRIEPI

8:30 AM
Molecular Beam Epitaxy of Cubic Group III-Nitrides on Free-Standing 3C-SiC Substrates: *Donat Josef As*[1]; Stefan Potthast[1]; Joerg Schoermann[1]; Shun Feng Li[1]; Klaus Lischka[1]; Hiroyuki Nagasawa[2]; Masayuki Abe[2]; [1]University of Paderborn; [2]HOYA Advanced Semiconductor Technologies Co., Ltd.

The absence of polarization fields in cubic III-nitrides may be advantageous for device applications, however, the metastability of the cubic phase imposes stringent conditions on growth procedure. Recently, high quality, bulk-like 3C-SiC substrates became available by HOYA Advanced Semiconductor Technologies Co., Ltd. On such 3C-SiC substrates molecular beam epitaxy (MBE) has been performed with the goal to improve significantly the structural perfection of cubic III-nitrides and to enhance the interface quality of layered structures like superlattices (SLs), distributed Bragg reflectors (DBRs) and multi quantum wells (MQWs). Experiments of the adsorption and desorption kinetics of metal (Al, Ga, In) layers on c-GaN revealed that optimum growth conditions exists when a constant 1 monolayer gallium coverage is established on the growing c-GaN surface. The presence of indium in sub-monolayer quantity resulted in a further decrease of the surface roughness. The improvement of the structural properties of cubic III-nitride layers and multilayers grown on 3C-SiC substrates is demonstrated by a) 1 μm thick c-GaN layers with a minimum x-ray rocking curve width of 16 arcmin, b) c-AlGaN/GaN and c-InGaN/GaN MQWs which showed four to five satellite peaks in X-ray diffraction, c) weakly damped oscillations of the RHEED intensity after growth interruption.

8:45 AM
Atomic Layer Epitaxy of $(Si_{1-x}C_{1-y})Ge_{x+y}$ Layers on 4H-SiC: *Jörg Pezoldt*[1]; Thomas Kups[1]; Petia Weih[1]; Thomas Stauden[1]; Oliver Ambacher[1]; [1]TU Ilmenau

For the improvement of device properties heterojunctions are of great importance. SiC exhibit different possibilities to form epitaxial heterostructures. One application of the β-SiC/α-SiC heterocomposition which allows the fabrication of chemical homogeneous heteropolytype structures. Another possibility consists in the growth of III-N materials on SiC. An alternative approach is the growth of ternary $(Si_{1-x}C_{1-y})Ge_{x+y}$ alloys on SiC. The epitaxial layers were grown on off axis 4H-SiC substrates by solid source molecular beam epitaxy in a temperature range between 750 and 950°C. Reflection high energy electron diffraction and transmission electron microscopy (TEM) investigations show that the grown epitaxial layer consists of 3C-$(Si_{1-x}C_{1-y})Ge_{x+y}$. Energy dispersive X-ray (EDX) analysis revealed a decrease of the Ge incorporation versus substrate temperature. This effect is due to the fixed Si/Ge ratio during the epitaxial growth. The Ge distribution within the 3C-$(Si_{1-x}C_{1-y})Ge_{x+y}$ was studied by monitoring EDX line scans during TEM investigations. The Ge profile was found to be nearly homogeneous. The carried out investigations by atomic location by channeling enhanced microanalysis allowed the conclusion that Ge is located mainly at C lattice sites.

9:00 AM
Relaxation Mechanism of the Defect-Free 3C-SiC Epitaxial Films Grown on Step-Free 4H SiC Mesas: *Hui Du*[1]; Marek Skowronnski[1]; Philip G. Neudeck[2]; Andrew J. Trunek[2]; D. J. Spry[2]; J. A. Powell[2]; [1]Carnegie Mellon University; [2]NASA Glenn Research Center

Cross-sectional transmission electron microscopy (TEM) was used to investigate the microstructure of the 3C-SiC films deposited on atomically flat (completely free of surface steps) 4H-SiC mesas arrayed across on-axis 4H-SiC substrates. The nominal layer thickness was 10 µm and was considerably larger than critical thickness determined by either Matthews and Blakeslee or People and Bean models. Threading dislocation densities determined by KOH etching were as low as $10^4 cm^{-2}$ and much below densities typical of relaxed heteroepitaxial layers. However, misfit dislocations with Burgers vectors of <11-20> were observed in planes parallel to the 3C/4H SiC interface. We propose a new relaxation mechanism where misfit dislocation half loops nucleate at mesa edges and glide along the atomically flat interface.

9:15 AM
Single-Domain 3C-SiC Epitaxially Grown on 6H-SiC by VLS Mechanism: *Maher Soueidan*[1]; Gabriel Ferro[1]; John Stoemenos[2]; E. K. Polychroniadis[2]; Didier Chaussende[3]; Felipe Soares[4]; Sandrine Juillaguet[4]; Jean Camassel[4]; Yves Monteil[1]; [1]Laboratoire des Multimatériaux et Interfaces; [2]Aristotle University of Thessaloniki; [3]INPGrenoble-CNRS; [4]Groupe d'Etude des Semiconduteurs

Vapour-Liquid-Solid (VLS) mechanism was applied to grow 3C-SiC epitaxial layers on 6H-SiC(0001) on axis, Si face substrate. Ge-Si melt was fed by propane at 1250°C for 1h. The surface morphology after growth is highly step bunched. No spiral growth was observed on any sample. The 3C-SiC polytype was identified on such layers by micro-Raman spectroscopy and confirmed by low temperature photoluminescence. Electron backscattering diffraction showed that the layer is single domain, i.e. the 3C-SiC material has only one orientation without any hexagonal inclusion. Cross section and plan view TEM investigations confirmed the absence of double positioning boundary in the layer. The only defects found were stacking faults (density of 4.103 cm^{-1}) which form at the interface and propagate through the layer. The single-domain layers grown in this study were homogeneous on the entire surface of 1x1 cm^2 sample. There is no doubt that identical result could be achieved on larger areas. In regards of these results, the VLS approach is very promising for growing single-domain 3C-SiC layers at relatively low temperature on 6H-SiC substrate.

9:30 AM
Structure Evolution of 3C-SiC on Cubic and Hexagonal Substrates: *Rositza Yakimova*[1]; Mikael Syväjärvi[1]; Reza G. Yazdi[1]; [1]Linkoping University

Progress in the crystal growth of 3C-SiC has been regarded as a key issue for epitaxy and device developments related to this polytype. We report on growth of 3C-SiC by sublimation process in vacuum with the aim to ultimately select conditions for single polytype growth of bulk crystals. The 3C polytype occurrence, growth mechanism and structure evolution have been in focus of the study. To gain understanding of the initial formation of the cubic polytype, growth was performed on various substrates, such as 6H- and 4H-SiC (on-axis and vicinal), as well as freestanding 3C-SiC (undulated) wafers. The vicinal substrates were chosen to have a small miscut in order to prevent preferable nucleation of hexagonal polytypes. The growth configuration used allowed a high growth rate, e.g. up to 180 µm/h, respectively very thick layers. The grown cubic polytype was confirmed by means of PL, LEED patterns and HRTEM. Despite the 3C polytype was better reproduced on the 3C wafers, 6H substrates may be preferable if the 3C nucleation is well controlled, which can be achieved by selecting the initial temperature ramp up and substrate orientation. This will limit the number of nucleation centers and decrease the defective boundaries.

9:45 AM Coffee Break

FBP.Plenary Session II

Friday, 10:45am-12:15pm
September 23, 2005

Room: Allegheny Ballroom II & III
Location: Westin Pittsburgh

Session Chairs: W. R.L. Lambrecht, Case Western Reserve University; H. McD. Hobgood, Cree, Inc.

10:45 AM Plenary
Si-SiO2 and SiC-SiO2 Interfaces for MOSFETS – Challenges and Advances: *Sokrates T. Pantelides*[1]; [1]Vanderbilt University

The Si-SiO2 interface has been at the heart and core of microelectronics. It is in fact the only semiconductor-insulator interface that has consistently met the stringent criteria for MOSFETs. Tunneling limits through ultrathin SiO2 gate dielectrics are now calling for "alternate dielectrics" but the prospects are still uncertain. For power devices, one needs an "alternate semiconductor" with a wide energy gap. SiC has been a top candidate, largely because its native oxide is also SiO2. Yet, the SiC-SiO2 interface is a poor cousin of Si-SiO2. This talk will highlight the differences and similarities between the two and recent experimental and theoretical advances in the oxidation process, interface bonding, the nature of intrinsic interface defects, defect passivation with nitrogen and/or hydrogen, channel mobilities, and the ultimate objective: devices. Collaborators: Vanderbilt U: L. C. Feldman, S. Dhar, K. McDonald, R. Weller, M. DiVentra, S. Wang, S. Kim, S. N. Rashkeev, A. Franceschetti, L. Tsetseris, R. D. Schrimpf, D. M. Fleetwood; Auburn U: J. R. Williams, G. Chung, S. R. Wang, A. C. Ahyi, T. Isaacs-Smith, C. C. Tin; Purdue U: J. Cooper; Oak Ridge National Lab: S. J. Pennycook, G. Duscher, K. Van Benthem.

11:25 AM Penary
Energy Efficiency: The Commercial Pull for SiC Devices: *John W. Palmour*[1]; [1]Cree, Inc.

As SiC RF and power devices have become commercially available, a common theme for their adoption is the system efficiencies that they can enable. In the RF arena, broader bandwidths are required for power amplifiers to enable higher data rates. SiC MESFETs up to 60 Watts are now commercially available which allow unprecedented bandwidths to be achieved efficiently. These devices also offer the highest reliability among the wide bandgap RF devices being developed. Power devices in SiC offer very significant efficiency gains over silicon devices. The first devices being manufactured in volume are SiC Schottky diodes, which are replacing Si PiN diodes in switch-mode power supplies, and are emerging in applications for motor controls and hybrid electric vehicles. These devices show tremendous advantages over silicon in terms of lower switching losses, higher temperature operation, higher switching frequency and improved efficiency. The potential for SiC power switches such as MOSFETs and BJTs are equally exciting for achieving further improvements in efficiency. Examples of progress in the development of SiC power devices, as well as circuit demonstrations of their efficiency and potential markets will be discussed. With energy usage and costs rapidly increasing, higher system efficiencies will drive SiC device demand.

12:05 AM Closing Remarks and Adjournment

2005 International Conference on Silicon Carbide & Related Materials - Symposium at a Glance

	Monday AM	Monday PM	Tuesday AM	Tuesday PM	Wednesday AM	Wednesday PM	Thursday AM	Thursday PM	Friday AM
Ballroom I	MAP.Plenary Session I (8:30 AM) MB1.Bulk Growth I (10:45 AM)	MC1.Extended Defects I (4:30 PM)	TA1.Advanced Processing (8:30 AM) TB1.Point Defects I (10:45 AM)	TC1.Extended Defects II (4:30 PM)	WA1.Bulk Growth II (8:30 AM) WB1.Dopants and Impurities (10:45 AM)	WC1.Novel Characterization and Structures (4:30 PM)	RA1.Point Defects II (8:30 AM) RB1.EPI III: Homoepitaxy, Patterned Growth (10:45 AM)	RC1.Vibrational and Optical Properties (4:30 PM)	FA1.Surfaces, Interfaces and Planar Defects (8:30 AM)
Ballrooms II & III	MB2.Unipolar Devices & Detectors (10:45 AM)	MC2.Schottky and Bipolar Devices (4:30 PM)	TA2.EPI I: Multi-Wafer, Halide Assisted Epitaxy (8:30 AM) TB2.EPI II: Defect Reduction Growth Mechanisms (10:45 AM)	TC2.HF Devices (4:30 PM)	WA2.MOS Processing I (8:30 AM) WB2.MOS Processing II (10:45 AM)	WC2.MOSFETs (4:30 PM)	RA2.Novel Devices and Applications (8:30 AM) RB2.Device Reliability and Characterisation (10:45 AM)	RC2.Contacts (4:30 PM)	FA2.EPI IV: Heteroepitaxy of Cubic Crystal Structures (8:30 AM) FBP. Plenary Session II (10:45 AM)
Spirit of Pittsburgh Ballroom Foyer		MP.Poster Sessions (1:50 – 4:10 PM) MPG1.Bulk Growth I MPG2.EPI I MPP1.Device Processing MPD1.Diodes MPM1.Doping MPM2.Electrical & Optical Properties I MPM3.Extended Defects I MPM4.Novel Characterization and Structures I MPM5.Related Materials I MPM6.Surfaces and Interfaces I		TP.Poster Sessions (1:50 – 4:10 PM) TPG1.EPI II TPP1.MOS Processing TPD1.Reliability & Simulation TPM1.Point Defects TPM2.Electrical & Optical Properties II TPM3.Extended Defects II TPM4.Novel Characterization and Structures II TPM5.Related Materials II TPM6.Surfaces and Interfaces II		WP.Poster Sessions (1:50 – 4:10 PM) WPG1.Bulk Growth II WPP1.Advanced Processing WPD1.Switches WPM1.Transition Metal, Rare-Earth Dopants WPM2.Electrical & Optical Properties III WPM3.Extended Defects III WPM4.Novel Characterization and Structures III WPM5.Related Materials III WPM6.Surfaces and Interfaces III		RP.Poster Sessions (1:50 – 4:10 PM) RPP1.Contact Processing RPD1.Novel Devices and Applications RPM1.SIMS & Electrical Properties of Defects RPM2.Electrical & Optical Properties IV RPM3.Extended Defects IV RPM4.Novel Characterization and Structures IV RPM5.Related Materials IV RPM6.Surfaces and Interfaces IV	

PITTSBURGH PENNSYLVANIA

Late September in Pittsburgh brings comfortable temperatures with an average of 63 degrees. No matter how often you emerge from the Fort Pitt tunnel, the view of Pittsburgh is always magnificent, with the fountain at the Point, Heinz Field, and riverboats cruising along the three rivers.

What do you want to do? Chances are you can do it in Pittsburgh. Art abounds, culture is around every corner, and history is right at home here. Take time to explore the great outdoors, Broadway shows, feared roller coasters, prestigious museums…pack your camera and your walking shoes.

Pittsburgh isn't just a product of steel mills any longer. A world-class technology hub with recognized innovation in all areas of the industry, the Pittsburgh region is home to some of the most dynamic ventures, both startup and Fortune 500. Here, companies are developing the next generation of software and Internet applications, researching tomorrow's tissue engineering technologies, and perfecting advanced manufacturing techniques. We're capitalizing on our unique combination of natural and cultural amenities and a strengthening technology infrastructure to fuel our growth. The technical and scientific side of Pittsburgh is seen in the research departments of its renowned universities such as Carnegie-Mellon, Duquesne, and the University of Pittsburgh, and in its hospitals, where patients from all over the world travel for life-saving transplant operations.

For more information about the city of Pittsburgh, visit http://www.visitpittsburgh.com.

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Activities may be scheduled through the hotel's concierge between 7 a.m and 8 p.m.

Pittsburgh Walking Tours include three historic districts and are provided by the city planning department's Historic Review Commission. The commission was established in 1979 to administer the historic districts and structures designated by Pittsburgh City Council.

Other Tours:

Fourth Avenue - Pittsburgh's old banking and financial district, at one time second only to Wall Street.

Grant Street - some of the most handsome civic buildings in the country.

Mellon Square - a cornucopia of historical office buildings, department stores, churches, and park space.

Monongahela Wharf - a glimpse of what Pittsburgh was like as a bustling harbor town.

Evening Tour of Pittsburgh's Downtown Churches - some served the very earliest congregations in the United States.

To get walking, visit www.city.pittsburgh.pa.us/wt.

Pittsburgh Pirates are in town cracking the bats from September 16 through 18. The Pirates' home is PNC Park, a new riverfront facility combining the best features of yesterday's ballparks - rhythmic archways, steel trusswork and a natural grass playing field - with the latest in fan and player amenities and comfort.

Promotions at the games include Jack Wilson in The Box Day for children and All-Star Collectible Cards for all fans.

For tickets, log on to http://pittsburgh.pirates.mlb.com or call (877) 893-BUCS.

ATTRACTIONS WITHIN A ONE-MILE RADIUS

Benedum Center for Performing Arts hosts the Civic Light Opera, Pittsburgh Ballet Theatre, Pittsburgh Dance Council, Pittsburgh Opera, and Broadway Series.
For show information, call (412) 456-6666 or visit www.pgharts.org.

Andy Warhol Museum offers diverse audiences of artists, scholars and the general public the opportunity to creatively interact with the art and life of Andy Warhol.

The Warhol is one of the four Carnegie Museums of Pittsburgh. Opened in 1994, it features extensive permanent collections of art and archives on one of the most influential American artists of the twentieth century. It is also a primary resource for anyone seeking insights into contemporary art and popular culture. Find museum details at www.warhol.org.

Heinz Hall for the Performing Arts hosts the Pittsburgh Symphony Orchestra which has two performances scheduled at the time of ICSCRM 2005:

Sunday, September 18 at 2:30 p.m. Rafael Fruhbeck De Burgos conducts the orchestra with selections of *The Star-Spangled Banner,* Ludwig van Beethoven Symphony No. 6 in F Major, Opus 68 "Pastoral," and Stravinsky's *Le Sacre du printemps (*The Rite of Spring).

Friday and Saturday, September 23 and 24, at 8 p.m. and Sunday, September 25, at 2:30 p.m. the orchestra features selections sung by Chen Reiss, soprano; Scott Scully, tenor; and the Mendelssohn Choir of Pittsburgh.
For more information, visit www.pittsburghsymphony.org.

ATTRACTIONS

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