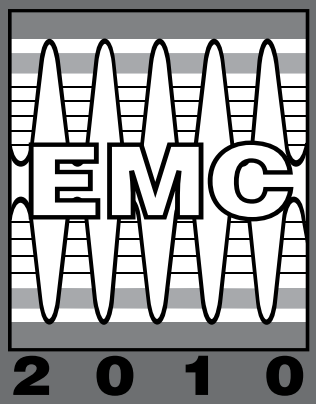


52nd ELECTRONIC MATERIALS CONFERENCE and Exhibition

June 23-25, 2010
University of Notre Dame,
Notre Dame, Indiana

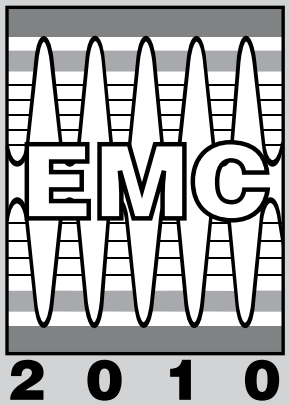
FINAL PROGRAM

Sponsored by:

TMS

Electronic, Magnetic
& Photonic
Materials Division

www.tms.org/EMC.html



It's Time to Get Electrified!

Welcome to the 52nd Annual Electronic Materials Conference!

Proudly presented by the Electronic, Magnetic & Photonic Materials Division of TMS

You are about to experience the premier annual global forum focusing on the preparation and characterization of electronic materials.

Registration Agenda

EMC 2010 attendees have a variety of opportunities to learn, network, and advance with electronic materials professionals and students for three illuminating days. Here is a summary of the must-attend events your registration* covers:

- All Technical Sessions
- Admission to the Exhibition
- Wednesday Night Welcoming Reception
- Coffee Breaks
- Thursday Night Banquet at the Northern Indiana Center for History and the Studebaker Museum

**One-day fee does not include the Banquet.*

Double Your Conference Experience

EMC is coordinated with the Device Research Conference (DRC), also held on-site, June 21-23. Badges will be accepted for admittance to the technical sessions at both conferences on Wednesday, June 23.

Table of Contents **Page**

About The Conference

Technical Sessions

The technical program commences with the plenary session on Wednesday, June 23 at 8:30 a.m. The plenary session will be held in Jordan Auditorium, Mendoza College of Business. All other sessions will be held in DeBartolo Hall.

Networking and Social Events

Welcoming Reception

Wednesday, June 23, 6 to 8 p.m.
McKenna Hall, University of Notre Dame

Take advantage of this relaxed occasion to network with familiar colleagues or to meet new industry professionals! This is also a chance to interact with exhibitors in a casual setting to learn firsthand about their cutting edge products and services.

Banquet

Thursday, June 24, 6:30 to 9 p.m.
Center for History and the Studebaker Museum • Northern Indiana

Dine in this magnificent historic site showcasing an elegant, 38-room Victorian mansion, a charming circa 1930's cottage, a gallery chronicling local history, a collage of Notre Dame history, a children's museum, and compelling exhibitions. In addition, the Studebaker Museum will lead visitors through a century of automotive development.

Tickets include dinner, entrance to the museums, and bus transportation to/from the University of Notre Dame. This event is free to both full conference and student registrants. Guest and one-day registrant tickets are $65 each and $30 for children 12 and under.

Buses wil board at McKenna Hall beginning at 5:15 p.m.

Purchase tickets on-site at the EMC registration desk until 5 p.m. on Wednesday, June 23.

Break Refreshments

Coffee, tea and soft drinks will be offered in the exhibition and break areas during morning and afternoon session intermissions.

General Information

Campus Smoking Policy
In accordance with St. Joseph County Ordinance #04-06 and LEED certification requirements, the University of Notre Dame prohibits smoking within 25 feet of all buildings and stadiums, as well as in all vehicles owned, leased or operated by the University.

Computer/Network Facilities
Free wireless Internet access is available for personal computers through ResNet, the University of Notre Dame's high-speed network wiring in all residence halls and public areas on campus. Guest ID's will be issued during registration.

Messages
Telephones and a message board will be located near the EMC registration desk on the first level of McKenna Hall. Messages will be posted on the board throughout the conference.

Audio/Video Recording Policy
TMS reserves the rights to any audio and video reproduction of all presentations at every TMS-sponsored meeting. Recording of sessions (audio, video, still photography, etc.) intended for personal use, distribution, publication, or copyright without the express written consent of TMS and the individual authors is strictly prohibited.

Americans With Disabilities Act
TMS strongly supports the federal Americans with Disabilities Act (ADA) which prohibits discrimination against, and promotes public accessibility for, those with disabilities. In support of, and in compliance with, ADA, we ask those requiring specific equipment or services to indicate their needs on the enclosed housing form or contact TMS Meeting Services in advance.

Refund Policy
The deadline for all refunds was June 4, 2010. No refunds are issued at the meeting. All fees and tickets are non-refundable after the June 4, 2010 deadline.


N
DOUGLAS ROAD
JUNIPER ROAD
Warren Golf Course
3010
WARREN GOLF COURSE ENTRANCE
WILSON DRIVE
STEPAN DRIVE
HOLY CROSS DRIVE
ST. MARY'S ROAD
St. Joseph's Lake
St. Mary's Lake
A17 Lot
D2 North Lot
D2 Middle Lot
D2 South Lot
B16 Lot
East Gate
1174
A18
A15 Lot
A9 Lot
Grotto
Main Building
Basilica
Hesburgh Library
CAVANAUGH DRIVE
EDDY DRIVE
CARROLL DRIVE
D6 North Lot
DORR ROAD
A12
A11
A10
B2 Library Lot
Visitor Lot
BULLA ROAD
B21 Lot
LEAHY DRIVE
PALMER STREET
NORTH TWYCKENHAM DRIVE
9-Hole Golf Course
3002
Suite Museum
Notre Dame Stadium
Joyce Center
Purcell Pavilion
COURTNEY LANE
VANESS
MOOSE KRAUSE CIRCLE
Morris Inn Lot
Bookstore Basketball Courts
Hammes Bookstore
Eck Visitors Center
Bookstore Lot time-limited parking
B1 Lot
C1 Lot
Gold Lot
Special Event Lot
Main Gate
1173
Visitor Lot
DeBartolo Performing Arts Center
Cedar Grove Cemetery
1204
Irish Green
3014
NOTRE DAME AVENUE
EDDY STREET
JOYCE DRIVE
IVY COURT
EDISON ROAD
ANGELA BOULEVARD
Main Entrance
Eddy Street Commons
1 2 3 4 5 6 7
A B C D E F G H

Campus Map

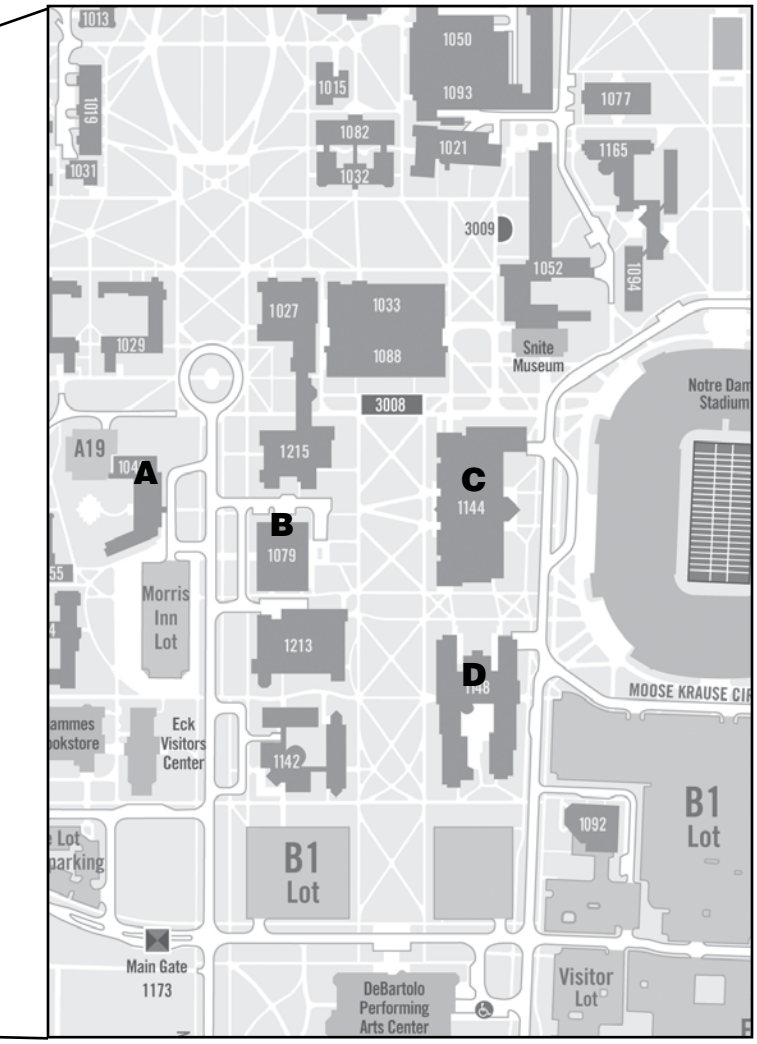
Quick Reference:

A: Morris Inn

B: Center for Continuing Education - McKenna Hall

C: DeBartolo Hall

D: Jordan Auditorium, Mendoza College of Business



LISTING OF CAMPUS LOCATIONS

Visit online at map.nd.edu

POINTS OF INTEREST

4E Basilica of the Sacred Heart
4G DeBartolo Performing Arts Center
4G Eck Visitors Center
3D Grotto of Our Lady of Lourdes
3G Hammes Notre Dame Bookstore
5E Hesburgh Library
6F Joyce Center
4E Main Building (Admissions)
5F Notre Dame Stadium
5F Snite Museum of Art
St. Mary's and St. Joseph's Lakes
Visitor Parking Lots at 5H and 6D

ALPHABETICAL LISTING

4E Admissions (Main Building)
4G Alumni Association/Eck Visitors Center
4F Alumni Hall 1029
7G Alumni Field (Soccer) 3001
6G Alumni Stadium (Soccer) 1216
7G Arlotta Stadium (Lacrosse) 1218
6F Athletic and Convocation Center (Joyce Center)
3B Ave Maria Press 1156
3E Badin Hall 1016
4E Basilica of the Sacred Heart
6E (Ricci) Band Rehearsal Hall 1100
6G Batting Building 1190
4F Biolchini Hall of Law 1027
4C Boat House 1007
3E Bond Hall (Architecture) 1020
3G (Hammes Notre Dame) Bookstore
5E Breen–Phillips Hall 1040
4D Brownson Hall 1003
5D Cafeteria (North Dining Hall) 1057
3F Cafeteria (South Dining Hall/ Reckers) 1026
1E Carroll Hall 1017
4E Cavanaugh Hall 1036
3H Cedar Grove Cemetery 1204
4E Clarke Memorial Fountain 3005
3E Coleman-Morse (First-Year of Studies) 1163
3D Columba Hall 1002
3E Corby Hall 1014
7F Courtney Tennis Center 3004
5B (Notre Dame Federal) Credit Union 1181
4E Crowley Hall of Music 1015
4F Cushing Hall of Engineering 1033
4F DeBartolo Hall 1144
4G DeBartolo Performing Arts Center
5F Decio Faculty Hall 1094
3F Dillon Hall 1030
3F Duncan Hall 1211
6D Early Childhood Development Center 1146
4D Earth Sciences Building 1004
5D East Gate 1174
7G Eck Baseball Stadium 1145
4F Eck Hall of Law 1215
7F Eck Tennis Pavilion 1096
4G Eck Visitors Center/Alumni Association
4H Eddy Street Commons (Development, Investment) 9012
5C Engineering North 1205
4H Ernestine Raclin-O.C. Carmichael Hall 6103
5C Facilities Building 1169
5C Facilities/Maintenance Center 1059
5D Farley Hall 1044
4E Fieldhouse Mall 3005
5D (Thomas Coleman) Fire Station 1043
3E First Year of Studies 1163
7D Fischer Graduate Community Center 1103
6D Fischer Graduate Residences 1104–1136
7D Fischer Visiting Faculty Apartments 1137/1138/1140/1141
3F Fisher Hall 1051
4F Fitzpatrick Hall of Engineering 1088
5D Flanner Hall 1085
4B Food Services Support Facility 1153
5E Freimann Life Science Center 1080
5E Galvin Life Sciences Center 1080
5E Geddes Hall (Center for Social Concerns, Institute for Church Life) 1212
5D Grace Hall 1086
3D Grotto of Our Lady of Lourdes
6F Guglielmino Athletics Complex 1206
7F Haggar Fitness Complex 1097
4D Haggar Hall 1037
3G Hammes Notre Dame Bookstore
5D Hammes Mowbray Hall (Security Police, Post Office) 1192
5F Hank Family Center for Environmental Sciences 1149
4H Harper Hall 1221
4E Hayes–Healy Center 1082
4D Health Services (St. Liam Hall) 1035
4G Hesburgh Center for International Studies (Kroc Institute / Kellogg Institute / Greenfields Cafe) 1142
5E Hesburgh Library
5C Hessert Aerospace Research Center 1041
4C Holy Cross House 1060
3E Howard Hall 1023
4E Huddle (LaFortune Food Court) 1012
4E Hurley Hall (Science) 1032
5E Information Technology Center 1061
6H Innovation Park 1220
4D Institute for Educational Initiatives 1005
4H Investment Office 9012
4H Irish Green 3014
5F Isis Gallery (O'Shaughnessy Hall) 1052
6E Jordan Hall of Science 1193
6F Joyce Center
4D Keenan Hall 1055
3F Keough Hall 1178
3E Knights of Columbus Council Hall 1031
5D Knott Hall 1098
4E LaFortune Student Center/Huddle 1012
4B (St. Michael's) Laundry 1143
6F LaBar Practice Complex 3003
4D Laundry Pick-Up Center 1167
5G Legends 1092
4D Lewis Hall 1078
7F Loftus Sports Center 1097
3E Log Chapel 1018
3E Lyons Hall 1024
4D Mail Distribution Center 1167
4E Main Building (Graduate School)
4G Main Gate 1173
5E Malloy Hall 1165
5B Mason Support Services Center 1101
3F McGlinn Hall 1154
4F McKenna Hall (Notre Dame Conference Center) 1079
7H Melissa Cook Stadium (Softball) 1217
4G Mendoza College of Business 1148
7F Meyo Field 1097
3C Moreau Seminary 1056
4F Morris Inn 1049
3E Morrissey Hall 1025
3E Morse Center for Academic Services 1163
4E Nieuwland Science Hall 1050
5D North Dining Hall 1057
4F Notre Dame Conference Center (McKenna Hall) 1079
5B Notre Dame Federal Credit Union 1181
2F Notre Dame Golf Course 3002
5F Notre Dame Stadium
6D O'Hara-Grace Graduate Residences 1087
3E Old College 1001
3F O'Neill Hall 1151
5F O'Shaughnessy Hall (Arts & Letters) 1052
1D Our Lady of Fatima House and Shrine 1170
3F Pangborn Hall 1054
5B Paris House (Marital Therapy and Research Clinic) 1182
6E Pasquerilla Center (ROTC) 1102
5D Pasquerilla Hall East 1091
5D Pasquerilla Hall West 1089
5D Post Office 1192
4D Power Plant 1034
3E Presbytery 1006
4C Province Archives Center 1183
6G Purcell Pavilion/Ticket Office
5E Radiation Research Building 1077
3F Reckers/Public Cafeteria 1026
4B Reyniers Life Annex 1045
4B Reyniers Life Building 1046
6E Ricci Band Rehearsal Hall 1100
4E Riley Hall of Art and Design 1021
7B Rolfs Family All Season Golf Facility 1209
2F Rockne Memorial 1039
6F Rolfs Aquatic Center 1083
6F Rolfs Sports Recreation Center 1157
3G Ryan Hall 1214
4E (Basilica of the) Sacred Heart
3C Sacred Heart Parish Center 1185
5D Security Office 1192
4F Sesquicentennial Common 3008
5F Shaheen Mestrovic Memorial 3009
5D Siegfried Hall 1099
5F Snite Museum of Art
3D Solitude of St. Joseph (Columba Hall) 1002
4E Sorin Hall 1013
3F South Dining Hall/Reckers 1026
4D St. Edward's Hall 1011
4G Stinson Remick 1213
4D St. Liam Hall 1035
4B St. Michael's Laundry 1143
4D Stanford Hall 1058
5C Stepan Center 1062
4E Stepan Chemistry Hall 1093
4E Student Center (LaFortune) 1012
2E Telecommunications 1042
7F Tennis Courts 3004
5D Thomas Coleman Fire Station 1043
6G Ticket Office (Purcell Pavilion)
6H Track and Field 3015
1A University Village 1064–1075
3E Walsh Hall 1019
7B Warren Golf Clubhouse 1160
7B Warren Golf Course 3010
4E Washington Hall 1010
5D Water Tower 1191
3F Welsh Family Hall 1155
6D Wilson Commons 1186
3A Wind Tunnel 1210
1E WNDU Stations 1187
4D Zahm Hall 1038

EMC Exhibition

Don't miss this opportunity to meet the providers of electronic materials technologies and services and get acquainted with their capabilities and products.

Exhibit Dates and Hours

Wednesday, June 23: 9:30 a.m. to 1:30 p.m.; 3 to 4 p.m. and 6 to 8 p.m.
Thursday, June 24: 10 a.m. to 1:30 p.m. and 3 to 4 p.m.

Exhibitors *(As of 5/19/10)*

A complete list and company descriptions can be found in the EMC Exhibit Directory on site

- Agilent Technologies
- Big C
- Lake Shore Cryotronics, Inc.
- MMR Technologies, Inc.
- Omicron NanoTechnology USA
- SAFC Hitech
- Riber
- United Mineral & Chemical Corp.
- Veeco Instruments, Inc.
- Wafer Technology

Awards

John Bardeen Award

Established in 1994, this award recognizes an individual who has made outstanding contributions, and is a leader in the electronic materials field.

2010 Recipient: Eugene Haller
University of California – Berkeley;
Lawrence Berkeley National Laboratory

Citation: For seminal contributions to the materials science and technology of isotopically engineered semiconductors.

"Winning the 2010 John Bardeen Award of TMS is a great honor and a much appreciated recognition of the research contributions that my collaborators, students, postdocs, and I have made. The award carries the name of one of my greatest heroes in the sciences, John Bardeen. I had the fortune to speak with John Bardeen on a few occasions. I was always impressed by his friendly and low-key style of discussing science. As a young postdoctoral fellow at the Rad Lab in Berkeley (now the Lawrence Berkeley National Laboratory), I discussed our ultra-pure germanium research and development with John Bardeen who at the time was reviewing our work for the Atomic Energy Commission (now the Department of Energy). He listened carefully with an approving smile!"

About John Bardeen

John Bardeen's career of theoretical and experimental research set the foundation for the current state of understanding of electronic materials. Two areas in which Bardeen had great impact were the invention and development of the solid-state transistor and the theory that developed greater understanding of superconductivity.

Nominate Your Colleague for the TMS 2011 John Bardeen Award!

For Award Criteria and Additional Information pick up a nomination visit the TMS Web site at: **www.tms.org/Society/honors.html**.

Student Best Paper Award

Student awards are given annually by the Electronic Materials Committee for the best presentations at the conference. Student papers are judged on both scientific content and presentation at the Electronic Materials Conference. The awards will be presented during the plenary session on Wednesday morning, June 24, in McKenna Auditorium.

Recipients

Sebastien Vincent, *Soitec S.A., Bernin, France*
"Study of the Formation, Evolution and Dissolution of Interfacial Bonding Defects Based on the Hydrogen Storage and Diffusion Mechanisms."
Advisor: Professor Francois Rieutord

John Simon, *University of Notre Dame, Notre Dame, Indiana, USA*
"Polarization Enhanced p-Type Conductivity in Graded N-Face AlGaN Slabs."
Advisor: Professor Debdeep Jena

Charles Brooks, *Pennsylvania State University, University Park, Pennsylvania, USA*
"Growth and Microstructure of Homoepitaxial Strontium Titanate Thin films by Molecular-Beam Epitaxy."
Advisor: Professor Darrell Schlom

Shriram Shivaraman, *Cornell University, Ithaca, New York, USA*
"Epitaxial Graphene Micro-Bridges."
Advisor: Professor Michael Spencer

Proceedings

Proceedings and Publications

EMC does not publish formal conference proceedings; however, the *Journal of Electronic Materials (JEM)* encourages both presenter and attendees to submit manuscripts of their work.

About *JEM*

JEM is a monthly archival technical journal of TMS and the Institute of Electrical and Electronics Engineers (IEEE). Articles are reviewed, selected and edited by peers who serve as voluntary members of the editorial board, the board of associate editors, or section editors.

JEM Content

JEM is a forum for the rapid circulation of the results of original research. It contains technical papers detailing critical new developments in the electronics field, as well as invited and contributed review papers on topics of current interest. The journal focuses on electronic memory and logic structures, magnetic-optical recording media, superlattices, packaging, detectors, emitters, metallization technology, superconductors, and low thermal-budget processing and includes general papers on electronic materials for device application, structure making, reliability, and yield. Articles on methods for preparing and evaluating the chemical, physical, and electronic properties of electronic materials are also included.

JEM Subscription

2010 and 2011 *JEM* issues will include manuscripts of papers presented at the 2010 Electronic Materials Conference. Individuals may subscribe to *JEM* by contacting Springer, the journal's publisher, at:
In North America
Telephone (800) 777-4643
E-mail journals-ny@springer.com
Outside North America
Telephone (212) 460-1500 or +49 (0) 6221-345-4303
E-mail subscriptions@springer.com

JEM Editorial Board

Suzanne E. Mohney, Editor
Pennsylvania State University, USA
Theodore C. Harman, Editor Emeritus
Massachusetts Institute of Technology, USA

JEM Associate Editors

Husam N. Alshareef, *King Abdullah University of Science & Technology, Saudi Arabia*
John Baniecki, *Fujitsu Laboratories, Japan*

Continued →

JEM Associate Editors Continued

Katayun Barmak, *Carnegie Mellon University, USA*
Ishwara Bhat, *Rensselaer Polytechnic Institute,USA*
L.J. Brillson, *Ohio State University, USA*
Sinn-wen Chen, *National Tsing Hua University, Taiwan*
Deborah Chung, *University of Buffalo, USA*
Kurt G. Eyink, *Air Force Research Laboratory, USA*
Darrel Frear, *Freescale Semiconductor,USA*
Rachel S. Goldman, *University of Michigan, USA*
William C. Mitchel, *Air Force Research Laboratory,USA*
Alberto Salleo, *Stanford University,USA*
Robert Stahlbush, *Naval Research Laboratory,USA*
Michael Tischler, *OCIS Technology LLC, USA*
Jian Xu, *Pennsylvania State University, USA*
Jihui Yang, *GM R&D Center, USA*

Editorial Oversight Committee

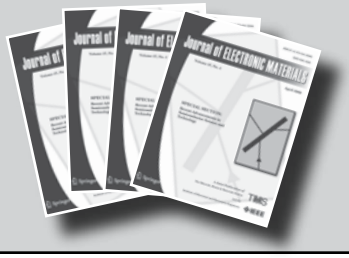
L.J. Guido, *Virginia Polytechnic Institute, USA*
J.L. Merz, *University of Notre Dame, USA*
L S. Rea, *Wright-Patterson Air Force Base, USA*
T.D. Sands, *Purdue University, USA*
X. Zhou, *Nanyang Technological University, Singapore*

New Professional Honor…

JEM Best Paper Award

TMS is accepting nominations for the new *JEM* Best Paper Award. The accolade will recognize outstanding scientific or engineering contributions to the *Journal of Electronic Materials*, while also increasing the visibility of the journal. Papers published in *JEM* from July 2009 through June 2010 are eligible for nomination. The inaugural award will be presented at the TMS 2011 Annual Meeting in San Diego, California. Nominations will be accepted from anyone, including the *JEM* editor and associate editors, through October 15, 2010.The final decision will be made by the Editorial Oversight Board, which is devoid of editors.

To nominate a paper, please submit a copy along with the nominator's letter of endorsement and recommendation to Deborah Price, Student Affairs & Awards Administrator, **price@tms.org.**



Conference Organizers

Electronic Materials Committee

OFFICERS:

Mark Goorsky, *Chairperson*
University of California, Los Angeles, USA

Robert Biefeld, *Past Chairperson*
Sandia National Laboratories, USA

Christian Wetzel, *Vice Chairperson*
Rensselaer Polytechnic Institute, USA

Andrew A. Allerman, *Treasurer*
Sandia National Laboratories, USA

Archie Holmes, *Secretary*
University of Virginia, USA

Zi-Kui Liu, *Chair EMPMD*
Pennsylvania State University, USA

Members

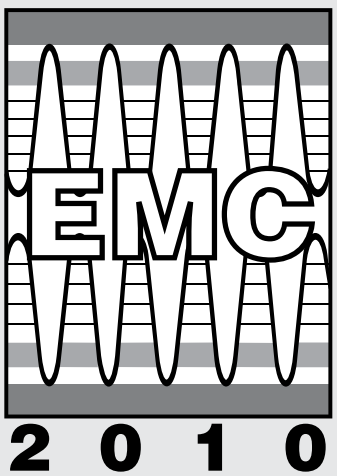
Andrew Allerman, *Sandia National Laboratories, USA*
Brian Bennett, *Naval Research Laboratories, USA*
Robert Biefeld, *Sandia National Laboratories, USA*
Len Brillson, *Ohio State University, USA*
Ralph Dawson, *University of New Mexico, USA*
Russ Dupuis, *Georgia Institute of Technology, USA*
Kurt Eyink, *Air Force Research Laboratories, USA*
Patrick Fay, *University of Notre Dame, USA*
Douglas Hall, *University of Notre Dame, USA*
Theodore C. Harman, *Massachusetts Institute of Technology-- Lincoln Laboratory, USA*
Thomas Jackson, *Pennsylvania State University, USA*
David Janes, *Purdue University, USA*
Debdeep Jena, *University of Notre Dame, USA*
Kei-May Lau, *Hong Kong University of Science & Technology*
Pat Lenahan, *Pennsylvania State University, USA*
Mike Manfra, *Purdue University, USA*
Jim Merz, *University of Notre Dame, USA*
Suzanne Mohney, *Pennsylvania State University, USA*
Pete Moran, *Michigan Technical University, USA*
Sarah Olsen, *Newcastle University, UK*
Jamie Phillips, *University of Michigan, USA*
Joan Redwing, *Pennsylvania State University, USA*
Steve Ringel, *Ohio State University, USA*
Alberto Salleo, *Stanford University,USA*
Tim Sands, *Purdue University,USA*
Akio Sasaki, *Osaka Electro-Communication University, Japan*

Tae-Yeon Seong, *Korea University*
Ben Shanabrook, *Naval Research Laboratory, USA*
Glen Solomon, *NIST/University of Maryland, USA*
Robert Stahlbush, *Naval Research Laboratory, USA*
Mike Tischler, *Quanlight, USA*
Charles Tu, *University of California, San Diego, USA*
Eric Wachsman, *University of Florida, USA*
Christine Wang, *Massachusetts Institute of Technology-- Lincoln Laboratory, USA*
William Wong, *Palo Alto Research Center, USA*
Jerry Woodall, *Purdue University, USA*

Invited Organizers for EMC 2010

The Electronic Materials Conference wishes to thank the following invited organizers for their support and contribution to the technical program presented at this year's conference:

Joel Ager, *Lawrence Berkeley Laboratory, USA*
Martin Allen, *University of Canterbury, New Zealand*
Ian Appelbaum, *University of Maryland, USA*
Andrew Armstrong, *Sandia National Laboratories, USA*
Ganesh Balakrishnan, *University of New Mexico, USA*
Seth Bank, *University of Texas -- Austin, USA*
Kris Bertness, *National Institute of Standards and Technology, USA*
Mayank Bulsara, *Massachusetts Institute of Technology, USA*
Joshua Caldwell, *Naval Research Laboratory, USA*
Michael Chabinyc, *University of California -- Santa Barbara*
Cindy Colinge, *Tyndall National Institute, UK*
Reuben Collins, *Colorado School of Mines, USA*
John Conley, *Oregon State University, USA*
Suman Datta, *Pennsylvania State University, USA*
Theeradetch Detchprohm, *Rensselaer Polytechnic Institute, USA*
Alan Doolittle, *Georgia Institute of Technology, USA*
Michael Dudley, *State University of New York at Stony Brook, USA*
Partha Dutta, *Rensselaer Polytechnic Institute, USA*
Randall Feenstra, *Carnegie Mellon University, USA*
Eugene Fitzgerald, *Massachusetts Institute of Technology, USA*
Michael Flatte, *University of Iowa, USA*
Mike Gerhold, *Army Research Laboratory, USA*
Avik Ghosh, *University of Virginia, USA*
Rachel Goldman, *University of Michigan, USA*
David Gundlach, *National Iinstitute of Standards and Technology, USA*
Evgeni Gusev, *Qualcomm MEMS Technologies, USA*
Karl Hobart, *Naval Research Laboratory, USA*
Julia Hsu, *Sandia National Laboratories, USA*
Brett Hull, *Cree, Inc., USA*
Oana Jurchescu, *Wake Forest University, USA*
Thomas Kuech, *University of Wisconsin, USA*
Lincoln Lauhon, *Northwestern University, USA*
Amy Liu, *IQE, Inc., USA*
Xinyu Liu, *University of Notre Dame, USA*
Maria Losurdo, *CNR-IMIP, Italy*
James Lu, *Rensselaer Polytechnic Institute, USA*
Yicheng Lu, *Rutgers University, USA*
Charle Lutz, *Kopin Corporation, USA*
Theresa Mayer, *Pennsylvania State University, USA*
Thomas Myers, *Texas State University, USA*
Yasushi Nanishi, *Ritsumeikan University, Japan*
Lisa Porter, *Carnegie Mellon University, USA*
Sandhu Rajinder, *Northrop Grumman Space Technology, USA*
Shriram Ramanathan, *Harvard University, USA*
Laura Rea, *Air Force Research Laboratories, USA*
Nitin Samarth, *Pennsylvania State University, USA*
James Speck, *University of California, Santa Barbara, USA*
Mike Spencer, *Cornell University, USA*
Sussan Stemmer, *University of California, Santa Barbara, USA*
Kodambaka Suneel, *University of California, Los Angeles, USA*
Alec Talin, *NIST, USA*
Masaaki Tanaka, *University of Tokyo, Japan*
Raymond Tsui, *Motorola Laboratories, USA*
Bruce Wessels, *Northwestern University, USA*
Michael Wraback, *U.S. Army Research Laboratory, USA*
Ya-Hong Xie, *University of California, Los Angeles, USA*
Huili (Grace) Xing, *University of Notre Dame, USA*
Cheng Yang, *Purdue University, USA*
Ed Yu, *University of Texas at Austin, USA*
Joshua Zide, *University of Delaware, USA*



New Professional Honor…

Journal of ELECTRONIC MATERIALS

JEM Best Paper Award

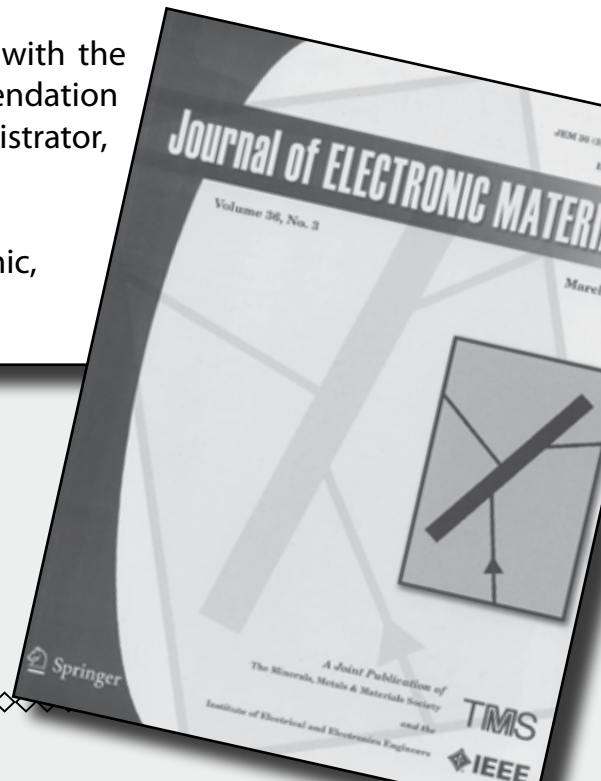
TMS is accepting nominations for the new JEM Best Paper Award.

The accolade will recognize outstanding scientific or engineering contributions to the *Journal of Electronic Materials*, while also increasing the visibility of the journal. Papers published in *JEM* from July 2009 through June 2010 are eligible for nomination. Nominations will be accepted from anyone, including the *JEM* editor and associate editors, through October 15, 2010. The final decision will be made by the Editorial Oversight Board, which is devoid of editors.

Winners will receive a waiver to attend either the **TMS 2011 Annual Meeting and Exhibition** in San Diego, California, or **EMC 2011** at the University of California, Santa Barbara, to accept their award.

To nominate a paper, please submit a copy along with the nominator's letter of endorsement and recommendation to **Deborah Price**, Student Affairs & Awards Administrator, **price@tms.org**.

This award is supported by *JEM* and the TMS Electronic, Magnetic & Photonic Materials Division.



TMS
EMPMD
Electronic, Magnetic & Photonic Materials Division

Wednesday AM June 23, 2010		Wednesday AM June 23, 2010		Wednesday AM June 23, 2010	
EMC Student Awards and Plenary Lectures Room: Jordan Auditorium Mendoza College of Business		**Session A: High-K Gate Dielectrics Room: 102**		**Session B: Non-Destructive Characterization Room: 126**	
8:20 AM	Awards Ceremony	10:00 AM	A1, (Invited), The Electrical Properties of Metal/Gd_{2O3}Si Gate Stacks and Their Dependence on the Structure of the Oxide Layer .....Moshe Eizenberg	10:00 AM	B1, Innovative Time-Resolved Optical Characterization Techniques for Monitoring of Carrier Dynamics in Wide Band Gap Semiconductors .....Kestutis Jarasiunas
				10:20 AM	B2, Raman Characterization Methodologies Suitable for Determining Graphene Thickness and Uniformity .....David Tomich
8:30 AM	(Plenary), Epitaxial Graphene: Designing a New Electronic Material .....Walter A. de Heer	10:40 AM	A2, (Student), Spin Dependent Trap Assisted Tunneling in Gd_2O_3 Dielectrics .....Brad Bittel	10:40 AM	B3, (Student), Characterizing the RF Properties of Semiconductors under Optical Illumination .....Youssef Tawk
		11:00 AM	A3, Crystalline Lattice-Matched $Ba_{0.7}Sr_{0.3}O$ on Si(001) as Gate Dielectric ..... Herbert Pfnür	11:00 AM	B4, (Student), Admittance Spectroscopy of GaSb(100) and ALD / PEALD Al_2O_3 Dielectric Interface with Various Surface Treatments .....Ashkar Ali
9:20 AM	Break	11:20 AM	A4, (Student), Rare-Earth Scandates/Tin Gate Stack on High Mobility Strained SOI for Fully Depleted (FD) Mosfets .....Eylem Durgun Özben	11:20 AM	B5, (Student), High Temperature Coefficient of Resistance Sputtered A-Ge for Uncooled Microbolometer Applications .....Hang-Beum Shin
		11:40 AM	A5, Late News	11:40 AM	B6, (Student), Temperature Dependence of the Lattice Constant of Popular III-Sb Binary and Quarternary Alloys .....Magnus Breivik

Wednesday AM June 23, 2010		Wednesday AM June 23, 2010		Wednesday AM June 23, 2010	
Session C: Nanoscale Characterization Room: 129		**Session D: Narrow Bandgap Semiconductor Bulk Materials and Devices Room: 131**		**Session E: Materials Integration: Wafer Bonding Room: 138**	
10:00 AM	C1, (Student), Pulsed-Laser Atom Probe Tomographic Analysis of Ge-Ge/Co/Mn Thin-Film Superlattices .....James Riley	10:00 AM	D1, (Invited) Review of Narrow Bandgap Semiconductor Based THz-Emitters .....Ingrid Wilke	10:00 AM	E1, (Student), Investigation of Physisorbed and Chemisorbed Sulfur Species for GaAs Wafer Bonding .....Michael Jackson
10:20 AM	C2, (Student), Atomic Scale Gate Electrode Formed by a Charged Defect on GaAs(110) .....Donghun Lee	10:20 AM	D2, (Student), Electrical and Optical Studies of Melt Grown Optical Grade $InAs_{1-y}P_y$ .....Jean Wei	10:20 AM	E2, (Student), AlGaAs/GaAs/GaN Wafer Fused HBTs with Ar Implanted Extrinsic Collectors .....Zongyang Hu
10:40 AM	C3, Ordered Assemblies of Bimetallic Nanostructure Arrays Utilizing a Self-assembled Disilicide Nanowire Template .....Talin Ayvazian	10:40 AM	D3, (Student), Electrical and Optical Properties of Bulk Ternary $In_xGa_{1-x}As$ .....Austin Berstrom	10:40 AM	E3, (Student), Effect of Surface Activation for Ge-Si Integration Using Wafer Bonding .....Ki Yeol Byun
11:00 AM	C4, (Student), Scanned Probe Characterization of Self-Assembled ErAs/GaAs Semimetal/Semiconductor Nanostructures Grown by Molecular-Beam Epitaxy .....Keun Woo Park	11:00 AM	D4, (Student), Optical and Thermal Properties of III-V Bulk Ternary $In_xGa_{1-x}Sb$ and $In_xGa_{1-x}As$ Crystals .....Shekhar Guha	11:00 AM	E4, (Student), Strain, Annealing, and Exfoliation in Hydrogen Implanted GaN for Layer Transfer Applications .....Eric Padilla
11:20 AM	C5, Late News	11:20 AM	D5, Late News	11:20 AM	E5, Optimization of Adhesive Wafer Bonding for Silicon .....Sue Holl
11:40 AM	C6, Late News	11:40 AM	D6, Late News	11:40 AM	E6, Development of Surface Activation Based Nano-Bonding and Interconnect System .....Matiar Howlader

Wednesday AM June 23, 2010		Wednesday PM June 23, 2010		Wednesday PM June 23, 2010	
Session F: Silicon Carbide Devices Room: 155		**Session G: Oxide Semiconductor Thin Film Transistors Room: 102**		**Session H: Materials and Devices for Flexible Electronics Room: 126**	
10:00 AM	F1, (Invited), Applications of SiC Power Devices – A Materials and Device Perspective .....Anant Agarwal	1:30 PM	G1, (Student), Temperature Dependent Measurements of ZnO TFTs .....Devin Mourey	1:30 PM	H1, (Student), Molecular Contact Doping in Organic Thin-Film Transistors .....Frederik Ante
		1:50 PM	G2, (Student), Flexible ZnO Temperature Sensors on Plastic Substrate .....Dalong Zhao	1:50 PM	H2, (Student), Gate Dielectric Thickness Dependence of OTFT Performance .....Yuanyuan Li
10:40 AM	F2, Review of the Dominant Scattering Mechanisms in SiC MOS Devices .....Jody Fronheiser	2:10 PM	G3, (Student), Improvement of $InGaZnO_4$ TFT Device Performance on Glass and Paper Substrates .....Erica Douglas	2:10 PM	H3, (Student), Arylene Diimide-Thiophene Semiconductors for n-Channel Field-Effect Transistors .....Rocio Ponce Ortiz
11:00 AM	F3, (Student), A Comparative Study of Thermal and Deposited Gate Oxides on 4H SiC .....Sarah Haney	2:30 PM	G4, Sputtering of ZnO Thin Films for TFT on Polyimide Substrates .....Faraz Khan	2:30 PM	H4, (Student), Advanced X-Ray Peak Shape Analysis of Organic Semiconductors: Insights into Crystalline Size, Strain, Intragrain Disorder and Implications for Charge Transport .....Jonathan Rivnay
11:20 AM	F4, (Student), Magnetic Resonance Studies of 4H SiC MOS Structures .....Brad Bittel	2:50 PM	G5, (Student), Zinc-Tin-Oxide Thin-Film Transistors with Al_2O_3 and ZrO_2 Gate Dielectrics .....Josh Triska	2:50 PM	H5, Probing Stress Effects in Single Crystal Organic Transistors by Scanning Kelvin Probe Microscopy .....Lucile Teague
11:40 AM	F5, Influence of Geometry on Silicon Carbide JBS Diodes Conduction .....Maxime Berthou	3:10 PM	Break	3:10 PM	Break
		3:30 PM	G6, (Student), Study of CV and Admittance Characteristics of ALD High-K Dielectric ZnO Capacitors .....Jeffrey Siddiqui	3:30 PM	H6, (Student), Study on the Resistance of Stretchable Electrodes from Surface Morphology Aided by Computer Modeling .....Wenzhe Cao
		3:50 PM	G7, (Student), Transparent Rectifying Contacts - A New Concept for Transparent Electronics .....Alexander Lajnl	3:50 PM	H7, (Student), Reverse Offset Roll Printing Using High Resolution Printing Plate for Electronic Application .....Nackbong Choi
		4:10 PM	G8, Transition from Hopping to Band-like Transport in Solution-Processed Amorphous Zinc Tin Oxide Thin-Film Transistors .....Chen-Guan Lee	4:10 PM	H8, (Student), A Novel Hybrid Electrical and Chemical Barrier Material for Flexible Electronics .....Lin Han
		4:30 PM	G9, (Student), A Comparative Study of the Effect of Heat Treatment on the Microstructure and Properties of Colloidal ITO Films and Cold-Sputtered ITO Film .....Salil Joshi	4:30 PM	H9, (Student), Heavily Doped ZnO Thin Films for Hybrid Inorganic Organic Devices .....Zaheer Khan
		4:50 PM	G10, Optimization of Dielectric Passivation of ZnO-Based Schottky Diodes .....Holger von Wenckstern	4:50 PM	H10, Late News

Wednesday PM June 23, 2010		Wednesday PM June 23, 2010		Wednesday PM June 23, 2010	
Session I: Nanomagnetic and Spintronic Materials Room: 129		**Session J: Thin Film Photovoltaics Room: 131**		**Session K: III-Nitride Nanowires Room: 138**	
1:30 PM	I1, An Organic-based Magnetic/Nonmagnetic Semiconductor as a Spin Polarized Carrier Source/Channel: Moving Toward Organic Spintronics .....Jung-Woo Yoo	1:30 PM	J1, MBE Growth of Metamorphic InGaP on GaAs and GaP for Wide-Bandgap Photovoltaic Junctions .....John Simon	1:30 PM	K1, Molecular Beam Epitaxy of Catalyst-free InGaN/GaN Nanowires on (001) Silicon and Nanowire Light Emitting Diodes .....Wei Guo
1:50 PM	I2, (Student), Effect of Perpendicular Magnetic Anisotropy on Emerging Magnetic Logic Devices .....Larkhoon Leem	1:50 PM	J2, (Student), $In_xGa_{1-x}As$ Metamorphic Buffer Layers for Lattice Mismatched Multi-Junction Solar Cells .....Peter Dudley	1:50 PM	K2, Photoluminescence of Bandgap-Graded Ingan Wires Grown by Molecular Beam Epitaxy .....Vladimir Protasenko
2:10 PM	I3, (Student), Observation of Antiferromagnetic Interlayer Exchange Coupling in a GaMnAs/GaAs:Be/GaMnAs tri-layer .....Jonathan Leiner	2:10 PM	J3, (Student), Quantum Dot n-i-p-i Photovoltaic Devices .....Michael Slocum	2:10 PM	K3, Growth of Dislocation-Free and High-Indium-Content InGaN/GaN Coaxial Nanowires .....Qiming Li
2:30 PM	I4, Electrical Spin Injection in a Hybrid Organic/Inorganic Spin-Polarized Light Emitting Diode (Spin-LED) .....Ezekiel Johnston-Halperin	2:30 PM	J4, Characterization of a <I>p-i-n</I> Photovoltaic Cell Containing InAs/GaAs Quantum Dots .....Andrey Semichaevsky	2:30 PM	K4, Threshold Studies of Optically Pumped GaN Nanowire Lasers .....John Schlager
2:50 PM	I5, Properties of MnAs/GaMnAs/MnAs Magnetic Multilayers and Their Application to High Temperature Vertical Spin Valves .....Debashish Basu	2:50 PM	J5, MBE growth of lattice-matched 6.1Å II-VI on GaSb substrates .....Xinyu Liu	2:50 PM	K5, GaN Nanowire MOSFETs with Fully Conformal Cylindrical Gates .....Paul Blanchard
3:10 PM	Break	3:10 PM	Break	3:10 PM	Break
3:30 PM	I6, (Student), The Magneto-Optic Kerr Effect (MOKE) as a Measure of Strain-Induced Ferromagnetism in $EuTiO_3$ Grown by Molecular-Beam Epitaxy .....Lei Fang	3:30 PM	J6, ZnO/ZnTeO/ZnTe Heterojunctions for Intermediate State Solar Cells .....Weiming Wang	3:30 PM	K6, Formation Mechanisms and Kinetics of Negative Nanowires in GaN and ZnO Using In-Situ Transmission Electron Microscopes .....Bong-Joong Kim
3:50 PM	I7, (Student), Magnetic Circular Dichroism (MCD) studies on GaMnAs .....Kritsanu Tivakornsasithorn	3:50 PM	J7, (Student), Copper Zinc Tin Sulfide Solar Cell Development by RF Sputtering from Binary Targets .....Jeffrey Johnson	3:50 PM	K7, (Student), Self-Assembled GaN/AlN Nanowire Superlattices on Si toward Non-Polar Intersubband Photonics .....Santino Carnevale
4:10 PM	I8, (Student), Magneto-Optical Spectroscopy of MOVPE grown Ferromagnetic Semiconductors .....Mithun M. Bhowmick	4:10 PM	J8, (Student), Chemical Vapor Deposition of $CsSnI_3$ Thin Films for Photovoltaic Applications .....Nicholas LiCausi	4:10 PM	K8, HVPE Homoepitaxy of p-type GaN on n-type Catalyst Free GaN Nanowires .....Aric Sanders
4:30 PM	I9, Micromagnetic Simulation of Focused Ion Beam Patterned Cobalt-Platinum Multilayers .....Gyorgy Csaba	4:30 PM	J9, (Student), Exploring More Effective Catalysts for Metal-Induced Growth of Thin Film Si .....Peter Mersich	4:30 PM	K9, Homoepitaxial Nucleation of GaN Nanowires in Grooves .....Alexana Roshko
4:50 PM	I10, (Student), Growth and Characterization of $In_{1-x}Mn_xSb$ Ferromagnetic Semiconductor Alloys using Metal Organic Vapor Phase Epitaxy (MOVPE) .....Caitlin Feeser	4:50 PM	J10, (Student), Enhanced Light Absorption in Thin-Film Silicon Solar Cells by Scattering from Sub-Surface Dielectric Nanoparticles .....James Nagel	4:50 PM	K10, Growth and Lift-Off of High-Quality GaN Thin Films Using Self-Assembled Silica Microsphere Monolayers .....Qiming Li

Wednesday PM June 23, 2010		Thursday AM June 24, 2010		Thursday AM June 24, 2010	
Session L: III-N HEMTs I Room: 155		**Session M: Graphene - Materials and Characterization Room: 102**		**Session N: Molecular Electronics and Chem / Bio Sensors Room: 126**	
1:30 PM	L1, Formation of Structural Defects in AlGaN/GaN High Electron Mobility Transistors under Electrical Stress .....Prashanth Makaram	8:20 AM	M1, (Invited), Material and Electronic Properties of CVD Graphene grown on Ni and Cu then Transferred to Insulators .....Yong Chen	8:20 AM	N1, STM Studies of Hybrid Inorganic-Organic Molecular Magnets on an Ultrathin Insulating Film .....Taeyoung Choi
1:50 PM	L2, (Student), Electrical Properties of GaN/AlN/GaN Heterostructures: Presence of 2DHG .....Satyaki Ganguly			8:40 AM	N2, (Student), Effect of Molecular Tilt Configuration and Interface Dipoles on Molecular Electronic Conduction .....Gunuk Wang
2:10 PM	L3, (Student), Study of Cause of G_m-Collapse for Higher Gate Voltages in N-Polar GaN HEMTs with Scaled GaN Channels .....Nidhi Nidhi	9:00 AM	M2, Fabrication and Characterization of Graphene Materials Grown via CVD on Copper Based Substrates .....Michelle Kelly	9:00 AM	N3, (Student), Improvement of Transfer Characteristics in Carbon Nanotube Field-Effect Transistors with Au Nano Clusters .....Yasuki Yamamoto
2:30 PM	L4, (Student), Polarization-Engineered Low-Leakage Buffers for Nitride HEMTs Grown by MBE .....Yu Cao	9:20 AM	M3, (Student), Kinetic Limitations in the Formation of Graphene on the C-face of SiC .....Luxmi Luxmi	9:20 AM	N4, Carbon Nanotube Field-Effect Transistor Biosensor with Schottky Barrier Control Gate Electrode .....Masuhiro Abe
2:50 PM	L5, (Student), The Influence of High-k Gate Dielectrics on Deep Traps in AlGaN/GaN High Electron Mobility Transistors Measured by Deep Level Spectroscopy Methods .....Qilin Gu	9:40 AM	M4, (Student), Graphene to Graphane: Novel Electrochemical Conversion and Possible Applications .....Kevin Daniels	9:40 AM	N5, (Student), Breakdown Statistics and Nanowire Device Integration of Self-Assembled Nano Dielectrics .....Ruth Anne Schlitz
3:10 PM	Break	10:00 AM	Break	10:00 AM	Break
3:30 PM	L6, PECVD-SiN, Si or Si/Al_2O_3-Capped ED-Mode AlN/GaN Inverters .....Tom Zimmermann	10:20 AM	M5, Growth of Few Layer Graphene on C-Face SiC .....Virgil Shields	10:20 AM	N6, Functionlization Studies on GaN Nanowires .....Devin Rourke
3:50 PM	L7, Late News	10:40 AM	M6, Graphene Growth on SiC, SiO_2, and Sapphire with Carbon Addition .....Jeonghyun Hwang	10:40 AM	N7, (Student), Olefin Metathesis Reaction on GaN (0001) Surfaces .....Matthew Makowski
4:10 PM	L8, Demonstration of Enhancement Mode AlN/Ultrathin AlGaN/GaN HEMTs Using Selective Wet Etching .....Travis Anderson	11:00 AM	M7, Ultrafast Transient Absorption Microscopy Studies of Carrier Dynamics in Epitaxial Graphene .....Libai Huang	11:00 AM	N8, (Student), Protection of ZnO Nanowires for Liquid-Phase Sensing .....Ashley Mason
4:30 PM	L9, (Student), Growth and Characterization of InGaN Heterojunction Bipolar Transistors .....Zachary Lochner	11:20 AM	M8, Comparison of Graphene Thickness Determination for MBE Grown Graphene on SiC using Raman, XPS, and TEM .....David Tomich	11:20 AM	N9, (Student) Signal-to-Noise Ratio Improvement of Magnetoelectric Laminate Sensor by Multilayer Structure and Direct Integration with Advanced Microelectronics .....Zhao Fang
4:50 PM	L10, (Student), High Temperature Transport Properties of GaN HEMTs with Various Heterostructure Designs .....Ronghua Wang	11:40 AM	M9, Late News	11:40 AM	N10, Late News

Thursday AM June 24, 2010		Thursday AM June 24, 2010		Thursday AM June 24, 2010	
Session O: SiC: Characterization and Growth Room: 129		**Session P: One-Dimensional Photovoltaics Room: 131**		**Session Q: Oxide Thin Films Room: 138**	
8:20 AM	O1, Analysis of Dislocation Interactions in Low Dislocation Density, PVT-Grown, Four-Inch Silicon Carbide Single Crystals ..... Michael Dudley	8:20 AM	P1, Fabrication of Individual Silicon Nanowire Radial Junction Solar Cells ..... Chito Kendrick	8:20 AM	Q1, Pulsed-dc Reactive Sputtering Vanadium Oxide Thin Films for Microbolometers ..... Bharadwaja Srowthi
8:40 AM	O2, Formation of a (5-1)-Bilayer-Height Complex Step-and-Terrace Structure on 4H-SiC (0001) by a Spiral Etching Process..... Jun Suda	8:40 AM	P2, Wire Textured Multicrystalline Silicon Solar Cells ..... Kejia Wang	8:40 AM	Q2, (Student), Defects in Low-κ; Dielectrics and Etch Stop Layers for Use as Interlayer Dielectrics in ULSI ..... Brad Bittel
9:00 AM	O3, Processes Controlling the Carrier Lifetime in n^- 4H-SiC Epilayers with low $Z_{1/2}$ Concentrations ..... Paul Klein	9:00 AM	P3, Efficiency Enhancements for Copper Contaminated Radial p-n Junctions over Planar p-n Junctions in Silicon ..... Alec Talin	9:00 AM	Q3, (Student), Nanocluster and Nanocrystalline Si Trap Distributions within $SiO_2/SiO_x/SiO_2$ Field Oxides for Radiation-Tolerant Electronics ..... Evan Katz
9:20 AM	O4, Comparative Studies of Carrier Dynamics in 3C-SiC Layers Grown on Si and 4H-SiC Substrates ..... Jawad Ul Hassan	9:20 AM	P4, (Student), Wafer Scale Si Nanowire Arrays for Photovoltaic Applications ..... Yi Jing	9:20 AM	Q4, (Student), Nanoscale Depth-Resolved Electronic Properties of HfO_2RPAN/Ge and HfSiON/RPAN/Ge Gate Dielectrics for Radiation-Tolerant Electronics ..... Zhichun Zhang
9:40 AM	O5, Expansion and Contraction of Stacking Faults in 4H-SiC ..... Nadeemullah Mahadik	9:40 AM	P5, Late News	9:40 AM	Q5, (Student), Nano-Gap Electrodes Formed at the Exposed Edge of Au/Al_2O_3/Au Tunnel Structures Grown by Atomic Layer Deposition ..... Bing Hu
10:00 AM	Break	10:00 AM	Break	10:00 AM	Break
10:20 AM	O6, Influence of Stacking Fault Generation and Half Loop Array on Electrical Behavior of 4H-SiC 10 kV PiN Diodes ..... Qingchun (Jon) Zhang	10:20 AM	P6, (Student), Branched ZnO/Si Nanowire Heterostructure Based Photoelectrochemical Cell for Efficient Water Splitting ..... Ke Sun	10:20 AM	Q6, (Student), Surface-Interface Conductivity in Thin Film Gd-doped CeO_2 ..... Matthew Swanson
10:40 AM	O7, Reducing Basal Plane Dislocation Density in Nitrogen and Aluminum Doped 4H-SiC Epilayers ..... Virginia Wheeler	10:40 AM	P7, Solar Cells Based on ZnO/ZnS Core-Shell Nanowires Arrays ..... Aurelien Du Pasquier	10:40 AM	Q7, Growth of Heteroepitaxial $SrRuO_3$ Electrodes on CeO_2 Buffered R-Plane Al_2O_3 Substrates by RF Magnetron Sputtering ..... Madhana Sunder
11:00 AM	O8, Improved Surface Morphology of 4H-Sic Homoepitaxial Layers Grown on Si-Face 4° off-Axis Substrates ..... Swapna Sunkari	11:00 AM	P8, (Student), Fabrication of Subwavelength Pillar Arrays on GaAs by Confined Self-Assembly Technique for Broadband Antireflection Coating ..... Dae-Seon Kim	11:00 AM	Q8, (Student), Evidence of Ferroelectricity Induced by Epitaxial Strain in Calcium Titanate Thin Films Grown by Molecular-Beam Epitaxy ..... Charles Brooks
11:20 AM	O9, (Student), High-Purity Semi-Insulating 4H-SiC Homoepitaxy at a High Growth Rate Using Dichlorosilane for High Power Devices ..... Iftekhar Chowdhury	11:20 AM	P9, (Student), Hybrid Solar Cell Based on Patterned Nanopillar/P3HT Heterojunction ..... Giacomo Mariani	11:20 AM	Q9, Synchrotron Spectroscopy Detection of Spin-Polarized Bands and Hopping-Induced Mixed Valence for Ti and Sc in $GdSc_{1-x}Ti_xO_3$ for x = 0.18 and 0.25 ..... Gerald Lucovsky
11:40 AM	O10, Vanadium Doping using VCl_4 Source during the Chloro-Carbon Epitaxial Growth of 4H-SiC ..... Yaroslav Koshka	11:40 AM	P10, Dissociation of Photo-Generated Excitons on Carbon Nanotubes at Type-II Heterojunctions ..... Dominick Bindl	11:40 AM	Q10, Application of Many Electron Charge Transfer Multiplet (CTM) Theory to Band Edge and Band Defect States in High-K Gate Dielectrics and Complex Functional Oxide Thin Films ..... Gerald Lucovsky

Thursday AM June 24, 2010		Thursday AM June 24, 2010		Thursday PM June 24, 2010	
Session R: ZnO Growth and Doping Room: 141		**Session S: Light Emitting Diodes and Laser Diodes Room: 155**		**Session U: Graphene and Nanotubes - Devices Room: 102**	
8:20 AM	R1, (Student), Nucleation Layer Based Optimization of MOCVD Grown ZnO by In Situ Laser Interferometry ..... Jens-Peter Biethan	8:20 AM	S1, Effect of Inaln Electron Blocking Layer in Visible Light-Emitting Diodes on Quantum Efficiency Grown by Metalorganic Chemical Vapor Deposition ..... Hee Jin Kim	1:30 PM	U1, (Student), Sub-20 nm Patterning of Graphene Nanoconstrictions Using Nanosphere Lithography and Characterization of Its Electronic Properties ..... Nathaniel Safron
8:40 AM	R2, (Student), Influence of Substrate Temperature and Post-Deposition Anneal on Material Properties of Ga-Doped ZnO Prepared by Pulsed Laser Deposition ..... Robin Scott	8:40 AM	S2, (Student), Fabrication of GaN-based Laser Diode and Laser Diode Facet Formation ..... Wenting Hou	1:50 PM	U2, (Student), Carrier Transport in Graphene P-N Junctions ..... Tian Fang
9:00 AM	R3, Epitaxial Electrochemical-Deposition of ZnO on Graphite and p-GaN Substrates ..... Kazuyuki Uno	9:00 AM	S3, Performance Improvement of Alingan Visible Laser Diodes by Epitaxial Layer Design ..... Jianping Liu	2:10 PM	U3, Epitaxial Graphene Materials Integration: Effects of Dielectric Overlayers on Structural and Electronic Properties ..... Joshua Robinson
9:20 AM	R4, (Student), Control of ZnO Epitaxial Growth via Focused Ion Beam Induced Damage in Lattice-Mismatched Substrates ..... Blake Stevens	9:20 AM	S4, (Student), Enhancement of the Light-extraction Efficiency of GaN-based Light-emitting Diodes using a Graded-Refractive-Index Layer ..... Byung-Jae Kim	2:30 PM	U4, Comparison of Ballistic Performance of Graphene and Planar III-V MOSFETs for RF Low Voltage Applications ..... Lingquan (Dennis) Wang
9:40 AM	R5, Properties of Nitrogen Molecules in ZnO ..... Norbert Nickel	9:40 AM	S5, (Student), Nano-Fabrication of Green AlGaInN LEDs – Structural Wavelength Control and Enhanced Light Extraction ..... Christoph Stark	2:50 PM	U5, Graphene Fundamental Trade-offs and Asymmetric Bandgap Opening ..... Frank Tseng
10:00 AM	Break	10:00 AM	Break	3:10 PM	Break
		Session T: AlGaN Growth and Devices Room: 155			
10:20 AM	R6, High-Quality p-Type ZnO Layers Grown by Co-Doping of N and Te ..... Seunghwan Park	10:20 AM	T1, (Student), Polarization Induced p-Doped Nitride Quantum Well UV LEDs ..... Jai Verma	3:30 PM	U6, Hall Effect Mobility of Epitaxial Graphene on Si-Face SiC ..... Shin Mou
10:40 AM	R7, Magnetic Properties of Mn and N Doped ZnO .....Mathrubhutham Rajagopalan	10:40 AM	T2, Structural Characterization of Highly Conducting $Al_xGa_{1-x}N$ (x >50%) for Deep Ultraviolet Light Emitting Diode ..... Joseph Dion	3:50 PM	U7, (Student), Highly Efficient Photovoltaic Devices with Transparent Graphene Electrode and TiOX Layer ..... Minhyeok Choe
11:00 AM	R8, Effects of p-Type Doping on the ZnO Based Diluted Magnetic Semiconductor Thin Films ..... Liping Zhu	11:00 AM	T3, Epitaxial Growth and Doping of AlGaN alloys on AlN Single Crystal Substrates ..... Ramón Collazo	4:10 PM	U8, (Student), Integrated Circuits Based on Carbon-Nanotube Transistors and Amorphous-Carbon Thin-Film Load Resistors .....Hyeyeon Ryu
11:20 AM	R9, (Student), Hydrothermal Synthesis of Wide Bandgap $Be_xZn_{1-x}O$ Nanorods for Solar Blind Photodetection ..... Ke Sun	11:20 AM	T4, (Student), Morphological Development of Homoepitaxial AlN Thin Films Grown by MOCVD ..... Anthony Rice	4:30 PM	U9, Late News
11:40 AM	R10, (Student), Synthesis and Charaterization of p-NiO/n-ZnO Heterojunction Diode by Spray Pyrolysis ..... Namseok Park	11:40 AM	T5, (Student), Aluminum Gallium Nitride Alloys Grown via Metal Organic Vapor Phase Epitaxy using Digital Alloy Growth Technique ..... L. Rodak	4:50 PM	U10, Late News

Thursday PM June 24, 2010		Thursday PM June 24, 2010		Thursday PM June 24, 2010	
Session V: Quantum Dots, Boxes, and Wires Room: 126		**Session W: Semiconducting and Metallic Nanowires Room: 129**		**Session X: Narrow Bandgap Semiconductors: Infared Detectors and Lasers Room: 131**	
1:30 PM	V1, Toward Conversion from Electron Pairs to Photon Pairs in Quantum Dots ..... Ikuo Suemune	1:30 PM	W1, (Student), Single Crystalline Wurtzite GaAs Nanoneedles Epitaxially Grown on Highly Lattice-Mismatched Sapphire with Bright Luminescence ..... Wai Son Ko	1:30 PM	X1, Minority Carrier Lifetime in LWIR Type II Superlattice Detector Structures Using Time-Resolved Photoluminescence .....Blair Connelly
1:50 PM	V2, Tensile-Strained Self-Assembled III-V Nanostructures ..... Paul Simmonds	1:50 PM	W2, Twinning Superlattice in VLS Grown <110> Planar GaAs Nanowires Induced by Impurity Doping ..... Xiuling Li	1:50 PM	X2, (Student), MOCVD Growth of InAs/GaSb Type-II Superlattice Structures and Photodiodes for Mid-Infrared Detection ..... Yong Huang
2:10 PM	V3,(Student), Self-Assembled $In_{0.5}Ga_{0.5}As$ Quantum Dots on GaP(001) ..... Yuncheng Song	2:10 PM	W3, (Student), Photoluminesence of InGaAs Nano-Pillar Arrays on GaAs Substrate ..... Joshua Shapiro	2:10 PM	X3, (Student), Investigation of Passivation Techniques on InAs/GaSb Strained Layer Superlattice Long Wave Infrared Detectors ..... Maya Narayanan Kutty
2:30 PM	V4, Late V4, (Student), Time-Resolved Spectroscopy of Single Colloidal CdSe Nanowires with Picosecond Resolution ..... Joseph Herzog News	2:30 PM	W4, (Student), Synthesis and Characterization of GaAs/MnAs Core/Shell Nanowires ..... Nicholas Dellas	2:30 PM	X4, (Student), Investigation of Antimonide Infrared Detectors Based on the nBn Design ..... Stephen Myers
2:50 PM	V5, Late News	2:50 PM	W5, (Student), Contact Laser Annealing Effects on Indium Oxide Nanowire Transistors ..... Seongmin Kim	2:50 PM	X5, Late News
3:10 PM	Break	3:10 PM	Break	3:10 PM	Break
3:30 PM	V6, Resonant Periodic Gain InAs Quantum Dot VECSEL ..... Alexander Albrecht	3:30 PM	W6, (Student), Vertical InSb Nanowire Arrays Electrodeposited into Porous Anodic Alumina Templates on Silicon Substrates ..... Suprem Das	3:30 PM	X6, (Student), Quinternary GaInAsSbP on GaAs Substrates Grown by Metal Organic Vapor Phase Epitaxy (MOVPE) ..... Toby Garrod
3:50 PM	V7, Quantum Dot Light Emitting Devices and Exciton Recombination Zone ..... Seonghoon Lee	3:50 PM	W7, (Student), High Growth Rate and Control of Stanking Faults on InP Semiconductor ..... Thalita Chiaramonte	3:50 PM	X7, (Student), Growth of $GaAs_{1-x}Bi_x/Al_yGa_{1-y}As$ Multi-Quantum Well Structures on GaAs ..... Takuma Fuyuki
4:10 PM	V8, (Student), Thermal Stability in Emission Peak in Multilayer InAs/GaAs Quantum Dot Heterostructure in Laser Application ..... Subhananda Chakrabarti	4:10 PM	W8, Formation of Periodic Nanostructures through Kirkendall Constitutional Interdiffusion in Epitaxial Heterostructures ..... Patrick Taylor	4:10 PM	X8, (Student), Perforated (In)GaSb Quantum Wells on GaSb Substrates through the Use of As_2 Based In-Situ Etches ..... P. Ahirwar
4:30 PM	V9, Enhancement of Luminescence Efficiency in InAs/GaAs Quantum Dots by Proton Irradiation ..... Subhananda Chakrabarti	4:30 PM	W9, (Student), Thermal Conductivity of Aluminum Nanowires near Room Temperature: Direct Measurements and Theory ..... Nenad Stojanovic	4:30 PM	X9, (Student), Antimonide VECSELs on AlGaAs DBRs ..... T. J. Rotter
4:50 PM	V10, Late News	4:50 PM	W10, Simulation of the Influence of Grain Boundaries on Resistivity via the Wigner-Fokker-Planck Equation ..... Richard Sharp	4:50 PM	X10, (Student), Effect of Aluminum Composition on Current-Voltage Characteristics of AlGaSb/InAs Tunnel Junction ..... Yeqing Lu

Thursday PM June 24, 2010		Thursday PM June 24, 2010		Thursday PM June 24, 2010	
Session Y: III-N Nanostructures Room: 138		**Session AA: Oxide Defects, Localized States, and Nanostructures Room: 141**		**Session BB: III-V Novel Electronic Devices Room: 155**	
1:30 PM	Y1, (Student), Dislocation Filtering in GaN Nanorods ..... Robert Colby	1:30 PM	AA1, Vacancy Defect and Defect Cluster Energetics in Ion-Implanted ZnO ..... Leonard J. Brillson	1:30 PM	BB1, (Student), Demonstration and Room Temperature Electrical Characteristics of a Nitride Hot Electron Transistor with GaN Base of 10 nm ..... Sansaptak Dasgupta
1:50 PM	Y2, (Student), Threading Defect Elimination in GaN Nanostructures .....Ashwin Rishinaramangalam	1:50 PM	AA2, O-H-Li-Complex in Hydrothermally Grown Single Crystalline ZnO ..... Klaus Magnus Johansen	1:50 PM	BB2, (Student), Novel Cs-free GaN Photocathodes .... Fatemeh (Shadi) Shahedipour-Sandvik
2:10 PM	Y3, (Student), Yellow-Orange Luminescence from III-Nitride Nanopyramid Heterostructures ..... Isaac Wildeson	2:10 PM	AA3, Induced Gap States at Zinc Oxide Surfaces and Interfaces ..... S.M. Durbin	2:10 PM	BB3, Influence of MOVPE Growth Conditions on Intersubband Absorption in AlN –AlGaN Superlattices ..... Andrew Allerman
2:30 PM	Y4, (Student), Molecular Beam Epitaxial Growth and Characterization of InGaN/GaN Dot-in-a-Wire Nanoscale Heterostructures on Si..... Jiale Wang	2:30 PM	AA4, Optical Properties of Gd Implanted ZnO Single Crystals ..... John Kennedy	2:30 PM	BB4, (Student), Engineering Ferromagnetism in Gd-Doped GaN Two-Dimensional Electron Gases ..... Jing Yang
2:50 PM	Y5, (Student), Electrochemical Etching of GaN and Its Applications ..... Yu Zhang	2:50 PM	AA5, High-Resolution Laplace DLTS on $Mg_xZn_{1-x}O$ PLD Thin Films ..... Holger von Wenckstern	2:50 PM	BB5, Nearly Ideal Current-Voltage Characteristics of Schottky Barrier Diodes Directly Formed on GaN Free-Standing Substrates..... Jun Suda
3:10 PM	Break	3:10 PM	Break	3:10 PM	Break
Session Z: Point and Extended Defects and Doping in Wide Bandgap Materials Room: 138				**Session CC: III-N HEMTs II Room: 155**	
3:30 PM	Z1, Luminescence Recombination Dynamics of Ytterbium Implanted GaN Epilayers ..... Jingzhou Wang	3:30 PM	AA6, (Student), Observation of a Strong Polarization Induced Quantum-Confined Stark Effect in $Mg_XZn_{1-X}O$/Zno Quantum Wells ..... Matthias Brandt	3:30 PM	CC1, (Student), High Al Composition $Al_{0.72}Ga_{0.28}N$/AlN/GaN Heterostructures with High Mobility Two-Dimensional Electron Gases ..... Guowang Li
3:50 PM	Z2, Energy Levels of Nd^{3+} Ions in <I>In Situ</I> Doped AlN ..... Grace Metcalfe	3:50 PM	AA7, Low Temperature Electrochemical Growth of ZnO Nanobelts, Nanowalls, Nanospikes and Nanowires: Growth Mechanism and Field Emission Study ..... Debabrata Pradhan	3:50 PM	CC2, (Student), Two-Dimensional Electron Gas in $In_XAl_{1-X}N$/Aln/GaN Heterostructure Field-Effect Transistors Depending on Indium Composition ..... Suk Choi
4:10 PM	Z3, Correlation of InGaN Growth Parameters, Defects and MQW Radiative Efficiency for Blue to Green Emission ..... Andrew Armstrong	4:10 PM	AA8, (Student), Synthesis and Field Emission Characterizations of Well-Aligned Single-Crystal Al-Doped Zno Nanowires Grown at Low Temperature ..... Po-Yu Yang	4:10 PM	CC3, Source-Drain Regrowth by MBE in Metal-Face AlN/GaN HEMTs ..... Chuanxin Lian
4:10 PM	Z4, (Student), Proton-Irradiated AlGaN/GaN HEMT at 5 MeV Protons ..... Hong-Yeol Kim	4:30 PM	AA9, (Student), Correlation of ZnO Polar Surface Nanostructure with Native Point Defects ..... Tyler Merz	4:30 PM	CC4, (Student), AlGaN/GaN High Electron Mobility Transistors for Large Current Operation Achieved by Selective-Area Growth Using Plasma-Assisted Molecular Beam Epitaxy ..... Liang Pang
4:30 PM	Z5, Effect of Traps Spatial Localization on GaN HEMT Static Characteristics ..... Alessandro Chini	4:50 PM	AA10, (Student), Evolution and Growth of Nanostructures on ZnO with Staged Annealing ..... Daniel Doutt	4:50 PM	CC5, Transport Studies of AlGaN/GaN Heterostructures with Variable SiN_x Passivant Stress ..... Giacinta Parish

Friday AM June 25, 2010		Friday AM June 25, 2010		Friday AM June 25, 2010	
Session DD: Oxide Semiconductor Heterojunction Diodes Room: 102		**Session EE: Epitaxy Materials and Devices Room: 126**		**Session FF: Si and Ge Nanowires Room: 129**	
8:20 AM	DD1, Ultraviolet Photodetectors with Novel Oxide Thin Films ..... Shizuo Fujita	8:20 AM	EE1, (Student), Overgrowth Investigation of Epitaxial Semimetallic Nanoparticles for Photonic Devices ..... Adam Crook	8:20 AM	FF1, (Student), The Influence of the Catalyst on Dopant Incorporation During Si and Ge Nanowire Growth ..... Justin Connell
8:40 AM	DD2, (Student), Polarization-sensitive Schottky Photodiodes Based on A-plane ZnO/ZnMgO Multiple Quantum-wells ..... Gema Tabares	8:40 AM	EE2, (Student), Regrown InGaAs Tunnel Junctions for TFETs ..... Guangle Zhou	8:40 AM	FF2, Size Effects in Semiconductor Nanowire Synthesis at the Ultimate Limit ..... Shadi Dayeh
9:00 AM	DD3, A New Approach to Make ZnO-Cu_2O Heterojunctions for Solar Cells ..... Aurelien Du Pasquier	9:00 AM	EE3, (Student), Molecular Beam Epitaxy of Very Thin Fluoride Films on Ge(111) and its Application to Resonant Tunnelling Diodes ..... Keita Takahashi	9:00 AM	FF3, (Student), Growth and Applications of Silicon/Germanium Axial Nanowire Heterostructures ..... Cheng-Yen Wen
9:20 AM	DD4, (Student), Double Heterojunction Metal-Semiconductor-Metal Photodetector Using Zno/Si Structure ..... Tingfang Yen	9:20 AM	EE4, (Student), Hole Mobility Improvement in Strained InGaSb Quantum Well with Carbon Doping ..... Chichih Liao	9:20 AM	FF4, (Student), SiGe/Si Selective Etch Structures for Nanowire Release and Assembly ..... Sharis Minassian
9:40 AM	DD5, (Student), A Study of Indium Doped-ZnO/p-Si(111) Diode Characteristics with Various In Mole Fraction ..... Jong Hoon Lee	9:40 AM	EE5, (Student), Growth and Thermal Conductivity of Polycrystalline GaAs Grown on CVD Diamond using Molecular Beam Epitaxy ..... Stephen Clark	9:40 AM	FF5, Diffusion Formation of Nickel Silicides Contacts in Silicon Nanowires ..... Michael Beregovsky
10:00 AM	DD6, (Student), Effects of High - Energy Electron Irradiation on Pd/ZnO/Si MSM Photodetector: Conduction Mechanisms and Radiation Resistance ..... Franklin Catalfamo	10:00 AM	Break	10:00 AM	Break
10:20 AM	Break	10:20 AM	EE6, Thick HVPE Growth of Patterned Semiconductors for Nonlinear Optics ..... Candace Lynch	10:20 AM	FF6, (Student), Comparative Study of Ni-silicide and Germanide Formation in Contacts to Si and Ge Nanowires .....Nicholas Dellas
10:40 AM	DD7, Late News	10:40 AM	EE7, (Student), Effects of Carrier Localization on Emission Spectra of Dilute GaAsN Materials Doped with Silicon ..... Yan He	10:40 AM	FF7, (Student), High Responsivity Vertical Si Nanowire Photodetector Arrays .....Yi Jing
11:00 AM	DD8, Late News	11:00 AM	EE8, (Student), Fabrication and Characterization of Free-Standing InGaAs/GaAs Quantum Dot Microbelt-like Optical Resonators ..... Feng Li	11:00 AM	FF8, Si Nanowire Mats for Large-area Electronics .....William Wong
11:20 AM	DD9, Late News	11:20 AM	EE9, MBE Grown InGaAsSbN/GaSb Single Quantum Wells for Mid-Infrared Applications ..... Sudhakar Bharatan	11:20 AM	FF9, Jet-printed and Dielectrophoretically Aligned Nanowires for Large Area Electronics .....Sourobh Raychaudhuri
11:40 AM	DD10, Late News	11:40 AM	EE10, Late News	11:40 AM	FF10, Late News

Friday AM June 25, 2010		Friday AM June 25, 2010		Friday AM June 25, 2010	
Session GG: Thermoelectrics and Thermionics Room: 131		**Session HH: Semiconductor Processing, Surfaces and Contacts Room: 138**		**Session II: Heteroepitaxy on Silicon Room: 141**	
8:20 AM	GG1, (Student), Bulk-like Thermionic Energy Conversion Device Fabricated from Laminated Nanostructured Metal/ Semiconductor Superlattices ..... Jeremy Schroeder	8:20 AM	HH1, (Student), Effect of Contact Modification on Charge Transport at Different Length Scales in Poly(3-Hexylthiophene)-Based Bottom-Contact Field-Effect Transistors ..... Kumar Singh	8:20 AM	II1, (Student), Reduction in Operation Voltage of Light Emitting Diodes Fabricated in Si/III-V-N/Si Heterostructure ..... Keisuke Yamane
8:40 AM	GG2, (Student), Epitaxial Growth of Transition Metal Nitrides on MgO via DC Magnetron Sputtering ..... Robert Wortman	8:40 AM	HH2, (Student), Low Pressure Chemical Vapor Deposition of Conformal Boron Thin Films on Deep RIE-Etched Si Substrates ..... Nicholas LiCausi	8:40 AM	II2, GaN/AlN Heterostructures on Vertical {111} Fin Facets of Si (110) Substrates ..... Mark Holtz
9:00 AM	GG3, (Student), Enhancement of Thermoelectric Efficiency in $Si_{1-x}Ge_x$/Si Heterostructures ..... Md Hossain	9:00 AM	HH3, (Student), Assessment of the Passivation Capabilities of Two Different Covalent Modifications on GaP (100) ..... David Richards	9:00 AM	II3, (Student), 2µm Thick Device Quality GaN on Si(111) Using AlGaN Graded Buffer ..... Benjamin Leung
9:20 AM	GG4, Isothermal Method for Rapid, Steady-State Measurement of Thermoelectric Materials and Devices ..... Patrick Taylor	9:20 AM	HH4, (Student), Comparison of Ga-Polar and N-Polar GaN by KOH Photoelectrochemical Etching ..... Younghun Jung	9:20 AM	II4, (Student), Compositionally-graded Layers Composed of Tandem InGaAs InGaP Alloys and Pure GaAsSb Alloys to Engineer the InP Lattice Constant on GaAs Substrates ..... Li Yang
9:40 AM	GG5, Late News	9:40 AM	HH5, (Student), N-Type Electrodes for GaN-Based Vertical Light Emitting Diodes ..... Tae-Yeon Seong	9:40 AM	II5, Characterization of Standard and Ferromagnetic Schottky Barriers on GaP/GaP and GaP/Si Epi-Layers ..... Chris Ratcliff
10:00 AM	Break	10:00 AM	Break	10:00 AM	Break
10:20 AM	GG6, (Student), Thermomagnetic Transport Properties of $(Ag_xSbTe_{x/2+1})_{15}(GeTe)_{85}$ Thermoelectric Materials ..... Yi Chen	10:20 AM	HH6, (Student), In-situ Ohmic Contacts to p-InGaAs ..... Ashish Baraskar	10:20 AM	II6, Silicon Nanostructures Ion Implanted with Carbon and Nitrogen as an Electron Emitting Device ..... Damian Carder
10:40 AM	GG7, (Student), Thermoelectric Properties of Sn-Rich $Pb_{1-x}Sn_xTe$ Alloys Doped with Indium ..... Yibin Gao	10:40 AM	HH7, (Student), Degradation of Ohmic and Schottky Contacts on InGaAs MHEMTs during Bias Stressing ..... Erica Douglas	10:40 AM	II7, High-Quality (211)B CdTe on (211) Si Substrates Using Metal-Organic Vapor-Phase Epitaxy ..... Sunil Rao
11:00 AM	GG8, (Student), Incorporation of $AgSbTe_2$ to $Pb_{1-x}Sn_xTe$ by Mechanical Alloying of End Compounds ..... Aaron D. LaLonde	11:00 AM	HH8, (Student), Characterization of Thin InAlP Native Oxide Gate Dielectric Layers for GaAs MOSFET Applications ..... Wangqing Yuan	11:00 AM	II8, (Student), Metalorganic Vapor Phase Epitaxial Growth of (211)CdTe on Nanopatterned (211)Ge/Si Substrates using Full Wafer Block Copolymer Lithography ..... Shashidhar Shintri
11:20 AM	GG9, (Student), Electron Transport Properties of Mechanically Alloyed N-type $Pb_{1-x}Sn_xTe$ Thermoelectric Elements ..... Lakshmi Krishna	11:20 AM	HH9, Post-Growth InGaAsP Quantum Well Intermixing for High Saturation Power Semiconductor Optical Amplifiers ..... Jonathan Klamkin	11:20 AM	II9, (Student), Effects of Ex-Situ Cycle Annealing on Dislocation Densities of HgCdTe/CdTe/Si Layers ..... Stuart Farrell
11:40 AM	GG10, Late News	11:40 AM	HH10, Late News	11:40 AM	II10, Late News

Friday AM June 25, 2010	
Session JJ: Nonpolar-Semipolar III-Ns Room: 155	
8:20 AM	JJ1, (Student), Internal Quantum Efficiency of Polar and Non-Polar GaInN/GaN Multiple Quantum Wells ..... Liang Zhao
8:40 AM	JJ2, (Student), Optical Polarization of Non-polar GaInN/GaN LEDs ..... Shi You
9:00 AM	JJ3, (Student), Anisotropic Carrier Mobility in GaN Quantum Well Grown in Non-polar Direction: Polarization Induced Dipole and Interface Roughness Scattering ..... Aniruddha Konar
9:20 AM	JJ4, MBE Growth of Nitrogen-Face Aluminum Nitride by Polarity Inversion Using Magnesium Overdoping ..... Craig Moe
9:40 AM	JJ5, Electro-Thermo-Mechanical Simulation of AlGaN/GaN HFETs and MOSHFETs ..... Anusha Venkatachalam
10:00 AM	Break
Session KK: Indium Nitride Room: 155	
10:20 AM	KK1, Mg Doped InN and Search for P-type InN ..... Ke Wang
10:40 AM	KK2, (Student), Dislocation Reduction via Epitaxial Lateral Overgrowth of InN by Selective-area-growth of RF-MBE ..... Jumpei Kamimura
11:00 AM	KK3, Growth Orientation Control of InN by Pulsed eXcitation Deposition ..... Hiroshi Fujioka
11:20 AM	KK4, (Student), Optical and Electrical Transport Properties of Nearly Intrinsic and Si-doped InN Nanowires ..... Yi-Lu Chang
11:40 AM	KK5, (Student), Growth Optimization of Si_3N_4 on GaN by Metal-Organic Chemical Vapor Deposition ..... Brian Swenson

Plenary Session

Wednesday AM Room: Jordan Auditorium, Mendoza College of Business
June 23, 2010 Location: University of Notre Dame

8:20 AM Awards Ceremony

8:30 AM Plenary
Epitaxial Graphene: Designing a New Electronic Material: *Walter A. de Heer*[1]; [1]Georgia Institute of Technology

Since 2001 the Georgia Tech epitaxial graphene research team and its collaborators have developed the new field of epitaxial graphene electronics. The current status of epitaxial graphene research will be presented, including the production methods and recent results from various characterization investigations. Methods have been developed to grow monolalyer and multilayer epitaxial graphene (MEG) on the C-face of hexagonal silicon carbide with of up to 100 graphene sheets and its extraordinary transport properties have been demonstrated, including the quantum Hall effect. The monolayer films have high mobilities and exhibit the half integer quantum Hall effect. The Georgia Tech Confinement Controlled Sublimation method to produce uniform epitaxial graphene layers will be explained. Surprisingly, the properties of MEG are closely related to monolayer graphene rather than graphite, as a result of an unusual rotational stacking of the graphene layers that causes the graphene sheets to electronically decouple. Consequently the electronic band structure of MEG is composed of Dirac cones. The charge carriers are chiral and exhibit a non-trivial Berry 's phase. Weak anti-localization and quantum confinement has been demonstrated. Landau level spectroscopy further exhibits record-breaking room temperature mobilities and well resolved Landau levels below 1 T, indicating extremely low carrier densities and good homogeneity of the material. Efforts towards large-scale electronic device patterning will be reviewed.

9:20 AM Break

Session A: High-K Gate Dielectrics

Wednesday AM Room: 102
June 23, 2010 Location: University of Notre Dame

Session Chairs: John Conley, Oregon State University; Peter Moran, Michigan Technological University

10:00 AM Invited
A1, The Electrical Properties of Metal/Gd_2O_3/Si Gate Stacks and Their Dependence on the Structure of the Oxide Layer: *Moshe Eizenberg*[1]; Eran Lipp[1]; [1]Technion-Israel Institute of Technology

Future downscaling of metal-oxide-semiconductor (MOS) devices relies on the successful introduction of high-k dielectrics and metal electrodes, which will replace the traditional poly-Si/SiO_2 gate-stack. Gd_2O_3 is one of the only materials that have been reported to suit the industry's requirements for 2016. In addition, Gd_2O_3 has a low lattice mismatch to Si, which enables the growth of a single-crystalline oxide layer. Additional structures can be obtained by controlling the oxide growth temperature and substrate orientation. The aim of this research is to study the effect of oxide structure on the electrical properties of metal/Gd_2O_3/Si gate stacks. Electrical properties were studied by examining MOS capacitors with either Pt or Ta as the metal gates. Three different structures of Gd_2O_3 were deposited by molecular-beam epitaxy (MBE). Amorphous layers were deposited at 90°C, while layers deposited at 600°C were crystalline, and their morphology was observed to depend on the Si orientation. Single-crystalline layers were obtained on Si(111), whereas on Si(100), domain-structured layers were obtained. In the case of domain-structured Gd_2O_3, a silicate-like interfacial layer was observed at the oxide/Si contact. Electrical measurements revealed that the k-value of this interfacial layer is lower than that of the oxide itself. The electrical properties of Gd_2O_3 were observed to be almost independent of the oxide structure. The oxide k-value was similar for all structures, however, the k-value of domain-structured Gd_2O_3 (17.7± 0.8) was somewhat higher than those of single-crystalline (16.3± 0.7) and amorphous (16.9± 0.8) layers. The electron effective mass in crystalline Gd_2O_3 was found to be (0.1± 0.02)•me, while for amorphous layers, a value of (0.5± 0.1)•me was obtained. The conduction mechanism through crystalline Gd_2O_3 was found to be contact-limited in most of the measured conditions; with a barrier height of (0.6± 0.1) eV at Pt/Gd_2O_3 interfaces. This value is explained by the existence of a defect-related energy band in the oxide. In contrast to the oxide properties, the extent of Fermi-level pinning at metal/Gd_2O_3 interfaces was found to be significantly affected by the oxide structure. At metal/single-crystalline Gd_2O_3 interfaces, Fermi-level pinning was negligible, while at metal/amorphous Gd_2O_3 interfaces, a dominant pinning effect could be observed. These results are explained in terms of the metal-induced gap states model.

10:40 AM Student
A2, Spin Dependent Trap Assisted Tunneling in Gd_2O_3 Dielectrics: *Brad Bittel*[1]; P.M. Lenahan[1]; E. Lipp[2]; M. Eizenberg[2]; [1]Penn State Univ.; [2]Technion-Israel Institute of Technology

We report on magnetic resonance detected via spin dependent trap assisted tunneling (SDT) in MBE deposited epitaxial single crystal Gd_2O_3[1-3] films 3.6nm thick on (111) Si substrates. In previous publications, we reported on the electrical properties, as well as the thermal stability of these films.[3-5] SDT is a relatively new technique;[6] this work represents the first report of the technique's utilization on Gd_2O_3 and, to the best of our knowledge, the first report of SDT on any epitaxial dielectric film on silicon. In SDT a magnetic resonance induced change in a trap assisted tunneling current is generated by simultaneously exposing the device under observation to a large magnetic field and microwave irradiation such that the microwave frequency and magnetic field satisfy the magnetic resonance condition of a defect with levels playing dominating roles in trap assisted tunneling. In our study, we observe a single magnetic resonance line characterized by g=1.9996 and a peak to peak line with of 14 Gauss. The SDT response is strongly bias dependent. We are unable to detect any SDT response for positive gate polarities and observe an SDT response in which the absolute amplitude which grows monotonically with increasing negative gate magnitudes, up to the point that our preamplifiers saturate. However, the relative strength of the SDT response, that is the ratio of the SDT induced tunneling current change divided by the absolute magnitude of the tunneling current is fairly sharply peaked, at a gate bias of approximately minus one volt. Our results are consistent with a defect with levels in the upper part of the Gd_2O_3 band gap. Such a defect level may explain the findings of our conductivity studies, which also indicate the existence of a defect-related energy state in the oxide band-gap. A fairly extensive literature dealing with conventional electron paramagnetic resonance measurements on large volume samples containing Gd_2O_3 exists.[7-9] These studies almost invariably report observation of a spectrum with a zero crossing g = 2.0 which is generally assigned to Gd^{3+} ions. We cannot at this point in our study conclude that the observed SDT response has the same origin, and note only that such an assignment appears to be plausible. [1] M. Czernohorsky, et al., Appl. Phys. Lett. 88, 152905 (2006). [2]Q.Q. Sun, et al., Appl. Phys. Lett. 92, 152908 (2008). [3]E. Lipp, et al., MRS Proc. 996E, H03-08 (2007). [4] E. Lipp, et al., Appl. Phys. Lett. 93, 193513 (2008). [5] E. Lipp, et al., J. Appl. Phys. 106, 113505 (2009). [6]J.T. Ryan, et al., Appl. Phys. Lett. 95, 103503 (2009). [7]D.L. Griscom, J. Non-Cryst. Solids. 40, 211 (1980). [8]C.M. Brodbeck, J. Chem. Phys. 83, 4285 (1985).[9]I. Ardelean et al., J. Non-Cryst. Solids. 353, 2363 (2007).

11:00 AM
A3, Crystalline Lattice-Matched $Ba_{0.7}Sr_{0.3}O$ on Si(001) as Gate Dielectric: *Herbert Pfnür*[1]; Dirk Müller-Sajak[1]; Alexander Cosceev[1]; Karl Hofmann[1]; [1]Leibniz Universität Hannover

The alkaline-earth metal oxides BaO and SrO as insulators with high relative dielectric constants of 34 and 14.5, and with band gaps of 4.2 and 6.3 eV, respectively, crystallize in the cubic rock salt structure and are miscible. As we have demonstrated previously, the mixed oxide $Ba_{0.7}Sr_{0.3}O$ can be grown

epitaxially with the average lattice constant of Si (5.43 Å) as a lattice-matched monocrystalline film on Si(001), with a band gap of 4.3 eV and conduction and valence band offsets of approximately 1.0 eV and 2.2 eV to Si. Oxide films with thicknesses between 5 and 20 nm were prepared by molecular beam epitaxy with the samples at room temperature. Pure BaO and SrO grow only as amorphous layers because of their significant lattice mismatch (+2.4% of BaO, -5.2% for SrO) with respect to Si(001). For the mixture of 70% BaO and 30% SrO, however, perfectly crystalline $Ba_{0.7}Sr_{0.3}O$ films were grown, as revealed by X-ray photoelectron spectroscopy (XPS) and LEED. The interface to Si(001) is atomically sharp with no formation of SiO_2 or silicide. For the electrical measurements, Au/$Ba_xSr_{1-x}O$/n-Si(001) MOS capacitors were fabricated by growing a 110 nm thermal SiO_2 layer, by lithographical patterning of active windows, and by deposition of the $Ba_xSr_{1-x}O$ films and Au metal gates in situ through openings in a tungsten mask overlapping the active windows. These diodes were analyzed by C-V and I-V measurements. They exhibited typical high-frequency C-V curves without frequency dispersion in the frequency range between 50 kHz and 1 MHz. All C-V curves had only negligible hystereses (<1 mV), indicating the absence of significant rechargeable trap densities in the oxides. The flatband voltages are within 0.3 V of the expected Au/n-Si work function differences, suggesting the absence of larger oxide charges. The effective dielectric constants $\varepsilon_{eff} = C_{acc,max} \times d_{ox}/\varepsilon_0$ determined within a 3-element model are only slightly (10-15%) below the bulk values, which indicates the absence of appreciable interface layers. The leakage current density (at $V_G = V_{FB}+1V$) is comparatively large in the amorphous diodes, but it is several orders of magnitude lower (2.1×10^{-5}A/cm^2) in the crystalline $Ba_{0.7}Sr_{0.3}O$ diode. The $Ba_{0.7}Sr_{0.3}O$ diode has a minimum interface trap density value, D_{it}, of only 6.3×10^{10} cm^{-2}eV^{-1}, two orders of magnitude below the amorphous oxides. These very low D_{it} values are comparable to those of the SiO_2/Si interface. Both low leakage currents and low D_{it} seem to be related to the perfectly lattice matched crystalline $Ba_{0.7}Sr_{0.3}O$/Si interface. We conclude that the crystalline gate oxide $Ba_{0.7}Sr_{0.3}O$ displays remarkable electrical properties without any (N_2/H_2) postdeposition annealing procedures: high effective dielectric constant, absence of hysteresis, low leakage currents, and very low interface trap densities in the range of SiO_2/Si.

11:20 AM Student

A4, Rare-Earth Scandates/Tin Gate Stack on High Mobility Strained SOI for Fully Depleted (FD) Mosfets: *Eylem Durgun Özben*[1]; J. M. J Lopes[1]; A. Nichau[1]; R. Luptak[1]; Roeckerath[1]; S. Lenk[1]; A. Besmehn[1]; B. Ghyselen[1]; Q.-T. Zhao[1]; J. Schubert[1]; S. Mantl[1]; [1]Jülich Research Center

High permittivity materials are needed for high performance applications in CMOS technology. Among those materials, rare-earth scandates ($REScO_3$, RE= Tb, Gd, La..) have gained considerable attention due to their excellent properties [1]. They show high thermal stability on silicon ranging from 800°C to 1000°C, κ values in the range of 23-29 and large optical band gaps (>5 eV) and band offsets to silicon (2-2.5 eV) [2 and references therein]. Silicon on insulator (SOI) and strained silicon on insulator (sSOI) are considered as promising channel materials for MOSFETs due to excellent dielectric isolation between devices, reduction in parasitic capacitance and increase in circuit speed. In this study, we have investigated Terbium scandate ($TbScO_3$), Gadolinium scandate ($GdScO_3$) and Lanthanum scandate ($LaScO_3$) as gate dielectrics on SOI and sSOI substrates in fully depleted (FD) MOSFETs. $TbScO_3$ and $GdScO_3$ films were grown by electron beam evaporation while $LaScO_3$ films were grown by molecular beam deposition. Device preparations were carried out with a conventional gate last process (for $GdScO_3$) and a replacement gate process (for $TbScO_3$ and $LaScO_3$). The composition of the films was measured by Rutherford back scattering spectrometry. For all of the films, the RBS results reveal a ratio of 1:0.9-0.95 for the metallic elements (Tb:Sc, Gd:Sc, La:Sc). Film chemistry together with the silicon/high-κ interface was investigated using X-ray photoelectron spectroscopy. For as deposited samples, a silicate like interface is observed. After thermally treating the films in oxygen and forming gas ambient consecutively, the $TbScO_3$ keeps the inter-layer in silicate form, while for $LaScO_3$ a silicate-SiO_2 like interface is observed. Devices were prepared and electrically characterized. Due to process differences, in the conventional gate last MOSFETs a high series resistance has been observed which degrade the device performance. Despite this, well behaved output and transfer curves with high output current and I_{on}/I_{off} ratios up to 10^9 with a steep subthreshold slope could be observed. The mobilities of the devices extracted either by split CV or $I_d/\sqrt{(g\_m)}$ technique are about 147-185 cm^2/Vsec for SOI and around 350-400 cm^2/Vsec for sSOI devices. [1] J. Robertson, J. Appl. Phys. 104, 124111 (2008). [2] E. Durgun Özben, J.M.J. Lopes, M. Roeckerath, St. Lenk, B. Holländer, Y. Jia, D.G. Schlom, J. Schubert, S. Mantl, Appl. Phys. Lett. 93, 052902 (2008).

11:40 AM

A5, Late News

Session B: Non-Destructive Characterization

Wednesday AM — Room: 126
June 23, 2010 — Location: University of Notre Dame

Session Chairs: Kurt Eyink, Wright-Patterson AFB; Gregory Triplett, University of Missouri-Columbia

10:00 AM

B1, Innovative Time-Resolved Optical Characterization Techniques for Monitoring of Carrier Dynamics in Wide Band Gap Semiconductors: *Kestutis Jarasiunas*[1]; Tadas Malinauskas[1]; Ramunas Aleksiejunas[1]; Arunas Kadys[1]; Saulius Nargelas[1]; Vytautas Gudelis[1]; [1]Vilnius University

The given report presents innovative nonlinear optical techniques and demonstrate their metrological potential for *ex-situ* monitoring of nonequilibrium carrier dynamics in wide band gap materials and for determination of electronic parameters. We took advantage of laser-induced transient and spatial modulation of the optical properties of a semiconductor using its excitation by a short pulse of light-interference field and recording a transient diffraction grating. Development of transient grating (TG) techniques required to combine interdisciplinary knowledge in nonlinear optics, dynamic holography, semiconductor physics and technology. This novel methodological approach provided much deeper insight into materials properties due to specificity of nonequilibrium processes at isothermal relaxation stage: in contrast to linear optical properties at equilibrium state, the *nonlinear* optical spectroscopy of photoexcited semiconductors opened access to a variety of *nonequilibrium* processes. Consequently, the innovative time-resolved metrology via optical monitoring of spatial and temporal carrier dynamics provided direct and quantitative information about electronic parameters, which directly revealed materials quality and allow to predict a device performance. Experimentally, different TG schemes have been utilized to disclose various mechanisms of optical nonlinearities in pico- and nanosecond time domains. These schemes represent three cases of recording/reading the dynamic holograms - thin diffraction gratings (1), Bragg gratings (2), and transient reflection gratings (3). Combining these schemes with the mechanisms for modulation of the optical and electrical properties enabled investigation of free-carrier (and electron spin) dynamics via free-carrier (or exciton) nonlinearity (1), free carrier and space-charge filed dynamics via photorefractive nonlinearity (2), and selectively study a recovery of optically recharged deep traps in presence of other recombination channels via gratings in deep traps (3). The developed algorithms were used to extract from the diffracted optical signal the important electronic parameters, which directly revealed materials quality, namely, the nonequilibrium carrier lifetime, bipolar and/or monopolar diffusion coefficients, carrier diffusion length, recombination rate at a surface, in the bulk, or at interface, threshold of stimulated recombination, type of carriers photoexcited from deep traps, rate of recovery of recharged traps. We demonstrate the *metrological capabilities* of TG techniques by investigating carrier dynamics in various wide bandgap materials: III-nitride heterostructures grown on different substrates (sapphire, Si, SiC), InGaN alloys with varying In content, quasi-bulk GaN, In-rich and InN layers, cubic and hexagonal SiC polytypes, heavily doped III-V layers, and synthetic diamonds. Time-resolved TG technique was found more advantageous than the time-resolved photoluminescence, as it allowed to clarify the origin of fast

photoluminescence transients in thick GaN layers as carrier in-depth diffusion. Moreover, picosecond TG enabled direct determination of carrier lifetime and diffusion length in a wide range of threading dislocation density in GaN layers, to separate contributions of radiative and nonradiative recombination channels for analysis of a quantum efficiency droop problem.

10:20 AM

B2, Raman Characterization Methodologies Suitable for Determining Graphene Thickness and Uniformity: *David Tomich*[1]; John Hoelscher[1]; Jeongho Park[1]; Bruce Claflin[1]; Kurt Eyink[1]; William Mitchel[1]; [1]USAF/AFRL

Graphene has seen an exponential increase in interest since it was isolated by Geim et al. in 2004 via mechanical exfoliation. A brief survey of the current literature will find numerous groups using everything from mechanical exfoliation of graphite, to silicon sublimation of SiC, to chemical vapor deposition on metal crystals to produce single to few layer graphene. The attraction to graphene is due largely to its unconventional band structure which is a promising pathway towards nanoscale carbon electronics. Raman spectroscopy is a powerful non-destructive probe that has been used extensively over the past few decades to study carbon based materials, so applying confocal Raman spectroscopy to graphene is a natural extension. Several analysis methods have been used to determine the quality of graphene films and to determine the number of graphene layers present in these films. We have examined several of these methodologies and applied them to determine the uniformity of a graphene layer grown on a 2-inch 4H-SiC wafer by Si sublimation.We have examined Raman spectra from a series of 1 µm diameter spots evenly spaced across the sample and determined peak positions, peak heights, FWHM and integrated peak intensities for the D, G and 2D graphene bands after subtracting the SiC bands. These data were analyzed by looking at the G to 2D band integrated intensity ratio, SiC signal attenuation, 2D band full width at half maximum of a single Lorentzian and 2D multiple peak fitting to determine the layer thickness at each location. While most of these analyses appear to be adequate to determine cross-wafer uniformity, there is little agreement between these approaches on the number of layers present. We will discuss the different analysis methods and their relative accuracies and sources of error in relation to our data.

10:40 AM Student

B3, Characterizing the RF Properties of Semiconductors under Optical Illumination: *Youssef Tawk*[1]; Alex Albrecht[2]; Sameer Hemmady[1]; Ganesh Balakrishnan[2]; Christos Christodoulou[1]; [1]University of New Mexico; [2]Center for High Technology Materials

The ability to alter the Radio Frequency (RF) conductivity of semiconductor materials by exposing them to light of suitable wavelength is opening up several exciting possibilities in the field of reconfigurable microwave systems. For instance, such materials can be used as optically-activated switches to dynamically alter the RF behavior of microwave circuit components and antennas in a rapid and controlled fashion, thereby paving the way for reconfigurable systems such as Cognitive Radios. Characterizing the change in the RF properties of such materials (RF conductivity, loss tangent, dielectric constant, etc.) as a function of the incident light-intensity is thus critical to the proper design and engineering of such reconfigurable systems.In this talk, we present a solid-state model that predicts the change in the RF properties of semiconductor materials as a function of incident light intensity from a suitably energetic laser. We then apply this model to a piece of silicon (smaller than a wavelength at the microwave frequencies of interest) and predict the change its dielectric constant, RF conductivity and dielectric losses as a function of the laser power. This model is then experimentally validated by performing microwave measurements on a stripline circuit incorporating a silicon bridge and compared with numerical electromagnetic simulations. Finally, we show the applicability of this model to reconfigurable systems, by demonstrating the performance of a reconfigurable antenna whose RF properties are controlled by the ON/OFF state of optically activated silicon switches. Good agreement between the measured RF response of the antenna and numerical simulations validate that the solid-state model accurately describes the behavior of the semiconductor material under varying intensities of light illumination.

11:00 AM Student

B4, Admittance Spectroscopy of GaSb(100) and ALD/PEALD Al_2O_3 Dielectric Interface with Various Surface Treatments: *Ashkar Ali*[1]; Himanshu Madan[1]; Mantu Hudait[1]; Dalong Zhao[1]; Devon Mourey[1]; Thomas Jackson[1]; Suman Datta[1]; [1]The Pennsylvania State University

Antimonide based compound semiconductors have gained considerable interest in recent years due to their superior electron and hole transport properties. Schottky gated quantum well transistor architectures using InSb [1, 2] and $In_xGa_{1-x}Sb$ [3] have been demonstrated with excellent electron and hole mobility. Complementary n-MOS and p-MOS quantum well FETs (MOS-HEMTS) integrating a high quality dielectric is needed to demonstrate a scalable device architecture for 15 nm logic technology node and beyond. It is hypothesized that an ultra-thin GaSb surface layer is more favorable toward high-k integration than $In_{0.2}Al_{0.8}Sb$ barrier as it avoids Al at the interface and the associated surface oxidation. Here, we study the effects of various surface passivation approaches on the capacitance-voltage characteristics of Te-doped n-GaSb(100) MOS capacitors made with ALD and Plasma Enhanced ALD (PEALD) Al_2O_3 dielectric. PEALD was employed to reduce the thermal budget of dielectric deposition, particularly important for antimonide semiconductors. The control sample without surface preparation showed a pinned Fermi level. From the admittance spectroscopy analysis, we conclude that the ALD samples show weak Fermi level pinning along with very fast interface trap response. The PEALD samples show well modulation of the Fermi level along with weak inversion. It is believed that the absence of water precursor in PEALD process, coupled with low thermal budget, leads to a better quality interface. In summary, we have demonstrated GaSb MOS capacitors with unpinned Fermi level at the oxide semiconductor interface using PEALD Al_2O_3. XPS measurements are under progress to investigate the residual chemical species at the interface after the various surface preparation techniques.

11:20 AM Student

B5, High Temperature Coefficient of Resistance Sputtered A-Ge for Uncooled Microbolometer Applications: *Hang-Beum Shin*[1]; Myung-Yoon Lee[1]; David John[1]; Nikolas Podraza[1]; Thomas Jackson[1]; [1]The Penn State University

Hydrogenated amorphous silicon, amorphous germanium, and their alloys are of interest for uncooled infrared sensing microbolometer devices. In these applications, the properties of interest include controllable resistivity, high temperature coefficient of resistance TCR values, and low 1/f noise. Amorphous silicon (a-Si) and germanium (a-Ge) films exhibit relatively high TCR, may be deposited as uniform layers, and are prepared using more mature deposition processes than the other commonly used material in these types of devices, vanadium oxide. Recently, plasma enhanced chemical vapor deposited boron doped amorphous silicon germanium ($a\text{-}Si_{1-x}Ge_x$:H:B) and magnetron sputtered silicon germanium oxide ($SiGe_xO_y$) films have been reported with relatively high TCR values of -2.7 %/K and -4.86 %/K for films with resistivities of 100 Ocm and 245 Ocm, respectively [1,2]. Optimization of the $a\text{-}Si_{1-x}Ge_x$:H system for use in devices requires a better understanding of the relationship between TCR and 1/f noise in films with resistivity relevant to the current demands of the read out circuitry. To assess how variations in composition and structure affect these electrical characteristics, a-Ge films have been deposited using DC magnetron sputtering in mixed atmospheres of argon, hydrogen and nitrogen. After sputtering, titanium top electrodes are prepared in a transfer length method (TLM) pattern for measurement of resistivity and TCR, while resistors with three different volumes are made for volume normalization of the 1/f noise measurement. The TCR is typically measured from room temperature to 55C. Spectroscopic ellipsometry over a range from 1.2 to 3.35 eV is used to extract the a-Ge film thickness and approximate the band gap obtained by fitting the complex dielectric function spectra using a Tauc-Lorentz oscillator [3]. The TCR and equivalent activation energy can be thought of as a function of the tail states in the band structure, so that different slopes of the tail state densities influence how many carriers proportionally occupy these localized states with respect to the extended states in the conduction or valence band as temperature increases. Nitrogen dopant in germanium has been reported to have an activation energy of 0.23 eV by photoluminescence measurements with a corresponding TCR of

-3.1 %/K [4,5], which are in agreement with our TCR measurements. Thus, it is desirable to draw correlations between the deposition conditions and the 1/f and TCR characteristics in terms of the tail states. In this work, a-Ge films have been prepared under variable deposition temperatures, sputtering atmospheres containing hydrogen and nitrogen, and with boron co-sputtering to assess how variations in the electrical properties (resistivity, TCR, 1/f noise) correlate to film composition and microstructure.

11:40 AM Student

B6, Temperature Dependence of the Lattice Constant of Popular III-Sb Binary and Quarternary Alloys: *Magnus Breivik*[1]; Tron Arne Nilsen[1]; Saroj Kumar Patra[1]; Geir Myrvågnes[1]; Espen Selvig[2]; Bjørn-Ove Fimland[1]; [1]Norwegian University of Science and Technology (NTNU); [2]Norwegian Defence Research Establishment (FFI)

III-Sb alloys are of great interest for mid-infrared (2-5 µm) optoelectronics. For epitaxial growth of structures based on these materials, it is important to have accurate values of the lattice constants both at room temperature and at the growth temperature, due to thermal misfit. This is particularly important when thick layers with minimal dislocation density are needed, such as AlGaAsSb cladding layers in mid-infrared laser structures. Using X-ray diffraction (XRD), the lattice constants of GaSb [1], Al0.90Ga0.10AsySb1-y [2], and AlSb (preliminary) have been measured up to 550°C, as literature data on the lattice constant for these materials are either differing or lacking at higher temperatures. The lattice constants of unstrained AlGaAsSb and AlSb were obtained using asymmetric XRD measurements [3] of strained epilayers grown on either GaSb(001) or GaAs(001) substrates in a Varian Gen II Modular molecular beam epitaxy (MBE) system. The technique allows determination of the in-plane and out-of-plane lattice constants, from which the lattice constant of unstrained material was calculated. For GaSb, measurements were performed on epiready GaSb(001) wafers. The following polynomial functions for the temperature dependent lattice constants were deduced from our measurements: a_AlSb = 6.1350 + 3.20E-5*T a_GaSb = 6.0959 + 3.37E-5*T + 5.63E-8*T^2 - 1.29E-10*T^3 + 1.05E-13*T^4 a_AlGaAsSb = 6.1310 -0.4702*y + 2.856E-5*T + 5.03E-9*T^2 (0.003<y<0.065)All lattice constants are given in Å, and all temperatures are in °C. The polynomial functions are valid from room temperature up to approximately 550°C. Our data suggest that some of the literature values need revision, in particular for AlSb.

Session C: Nanoscale Characterization

Wednesday AM
June 23, 2010

Room: 129
Location: University of Notre Dame

Session Chairs: John Schlager, NIST; Lincoln Lauhon, Northwestern

10:00 AM Student

C1, Pulsed-Laser Atom Probe Tomographic Analysis of Ge-Ge/Co/Mn Thin-Film Superlattices: *James Riley*[1]; Daniel Perea[2]; Lincoln Lauhon[1]; Frank Tsui[3]; [1]Northwestern University; [2]Los Alamos National Laboratory; [3]University of North Carolina

Magnetic semiconductors can provide the basis for spintronic devices that utilize electron spin to store and transmit information. Dilute magnetic semiconductors are made by doping semiconductors with paramagnetic impurities, such as Mn, which may become ferromagnetically ordered through interactions with itinerant carriers. Magnetic dopants typically have a low solubility in the semiconductor host, making the alloys unstable with respect to the formation of small clusters and phase segregation. As clusters as small as dimers can be ferromagnetic, it is important to characterize the material inhomogeneity on the smallest length-scales and with the highest possible sensitivity. Pulsed-laser atom probe tomography (PLAP) can be used to examine variations in the composition of a material with sub-nanometer spatial resolution and single atom sensitivity, making it a uniquely powerful tool. It compliments transmission electron microscopy (TEM) based techniques, which provide excellent spatial resolution but are less sensitive to composition, and secondary ion mass spectroscopy (SIMS), which provides single atom sensitivity but has relatively poor spatial resolution. We have used PLAP to analyze a superlattice structure consisting of alternating layers of intrinsic Ge and Ge co-doped with Co and Mn. The Ge-Ge1-x-yCoyMnx superlattice thin film was grown by the Tsui group by molecular beam epitaxy (MBE). A section of the thin film was prepared for PLAP analysis by a lift-out and milling process using a focused ion beam (FIB) to create a needle-shaped specimen with a tip diameter less than 100 nm. The specimen was analyzed using PLAP with a 523 nm laser with a pulse energy of 0.6 nJ, a pulse frequency of 100 kHz, and an evaporation rate of 0.2% at a temperature of 80 K. Approximately 4.5 million atoms were collected. Analysis of the 3-D reconstruction revealed Co and Mn rich clusters within the co-doped layers. Within an isolated co-doped layer, we determined the composition of Co and Mn within the 'clusters' to be 12% and 6%, respectively, which is nearly a factor of two higher than the average concentration within the entire layer. Further, a 1-D concentration profile taken along the PLAP analysis direction and parallel to the growth direction indicated enhanced Co and Mn concentrations at the interfaces between the intrinsic Ge and co-doped Ge layers. Co-Mn dimers are expected to inhibit Mn diffusion and stabilize the films against secondary phase formation. Radial distribution function (RDF) analysis was therefore performed on the PLAP data and compared with RDFs generated from a random alloy. The RDF analysis confirmed that the Co distribution influenced the Mn distribution, but the resolution was not sufficient to detect the Co-Mn dimers.

10:20 AM Student

C2, Atomic Scale Gate Electrode Formed by a Charged Defect on GaAs(110): *Donghun Lee*[1]; Jay Gupta[1]; [1]Ohio State University

Electric-field control of spin-spin interactions at the atomic level is desirable for spintronics and spin-based quantum computation. Here we demonstrate the realization of an atomic-scale gate electrode formed by a single charged vacancy on the GaAs(110) surface[1]. A low temperature scanning tunneling microscope is used to position these vacancies with atomic precision. Tunneling spectroscopy suggests that the vacancies influence the in-gap resonance of Mn, Co and Zn acceptors via an interplay of band bending and Coulomb electrostatics. We find that this electrostatic field can be used to tune the magnetic coupling between pairs of Mn acceptors. This suggests an avenue for controlling spin-spin interactions on the atomic scale. [1] D. Lee and J.A. Gupta (in preparation).

10:40 AM

C3, Ordered Assemblies of Bimetallic Nanostructure Arrays Utilizing a Self-Assembled Disilicide Nanowire Template: *Talin Ayvazian*[1]; Aniketa Shinde[1]; Regina Ragan[1]; [1]University of California-Irvine

Metal nanostructures have demonstrated extraordinary properties: the capacity for single molecule detection in plasmon resonance biosensors, chemical sensitivity and higher performance in catalytic processes than their bulk counterparts. One of the most significant challenges is the fabrication of nanostructure arrays with monodisperse size, shape and high density using low cost and high throughput technique. We will present a unique template-based fabrication process for dense ordered arrays (~1E11 cm^-2) of bimetallic core-shell nanostructures with monodisperse size and shape, over large area (>1mm^2), and having feature size and inter-particle spacing unattainable with electron beam lithography. A combination of scanning probe microscopy and density functional theory is used to understand the fabrication of these one dimensional structures. Noble metal deposited via physical vapor deposition on a nanowire template combined with reactive ion etching produce noble metal core-shell nanowire and nanoparticle arrays with mean feature size of approximately 8 nm. Rare earth disilicide nanostructures are used as self-assembled templates on Si(001). Scanning tunneling microscopy has shown that noble metal forms clusters on RESi2 nanowire surfaces, and scanning electron microscopy backscattered images has shown that noble metal preferentially aggregates on the nanowire surfaces as opposed to the Si substrate. Noble metal coverage is used to select nanoparticle versus nanowire arrays after reactive ion etching. Experimental variables such as annealing time and temperature are explored to optimize selective aggregation of noble metal on nanowire surfaces.

The work functions of these structures can be tuned by varying size and shape of the disilicide template, as demonstrated by Kelvin Probe force microscopy. Au and Pt core-shell structures show work functions within the range of 3.7 – 4.0 eV, less than respective bulk work functions. Using the Vienna ab initio Simulation Package, theoretical modeling is combined with scanning probe microscopy for deeper insight of thermodynamics and kinetics driving template formation. We provide a platform to answer challenging issues regarding nucleation, nanowire-substrate interface, and morphology of RESi2-x nanowires on Si(001). Synergistic STM characterization and ab initio calculations reveal that the stable adsorption geometries of the wetting layer lead to nanowire orientation perpendicular to Si dimer rows and thereby in unidirectional nanowire arrays on vicinal Si(001) surfaces. Formation energy calculations for narrow YSi2 nanowires provide insight into the mechanisms that stabilize nanowire structures, such as internal strain relaxation and nanowire surface reconstruction. These studies will lead to achieving more control over the template assembly to further optimize the fabrication of bimetallic core-shell nanostructures.

11:00 AM Student
C4, Scanned Probe Characterization of Self-Assembled ErAs/GaAs Semimetal/Semiconductor Nanostructures Grown by Molecular-Beam Epitaxy: *Keun Woo Park*[1]; Adam Crook[1]; Hari Nair[1]; Seth Bank[1]; Edward Yu[1]; [1]University of Texas at Austin

Rare-earth monopnictide semimetallic nanoparticles embedded epitaxially in III-V compound semiconductors are of outstanding interest for application in a variety of solid-state devices including multijunction tandem solar cells, thermoelectric devices, and terahertz radiation sources. In the case of multijunction tandem solar cells, the semimetallic nanoparticles have been shown to yield dramatic increases in the electrical conductivity of tunnel junctions located between individual pn junction diodes in the tandem cell stack, with this improvement postulated to occur as a consequence of a two-step, rather than a single-step, electron tunneling process enabled by the electronic states in the nanoparticles. However, verification of this hypothesis and further optimization for solar cell and other applications will require an improved understanding of the spatial distribution of, electronic structure within, and electrical current transport through and in the vicinity of the nanoparticles and nanoparticle-semiconductor interfaces. We have used atomic force, scanning capacitance, and conductive atomic force microscopy to characterize nanoscale charge distributions and current transport in ErAs nanoparticle/GaAs heterostructures grown by molecular-beam epitaxy. Sample structures consisted of n-GaAs (001) substrates on which were deposited 200nm n+ GaAs ($n \sim 5\times10^{18}cm^{-3}$), an ErAs nanoparticle layer, and a 5-15nm p+-GaAs cap layer ($p \sim 5\times10^{19}cm^{-3}$). Scanned probe microscopy studies were performed at room temperature in ambient atmosphere using a Veeco Dimension 3100 Nanoscope IIIa microscope system. Scanning capacitance images obtained with dc sample bias voltages ranging from -1.0V to +2.0V reveal marked lateral variations in local carrier accumulation behavior in the sample, at typical lateral length scales of ~20-100nm. On the basis of analytical and numerical modeling, areas for which substantial modulation of near-surface electron and hole concentrations occurs are taken to correspond to regions below which no ErAs is present. Those areas for which little near-surface carrier modulation is observed are taken to correspond to regions above ErAs nanoparticles; in these areas, the capacitance signal over a broad range of bias voltages is dominated by carrier modulation within the nanoparticles rather than in the surrounding semiconductor material, leading to a weak dependence of capacitance on dc bias voltage and suppressed scanning capacitance signal contrast. The projected coverage of the GaAs interface region by ErAs nanoparticles implied by this interpretation is in good agreement with that expected from epitaxial growth conditions. Conductive atomic force microscopy measurements performed on these structures suggest that areas for which ErAs nanoparticles are present below the surface are generally, but not universally, associated with substantially increased electrical conductivity, consistent with the improvement in tunnel junction conductivity observed in electrical device measurements. These studies provide a foundation for detailed analysis of electronic structure and current transport behavior associated with ErAs nanoparticles embedded epitaxially in GaAs, and for understanding and optimizing their consequences for device behavior.

11:20 AM
C5, Late News

11:40 AM
C6, Late News

Session D: Narrow Bandgap Semiconductor Bulk Materials and Devices

Wednesday AM
June 23, 2010

Room: 131
Location: University of Notre Dame

Session Chairs: Partha Dutta, Rensselaer Polytechnic Institute; Shekhar Guha, Wright Patterson Air Force Base

10:00 AM Invited
D1, Review of Narrow Bandgap Semiconductor Based THz-Emitters: *Ingrid Wilke*[1]; Suranjana Sengupta[1]; [1]Rensselaer Polytechnic Institute

An important method to generate THz-radiation pulses is the excitation of semiconductors by femtosecond (fs) near-infrared (nir) laser pulses. The interest in THz-waves, which are located between microwaves and the infrared in the electromagnetic spectrum, is rapidly growing. This development is driven by the availability of novel electronic and optical THz-radiation sources and THz-detectors, the exploration and exploitation of materials properties in the THz-frequency range and the success of real-world THz-system applications such as THz-imaging and THz-sensing. Narrow bandgap semiconductors are great sources of THz-radiation for more compact and lightweight time-domain THz-systems operated by fs lasers lasing at wavelengths between 1.0-1.6 microns. In order to optimize THz-emission from narrow bandgap semiconductors it is important to understand the THz-emission process as determined by semiconductor properties. For this purpose we have investigated THz-emission from GaSb, GaxIn1-xSb and GaxIn1-xAs for a wide range of compositions and range of electronic properties. The III-V ternary alloy semiconductor GaxIn1-xAs is a very interesting terahertz materials system because its bandgap can be tuned from 0.36–1.42eV by variation in the Ga mole fraction from x=0 to 1. The growth of binary and particularly ternary III-V semiconductors crystals is challenging since precise control of heat and mass transport in the high temperature melt during the crystal growth is necessary for obtaining high quality application worthy material. For our experiments, a hybrid vertical Bridgman and gradient freezing directional solidification process was employed for the growth of high quality GaSb, GaxIn1-xSb and GaxIn1-xAs crystals.We review our experiments on THz-emission from narrow bandgap semiconductors excited by fs nir laser pulses. The Ga1-xInxSb material system enables the study of the influence of carrier concentrations on the THz-emission process in narrow bandgap semiconductors. The study demonstrates the existence of a compromise between the positive effect of high electron temperature provided by narrow bandgap materials and the negative effect of high intrinsic carrier concentrations. The influence of the majority and minority carrier types and concentrations on THz-emission strength was investigated using GaSb:Te. By varying the majority and minority carrier type and carrier concentrations over three orders of magnitude the THz-emission mechanism in GaSb can be tuned from being dominated by the photo-Dember effect to being dominated by surface-field acceleration. Within each regime photo-Dember based THz-emission and surface-field acceleration based THz-emission are maximized under specific majority and minority carrier concentrations. Furthermore, we have investigated the relationship between electrical and structural properties of GaxIn1-xAs and THz-radiation emission. We demonstrate that primarily optical rectification and surface-field acceleration contribute to THz-emission from GaxIn1-xAs depending on the Ga mole fraction x. A semi-large aperture Ga0.69In0.31As:Fe THz antenna emitter has superior performance compared to conventional THz-emitters because of femtosecond carrier lifetimes, ultrafast mobilities and high electrical resistivity.

10:20 AM Student

D2, Electrical and Optical Studies of Melt Grown Optical Grade $InAs_{1-y}P_y$: *Jean Wei*[1]; Yung Kee Yeo[2]; Jacob Barnes[1]; Leo Gonzalez[3]; Shekhar Guha[3]; Robert Hengehold[2]; Geeta Rajagopalan[4]; [1]General Dynamics IT; [2]Air Force Institute of Technology; [3]Air Force Research Laboratory; [4]United Semiconductors LLC

Bulk grown ternary III-V semiconductors are promising candidates for optoelectronic and photonic applications. These applications require materials free from extended defects such as inclusions, precipitates and cracks that scatter light during its propagation through the bulk of sample. Growth of optical grade bulk crystals requires stringent control over the synthesis and growth conditions in order to avoid the optical defects. Bulk ternary $InAs_{1-y}P_y$ poly-crystals with diameter up to 50 mm were grown from pseudo-binary InP-InAs melt using the vertical Bridgman technique. The electrical and optical properties of these $InAs_{1-y}P_y$ (y = 0 to 0.7) were investigated as a function of alloy composition and sample temperature. Data from Hall effect, photoluminescence (PL), refractive-index, and optical transmission measurements as a function of composition and temperature will be presented along with the role of growth conditions on the optical transparency. As-grown undoped crystals have been found to exhibit n-type conductivity irrespective of the alloy composition. Though the bulk $InAs_{1-y}P_y$ substrates show high optical transmission up to long wavelengths as well as high carrier mobility, they exhibit random micro-scale compositional fluctuations across the substrate area. Future advancements in crystal growth are necessary to achieve spatially homogeneous alloy compositions to avoid the random light scattering regions.

10:40 AM Student

D3, Electrical and Optical Properties of Bulk Ternary $In_xGa_{1-x}As$: Jean Wei[1]; *Austin Berstrom*[2]; Yung Kee Yeo[2]; Shekhar Guha[3]; Leo Gonzalez[3]; Robert Hengehold[2]; Geeta Rajagopalan[4]; [1]General Dynamics IT; [2]Air Force Institute of Technology; [3]Air Force Research Laboratory; [4]United Semiconductors LLC

Advances in crystal growth techniques have allowed successful growth of good optical grade melt-grown bulk ternary $In_xGa_{1-x}As$ crystals using the vertical Bridgman technique. These crystals are promising candidates for electro-optical and photonic applications at long wavelength ranges beyond the capability of today's epilayer semiconductor devices. In order to fully utilize these ternary alloys, the electrical and optical properties of the recent melt-grown bulk $In_xGa_{1-x}As$ (x = 0.75 to 1) have been investigated as a function of temperature and indium mole fraction x through photoluminescence, Hall effect, and absorption spectroscopy measurements. Hall effect measurements revealed moderate n-type doping with carrier concentrations ranging from 1.5 to 9.6×10^{16} cm^{-3} at 10 to 15 K. Hall mobility increased with rising indium content, and mobility values at 15 K ranged from 1.5×10^4 $cm^2/V\cdot s$ for $In_{0.75}Ga_{0.25}As$ to 3.5×10^4 $cm^2/V\cdot s$ for InAs. Laser excitation power dependent PL measurements at 12 K and temperature dependent PL measurements at temperatures ranging from 12 to 140 K showed band-to-band, free-to-bound, and donor-acceptor pair transitions.

11:00 AM Student

D4, Optical and Thermal Properties of III-V Bulk Ternary $In_xGa_{1-x}Sb$ and $In_xGa_{1-x}As$ Crystals: Jean Wei[1]; *Shekhar Guha*[2]; Leo Gonzalez[2]; Jacob Barnes[1]; Yung Kee Yeo[3]; Geeta Rajagopalan[4]; [1]General Dynamics IT; [2]Air Force Research Laboratory; [3]Air Force Institute of Technology; [4]United Semiconductors LLC

$In_xGa_{1-x}Sb$ and $In_xGa_{1-x}As$ are ternary semiconductor materials widely used in optical fiber communication, lasers, optical switches, and infrared optical detectors. Because of the crystal lattice constant mismatch, it has been difficult to grow uncracked thick $In_xGa_{1-x}Sb$ and $In_xGa_{1-x}As$ layers on binary compounds. Therefore, previous studies were focused on thin film $In_xGa_{1-x}Sb$ and $In_xGa_{1-x}As$ epitaxial layers, and thus most optical parameters of bulk $In_xGa_{1-x}As$ and $In_xGa_{1-x}Sb$ crystals are unknown. Recent advances in crystal growth techniques have allowed successful growth of good melt-grown bulk ternary $In_xGa_{1-x}Sb$ and $In_xGa_{1-x}As$ crystals using the vertical Bridgman technique. In this work, optical properties of $In_xGa_{1-x}Sb$ and $In_xGa_{1-x}As$ bulk crystals have been investigated using Michelson and Fabry-Perot interferometers and Fourier transform infrared spectroscopy. The refractive index value, n, the thermo-optical coefficient, dn/dT, and absorption coefficient were measured as a function of wavelength, temperature, and indium mole fraction x, all of which are very important parameters in optoelectronic device applications.

11:20 AM
D5, Late News

11:40 AM
D6, Late News

Session E: Materials Integration: Wafer Bonding

Wednesday AM
June 23, 2010

Room: 138
Location: University of Notre Dame

Session Chairs: Cindy Colinge, Tyndall National Institute; Mark Goorsky, University of California, Los Angeles

10:00 AM Student

E1, Investigation of Physisorbed and Chemisorbed Sulfur Species for GaAs Wafer Bonding: *Michael Jackson*[1]; Mark Goorsky[1]; [1]UCLA Materials Science and Engineering

This study demonstrates that a vacuum passivation method that exposing III-V surfaces to sulfur vapor under UV illumination can be utilized for direct bonding and is useful to study the role of sulfur at the interface. The treatment of III-V surfaces with sulfide-containing solutions is known to improve the surface electronic properties for Schottky contacts and passivation of heterojunction bipolar transistors, due to replacement of surface oxide with a sulfur-containing layer. Various sulfide solution passivation methods have been reported for direct bonding including thiourea in NH_4OH, $(NH_4)_2S$ in aqueous and alcohol solutions, with the latter treatment shown to improve the conductivity of bonded p-GaAs/n-InP. The potential of using vacuum based sulfur passivation for wafer bonding have not been explored, so this study investigates the optimization to be performed to ensure smooth bondable surfaces are maintained. Evaporation of sulfur onto the GaAs surface is not self-limiting; thus the deposited layer contains a mixture of chemisorbed and physisorbed sulfur species. This physisorbed sulfur does not facilitate good adhesion between bonded wafers, causing bond failure and surface roughening during heat treatments at temperatures up to 400°C. This physisorbed sulfur is not readily removed using common solvents. therefore, a desorption process was employed to increase the ratio of chemisorbed sulfide to physisorbed sulfur. The wafers are annealed in vacuum to remove the physisorbed sulfur, which has a vapor pressure of 10^{-4} Torr between 60-80°C. Through monitoring the surface quality by AFM and subsequent bonding, a 5 minute dose of UV-sulfur at 60°C under 10^{-6} Torr vacuum, followed by a 5 minute vacuum desorption at 75°C removes the physisorbed sulfur to maintain a clean surface suitable for direct bonding. The chemisorbed sulfur remains after this step, as XPS taken at surface sensitive grazing angle confirms the presence of As-S (the presence of Ga-S cannot be as conclusively determined due to the small binding energy differences for $2p_{3/2}$ Ga-O, Ga-S, and Ga-As). XPS also shows that sulfur treated surfaces have a reduced As-O and Ga-O signal compared to surfaces etched in NH4OH, which is essential for wafer bonding where high electrical conductivity is desired. Wafer bonding of the UV-S and S desorbed samples show excellent adhesion for GaAs/GaAs and InP/InP bonded pairs that result in bulk fracture strength after annealing at 400°C and 300°C respectively, with minimal compressive forces. It has been shown that sulfur may play a key role in facilitating III-V wafer bonding with mechanically strong interfaces with minimal oxide incorporation, and further study into the reaction and desorption of sulfur on III-V surface will aid in developing a low-cost efficient procedure for materials integration without high processing temperatures or large compressive forces.

10:20 AM Student

E2, AlGaAs/GaAs/GaN Wafer Fused HBTs with Ar Implanted Extrinsic Collectors: *Zongyang Hu*[1]; Chuanxin Lian[1]; Zhen Chen[2]; Yu-Chia Chang[2]; Huili(Grace) Xing[1]; [1]University of Notre Dame; [2]University of California, Santa Barbara

Heterojunction bipolar transistors based on AlGaAs/GaAs/GaN structures are promising for high frequency and high power applications thanks to the high

breakdown field in GaN collector and the low contact resistances to both n- and p-GaAs. Due to the large lattice mismatch between GaAs and GaN, we have explored these heterostructures using wafer bonding instead of epitaxial growth. Previously we reported the wafer fused HBTs with DC current gains as high as 20 and breakdown voltages of ~ 35V. We have also fabricated RF HBTs exhibiting a small signal cutoff frequency fT ~ 2.6 GHz. Our experiments showed that one of the challenges to increase the speed of the wafer-fused HBT was to make ohmic contacts to a thinner GaAs base without shorting to the GaN collector. To this end, we have investigated insulating extrinsic collectors by using Ar ion implantation. Ar ion implantation was first performed in the extrinsic collector region on the GaN wafer, following an alignment marker etch into GaN. The inverted emitter/base AlGaAs/GaAs wafer and the GaN collector wafer were then brought together, followed by a thermal annealing at 550°C for 1 hr. The ion implanted region on GaN remained to be insulating after this high temperature annealing. We found that the annealing temperature had to be increased from 450°C to 550°C to ensure a high bonding yield (> 80 %) when employing the ion implanted extrinsic collector. A more careful examination revealed that a ridge (~ 0.5 nm high) formed between the ion-implanted region and the region protected by the mask, which we currently believe contributes to the necessary annealing temperature increase. To understand the effects of the ion-implantation, we first compared the p-GaAs/n-GaN base/collector diode and p-GaAs/implanted GaN/n-GaN base/insulator/collector structure. We found that the base/insulator/collector structure indeed showed much lower leakage current in both forward and reverse bias directions, as desired, as well as a more uniform breakdown voltage. HBTs with the Ar+ implanted extrinsic collector were demonstrated with a current gain of 2 - 3 and a breakdown voltage of ~ 55 V. These are very encouraging results. Future improvements in device performance are expected when the fabrication processes, especially the wafer surface cleaning, are further optimized.

10:40 AM Student

E3, Effect of Surface Activation for Ge-Si Integration Using Wafer Bonding: *Ki Yeol Byun*[1]; Isabelle Ferain[1]; Ran Yu[1]; Cindy Colinge[1]; [1]Tyndall National Institute

Germanium is a candidate to replace Si in the channel of future high performance p-channel metal-oxide semiconductor field effect transistors (MOSFET) device due to its better hole transport properties. Ge to Si direct wafer bonding methods have been studied for use in high-performance photo-detectors as well as high-quality epitaxial templates for GaAs growth. In this work, we propose an alternative method for the Ge-Si integration which has less defective interfaces with low thermal budget. Structural investigations show that successful low temperature Ge to Si wafer bonding can be achieved for heterogeneous integration. In the experiment, 4-inch ‹100› oriented p-type Ge (Ga doped, resistivity = 0.016 O.cm) were selected for bonding. Prior to bonding, the Ge and Si wafers were cleaned in an SC1-equivalent solution with ozone for Si and without ozone for Ge. Wafers were then loaded into AML AW04 aligner bonder and vacuum was applied. The wafers were then exposed for 10 minutes to either oxygen or nitrogen free radicals (chamber pressure was 1 mbar at 100 W) generated by a remote plasma ring. After exposure the wafers were bonded in-situ under a pressure of 1kN applied for 5 minutes at a chamber pressure of 10-5 mbar. The wafers were annealed in-situ at 100°C for 1 hour with an applied pressure of 500N in vacuum followed by an ex-situ anneal at 200°C for 24 hours in order to enhance bond strength. The same wafers were then annealed again at 300°C for 24 hours. The ramp-up rate was set to 0.5°C/min in both cases. After anneal Ge-Si bonded pairs remained intact due to a slow ramp-up rate. Structural analysis of buried interfaces was studied by SAM and HR-TEM. The formation of interface defects during low temperature anneal depends on the surface activation technique. Due to the remote plasma configuration, ions which escape the mesh ring do not strike the wafer surface at high velocity. The latter has been confirmed by AFM and HR-TEM analysis showing that there was no significant surface damage after radical exposure of bare Ge and Si wafers. Buried interfaces of bonded pairs were inspected using SAM after annealing at 200°C 24 hours. This low temperature process using surface activation is a way to achieve high quality interfaces without activation induced surface damage. Our structural analyses show that surface activated wafer bonding process is very suitable for Ge-Si integration with low thermal budget and low defect density at bonded interfaces. Additional experiments are being performed to characterize thoroughly the chemical properties at bonded interfaces.

11:00 AM Student

E4, Strain, Annealing, and Exfoliation in Hydrogen Implanted GaN for Layer Transfer Applications: *Eric Padilla*[1]; Anthony Pangan[1]; Michael Jackson[1]; Mark Goorsky[1]; [1]University of California, Los Angeles

Transfer of GaN layers to alternate substrates is limited by the very few efforts in this area which address how different annealing conditions impact both the implant-induced strain as well as successful exfoliation. Understanding implant-induced strain evolution has led to successful exfoliation and layer transfer in zincblende III-V and Group IV semiconductors. In this study, we modeled the strain in as-implanted GaN substrates, studied how two distinct strain related regions changed differently with annealing, and developed a series of two-step annealing processes to relate the exfoliation of GaN layers with the changes in the strain profiles. Successful GaN exfoliation of 1 µm thickness was achieved – this is significantly thicker than has been reported elsewhere. 18mm x 18mm GaN wafers were implanted with a dose ranging from $0.5x10^{17}$ H^+/cm^2 to $1.5x10^{17}$ H^+/cm^2. All implants were conducted at 77 K and 200 keV. Analysis and modeling of the strain distribution in as-implanted GaN via triple axis diffraction scans showed that two distinct strain peaks were present – one near the surface and the second at the projected range. Such a double peak was not observed in the implant of standard III-V or Group IV materials. After annealing at temperatures from 150°C to 375°C for extended times (1-40 hours), the shallow strain peak was observed to shift toward the substrate, indication a reduction in strain, whereas the strain in the peak from near the projected range decreased monotonically as the annealing temperatures increased to 300°C but showed a reversal, i.e., a reduction in the strain change such that annealing at 375°C resulted in no shift to the strain peak associated with the projected range strain. This result indicated that defects from the two regions interact at lower temperatures but not at the higher annealing temperatures and thus may produce different types of defect structures. These results were used to design a two stage annealing procedure in which hydrogen-related platelets nucleate at a lower temperature and subsequently grow and induce exfoliation after higher temperature annealing. Presented here are results from low temperature steps performed at either 150°C or 375°C for 20 hours followed by high temperature annealing (> 650°C). The 150°C first step combination produced a series of small (< 1 µm) blisters whereas the 375°C first step combination led to the production of several µm-sized exfoliated sections (with removal of 1 µm thick layers) as well as large (several µm) irregular-shaped blisters, indicating that the latter process is more suitable for layer transfer. Transmission electron microscopy, atomic force microscopy and Noamrski imaging were used in addition to the high resolution x-ray scattering and dynamical scattering models.

11:20 AM

E5, Optimization of Adhesive Wafer Bonding for Silicon: *Sue Holl*[1]; Srinivasulu Korrapati[1]; Cindy Colinge[2]; [1]CSUS; [2]Tyndall National Institute

Optimization of bonding parameters to develop a low temperature adhesive wafer bonding process producing a defect free and relatively strong bond in pairs of 6 inch silicon wafers was studied. SU-8 was used as the intermediate adhesive. The Key Process Input Variables of soft bake temperature, UV exposure dose and bonding temperature were studied. Three different values were chosen for each process variable and the bonding process was repeated in random order for all possible combinations of process variables. The soft bake temperature and time combinations tested were 70°C for 60 seconds, 90°C for 30 seconds and 95°C for 300 seconds. UV exposure times of 5, 10 and 15 seconds at 10 mW/cm2 were used to produce exposure energies of 50 mJ/cm2, 100 mJ/cm2and 150 mJ/cm2 respectively. Bonding temperatures of 90°C, 115°C and 140°C for 30 minutes were studied to optimize the curing process. The quality of the wafer bonds was determined by two Key Process Output Variables: the fraction of interfacial area in intimate contact, measured by void area, and the strength of the bond interaction, measured by fracture strength. Bond characterization, including bond interface imaging to detect defects and measure void area, and

tensile testing to calculate the fracture strength, was performed on all bonded pairs. The bonded wafers were scanned using a Sonoscan Scanning Acoustic Microscope (SAM) and C-Scan images were used to determine void area. The bonded wafers were diced into 5mm X 5mm test specimens and each was scanned using SAM to determine the bond area. Tensile testing was done on the diced test specimens from each bonded pair to calculate the fracture strength. A general linear statistical model was developed to perform analysis of variance to determine the impact of the process input variables on the process output variables. The bonding parameters soft bake temperature, UV exposure dose and bonding temperature were successfully optimized to develop an adhesive wafer bonding process for 6 inch silicon wafers that produces defect free, strong bonds using SU-8 as an intermediate adhesive layer. The optimum conditions are soft bake temperature of 90°C, UV exposure of 100 mJ/cm2 and bonding temperature of 115°C. This work was supported by the Science Foundation Ireland grant 07/IN/I937: Low Temperature Wafer Bonding for Heterogeneous Integration.

11:40 AM

E6, Development of Surface Activation Based Nano-Bonding and Interconnect System: *Matiar Howlader*[1]; Tadatomo Suga[2]; Akira Yamauchi[3]; [1]McMaster University; [2]The University of Tokyo; [3]Bondtech Co. Ltd.

A nano-bonding and interconnect system (NBIS) equipment has been developed for three dimensional integration of emerging electronic and biomedical systems at room temperature. This article reports the development of NBIS with some preliminary bonding results of semiconductors and metals. The NBIS accommodates specimens as big as 2-inch wafers. The NBIS consists of a load lock chamber and bonding chamber separated by a gate valve. The load lock chamber has six stage elevators to hold the specimens. An automated transfer rod is used to transfer the specimens from the load lock chamber to the bonding chamber. An ultra high vacuum (UHV) pressure of 10-7 Pa is maintained in the bonding chamber using a high efficient turbo molecular pump. The bonding chamber is equipped with a high precision alignment system and a bonding head. An electrostatic chuck is used to hold the top specimen. Two infrared (IR) cameras are equipped to detect the alignment marks of the substrate and chip. The piezo elements attached to the bonding head and the Z axis units attached to the piezo walking table are used to perform the parallel adjustment function of the top and bottom wafers. The top and bottom specimens are activated in the bonding chamber either by Argon (Ar) ion bombardments or Ar-fast atom beam (FAB). Two FAB sources are installed at 45 degree in the bonding chamber to activate the top and bottom wafers. A single Ar ion source installed in bonding chamber is used to activate the top and bottom specimens simultaneously. After the activation, the top and bottom specimens are finally aligned by using the bottom IR camera. The alignment includes automated parallel adjustment, position detection, and alignment systems. The piezo elements installed on the bonding head serve as actuators for the top parallel adjustment. The Z-axis units mounted on the piezo walking table serve as actuators for the bottom parallel adjustment. The parallelism of the top and bottom wafers is detected through the height displacement of parallelism detection points at three Z axis units by means of the lower IR camera and is automatically adjusted through the operation of the top and bottom actuators, respectively. An automated repetitive correction enables an alignment accuracy of less than 100 nm. After the alignment, the top wafer is brought down and contacted with bottom wafer. Preliminary bonding results of Si/Si, Si/Ge and Si/GaAs using NBIS show void free interface with bonding strength equivalent to bulk fracture strength of the wafers. Further research on three-dimensional integration for high-density interconnection will be presented. For this purpose, a number of 1 millions of 3 µm size Cu bumps over an area of 5x6 mm were bonded to achieve the daisy chain structure.

Session F: Silicon Carbide Devices

Wednesday AM
June 23, 2010

Room: 155
Location: University of Notre Dame

Session Chairs: Joshua Caldwell, Naval Research Lab; Michael Dudley, Suny-Stony Brook Univ

10:00 AM Invited

F1, Applications of SiC Power Devices – A Materials and Device Perspective: *Anant Agarwal*[1]; [1]Cree, Inc

The recent surge in the demand for SiC Power Schottky diodes in commercial applications suggests that a number of key material and device issues pertaining to the defects, design, production, cost, reliability and applications issues with respect to the diodes have been successfully addressed by the SiC community, at large. The relatively low voltage SiC diodes (600 to 1700 V) are currently being used in Switch Mode Power Supplies and Power Converters for Solar Cells. The next big mass-market for SiC diodes will be in the Hybrid and Plug-In Automotive segment, provided the benefits of using the SiC diodes out-weigh the cost of the diodes. In this respect, it is important to see the overall impact on the system cost rather than simply concentrating on the component cost. In this paper, we will present the cost/benefit analysis of above mentioned applications and try to identify the critical issues that may be addressed in future to improve the cost/benefit ratio in favor of using SiC diodes. For applications requiring higher voltage Schottky diodes and/or PiN diodes, the recombination-induced Stacking Faults and their effects on reverse leakage currents as well as forward conduction are important issues that need to be addressed. In addition, doping and uniformity of life-time are critical issues. Furthermore, there are significant device design challenges to optimize the design for high voltage applications such as designing for high dv/dt, avalanche and surge ratings. There are multiple well known issues with SiC power MOSFETs and IGBTs such as low inversion layer mobility, low threshold voltage and oxide reliability. While a significant research focus is being directed on these issues, many significant process integration issues, which impact the cost of the product such as high temperature ion-implantation and activation, need to be addressed. The cost/benefit analysis of MOSFETs and IGBTs for applications in Converters for Solar Cells, Hybrid and Plug-In Automotive segment and Smart Grids will be presented.

10:40 AM

F2, Review of the Dominant Scattering Mechanisms in SiC MOS Devices: *Jody Fronheiser*[1]; Vinayak Tilak[1]; Kevin Matocha[1]; Greg Dunne[1]; [1]GE Global Research

Silicon Carbide (SiC) based power MOS devices are well suited for high efficiency, high power and high temperature electronics. To date, the poor quality of the SiO2/SiC interface has limited device performance and is the key technical challenge delaying insertion into commercial applications. This highly defective interface leads to a high density of interface traps, low inversion layer mobility, and instability in threshold voltage by temperature and bias stress-induced instabilities. A reduction in the interface trap density and a subsequent increase in inversion layer mobility has been achieved using a post oxidation anneal in nitric oxide yielding mediocre mobilities of 20-30 cm2/Vs. Gates oxides grown in the presence of Sodium (Na) have shown a low density of near interface traps and have demonstrated the highest reported field effect mobility on (0001) 4H MOSFETs up to 150 cm2/Vs. Despite advances in oxidation techniques to improve the SiO2/SiC interface device performance is still below material entitlement. In this article we review the scattering mechanisms most likely responsible for the reduced inversion layer mobility. The main scattering mechanisms: Coulomb scattering, surface roughness scattering, and phonon scattering are discussed for 4H and 6H polytypes in addition to Na contaminated oxides. Similar to Silicon, Coulumb scattering in SiC dominates at low surface electric fields due to interface trapped and positive fixed charge at or near the interface. However at high surface fields SiC does not follow the universal phonon behavior seen in Silicon. This characteristic behavior shows a monotonic

decrease in mobility with increasing surface electric field. Likewise the mobility decreases with increasing temperature. In SiC, Gated Hall measurements taken on 4H MOS devices show the mobility is unchanged to both higher surface fields and increased temperature over the ranges of 0.1 – 0.7 MV/cm and 300 – 425 K respectively. On the other hand, measurements on 6H devices showed a decrease in Hall mobility as a function of temperature and surface electric field suggesting phonon limited mobility for this polytype. Furthermore, phonon limited mobility calculations show a close agreement between simulated and measured Hall effect mobility for 6H while in 4H the measured mobility is ~10 – 25 times lower than expected, suggesting surface roughness scattering. This conclusion is supported by characteristics observed in oxides grown in the presence of Na. The measured inversion charge density as a function of gate voltage for nitrided oxides is roughly 50% of the ideal inversion charge as compared to the Na sample that is nearly ideal, indicating a lower density of interface traps. Although the mobility is high it does not approach phonon scattering entitlement. These results strongly indicate that the inversion layer mobility in 4H SiC is limited by surface roughness scattering at nominal gate voltages.

11:00 AM Student

F3, A Comparative Study of Thermal and Deposited Gate Oxides on 4H SiC: *Sarah Haney*[1]; Veena Misra[1]; Mark Johnson[1]; Juan-Carlos Idrobo[2]; Anant Agarwal[3]; [1]NCSU; [2]Oak Ridge National Labs; [3]Cree

Conventional silicon carbide (SiC) MOSFET fabrication relies on thermal oxidation of the SiC for formation of the silicon dioxide (SiO_2) gate oxide. While this direct oxidation is advantageous from a fabrication standpoint, the resulting MOS devices have exhibited significant interface trap densities, Dit, which reduce effective inversion layer mobility by capturing free carriers as well as via enhanced scattering. More recent studies have further linked this low mobility to a transition region between the SiC and SiO_2, on the SiC side, formed during the thermal oxidation of the SiC.[1] This region has been attributed to increased carbon concentration produced by the thermal oxidation.[2] In this work, we have investigated the atomic layer deposition, ALD, of SiO_2 onto SiC compared to thermal oxidation of SiC. The absence of the carbon out diffusion and subsequent build-up due to thermal oxidation is anticipated to result in an interface free of transition regions when depositing SiO_2 onto SiC with ALD. Capacitors have been formed on 4H-SiC with the following oxide treatments: thermal oxidation at 1175°C, thermal oxidation at 1175°C followed by an nitric oxide, NO, anneal at 1175°C, and ALD of SiC at 150°C followed by an NO anneal at 1175°C. ALD of the SiO_2 was performed using 3-aminopropyltriethoxysiliane (3-APTES), ozone and water. Deposition rates of approximately 0.67Å/cycle are recorded for the process. Thermal oxidation processes consisted of dry oxidation at 1175°C followed by an argon anneal at 1175°C and finally by a 950°C wet oxidation. Capacitance-voltage curves of the samples show improved characteristics for the ALD+NO and thermal+NO samples. While this is expected due to the nitridation of the oxide, the ALD +NO capacitors showed good initial results. A flat band voltage of approximately 0V was recorded as well as D_{it} (calculated from HF and LF C-V curves) in the 7.6E+11 range at 0.2eV from the conduction band edge. This is slightly less than D_{it} values from the thermal oxidation + NO sample which recorded D_{it} of 8.6E+11 at 0.2eV from the band edge. STEM analysis of the ALD+NO sample has been completed, including electron energy loss spectroscopy (EELS) and Z-contrast imaging. Z-contrast imaging showed an amorphous SiO_2 layer and an abrupt interface, with no indication of a transition region. This abrupt interface was also seen in the EELS data which shows no appreciable difference in Si/C ratios throughout the SiC. XPS of the ALD oxides was also performed. Since the effective inversion layer mobility is, most likely, determined by D_{it} as well as transport properties of the transition layer, it is expected that FETs made with the ALD +NO process (in progress) will yield better effective mobility.

11:20 AM Student

F4, Magnetic Resonance Studies of 4H SiC MOS Structures: *Brad Bittel*[1]; P.M. Lenahan[1]; J. Fronheiser[2]; A. Lelis[3]; [1]Penn State Univ.; [2]GE Global Research; [3]US Army Research Lab

SiC/SiO2 interface/near interface defects limit device performance, contributing to low effective channel nobilities and can cause large threshold voltage instabilities. We report on series of measurements utilizing conventional electron paramagnetic resonance (EPR) as well as two electrically detected magnetic resonance EDMR techniques, spin dependent recombination (SDR) and a relatively new technique spin dependent trap assisted tunneling (SDT), to overcome the limits of previous resonance studies on SiC. Last year we reported on conventional EPR measurements utilizing both 30% 13C enriched epi layers and structures with the naturally abundant 1.1% 13C epi layers. The 13C acts as a "marker" allowing some measure of the physical distribution of defects. We have extended this work to EDMR on fully processed MOSFETs with 30% 13C isotopic enrichment. These EDMR results strongly suggest that the defects observed are not amorphous carbon clusters or carbon vacancies, and are consistent with previous EDMR studies which suggest silicon vacancies or silicon vacancy related defects. [1-3] Utilizing EMDR measurements we observe gross changes in the spectrum due to different oxidation processes including sodium enhanced oxidation and two different deposited SiO2 oxidation techniques. These different oxidation processes result in very different field effect mobility and EDMR spectrum. The EDMR spectrum amplitude scales inversely with mobility in all cases except for the sodium enhanced oxidation. The sodium enhanced spectrum also displays an additional center not present in the other oxidation processes. This result suggests that the increased mobility from the sodium oxidation processes is not due to a reduction in interface/near interface traps. Preliminary spin dependent trap assisted tunneling (SDT) measurements on SiC MOS capacitors show an SDT spectrum that is, within the limits of the measurement to date, essentially identical to the well known E' defect spectrum. E' defects are the dominant deep level defects in SiO2 in Si based MOSFETs. [4] This is the first report of SDT in SiC MOS capacitors and the technique shows great promise in helping to unravel the performance limiting defects located in SiO2 on SiC and other material systems. [5] [1] M. Dautrich et al., Appl. Phys. Lett. 89, 223502, (2006). [2] D. Meyer et al., Mat. Sci. Form. 483, pp. 593-596, (2005). [3] C. Cochrane et al., Mat. Sci. Form. 600-603, pp. 719-722, (2009). [4] P.M. Lenahan et al., J. Vac. Sci. Technol., B, 16, pp. 2134-2153, (1998).[5]J. T. Ryan, et al., Appl. Phys. Lett. 95, 103503 (2009).

11:40 AM

F5, Influence of Geometry on Silicon Carbide JBS Diodes Conduction: *Maxime Berthou*[1]; [1]CNM

As Silicon Carbide production qualities and quantities increase, industrial High Voltage applications become real. Industrialization of Silicon Carbide Diodes requires a cost effective production and thus simplification of the fabrication process and increase in the production yield. Because of its unipolar conduction, schottky diode presents the advantage of low current recovery. However the elevated surface electric field makes its reliability very sensitive to it schottky metal imperfections. Moreover, the reverse current is due to tunneling through the schottky barrier and thus it is modulated by surface electric field and temperature. JBS Diodes have been invented in order to reduce surface electric field by pinching the channel under the schottky contact between P boxes. However the P/N junction conduction in direct polarization makes its current recovery more important and temperature dependant. JBS diodes with different sizes and a pure schottky diode have been simulated in direct polarization. The P boxes bipolar conduction has been virtually minimized by the adjunction of a resistance symbolizing the highly resistive ohmic contact. Moreover 1.2kV diodes with the same design parameters (12µm 5.25x1015cm-3) have been fabricated and characterized with Iak(Vak) up to 4V and down to -1500V. Diodes have been fabricated with a tungsten schottky contact, a P+ implantation to create field stopper and P boxes, a P- implantation for the JTE extention and a N+ implantation for the channel stopper. Direct characterization of devices have been conducted under probe with Kelvin measurement, pure schottky diodes exhibited a dynamic resistance around 5.8mOhm.cm2 an Ideality factor of 1.08 , JBS1 with 8µm schottky width and 3µm wide P boxes exhibit dynamic resistance around 7mOhm.cm2, JBS2 is 6.2mOhm.cm2 with a Schottky width of 6µm and JBS3 exhibit 5.55mOhm.cm2 for a schottky width of 8µm. schottky diodes exhibit 100uA for a revert polarization of 1250V and JBS diodes exhibit a leaking current of 100uA at 1400V for JBS3, 1500V for JBS2 and 1600V for JBS1. Simulation predicts 3.6mOhm.cm2 for the Schottky, 3.86mOhm.cm2 for JBS3 and 4.3mOhm.cm2 for JBS1. One should consider that contact resistivity

and schottky barrier imperfection have not been considered in the simulation. However measurements have been performed under probes without real Kelvin contact on back side. Results from simulation and characterization show only unipolar conduction. Moreover, current density is not proportional to the schottky areas in each chip. However, simulation results show that the current flows under the P boxes. Which explain the modulation of the resistivity only by the area of conduction under the whole diode and not only the schottky area. Thus it is possible to optimize the P boxes geometry and size so that one can take advantage of the schottky direct properties and JBS reverse advantages.

Session G: Oxide Semiconductor Thin Film Transistors

Wednesday PM
June 23, 2010

Room: 102
Location: University of Notre Dame

Session Chairs: John Conley, Oregon State Univ; Tom Jackson, Penn State Univ

1:30 PM Student

G1, Temperature Dependent Measurements of ZnO TFTs: *Devin Mourey*[1]; Dalong Zhao[1]; Thomas Jackson[1]; [1]Penn State University

PEALD ZnO transistors on glass and polyimide substrates have field-effect mobility > 20 $cm^2/V•s$, good bias-stress stability, and circuits with < 10 ns/stage propagation delay.[1] For high-performance TFTs, self-heating can result in high temperatures on low-cost, low-thermal conductivity substrates such as glass (1.3 W/m•K) and polyimide (0.15 W/m•K). To understand thermal effects we have measured devices from 10 K to 400 K. A plot of $\ln(\mu_e)$ versus 1/T shows that the field-effect mobility is weakly activated between 400 K and 100 K with activation energy of ~ 10 meV. For comparison, in amorphous silicon the activation energy is often > 150 meV due to the large density of localized tail states.[2] For PEALD ZnO, as the temperature decreases below 100 K the activation energy decreases and as a result PEALD ZnO TFTs operate with mobility > 1 $cm^2/V•s$ even at temperatures < 10 K. The temperature behavior can be well described using a percolation model assuming a Gaussian distribution of barriers above the conduction band edge. This model has previously been applied to temperature dependent Hall-effect measurements in doped indium-gallium-zinc oxide films. [3] By fitting temperature dependent behavior at constant $V_G - V_T$ we examine how the model barrier height changes with channel carrier accumulation. In our oxide TFTs, we find that the barrier height and standard deviation steady decrease from ~ 50 ± 20 meV at 5 x $10^{12}/cm^2$ to ~ 7 ± 6 meV at 1.4 x $10^{13}/cm^2$ and the temperature independent mobility prefactor increases from 12 to 22 $cm^2/V•s$. This reduction of barrier height and distribution width provides a mechanism for the carrier concentration dependent mobility observed in nearly all oxide thin films and devices. In addition, at the highest accumulations the barrier height becomes very small which is consistent with the good performance of these devices even at very low temperature. We also find a fully reversible, nearly linear positive shift in threshold voltage with decreasing temperature from 300 K to 100 K with a charge coefficient of about -4 nC/cm^2K. While the origin of this charge is not fully understood, ZnO films deposited by PEALD are highly textured (002) and may exhibit a pyroelectric charge with changes in temperature, although the threshold voltage shifts below 100 K are likely not related to pyroelectric charge. The temperature dependent characteristics of these TFTs demonstrate that PEALD ZnO does not contain a large concentration of deep subgap traps as often found in other low-deposition-temperature thin film systems. [1] D. A. Mourey, et. al., IEEE Trans. on Elec. Devices, 57, 530-534, 2009. [2] T. Tiedje, et. al., Physical Review Letters, 46, 1425, 1981. [3] T. Kamiya, et. al., J. Display Technol., 5, p. 462-467, 2009.

1:50 PM Student

G2, Flexible ZnO Temperature Sensors on Plastic Substrate: *Dalong Zhao*[1]; Devin Mourey[1]; Thomas Jackson[1]; [1]Pennsylvania State University

We have previously demonstrated plasma enhanced atomic layer deposition (PEALD) ZnO thin film transistors (TFTs) and circuits on polyimide substrates at 200 °C with field-effect mobility > 20 cm^2/Vs, excellent bias stress stability, and circuits with propagation delay < 20 ns/stage[1]. PEALD ZnO TFTs have a linearly decreasing threshold voltage with increasing temperature and we have explored the use of arrays of these devices as flexible, thin film temperature microsensors. Flexible temperature sensors have previously been reported based on platinum resistors with small dimensions < 100 × 100 µm and with good temperature resolution of ~2 °C.[2] The flexible temperature sensors described here have comparable size, but provide improved sensitivity and lower current operation, as well as simple integration with additional TFTs for sensor select and isolation. In this work, ZnO TFT temperature sensors were fabricated on 25 µm thick polyimide substrates using PEALD at 200 °C and a previously described TFT fabrication process [3]. Several designs of nine individual 100 × 5 µm ZnO pyroelectric TFTs were fabricated on 2 cm long and 500 µm wide flexible probes and in some designs line select TFTs were also integrated. Devices on these polyimide substrates typically had field-effect mobility of 10 - 15 cm^2/Vs. The temperature dependence of typical flexible devices was measured from 20 to 70 °C and a reversible linear shift in threshold voltage was observed, with associated pyroelectric charge coefficient of 1.5 nC/cm^2K. When measured in the subthreshold regime at constant gate bias, a small change in threshold voltage results in a large change in conductance, and provides good temperature sensitivity. Devices were calibrated between 20 – 35 °C using a surface mounted thermocouple and a gate voltage of -3 V and constant drain current of 4 nA. Sensitivity depends on the bias conditions and in the subthreshold a maximum of > 350 mV/°C is observed. This change is equivalent to an effective temperature coefficient of resistance of more than 10%. Using a more complex biasing approach it is possible to adjust the sensor sensitivity and dynamic range to suit various applications. These results demonstrate that high performance ZnO pyroelectric TFTs can be used for temperature sensing on flexible substrates and may provide opportunities in novel non-planar and integrated temperature arrays. [1] D. A. Mourey, D. A. Zhao, and T. N. Jackson, IEDM, paper 8.5, 2009. [2] Y. Moser and M. A. M. Gijs, J. of Microelectromechanical Systems, 16, 1349-1354, 2007. [3] D. A. Mourey, D. A. Zhao, J. Sun, and T. A. Jackson, IEEE Trans. Electron Devices, 57, 530-534, 2010.

2:10 PM Student

G3, Improvement of $InGaZnO_4$ TFT Device Performance on Glass and Paper Substrates: *Erica Douglas*[1]; Wantae Lim[1]; Youngwoo Heo[2]; David Norton[1]; Fan Ren[1]; Stephen Pearton[1]; [1]University of Florida; [2]Kyungpook National University

$InGaZnO_4$ thin film transistors (TFTs) show exceptional promise for use in the backplane of active matrix organic light emitting diodes (AMOLEDs) and liquid crystal displays (LCDs) [1-3]. This is due to their high electron mobility and exceptional surface smoothness. $InGaZnO_4$ can also be deposited by sputtering at room temperature. This allows for TFTs to be fabricated on a variety of substrates, including glass, plastics and even paper [4]. Stability for unpassivated and SiO_x passivated devices under bias were investigated. Little to no effect to the threshold voltage (VTH) and subthreshold gate voltage swing was observed for gate bias at 5V. However, at voltages greater than 10V, both unpassivated and passivated devices showed positive VTH and S shifts. The positive VTH and S shifts after constant gate voltage stress (+20 V) for 1000 s were 1.8 V and 0.72 V decade-1 for the unpassivated devices and 1 V and 0.42 V decade-1 for the passivated devices, respectively. SiO_x passivation, though, significantly reduced the shift in TFT characteristics. Dual gate TFTs were fabricated on glass for OR logic operation. Compared to bottom-gate (BG), top-gate (TG) TFTs exhibited better device performance, with higher saturation mobility, drain current on-to-off ratio, lower threshold voltage, and subthreshold gate-voltage swing. This improved performance was mainly attributed to low process-induced damage or low parasitic capacitance between gate and source/drain and low parasitic resistance between channel and source/drain in top-

contact TFT configuration (coplanar type). These results demonstrated that DG InGaZnO$_4$ TFTs are effective in improving device performance. This paper also reports on the fabrication of IGZO TFTs on paper, and the effect of various planarization layers in order to improve device performance. As a water and solvent barrier layer, cyclotene (BCB 3022-35 from Dow Chemical) was spin-coated on the entire paper substrate. TFTs on the paper substrates exhibited device characteristics only slightly inferior to those obtained from devices on glass substrates. The uneven surface of the paper sheet led to relatively poor contact resistance between source-drain electrodes and channel layer. The ability to achieve InGaZnO TFTs on cyclotene-coated paper substrates demonstrates the enormous potential for applications such as low-cost and large area electronics.

2:30 PM

G4, Sputtering of ZnO Thin Films for TFT on Polyimide Substrates: Xiaotian Yang[1]; Chieh-Jen Ku[1]; *Faraz Khan*[1]; Pavel Reyes[1]; Chung Kuo[1]; Yicheng Lu[1]; [1]Rutgers University

ZnO thin film transistors (TFTs) have drawn great interest over the last five years. It appears likely to find use in flat panel displays, radio-frequency electronics, and low-cost large-area electronics, depending on the device performance using various growth methods such as MOCVD, ALD, PLD or Sputtering. We report on the fabrication of flexible sputtered ZnO-based TFTs, with field-effect mobility > 1.0 cm2/Vs suitable for use in low-cost large-area flexible electronics. A 100 µm thick polyimide substrate is used as the flexible substrate, and the correlation of sputtering conditions and ZnO electrical properties were investigated. Prior to all device processing, the substrates are pretreated at 300ºC for 3 hours to improve thermal dimensional stability and are passivated with 300nm PECVD silicon dioxide. Then, a 100nm thick aluminum layer was evaporated on the substrate as the common-gate electrode and a 180nm thick silicon dioxide was deposited at 250ºC by PECVD as the gate dielectric. To form the semiconducting layer, a 100nm thick ZnO was deposited using rf sputtering with the substrate held at 100ºC. The ZnO film was patterned with photolithographic etching and Al or Ti was deposited for the source and drain contacts with lift-off metallization. Because the stoichiometric ratio of oxygen and zinc is strongly related with the defect-associated shallow doping, dominantly zinc vacancy (Vzn) and oxygen vacancy (Vo), consequently, producing the n-type carriers, we use the ratio of oxygen to argon pressure during the sputtering (0:10 to 3.3:10) to control the ZnO composition. The electrical testing shows that device performance of ZnO TFTs on flexible substrates are much improved when a lower O2 to Ar pressure ratio is used, particularly, the on-off current ratio increases by four orders of magnitude to 10^6 and saturation mobility improved from less than 0.01 to 1.5 cm2/Vs. This indicates that the incorporation of oxygen in ZnO films is controlled by the oxygen to argon pressure, as well as the electron concentration and conductivity. Device modeling is conducted to simulate this effect. In addition, a thermal treatment after device fabrication significantly improves I-V characteristics and the gate dielectric quality, where samples were subjected to annealing at 250ºC for 3 hours in nitrogen ambient. The leakage current through gate electrode and the off state current are repressed. However, an improvement or an alternative of gate dielectric is necessary to achieve higher performance and a proper yield in comparison with state of art results today.

2:50 PM Student

G5, Zinc-Tin-Oxide Thin-Film Transistors with Al_2O_3 and ZrO_2 Gate Dielectrics: *Josh Triska*[1]; John Conley[1]; Rick Presley[1]; John Wager[1]; [1]Oregon State University

Amorphous hydrogenated silicon (*a*-Si:H) is currently the dominant material for the thin-film transistor (TFT) backplanes used to drive liquid crystal displays, but it exhibits several drawbacks which limit its use in future display technologies. The drawbacks of *a*-Si:H include low electron mobility that is limited to ~1 cm^2/V•s, lack of transparency, and well-known instabilities under bias stress and light exposure. Despite these instabilities, the use of silicon nitride as a gate dielectric has allowed for operation stable enough that *a*-Si:H has dominated the flat panel display market. However, the requirements for the current driver in OLED displays, where high mobility is needed and any shifts in threshold voltage (V_{th}) will affect pixel brightness, may limit the use of *a*-Si:H for this application. A new class of amorphous oxide semiconductor (AOS) has recently been developed which exhibits high mobilities (>10cm^2/V•s) and can be processed at low temperatures. Thin-film transistors with AOS channels are promising candidates for OLED displays and transparent applications. In particular, zinc-tin-oxide (ZTO) is a promising channel material due to its relatively high mobility of ~15 cm^2/V•s at low processing temperatures and inexpensive base elements. In this work, TFTs with ZTO channels and ALD Al_2O_3 gate dielectrics are shown to exhibit good mobility and subthreshold slope, but exhibit positive V_{th} shifts under positive gate bias stressing for up to ~10^5 seconds. The use of a thin PECVD SiO_2 capping layer to modify the channel/dielectric interface is shown to improve device stability. Initial TFTs fabricated using ALD ZrO_2 gate dielectrics (with TEMAZ and H_2O as ALD precursors) are found to exhibit performance similar to that of Al_2O_3 devices. An investigation of ZrO_2 device stability under positive gate bias stressing is underway and will be compared to TFTs with Al_2O_3 and SiO_2 gate dielectrics.

3:10 PM Break

3:30 PM Student

G6, Study of CV and Admittance Characteristics of ALD High-K Dielectric ZnO Capacitors: *Jeffrey Siddiqui*[1]; Du Nguyen[2]; Jamie Phillips[1]; Kevin Leedy[3]; Burhan Bayraktaroglu[3]; [1]University of Michigan; [2]Michigan State University; [3]Air Force Research Laboratory

ZnO Thin Film Transistors (TFTs) have attracted attention due to high carrier mobility in the material. Many possible applications including low cost and/or flexible electronics exist. Recent results on these devices include the demonstration of high-performance operation at microwave frequencies [1]. The incorporation of high-k dielectrics is expected to further improve device performance, but there are few reports of the detailed electronic characteristics of ZnO/high-k dielectric interfaces. In this work, the characteristics of ZnO heterojunctions with high-k Al_2O_3 and HfO_2 dielectrics deposited by atomic layer deposition will be presented with emphasis on capacitance-voltage and admittance spectroscopy characteristics of metal-dielectric-ZnO structures. Materials consist of high-k dielectric thin films including Al_2O_3 and HfO_2 deposited by atomic layer deposition with and without remote oxygen plasma and ZnO thin films deposited by pulsed laser deposition. Capacitor test structures are in the bottom gate configuration using Pt/Ti/SiO_2/Si substrates with top metal contacts of Ti/Pt for metal-dielectric-metal structures and Ti/Al/Au ohmic contacts to ZnO for metal-dielectric-ZnO structures. Capacitance-voltage and current-voltage characteristics were measured using a Keithley 4200 system with CVU module. The metal-dielectric-metal capacitors indicate that Al_2O_3 and HfO_2 have dielectric constants of approximately $10\varepsilon_0$ and $20\varepsilon_0$ and leakage currents of less than $2x10^{-9}$ and $2x10^{-7}$ A/cm^2, respectively. Both films have breakdown fields of approximately $3x10^6$ V/cm. Capacitance-voltage characteristics of metal-dielectric-ZnO structures show clear accumulation and depletion behavior with varying turn-on voltage of less than 1 V for Al_2O_3 dielectrics and more than 2 V for HfO_2 dielectrics. The higher threshold voltage observed for the HfO_2 dielectrics may be due in part to interfacial defects. Admittance spectroscopy measurements were also conducted on the samples to evaluate the interface charge concentration. Variations in turn-on voltage, interfacial charge concentration, and energetic dependence of interfacial charge will be presented for the various dielectric thin films and discussed in the context of ZnO TFT performance. [1] B. Bayraktaroglu, K. Leedy, R. Neidhard, "Microwave ZnO Thin Film Transistors," IEEE Elec. Dev. Lett., vol. 29. No. 9, Sep. 2008.

3:50 PM Student

G7, Transparent Rectifying Contacts - A New Concept for Transparent Electronics: *Alexander Lajn*[1]; Heiko Frenzel[1]; Holger von Wenckstern[1]; Marius Grundmann[1]; [1]Universität Leipzig

Transparent electronic in combination with transparent light emitters permit the fabrication of fully transparent displays. Thus, new designs involving higher information content, better ergonomics, lower power consumption and new aesthetic aspects are feasible; e.g. in car wind shields, windows, sun glasses, monitors or cell phones. We report on the fabrication of fully transparent diodes, field-effect transistors and inverters, based on a new concept employing transparent rectifying contacts (TRC) for transparent electronics. The TRC

consist of a combination of a reactively dc-sputtered Ag_xO or PtO_y layer and a transparent and highly conducting capping layer; the total thickness is only 10 nm. With that an average transmission of 70% and 60% in the visible spectral range was achieved for the complete device structure on a ZnO thin film with Ag_xO and PtO_y, respectively. The so formed Schottky-like diodes exhibit maximum effective barrier heights of 0.87 eV, ideality factors of 1.47 and rectification ratios of 5×10^6, which are similar to their opaque counterparts [1]. Using such kind of contacts as gate contacts in transparent metal-semiconductor field-effect transistors (TMESFET), on/off-ratios of ~10^6 and channel mobilities of up to 11.9 cm^2/Vs, which are only slightly lower than for opaque MESFETs [2, 3], were achieved. With that, our devices meet the requirements for the use in transparent displays formulated by Wager [4]. Moreover the TMESFETs require small voltage sweeps of only 2.7 V for switching between on and off-state. This is due to the absence of a voltage drop at a gate insulator, as it occurs in metal-insulator-semiconductor-FETs. Furthermore, with 120 mV/dec, the subthreshold slope of the TMESFETs already approaches the thermodynamic limit of 60 mV/dec. These advantages of MESFET were successfully transferred to integrated inverters, which have a maximum gain of ~200 at a supply voltage of 4 V and a low uncertainty level of ~0.3 V. Their performance is superior among the transparent inverters reported so far (e.g. [5]) and clears the way to fully transparent logic integrated circuits. This work is supported by Deutsche Forschungsgemeinschaft within the framework of Sonderforschungsbereich 762 “Functionality of Oxidic Interfaces” and the Graduate School “Leipzig School of Natural Sciences - BuildMoNa” as well as the European Social Fund and Studienstiftung des deutschen Volkes. [1] A. Lajn, et al., J. Vac. Sci. Technol. B, 27, 1769 (2009); [2] H. Frenzel, et al., Appl. Phys. Lett., 92, 192108 (2008); [3] H. Frenzel, et al., Appl. Phys. Lett., 95, 153503 (2009); [4] J. F. Wager, Science, 300, 1245 (2003); [5] J. H. Na, et al., Appl. Phys. Lett., 93, 213505 (2008).

4:10 PM

G8, Transition from Hopping to Band-like Transport in Solution-Processed Amorphous Zinc Tin Oxide Thin-Film Transistors: *Chen-Guan Lee*[1]; Brian Cobb[1]; Ananth Dodabalapur[1]; [1]University of Texas at Austin

Amorphous oxide semiconductors have attracted much attention because of their high mobility, stability in ambient air and easy processing by solution approaches. Band-like transport is possible for amorphous oxide semiconductors because of their large neighboring ns orbital overlapping, which is insensitive to distorted Metal-Oxide-Metal chemical bonds. In this study, we combine solution-processed zinc tin oxide (ZTO) together with solution-processed high-k dielectric, ZrO_2, to study the nature of charge transport as a function of gate bias. A top-contact configuration is employed while the substrate and the gate electrode are glass and AuPd, respectively. The ZrO_2 precursor solution was spin-coated in a nitrogen box at 2000 rpm for 30 seconds and was kept in nitrogen box for one hour to evaporate the residual solvent (2-methoxyethanol). Then, the spin-coated film was annealed on a hot plate in air at 500°C for one hour. The deposition process of gate dielectric was repeated once to achieve a thickness of ~90nm. The ZTO precursor solution (0.2 M of $ZnCl_2$ and $SnCl_2$ in acetonitrile) was spin coated in nitrogen box at 6000rpm for 30 seconds and followed by a soft bake at 100°C for 30 minutes. The spin-coated film was annealed on a hot plate in air at 500°C for one hour. Al source/drain electrodes were patterned by shadow mask with an aspect ratio of 20 (L=50µm). The capacitance value for this dual layer ZrO_2 dielectric is ~250 nF/cm^2, the on/off ratio is >10^6 and a saturation mobility of 16 cm^2/V.s is obtained at V_G=V_D=5V at room temperature. The mobility is carrier concentration dependent. Transfer curves with higher carrier concentration (V_{DS}=10V and V_G=0~10V) are compared at different temperatures ranging from 77K to 333K. When plotting mobilities vs. (V_G-V_{ON}), we can find that the mobility decreases with decreasing temperature at lower sheet carrier concentration (V_G-V_{ON}<7V), which suggests localized transport. In contrast, the mobility decreases with increasing temperature at higher sheet carrier concentration (V_G-V_{ON}>7V), which suggests band-like transport. The V_{ON} is the onset voltage, which corresponds to the voltage that the carrier concentration starts to accumulate with increasing gate voltage. The activation energies at different V_G-V_{ON} are calculated and show that the activation energies decrease with increasing sheet carrier concentration. These results are in accordance with Motts mobility edge model - at lower sheet carrier concentration (lower V_G-V_{ON}), the Fermi level is in the band tail states and the transport is likely dominated by multiple trap and release of electrons by relatively shallow traps. However, the Fermi level moves towards the band edge at higher sheet carrier concentration and the transport is band-like. Conductivities at different sheet carrier concentrations are extracted from the linear regime of the output characteristics (V_DI_D) and the result shows that the conductivity increases with raising temperature for all sheet carrier concentrations. At the highest sheet carrier concentrations, the conductivity values are slightly less than 100(S/cm), implying that the conductivity is still in insulator regime, although approaching the metallic limit.

4:30 PM Student

G9, A Comparative Study of the Effect of Heat Treatment on the Microstructure and Properties of Colloidal ITO Films and Cold-Sputtered ITO Films: *Salil Joshi*[1]; Gregory Book[1]; Rosario Gerhardt[1]; [1]Georgia Institute of Technology

Indium Tin Oxide (ITO) is an important transparent conductor that finds widespread applications in displays and other optoelectronic technologies. Fabrication of circuits and coatings from colloidal ITO has the advantage of being less wasteful as compared to sputtering, and may be advantageous for use on flexible and complex-shaped substrates that cannot withstand high temperatures. This study deals with the comparison of the effect of processing treatment such as oxygen plasma and heat treatment, on colloidal ITO films and cold-sputtered ITO films. Colloidal, fully crystalline ITO nanoparticles were made by a non-aqueous synthesis technique starting from acetate precursors [1]. Films were fabricated on glass and quartz substrates. ITO coatings were also fabricated using RF sputtering on identical, non-heated substrates. The microstructural changes in the ITO films were characterized through AFM and SEM. The electrical and optical properties were characterized using impedance spectroscopy and UV-visible absorption spectroscopy.The ITO films were heat treated in an atmosphere of argon or commercial air at 150°C, 300°C, and 450°C. Heat treatment of cold-sputtered ITO films changed properties such as transmittance in the visible region, optical band gap and the electrical resistivity of the films. Heat treating in air was seen to increase the resistivity, while heat treating in argon was seen to decrease the resistivity. The as-cold sputtered ITO films are amorphous, and are brown in color. Their transmittance increased significantly on heating. These changes can be related to the onset of crystallization, and changes in the carrier concentration due to the changes in the oxygen stoichiometry with heat treatment. In contrast, the colloidal ITO films are fully transparent as coated, because the colloidal nanoparticles are fully crystalline. Heat treatment at 300°C in argon caused a reduction in the transmittance in the colloidal ITO film due to charring of the organics. The electrical properties of the spin-coated colloidal ITO films were also significantly modified by the presence of the non-conducting ligands. The electrical properties vary as a function of sintering and non-stoichiometry as the oxygen content is varied. The removal of the non-conducting ligands from the colloidal ITO by oxygen plasma prior to heat treatment should improve the electrical properties. The effect of oxygen plasma on the electrical and optical properties will also be presented. [1] C. J. Capozzi, I. N. Ivanov, S. Joshi, and R. A. Gerhardt, “The effect of the atmosphere on the optical properties of as-synthesized colloidal indium tin oxide”, Nanotechnology, vol. 20, p. 145701, 2009.

4:50 PM

G10, Optimization of Dielectric Passivation of ZnO-Based Schottky Diodes: *Holger von Wenckstern*[1]; Stefan Müller[1]; Matthias Schmidt[1]; Florian Schmidt[1]; Marius Grundmann[1]; [1]Universität Leipzig

Schottky barrier contacts on ZnO have been studied with renewed interest in recent years. They are used in, e.g., photodetectors, metal-semiconductor field-effect transistors and gas sensors but are also of high importance for electrical characterization of ZnO by space charge layer spectroscopy since ZnO pn-diodes are not available. The optimization of Schottky diode properties focused on surface preparation and the choice of the Schottky barrier material so far. Recently it was demonstrated that the rectifying properties of high-quality Schottky contacts may degrade under reduced pressure [1]. This is caused by vacuum-activated surface conduction strongly reducing the parallel resistance

R_p and by that increasing the leakage current of the Schottky diodes [1]. On the one hand this presents a major drawback considering the usage of, e.g., ZnO UV photodetectors in outer space; on the other hand it is disadvantageous for electrical characterization techniques performed under cryogenic conditions such as deep level transient spectroscopy. In a proof of concept study we demonstrated that dielectric passivation of ZnO Schottky diodes suppresses the formation of the vacuum-activated surface conduction path [2]. In this contribution we report on different strategies used to optimize such dielectric passivation. We used ZnO thin films grown on 2 inch sapphire wafers by pulsed-laser deposition (PLD). The samples were cut into pieces. On some pieces we reactively sputtered planar Schottky contacts prior to dielectric passivation (approach B); for other pieces the passivation was deposited prior to the Schottky contacts (approach C). The electric properties are compared to non-passivated diodes (approach A). The masks needed to define the contacts and passivations were realized by standard photolithography. The dielectric passivation, either being $CaHfO_3$ or Al_2O_3, was grown at room temperature by PLD. For each passivation at least 40 Schottky contacts were produced on one sample piece and are compared to diodes realized on another piece of the same wafer in order to obtain a significant set of data. For characterization we used current-voltage measurements; selected samples were investigated by thermal admittance spectroscopy, deep level transient spectroscopy and depth-resolved cathodoluminescence (CL). The results show that dielectric passivation increases the CL UV/VIS ratio for excitation close to the surface, it does not introduce additional defects and it suppresses the formation of a vacuum-activated surface conduction path. Further, the parallel resistance of Al_2O_3-passivated diodes is in average higher than that of non- or $CaHfO_3$-passivated diodes; the scatter of R_p is largest for non-passivated diodes. Our results show that it is favorable to realize the passivation prior to the Schottky contacts (approach C). [1]M. Allen *et al.*, IEEE Transaction on Electron Devices 56, 2160 (2009). [2]von Wenckstern *et al.*, J. Electron. Mater. available online, DOI: 10.1007/s11664-009-0974-1.

Session H: Materials and Devices for Flexible Electronics

Wednesday PM
June 23, 2010

Room: 126
Location: University of Notre Dame

Session Chairs: Oana Jurchescu, Wake Forest University; Alberto Salleo, Stanford University

1:30 PM Student

H1, Molecular Contact Doping in Organic Thin-Film Transistors: *Frederik Ante*[1]; Tobias Canzler[2]; Ansgar Werner[2]; Ute Zschieschang[1]; Klaus Kern[3]; Hagen Klauk[1]; [1]Max Planck Institute for Solid State Research, Stuttgart, Germany; [2]Novaled AG, Dresden, Germany; [3]Ecole Polytechnique Fédérale de Lausanne, Switzerland

The drain current of organic thin-film transistors (TFTs) is often limited by the energy barrier at the interface between the semiconductor and the source/drain contacts. This energy barrier can be reduced by choosing a contact metal with a work function matching the frontier orbital energy of the semiconductor [JAP 96, 7312, 2004], by modifying the metal work function with a thin oxide layer [APL 92, 013301, 2008], or by introducing a self-assembled monolayer (SAM) with an appropriate dipole moment [JACS 128, 1788, 2006]. Here we show that the contact barrier in organic TFTs can also be reduced by introducing a thin layer of a strong molecular dopant at the semiconductor/contact interface. Our TFTs are based on the organic semiconductor dinaphtho-[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT). The dopant (NDP-9, provided by Novaled AG) is a small organic molecule with a LUMO energy below the HOMO energy of DNTT, so electrons are transferred from the DNTT to the dopant, increasing the local density of excess holes in the DNTT near the contacts. Transistors with a channel length between 10 and 60 µm are fabricated using polyimide shadow masks and consist of Al gates (30 nm thick), an AlOx/SAM gate dielectric (5.7 nm), vacuum-deposited DNTT (30 nm), a thin dopant layer (~1 nm) and Au top contacts (30 nm). The mobilities of undoped transistors (with a contact resistance of 0.66 kOhm-cm) range from 0.9 cm^2/Vs (L = 10 µm) to 2.2 cm^2/Vs (L = 60 µm). For contact-doped transistors (with a contact-resistance of 0.38 kOhm-cm) the mobilities are between 1.3 cm^2/Vs (L = 10 µm) and 2.3 cm^2/Vs (L = 60 µm). To fabricate top-contact DNTT TFTs with sub-micron channel length, we have expanded a process reported by Tsukagoshi et al. [APL 91, 113508, 2007]. A narrow suspended resist bridge is defined across the Al/AlOx/SAM gate stack by electron-beam lithography using a multi-layer resist process. The organic semiconductor is deposited underneath the bridge by two angled evaporations (45° and 135°). Finally the organic dopant and the Au source/drain contacts are evaporated at an angle of 90°, so that the resist bridge serves as a high-resolution shadow mask to define the channel length. The 150 nm long transistors have a mobility of 0.05 cm^2/Vs, an on/off current ratio of 10^6 and a transconductance of 0.4 S/m. In the undoped transistors a deviation from the ideal transistor behavior is observed for small drain-source voltages (Schottky contacts). In contrast, the contact-doped transistors have a reduced contact barrier and improved transistor behavior, especially at small drain-source voltages (ohmic contacts). In summary, we have shown an improvement of top-contact organic TFTs with a channel length from 100 nm to 60 µm by introducing a molecular dopant into the contact area.

1:50 PM Student

H2, Gate Dielectric Thickness Dependence of OTFT Performance: *Yuanyuan Li*[1]; Devin Mourey[1]; Dalong Zhao[1]; Haoyu Li[1]; Marsha Loth[2]; John Anthony[2]; Thomas Jackson[1]; [1]Penn State University; [2]University of Kentucky

Solution based organic semiconductors have been widely investigated for their potential in low cost flexible electronics. Organic thin film transistors (OTFTs) fabricated using spin casting of the p-type organic semiconductor 5,11-Bis(triethylsilylethynyl) anthradithiophene (diF-TES-ADT) have demonstrated mobility > 1 cm^2/V•s and a contact-related microstructure for pentafluorobenzenthiol treated electrodes on thermal SiO_2.[1,2] For organic devices and circuits on transparent and flexible substrates, dielectric materials are needed which can be easily deposited at low temperature on glass and flexible substrates. Al_2O_3 can be deposited by plasma enhanced atomic layer deposition (PEALD) at 200°C [3] and has been used to fabricate high-performance ZnO TFTs. In this work we have fabricated OTFTs with thin Al_2O_3 dielectric layers. The OTFTs for this work used a simple structure with gold source and drain electrodes photolithographically defined on a dielectric layer on a heavily doped n-type silicon wafer. We fabricated devices on 32 nm and 60 nm PEALD Al_2O_3 and 210 nm thermal SiO_2. PFBT was used to treat the Au electrodes provide the contact related microstructure, and HMDS was used to treat the dielectric layer. A 2.5 wt% solution of diF-TES-ADT chlorobenzene was spin coated on the substrates, and the expected contact-related microstructure was observed on all samples. diF-TES-ADT TFTs fabricated with 210 nm SiO_2 with 5 µm channel length had field-effect mobility of ~0.7 cm^2/V•s , threshold voltage of ~15 V, and on current is larger than 10^{-4} A at V_G = -20 V and V_D = -40 V. Similar OTFTs fabricated with 60 nm Al_2O_3 had field-effect mobility of ~0.2 cm^2/V•s, threshold voltage of ~1 V, and on current of ~ $5*10^{-5}$ A at V_G = -10 V and V_D = -20 V. Similar OTFTs fabricated on 32 nm Al2O3 had field-effect mobility of ~0.1 cm^2/V•s , threshold voltage of ~0.5 V and on current of ~ $4*10^{-5}$ A at V_G = -10 V and V_D = -15 V. Plotting the OTFT current as a function of the gate electrical field, including correcting for apparent threshold voltage, also shows that the OTFT current decreases with decreasing gate dielectric thickness. Preliminary two dimensional modeling suggests this unexpected result can be explained by two-dimensional electric field effects at a Schottky barrier between the organic semiconductor and source and drain contacts. [1] S. K. Park, SPIE Conference Digest, 100 (2007). [2] D. J. Gundlach, et al. Nature Materials, 7(3), 216-221 (2008). [3] D. A. Mourey, et al, IEEE Trans. Electron Dev., 57, pp. 530-4 (2010).

2:10 PM Student

H3, Arylene Diimide-Thiophene Semiconductors for n-Channel Field-Effect Transistors: *Rocio Ponce Ortiz*[1]; Hui Huang[1]; Antonio Facchetti[1]; Tobin Marks[1]; Yan Zheng[2]; Raul Blanco[3]; Helena Herrera[3]; Jose Segura[3]; [1]Northwestern University; [2]Polyera Corporation; [3]Complutense University of Madrid

Oligothiophenes and arylene-diimide derivatives are among the most used semiconductors in the fabrication of Organic Field Effect Transistors (OFETs). One intriguing strategy to improve the electrical behavior and/or achieve ambipolarity in organic semiconductors would be the combination of arylene diimide skeleton with thiophene rings within the same molecular structure. To this end, we have fabricated the first family of molecules consisting of β-naphthalenediimide and β-perylenediimide oligothiophenes. This family of semiconductors allows us to analyze the interplay of three different effects on device response: (i) oligothiophene backbone catenation; (ii) interchanging naphthalenediimide by perylenediimide substituents, and (iii) introducing a phenylene group in the olighothiophene backbone. Amphoteric redox behavior is recorded in these molecules by cyclic voltammetry, indicating the possibility of both electron extraction and injection from/into the conjugated p-system. Electrical measurements of vapor-deposited films measured in vacuum show electron field-effect mobilities as high as 0.35 $cm^2V^{-1}s^{-1}$ for semiconductor NDI-1T. Lower mobilities, on the order of 0.1-10-4 $cm^2V^{-1}s^{-1}$, are recorded for the remainder of the semiconductors. The remarkable variation in electrical behavior within the semiconductor family is analyzed by means of electrochemistry experiments, X-ray diffraction and Atomic Force Microscopy (AFM), and is aided by theoretical Density Functional Theory (DFT) calculations. It will be shown that the differences in carrier mobilities can be basically explained on the basis of molecular packing and film microstructural trends. Indeed, the best device performance is measured for NDI-1T films, where calculations predict the molecule to be basically flat, thus promoting a closely packed crystalline film which is consistent with a well-resolved single phase XRD pattern. Furthermore, AFM reveals the presence of large and well-connected grains. On the contrary, the poor electrical performance of NDI-3T is likely connected with the poor film crystallinity (in fact no diffraction peaks are detected in XRD experiments) and with the presence of very small grains with increased grain boundaries. Solution-processed OFETs were also fabricated and their electrical performance compared with that of the corresponding vapor-deposited films. Field-effect mobilities of 0.042 $cm^2V^{-1}s^{-1}$ and 0.011 $cm^2V^{-1}s^{-1}$ were obtained for PDI-1T and PDI-3T, respectively.

2:30 PM Student

H4, Advanced X-Ray Peak Shape Analysis of Organic Semiconductors: Insights into Crystalline Size, Strain, Intragrain Disorder and Implications for Charge Transport: *Jonathan Rivnay*[1]; Michael Toney[2]; Alberto Salleo[1]; [1]Stanford University; [2]Stanford Synchrotron Radiation Lightsource

Structure-property relations have guided the development and processing of organic electronic materials and devices over the past two decades, leading to films with field effect mobilities around 1cm^2/Vs. Such studies have focused on relative crystallinity, grain boundaries, film cracking, as well as molecular packing and orientation, in attempt to understand device-scale charge transport and performance. Grain size or grain boundary density is often cited as a reason for improved or degraded device performance. However, even the determination of grain size can be difficult: grain dimensions are often extracted from top-surface scanning probe techniques, rough estimation from X-ray peak widths or optical microscopy of crystalline domains with similar polarization extinction characteristics; the latter technique is especially common (and sometimes misleading) in small molecule films. Furthermore, the details of intra-grain order are important when considering charge transport within a grain. Deviations from ideal crystal packing will affect the crystalline transport and may shed light on the origins of intrinsic charge trapping in semi/polycrystalline organic materials. The study of disorder within crystalline grains is challenging due to the instability of organic materials under the prolonged electron beam exposure necessary for transmission electron microscopy. The small grain size, often on the order of tens of nanometers, further complicates characterization. One promising analysis technique is order-dependent Fourier X-ray peak shape analysis, developed by Warren and Averbach in the early 1950's. The Warren-Averbach (WA) analysis allows one to simultaneously extract grain size, as well as parameters relating to non-uniform strain and statistical disorder (paracrystallinity) within the grain, both of which are the primary causes of higher-order peak broadening. To this end, we present a series of datasets with crystalline order both out-of-plane and in-plane and discuss the implementation of WA analysis as a tool to extract disorder parameters. Diffraction data is collected from a number of solution processable, high performance transistor and solar cell materials, including poly(2,5-bis(3-alkylthiophene-2-yl)thieno[3,2-*b*]thiophenes) (PBTTT), poly{[N,N'-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6,-diyl]-alt-5,5'-(2,2'-bithiophene)}, P(NDI2OD-T2), and triisopropylsilane (TIPS) pentacene. We discuss how parameters extracted from WA analysis may influence charge transport. Experiments are designed to elucidate the effects of annealing, alignment and blending on grain size, inter-grain disorder and strain for a number of crystallographic directions. In general, we find that polymer grains exhibit paracrystalline disorder on the order of 2-6%, and small molecules <1%. We propose that this numerical representation of deviations from ideal crystalline order along with crystalline mobility (determined from device data fitting) and simulations is important for understanding crystalline transport and trapping in organic semiconductor thin films.

2:50 PM

H5, Probing Stress Effects in Single Crystal Organic Transistors by Scanning Kelvin Probe Microscopy: *Lucile Teague*[1]; Oana Jurchescu[2]; Curt Richter[3]; Sankar Subramanian[4]; John Anthony[4]; Thomas Jackson[5]; David Gundlach[3]; James Kushmerick[3]; [1]Savannah River National Laboratory; [2]Wake Forest University; [3]National Institute of Standards and Technology; [4]University of Kentucky; [5]The Pennsylvania State University

To date, scanning Kelvin probe microscopy (SKPM) has been utilized to correlate the relationship between film structure and charge transport in a number of organic thin-film transistor (OTFT) devices. This technique provides a direct measurement of the intrinsic charge transport in the active organic as well as providing a detailed view of charge injection at the source and drain contacts. For the work presented here, SKPM was used to simultaneously probe the potential distribution in electrically biased single crystal difluoro bis(triethylsilylethynyl) anthradithiophene (diF-TESADT) organic thin film transistors. DiF-TESADT is one of a number of organic materials being studied for potential use in organic based electronics,[1] and recent studies of diF-TESADT OTFTs have shown that charge mobilities on the order of 0.4 cm2/V•s can be achieved for spun-cast devices,[2] while charge mobilities of 6 cm2/V•s have been achieved for single crystal devices.[3] We will discuss our recent findings which suggest that significant changes in device performance can occur when the organic crystal is stressed over a timescale of a few minutes. More specifically, we will show SKPM data that reveal changes in potential drops at the contacts as a function of time. These results suggest that active organic material can become charged over a timescale of a few minutes, decreasing the current flow in the device from source to drain. [1] Gundlach, D. J.; Royer, J. E.; Park, S. K.; Subramanian, S.; Jurchescu, O. D.; Hamadani, B. H.; Moad, A. J.; Kline, R. J.; Teague, L. C.; Kirillov, O.; Richter, C. A.; Kushmerick, J. G.; Richter, L. J.; Parkin, S. R.; Jackson, T. N.; Anthony, J. E. Nature Mater. 2008, 7, 216-221. [2] Jurchescu, O. D.; Hamadani, B. H.; Xiong, H. D.; Park, S. K.; Subramanian, S.; Zimmerman, N. M.; Anthony, J. E.; Jackson, T. N.; Gundlach, D. J. Appl. Phys. Lett. 2008, 92, 132103. [3] Jurchescu, O. D.; Subramanian, S.; Kline, R. J.; Hudson, S. D.; Anthony, J. E.; Jackson, T. N.; Gundlach, D. J. Chem. Mater. 2008, 20, 6733-6737.

3:10 PM Break

3:30 PM Student

H6, Study on the Resistance of Stretchable Electrodes from Surface Morphology Aided by Computer Modeling: *Wenzhe Cao*[1]; Patrick Goerrn[1]; Oliver Graudejus[2]; Joyelle Jones[1]; Sigurd Wagner[1]; [1]Princeton University; [2]Arizona State University

Thin gold film electrodes on polydimethylsiloxane(PDMS) substrates can be reversibly stretched up to 80% without losing their electrical conductance. The resistance increases nearly linearly with increasing mechanical strain. With improving fabrication techniques the correlation between resistance and

strain has become more and more reproducible. Practical application requires a predictive model for this correlation, but no model exists that captures it. We describe a current percolation model that starts with the image analysis of scanning electron micrographs as the basis for the finite element modeling of the electrical potential distribution in the film.The samples are made by electron beam depositing 75nm thick gold films on PDMS and glass control substrates. The films on PDMS are patterned into 100µm wide and 5mm long electrodes. The baseline resistivity of the film is measured on the control sample.15µmx15µm fields of 8-bit grayscale SEM micrographs of the cracked gold film are processed for illumination correction and noise reduction and then converted to binary images–each pixel either representing conducting gold or non-conducting cracks. The potential distribution in the field is calculated from solving for each pixel Gauss's law under current conservation. From the calculated potential distribution we calculate the current density and the equivalent resistivity for each field selected from the SEM micrograph.We first studied unstrained electrodes. Their surface morphology was imaged by SEM and analyzed by the model we built. 15µmx15µm large fields of the micrograph are analyzed and averaged, resulting in a resistivity of $(3.05\pm0.14)x10^{-5}$Ohmcm. Applying this value to the 100µm wide and 5mm long electrode resulted in a simulated resistance of 211Ohms, which agrees well with the measured value of 215Ohms. Potential distribution maps of the 15µmx15µm fields show that the potential drops are most pronounced (i.e.,local resistances are highest) across cracks that are longer than 1µm, while they are small across smaller cracks. This indicates that cracks over 1µm in size contribute most to the excess resistance, above that of the gold film on glass.To study strained electrodes, samples were 1-D stretched to a precise strain value, and the resistance under strain was measured. Then the strained electrode was fixed by gluing it to a sample holder, and was imaged by SEM. As observed earlier, longer cracks formed with orientation mainly perpendicularly to the stretching direction. Locally some gold film also delaminates at the edge of cracks. Both crack lengthening (which is reversible)and film delamination contribute to the increase in resistance under strain. Applying the same approach as for the unstrained electrode above, the simulated resistance of an electrode strained by 15% is 834Ohms, again agreeing well with the measured resistance of 860Ohms. We will compare experiment with simulation, and describe our progress toward a predictive model.

3:50 PM Student

H7, Reverse Offset Roll Printing Using High Resolution Printing Plate for Electronic Application: *Nackbong Choi*[1]; Shahrukh A. Khan[1]; Jean Lavelle[2]; Jo Gallagher[2]; Mikhail Laksin[3]; Miltiadis Hatalis[1]; [1]Lehigh University; [2]CIRI, Northampton Community College; [3]IdeOn

Printed electronics is an emerging technology for large area electronics such as display, RFID, and flexible electronics to reduce manufacturing cost and improve throughput [1]. This research is focused on high resolution offset roll printing method to replace the expensive photolithography process which requires several steps to pattern one layer. This printing technique can also be used to directly print the soluble conductors and soluble semiconductor layer for all printed thin-film transistors (TFTs). The technique, championed by LG Display, was successfully used to demonstrate a 15" display where all etch resists were printed [2]. However, the versatility of this printing process can be further demonstrated by direct printing of soluble metals and semiconductors on flexible platform. In this work, we study reverse offset printing process and propose new method to form a high resolution printing plate. Employing this process, our work will encompass printing of high resolution electrode and devices. At first, we have focused on reverse offset printing method with particular emphasis given to blanket materials, printing plates and ink modification for fine print features. Blankets of this type of printing system require low surface energy, high hardness, smooth surface roughness, and uniform thickness. Instead of soft PDMS, silicone elastomer (methyl vinyl silicone) with high hardness is applied as blanket material. Etching methods such as wet etch, laser ablation, and dry etch are evaluated to pattern glass and Si wafers for realizing high resolution printing plate. Among these techniques, deep RIE shows good results having etch-profiles with deep and steep angles. To increase surface energy of plate, molybdenum with high surface energy is deposited on the surface of Si plate to easily take ink off of blanket with low surface energy. To print etch mask for replacement of photolithography, instead of developing new ink, commercial resist with 25% Novolak resin is modified by mixing high boiling point solvent to retard fast drying rate of ink. Finally very well defined patterns and line spaces of around 6um are achieved using this process. Using this verified process, we are in process of building TFTs where etch-resist is printed and metal layers are substituted by silver nanoparticles to achieve the small printed channel length. [1] Vivek Subramanian et al, Proceedings of IEEE, VOL. 93, No. 7, July 2005. [2] Youn Gyoung Chang et al, Journal of the SID 17/4 (2009), 301-307 (2009).

4:10 PM Student

H8, A Novel Hybrid Electrical and Chemical Barrier Material for Flexible Electronics: *Lin Han*[1]; Katherine Song[1]; Sigurd Wagner[1]; Prashant Mandlik[2]; [1]Princeton University; [2]Universal Display Corporation

Mechanical flexibility is attractive for many electronic applications, including flat-panel displays, electronic paper, medical X-ray sensor arrays, and photovoltaic modules. Making electronics flexible adds a new dimension to the design and utilization of electronic materials. Among the most important materials that need be made flexible is an optically clear insulator that can function as a gate dielectric and as an environmental permeation barrier. We introduced a new SiO2-silicone hybrid material that meets these functions. The hybrid consists of ~ 90% SiO2 and ~ 10% silicone polymer [1], which we deposit by plasma-enhanced chemical vapor deposition from a silicone monomer and excess oxygen on substrates at room temperature. Its electrical properties were evaluated on metal/~100 nm hybrid/p-type Si capacitors from measurements with an HP 4275A LCR meter and an HP 4155A parameter analyzer. The hybrid has a relative dielectric constant of 4.0, a leakage current of 0.08 □A/cm2 at an electrical field of 1 MV/cm, and a breakdown field of 8 MV/cm. To test its mechanical flexibility in a device, the hybrid was used the a gate dielectric in hydrogenated amorphous-silicon thin film transistors (a-Si: H TFTs). The TFTs can be bent to a tensile strain of up to 10 times of that of conventional a-Si:H / SiNx TFTs [2]. To test its permeability for atmospheric gases, we conducted accelerated tests at elevated temperature and humidity of hybrid encapsulated organic light-emitting diodes (OLEDs). At 65°C and 85% relative humidity, the water vapor transmission rate is at most 10^-6 g/m^2/ day [3]. Because the hybrid is deposited at room temperature from inexpensive sources, is mechanically flexible and electrically and chemically impermeable, it is a suitable material for flexible electronics. We report the dielectric properties of the hybrid, the electrical and mechanical performance of a-Si:H TFTs with the hybrid gate dielectric, and the permeability of the hybrid used as encapsulation for OLEDs.

4:30 PM Student

H9, Heavily Doped ZnO Thin Films for Hybrid Inorganic Organic Devices: Budhi Singh[1]; *Zaheer Khan*[1]; Subhasis Ghosh[1]; [1]Jawaharlal Nehru University, School of Physical Sciences

Organic solar cell (OSC) and organic light emitting diodes (OLEDs) require the use of conducting transparent electrode for allowing in and out of the active region of the devices. Transparent indium tin oxide (ITO) is the standard electrode used as anode in these devices. Besides cost, which is extremely critical for OSC, there are several problems. The most important is the control of the electrical and optical properties of ITO. Recently there is a serious search for alternate transparent electrode for organic devices. Moreover, there will be great demand of such material for future transparent electronics. In this case, in addition to transparent electrode, transparent n-type and p-type semiconductors will be required. In view of all these applications, heavily doped ZnO is being investigated with great interest. To be used as transparent conductive electrode in organic and transparent electronics, ZnO thin films have to be highly transparent in the visible and near infrared spectral range with a high electrical conductivity. Aluminum doped ZnO (AZO) could be suitable alternate to ITO for its low cost, low toxicity and excellent electrical and optical properties. We have grown 2% and 4% Al doped ZnO using RF sputtering on quartz substrate, with growth temperature varying from room temperature to 600°C. Sputtering targets were prepared by conventional solid-state reaction route. Commercially available ZnO (99.99%) and Al_2O_3 (99.99%) powders from Aldrich, were mixed in stoichiometric amount, grounded for 4hrs and finally sintered at 700°C for

10 hrs. Argon and oxygen mixture (6:4) were used as sputtering gases. All the grown films were polycrystalline, monophasic and highly c-axis oriented with no evidence of Aluminum impurity. Optical reflectance was more than 90% with not much variation in the optical bandgap. AFM and STM study showed that the film morphology was grainy and intergrain connectivity increased with increasing substrate temperature. The surface roughness was less than 2.3nm and the average grain size was ~ 145nm. It has been shown that desirable properties show nonmonotonic dependence on the growth temperature. Highest electron concentration of $3x10^{19}cm^{-3}$ with more than 90% transparency has been obtained in samples grown at 500°C. A hybrid p-n junction diode was fabricated by using p type organic semiconductor zinc phthalocyanine (ZnPc) and n type AZO with rectification ratio of 10^2. In this case bottom AZO layer grown at 500°C with resistivity of 60mOcm is used as electrode and the subsequent AZO layer grown at room temperature with resistivity of 1.7Ocm is used as active n-layer in the hybrid pn junction diode. The electrical properties of p-n junction improve remarkably with higher growth temperature of bottom AZO electrode.

4:50 PM
H10, Late News

Session I: Nanomagnetic and Spintronic Materials

Wednesday PM
June 23, 2010

Room: 129
Location: University of Notre Dame

Session Chairs: Xinyu Liu, University of Notre Dame; Roberto Myers, Ohio State University

1:30 PM
I1, An Organic-Based Magnetic/Nonmagnetic Semiconductor as a Spin Polarized Carrier Source/Channel: Moving Toward Organic Spintronics: *Jung-Woo Yoo*[1]; V. N. Prigodin[1]; Chia-Yi Chen[1]; H. W. Jang[2]; C. W. Bark[2]; C. B. Eom[2]; A. J. Epstein[1]; [1]The Ohio State University; [2]University of Wisconsin

Recent years witnessed increasing research for exploiting carbon-based materials as a spin transporting channel, which introduces a new avenue for device integration and functionality [1]. Molecule/organic-based magnets, that allow chemical tuning of electronic and magnetic properties, are a promising new class of magnetic materials for future spintronics [2,3]. The advantages of using organic-based magnets as spin polarizers in spintronic applications include, chemical tunability, highly spin-polarized electronic nature [4], low temperature processing, optical control of magnetism and conductivity [5], etc. V(TCNE:tetracyanoethylene)$_x$ ($x \sim 2$) is the earliest developed room temperature molecule-based magnet [6]. It has ferrimagnetic coupling between the spins in the TCNE π^* orbital and spins in V^{II} $d(t_{2g})$ orbital with $T_c \sim 400$ K. This material also can be grown as a thin film via low-temperature (40 °C) chemical vapor deposition (CVD) [7]. Besides its robust room temperature magnetic ordering, the V(TCNE)$_x$ has unique electronic structure, as a 'half-semiconductor' [4], i.e., fully spin polarized non-overlapping valence and conduction bands The highly spin polarized electronic state was observed by magnetic circular dichroism [8]. In this talk, we present realization of an organic-based magnetic/non-magnetic semiconductor as an electron spin polarizer/spin transporting layer in the standard spintronic device geometry [1,9]. The application of organic small molecule films as the spin transporting layer has been studied recently However, conceptual understanding of how the spins are injected into and transport through these organic semiconductor films was missing. With careful study on film thickness, temperature, and bias dependencies, significant differences between tunneling and giant magnetoresistance were resolved [1]. In addition, the room tempearture organic-based magnet, V(TCNE)$_x$ was successfully incorporated into the standard magnetic tunnel junction device [9]. Our results unambiguously demonstrates spin filtering of current passing through a V(TCNE)$_x$ magnetic semiconductor film, with sebsequent tunneling of the spin polarized carriers through a the hybrid rubrene/LAO barrier while effectively conserving spin polarization. A detailed discussion on temperature dependence and applied bias dependence will be presented. [1] Yoo et al., Phys. Rev. B 80, 205207 (2009). [2] Miller and Epstein, Angew. Chem. Int. Ed. Engl. 33, 385 (1994). [3] Epstein, MRS Bull. 28, 492 (2003). [4] Prigodin et al., Adv. Mater. 14 1230 (2002). [5] Yoo et al., Phys. Rev. Lett. 97 247205 (2006). [6] Manriquez et al., Science 252, 1415 (1991). [7] Pokhodnya et al., Adv. Mater. 12, 410 (2000) [8] Kortright et al., Phys. Rev. Lett. 100, 257204 (2008).[9] Yoo et al., submitted for the publication.

1:50 PM Student
I2, Effect of Perpendicular Magnetic Anisotropy on Emerging Magnetic Logic Devices: *Larkhoon Leem*[1]; James Harris[1]; [1]Stanford University

Perpendicular Magnetic Anisotropy (PMA) materials have attracted interest as a viable material for future scaling of magnetic/spintronic devices. Recently, a number of logic devices have been proposed in magnetics/spintronics domain as a replacement for highly scaled CMOS technology [1,2]. Although PMA materials have not been adopted in these emerging devices, it may be useful for the device scaling purposes. We investigate the applicability of PMA materials to emerging devices: Magnetic Quantum Cellular Automata (MQCA) and Magnetic Coupled Spin-Torque Devices (MCSTD), through micromagnetic simulations. First, in MQCAs, the moments in the nanomagnets are initialized to the hard axis and are required to remain in that state until signals arrive. Previous work [1] utilized crystalline anisotropy along the hard axis to enhance the biaxial anisotropy. We examine the possibility of using PMA materials to induce the biaxial anisotropy: elongated shape along the nanomagnet easy axis creates in-plane magnetization stable states while the metastable state is perpendicular to the nanomagnet surface. K1 values that are used in [1] along the hard-axis are induced in a perpendicular direction for comparison. From micromagnetic simulations [3], signal propagation was unsuccessful in PMA based MQCA: dual magnetic domains or magnetization vortices were observed to prevent signal propagations. Weak anti-ferromagnetic coupling among nanomagnets in PMA based MQCAs can be explained by small saturation magnetizations and lack of a boost for hard-axis stability as in [1], where all the moments from nanomagnets point along their hard axis. Finally, incrementally scaled down nanomagnet heights made the signal propagation successful in PMA based MQCAs. Secondly, PMA materials can lower the energy consumption of MCSTD due to their low switching current density. To examine the applicability of PMA, MCSTDs with circular and elliptical cross section are simulated. For the circular structures, the switching voltage modulation due to the fringing fields from the input MTJs [2], the key switching mechanism for MCSTDs, was not observed. This also results from the small saturation magnetization of PMA materials. In addition, the free layers are too thin to create enough anti-ferromagnetic coupling between the neighboring MTJs in the perpendicular direction. Next, elongated elliptical MTJs were used to induce in-plane stable states to utilize the stronger magnetic dipole coupling among MTJs. CoFe50 with a larger saturation magnetization was used as well. Now, switching voltage modulation is demonstrated as in the original MCSTD with a significant reduction in current densities. In conclusion, PMA materials can be integrated into emerging magnetic logic devices with additional considerations to compensate for the inherent small saturation magnetizations of PMA materials. [1] D.Carlton et al., Nano Letters, vol.8, no.12 (2008); [2] L. Leem, J. Harris, J. Appl. Phys. 105, 07D102 (2009); [3] M.J. Donahue, D.G. Porter, Interagency Report NISTIR 6376, NIST (1999).

2:10 PM Student
I3, Observation of Antiferromagnetic Interlayer Exchange Coupling in a GaMnAs/GaAs:Be/GaMnAs Tri-Layer: *Jonathan Leiner*[1]; Hakjoon Lee[2]; Taehee Yoo[2]; Sanghoon Lee[2]; Brian Kirby[3]; Xinyu Liu[3]; Jacek Furdyna[1]; Margaret Dobrowolska[1]; [1]University of Notre Dame; [2]Korea University; [3]National Institute of Standards and Technology

It has been long predicted theoretically that with the correct combination of layer thickness and carrier doping, antiferromagnetic interlayer exchange coupling should be sustainable between GaMnAs layers separated by non-magnetic spacer layers. However such AF coupling was not observed until very recently when Chung and co-workers used polarized neutron reflectometry (PNR) to unambiguously identify antiferromagnetic coupling in a superlattice structure of GaMnAs separated by GaAs:Be spacers [1]. This exciting finding

has spurred recent theoretical work by Szalowski and Balcerzak [2], who point out that the RKKY-like carrier mediated magnetic exchange should be different for a superlattice from that in a single trilayer of GaMnAs/GaAs:Be/GaMnAs, due to drastically different boundary conditions. In this vein, Ref. [2] suggests that the trilayer structure provides a simpler, more fundamental system for understanding the basic exchange mechanisms in GaMnAs. Thus, there is significant interest in understanding interlayer exchange coupling in the trilayer structure.A series of GaMnAs/GaAs:Be/GaMnAs trilayers with various thicknesses and dopings of the GaAs:Be spacers were fabricated by low-temperature molecular beam epitaxy in the hope of establishing conditions under which antiferromagnetic interlayer exchange coupling (IEC) between the GaMnAs layers can occur in such structures. After cooling a trilayer with a 5 nm spacer layer and 3×10^{20} cm^{-3} Be doping below the GaMnAs Curie temperature in zero field, we observe increased low-field magnetoresistance and suppressed low-field magnetization below 35 K – suggesting spontaneous antiparallel alignment of the GaMnAs layers. PNR measurements taken under similar conditions were used to directly measure the field dependent magnetic depth profile, and confirm robust antiferromagnetic coupling of the separated GaMnAs layers. This result is fundamentally interesting, as theoretical work suggests that a spacer layer as thick as 5 nm should be marginal at best for supporting any type of coupling in this system. Details of how coupling varies with spacer properties, and the role of crystalline anisotropy in our trilayer samples will be discussed. [1] J.-H. Chung, S. Chung, Sanghoon Lee, B. Kirby, J. Borchers, Y. Cho, X. Liu, and J. Furdyna, Physical Review Letters 101, 1-4 (2008). [2] K. Szalowski and T. Balcerzak, Physical Review B 79, 1-11 (2009).

2:30 PM

I4, Electrical Spin Injection in a Hybrid Organic/Inorganic Spin-Polarized Light Emitting Diode (Spin-LED): L. Fang[1]; D. Duman[1]; C.-Y. Chen[1]; P. Truitt[1]; A. Epstein[1]; *Ezekiel Johnston-Halperin*[1]; [1]Department of Physics, The Ohio State University

The success of solid state electronics over the past sixty years has both driven and been driven by an increasingly sophisticated understanding of the electronic properties condensed matter systems. The success of the emerging field of semiconductor spintronics will require a fundamental understanding of spin in condensed matter systems comparable to this understanding of charge transport. For example, the organic-based ferromagnet V[TCNE]x is a promising spintronic material due to its room temperature ferromagnetism, semiconducting bandstructure and predicted 100% spin polarization at the Fermi energy. Here we present a recent investigation into the use of V[TCNE]x as a spin injector in a hybrid organic/inorganic spin-light emitting diode (spin-LED) structure. In this study, we detect circular polarization of the electroluminescence (0.6% at 0.1 T and 60 K) that follows the magnetization curve of V[TCNE]x. Moreover we observe that the photoluminescence from a V[TCNE]x coated LED does not show significant magnetic circular dichroism, demonstrating the first successful transfer of spin from an organic-based material into an inorganic semiconductor.

2:50 PM

I5, Properties of MnAs/GaMnAs/MnAs Magnetic Multilayers and Their Application to High Temperature Vertical Spin Valves: *Debashish Basu*[1]; Hyun Kum[1]; Wei Guo[1]; Pallab Bhattacharya[1]; [1]University of Michigan

Epitaxially grown hybrid ferromagnet/semiconductor heterostructures are currently of interest due to their potential application in spintronics devices. Lateral spin valves and devices based on such spin valves have been demonstrated. More recently, vertical spin valves and transverse magnetoresistance devices (TMR) devices consisting of semiconductor/ferromagnet multilayers have been reported. However device operation has generally been restricted to very low temperatures. We have investigated the epitaxy and properties of MnAs/GaMnAs/MnAs magnetic multilayer heterostructures. Vertical spin valves/TMR devices using these heterostructures demonstrate large magnetoresistance upto T~200K. The magnetic multilayer heterostructure was grown by molecular beam epitaxy (MBE). A 35 nm layer of ferromagnetic MnAs was first grown on a GaAs substrate at 250°C. This layer was annealed in the presence of As flux at 350°C in order to reduce the surface roughness. Thin layers (1 nm each) of GaAs and AlAs were deposited on the MnAs layer at 250°C. This was followed by a 8 nm layer of Ga0.1Mn0.9As and 1 nm layers of AlAs and GaAs layers respectively. The purpose of growing thin layers of AlAs/GaAs was to prevent the segregation of Mn atoms in the GaMnAs layer due to the proximity of the MnAs interface. The top 35 nm ferromagnetic MnAs layer was left un-annealed. X-ray diffraction and TEM measurements done on this multilayer film indicate a high degree of crystallinity of the MnAs contacts and absence of Mn clusters in the Ga0.1Mn0.9As sandwich layer. Vertical spin valves were fabricated with these multilayer heterostructures using standard micro-fabrication techniques. The current-voltage characteristics, measured both in the presence and absence of external magnetic field indicate dependence of the resistance of the device on the direction of magnetization of the ferromagnetic pads. Asymmetric control devices with no MnAs top layer, fabricated and characterized under the same conditions, show no such dependence. Distinct peaks were observed at ~350 Oe in the magnetoresistance (MR) measurements done on the vertical spin valves. The position of the peak closely matches the values obtained from separate magneto-optic Kerr effect measurements done on the polarizer and the analyzer pads. A peak MR value of 42 % was observed at 10K at a bias current of ~ 1 nA. MR values of >12 % was measured at temperatures above 150K. The MR vs temperature characteristic, which is non-linear, is influenced by the GaMnAs sandwich layer which is ferromagnetic at temperatures below 100 K and paramagnetic above this temperature. The enhancement of the MR values is attributed to this property of GaMnAs and also to its high crystallinity. Similar effects have been previously observed in all metallic spin valves with ferromagnetic sandwich layers. The characterization of this novel multilayer system will be presented and discussed.Work supported by NSF and ONR

3:10 PM Break

3:30 PM Student

I6, The Magneto-Optic Kerr Effect (MOKE) as a Measure of Strain-Induced Ferromagnetism in $EuTiO_3$ Grown by Molecular-Beam Epitaxy: *Lei Fang*[1]; JuneHyuk Lee[2]; E. Vlahos[3]; X. Ke[3]; Y. W. Jung[1]; L. Fitting Kourkoutis[2]; P. Ryan[4]; J. W. Freeland[5]; T. Heeg[2]; M. Roeckerath[6]; V. Goian[7]; M. Bernhagen[8]; R. Uecker[8]; C. Hammel[1]; K. M. Rabe[9]; S. Kamba[7]; J. Schubert[6]; D. A. Muller[2]; C. J. Fennie[2]; V. Gopalan[3]; P. Schiffer[3]; D. Schlom[2]; Ezekiel Johnston-Halperin[1]; [1]The Ohio State University; [2]Cornell University; [3]Penn State University; [4]Ames Laboratory; [5]Argonne National Laboratory; [6]JARA-Fundamentals of Future Information Technologies, Research Centre; [7]Na Slovance 2; [8]Max-Born-Straße 2; [9]Rutgers University

Recently biaxial strain has been predicted to induce a multiferroic ground state in $EuTiO_3$ and change its normally paraelectric and antiferromagnetic ground state into a state that is simultaneously ferromagnetic and ferroelectric. This multiferroic state is predicted to be a strong ferromagnet and also a strong ferroelectric. To assess these predictions that would establish $EuTiO_3$ as the world's strongest ferromagnetic ferroelectric, epitaxial $EuTiO_3$ thin films are grown on (001) $SrTiO_3$,(001) $(LaAlO_3)0.29$—$(SrAl1/2Ta1/2O_3)0.71$ (LSAT) and (110) $DyScO_3$ substrates by reactive molecular-beam epitaxy (MBE). Testing for ferromagnetism in the strained $EuTiO_3$ films is complicated by the large paramagnetic response of the $DyScO_3$ substrate. If a superconducting quantum interference device (SQUID) magnetometer is used under typical measurement magnetic fields, the paramagnetic response of the thick substrate swamps the signal from the strained $EuTiO_3$ film. For this reason magneto-optic Kerr effect (MOKE) is used to measure the magnetization of the strained films. Longitudinal continuous-wave (CW) MOKE geometry is used to measure the in-plane magnetization in a spectral window (690 nm to 750 nm) that is sensitive to the $EuTiO_3$ epilayer but not the $DyScO_3$ substrate. The MOKE response from the strained $EuTiO_3$ film exhibits a clear ferromagnetic hysterisis loop, with sharp switching to full saturation. The temperature dependence reveals a Curie temperature (TC) of 4.3 K. In comparison, unstrained $EuTiO_3$ films grown on $SrTiO_3$ and LSAT substrates were also measured and no ferromagnetic feature was observed for the control samples at all temperatures. Optical second harmonic generation (SHG) reveals that the unstrained $EuTiO_3$ films are not polar, as expected, but that the strained $EuTiO_3$/$DyScO_3$ passes through a phase transition at about 250 K to polar point group mm2, in agreement with theory,

and in this state domain switching by electric fields is observed. Our results thus establish that strain induces a strong multiferroic state in $EuTiO_3$ in agreement with predictions.

3:50 PM Student

I7, Magnetic Circular Dichroism (MCD) Studies on GaMnAs: *Kritsanu Tivakornsasithorn*[1]; Xinyu Liu[1]; M. Berciu[2]; J. Furdyna[1]; M. Dobrowolska[1]; [1]University of Notre Dame; [2]University of British Columbia

Current interest in spin-based electronics has generated a demand for materials in which magnetic properties occur simultaneously with a strong spin-dependent response of charge carriers. In this connection III-Mn-V ferromagnetic semiconductors – and GaMnAs in particular – continue to attract attention. Although there is general consensus that the ferromagnetic coupling between Mn spins in GaMnAs is mediated by holes contributed by Mn ions, the nature of the hole wavefunctions as well as the their location (valence band vs. an impurity band located at about 110 meV above the top of the valence band) is one of the most controversial topics in this field. There are many theoretical models discussed in the literature, but as yet there is no conclusive experimental result that can definitively resolve this issue. In order to address this controversy, we studied MCD on a series of $Ga_{1-x}Mn_xAs$ layers grown by MBE, with x ranging from 0.02 to 0.06. As was shown by Berciu et al [1], the MCD signal in GaMnAs arises primarily from a difference in the density of spin-up and spin-down states in the valence band brought about by the presence of the Mn impurity band. In particular, MCD spectra, for an as-grown and an annealed sample with x = 0.06, show the same general features as those observed on samples with Mn concentration ~0.01 reported in [1]. Specifically, the signal rises sharply in the vicinity of the energy gap and forms a very broad spectrum with two (as grown) or three (annealed sample) distinct peaks. The peaks correspond to the maximum contribution to the IB from the heavy hole (lower energy peak) and light hole (higher energy peak) bands. In the annealed sample the contribution from the Γ7 band is also clearly visible. In contrast, the spectra taken on $Ga_{0.98}Mn_{0.02}As$ samples co-doped with Be reveal that the MCD signal disappears in the vicinity of the energy gap for samples with Be concentration higher than 1×10^{20} cm^{-3}. In the case of Be-doped samples the Fermi level lies in the valence band, and consequently interband transitions at the band gap disappear. By contrast, the strong MCD signal observed at the band gap in undoped GaMnAs samples indicates a difference in the density of spin-up and spin-down states at the top of the valence band, and consequently points to the fact that the Fermi level must lie in the impurity band. [1] M. Berciu et al., Phys. Rev. Lett. 102, 247202 (2009).

4:10 PM Student

I8, Magneto-Optical Spectroscopy of MOVPE Grown Ferromagnetic Semiconductors: Giti Khodaparast[1]; *Mithun M. Bhowmick*[1]; Matthew Frazier[1]; Bruce Wessels[2]; Yasuhiro Matsuda[3]; [1]Virginia Tech; [2]Northwestern University; [3]University of Tokyo

The origin of ferromagnetism, which is apparently induced by free holes, has been an open question. Several models have been proposed; however, currently, there is no single theory that can provide an accurate prediction for Tc in different III-V DMSs for different carrier density regimes. The case for ferromagnetic semiconductor such as InMnAs, grown by MOVPE, is even more complex. Films with a carrier concentration of 1018 cm-3 have Tc of 330 K and the Tc is nearly independent of carrier concentration. Recently, the magnetoresistance of InMnAs/InAs p-n heterojunctions for magnetic fields of up to 18 T has been measured. At 300 K, giant magnetoresistance effects (2680 %) at 18 T were observed. A crucial factor in the design of any spin-sensitive device, on the basis of ferromagnetic semiconductor structures, is the electron-spin-relaxation time (T1) which must be reasonably long to allow for transport and processing of the spins. Most of the understanding of the spin relaxation in narrow gap (III,Mn)V ferromagnetic structures has been on the basis of the two color magneto-optical Kerr (MOKE) time-domain spectroscopy. The approach in this work was focused on the time and polarization-resolved differential transmission (PRDT) as well as the MOKE measurements. In the PRDT measurements, optically-injected, spin-polarized electrons were created/probed close to the fundamental gap of the ferromagnetic films, using circularly polarized pulses in the mid-infrared. The optical polarization is decaying exponentially with a decay constant related to the spin lifetime. Our PRDT observation suggested a spin relaxation of ~ 1ps at 290 K in an InMnAs film with 4% Mn content, consistent with our MOKE measurements. The Carrier dynamics demonstrated several relaxation regimes, strongly influenced by the initial pumping wavelength. Lowering the samples temperature to 77 K didn't change the carrier and spin relaxations time significantly. In addition, to understand the nature of the carrier states in the valence band of the ferromagnetic samples, high magnetic field cyclotron resonance (CR) measurements at 290 K and 7 K were performed. CR is a direct and accurate method for determining the effective mass and therefore the energy dispersion of carriers. We compare our results with reported studies in MBE grown InMnAs and InMnSb. Supported by: NSF-DMR-0507866, AFOSR Young Investigator Program 06NE231, NSF-Career Award DMR-0846834, NSF DMR 0804479.

4:30 PM

I9, Micromagnetic Simulation of Focused Ion Beam Patterned Cobalt-Platinum Multilayers: Xueming Ju[1]; Stephanie Wartenburg[1]; Markus Becherer[1]; Doris Schmitt-Landsiedel[1]; Paolo Lugli[1]; Wolfgang Porod[1]; *Gyorgy Csaba*[2]; [1]Technical University of Munich; [2]University of Notre Dame

This work introduces a computational micromagnetic model of Focused Ion Beam (FIB) irradiated Co/Pt multilayers and shows how FIB irradiation can be used to engineer field-coupled devices made from Co/Pt multilayers. Irradiation locally changes the magnetic properties of Co/Pt layer stacks and can be used as a one-step tool for defining magnetic nanostructures. High irradiation dose renders the material non-magnetic or paramagnetic, while a lower dose locally reduces anisotropy, exchange and saturation magnetization. We implemented the model of inhomogenously irradiated Co/Pt nanomagnets in a standard micromagnetic simulation software, OOMMF [1]. Using our simulation tool we show how FIB irradiation enables the definition of nucleation sites on a nanomagnet. This changes the reversal mode of the magnet – FIB-defined dots start switching from the side that received the highest dose [2]. Additionally, irradiation changes the strength of the magnetic dipole coupling between neighboring nanomagnets. For example, a nanomagnet partially irradiated at its left side shows a stronger coupling to its left neighbor than to the right one. We show how partial irradiation can be exploited in the design of field-coupled magnetic computing devices. In magnetic field coupling, information is represented by the magnetic orientation of single-domain nanomagnets and the magnetic signal is propagated and processed by their field-interactions [3]. Operation of the device requires precise control over the magnetic ordering. This is difficult to achieve [4], since field-interactions are reciprocal – the magnets jointly interact with all their neighbors so the direction of signal flow is not defined. Asymmetric irradiation of a nanomagnets can lead to non-reciprocal signal propagation and perfectly controlled, frustration-free ordering. Even large field-coupled structures can be demagnetized (put in their computational ground state) with a homogenous external field. We will show how shift registers and logic gates can be constructed from asymmetrically irradiated dots. [1] http://math.nist.gov/oommf/; [2] M. Becherer, J. Kiermaier, G. Csaba, J. Rezgani, C. Yilmaz, P. Osswald, P. Lugli, D. Schmitt-Landsiedel: Characterizing magnetic field-coupled computing devices by the Extraordinary Hall-effect presented at ESSDERC, Athens Sept 14-18 2000; [3] A. Imre, G. Csaba, L. Ji, A. Orlov, G. H. Bernstein, and W. Porod : Majority Logic Gate for Magnetic Quantum-Dot Cellular Automata Science 311 (5758), 205 (2006); [4] M. Becherer, G. Csaba, W. Porod, R. Emling, P. Lugli, D. Schmitt-Landsiedel,: Magnetic Ordering of Focused-Ion-Beam Structured Cobalt-Platinum Dots for Field-Coupled Computing IEEE Transactions on Nanotechnology, vol.7, no.3, pp.316-320, May 2008.

4:50 PM Student

I10, Growth and Characterization of $In_{1-x}Mn_xSb$ Ferromagnetic Semiconductor Alloys Using Metal Organic Vapor Phase Epitaxy (MOVPE): *Caitlin Feeser*[1]; John Peters[1]; Nidhi Parashar[1]; Bruce Wessels[1]; [1]Northwestern University

Dilute (III,Mn)V magnetic semiconductors have attracted interest for their potential applications in semiconductor based spintronic devices. Currently,

a major challenge in developing these materials is attaining a high Curie temperature for room temperature operation. Recent success in synthesizing phase pure ferromagnetic InMnAs (Tc of 330 K) and InMnSb (Tc of 590 K) films using MOVPE demonstrates that narrow-gap semiconductors are suitable for these devices. In this study, we focus on the In1-xMnxSb system and the role of Mn concentration in stabilizing the ferromagnetism. The InMnSb films are deposited on semi-insulating GaAs (100) substrate using atmospheric pressure metalorganic vapor phase epitaxy. Film growth involves trimethyl indium, trimethyl antimony, and bis(methylcyclopentadienyl) manganese precursors in a palladium-purified hydrogen carrier gas. Film growth has been studied between 400 and 440°C with Mn concentration ranging from x=0 to x=0.12, and over a range of III/V ratios. The typical film thickness ranges from 200 - 250 nm. For structural characterization, double crystal x-ray diffractometer (XRD) measurements with Cu-K\945:1 radiation are used to determine the phase diagram. For x < 0.05 the films are phase pure. For x > 0.05 the films show peaks at the (101) and (102) attributed to MnSb reflections. Mn concentration in the films is determined using the electron dispersive spectroscopy and has been found to increase with increasing growth temperature for a given III/V ratio. Crystallization of antimony to form surface droplets is observed in SEM for low III/V ratios. An increase in the surface roughness is observed with an increase in Mn content and subsequent formation of a second phase. Average root mean square surface roughness was 25 nm for these films. Field and temperature dependent magnetization were measured using a SQUID magnetometer. Irreversibility occurs when a ferromagnetic second phase is present. Both phase pure and two phase films show ferromagnetism with Tc greater than 350 K.

Session J: Thin Film Photovoltaics

Wednesday PM
June 23, 2010

Room: 131
Location: University of Notre Dame

Session Chairs: Steven Ringel, Ohio State University; Christian Wetzel, Rensselaer Polytechnic Institute

1:30 PM

J1, MBE Growth of Metamorphic InGaP on GaAs and GaP for Wide-Bandgap Photovoltaic Junctions: *John Simon*[1]; Stephanie Tomasulo[1]; Paul Simmonds[1]; Minjoo Lee[1]; [1]Yale University

Recently, multijunction solar cells have reached efficiencies of 41.1% by combining light absorbing materials with different lattice constants*. To achieve efficiencies above 50%, additional junctions may be needed, requiring the development of a wide bandgap (2-2.2eV) material to act as the top layer. In this work we demonstrate wide bandgap $In_yGa_{1-y}P$ grown on $GaAs_xP_{1-x}$ via solid source molecular beam epitaxy (SSMBE). Unoptimized $GaAs_xP_{1-x}$ buffers grown on GaAs exhibited asymmetric strain relaxation, along with formation of faceted defects (FDs) ~200 nm deep in the [01-1] direction. The density of the FDs was greatly reduced by lowering the grading rate, implying that their formation is related to the strain relaxation process. Strain relaxation increased from ~55% to ~85% for the cap layer by increasing the growth temperature from 580 to 700°C. Surface RMS roughness as low as 2.45 nm across a 30x30 μm^2 area was measured by AFM on buffers graded to x=0.8 while a threading dislocation density (TDD) of $7.5x10^5 cm^{-2}$ was measured by plan-view transmission electron microscopy (PVTEM). Graded buffers with x<0.7 had elevated FD densities that could not be reduced by slower grading. Cross-sectional TEM (XTEM) studies of the graded buffers showed evidence of dislocation pileups below the FDs, as well as formation of micro-cracks along [011] in buffers with x<0.7. Graded $GaAs_xP_{1-x}$ buffers on GaP showed symmetric and nearly-complete strain relaxation of the top layers when grown at substrate temperatures of 580°C. Surface RMS roughness of ~3.56 nm across a 15x15 μm^2 area was measured on buffers graded to x~0.7. No FDs or micro-cracks were observed in these buffers. A TDD of $3.2\text{-}7.5x10^6 cm^{-2}$ was obtained by PVTEM on $GaAs_{0.68}P_{0.32}$. $In_{0.29}Ga_{0.71}P$ layers were subsequently grown at 460°C on $GaAs_{0.6}P_{0.4}$ buffers on GaP. Intense room temperature photoluminescence at 2.16eV agrees with the composition extracted from x-ray measurements, implying a lack of CuPt ordering. Similar surface morphology and roughness as the underlying buffer were obtained. A smooth, coherent interface between the $GaAs_xP_{1-x}$ and $In_yGa_{1-y}P$ was observed by XTEM, with no evidence of phase separation, while selected area diffraction along [011] confirmed the lack of CuPt-B ordering. The low TDD, lack of ordering, and lack of phase separation in these $In_yGa_{1-y}P$ layers show that they are promising candidates for use as the top junction of a future multijunction cell. *Guter, et al, *Appl Phys Lett*, 94(22), 223504 (2009).

1:50 PM Student

J2, $In_xGa_{1-x}As$ Metamorphic Buffer Layers for Lattice Mismatched Multi-Junction Solar Cells: *Peter Dudley*[1]; Jeremy Kirch[1]; Toby Garrod[1]; Sangho Kim[1]; Luke Mawst[1]; Katie Radavich[1]; Steven Ruder[1]; Thomas Kuech[1]; Sabarni Palit[2]; Nam Jokerst[2]; [1]University of Wisconsin; [2]Duke University

In triple junction III-V solar cells, the use of a 0.95–1.05eV third junction is necessary to improve efficiency1. A common method for growing low defect density 1.0eV bandgap GaInAs on GaAs is to employ a graded Metamorphic Buffer Layer (MBL), which confines the defects. Recently, Wanlass and colleagues at NREL2 have produced a 38.9% efficient (81 suns) inverted triple junction cell, in which a $Ga_xIn_{1-x}P$ MBL is employed to allow for a 1.0eV In0.30Ga0.70As final junction3. While such devices are quite promising, the introduction of many dislocations into the solar cell structure, within the MBL, could impact the long-term reliability of the solar cell, especially when a concentrator is used. In addition, the surface morphology of MBL structures generally exhibit cross-hatching along the orthogonal (110) directions. We are investigating the MOVPE growth of $In_xGa_{1-x}As$ MBL structures with a focus on techniques to improve the surface morphology, optimize the lattice-matching of layers grown on top of the MBL, and lift-off devices which incorporate said layers. One method to improve the surface roughness of the MBL is through the use of Chemical-Mechanical Polishing (CMP). Preliminary results of the CMP process, showing improved surface morphology, are indicated by optical microscope images of the $In_xGa_{1-x}As$ MBL before and after CMP. Since accurate determination of the strain for layers grown on top of the MBL via off-axis XRD measurements has proven difficult, we adopted a trial and error method to optimize material quality. By varying the In composition of bulk InGaAs layers grown on top of the MBL and measuring the FWHM of the layer peak via XRD, we find that the compositional range giving the lowest FWHM can be considered to be lattice-matched. We also show the results of an initial investigation wherein we released an InGaAs QW PL structure from the underlying MBL and substrate, after bonding the thin film to a new carrier substrate. This structure utilized a sacrificial InGaP layer grown between the MBL and PL structure and selective chemical etching is utilized to lift-off the InGaAs QW test structure. Both the as-grown and lifted-off samples displayed room-temperature photoluminescence, though the QW PL intensity was reduced by a factor of four after lift-off. Future studies will focus on the growth and lift-off of 1eV solar cell devices from the MBL and implementation of the CMP process to improve surface morphology.

2:10 PM Student

J3, Quantum Dot n-i-p-i Photovoltaic Devices: *Michael Slocum*[1]; Steven Polly[1]; Chelsea Plourde[1]; Christopher Bailey[1]; Jeremiah McNatt[2]; Sheila Bailey[2]; Cory Cress[3]; David Forbes[1]; Seth Hubbard[1]; [1]Rochester Institute of Technology; [2]NASA-Glenn Research Center; [3]Naval Research Laboratory, Solid State Devices Branch

State of the art space solar cells utilize epitaxially grown III-V multijunction cells, with champion devices exceeding 30% conversion efficiency under 1-sun AM0 illumination. The ultimate efficiency is limited by the dual constraints of current matching in the series stack and lattice matching within the epitaxial structure to eliminate structural defects. This paper will focus on a novel approach of combining the benefits of an intermediate band solar cell (IBSC) with a device that depends almost exclusively on drift rather than diffusion currents to collect the carriers. A quantum dot nipi (QD-nipi) architecture consisting of repeating n-i-p-i epitaxial layers has been proposed to increase the radiation hardness of a device due to a decreased dependence upon diffusion length. This architecture will allow photo generated carriers to be rapidly

converted to majority carriers by drift, and conducted laterally through selective contacts positioned at opposite sides of etched V-groove channels in the device. Enhanced spectral conversion can occur by simultaneously adding QD to the stack. Demonstration of the QD-nipi configuration in a GaAs photovoltaic cell presents several challenges to device design and epitaxial growth. This paper will describe progress in addressing the two main challenges of creating selective ohmic contacts and determining the electric field profile. Results will be presented from epitaxial regrowth of GaAs within etched V-groove channels, concentrating on structural and electrical characteristics.

2:30 PM

J4, Characterization of a *p-i-n* Photovoltaic Cell Containing InAs/GaAs Quantum Dots: *Andrey Semichaevsky*[1]; Harley Johnson[1]; Simon Huang[2]; Rachel Goldman[2]; [1]UIUC; [2]University of Michigan

Improved external quantum efficiencies (EQE) of quantum dot (QD) intermediate band solar cells (IBSC) have been predicted theoretically[1] , and the increased photocurrent densities from solar cells with QD superlattices (SL) have also been demonstrated experimentally[2,3]. Design of QD solar cells requires a thorough understanding of the mechanisms responsible for the absorption of photons below the bulk semiconductor bandgap as well as for the charge carrier dynamics. In the present work, the spectral efficiencies of a *p-i-n* structure with InAs quantum dots (QD) in an intrinsic GaAs barrier are characterized both theoretically and experimentally for potential applications in photovoltaic solar cells. All structures are grown on Zn-doped *p*-GaAs (001) substrates by molecular beam epitaxy, using solid Ga, Be, Si, Al, In, and As sources. An initial Be-doped *p*-GaAs, a GaAs buffer layer, and a GaAs layer are grown, followed by three layers of the InAs/GaAs QD SL (2.6 monolayers of InAs and 5 nm GaAs spacer). For the QD *p-i-n* structure, the final QD layer is capped with 500 nm semi-insulating GaAs. Layers of *n*-GaAs, $Al_{0.3}Ga_{0.7}As$, and heavily doped n-GaAs are added. For the control *p-i-n* cell, QD layers are replaced with a 15 nm GaAs layer. A finite-element model of the single-particle Schrödinger-Poisson equations[4] in oblate spheroidal coordinate basis is used to predict the QD SL minibands and absorption spectra. The confinement potentials are found for the hydrostatic lattice mismatch strain [4], and the QD dimensions come from AFM and XSTM characterization. Calculated SL absorption spectra are then used in a macroscopic carrier transport model (carrier photogeneration and recombination, drift and diffusion currents, quantum transport in the QD SL) to determine the photocurrent density. The photogeneration and recombination rates in our model are material composition- and spatially dependent. Increased photocurrent density due to the QD SL at wavelengths above the absorption edge of bulk GaAs (870 nm) is observed in both our theoretical and experimental results. Predicted and measured spectral EQEs are in reasonable agreement, although, if quantum transport effects in the QD SL (carrier trapping and Auger recombination in QDs) are not included, predicted photocurrent densities exceed those measured experimentally. The spectral efficiency of the QD solar cell is also found to be strongly affected by QD size and by the quantum mechanical coupling between SL layers. [1] A. Luque and A. Marti, Phys. Rev. Lett. 78, 5014 (1997). [2] A. Luque, A. Marti, C. Stanley, N. Lopez, L. Cuadra, D. Zhou, J. L. Pearson, and A. McKee, J. Appl. Phys. 96, 903 (2004). [3] C.O. McPheeters, C.J. Hill, S.H. Lim, D. Derkacs, D.Z. Ting, and E.T. Yu, Journal of Applied Physics 106, 056101 (2009). [4] J.H. Davies, The Physics of Low-dimensional Semiconductors: an Introduction (Cambridge University Press, 1998), 438 pp.

2:50 PM

J5, MBE Growth of Lattice-Matched 6.1Å II-VI on GaSb Substrates: *Xinyu Liu*[1]; D. Ding[2]; S. Wang[2]; S.-N. Wu[2]; X. Zhang[2]; J. Fan[2]; J.-J. Liu[2]; X. Lu[2]; S. Johnson[2]; D. Smith[2]; J. Furdyna[1]; Y.-H. Zhang[2]; [1]University of Notre Dame; [2]Arizona State University

Monolithic integration of lattice-matched II-VI (MgZnCd)(SeTe) and III-V (AlGaIn)(AsSb) semiconductors on 6.1 Å substrates such as GaSb and InAs provides a novel approach for ultra-high efficiency multijunction (MJ) solar cells. These materials have direct bandgaps, covering the entire solar spectrum from 3.0 eV to 0.4 eV. The simulation of a practical four-junction solar cell based on the constituent II-VI materials show that the achievable energy conversion efficiency is 40% under 1 sun and 47% under 1000 suns. It is shown that high quality II-VI materials such as undoped ZnTe and ZnCdTe grown on GaSb substrates can be achieved. Excellent material structural, interfacial, and optical properties are revealed using post-growth characterizations including X-ray diffraction (XRD), transmission electron microscopy (TEM), and photoluminescence (PL). Moreover, we have extensively investigated short-period superlattices (SSLs) of CdSe and CdTe digital alloys grown using ZnTe buffer layers on GaSb or InAs substrates. High-resolution transmission electron micrographs showed that the CdSe-CdTe SSL had very high quality for approximately 25–50 periods closest to the substrate but that considerable stacking faults and microtwins were visible in layers near the top surface of the sample. In addition, we also successfully fabricated single-junction II-VI semiconductor heterostructure solar cells consisting of n-type CdSe and p-type ZnTe grown on GaSb substrates. The current-voltage measurements reveal expected diode-like rectifying characteristics with considerable photo current and strong photovoltaic effects under light illumination, indicating that the idea of using monolithic integration of lattice-matched II-VI and III-V semiconductors on GaSb is indeed very promising for ultra-high efficiency multijunction solar cells.It is important to note that the interfaces between II-VI and III-V materials have some very interesting properties that are yet not been thoroughly investigated. Since the constituent elements of the II-VI and III-V materials have been proven to be dopants for each other, novel devices such as tunnel junctions could be invented by taking advantage of well-controlled interdiffusion of different elements across the interfaces to create heavily doped regions near the interface. Moreover, the type-II band edge alignment between certain II-VI and III-V materials may further help to improve the performance of tunnel junctions. This paper reports our recent study of a set of carefully designed ZnTe/GaSb samples with various interface growth conditions and the re-growth of GaSb epilayers on ZnTe buffer layers. A typical sample structure of the latter consists of a 300 nm GaSb grown on ZnTe buffer layer with various thicknesses. The impact of ZnTe buffer layer thickness on the morphological and structural properties of the top GaSb epilayers has been investigated. Two-dimensional growth of GaSb epilayers is quickly obtained after the deposition of 1-2 nm GaSb on Zn-terminated surface. XRD and HRTEM measurements of these samples will be reported at the conference.

3:10 PM Break

3:30 PM

J6, ZnO/ZnTeO/ZnTe Heterojunctions for Intermediate State Solar Cells: *Weiming Wang*[1]; Jamie Phillips[1]; [1]The University of Michigan

A single junction solar cell with intermediate electronic states can extend the absorption spectrum by a multi-photon process without sacrificing the open-circuit voltage, where conversion efficiency as high as a triple junction cell may be possible [1]. ZnTeO has been used to demonstrate intermediate state/band solar cells using OTe substitutional impurities with resulting intermediate states at approximately 0.4eV-0.7eV below the conduction band edge and optical absorption coefficient of approximately $10^4 cm^{-1}$[2]. Initially, ZnTeO solar cell devices have been implemented in a p-ZnTe/ZnTeO/n-GaAs structure since it is difficult to achieve n-type ZnTe. Extended optical response at longer wavelength and sub-bandgap photocurrent response have demonstrated absorption via the multi-photon process [3]. However, the device performance is severely limited by non-ideal material properties and parasitic device parameters including high dislocation density due to the ZnTe/GaAs lattice mismatch and cross doping at the ZnTe/GaAs II-VI/III-V electrical junction. In this work, n-ZnO is proposed as an alternative heterojunction material for ZnTeO-based solar cells. While ZnO appears to be an attractive candidate due to its potential role as a wide-bandgap window layer with low resistivity and chemical compatibility with ZnTeO, there are challenges associated with the differing crystal structure of ZnO (wurtzite) and ZnTe (zincblend). The growth, structural properties, and electrical characteristics of ZnO/ZnTe heterojunctions will be presented. Improved diode ideality factor is observed for the ZnO/ZnTe diodes (n<2) in comparison to ZnTe/GaAs (n>3). However, reverse saturation current for these devices remains high, likely due to the differing crystal structures. In order to improve these characteristics, intermediate n-ZnSe (zincblend) buffer layers have been incorporated to reduce leakage current and improve photovoltaic

response for diodes with ZnTe-based absorber layers. [1]A. Luque, A. Marti, "Increasing the Efficiency of Ideal Solar Cells by Photon Induced Transitions at Intermediate Levels"Phys. Rev. Lett. 78, 5014 (1997); [2] W. Wang, W. Bowen, S. Spanninga, S. Lin and J. Phillips, "Optical characteristics of ZnTeO thin films synthesized by pulsed laser deposition and molecular beam epitaxy", Journal of Electrical Material , v 38, n 1, p 119, January 2009; [3] W. Wang, A. Lin, J. Phillips, "Intermediate band photovoltaic solar cell based on ZnTeO", Applied Physics Letter, v. 95, 011103 July 2009.

3:50 PM Student

J7, Copper Zinc Tin Sulfide Solar Cell Development by RF Sputtering from Binary Targets: *Jeffrey Johnson*[1]; Ashish Bhatia[1]; Haritha Nukala[1]; Win Maw Hlaing Oo[1]; Liz Lund[1]; Mike Scarpulla[1]; Loren Reith[1]; [1]University of Utah

Here we report on our research on the deposition an characterization of Cu2ZnSnS4 (CZTS) thin films by RF sputtering from a single CZTS target and by co-sputtering from multiple binary targets on Mo-coated glass. Grain size versus substrate versus temperature was evaluated by XRD, EBSD and AFM. Attempts to detect and identify defect levels via electrical impedance measurements and photoacoustic measurements will be discussed as well as optical transmission, resistivity and Hall effect and photoconductivity. To evaluate the electrical characteristics using the follow full cell stack molybdenum back contact, CZTS absorber layer, CdS/ZnS window layer and ZnO:Al buffer layer to measure IV curves from various light and dark condition.

4:10 PM Student

J8, Chemical Vapor Deposition of $CsSnI_3$ Thin Films for Photovoltaic Applications: *Nicholas LiCausi*[1]; Sunil Rao[1]; Ishwara Bhat[1]; Jim Wang[2]; Nemanja Vockic[2]; Matt Pfenninger[2]; John Kenney[2]; Zhuo Chen[3]; Kai Shum[3]; [1]Rensselaer Polytechnic Institute; [2]OmniPV Inc.; [3]The City University of New York

In order to lower cost of solar cells, there is a push to make high-efficient thin film solar cells which are grown on non-crystalline substrates such as glass. However, films grown on glass are typically polycrystalline or amorphous and usually have low efficiency due to defects, grain-boundaries, etc. Another alternative method to reduce cost is to use a thin film that can absorb the solar radiation broadly and reemit the energy at a narrow wavelength band suitable for absorption by silicon solar cells. For this to be cost effective, the luminescence conversion efficiency should be very high. We have explored the use of a new class of materials, namely perovskite semiconductor $CsSnI_3$ thin films, for this purpose that luminescence at 950nm. This film has exhibited high photoluminescence conversion efficiency and shows potential for use as a "spectral down converter" in photovoltaic applications. $CsSnI_3$ films have been grown on glass substrates in a low pressure chemical vapor deposition (CVD) reactor using cesium formate (CF), tetramethyl-tin (TET), and ethyl-iodide (EI) as the cesium, tin and iodine precursors, respectively. Both TET and EI are liquids at room temperature with sufficiently high vapor pressures and hence these could be transported to the reaction zone using standard carrier gas bubbling method. However, CF is a solid with relatively low vapor pressure and transport to the reaction zone was challenging. To evaluate whether growth by this method is possible, we used two primary methods. In the first method, cesium formate is dissolved in methanol. The glass substrate is then dipped in this solution and subsequently dried on a hotplate at 80°C. This creates a film varying in thickness from ~20-100 µm. The substrate is then loaded into the CVD chamber and heated to the growth temperature. Reaction to get $CsSnI_3$ was accomplished by passing TET and EI precursors using hydrogen as the carrier gas. Growth proceeds for 30-40 minutes and the sample is cooled under H_2 flow. The films are characterized by photoluminescence (PL) as well as scanning electron microscopy, energy dispersive x-ray analysis and x-ray fluorescence.In the second method, CF is first transported to the wafer by passing nitrogen over CF kept in a heated crucible, followed by passing TET and EI using hydrogen as the carrier gas. The second method resulted in more uniform film compared to the first method, but the overall thickness of the films is much lower. Growth temperatures of 300 – 600°C have been explored with the best PL efficiency obtained at 475°C. Further studies on the growth and film characterization will be carried out and the results will be reported at the conference. This is the first report of $CsSnI_3$ growth by the CVD method.

4:30 PM Student

J9, Exploring More Effective Catalysts for Metal-Induced Growth of Thin Film Si: *Peter Mersich*[1]; Wayne Anderson[1]; [1]University at Buffalo

Thin film microcrystalline Si (µc-Si) is an attractive material due to improved optical absorption compared to single crystal Si, as well as, increased mobility when compared to amorphous Si (a-Si). Producing high quality µc-Si at an affordable price is a particular challenge. Metal-induced growth (MIG) is a method of producing thin film µc-Si at temperatures of 625 °C and below. Similar to metal-induced crystallization, MIG has the advantage of depositing and crystallizing Si in a single step, while simultaneously forming an ohmic back contact. While MIG with a Ni catalyst has typically yielded good results, the process does not occur below 575 °C. Al and Cu offer significantly reduced crystallization temperatures, and consequently, lower cost. The mechanism by which crystallization occurs differs depending on the metal properties. Metals like Ni and Cu initially form a silicide compound. With Ni, this silicide precipitates through the Si and crystallizes it by the diffusion of Ni and Si atoms. Since Cu forms a metal-rich silicide, this compound does not precipitate and instead provides enough latent heat to activate the phase transition to crystallized Si. Al does not form a silicide. Instead, Si atoms diffuse into the metal and form nucleation sites where Si grains will grow that eventually come into contact with each other and form a continuous film. The MIG process began with thermal evaporation of the metal film. This was then coated with Co to modulate the Si grain growth and improve film quality. When Si was subsequently sputtered at an elevated temperature, the metal film acted as a catalyst to crystallize the Si and form a continuous µc-Si film. After deposition, films were annealed at 700 °C for 2 hr in forming gas. The appearance of distinct facets along the surface of the film indicated strong crystallization throughout the film. A strong presence of metal near the surface of films using Al compared to films using Ni and Cu signified metal contamination throughout the film. While x-ray diffraction demonstrated strong Si peaks with each metal, the film using Al observed extraneous peaks not indicative of µc-Si. Application of these films was explored by fabricating Schottky photodiodes, which were measured under dark and one-sun illumination conditions. Linearity in the log-log plot of dark forward bias indicated space charge limited conduction in films using Al likely due to considerable metal contamination. This trend also applied to the photo-response, where the fill factor greatly suffered. Films using Cu obtained performance closer to those with Ni. While Al is capable of reducing the crystallization temperature the most, its properties may not make it suitable for MIG. With optimized thickness, Cu may serve to realize a lower cost MIG process, while maintaining film quality.

4:50 PM Student

J10, Enhanced Light Absorption in Thin-Film Silicon Solar Cells by Scattering from Sub-Surface Dielectric Nanoparticles: *James Nagel*[1]; Michael Scarpulla[1]; [1]University of Utah

Thin-film silicon solar cell technology has been receiving a great deal of attention in recent years as an avenue for reducing the bulk material costs of photovoltaic devices. In particular, silicon is especially promising due to the well-established infrastructure for its production, as well as its natural abundance and non-toxicity. Unfortunately, silicon also suffers from long absorption lengths towards the red end of the visible spectrum, thereby severely limiting efficiency as the cell thickness is reduced. One common solution to this problem is to scatter light into lateral directions within the cell [1], thereby forcing light to propagate through more material over the same given depth. Unfortunately, such approaches have typically required feature sizes on the order to several microns, which is unfeasible when the cell itself is only 1-10 um in depth. Another method that has received significant attention in recent years has focused on light-scattering from surface plasmons on noble-metal nanoparticles placed over the cell [2, 3, 4]. This method works primarily by the same principle of light-trapping via lateral scattering within the cell, and does so with particles less than 100 nm in size. However, plasmonic enhancement has yet to be demonstrated in the presence of an anti-reflective coating (ARC), which is an essential component for capturing light within a solar cell. To take advantage of both the light collection from an ARC and the path-length enhancement from lateral scattering, we propose that nano-sized scatterers be

placed directly within the bulk material of the cell itself. As a demonstration of this concept, we used numerical computations from a finite-difference time-domain (FDTD) algorithm to simulate a 1.0 µm crystalline silicon (c-Si) solar cell with a 75 nm ARC composed of Si3N4. We then inserted nano-sized particles of SiO2 directly within the active layer of the cell to scatter light after passing through the ARC. We present the results of several simple geometries, including the full absorption function across the entire visible spectrum for each case. Our results indicate total absorbed power gains on the order of 5-10% when averaged across the visible spectrum, with most of the gain falling above 400 nm in wavelength. Around narrow bandwidths, some geometries can even surpass 70% in total absorbed power. We also explore the use of Au nanospheres as plasmonic scatterers in the presence of an ARC, with results that are inferior to the use of sub-surface dielectrics.

Session K: III-Nitride Nanowires

Wednesday PM
June 23, 2010

Room: 138
Location: University of Notre Dame

Session Chairs: Aric Sanders, NIST; Debdeep Jena, Univ of Notre Dame

1:30 PM

K1, Molecular Beam Epitaxy of Catalyst-Free InGaN/GaN Nanowires on (001) Silicon and Nanowire Light Emitting Diodes: *Wei Guo*[1]; Meng Zhang[1]; Pallab Bhattacharya[1]; [1]University of Michigan

There is a need to develop reliable white light emitting diodes (LEDs) as energy efficient light sources for the next generation. (In)GaN materials have attracted a great deal of attention due to their wide bandgap ranging from 0.7 (infrared) to 6eV (ultra-violet). (In)GaN nanowires can be grown with reduced defect density on silicon substrates since the large surface-to-volume ratio helps to accommodate the mismatch strain. We have investigated molecular beam epitaxial growth of catalyst-free (In)GaN nanowires directly on (001) silicon substrates, doping in the nanowires, and the characteristics of LEDs made with the nanostructures. Catalyst-free nanowires were grown on silicon substrates by plasma-assisted MBE using a radio frequency plasma source to activate the nitrogen. Unlike conventional III-nitride nanostructure growth, a few monolayer of gallium were first deposited at 800°C onto the substrate in the absence of N2 plasma. In order to study the nanowire growth mechanism, silicon substrates with different orientations, (100) and (111), were employed. The InGaN and GaN nanowires were grown under highly N-rich conditions. To achieve different emission wavelengths, InGaN nanowires with varied indium compositions were synthesized at 550°C. In addition, the indium composition was changed both gradually and abruptly along the nanowires during the growth to obtain broad and "white" emission. Structural characteristics of the nanowires grown on Si were studied using SEM. High density (~ 10^(11)cm^(-2)) nanowires were grown with diameters ranging from 10 to 50nm. HR-TEM image shows InGaN nanowires free of dislocations on (001) silicon. A lattice constant of 5.4 Å, which corresponds to 25% indium composition in the alloy, was derived from the SAD pattern. A cross-sectional TEM study of the GaN nanowires grown on silicon (100) and (111) substrates shows that in both cases growth proceeds along the c-axis. Room temperature PL spectra ranging from ultraviolet to red were obtained from nanowires with different indium compositions. Broad emission with 140nm FWHM was recorded from InGaN nanowires with gradually changed indium composition during epitaxy. Such emission is representative of "warm" white light. LEDs heterostructure consisting of p-type GaN, undoped InGaN with varied indium compositions and n-type GaN were grown on n-type (100) silicon substrate. After planarization and formation of p- and n-ohmic contacts, the I-V characteristics were measured. A series resistance of 50 O is derived from these characteristics. White light was emitted by the nanowire LED at room temperature at a forward bias current of 100 mA. These characteristics of the nanowires and LEDs will be presented.

1:50 PM

K2, Photoluminescence of Bandgap-Graded InGaN Wires Grown by Molecular Beam Epitaxy: *Vladimir Protasenko*[1]; Kevin Goodman[1]; Thomas Kosel[1]; Huili Grace[1]; Debdeep Jena[1]; [1]University of Notre Dame

Due to exceptional chemical stability and excellent mechanical, thermal, and electro-optical properties, the InGaN ternary alloy is a material of a choice for light emitting diodes (LEDs) and lasers operating in UV or near-UV spectral range. The usefulness of the material also stems from bandgap tunability; energy bandgap can be adjusted over broad range by proper choice of In concentration. For strained InGaN thin films grown on GaN, as the In concentration increases above ~10%, formation of structural defects and compositional disorder have been observed by high resolution TEM and atomic force microscopies, and by X-ray diffraction. On the other hand, for GaN semiconductor, it has been already demonstrated that shift from planar two-dimensional (2D) geometry of films to one-dimensional (1D) wires substantially suppresses the density of defects. So far, our attempts in growing ternary InGaN wires by MBE with ~20% In composition (suggested emission peak ~530 nm) uniformly distributed along the growth axis yield unexpected results. While the SEM micro-photographs unambiguously demonstrate successful non-catalytical growth of wires, low temperature photoluminescence (PL) studies, performed on wire ensembles, revealed broad emission spectra covering 360-700 nm range. In contrast, photoluminescence of a ~200 nm thick InGaN thin film with ~20% In content is well centered around 530 nm. At room temperature, a broad emission of wires collapses into 500-550 nm spectral range. To pinpoint the origin of a broad photoluminescence of wire ensembles, single wire PL and energy dispersive X-ray (EDX) measurements have been carried out. In PL experiments, substantial variations of the InGaN emission spectra of individual wires have been observed. While some wires show exhibit strong single peak emission, weaker and multiple peak emission of another wires indicates the essential intra-wire fluctuations of the In composition. On a separate set of single wires, EDX revealed gradual changes of In composition along the growth axis with the maximum concentration peaked near the wire tip. The EDX data in conjunction with scanning transmission electron microscopy and atomic force microscopy allowed us to estimate low temperature emission quantum yield of single wires. The estimates resulted in QY >10% and indicated that the surface of InGaN wires does not terribly quench the emission. The room temperature QY is about 10 times less than that measured at 4K. Currently, the development of a growth model for graded InGaN wires is in the progress, but, nevertheless, our data distinctly demonstrate the successful synthesis of compositionally graded InGaN wires using plasma assisted MBE. These defect-free wires offer not only a potential solution for a material suitable for the green emission but have potential applicability to broadband emission devices possibly as integrated phosphors.

2:10 PM

K3, Growth of Dislocation-Free and High-Indium-Content InGaN/GaN Coaxial Nanowires: *Qiming Li*[1]; George Wang[1]; [1]Sandia National Laboratories

High indium incorporation in InGaN is highly desirable for realizing high performance green and red III-nitride based light-emitting diodes. However, the large lattice mismatch between InGaN and GaN results in a high compressive strain energy density in InGaN, which leads to limited indium incorporation and high threading dislocation densities. In this work, we demonstrate the growth of dislocation-free InGaN layers on the sidewalls of GaN nanowires grown via Ni-catalyzed metal organic chemical vapor deposition (MOCVD). Indium incorporations as high as 40-60% in the shell layers were reached, as confirmed by scanning transition electron microscopy (STEM), energy dispersive x-ray spectroscopy, and spatially resolved cathodoluminescence microscopy. In order to better understand the results, the strain energy density distribution in an InGaN/GaN coaxial nanowire was calculated using finite element analysis. The indium distribution in the InGaN shell layer was found to be influenced by the strain energy density distribution. The observed high indium incorporation and lack of dislocations in the InGaN shell growth is attributed to the unique strain relaxation of the InGaN/GaN coaxial nanowires. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the

United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

2:30 PM

K4, Threshold Studies of Optically Pumped GaN Nanowire Lasers: *John Schlager*[1]; Alexana Roshko[1]; Aric Sanders[1]; Kris Bertness[1]; Norman Sanford[1]; [1]NIST

GaN nanowires grown by plasma-assisted molecular beam epitaxy (PAMBE) have shown to be made up of defect-free, c-axis-oriented, wurtzite material exhibiting hexagonal cross sections, narrow x-ray signatures, bright photoluminescence (PL) , and long (> 2ns) PL lifetimes. In addition, time-resolved photoluminescence (TRPL) measurements yield room-temperature surface recombination velocity (SRV) values of ~ 1×10^4cm/s for both doped and undoped nanowires without any special surface treatments. These relatively low SRV values were obtained under strong excitation conditions similar to those present during nanowire laser operation. Low SRV values indicate that efficient nanowire laser operation, where radiative recombination is the preferred route for photo- or electrically generated carriers, may be possible. In this work, the lasing thresholds of twenty-one optically pumped GaN nanowires grown by PAMBE and dispersed onto fused silica were measured. The excitation source was a frequency-quadrupled, Q-switched Nd:YVO_4 laser (266nm, 15kHz repetition rate, 8ns pulse duration, 8.5mW average power). Peak power intensities at the sample were kept below 10MW/cm^2 to avoid nanowire and substrate damage. The dimensions and morphology of the wires were determined with field-emission scanning electron microscopy (FESEM). Wire lengths ranged from 10.5µm to 18.7µm, and wire diameters ranged from 245nm to 1212nm. The wires had varying degrees of taper and different end qualities. With diameters of greater than 200nm and a material index of refraction of ~2.7, these GaN nanowires are multimode waveguides with strong confinement that can support over 20 transverse modes. The lasing thresholds were not strong functions of nanowire diameter, but depended more on wire morphology and wire-end quality. The threshold peak intensities varied from 203kW/cm^2 up to 3.26MW/cm^2. The lowest lasing threshold was obtained in a wire with no measurable taper and flat and perpendicular end facets. With increasing pump power, the wires first emitted photoluminescence (PL) at a wavelength of ~ 364nm (3.41eV), near the room-temperature bandgap of GaN. With higher pump powers, peak luminescence shifted to the red until narrow emission lines appeared around 371nm. The peak intensities of these lines, unlike the PL at 364nm, then increased superlinearly with pump power. The lasing spectra typically exhibited multiple lines corresponding to the oscillation of multiple axial modes. The axial mode separations ranged from 0.53nm to 1.2nm and were related to the roundtrip optical path lengths of these highly dispersive nanowire laser cavities. The discrepancy between the observed axial mode spacing and that calculated with an isotropic index indicates that the crystalline or birefringent nature of GaN is important to lasing behavior. Nanowires with good morphology (low taper) and flat ends are essential for low-threshold laser operation.

2:50 PM

K5, GaN Nanowire MOSFETs with Fully Conformal Cylindrical Gates: *Paul Blanchard*[1]; Kris Bertness[1]; Todd Harvey[1]; Aric Sanders[1]; Norman Sanford[1]; Steven George[2]; Dragos Seghete[2]; [1]National Institute of Standards and Technology (NIST); [2]University of Colorado

Due to their unique morphology, large direct bandgap, and excellent crystalline quality, GaN nanowires (NWs) grown by molecular beam epitaxy (MBE) are a promising material for the development of next-generation nanoscale electronic devices. In particular, GaN NW field effect transistors (FETs) have attracted significant interest both for potential device applications and for their usefulness in characterizing NW properties. However, previous GaN NW FETs have relied upon gates that do not make conformal contact to the entire nanowire circumference—at best, the NW has been sandwiched between a top and a bottom gate. This approach has generally led to inefficient gating. In addition, the asymmetric gate geometry of such devices makes it difficult to accurately extract NW carrier concentration from measured threshold voltages. In this report, we demonstrate novel n-type GaN NW metal oxide semiconductor FETs (MOSFETs) with symmetric, fully conformal cylindrical gates. After the MBE NW growth process, the as-grown NWs were conformally coated with approximately 43 nm of Al_2O_3 (k ~7.6) and 35 nm of W via atomic layer deposition (ALD). The coated NWs were then harvested from the growth substrate and aligned by dielectrophoresis across electrodes on the device substrate. After masking the central gate region of each NW with photoresist, the W and Al_2O_3 layers were removed from the two end regions (source and drain) of the NW by tungsten etchant and 10:1 buffered oxide etchant (BOE). Finally, ohmic source and drain contacts and a contact to the W/Al_2O_3 gate were deposited. The completed surround-gate MOSFETs operated as n-channel depletion mode devices, with each device containing a single NW. Threshold gate voltages were typically between -5 and -12 V, with subthreshold gate leakage current on the order of 1 pA or less. On/off current ratios as high as 10^9 were achieved with a drain-source bias of 5 to 6 V. Maximum transconductances exceeded 10 µS. These characteristics compare favorably with the best GaN NW-based FETs that have been previously demonstrated. By taking advantage of the radial symmetry of the gate and applying simple electrostatic analysis by use of Gauss' Law, the NW carrier concentrations were estimated from the threshold voltages to be between 4×10^{17} and 9×10^{17} cm^{-3}. Although these devices had excellent pinchoff characteristics, the NW MOSFETs also showed significant memory effects in gating. Hysteresis occurred during bi-directional gate voltage sweeps. In addition, threshold voltages sometimes drifted during repeated gate bias, resulting in uncertainty in the calculation of carrier concentration. These effects are most likely due to charge trapping at the NW/oxide interface or within the ALD Al_2O_3 layer. The nature of these charge traps is the subject of ongoing investigation.

3:10 PM Break

3:30 PM

K6, Formation Mechanisms and Kinetics of Negative Nanowires in GaN and ZnO Using In-Situ Transmission Electron Microscopes: *Bong-Joong Kim*[1]; Eric Stach[1]; [1]Purdue University

Crucial to nanotechnology is the creation of nanoscale building blocks of various sizes and shapes. Nanostructures of wide band-gap gallium nitride and zinc oxide are of particular interest because of their applications in short-wavelength optoelectronic devices and high-power/high-temperature electronics. Here, we present in-situ microscopy studies of formation mechanisms and kinetics of negative nanowires (analogous to hollow nanopipes) in the temperature regime where GaN and ZnO are spontaneously decomposed. By heating the GaN layers above 925 °C, nitrogen desorption first becomes visible at the thinnest edges of the sample. Concomitant with this is the preferential dissociation of GaN along the {10-10} prism planes, resulting in the formation of hexagonal vertical negative nanowires in [0001] with a slight tapering. We also find that liquid Ga droplets formed by this decomposition accumulate at the edge of the facetted wires with no need for the addition of a liquid-forming metal layer. These droplets subsequently lead to the creation of lateral negative nanowires growing in the close-packed <10-10> by the solid-liquid-vapor (SLV) mechanism and the resulting structures are often kinked. Our quantitative measurements show that the growth rates of the laterally grown negative nanowires are independent of the wire diameter, indicating that the rate-limiting step is decomposition of GaN on the gallium droplet's surface. We compare the above with evaporation of defect free ZnO layers at the annealing temperatures at 500 ~ 900 °C. Similar to GaN, we find the development of vertical negative nanowires, but no lateral negative nanowire formation, which could be related to the absence of a liquid-forming catalyst during evaporation. Similar annealing experiments were conducted by adding an evaporated Au layer on the ZnO film. Up to 900 °C, the Au drops remain solid and promote the selective evaporation of ZnO, creating vertical negative nanowires via the solid-solid-vapor (SSV) mechanism. Interestingly, the coarsening of the Au catalytic drops is found to be negligible up to 800 °C. These nanoscale features offer promise as controllable templates and patterns for the creation and integration of a broad range of nanoscale materials systems, with such potential applications as solar cells, LEDs, and FETs.

3:50 PM Student

K7, Self-Assembled GaN/AlN Nanowire Superlattices on Si toward Non-Polar Intersubband Photonics: *Santino Carnevale*[1]; J Yang[1]; P Phillips[1]; M Mills[1]; R Myers[1]; [1]Ohio State University

We examine coaxial growth of m-plane AlN/GaN superlattices (SLs) formed on self-assembled nanowires (NWs). Vertically aligned, c-plane oriented NW structures are grown on economical Si (111) by plasma-assisted molecular beam epitaxy. Previous reports indicate that these NWs are nearly defect free since threading dislocations terminate at the wires' base. Here we describe studies on the coaxial growth of SLs on the m-plane NW side walls. M-plane growth avoids band bending due to polarization charge, while the radial confinement allows for intersubband transitions normal to the Si substrates. Strain accommodation in the NWs allows for the formation of heterostructures with large conduction band offsets without adding dislocations that occur in planar films. Samples are grown in the N-rich regime at temperatures ranging from 700 to 800 °C at various combinations of III/V ratio and substrate temperatures to map out the growth phase diagram. Previous NW work has examined monotonic effects of group-III-flux, active nitrogen and substrate temperature on NW growth, but are not yet mapped into a growth phase diagram. We map out the NW density and radius dependence on calibrated III/V ratio and substrate temperature. This reveals systematic variations in NW density and growth rates, as well as the boundaries between 3D NW growth and 2D planar growth of GaN in the heavily N-rich regime. Using this information, NW density is controllable over two orders of magnitude. NW SLs are formed by first nucleating GaN NWs of a desired density and size and then alternately depositing GaN and AlN. Radial and horizontal growth rates calculated from SEM and z-contrast TEM measurements are used to design NW SLs for near-infrared intersubband transitions. Preliminary optical absorption and emission measurements of NW ensembles are presented.

4:10 PM

K8, HVPE Homoepitaxy of p-Type GaN on n-Type Catalyst Free GaN Nanowires: *Aric Sanders*[1]; Norman Sanford[1]; Paul Blanchard[1]; Kris Bertness[1]; John Schlager[1]; Andrew Herrero[1]; Christopher Dodson[1]; Albert Davydov[1]; Denis Tsvetkov[1]; Abhishek Motayed[1]; [1]National Institute of Standards and Technology (NIST)

Hydride Vapor Phase Epitaxy (HVPE) is a well established growth technique for the deposition of high free hole concentration p-type gallium nitride. It, like other gallium nitride growth techniques, suffers from the lack of high quality lattice matched substrates. We present the growth of p-type HVPE GaN using catalyst free GaN nitride nanowires as a lattice matched substrate. The nanowires were grown using plasma assisted molecular beam epitaxy (PAMBE), which has been shown to produce GaN of excellent quality on Si(111) substrates[1]. After wire growth, the n-type, silicon doped nanowires were used as a growth scaffold for p-type magnesium doped gallium nitride grown using HVPE. For small thicknesses of HVPE growth the resultant n-p material takes the form of core-shell nanowires. Scanning electron micrographs show distinctive dopant contrast between the p-type material and the n-type nanowires[2]. This contrast shows that the n-doped nanowire cores retain there hexagonal profile during the HVPE growth process. In addition, X ray diffraction under three symmetric and three asymmetric conditions reveal that the a and c lattice parameters of the nanowires remain unchanged after the HVPE deposition. The lattice parameters for three nanowire growths be fore and after HVPE growth fell between .518432 nm and .518536 nm for the c parameter and .31888 nm and .31910 nm for the a parameter. This is in agreement with other reported values for strain free GaN[3,4]. Photoluminescence at 4K for before HVPE growth shows near band emission at 3.472eV with clear phonon replicas and no observable sub bandgap features. After HVPE growth of p-type material, photoluminescence reveals the appearance of energy features at 2.8-3.0eV and 3.3eV that are associated with Mg incorporation in gallium nitride[5]. The spatially resolved morphology emission properties of the nanowires using electron microscopy will also be discussed. Finally, several electrical measurements determining material conductivity and carrier polarity will be presented. 1. K. Bertness et al., Catalyst-free growth of GaN nanowires. Journal of Electronic Materials (2006), 35, (4), 576-580. 2. M. El-Gomati et al.,Why is it possible to detect doped regions of semiconductors in low voltage SEM? Surf. Interface Anal. (2005); 37: 901–911. 3. Moram and Vickers, X-ray diffraction of III-nitrides, Rep. Prog. Phys. 72 (2009) 036502. 4. S.Porowski, Bulk and homoepitaxial GaN-growth and characterisation, J. Cryst. Growth 190, 153 (1998). 5. Reshchikov and Morkoc, Luminescence properties of defects in GaN. JAP 97, 06301 (2005).

4:30 PM

K9, Homoepitaxial Nucleation of GaN Nanowires in Grooves: *Alexana Roshko*[1]; Kris Bertness[1]; Todd Harvey[1]; Aric Sanders[1]; Matthew Brubaker[1]; Devin Rourke[1]; [1]NIST

In an effort to elucidate their nucleation mechanism, GaN nanowires were grown homoepitaxially by plasma-assisted molecular beam epitaxy on grooved substrates. The GaN templates consisted of 10 µm thick GaN (0001) films on Al_2O_3 substrates, with mechanically scribed grooves along the [11-20] and [1-100] directions and at 45 ° between these directions. It was found that the nanowires nucleated only in grooves on the GaN templates, not on the smooth (0001) surfaces. Based on the six sided nature of the nanowires it is concluded that they have a [0001] growth axis, as do GaN nanowires grown on Si (111) and on Al_2O_3 (0001) substrates with AlN buffers.[1-3] Also, analogous to many heteroepitaxial GaN nanowire growths, a matrix layer was formed across the entire substrate.[2-4] This matrix was comprised of dense hexagonal pits which were quite uniform on the smooth substrate surface but had steeper side walls and were less regular in the substrate grooves. Unlike growths on Si (111) and Al_2O_3 (0001), where the majority of nanowires grow perpendicular to the substrate surface,[1-4] the homoepitaxial nanowires grew at a wide range of orientations relative to the substrate normal. In addition the nanowires grew with a wide range of diameters (30 to 1000 nm), probably due at least in part to nanowire coalescence. In spite of their substantial variations in growth orientation and diameter, the nanowires have similar heights. The nanowire growth in the mechanically scribed grooves varied substantially from one groove to another and also frequently within a groove as well. These variations included: grooves completely filled with wires, grooves with almost no wires, grooves with both regions of wires and regions with no wires, and grooves with "rows" of wires. Interestingly the average nanowire diameter frequently differed from one "row" of wires to another along the same groove, indicating that the nanowire nucleation process was influenced by surface orientation or extent of damage/strain introduced by scribing. Growth of nanowires on substrates with etched grooves will also be discussed. 1. M. Yoshizawa, et al. Jpn. J. Appl. Phys. 36 L459 (1997). 2. E. Calleja, et al. Phys. Rev. B 62, 16826 (2000). 3. K.A. Bertness, et al. Phys. Stat. Sol 2, 2369 (2005). 4. A. Trampert, et al. p. 167 in Proc. 13th Int. Conf. on Microscopy of Semicond. Matls, edited by A. G. Cullis and P. A. Midgley, IOP Conf. Ser. No. 180 (2003).

4:50 PM

K10, Growth and Lift-off of High-Quality GaN Thin Films Using Self-Assembled Silica Microsphere Monolayers: *Qiming Li*[1]; George Wang[1]; [1]Sandia National Laboratories

We demonstrate that self-assembled monolayers of silica microspheres can be used as inexpensive, selective growth masks for both significant threading dislocation density reduction and laser-free lift-off of GaN epilayers and devices. Silica microspheres self-assemble into a close-packed monolayer on the surface of an initial GaN epilayer on sapphire using a Langmuir-Blodgett method. In a subsequent GaN regrowth, the silica microspheres effectively terminate the propagation of threading dislocations. As a result, the threading dislocation density, measured by large area AFM and CL scans, is reduced from 3.3 × 109 cm-2 to 4.0 ×107 cm-2. This nearly two orders of magnitude reduction is attributed to a dislocation blocking and bending by the unique interface between GaN and silica microspheres. The sequential wet etching of the samples in HF solution removes the silica microspheres sandwiched between the GaN epilayers and the growth template. Further wet etching of the samples in KOH solution successfully detaches the GaN epilayers from the growth templates. Micro-channels are created on the GaN epilayers by plasma etching in order to facilitate the uniformity of the wet etches. This laser-free lift-off technique may be potentially applied to lift-off GaN homoepitaxial thin film device from GaN bulk substrates. Sandia is a multiprogram laboratory operated by Sandia

Corporation, a Lockheed Martin Company, for the United States Department of Energy under contract DE-AC04-94AL85000.

Session L: III-N HEMTs I

Wednesday PM
June 23, 2010

Room: 155
Location: University of Notre Dame

Session Chairs: Siddharth Rajan, The Ohio State University; Debdeep Jena, University of Notre Dame

1:30 PM

L1, Formation of Structural Defects in AlGaN/GaN High Electron Mobility Transistors under Electrical Stress: *Prashanth Makaram*[1]; Jungwoo Joh[1]; Carl Thompson[1]; Jesus Del Alamo[1]; Tomas Palacios[1]; [1]Massachusetts Institute of Technology

Gallium nitride (GaN) based devices are of interest for a variety of radar and communication applications due to their ability to operate at high-power and high frequency. We have previously carried out extensive electrical reliability characterization of AlGaN/GaN high electron mobility transistors (HEMTs) and found that degradation is driven by electric field. High-voltage stress results in an increase in off-state gate current, IGoff and drain resistance, RD, along with a decrease in maximum drain current, IDmax. Transmission electron microscope (TEM) cross sectional image has shown that electrical degradation is closely related to structural damage in the GaN cap and AlGaN barrier layers. Although the TEM analysis shows a detailed cross section of the defect area, it is an extremely localized technique. In order to better understand the structural degradation of AlGaN/GaN HEMTs under electrical stress, a planar view of defect formation is required. In this work, we study plane view structural degradation of AlGaN/GaN HEMTs after electrical stress by removing the SiN passivation layer and all the metals from the sample. We then use atomic force microscope (AFM) and scanning electron microscope (SEM) to image the semiconductor surface. In a series of OFF state (low ID, high VDS) experiments, identical devices were step-stressed up to various VDG's from 15 to 57 V at 150 C of base plate temperature. The critical voltage Vcrit for which a sharp increase of gate current occurs [2] was determined to be around 20 V for this condition. For Vstress>Vcrit, significant permanent decrease in IDmax of up to 10% as well as a large increase in current collapse took place. While the surface of a non-stressed device was found to be smooth after gate removal, AFM images of stressed devices revealed that a line-shaped indentation developed along the gate edge on the drain side for all stressed devices. For devices stressed at high voltage, the same feature, but more shallow, was found on the source side as well. In addition, beyond the critical voltage we observed nanopipe or pit formation at the drain side edge of the gate. These pits grow in density and size along the gate as the stress voltage increases. In order to understand time evolution of these crystallographic defects, we have also performed OFF-state stress tests at VDG=50 V. Two devices were stressed for 10 and 1000 minutes, respectively. We observe that as the device is stressed for longer times, the pits grow and merge to form a continuous defective region along the gate finger. This represents the first planar view of structural defects in electrically stressed GaN HEMTs. The methodology described here will enable better understanding of the evolution of defect formation under various electrical stress conditions.

1:50 PM Student

L2, Electrical Properties of GaN/AlN/GaN Heterostructures: Presence of 2DHG: *Satyaki Ganguly*[1]; Debdeep Jena[1]; [1]University of Notre Dame

Large band offsets coupled with the highest possible spontaneous and strain induced polarization fields in AlN/GaN heterostructures have led to the formation of two-dimensional electron gas (2DEGs) with densities in excess of $1x10^{13}cm^{-2}$. However, it is necessary to grow a thin epitaxial cap layer of GaN on top of the AlN/GaN heterostructure in many device applications. In this work we study the total charge density and mobility of the resulting conducting channels with respect to the GaN cap thicknesses. For this study the MBE growths were performed under metal rich conditions. A series of samples with a thin 1.5nm AlN nucleation layer (to eliminate the buffer leakage), followed by 235nm UID GaN, 3.5nm AlN barrier and GaN cap thicknesses ranging from 0nm to 40nm were grown. 'In' contacts in the van-der Pauw geometry were made for Hall Effect measurements. With the increase of the GaN cap layer thickness, the measured carrier density increased from $1x10^{13}$ cm^{-2} (no GaN cap) to ~$5x10^{13}cm^{-2}$ (40nm GaN cap) at RT. The trend obtained here is contradictory to an earlier report. The carrier mobility measured in this work shows a slight increase at the beginning (1000 cm^2/V-s for no GaN cap to 1100 cm^2/V-s for 4nm GaN cap) and then decreases steadily from 1100 cm^2/V-s (4nm GaN cap) to ~529 cm^2/V-s (40nm GaN cap) at RT. The trend as obtained from the experimental data is well explained by considering the formation of two-dimensional hole gas (2DHG) at the GaN/AlN interface near the surface. With the increase of GaN cap layer thickness, the valence band edge in the GaN cap layer starts approaching the Fermi level, resulting in the formation of a 2DHG. A simple analytical model considering the formation of both 2DEG and 2DHG (which was overlooked in earlier report) reveals the decreasing and increasing trend of 2DEG and 2DHG respectively with the increase of GaN cap thickness. The total carrier density and total mobility formulated from the two carrier Hall model, is given as $n_t = (n\mu_n + p\mu_p)^2/ (p\mu_p^2 - n\mu_n^2)$; $\mu_t = |(p\mu_p^2 - n\mu_n^2)/ (n\mu_n + p\mu_p)|$. Assuming μ_n~1000 cm^2/V-s (which is quite reasonable as evident from the experimental data), μ_p~400 cm^2/V-s (to fit the experimental data) and calculating n and p from the analytical model, the total carrier charge density and mobility with varying GaN cap thicknesses are determined. It has been found that the experimentally obtained and the analytically calculated total carrier charge density and mobility are in reasonable agreement. The simultaneous presence of 2DEG and 2DHG in this structure opens the possibility of various novel applications such as GaN based natural super junctions for high voltage switching.

2:10 PM Student

L3, Study of Cause of G_m-Collapse for Higher Gate Voltages in N-Polar GaN HEMTs with Scaled GaN Channels: *Nidhi Nidhi*[1]; Oliver Bierwagen[1]; Sansaptak Dasgupta[1]; David Brown[1]; Stacia Keller[1]; James Speck[1]; Umesh Mishra[1]; [1]University of California Santa Barbara

N-polar GaN/AlGaN HEMTs have been of interest to the nitrides community recently due to their several advantages over Ga-polar GaN-based HEMTs such as lower contact resistance, better electron confinement and enhancement mode operation. Currently, N–polar GaN HEMTs are being scaled to achieve X and Ka band performances. Scaling in N-face HEMTs, however involves scaling of GaN channel along with gate-length, in comparison to Ga-face where the barrier material is scaled instead of the channel. Scaled self-aligned HEMTs on N-face with regrown access regions reported by Nidhi et. al. at IEDM 2009 demonstrated significant reduction in access resistance. However, even though gm remained flat for large values of current due to no source choke in a self-aligned structure, it was observed that gm fell rapidly with higher gate biases even before the gate was forward biased. In this paper, this anomalous gm-collapse for higher gate voltages has been studied by using low temperature Hall and gated TLM measurements. It has been proposed that as the GaN channel thickness is scaled, application of higher gate biases shifts the centroid of the 2-dimensional electron-gas towards the GaN/SiNx-insulator interface, thereby causing mobility degradation which then causes the transconductance to collapse. It is proposed that the insertion of AlN interlayer above the GaN channel could help prevent the penetration of electron wavefunction into the SiNx due to the barrier created by the band-edge discontinuity and reverse polarization fields, and hence reduce the interface roughness and remote impurity scattering from the SiNx interface.

2:30 PM Student

L4, Polarization-Engineered Low-Leakage Buffers for Nitride HEMTs Grown by MBE: *Yu Cao*[1]; Guowang Li[1]; Ronghua Wang[1]; Chuanxin Lian[1]; Tom Zimmermann[1]; Grace Xing[1]; Debdeep Jena[1]; [1]University of Notre Dame

Buffer leakage is a vexing problem in the development of nitride HEMTs. It degrades the on/off ratio in digital devices, decreases the device speed in high-speed analog applications, and compromises the breakdown property in high-voltage switching applications. This problem exists in HEMTs grown on both

semi-insulating (SI) SiC and GaN substrates/templates. On SI GaN templates, high-quality Al(Ga)N/GaN heterojunctions can be achieved using just a few hundred nm GaN buffer layer, which greatly reduces required epitaxial resources and time. Recently, we reported a dopant-free approach by engineering the polarization effect. Insertion of an ultrathin AlN nucleation layer (NL) greatly reduces the buffer leakage, and leads to a much steeper subthreshold slope of HEMT devices and the on/off ratio increased from 10^2 to 10^6. Motivated by this prior result, we have performed a systematic study of the buffer leakage dependence on the AlN nucleation layer thickness, and growth conditions. Two series of AlN/GaN HEMTs were grown by MBE to investigate the buffer leakage as a function of a)the metal fluxes and the b)NL thickness in MBE growth. In the first series (a), the AlN NL thickness was fixed at 1.5 nm, while the Al flux F(Al) for this NL was varied from ~4.0e-8 Torr to ~1.7e-7 Torr. The NL grown in Al metal-rich regime results in high buffer leakage. The NL grown in the intermediate regime shows good buffer insulation at low bias, but breaks down rapidly at high bias. The N-rich growth condition is found to result in the most insulating buffer, where the leakage current density is less than 10 nA/mm at 10 V DC bias. The nitrogen-rich grown AlN NL prohibits the diffusion of the n-type impurities like silicon and oxygen from the substrate into the GaN buffer. Meanwhile, a natural AlN back barrier is formed, which provides better 2DEG confinement and prevents electrons flowing to the regrowth region under bias. The second series (b) were grown with NL thicknesses 1.5 nm, 3.0 nm, 4.5 nm and 9.0 nm. The buffer leakage mapping across a 1x1 cm2 sample with a 1.5 nm AlN NL shows leakage less than 5 nA/mm in all dies except the one. In samples with thicker AlN NLs, the leakage current has large spans, sometimes varying from nA/mm to mA/mm. It is clear that thick AlN NLs are not suitable for HEMTs. We conclude that the nucleation layer needs to be well designed to avoid forming new conducting paths in the buffer layer. A 1.5 nm AlN nucleation layer grown in the N-rich regime with Al flux of ~4.1e-8torr achieves highly insulating buffer with a high degree of uniformity. This result presents an attractive route towards GaN-based digital and high voltage devices in the future.

2:50 PM Student

L5, The Influence of High-k Gate Dielectrics on Deep Traps in AlGaN/GaN High Electron Mobility Transistors Measured by Deep Level Spectroscopy Methods: *Qilin Gu*[1]; Aaron Arehart[1]; Andrew Malonis[1]; Omair Saadat[2]; Tomas Palacios[2]; Steven Ringel[1]; [1]The Ohio State University; [2]Massachusetts Institute of Technology

Surface passivation by dielectric layers has been extensively used to address reliability issues related to gate leakage current associated with surface states for GaN electronics. For this purpose, high-k dielectric materials with excellent thermal stabilities are of great interest and recent efforts demonstrated that AlGaN/GaN HEMTs passivated by Al_2O_3, Ga_2O_3, and HfO_2 exhibit significant reduction in gate leakage and enhancements in drain current.[1] However, the effects of high-k dielectrics on the presence and evolution of trap states are relatively unexplored. Given the connection between traps, passivation and reliability, this area is of great interest. Here, we employed constant-drain-current-based deep level optical and transient spectroscopies[2] (CI_D-DLOS/CI_D-DLTS) to investigate correlations between deep levels and specific high-k dielectrics in AlGaN/GaN HEMTs. Ga-face AlGaN/GaN devices with 2 nm GaN cap layers were grown on Si (111) substrate by Nitronex using metalorganic chemical vapor deposition. One sample was processed without passivation, whereas two other samples were passivated by 15 nm Al_2O_3 and 15 nm HfO_2 high-k dielectrics, respectively, deposited by atomic layer deposition to form metal-oxide-semiconductor (MOS)-HEMTs. CI_D-DLOS measurements revealed trap levels at E_C-3.10 eV and E_C-3.85 eV for un-passivated devices, matching those observed earlier for AlGaN layers,[2,3] an additional level at E_C-1.68 eV, and a level at ~E_C-2.6 eV likely due to the V_{Ga} in GaN. Passivation resulted in significant differences in the DLOS spectra. The most obvious result is a >5X increase in total trap concentration for the HfO_2 passivated device – noting that sources for most of these traps have been previously assigned to carbon or cation vacancy defects in GaN and AlGaN.[3-4] More striking is the appearance of a new trap with an ~E_C-1.8 eV onset and concentration of ~1-2×10^{12} cm^{-2}, which might be associated with the HfO_2/GaN interface or the HfO_2 itself. The high trap concentration creates a large threshold voltage shift upon optical excitation of individual traps. This effect was not apparent for the Al_2O_3-passivated sample, which revealed relatively little impact based on CI_D-DLOS alone. We are presently performing CI_D-DLTS measurements to observe traps closer to E_C than possible by CI_D-DLOS to obtain a comprehensive picture. However, pulsed I-V results from these devices are also revealing and consistent with the trap spectroscopy results where the HfO_2 passivated device displays the largest drain-current dispersion while Al_2O_3 passivation both reduces dispersion and increases the drain current magnitude compared to the un-passivated device – both of which may result from successful passivation of shallower states that we are currently exploring by CI_D-DLTS. [1] O. I. Saadat, et al., IEEE Electron Device Lett.,30,1254(2009). [2] A. Arehart, PhD dissertation, The Ohio State University, 2009. [3] A. Armstrong et al., Appl. Phys. Lett.,89,262116(2006).[4] A. Hierro et al., Appl. Phys. Lett.,77,1499(2000).

3:10 PM Break

3:30 PM

L6, PECVD-SiN, Si or Si/Al_2O_3-Capped ED-Mode AlN/GaN Inverters: *Tom Zimmermann*[1]; Yu Cao[1]; Guowang Li[1]; Ronhua Wang[1]; Patrick Fay[1]; Greg Snider[1]; Debdeep Jena[1]; Huili Xing[1]; [1]University of Notre Dame

Enhancement-depletion-mode subcritical barrier AlN/GaN inverters have been fabricated. In subcritical heterostructures there is no 2DEG at the AlN/GaN interface. Additional cap-layers on top of the ultra-thin AlN barrier can reliable enhance a 2DEG at the heterointerface with high 2DEG-densities in excess of 10^{13} cm^{-2}. CAT-CVD-, Silicon- and Si/CAT-CVD-caps got already explored but Silicon caps proofed instable over time in air and PECVD-SiN with a sheet-resistance-optimized thickness of about 15 nm is too thick for gate-dielectrics. In contrast, a thin Si (2 nm / ALD-Al_2O_3(4 nm) cap layer reliably enhances a 2DEG in subcritical AlN/GaN heterostructures with 1.5 nm AlN barrier and highly insulating buffer. The induced 2DEG results in a low heterostructure sheet resistance of ~320 Ohm/sq. with a very high sheet charge density of ~4x10^{13} cm^{-2}. The demonstrated inverter is operating at V_{DD} = 5 V and consists of an enhancement- and depletion-mode HEMT with 1.5 nm thin subcritical AlN barrier, a low-power PECVD-SiN cap-layer and ebeam-Al_2O_3 gate oxide. The low-power SiN deposition in a standard PECVD shall avoid plasma-damage to the heterostructure. Ohmic contacts are deposited on top of SiN layer and get RTP-annealed. Gate-length for e-mode and d-mode FET are 3 µm and 2 µm, respectively. The sub-thresholdslope of ~600 mV/decade and a threshold voltage V_{th} = -1.2 V for the depletion-mode FET in the inverter has similar absolute values like the used enhancement-mode FET with ~620 mV/decade ss-swing and V_{th} = +1.1 V. Further technological optimization especially of ohmic contacts will lead to similar high DC-output current levels in e- and d-mode subcritical AlN/GaN devices and will enable the monolithic integration of enhancement- and depletion-mode AlN/GaN HEMTs for digital logic applications.

3:50 PM

L7, Late News

4:10 PM

L8, Demonstration of Enhancement Mode AlN/Ultrathin AlGaN/GaN HEMTs Using Selective Wet Etching: *Travis Anderson*[1]; Marko Tadjer[2]; Michael Mastro[1]; Jennifer Hite[1]; Karl Hobart[1]; Charles Eddy[1]; Fritz Kub[1]; [1]Naval Research Laboratory; [2]University of Maryland

The AlGaN/GaN High Electron Mobility Transistor (HEMT) has attracted considerable attention as a candidate next-generation device for both microwave and high power switching applications. While significant progress has been made toward developing depletion mode devices, a normally-off device is highly desirable for two key applications: power converters and digital logic circuits. Most efforts toward normally-off operation have focused on plasma processing methods to selectively modify the charge distribution only in the region under the gate, either by inductively coupled plasma (ICP) etching or fluorine-based plasma exposure. In this work, a reliable and selective wet etch structure is demonstrated. This structure consists of a GaN buffer layer, an ultrathin AlGaN layer (<8 nm) for threshold voltage control, and an AlN cap

layer to increase the polarization charge and reduce resistance in the source-drain access regions. A selective wet etch process has been developed based on literature reports that AlN is etched in heated AZ400K photoresist developer. A set of test samples with an 8 nm AlGaN layer were initially used to study the wet etch process and verify selectivity. XPS characterization confirmed that the etch is selective to AlN, and stopped on layers containing Ga. SEM images were taken on ungated samples, and indicated lateral etching of the AlN layer due to the isotropic nature of the wet etch process. A study of threshold voltage indicated a shift from -1.3V on an unetched structure to -0.4V after 10 minutes of etching, then no further change up to 70 minutes, supporting the etch stop hypothesis. The current level degraded with each subsequent etch step, which was thought to be due to the increase the resistance in the source-drain access regions due to the lateral etching. This is consistent with measurements of the on-resistance from gated device testing. A sample with a 4 nm AlGaN layer, etched using the optimized etch time, demonstrated a threshold voltage of +0.21V, shown in Figure 3. The threshold voltage values for both 8 nm and 4 nm AlGaN layers are consistent with theoretical calculations and literature reports from structures with comparable AlGaN thickness. While current density was low, it is comparable to that found in an unetched structure with similar sheet resistance and charge density.

4:30 PM Student

L9, Growth and Characterization of InGaN Heterojunction Bipolar Transistors: *Zachary Lochner*[1]; Hee Jin Kim[1]; Suk Choi[1]; Yi-Che Lee[1]; Yun Zhang[1]; Jae-Hyun Ryou[1]; Shyh-Chiang Shen[1]; Russell Dupuis[1]; [1]Georgia Institute of Technology

The device operation of InGaN/GaN heterojunction bipolar transistors (HBTs) grown by metalorganic chemical vapor deposition is examined. InGaN is used in the p-type base layer for NpN III-nitride HBTs due to its improved p-type electrical properties, as well as its lower bandgap energy relative to that of GaN, resulting in reduced base contact and sheet resistance. The strain induced between the InGaN base and outer GaN emitter and collector layers leads to material defects, such as dislocation and V-defects, degrading the quality of the base and emitter, and hence inhibiting the device performance. Thus a graded base-collector (BC) and base-emitter (BE) structure was previously developed to improve crystal qualities at each interface and improve the current gain. This study compares structures with two different Indium concentrations, 3% and 5%, each employing the graded junction design. The HBT structures presented in this study consists of a 70 nm n^{++}-GaN:Si ($n=1\times10^{19}$ cm^{-3}) emitter, a 30 nm n^{++}-$In_xGa_{1-x}N$:Si ($n=1\times10^{19}$ cm^{-3} x=0.03/0.05-0) graded emitter, a 100 nm p^{+}-$In_xGa_{1-x}N$:Mg base ($p=2.5\times 10^{18}$ cm^{-3}, x=0.03, 0.05), a 30 nm $In_xGa_{1-x}N$:Si graded collector ($n=1\times10^{18}$ cm^{-3}, x=0-0.03/0.05), a 0.5 µm n-GaN:Si collector ($n=1\times10^{17}$ cm^{-3}), and 1.0 µm n^{+}-GaN:Si subcollector ($n=2\times10^{18}$ cm^{-3}). The BC grading layer was grown by ramping the trimethylindium (TMI) flow rate, while the BE grading layer utilized both TMI and temperature ramping. The Indium composition was varied by adjusting the base growth temperatures to 850°C and 820°C for 3% and 5% respectively. Separate samples were grown just up to the base to compare the surface morphology of $In_{0.03}Ga_{0.97}N$ and $In_{0.05}Ga_{0.95}N$ by atomic force microscopy. The $In_{0.05}Ga_{0.95}N$ base-only sample had a higher pit density than the $In_{0.03}Ga_{0.97}N$ counterpart, as is expected from higher strain conditions. The effects of these defects are reflected in the device performance. If we consider the band offset between the InGaN base and GaN layer, the HBTs with p-$In_{0.05}Ga_{0.95}N$ base are expected to show higher current gain than HBTs with p-$In_{0.03}Ga_{0.97}N$ base. However, typical current gains for HBTs with p-$In_{0.03}Ga_{0.97}N$ base were found to be around 82 and the current gains for HBTs with p-$In_{0.05}Ga_{0.95}N$ base were around 35, lower than that of the HBTs with p-$In_{0.03}Ga_{0.97}N$ base. It is supposed that the higher defect density compromises the benefits of the lower bandgap. Several other device configurations have also been considered in order to improve performance, including a single quantum well and superlattice base structure. It is theorized that the quantum confinement will aid lateral carrier transport within the base.

4:50 PM Student

L10, High Temperature Transport Properties of GaN HEMTs with Various Heterostructure Designs: *Ronghua Wang*[1]; Yu Cao[1]; Guowang Li[1]; Tom Zimmermann[1]; Chuanxin Lian[1]; Xiang Gao[2]; Shiping Guo[2]; Debdeep Jena[1]; Huili Xing[1]; [1]University of Notre Dame; [2]IQE RF LLC

GaN based HEMTs are being developed for high-temperature, high-power and high-frequency applications. The advantages over traditional GaAs and Si based electronic devices are the wide band gap, and high carrier densities. At high current levels, the channel reaches high temperatures in AlGaN/GaN HEMTs, with a corresponding drop in the conductance of the two-dimensional electron gas (2DEG). To improve the high-power and high-temperature device performance, it is necessary to understand the high temperature transport properties of nitride transistors. In this work, high temperature Hall-effect measurements were performed for GaN HEMTs employing various heterostructures. Five different HEMT heterostructures were studied in a comparative fashion-(a) Al0.28Ga0.72N/GaN, (b) Al0.28Ga0.72N/AlN/GaN, (c) Al0.83In0.17N/AlN/GaN, (d)Al0.80Ga0.20N/AlN/GaN, and (e) AlN/GaN. Mesa-isolated van der Pauw geometries with annealed Ti/Al/Ni/Au contacts were used for Hall-effect measurements, which were performed with a Lakeshore HMS system over the temperature range 25°C<T<475°C. The 2DEG density Ns drops slightly from 25 to 200°C and then increases monotonically for Sample (a)-(c), but increased slowly from 25 to 400°C, and then sharply till 475°C in Sample (d)-(e). The charge density in each sub-band Ns (i) is related with Ef-Ei and T, and $N_s\alpha T$ in our study arrange with a constant Ef-Ei. But the band gap shrinkage with increasing temperature leads to a smaller Ef-Ei, and therefore Ns decreased first in Sample (a)-(c). But in Sample (d) and (e), thermal expansion should be considered because both structures have a very large piezoelectric polarization, which strongly depends on the strain. For all the samples, Ns increased sharply for T>400°C. This is possibly associated with the thermal ionization of deep-levels and traps in GaN buffers, but needs more work to verify. The 2DEG mobility drops with increasing temperature, and merges to ~200 cm2/V.s at 475°C irrespective of the heterostructure design. Taking Sample (a) and (b) as examples, acoustic phonon (AP) scattering, longitudinal optical (LO) phonon scattering, and alloy disorder scattering mechanisms were taken into account to model the mobility temperature-dependence, and resulted in a good match with the experimental results. When the temperature is higher than 200°C, LO phonon scattering becomes dominant, and the mobility becomes independent of the specific nature of the heterostructure. When the temperature is lower than 200°C, the slight mobility variation is related with the 2DEG density; LO phonon scattering is stronger for higher carrier density, leading to a lower mobility. In summary, high temperature transport properties in various GaN HEMT heterostructures from 25 to 475°C have been investigated using Hall-effect measurements. The 2DEG density change varies in different structures but increases generally, and the mobility drops as temperature increases. At temperatures higher than 400°C, LO phonon scattering limits the mobility to 200 cm2/V.s for all studied heterostructures.

Session M: Graphene - Materials and Characterization

Thursday AM
June 24, 2010

Room: 102
Location: University of Notre Dame

Session Chairs: Michael Spencer, Cornell University; Randall Feenstra, Carnegie Mellon University

8:20 AM Invited

M1, Material and Electronic Properties of CVD Graphene Grown on Ni and Cu then Transferred to Insulators: Helin Cao[1]; Qingkai Yu[2]; Luis Jauregui[1]; Deepak Pandey[1]; Robert Colby[1]; Jifa Tian[1]; Nathan Guisinger[3]; Eric Stach[1]; Steven Pei[2]; *Yong Chen*[1]; [1]Purdue Univ; [2]University of Houston; [3]Argonne Nat Lab

We have synthesized large scale (up to several inches) graphitic and graphene thin films by chemical vapor deposition (CVD) on polycrystalline Ni (1,2) and Cu (3) foils and systematically characterized their structural and electronic properties after transferred onto insulating SiO2 (on doped Si) substrates. For films grown on Ni (1,2), structural characterizations by atomic force microscopy (AFM), scanning tunneling microscopy (STM), cross-sectional transmission electron microscopy (XTEM)(4) and spectroscopic Raman mapping confirm that such large scale graphitic thin films contain both thick graphite regions and thin regions of few layer graphene. The films also contain many wrinkles, with sharply-bent tip and dislocations revealed by XTEM, yielding insights on the growth and buckling processes of the film. Measurements on mm-scale back-gated transistor devices fabricated from the transferred film show ambipolar field effect with resistance modulation ~50% and carrier mobilities reaching ~2000 cm^2/Vs. We also demonstrate quantum transport of carriers with phase coherence length over 0.2 μm from the observation of 2D weak localization in low temperature magneto-transport measurements. Our results show that despite the non-uniformity and surface roughness, such large-scale, flexible thin films can have electronic properties promising for device applications. For films grown on Cu (3), we show they consist dominantly of monolayer graphene as indicated by Raman mapping. STM imaging shows monolayer graphene lattice. Low temperature transport measurements are performed on micro devices fabricated from such CVD graphene, displaying ambipolar field effect (with on/off ratio ~5 and carrier mobilities up to ~3000 cm^2/Vs) and "half-integer" quantum Hall effect, a hall-mark of intrinsic electronic properties of monolayer graphene. We also observe weak localization and extract information about phase coherence and scattering of carriers by disorder in the graphene. Finally, we have measured the thermal conductivity of suspended CVD graphene to be ~3000 W/m-K, comparable with that of exfoliated graphene, by combining electronic transport and Raman thermometry (5). 1. Q. Yu et al., Applied Physics Letters, 93, 113103 (2008); 2. H. Cao et al., Journal of Applied Physics, 107, in press (2010) DOI: 10.1063/1.3309018; 3. H. Cao et al., Applied Physics Letters, accepted (2010) (arXiv: 0910.4329); 4. R. Colby et al., Diamond and Related Materials 19, 143 (2010); 5. L. Jauregui et al., ECS Transactions (Proc. ECS-217), in press (2010).

9:00 AM

M2, Fabrication and Characterization of Graphene Materials Grown via CVD on Copper Based Substrates: *Michelle Kelly*[1]; Kristof Tahy[1]; M. Jane Fleming[2]; Barbara Raynal[1]; Vladimir Protasenko[1]; Huili Xing[1]; Debdeep Jena[1]; [1]University of Notre Dame; [2]Saint Mary's College

The exceptional electrical properties of graphene materials have led to an explosion of research investigating graphene's potential as the foundation for a future generation of devices as well as developing methods of producing high quality graphene materials. Material quality and our ability to manipulate graphene's properties will ultimately determine the success of graphene as a device platform. Recently, the formation of single layer graphene via catalyzed-chemical vapor deposition (CVD) on copper foils has generated rapidly a rapidly growing body of research on graphene materials produced by CVD on copper based substrates.[1] In this work, we explore growth conditions by CVD of graphene on metal substrates with subsequent structural and electrical characterization. We deposit single layer graphene films using catalyzed-CVD on copper foil, evaporated copper films, and copper-nickel alloy substrates. Pre-growth chemical and thermal treatment of the copper catalyst material enables graphene deposition at temperatures ranging from 800-1050 \176C. Following growth, graphene sheets are transferred to a range of host substrates using wet etch methods similar to those described in other work1 or processed in place by undercutting evaporated copper films as demonstrated by Levendorf et.al.[2] Using Raman mapping, we show that we can routinely produce large area single-layer graphene with Raman spectra showing a characteristic 2D:G peak ratio of ~2 that is uniform over large regions. Additional supporting characterization is made using SEM and AFM. One promising future application for graphene materials is in radiofrequency (RF) devices. We have previously reported RF device performance for epitaxial graphene from SiC substrates.[3] RF device characteristics of graphene derived from SiC will be compared to CVD graphene on metal substrates. [1]Li, X., et. al. Science, 324, 1312-1314 (2009). [2]Levendorf, M.P., et.al. Nano Letters, 9, 4479-4483 (2009). [3]Tahy, K., et. al. Conference digest of the 67th DRC(2009).

9:20 AM Student

M3, Kinetic Limitations in the Formation of Graphene on the C-Face of SiC: *Luxmi Luxmi*[1]; Nishtha Srivastava[1]; Patrick Fisher[1]; Randall Feenstra[1]; [1]Carnegie Mellon University

Correlated atomic force microscopy (AFM) and low-energy electron microscopy (LEEM) measurements are used to study the formation of epitaxial graphene on the two different faces of SiC{0001} – the (0001) surface (*Si-face*) and the (000-1) surface (*C-face*). The graphene formation is found to occur in quite different ways in the two cases. For the Si-face, using graphene preparation by annealing the SiC wafer in vacuum, graphene is found to form predominantly in a layer-by-layer mode for graphene thickness greater than 2 monolayers (ML). For thinner graphene, e.g. with an average thickness of 1 ML, vacuum annealing produces considerable inhomogeneity in the thickness, but the use of annealing in an argon environment is found to enable the formation of uniform ML-thick film.[1] Thus, for the Si-face, the techniques for reproducible formation of uniform, constant-thickness graphene films seem to be well in hand. The situation for the C-face is, however, quite different. For one thing, the temperature required for formation of a given graphene thickness, ≈4 ML, on the C-face are about 200°C lower than for the Si-face. We find that this reduction in temperature yields greatly differing motion of surface steps during graphene formation for the two cases. For the Si-face the steps are found to form bunches, separated by typically 10 μm or more, with large, flat terrace separating the bunches. In contrast, for the C-face, motion of steps is limited to a few μm, and we observe in LEEM graphene domains with a wide range of thicknesses and limited in lateral extent to a few μm. This limited motion of the surface steps provides evidence, we believe, of a significant kinetic limitation in the graphene formation for the C-face. We have performed both AFM and LEEM on identical locations of a C-face graphene film, from which we determine *lower surface morphology* on areas having *thicker graphene*, thus also providing evidence for limited kinetics in the graphene formation on the C-face by vacuum annealing. Unlike the situation for the Si-face, we have not thus far been able to produce ML-thick graphene on the C-face using argon annealing; rather, we obtain either very thick films or zero graphene thickness. These studies are continuing, with the use of a disilane environment as an alternative to the argon environment.[2] This work is supported by NSF. [1]C. Virojanadara, M. Syväjarvi, R. Yakimova et. al., Phys. Rev. B 78, 245403 (2008). [2]R. M. Tromp and J. B. Hannon, Phys. Rev. Lett. 102, 106104 (2009).

9:40 AM Student

M4, Graphene to Graphane: Novel Electrochemical Conversion and Possible Applications: *Kevin Daniels*[1]; Biplob Daas[1]; Rui Zhang[1]; John Weidner[1]; Christopher Williams[1]; Tangali Sudarshan[1]; MVS Chandrashekhar[1]; [1]University of South Carolina

Graphene hydride, or better known as graphane is as thermodynamically stable as comparable hydrocarbons, more stable than metal hydrides and more

stable than graphene by ~0.15eV. This along with its large hydrogen storage capacity 7.7 wt%, which exceeds the DOE 2010 goal, also makes it an ideal candidate for hydrogen storage. The difficulty with forming graphane is the need for atomic hydrogen. Techniques implemented by other groups involve in situ development of atomic hydrogen by hydrogen plasma or pumping explosive gases into the furnace. These techniques are costly, dangerous and lack controllability needed for possible device applications. In this paper, we demonstrate an alternative electrochemical means to generate atomic hydrogen, simplifying the synthesis and controllability of graphane formation. On-axis, semi-insulating, 6H-SiC substrates were used to form epitaxial graphene at ~1400°C in vacuum as starting material for graphane production. The ratio of the graphene Raman G-peak to the disorder D-peak was >10, showing the high quality of the starting material. Atomic hydrogen was generated using a home-built electrochemical setup with current applied though a 10% sulfuric acid solution, with a Pt wire and exposed graphene as the anode and cathode, respectively. With this setup, H+ ions are attracted to the exposed graphene. Cyclic voltammetry, with a Hg_2SO_4 reference (0.67V vs. NHE) revealed that this conversion occurs at ~0.2V below the hydrogen evolution potential in water. Using the potential thus determined, conversion to graphane was performed until the conductivity of the graphane decreased to unmeasurable levels. This conversion was confirmed using graphane's known Raman peaks. As expected, there was a sharp increase in the D peak as well as a red shift in the peak from 1340cm^{-1} to 1330cm^{-1}, likely caused by the formation of sp^3 bonds. Another peak at ~2930cm^{-1} was an indication of C-H bonds. A fluorescence background, along with increased SiC substrate signal was also observed in the working area, suggesting the presence of a bandgap in the material. This conversion was distinguished from lattice damage by reversal back to graphene by annealing in argon for 4 hours at 1000°C. The Raman spectra of the area after reversal clearly shows disappearance of the C-H peak at ~2930cm^{-1} showing desorption of hydrogen in the material. The D peak shifted back to pre-conversion state at 1340cm^{-1} and fluorescence background was no longer present. While the D and G peaks shifted back to pre-conversion positions, their intensities show that there was some residual damage most likely caused by the strain of the hydrogenation. The conductivity of the graphane samples increased by ~100-1000x from pre-conversion graphene levels, without significant degradation of surface morphology, increase in roughness from 1.04nm to 1.62nm. Further optimization is expected to reduce this residual damage.

10:00 AM Break

10:20 AM

M5, Growth of Few Layer Graphene on C-Face SiC: *Virgil Shields*[1]; MVS Chandrashekhar[1]; Shriram Shivaraman[1]; Michael Spencer[1]; Gary Tompa[2]; Nick Sbrockey[2]; [1]Cornell University; [2]Structured Materials Industries, Inc.

Growth of few monolayer graphene on (0001-bar) SiC has been achieved using a slow cooldown temperature technique. Normal growth on (0001-bar) SiC results in relatively thick graphene comprised of a large number of folds and pores that penetrate the layers compared to thinner (0001) face growth having virtually no folds or pores. The presence of the folds and pores can negatively affect the graphene electrical characteristics and impair potential device performance. This process has resulted in a significant reduction in thickness, folds and pores making the (0001-bar) surface comparable to the (0001) surface. On-axis semi-insulating 6H-SiC was used for graphene growth by thermal decomposition. The surfaces of the SiC substrates were CMP polished only and not hydrogen etched. The (0001-bar) SiC graphene layers were grown at an ultimate temperature of about 1400°C for 30 minutes at a vacuum pressure in the upper 10^{-6} torr range. The process included a rapid increase to the growth temperature in two steps and a slow cooldown rate of less than 10°C per minute from the point of growth. Using this process, a reduction in surface roughness from about 23nm (without slow cooling) to less than 2nm (with slow cooling) was achieved. AFM and Raman data was used to determine the thickness of the graphene layers. The morphology was observed to be comparable to that of few monolayer (less than four) graphene on the (0001) SiC face.

10:40 AM

M6, Graphene Growth on SiC, SiO_2, and Sapphire with Carbon Addition: *Jeonghyun Hwang*[1]; Virgil Shields[1]; Chris Thomas[1]; Shriram Shivaraman[1]; Dong Hao[1]; Moonkyung Kim[1]; Michael Spencer[1]; [1]Cornell University

In this study, we report growth of graphene/graphite on SiC, SiO_2, and sapphire using carbon addition technique. The growths were carried out in a conventional cold wall CVD reactor which has been used for SiC epitaxy. On-axis 6H-SiC, SiO_2 on SiC, and sapphire (0001) substrate were heated up (1250°C to 1650°C) under Ar environment (100 to 600 Torr), and propane (C_3H_8) was supplied as a carbon source. The propane was provided as a mixture form (10% propane in Ar) and was thermally cracked at the growth temperature. Typical growth time was 3min to 10min. Raman spectroscopy with 488nm laser was employed to characterize the grown graphene/graphite. Raman spectra clearly showed the signature of multilayer graphene or graphite; G-peak (~1580cm^{-1}) and 2D-peak (~2700cm^{-1}). Also, disorder related D-peak (~1350cm^{-1}) was observed and the ratio of the intensity of D-peak and G-peak (I_D/I_G) varied depending on growth condition. Thickness of graphene was estimated based on the attenuation of Raman signal of substrate. In contrast to thermal decomposition of SiC in which the number of graphene layer is limited by Si evaporation, this carbon addition technique allowed multi-layer graphene or graphite formation on both the Si-face and C-face SiC, and also on SiO_2 and sapphire. The thickness (from 3 monolayer to ~100 monolayer) could be controlled by growth time, propane flow rate, and growth temperature. Thickness increased linearly after first ~3min, but the initial nucleation and growth dynamics are still under investigation. As the flow rate of mixture (propane + Ar) increased from 10sccm to 40sccm, the thickness of graphene increased linearly. The thickness and growth temperature showed exponential relation and this could be explained by propane cracking efficiency. The I_D/I_G decreased from ~0.7 to ~0.4 when growth chamber pressure was 100Torr, as growth temperature increased from 1350°C to 1650°C. By increasing the chamber pressure to 600Torr, the I_D/I_G ratio improved significantly. The ratio decreased to ~0.1 on all the SiC, SiO_2 and sapphire substrate at 1650°C. This indicates that crystallization at high temperature with reduced surface evaporation or decomposition is important to get high quality material. To confirm this graphene or graphite formation is not induced by thermal decomposition on SiC, SiC was heated up under the same condition but without propane flow, which resulted in no signature of graphene/graphite by Raman spectroscopy. Hall measurements with Van der Pauw geometry showed ~100 cm^2/Vsec mobility with 3~4E14 cm^{-2} sheet carrier (electron) density in 5mmx5mm sample. More growth optimization and material characterizations (such as TEM and X-ray) will be performed and presented. Also, growth with different hydrocarbon gas (Acetylene, Ethylene, and Methane) will be investigated and compared.

11:00 AM

M7, Ultrafast Transient Absorption Microscopy Studies of Carrier Dynamics in Epitaxial Graphene: *Libai Huang*[1]; Gregory Hartland[1]; Li-Qiang Chu[1]; L Luxmi[2]; Randall Feenstra[2]; Chuanxin Lian[1]; Kristof Tahy[1]; Huili Xing[1]; [1]University of Notre Dame; [2]Carnegie Mellon University

Energy exchange between the electrons and phonons is particularly important to electron transport, and understanding this process will be vital for the realization of future graphene-based electronics. Epitaxial growth is a very promising approach for practical applications, as it has the ability to prepare graphene on a large scale and supported on a substrate. However, epitaxially grown graphene is highly inhomogeneous, with variations in the sample thickness occurring over length scale of a few micrometers. It is also not clear how substrate interactions affect the carrier dynamics. To pave the road for electronic devices based on epitaxial graphene, characterization methods with high spatial resolution are needed to understand these effects. Here we present transient absorption microscopy as a novel tool to characterize graphene, and to interrogate the charge carrier dynamics. This technique has the ability to directly image carrier dynamics with a diffraction-limited spatial resolution and a time resolution of ~ 200 fs. The intensity of the transient absorption signal is shown to correlate with the number of graphene layers. The carrier cooling exhibits a bi-exponential decay, consisting of an instrument-response limited fast decay time t1 (< 0.2 ps) and a slower decay time t2. The value of t2 was found to increase

with increasing pump fluence. The fast decay is assigned to coupling between the electrons and optical phonons in graphene, and the slower decay is attributed to the hot phonon effect. At high pump intensities the slow decay reaches a limiting value, which is assigned to the relaxation time of the optical phonons. The contribution of the slow component to the overall decay was found to vary with spatial position in the sample. This is attributed to differences in coupling between the graphene and the substrate. Transient absorption images at different delay times also reveal variation in optical phonon lifetime that was not related to graphene thickness. These results point to transient absorption microscopy as a potentially important tool for characterizing the electrical conductivity of graphene through measurement of the lifetime of optical phonon modes excited by charge carrier relaxation.

11:20 AM

M8, Comparison of Graphene Thickness Determination for MBE Grown Graphene on SiC Using Raman, XPS, and TEM: *David Tomich*[1]; John Boeckl[1]; Jeongho Park[1]; John Hoelscher[1]; Larry Grazulis[1]; Kurt Eyink[1]; Chip Claflin[1]; William Mitchel[1]; [1]Air Force Research Laboratory

Graphene's exponential rise in interest since its isolation by Geim et al. in 2004 has led to a plethora of publications using different techniques to determine the number of graphene layers present. The techniques range from the very quick and simple optical interference microscopy for exfoliated graphene on SiO2/Si substrate to the tedious and time consuming sample preparation for Transmission Electron Microscopy (TEM) for sublimation grown graphene on SiC. Raman spectroscopy is one of the most reported tools used to determine graphene thickness due to its ease of use, non-destructive nature and wide availability. Raman spectroscopy has been used extensively over the past few decades to study carbon based materials, so the study of this perfect two dimensional form of carbon with Raman is a natural application. Several methods have been used to glean information from the Raman spectrum to relate the number of layers or quality to the electronic properties. We have examined several of these methodologies along with photoelectron spectroscopy and TEM in order to determine an accurate, consistent and rapid process to guide our graphene growth experiments. We have examined x-ray photoelectron spectra (XPS), confocal Raman spectra and TEM images from portions of the same sample in an effort to determine the relative accuracies of these techniques. Growths were conducted in an EPI (Veeco) 930 MBE tool with a modified graphite heater to facilitate growth temperatures up to 1600°C. Films were grown on the chemical-mechanical polished (CMP) Si-face of 6H SiC semi-insulating substrates diced into 10 x 10 mm2 samples. Atomic force microscopy images of the growths indicate good step flow growth with RMS roughness less than 5 nm over 20 x 20 µm2.

11:40 AM

M9, Late News

Session N: Molecular Electronics and Chem / Bio Sensors

Thursday AM
June 24, 2010

Room: 126
Location: University of Notre Dame

Session Chairs: Takhee Lee, Gwangju Institute of Science and Technology; Jay Gupta, Ohio State University

8:20 AM

N1, STM Studies of Hybrid Inorganic-Organic Molecular Magnets on an Ultrathin Insulating Film: *Taeyoung Choi*[1]; Jay Gupta[1]; [1]Ohio State University

The interplay of electronic structure and magnetic properties has been of interest in various organic materials. For example, transition metal -- tetracyanoethylene (TCNE) complexes form a family of organic magnets with Curie temperatures exceeding room temperature. TCNE has a strong electron affinity that facilitates chemical bond formation and charge transfer with metals. However, the chemical bonding and its influence on electronic and magnetic properties is not well understood at the atomic scale. We use scanning tunneling microscopy to build Co-TCNE and Fe-TCNE complexes with atomic manipulation on an ultrathin insulating layer (Cu2N on Cu(100)). Cu2N decouples the complexes from the conducting substrate, which impacts their electronic and magnetic properties. Tunneling spectroscopy on the complexes shows molecular orbitals and inelastic steps due to various vibrational modes and spin excitations. The degree of charge transfer between single magnetic atoms and molecules could explain the observed difference in energies of these steps among the complexes. The ability to connect such complexes with additional metal atom chains provides an opportunity to study spin and charge transport through single molecules with atomically precise contacts.

8:40 AM Student

N2, Effect of Molecular Tilt Configuration and Interface Dipoles on Molecular Electronic Conduction: *Gunuk Wang*[1]; Tae-Wook Kim[1]; Jamin Ku[1]; Seok-In Na[1]; Gunho Jo[1]; Yonghun Kim[1]; Yun Hee Jang[1]; Dong-Yu Kim[1]; Takhee Lee[1]; [1]GIST

Controlling the charge transport characteristics through molecules between electrodes is important for understanding basic conduction mechanism and realizing potential device applications of molecular electronic systems. The charge transport characteristics in molecular junctions are influenced by molecular structure, metal-molecule contact, conformational effect, and energy level alignment of molecular orbitals with the Fermi levels of the electrodes[1,2]. We investigated the effect of the molecular configuration on the electronic transport in molecular junctions where the molecular configuration is controlled by conducting atomic force microscopy (CAFM)2. Our results indicate that the degree of tilting of alkanemonothiol molecules enhances chain-to-chain intermolecular charge transfer, so called through-space tunneling. We will show inflection points on a plot of ln (J/V2) vs 1/V with various tip-loading force of CAFM, consistent with the transition of the electronic transport mechanism from direct tunneling to Fowler-Nordheim tunneling[3]. Also, we will discuss recent results about the energy level alignment of molecular electronic devices with organic interlayer (PEDOT:PSS) by interface molecular dipoles. We demonstrate that the molecular orbital levels relative to the electrode's Fermi level shift to higher or lower energies according to the direction of the dipole moments at the junction interface when the junction temperature is increased. [1] G. Wang et al. Phys. Rev. B 76, 205320 (2007). [2] G. Wang et al. J. Am. Chem. Soc 131, 5980 (2003). [3] J. M. Beebe et al. Phys. Rev. Lett. 97, 026801 (2006).Acknowledgement: the National Research Laboratory Program, the National Core Research Center grant, the World Class University program of the Korean Ministry of Education, Science and Technology of Korea, and the Program for Integrated Molecular System at Gwangju Institute of Science and Technology.

9:00 AM Student

N3, Improvement of Transfer Characteristics in Carbon Nanotube Field-Effect Transistors with Au Nano Clusters: *Yasuki Yamamoto*[1]; Yasuhide Ohno[1]; Kenzo Maehashi[1]; Kazuhiko Matsumoto[1]; [1]Osaka University

During the past few years, carbon nanotubes (CNTs) have emerged as highly promising components of nanoscale electrical and electrochemical devices. In particular, carbon nanotube field-effect transistors (CNTFETs) have been extensively studied and have been expected for the highly sensitive and label-free biosensors. To increase sensitivity of CNTFET sensors, many unique techniques have been developed. Recently, CNTFETs decorated with metal particles has attracted strong interest. In device fabrication process, the method of depositing metal particles over the entire surface of CNTFETs is usually used. However, the current reduction and noise increase due to the induced defects and screening effect are crucial problems. In this study, we report the marked improvement of transfer characteristics in CNTFETs decorated with Au nano clusters. A decoration process of Au nano clusters was optimized, and additional electrical heating process was adopted to improve transfer characteristics. CNTs were synthesized on Si wafer covered with thermally grown SiO_2 layer via chemical vapor deposition method using patterned Co catalyst with ethanol as a source gas. After the growth of CNTs, 3-Å-thick Au nano clusters were deposited onto

entire device using an electron beam evaporator. Finally, 1 nm Ti and 40 nm Au pads as source and drain electrodes were formed. The channel length of devices was 3µm. Following the device fabrication, the electrical heating process was carried out. CNTFETs with Au nano clusters were electrically annealed by applying high voltage between source and drain electrode at the fixed back-gate voltage of 10 V. This electrical heating process affects the transfer characteristics in CNTFETs strongly. The marked increase in the drain current and improvement of transconductance were observed after the electrical heating process. This improvement in transfer characteristics by electrical heating was not observed in CNTFETs fabricated by conventional Au-decoration process. Therefore, this phenomenon was attributed to the combination of proposed structure and electrical heating process. It is expected that our CNTFETs with Au nano clusters are useful for sensor application.

9:20 AM

N4, Carbon Nanotube Field-Effect Transistor Biosensor with Schottky Barrier Control Gate Electrode: *Masuhiro Abe*[1]; Katsuyuki Murata[2]; Kazuhiko Matsumoto[3]; [1]National Institute of Advanced Industrial Science and Technology; [2]Core Research for Evolutional Science and Technology, Japan Science and Technology Agency; [3]The Institute of Scientific and Industrial Research, Osaka University

The carbon nanotube field-effect transistor (CNT-FET) is expected to be used in several applications. In particular, CNT-FET-based biosensors have been attracted because of its high sensitivity and stability. We have established CNT-FET biosensor and have succeeded detecting proteins [1, 2] and have clarified that the structure of the CNT-FET influenced the sensitivity of the biosensors [3]. In this study, we newly prepared a new structured CNT-FET for a biosensor. The performance as the biosensor of the new CNT-FET was compared with our traditional CNT-FET. In our new structured CNT-FET, the CNT channel is covered by insulator, and the gate electrode is placed above the interface of CNT channel and source-drain electrode. On the other hand, in our traditional CNT-FET, gate electrode is placed all round under the insulator. By using the new CNT-FET, Schottky barrier between the CNT channel and the source-drain electrode is independently controlled at the CNT-FET. In this paper the gate electrode of the new structured CNT-FET is called “Schottky gate electrode”. The Schottky gate voltage affected only the interface between CNT channel and drain source electrode and not effected the part of CNT under the sensing area of the CNT-FET biosensor. Therefore, the biosensor of the new CNT-FET has a possibility that have higher sensitivity than our traditional one. For the measurement, a silicone rubber pool was placed around the sensing area of the CNT-FET. 0.1 M Tris buffer (pH = 8.0) was poured onto the CNT-FET and drain current was measured. Drain voltage, electrolyte voltage and Schottky gate voltage were controlled during the measurement. The dependence of the drain current (ID)-electrolyte gate voltage (VEG) properties on the Schottky gate voltage (VSG) was measured. The transconductance at VD = 0.1 V and VEG = +0.4 V were 22.6 nS, 7.6 nS and 4.7 nS when Schottky gate voltage were VSG = +3 V, VSG = 0 V and VSG = -3 V, respectively. Therefore we succeeded in controlling current properties of CNT-FET in the solution by controlling Schottky barrier of CNT-FET. [1] M. Abe, K. Murata, A. Kojima, Y. Ifuku, M. Shimizu, T. Ataka, and K. Matsumoto: J. Phys. Chem. C, 111 (2007) 8667. [2] M. Abe, K. Murata, T. Ataka, and K. Matsumoto: Nanotechnology, 19 (2008) 551. [3] M. Abe, K. Murata, T. Ataka, and K. Matsumoto: J. Appl. Phys., 104 (2008) 104304.

9:40 AM Student

N5, Breakdown Statistics and Nanowire Device Integration of Self-Assembled Nano Dielectrics: *Ruth Anne Schlitz*[1]; KunHo Yoon[1]; Sara Renfrew[1]; Lisa Fredin[1]; Young-Geun Ha[1]; Tobin Marks[1]; Lincoln Lauhon[1]; [1]Northwestern University

Self-Assembled Nano Dielectrics (SANDs) are high-K molecular dielectrics grown by low-temperature solution processes. They offer great potential to enable high-performance electronics on unconventional substrates that are incompatible with the harsh conditions of conventional semiconductor processing. Furthermore, they have already been incorporated into a variety of devices incorporating both inorganic and organic components. However, if SANDs are to be scaled up successfully, they must have two characteristics: (1) they must be uniformly pinhole free on the scale of the device channel and (2) they must retain properties after device fabrication and processing. To this end, we present a failure analysis of SANDs, utilizing Weibull statistics to empirically determine a critical defect density in SANDs. Our quantitative failure analysis correlates synthesis conditions to the resultant Weibull slopes; typical ß values found are between 3 and 15. By comparison, reported ß values for other inorganic high-K dielectrics are on the same order, with reported values for many dielectrics typically less than 5, but as high as 14.4 for HfO2. Our studies of processing conditions qualitatively show the effects of post-synthesis processing on the SAND; while electron-beam lithography slightly degrades the performance of SAND, the resultant leakage current densities still compare favorably with inorganic dielectrics. Surprisingly, high-temperature anneals up to 400°C reduce the leakage current densities through the SAND and widen the range of processing conditions possible for a SAND device. We will discuss how the synthesis conditions of the SAND and subsequent processing of the parallel-plate capacitors used for the measurement influence the characteristic breakdown behavior. We also correlate these statistics with film morphology and capacitance. Finally, we present results from SAND integrated as a top gate dielectric in silicon nanowire transistors.

10:00 AM Break

10:20 AM

N6, Functionlization Studies on GaN Nanowires: *Devin Rourke*[1]; Christopher Dodson[1]; Aric Sanders[1]; Kristine Bertness[1]; Norman Sanford[1]; [1]NIST Boulder

We have fabricated and tested GaN nanowire bioFETs utilizing amine-reactive surface chemistry, and taken electrical measurements at various stages throughout the functionalization process. Test structures were fabricated with nanowires grown on Si with MBE. GaN nanowires were released into a suspension via ultrasonic agitation, pipetted onto pre-deposited Ti pads and aligned with dieletrophoresis, forming a two-terminal bridge structure. A capping layer of Ti/Al pins the wires to the substrate and forms two conformal electrical contacts. From this point, the most critical requirements for nanowire-based bioFET fabrication are electrical stability and effective surface functionalization. We have demonstrated the electrical stability of these two-terminal GaN nanowire bridge structures when submerged in solutions of pH 1, 4, 7 and 10. We attribute this stability to the inert, chemically robust GaN crystal structure. In addition, leakage current through the solutions was found to be approximately 1nA which is on average 10^5 times less than the current through the nanowire device. We demonstrate via fluorescence microscopy the amine-reactive surface functionalization of GaN nanowires. The preparation scheme utilizes successive wet chemical treatments, allowing on-chip functionalization of pre-fabricated bridge-type nanowire structures. We present strong evidence that piranha etch increases the concentration of reactive hydroxyl groups on the nanowire surface, increasing conjugation of methyl-terminated silane molecules (aminopropyltrimethoxysilane [APTMS]). We have collected I-V data from devices before and after silanization which indicate a 1.5x resistance increase with the deposition of silane. An amine-reactive rhodamine-derivative fluorescent dye is then reacted with the silane molecule, allowing for fluorescence imaging using a confocal scanning laser microscope (CSLM). The degree of functionalization is quantified by the intensity of fluorescence, calculated using selective area image processing and reported as pixel counts above background. We have thus demonstrated an electrically stable, amine-reactive, GaN nanowire-based device structure suitable for bioFET development. The photolithography process allows for integration into massively arrayed IC devices, and on-chip, post-processing functionalization provides flexibility of choice between other functionalization schemes yet to be developed.

10:40 AM Student

N7, Olefin Metathesis Reaction on GaN (0001) Surfaces: *Matthew Makowski*[1]; Dmitry Zemlyanov[2]; Albena Ivanisevic[1]; [1]Weldon School of Biomedical Engineering, Purdue University; [2]Birck Nanotechnology Center, Purdue University

An essential step towards designing new and versatile biosensors is to validate new methodologies for the attachment of biomolecules to the surface.

Gallium nitride (GaN) offers a number of promising properties for novel microfabricated sensors. A surface modification scheme was characterized using X-ray Photoelectron Spectroscopy (XPS) to adapt GaN for use in biosensors. Wafers of undoped GaN (0001) on sapphire were etched in boiling 2 M KOH for 5 minutes to remove the oxide layer. The exposed gallium atoms on the surface were covalently bound to hydrogen through a hydrogen plasma treatment. The wafers were subsequently passivated with chlorine in a solution of phosphorus pentachloride and benzoyl peroxide in chlorobenzene at 90°C for 30 minutes. An alkene termination on the surface was then achieved in 2 M allylmagnesium chloride in tetrahydrofuran at 55°C for 30 minutes. The surfaces were next primed for olefin metathesis by 13.8 mM first generation Grubbs catalyst in dichloromethane at 35°C for 30 minutes. The first run of the scheme resulted in the binding of an amine group by olefin metathesis through 0.5 M allylamine in dichloromethane at 35°C for 30 minutes. The second run consisted of 0.5 M 7-bromo-1-heptene in dicholoromethane at 35°C for 2 hours. The bromine served as a label for XPS to verify the binding of the hydrocarbon to the surface. A microfluidic chip composed of polyetheretherketone was constructed and implemented for the alkene termination, Grubbs priming and olefin metathesis reactions. This resulted in a decrease in reagent volumes and wafer handling. Following each surface termination step, XPS analysis identified the chemical species at the surface. The absence of a shoulder on the Ga 2p peak for the chlorine-terminated and bromine-terminated samples indicates that no substantial oxidation of the surface occurred following the passivation with chlorine and throughout the duration of the scheme. The Cl 2p spectrum is composed of a pair of doublet peaks. Gallium to chlorine bonds produced the doublet with the greater binding energy. The peak within the C 1s spectrum at 280.9 eV signifies the presence of the ruthenium within the Grubbs catalyst following the priming of the surfaces with the olefin metathesis catalyst. The single Br 3d peak indicates the presence of bromine on the GaN surface following the linkage of 7-bromo-1-heptene via olefin metathesis. The final bromine surface coverage was 4.0% of a monolayer. The demonstrated scheme is greatly versatile due to the Grubbs catalyst allowing for a wide variety of alkene-terminated molecules to covalently bind to the GaN surface via olefin metathesis. Future applications of this scheme toward the development of novel biosensors include the binding of peptides, proteins, or antibodies to GaN electronic devices.

11:00 AM Student

N8, Protection of ZnO Nanowires for Liquid-Phase Sensing: *Ashley Mason*[1]; Chien-Chih Huang[1]; Saki Kondo[1]; Myra Koesdjojo[1]; Vincent Remcho[1]; John Conley[1]; [1]Oregon State University

The use of metal-oxide nanowires (NWs) for sensing applications has become a highly active area of research in recent years as the high surface to volume ratio of NWs promises increased sensitivity to a target species. There are many challenges to NW sensing. Important considerations include the problem of device formation using cylindrical NWs and sensor selectivity, sensitivity, stability. High yield fabrication of NW devices and sensors requires alignment of the NWs to previously patterned lithographic features. In this work, directed growth and integration of ZnO nanobridge devices into an electrically accessible three-terminal device structure was achieved using photolithographically pre-patterned carbonized photoresist (C-PR) without the use of a metal catalyst, seed layer, or "pick and place". Electrical measurements of three-terminal field effect NW devices indicate bottom gate modulation of the conductivity of the n-type channel and Schottky type contact between the C-PR and the ZnO nanobridges. We demonstrate that these devices exhibit good ultraviolet (UV) sensitivity and gas phase sensitivity to O2 and humidity. In order to demonstrate selectivity, the strong bonding between biotin and streptavidin can be exploited. The functionalization of ZnO NWs with biotin is mainly controlled by the pH, with deionized (DI) water used as a carrier medium for the biomolecules. However, it is known that ZnO is soluble in H2O and we find that biotin coated ZnO NWs are dissolved completely within 24 hours. Demonstration of selective sensing using ZnO NWs in the liquid phase therefore requires a way to prevent the ZnO from dissolving. In this work, we examine ways to protect ZnO nanowires (NWs) during liquid-phase sensing. We demonstrate a possible coating used to protect the ZnO NWs during submersion in DI water. In one experiment, the contact angle of a DI water droplet was measured as a function of time for ZnO NWs functionalized with either biotin or or the protective coating. While the biotin coated sample exhibited a small contact angle immediately after the H2O droplet was applied, the protected ZnO NW samples showed strong a hydrophobic property. In another experiment, biotin and protected ZnO NW samples were soaked in DI water for 24 hours and monitored via dark-field microscopy. Whereas the biotin coated NWs were dissolved overnight, the protected NWs appeared to remain unchanged. ZnO nanobridge devices with the additional protective coating will be characterized for sensitivity to UV and O2. Demonstration of liquid-phase selective sensing is still underway.

11:20 AM Student

N9, Signal-to-Noise Ratio Improvement of Magnetoelectric Laminate Sensor by Multilayer Structure and Direct Integration with Advanced Microelectronics: *Zhao Fang*[1]; Ninad Mokhariwale[1]; Feng Li[1]; Suman Datta[1]; Qiming Zhang[1]; [1]The Pennsylvania State University

Magnetoelectric (ME) effect is the appearance of an electrical signal upon applying a magnetic field H and/or the appearance of a magnetic signal upon applying an electric field E. This has attracted a lot of interest because the materials featuring the ME effect have potential to be used as high sensitivity magnetic sensors, electrical current sensors, and other devices. Although the ME effect was first observed in single phase materials (e.g. Cr2O3), the composite laminates of the magnetostrictive layer (e.g. Terfenol-D and Metglas) and the piezoelectric layer (e.g. Pb(ZrTi)O3 (PZT), Pb(Mg1/3Nb2/3)O3-PbTiO3 (PMN-PT), and Polyvinylidene fluoride (PVDF)) have attracted much attention due to the strong coupling effect between the magnetostrictive and piezoelectric layers, which derive large ME response at room temperature. The principle of composite laminates is that a magnetic field induces a strain in the magnetostrictive layer by magnetostriction, and the strain is coupled to the piezoelectric layer, resulting in an electric polarization. Strain coupling requires suitable combination of magnetostrictive and piezoelectric layers for efficient displacement transfer. Among the ME composite laminates which exhibit large ME coupling coefficients, the ones with Metglas are particularly attractive due to their low saturation magnetization field and consequently a relatively low dc bias magnetic field (<20 Oe), which is highly desirable for high sensitivity magnetic sensors. In this paper, Metglas and PVDF are used as the magnetostrictive and piezoelectric layers respectively. To realize the applications for medical and life science research, it is desirable for ultra sensitive magnetic sensors to be highly sensitive, miniaturized, low-cost, and easy to operate. Successful exploitation of magnetic sensors is often inhibited by the presence of large volume of sensors and parasitic effects such as environmental noise and parasitic capacitances. In order to mitigate these problems, it is important to integrate the magnetic sensor with the signal conditioning circuitry as directly as possible. To obtain the electric signal from the piezoelectric layer, a custom-made charge mode read-out circuit is used to maximize the signal-to-noise ratio (SNR) and avoid the effect of stray capacitances. For charge mode read-out circuit, the noise analysis shows that the SNR is proportional to the square root of capacitance of the piezoelectric layer, which is confirmed by the experimental results in this paper. A multilayer structure for the piezoelectric layer is employed to increase the sensitivity without increasing the size of the sensor. Since the elastic modulus of Metglas (100-110 GPa) is much higher than that of PVDF (1-3 GPa), it's possible for one Metglas layer to drive multiple PVDF layers. Also the SNR for the custom-made charge mode read-out circuit is compared with that of a commercial charge amplifier.

11:40 AM

N10, Late News

Session O, SiC: Characterization and Growth

Thursday AM
June 24, 2010

Room: 129
Location: University of Notre Dame

Session Chairs: Robert Stahlbush, Naval Research Laboratory; Brett Hull, Cree, Inc.

8:20 AM

O1, Analysis of Dislocation Interactions in Low Dislocation Density, PVT-Grown, Four-Inch Silicon Carbide Single Crystals: *Michael Dudley*[1]; Balaji Raghothamachar[1]; Shayan Byrappa[1]; Gloria Choi[1]; [1]State University of New York at Stony Brook

Synchrotron White Beam X-ray Topography studies are presented of dislocation behavior and interactions in a new generation of one hundred millimeter diameter, 4H-SiC wafers grown using Physical Vapor Transport under specially designed low stress conditions. Such low stress growth conditions have enabled reductions of dislocation density by two or three orders of magnitude compared to the lowest previously reported levels. For example, detailed analysis of transmission geometry topographs recorded from wafers ranging in thickness from four hundred to seven hundred microns demonstrates extremely low defect basal plane dislocation (BPD) densities of just a few hundred per square centimeter on average (these are "true" dislocation densities computed by dividing measured dislocation line lengths from transmission topographs by the imaged crystal volume). Lowering of dislocation densities to such levels provides a unique opportunity to discern the details of dislocation configurations and interactions which were previously precluded due to complications of image overlap at higher dislocation densities. Among the phenomena observed in these studies is the conversion of non-screw oriented glissile BPDs into sessile threading edge dislocations (TEDs). This is observed to provide pinning points for the beginnings of the operation of single ended Frank-Read sources. In some regions, once converted TEDs are observed to re-convert back into BPDs, most probably through overgrowth by macrosteps. This can occur repetitively in a process which provides multiple BPD pinning points. Detailed models for such behavior will be discussed in detail. Detailed topography analysis will also be presented of the deflection of other threading defects into the basal plane which produces complex faulted defect configurations. Models for the creation of such deflected defect configurations will be presented and discussed. The implications of such substrate defect configurations on subsequently grown homoepitaxial layers and the prospects for further defect density reduction to unprecedented levels for Physical Vapor Transport grown SiC will be discussed.

8:40 AM

O2, Formation of a (5-1)-Bilayer-Height Complex Step-and-Terrace Structure on 4H-SiC (0001) by a Spiral Etching Process: *Jun Suda*[1]; Tsunenobu Kimoto[1]; [1]Kyoto University

We found a very unique step-and-terrace structure on 4H-SiC (0001) surfaces after high-temperature gas etching. Commercially available 2-inch n-type 4H-SiC (0001) just-oriented Si-face substrates were subjected to high-temperature gas etching, which was carried out by using a low-pressure hot-wall chemical vapor deposition system. The etching conditions were as follows: 120 min etching at 1550°C with a hydrogen gas flow of 30 slm and pressure of 20 Torr. The unique step-and-terrace structure consists of a periodic array of pairs of 5-bilayer (BL)-height step and opposite-signed 1-BL-height step. The separation of 5-BL-height and 1-BL-height steps was 200 nm. We revealed that the "(5-1)-BL-height step-and-terrace structure" were continuously generated by a spiral etching process at a screw-type threading dislocation. At the center of spiral pit, one 4-BL-height step appeared, indicating that the threading dislocation has Burgers vector of 1c. However, at very near the center, the 4-BL-height step was decomposed into a 5-BL-height step and an opposite-signed 1-BL-height step. Note that total step height was conserved, i.e., 4 BL. The pair of 5-BL-height and 1-BL-height steps formed a spiral pit. At the outside of spiral pit, the periodic array of (5-1)-BL-height step pairs was observed. It should be noted that some of spiral pits on the same 4H-SiC substrate did not have such a complex structure. They consisted of double spiral of 2-BL-height step, which are generally observed on 4H-SiC (0001) surface after etching. The author also investigated spiral etching of 6H-SiC (0001). In the case of 6H-SiC, only double spiral of 3-BL-height step was observed. We concluded that the core structure of spiral pit is the key to form the unique step-and-terrace structure. A mechanism for step-flow etching which conserves the step pairs is also discussed.

9:00 AM

O3, Processes Controlling the Carrier Lifetime in n^- 4H-SiC Epilayers with Low $Z_{1/2}$ Concentrations: *Paul Klein*[1]; Rachael Meyers-Ward[1]; K.-K. Lew[1]; Brenda VanMil[1]; C.R. Eddy[1]; D.K. Gaskill[1]; A. Shrivastava[2]; T.S. Sudarshan[2]; [1]Naval Research Laboratory; [2]University of South Carolina

The ability to grow epitaxial layers of 4H-SiC with low concentrations of the Z1/2 defect, the bulk defect that limits the lifetime in this material, has resulted in measureable increases in the observed lifetimes. However, achieving the even longer lifetimes necessary for very high voltage switching devices and for lifetime control requires an understanding of the recombination processes that limit the carrier lifetime in these low-$Z_{1/2}$ materials. In this work, differences in the temperature dependence of the lifetime for different recombination mechanisms have been employed to identify the process that controls the carrier lifetime in these materials. The temperature dependence of the carrier lifetime was measured at low injection for several low-$Z_{1/2}$ epilayers over a wide temperature range and compared to simulations. The bulk lifetime is expected to be slow-varying until the temperature becomes high enough to thermalize carriers that are trapped on deep defects back into the bands. Then the lifetime increases in a thermally activated manner with temperature, with the activation energy reflecting the depth of the trap. Surface recombination was modeled based on existing approximations to the solution of the one dimensional diffusion equation, taking into account recombination at the sample surface and at the substrate/epilayer interface. The simulated carrier lifetime is the sum of terms due to carrier diffusion to the surface and carrier capture at the surface, so that the slowest mechanism is the rate-limiting process. Surface capture at low injection leads to a thermally activated decrease in the lifetime with temperature due to surface band-bending, while at higher temperatures the diffusive component dominates and results in a power-law increase in the lifetime, following the temperature dependence of the diffusion coefficient. Due to the existence of the space charge region formed at the n_+/n_- interface, minority holes are repelled from the interface and the corresponding surface recombination velocity is greatly reduced. The behavior of surface recombination at high injection levels becomes distinctly different, as the band bending at the surface and at the interface disappears when the system is driven into flat-band conditions. The experimental results are consistent with carrier lifetimes dominated by surface recombination. No significant contribution from other bulk defects was observed, and upper limits to the bulk recombination rate were determined to be consistent with the measured $Z_{1/2}$ concentrations in these materials. There was also no discernable contribution from carrier capture at the epilayer/substrate interface. These results were found to be consistent with behavior expected under low injection conditions for epilayers grown on n_+ substrates.

9:20 AM

O4, Comparative Studies of Carrier Dynamics in 3C-SiC Layers Grown on Si and 4H-SiC Substrates: *jawad ul hassan*[1]; Patrik Scajev[1]; Kestutis Jarasiunas[1]; Masashi Kato[2]; Anne Henry[3]; Peder Bergman[3]; [1]Vilnius University; [2]Nagoya Institute of Technology; [3]linköping University

Large lattice mismatch and different thermal expansion coefficient leads to high structural defect density in 3C-SiC layers grown on Si substrates (3C/Si). These extended defects severely deteriorate optical and electrical properties of the crystal. Heteroepitaxial growth of 3C on hexagonal 4H-SiC substrates (3C/SiC) could be beneficial to avoid growth induced extended defects and hence may result in superior crystalline quality. We performed comparative studies of optical properties and carrier dynamics in 3C-SiC layers grown on Si and SiC substrates using three optical techniques. 3C-SiC n-type layers (nitrogen doping ~ $1x10^{17}$ cm^{-3} and thickness of ~ 300 μm) were grown on undullant Si substrates and free standing 3C layers were obtained after mechanically

polishing away Si substrate. Low doped n-type layers (nitrogen doping ~ 1 x 10^{15} cm^{-3} and thickness of ~ 100 µm) were grown on nominally on-axis 4H-SiC substrates using horizontal hot-wall chemical vapor deposition reactor in Linköping university. Important electronic parameters for 3C-SiC, such as carrier lifetime, diffusion coefficient and diffusion length were determined using different optical techniques. These included light diffraction on transient free carrier grating (TG), free carrier absorption (FCA) and time-resolved photoluminescence (TRPL). The measurements were made over a wide range of excess carrier densities, $\Delta N = 10^{16} - 10^{19}$ cm^{-3}, and temperatures, T = 80 - 800 K. The carriers were excited by a frequency tripled Nd:YLF-laser at 351 nm. Low temperature photoluminescence spectroscopy was also performed to observe the purity of the material. PL spectra at 5 K revealed similar features in both layers over wide energy range. The near band edge emission was dominated by nitrogen-bound exciton recombinations while very weak DAP transitions were observed at lower energies. In contrary, FCA decay kinetics provided very different carrier lifetimes of 16 ns in (3C/Si) layers and 100 ns in (3C/SiC) layers at room temperature, thus indicating higher structural quality of on-axis grown 3C/SiC layers. We note a long lifetime of ~130 ns at the backside of free standing 3C/Si layers (nearby 3C/Si interface). A higher density of SFs has been reported in this region; however, the origin of so long lifetime in high SF density region is not known. In the 3C/SiC layers, the temperature dependence of carrier lifetime in 80-800 K range revealed non-monotonous increase of lifetime from ~50 ns to ~300 ns. The TG decay times in both layers revealed similar D(T) dependences in 80-800K range, with bipolar mobility values of 140-160 cm^2/Vs at RT. The mobility and lifetime data in 3C/SiC layers provided carrier bipolar diffusion length of ~6.5 µm and hole diffusion length of ~4.5 µm, being the largest values reported up to now for 3C.

9:40 AM

O5, Expansion and Contraction of Stacking Faults in 4H-SiC: *Nadeemullah Mahadik*[1]; Robert Stahlbush[1]; Joshua Caldwell[1]; Karl Hobart[1]; [1]Naval Research Laboratory

Silicon Carbide (SiC) power devices such as p-i-n diodes, gate turn off thyristors, and bipolar junction transistors are known to have serious forward voltage degradation due to the expansion of Shockley type stacking faults (SSF) created by basal plane dislocations (BPD) in the 4H-SiC epilayers [1,2]. Initially, it was thought that these SSFs only expanded and never contracted in power devices. Recently, a contraction of SSFs was observed [3] at operating temperatures in these power devices, with application of low current bias. The mechanisms governing the expansion and contraction of these stacking faults is complex. In this work, we have utilized a recently developed [4], non-destructive ultra-violet photoluminescence (UVPL) mapping technique to investigate the expansion/contraction of SSFs from individual BPDs instead of clusters of BPDs. For this we used 20 um thick, 4H-SiC epilayers, grown on 4H SiC substrates, which were cut 8° off-axis towards the [11-20] direction The motion of SSFs was generated by stressing the faulted regions under variable UV laser intensities. The UVPL measurements were carried using an argon ion UV laser, with principle UV excitation lines at 364 nm and 351 nm and images were collected in the 600 to 1000 nm range. Focusing lenses were used to vary the laser light intensity at the imaged regions. A sequence of images from the faulted region under UV exposure was obtained using a computed controlled, liquid nitrogen cooled CCD detector mounted on the probe station. All the measurements were done at room temperature. Using this technique, we were able to obtain real time, in-situ images to investigate changes in SSFs and their bounding partials originating from individual BPDs. The timed sequence of exposures were started under high laser power intensity (~1-2 $x10^{-3}$ $W/\mu m^2$) in order to expand the SSFs and observe motion of the bounding partials. Following this, a next set of UV exposures at lower power (~1-2 $x10^{-5}$ $W/\mu m^2$) was performed. The images observed, for the first time, show the contraction of individual SSFs and a reverse motion of the bounding partials. The motion of SSFs and the bounding partials during expansion and contraction of the SSFs are found to be different and will be discussed in the presentation. [1] J. P. Bergman, et. Al, Mater. Sci. Forum 353-3 (2000) 299; [2] R. E. Stahlbush, et. Al, Mater. Sci. Forum 389 (2002) 427; [3] J. D. Caldwell, et. Al, Appl. Phys. Lett. 90 (2007) 143519; [4] R. E. Stahlbush, et. Al, Mater. Sci. Forum 556-557 (2007) 295.

10:00 AM Break

10:20 AM

O6, Influence of Stacking Fault Generation and Half Loop Array on Electrical Behavior of 4H-SiC 10 kV PiN Diodes: *Qingchun (Jon) Zhang*[1]; Anant Agarwal[1]; Robert Stahlbush[2]; Charles Scozzie[3]; Albert Burk[1]; Michael OLoughlin[1]; [1]CREE; [2]Naval Research Laboratory; [3]Army Research Laboratory

The influence of stacking fault (SF) generation on the reverse blocking and reverse recovery characteristics has been investigated on SiC 10 kV, 1 A PiN diodes. For the first time, we have observed that the generation of SFs under forward biased stress increases the reverse leakage current, and reduces the stored charges. The SiC PiN diode was made on a 125 µm-thick SiC drift layer with Nd = $5\text{-}6\times10^{14}$ cm^{-3}. Aluminum ion-implantation was used to form the P^+N junctions. Multiple-zone JTE was implanted by Boron around the device periphery. The PiN diodes with different BPD densities and half loop array (HLA) density were selected and stressed with 1 A DC (~30 A/cm^2) flowing such that the implanted P^+N junction was forward biased. The forward and reverse I-V characteristics and reverse recovery performance were measured before and after electrical stress. The diode made on a high BPD density material has shown a significant forward voltage drop increase after electrical stress as shown previously. More significantly, the reverse leakage current was dramatically increased and the breakdown voltage was decreased. A reduced stored charge after stress was observed from reverse recovery tests before and after stress with the same forward current, which indicates a carrier lifetime reduction. On the contrary, the PiN diode made on BPD-free material didn't show any degradation in all electrical characteristics. The effect of the presence of half loop arrays will also be investigated. More data and detailed analysis will be presented in the full paper. This research was funded through the Cooperative Agreement W911NF-04-2-0022 program supported by the Army Research Laboratory in Adelphi, Md.

10:40 AM

O7, Reducing Basal Plane Dislocation Density in Nitrogen and Aluminum Doped 4H-SiC Epilayers: *Virginia Wheeler*[1]; Brenda VanMil[1]; Rachael Myers-Ward[1]; Charles Eddy[1]; Robert Stahlbush[1]; Nadeemullah Mahadik[1]; D. Kurt Gaskill[1]; [1]Naval Research Laboratory

Silicon carbide (SiC) is a promising material for high-temperature, high-voltage, and high-power switching applications. However, extended defects propagating from the substrate into the epitaxially grown active regions of these bipolar devices still limit device reliability and performance. Basal plane dislocations (BPDs) are of particular concern since they act as nucleation sites for Shockley-type stacking faults, which can cause degradation in minority carrier lifetimes and forward voltage drifts [1]. Several methods have been investigated to reduce the BPD density in epilayers on 8° off-cut wafers including KOH etching prior to growth [2,3], varying growth parameters [4], and *ex-situ* or *in-situ* growth interrupts [5,6]. Previous studies showed that *in-situ* growth interrupts notably enhance the BPD to TED conversion in low-doped n-type SiC layers, but for power devices it is critical to have BPD mitigation in the n^+ buffer layer to prevent any deleterious effects from SF formation in forward bias operation. This work investigates the effect of nitrogen and aluminum doping on the BPD to TED conversion efficiency. Epitaxial layers were grown in an Aixtron/Epigress VP508 horizontal hot-wall reactor on n^+ 4H-SiC substrates off-cut 8° toward the <11-20> direction. All films investigated were deposited using a standard silane (2% SiH_4 in H_2) and propane (C_3H_8) chemistry at 1580°C and 100 mbar pressure. Previous studies showed that a high BPD conversion efficiency could be obtained using an *in-situ* 45 min. growth interrupt at 1580°C with 10 sccm of propane [6]. For this work, the optimized growth interrupt was employed in a series of unintentionally doped (UID) and intentionally doped (ID) films. Intentional doping was achieved using a nitrogen and trimethylaluminum sources for n-type and p-type films respectively. Ultraviolet photoluminescence (UVPL) imaging was utilized to identify the BPDs extending into and through the grown epilayers. Atomic force microscopy and Nomarski microscopy was used to evaluate the surface roughness and film morphology. The effectiveness of an *in-situ* growth interrupt was found to be dependent on

nitrogen doping concentration. Conversion efficiency profiles show an abrupt increase in BPD conversion at the growth interrupt for low-doped nitrogen films ($<10^{16}cm^{-3}$), while epilayers with high nitrogen concentrations show minimal BPD conversion at the interrupt and overall. The effect of growth rate and film thickness on BPD conversion efficiency in highly doped nitrogen layers will also be presented. For UID p-type films (hole concentrations $<5x10^{15}$ cm^{-3}), BPD conversion took place throughout the epilayer. This phenomenon is similar to that observed in 4° material [7], but the conversion rate is much slower in the 8° material. ID aluminum films exhibited less total BPD conversion, suggesting that Al not responsible for spontaneous conversion in UID films. SIMS data will be presented for comparison.

11:00 AM

O8, Improved Surface Morphology of 4H-SiC Homoepitaxial Layers Grown on Si-Face 4° off-Axis Substrates: *Swapna Sunkari*[1]; Timothy Oldham[1]; Janna Casady[1]; Jeffrey Casady[1]; [1]SemiSouth Laboratories, Inc.

Homoepitaxial growth on 4H-SiC substrates is a key technology to fabricate unipolar and bipolar devices. Smooth surface morphology free of macroscopic step-bunching and fewer defects in the epilayers is recognized as one of the key issues for improving device performance. The quality of the epitaxial layers grown mainly depends on the process conditions and to some extent on the underlying substrate and its off-axis orientation. Optimized process conditions can highlight or suppress the crystalline imperfections as certain morphological defects on the epilayer, which can significantly influence the electrical characteristics of the devices fabricated. Epitaxial layers were grown at temperatures between 1550 -1650 ºC and pressures between 75 and 150 torr. Nomarski optical microscope and an Optical Surface Analyzer (OSA) inspection system were used to count and analyze defects both on substrates and epitaxial layers. In our previous work, we demonstrated that good quality epilayers with relatively smooth surface morphology and fewer defects can be grown on 4° off-axis substrates [1]. In this study, we present our recent process development efforts of growing epilayers free from step-bunching and very few growth related epi-defects. We optimized the process conditions by varying the C/Si ratio and process pressure keeping the growth temperature and SiH_4 flow rate fixed to our standard process. The C/Si ratio was varied in a limited range from 1.2 to 2.0 by changing only carbon precursor flow rate. After preliminary results it was noted that the step-bunching became more pronounced with increasing thickness of the epilayers [2, 3]. A 6µm thick epilayer had a smooth surface morphology with no step-bunching; whereas the step-bunching became noticeable when a 15µm thick epilayer was grown under same conditions. Our standard 4° process reproducibly produces an intra wafer thickness uniformity of 2%, with a growth rate of 5 µm/hr, doping uniformity of 6%, surface roughness Ra 1.93 nm, and total defect densities around 3.2 cm^{-2}. The new process resulted in repeated intra wafer thickness uniformity of 3%, with an increased growth rate of 6.3 µm/hr, and doping uniformity of 8%. Much smoother surface Ra 1.1 nm has been achieved with a reduced total defect densities around 1.8 cm^{-2}, which includes substrate defect densities around 0.75 cm^{-2}. Also these optimized conditions resulted in a much cleaner process therefore reducing the maintenance cycle time. The low defect density and improved surface morphology of epitaxial layers resulted in the production of 10A schottky diodes with a good yield of 72%. Further process improvement with varying temperature and ramp-up conditions is underway to achieve reduced defect densities and a smoother surface.

11:20 AM Student

O9, High-Purity Semi-Insulating 4H-SiC Homoepitaxy at a High Growth Rate Using Dichlorosilane for High Power Devices: *Iftekhar Chowdhury*[1]; MVS Chandrashekhar[1]; Pawel Kaminski[2]; Roman Kozlowski[2]; Paul Klein[3]; Joshua Caldwell[3]; Kurt Gaskill[3]; Tangali Sudarshan[1]; [1]University of South Carolina; [2]Institute of Electronic Materials Technology; [3]Naval Research Laboratory

High voltage SiC devices (~10kV) are of great interest in recent years for smartgrid and other power conversion applications. Recent demonstrations include PiN diodes, Schottky barrier diodes, DMOSFET and implanted VJFET. Epitaxial layers ~100 µm are required to obtain a breakdown voltage ~10 kV. To obtain such large thickness with standard epitaxy processes ~6-7µm/hr, a process time of more than 10 hours is required with the consequent high cost. A new process that overcomes this limitation by adding HCL or using halide precursors has been developed recently. However, the growth of thick epitaxial layers (>50µm) with low doping concentration (<1E14 cm^{-3}) remains a very difficult task, since the surface morphology usually degrades, exhibiting various morphological defects. In this paper, we will present results on high quality, thick 4H-SiC (0001) 8^0 off-axis toward (11-20) that have been grown in a vertical hot-wall chemical vapor deposition (CVD) furnace (temperature 1500^0-1700^0C, pressure 80-300 torr) at a high growth rate using a novel precursor Dichlorosilane, a kinetically favorable halide precursor. RMS roughness in the range of 0.3-0.4 nm with no morphological defects (carrots, triangular defects etc.) has been shown at growth rates 30-100 µm/hr, 5-16 times higher than the conventional speed. The surfaces were specular. Microwave photoconductive decay (µPCD) measurement showed high injection lifetime in the range of 2µs. Site-competition epitaxy was clearly observed over a wide C/Si ratio window (0.9-1.7), with doping concentration <1E14 cm^{-3}. By maintaining a highly pure growth environment and adjusting the C/Si ratio, we have systematically produced thick high purity semi-insulating (HPSI) epilayers over a C/Si ratio window of 1.3-1.5, a regime we call defect-competition epitaxy. The full width at half maximum (FWHM) obtained using x-ray rocking curves was as narrow as 8arcsec, which indicates the high quality of the epilayers. Micro-Raman spectroscopy showed the 4H polytype uniformity of these HPSI-layers. Resistivity of $1.5x10^9$ Ohm-cm was determined using transmission line model (TLM) method. Comparison of secondary ion mass spectra (SIMS) between a low doped n- epilayer grown at lower C/Si ratio (~0.9) and a HPSI-epilayer grown at higher C/Si ratio (~1.4) showed no differences in terms of N, Al and B residual impurity concentrations. A correlation of impurity concentration with measured resistivity implied a compensating trap concentration of $\sim10^{15}$ cm^{-3} present in the HPSI-epilayer. High resolution photo induced transient spectroscopy (HRPITS) analysis identified these traps as Si-vacancy related deep defect centers, with no detectable EH6/7 and $Z_{1/2}$ levels, consistent with the higher C/Si ratio.

11:40 AM

O10, Vanadium Doping Using VCl_4 Source during the Chloro-Carbon Epitaxial Growth of 4H-SiC: Bharat Krishnan[1]; Siva Kotamraju[1]; *Yaroslav Koshka*[1]; [1]Mississippi State University

Bulk growth of semi-insulating (SI) SiC has been extensively investigated, and various growth techniques for producing SI SiC wafers have been commercialized. However, relatively few reports are available on epitaxial growth of SI SiC. In this work, we report the first data on using VCl_4 as a vanadium source during the chloro-carbon epitaxial growth of 4H-SiC. The previously developed chloro-carbon epitaxial growth technique based on using chloromethane (CH_3Cl) as the carbon precursor was used. $SiCl_4$ was used as the silicon precursor. In situ vanadium doping was carried by H_2 bubbling of vanadium tetrachloride (VCl_4). While the low-temperature chloro-carbon epitaxial growth has been traditionally conducted at 1300°C in our previous work, the early vanadium-doping experiments in this work utilized a higher growth temperature of 1450°C. In addition, experiments at 1600°C were also conducted to achieve thick epitaxial layers better suitable for comprehensive materials characterization. Steep dependence of V concentration (measured by SIMS) on VCl_4 flow rate (controlled by changing the H_2 flow rate through the bubbler at a fixed bubbler temperature) was observed. It appears that the steepness of the dependence increased when approaching the limit of the V concentration before morphology degradation. Featureless epilayer surface was observed by SEM in the epitaxial layers grown at 1450°C with VCl_4 flow rates of up to ~0.0013-0.0014 sccm (corresponding to [V] = $4\text{-}6x10^{16}$ cm^{-3}). At higher VCl_4 flows, triangular-shaped defects formed, and their concentration increased with the vanadium supply. Electrical activation of the incorporated vanadium was confirmed by the increase in the intensity of the V-related infrared photoluminescence (PL) by almost an order of magnitude in the epitaxial layer doped to [V] = $4x10^{16}$ cm^{-3} as compared to an undoped reference epitaxial layer. Electrical measurements in lower-doped samples showed the values of the net donor concentration consistent with a partial compensation of nitrogen donors with vanadium acceptors. At higher V flow, full compensation and semi-

insulating behavior was observed. In a 50 µm-thick sample grown at 1600°C, non-contact capacitance based resistivity measurements revealed the values of resistivity in the range of 2-4x10^5 Ohms-cm. Thick epitaxial layers grown at 1600°C, with the growth rate in the range from 60 to 90 µm/hr, were used to evaluate the effect of V doping on the crystalline quality. While a defect-free epilayer surface morphology was observed in thick epitaxial layers exhibiting semi-insulating behavior, the X-ray rocking curves showed significant broadening. The FWHM increased from around 14 arcsec in the reference (undoped) sample to as high at 60 arcsec in the vanadium doped sample. Detailed investigation of the morphology degradation versus V flow during the growth at 1450°C and 1600°C will be presented.

Session P: One-Dimensional Photovoltaics

Thursday AM
June 24, 2010

Room: 131
Location: University of Notre Dame

Session Chairs: Joan Redwing, Pennsylvania State University; Mike Scarpulla, University of Utah

THURSDAY AM

8:20 AM

P1, Fabrication of Individual Silicon Nanowire Radial Junction Solar Cells: *Chito Kendrick*[1]; S Eichfeld[1]; Y Ke[1]; X Weng[2]; J Redwing[1]; X Wang[3]; T Mayer[3]; [1]Department of Materials Science and Engineering, Penn State University; [2]Materials Research Institute, Penn State University; [3]Department of Electrical Engineering, Penn State University

Radial p-n silicon nanowire (SiNW) solar cells are of interest as a potential pathway to increase the efficiency of crystalline silicon photovoltaics by reducing the junction length and surface reflectivity. Our studies have focused on the use of vapor-liquid-solid (VLS) growth technique to produce p-type silicon nanowires to act as the collection core of the solar cell. For the n-type shell layer, both low pressure chemical vapor deposition (LPCVD) and thermal diffusion of phosphorus have been investigated. The effect of process parameters and junction formation technique were investigated using single wire measurements which provides information on the diode characteristics and solar cell properties. High aspect ratio p-type SiNW arrays (300 - 500 nm diameter) were initially grown on both patterned and unpatterned gold-coated (111) Si substrates by CVD using $SiCl_4$ as the source gas and B_2H_6 as the p-type dopant source. Four point resistance measurements on individual p-type silicon nanowires indicated a nanowire resistivity of 0.01 O-cm for a $SiCl_4$:B_2H_6 ratio of 1x10^{-4}. Prior to the junction fabrication, the gold tips were removed from the wires using Transene gold etchant for 40 minutes at a solution temperature of 40°C. Additional cleaning was done by thermally oxidizing the wires for 2 hours to produce a 150 nm thick SiO_2 layer, which was later removed before the n-type shell fabrication. The oxidation process also thins the wires to diameters that are needed for electrical measurements. The epitaxial re-growth of n-type Si shell layers on the Si nanowires was then investigated using SiH_4 as the source gas and PH_3 as the dopant. Highly conformal coatings were achieved on nanowires up to 25 µm in length. The microstructure of the Si shell layer changed from polycrystalline to single crystal as the deposition temperature was raised from 650°C to 950°C. For the thermal diffusion of the n-type shell, an annealing temperature of 1000°C was applied for 13 minutes with the introduction of $POCl_3$ dopant gas.Electrical test structures were fabricated by aligning released SiNWs onto pre-patterned substrates via field-assisted assembly followed by selective KOH etching to remove part of the n-type shell layer before contact deposition. Preliminary current-voltage measurements of the radial p-n SiNWs diodes fabricated with re-grown Si shell layers demonstrate rectifying behavior with an ideality factor of 1.67 and low reverse leakage current.

8:40 AM

P2, Wire Textured Multicrystalline Silicon Solar Cells: *Kejia Wang*[1]; Oki Gunawan[1]; Naim Moumen[1]; George Tulevski[1]; Hisham Mohamed[2]; Babak Fallah[3]; Emanuel Tutuc[3]; Supratik Guha[1]; [1]IBM T.J. Watson Research Center; [2]Egypt-IBM Nanotechnology Research Center Labs; [3]University of Texas Austin

Currently the multicrystalline (MC) Silicon is an important material for solar cell market because of its low cost and easy assembly into modules. One of the main challenges for MC Si solar cells is that there is no satisfactory and easy process for texturing MC Si surface to reduce reflectance. For single crystal Si, the commonly use method to texture surface is KOH based solution etching. However, this process cannot be used for MC Si due to the anisotropic nature of KOH etching. In this work, we have investigated enhanced light trapping in MC Si solar cell using wire array texturing. MC Si surface was first functionalized using aminopropyltriethoxysilane (amino-silane). Then one monolayer carboxyl polystyrene micronspheres was patterned onto Si surface as shown in Figure 1. This process requires no spinning based steps and easy to scale up to larger wafer sizes. Then, using this monolayer microsphere as the etching mask, wires were etched using reactive ion etching to texture the MC Si surface (Figure 2). The measured reflectivity spectra in Figure 3 showed that there was a significant drop in the reflectivity for the wire textured MC Si devices. The weighted average reflectivity (WAR) respect to solar spectrum AM1.5 was used to evaluate the reflectance. Before wire texturing, the WAR for MC Si is ~ 22.6%. After the wire texturing, the WAR drops to 13.5%. Compared with standard KOH textured single crystal Si, which has a WAR of 11.9%, this wire texturing provide an efficient way to reduce the surface reflectance of MC Si. Solar cell devices were then fabricated based on the wire textured MC Si. The wire textured device performance and the control planar MC Si device were measured and plotted in Figure 4. The wire textured devices display 20% higher short circuit current densities, which is due to the enhanced light trappings. The efficiency of the wire textured MC Si solar cell is ~ 7.5%, which is also same as the planar MC Si solar cell. The device performance of wire textured MC Si solar cell is limited by the higher series resistance (6-9O), compared to 2.6 O of a planar control sample. Using a Jsc-Voc measurement we can exclude this series resistance effect, we observe 7~16% enhancement in pseudo-efficiencies for wire textured MC Si solar cells.

9:00 AM

P3, Efficiency Enhancements for Copper Contaminated Radial p-n Junctions over Planar p-n Junctions in Silicon: Akram Boukai[1]; *Alec Talin*[2]; Gregg Gallatin[2]; Aaron Katzenmeyer[3]; Peidong Yang[4]; [1]University of Michigan; [2]NIST; [3]Sandia National Laboratories; [4]UC Berkeley

The need to employ high purity, semiconductor grade Si in the fabrication of Si solar cell significantly increases the cost of Si based photovoltaics. Reducing this cost by employing cheaper, metallurgical grade Si would also substantially degrade cell performance due to the diminished carrier diffusion length. Radial pn junction solar cells based on vertical arrays of Si nanowires have been proposed as a possible route to circumvent the requirement for high purity material by orthogonalizing the direction of light absorption and minority carrier diffusion necessary to reach the junction. Here we present first experimental results on radial pn junction arrays fabricated by a combination of optical lithography and deep reactive ion etching deep vias in boron doped Si wafers followed by pn junction formation using a spin-on glass phosphorus source. To simulate the effects of impurities in metallurgical grade Si, we intentionally contaminate our devices by depositing Cu films on the back side followed by thermal annealing. Cu contamination decreases the electron diffusion length from ~500 µm for clean Si to ~0.3 µm for the contaminated Si, as measured using electron beam induced current technique. We test our devices under simulated 1 sun conditions and report that while planar Si pn junction has superior performance for clean semiconductor grade Si, the radial arrays outperform the planar junction formed with Cu contaminated Si. Furthermore, we demonstrate that radial junctions with a 4 µm pitch perform better than those with a 10 µm pitch, and that the device performance is consistent with a simple model based on solution of the Poisson and carrier diffusion equations for the radial geometry pn junctions.

9:20 AM Student

P4, Wafer Scale Si Nanowire Arrays for Photovoltaic Applications: *Yi Jing*[1]; Ke Sun[1]; Deli Wang[1]; [1]University of California, San Diego

Photovoltaic devices are attractive candidates for clean and renewable energy sources. Although the majority of the commercial solar cells are based on Si thin film devices, vertical aligned Si nanowire array is a promising alternative for low cost and high efficiency photovoltaic devices because of enhanced light absorption and improved carrier separation/collection. In this research, large area coaxial Si p-n junction nanowire solar cells were fabricated and characterized. Instead of conventional VLS growth, a HF based aqueous solution method was employed to etch vertical aligned Si nanowire array with desired doping and crystalline orientation. Without size limitation, multiples Si wafers can be etched together to produce nanowire arrays, which greatly reduces the cost. The length of the nanowires can be easily controlled by tuning the etching time. In this report, test grade 2-inch n-type (100) Si wafers were used. After solvents cleaning, Si wafers were immersed into an aqueous solution of HF and silver nitrate with a concentration of 5M and 0.02M respectively for 11 minutes at 50°C, resulting in ~2μm long vertical aligned nanowire arrays on wafer surfaces. The produced silver film on top of nanowires was removed using nitric acid. The coaxial p-n junction was formed by boron diffusion into the etched Si nanowires. Transparent indium tin oxide (ITO) was sputtered onto the surface of the nanowires as front contact and indium back electrode was formed using soldering iron. The nanowire devices were characterized under dark and with AM1.5 solar simulator illumination: an open-circuit voltage of 0.51V and a short-circuit current density of 40.5mA/cm^2 were obtained. The devices showed an energy conversion efficiency of 3.0% and fill factor of 0.25. Further improvement of front and back contacts are investigated to enhance the efficiency. This research will lead to a low cost fabrication process, mass manufacturable, high effieciency Si nanowires p-n junction solar cells.

9:40 AM

P5, Late News

10:00 AM Break

10:20 AM Student

P6, Branched ZnO/Si Nanowire Heterostructure Based Photoelectrochemical Cell for Efficient Water Splitting: *Ke Sun*[1]; Banu Khaleda[1]; Yi Jing[1]; Namsoek Park[1]; Deli Wang[1]; [1]University of California, San Diego

Design and synthesis of nanoscale heterostructures has attracted significant attentions in recent years because of their unique properties, diverse functionalities, and potential applications in photovoltaics and photocatalytics [1]. Various nanowire-based heterostructures, such as axial, radial/core-shell, and branched structure, have been developed and studied, due to their prominent tunable functionalities and greatly enhanced surface reactivity. These types of structure have helped scientists in hydrogen generation from water splitting. In principle, nanoheterostructure is working as a photoelectrochemical (PEC) anode/cathode generating electron/hole pairs from incident photons and then generated electrons reduce hydrogen ions. In this work, we report our research effort on developing efficient PEC cells for water splitting based on a branched n-ZnO/p-Si nanowire heterostructure from a cost-efficient and robust solution-phase integration process. Wafer-scale and highly dense vertical arrays of Si nanowire arrays were prepared using metal-assisted electroless etching [2]. SEM and TEM investigations show the vertical alignment, smooth surface of etched Si nanowires and large variations in diameter (average around 70nm). ZnO nanowires, intrinsically n-type, were then synthesized on the ZnO seeded Si nanowire arrays using hydrothermal method. SEM studies show the growth of ZnO nanowires in between Si nanowires to form branched heterostructures with average diameter of 50nm and average length of 250nm. The ZnO/Si n/p heteorstructures is then immersed in neutral electrolytes (pH=7) due to the less stability of ZnO in acidic or basic solution [3] and the photoelectrochemical production of hydrogen were tested under solar illustration (AM 1.5G) and the overall hydrogen production efficiency of the PEC cell is evaluated. The branched nanowire configuration enables low cost direct integration of heterogenerous nanomaterials with reduced defect density for high efficiency hydrogen generation.

10:40 AM

P7, Solar Cells Based on ZnO/ZnS Core-Shell Nanowires Arrays: *Aurelien Du Pasquier*[1]; Shamgzhu Sun[2]; Elan Coleman[2]; Bruce Willner[2]; Gary Tompa[2]; [1]Rutgers State University; [2]SMI, Inc.

ZnO nanorod arrays have been proposed for their application in photovoltaic devices, owing to the ease of growing arrays of high crystalline quality, low cost and low toxicity of ZnO, and well controlled length and shape nanowires. Since ZnO is an n-type semiconductor with a wide bandgap of 3.3 eV, visible light absorption must be provided by an associated p-type semiconductor. In particular, extremely thin absorber (ETA) solar cells could greatly benefit from this nanostructure, because light absorption would occur parallel to the length of the nanorods, but charge separation can occur normal to the nanorods, with increased efficiency. Hybrid photovoltaic devices have been demonstrated using poly (3-hexylthiophene) (P3HT) as light absorber and hole transport phase [1], and band alignment with ZnO can be achieved with Mg doping of ZnO [2]. Another approach is to design n-core/p-shell structures using a core of ZnO nanowires and a shell of ZnS. Bandgap control is achieved through the staggered type II heterojunction, where the effective bandgap at the junction can be calculated as the difference between the valence band level of ZnS, and the conduction band level of ZnO [3]. ZnO/ZnS core-shell nanorods have been prepared from solution grown ZnO nanorods [4]. ZnO/ZnTe core-shell nanorods have also been prepared by chemical vapor deposition [5]. Here, we will present initial MOCVD growth results of ZnO-ZnS core-shell nanostructures characterized via SEM, XRD and UV-vis spectroscopy. Their efficiency in photovoltaic devices of the type FTO/ZnO-ZnS/Au and FTO/ZnO-ZnS/P3HT/Au will be reported by external quantum efficiency and I-V measurements under simulated sunlight. References: Olson, DC Lee, YJ White, MS Kopidakis, N Shaheen, SE Ginley, DS Voigt, JA Hsu,,J.W.P. Journal of Physical Chemistry C 111, 16640-16645 (2007); J. Piris, N. Kopidakis, DC Olson, SE Shaheen, DS Ginley, and G Rumbles, Adv. Funct. Mater. 17, 3849–3857 (2007); J. Schrier, DO Demchenko, L-W Wang and AP Alivisatos, Nanolett. 7, 2377 (2007); JJ Uhlrich, R Franking, RJ Hamers, and TF Kuech, J. Phys. Chem. C 2009, 113, 21147–21154 21147; HY Chao, JH Cheng, JY Lu, YH Chang, CL Cheng, YF Chen, Superlattices and Microstructures 47, 160-164 (2010).

11:00 AM Student

P8, Fabrication of Subwavelength Pillar Arrays on GaAs by Confined Self-Assembly Technique for Broadband Antireflection Coating: *Dae-Seon Kim*[1]; Min-Su Park[1]; Yon-Kil Jeong[1]; Wu Lu[1]; Jae-Hyung Jang[1]; [1]Gwangju Institute of Science and Technology

Multilayer thin films are widely used for antireflection coatings of various devices such as solar cells, photodetectors, and optical amplifiers to minimize the optical loss due to surface reflections. Although thin film coatings are ideal for antireflection coatings in narrow band applications, subwavelength structures (SWS) are preferred for broad band applications. So far SWS have been fabricated by nanolithographic techniques such as electron beam lithography, nanoimprint lithography and holographic lithography. Even though these methods have successfully demonstrated SWS with good optical properties, low cost process technologies are highly needed for manufacturing of optical devices requiring broadband antireflection coating. In this study, SWS on GaAs substrates were fabricated by using the confined convective self-assembly1 method followed by inductively coupled plasma reactive ion etching (ICP-RIE). This method provides a much simpler and cheaper process and opens the possibility of large area SWS fabrication at low cost. Monolayer consisting of 300-nm-diameter polystyrene spheres were prepared on GaAs substrate using the confined convective self-assembly method. Either multilayer or monolayer polystyrene spheres could be assembled on the substrate by controlling the lift-up rate and the substrate temperature. The closely packed monolayer was subsequently treated by O2 reactive ion etching (RIE) process (30 mTorr chamber pressure, 30 SCCM O2). After the exposure to O2 plasma for 60 sec, the diameter of polystyrene spheres decreased from 300 nm down to 250 nm. The resulting 250-nm-diameter sphere arrays with 300-nm-pitch were used as the etching mask for the pattern transfer by ICP-RIE. Subwavelength structures consisting of pillar arrays with aspect ratios of 0.4, 1.35 and 3.63 were fabricated by controlling the etching time of ICP-RIE (7.5 SCCM SiCl4, 60 SCCM Ar). Finally the

remnant polystyrene spheres were removed by O2 RIE process. The reflectance of the fabricated SWS was measured at wavelength ranging from 300 to 1000 nm under the normal incidence. Reflectance of the bare GaAs substrate was higher than 30% throughout the wavelength range investigated in this study. For comparison, the GaAs substrates coated with single layer SiNX exhibited very low reflectance of 1% at the wavelength between 550 and 700 nm. The GaAs with SWS in this work exhibited reflectance lower than 8.5% throughout the wavelength range investigated. The low reflectance achieved by GaAs textured by the nano-pillar SWS is attributed to the nature of subwavelength structures which cannot be resolved by the incident light. Continuous transition of the effective refractive index from the top surface to the substrate dramatically reduces the surface reflection by minimizing the refractive index mismatch at the interface2. The fabrication details and the optical measurement results of the SWS with various aspect ratio and various fill factors will also be discussed.

11:20 AM Student

P9, Hybrid Solar Cell Based on Patterned Nanopillar/P3HT Heterojunction: *Giacomo Mariani*[1]; [1]University of California, Los Angeles

In this work, we present a hybrid solar cell design that combines together catalyst-free patterned GaAs nanopillar with P3HT polymer, mainly used in organic and plastic solar cell. Hybrid solar cells integrate conjugated polymers, responsible for high processability at low cost and high optical absorption coefficient, and semiconducting nanostructures, responsible for high mobility required in carrier extraction. We have investigated a hybrid photovoltaic cell realized by n-doped GaAs patterned nanopillars and P3HT (semiconducting polymer) that acts as a hole transport layer. Patterned nanopillars grown by MOCVD were exploited thanks to their catalyst-free growth mode that eliminates any catalyst (i.e. Au) diffusion into the nanopillars that could hinder the electron-hole pair extraction, such a paramount process in solar cells. Our inherently lattice-matched growth capability also avoids threading dislocations that normally act as recombination centers, worsening the leakage current in pn-junction based devices. Furthermore, surface state density in nanopillars is a major-concern problem that reduces the effective conductivity of the nanostructure due to a depletion region that creates near the interface. Many efforts have been carried out to quench this effect by passivating the nanostructures prior to device fabrication. Comparisons were made in terms of photocurrent density-voltage (J-V) characteristics and external quantum efficiency (EQE), standard figures of merit in the photovoltaic field. Passivated PV devices are measured along with un-passivated solar cells and control cell. The best un-passivated PV device exhibits an open circuit voltage (VOC) of 0.2V, short circuit current density (JSC) of 8.7 mA/cm2 and a fill factor (FF) of 32% whereas passivation showed a drastic change in terms of device performance. The best passivated PV device delivers a VOC=0.18V, JSC=8.6 mA/cm2 and a fill factor FF above 42%. All measurements are carried out under 1-sun AM 1.5 direct illumination at room temperature. Extremely low leakage currents in reverse-biased mode (ILEAKAGE<10nA) are detected. This can be attributed to a high-quality crystalline growth in the nanopillars. EQE characteristics for the passivated samples show a quantum efficiency above 50% between 650nm and 850nm, revealing a relative increase of ~10% with respect to the case without any passivation. With respect to previous work on catalysed growth, the power conversion efficiency went from η=1.04% (un-passivated device) to η=1.44% (passivated device). This work demonstrates the high dependency of hybrid nanostructured PV device performance in terms of exciton dissociation/transport/extraction when the nanopillars are chemically treated before processing. Also, the interpenetrating polymer/semiconductor network shows an outstanding current density whereas the open circuit voltage can be furtherly improved by a better work function alignment between P3HT and GaAs.

11:40 AM

P10, Dissociation of Photo-Generated Excitons on Carbon Nanotubes at Type-II Heterojunctions: *Dominick Bindl*[1]; Michael Arnold[1]; [1]UW Madison

Semiconducting single walled carbon nanotubes (s-SWCNTs) are attractive as absorbing materials in photovoltaic devices. S-SWCNTs have large absorption coefficients, ($> 10^5$ cm^{-1}) with optical bandgaps from 1.0 – 1.3 eV. In addition, s-SWCNTs have excellent charge transport properties, are solution processable, and offer enhanced photo-oxidative stability relative to photovoltaic polymers. Despite their promise, s-SWCNT have had limited impact in photovoltaics. A primary reason for this is the challenge associated with overcoming the large exciton binding energy (0.2 – 0.5eV) of photogenerated charge carriers in SWCNTs. In organic photovoltaics, exciton dissociation is achieved through a donor/acceptor type-II heterojunction in which the molecular orbital energy offset between the donor and acceptor is greater than the exciton binding energy. A similar strategy can be used to dissociate excitons in nanotubes; however, the energy levels of nanotubes are dependent on diameter, chiral angle, and local dielectric environment. For this reason, the selection of materials that form a type-II heterojunction with s-SWCNT is nontrivial. Here we experimentally evaluate donor/acceptor candidates for achieving exciton dissociation. We have utilized s-SWCNT/donor or acceptor/insulator/metal photoactive capacitors. In these capacitors, excitons are photogenerated in the nanotubes via near infrared (NIR) illumination at their E_{11} optical band gap transitions, and exciton dissociation is measured as a transient photocurrent and photovoltage response to modulated illumination. This technique is advantageous in that it does not utilize an externally applied bias and thus avoids misleading, photoconductive or heat-based changes in resistance and electrical current upon illumination even in the absence of exciton dissociation. Optical excitation in the NIR ensures that only the s-SWCNTs are excited rather than the donor or acceptor materials. We have characterized a variety of semiconducting polymers and small molecules as donors or acceptors to s-SWCNT using the photoactive capacitors. Dissociation of photogenerated excitons on s-SWCNT was observed at the interface of the nanotubes with fullerene-derivatives and poly(thiophene) derivatives such as P3HT and P3OT. In contrast to literature, no significant exciton dissociation was observed at interfaces with polymers such as MDMO-PPV or insulating polymers such as polycarbonate. PFO devices also failed to elicit a photoresponse. C60 interfaces resulted in the highest efficiency for exciton dissociation, a factor of three greater than C61-PCBM and all thiophene based devices - which were themselves an order of magnitude more responsive than PPV derived polymers. Our work demonstrates that s-SWCNT can serve as both electron donating and electron accepting materials in photovoltaic films. Through bias dependencies, it is concluded that exciton dissociation at the interface of fullerene/thiophene derivatives results in electron/hole transfer from s-SWCNT, respectively. Excitons photogenerated on C60, C61-PCBM, P3OT, P3HT and rr-P3HT in response to visible excitation were also dissociated at the interface.

Session Q: Oxide Thin Films

Thursday AM
June 24, 2010

Room: 138
Location: University of Notre Dame

Session Chairs: Bruce Hinds, University of Kentucky; Pat Lenahan, Pennsylvania State University

8:20 AM

Q1, Pulsed-dc Reactive Sputtering Vanadium Oxide Thin Films for Microbolometers: *Bharadwaja Srowthi*[1]; C. Venkatasubramanyam[1]; N. Fieldhouse[1]; B. Gauntt[1]; O. Cabarcos[1]; Myung Yoon Lee[1]; S. Ashok[1]; E. C. Dickey[1]; T. N. Jackson[1]; M. Horn[1]; [1]Penn State University

Current industry requirements for microbolometers include fabrication of VO_x thin films with high temperature coefficient of resistivity (TCR), low resistivity, low noise, good stability, and low temperature processing (<400 °C) for integration onto CMOS circuitry. In this work, VO_x films were deposited using pulsed dc sputtering as an alternative to the usual industry-used process of ion beam sputtering. Reactive sputtering often exhibits sputter gas composition hysteresis due to reaction of the target with the sputtering gases. We will discuss the process control of VO_x thin films grown in pulsed-dc reactive sputtering to tailor desired electrical properties. The process hysteresis in our pulsed dc sputtering was monitored using target current for various argon to oxygen ratios over a 5 - 100 mT pressure range. Film deposition rate, resistivity, and

temperature coefficient of resistance of the VO_x thin films deposited at various points on the sputtering gas composition curve also exhibited hysteretic behavior which could be tracked by the associated cathode current hysteresis. Structural characterization using X-ray diffraction, transmission electron microscopy (TEM), and Raman spectroscopy were utilized to correlate the film properties with the processing conditions. In particular, TEM analysis on the films processed with low processing pressures and oxygen partial pressures contained micro crystallites embedded in an amorphous VO_x matrix. These films also had film resistivity (0.1 to 1 ohm.cm) and TCR (-1.8 to -2.2% K^{-1}) in the range required for micro bolometer applications. Low temperature charge transport in vanadium oxide (VO_x) thin films was investigated to understand the correlation between the processing conditions and electrical properties. By using a combination of resistivity versus temperature measurements and simple theoretical arguments, it was identified that the temperature dependent resistivity, $\rho(T)$, of the VO_x thin films is dominated by a Efros-Shklovskii variable range hopping (ES-VRH) mechanism obeying the relation $\rho = \rho_o.\exp(T_o/T)^{0.5}$, where T_o is a measure of the degree of charge disorder of the VO_x films. Analysis in terms of charge hopping parameters in the low temperature regime was used to correlate film properties with the pulsed DC sputtering conditions. Finally, the 1/f noise of the VO_x films was measured and correlated with other film properties. The normalized power spectral density of pulse dc sputtered VO_x thin films was compared with ion beam sputtered films with comparable resistivity values (ρ_{dc} = 0.43 ohm.cm and 0.25 ohm.cm). The 1/f noise for samples deposited by the two techniques was similar. Assuming the carrier mobility is similar for films deposited by the two techniques this indicates that the Hooge parameter for pulsed dc sputtering and ion beam sputtered VO_x films is also similar. This suggests that the quality of pulsed dc sputtered VO_x thin films is comparable to industry quality ion beam deposited films.

8:40 AM Student

Q2, Defects in Low-κ Dielectrics and Etch Stop Layers for Use as Interlayer Dielectrics in ULSI: *Brad Bittel*[1]; P.M. Lenahan[1]; S. King[2]; [1]Penn State Univ.; [2]Intel Corp.

The electronic properties of low-κ dielectric thin films and etch stop layers (ESL) are important issues in present day ULSI development.1-6 The quality of low k dielectrics and there corresponding ESL is paramount to successful adoption of modern interlayer dielectrics (ILD). ESL are needed for ULSI processing and there is interest to find films with k values lower than the industry standard SiN with suitable properties. Leakage currents in general as well as reliability issues such as, time dependent dielectric breakdown (TDDM) and stress induced leakage currents (SILC) are critical problems that are not yet well understood in ILD. A topic of current interest is ultraviolet light (UV curing) of low-κ materials.5,6 We have made electron spin resonance (ESR) and current density versus voltage measurements on a moderately extensive set of dielectric/silicon structures involving materials of importance to low-κ interlayer systems. Most of the dielectrics studied involve various compositions of SiOC:H. In addition we have also made measurements on other dielectrics including SiO2, SiCN:H and SiN:H. In our study we have made ESR and current density versus voltage measurements both before and after exposing the dielectrics to UV light (hc/λ = 5 eV), and films that have experienced an industrial UV curing process. We observe extremely gross differences in the ESR spectra and leakage current versus voltage response of these low-κ films. We find that UV exposure consistently increases both the density of paramagnetic defects and the leakage current density at a given field. Paramagnetic point defects observed in these films include, E' centers, silicon dangling bond defects in which the silicon is back bonded to oxygen, possibly silicon and carbon dangling bond centers and likely organic radicals. Our preliminary results suggest the UV curing process creates paramagnetic centers which take part in trap assisted tunneling. This tunneling increases dielectric leakage current. Our preliminary results indicate quite clearly that the processing parameters have extremely gross effects upon defect densities within these films. 1. F. Chen et al. Proc. of the Forty Third Int. Rel. Phys. Sym., 501 (2008); 2. Y. Ou et al., J. Electrochem Soc. 155, (12) G283 (2008); 3. J. Michelon and R. J. O.M. Hoofman, IEEE Trans on Dev. and Mcr. Rel. 6, 169 (2006); 4. C. Y. Kim, et al., Coatings Technology, 202, 5688 (2008); 5. S. Eslava, et al., J. Electrochem Soc. 155, G155 (2008); 6. E. Marhrez, et al., J. Applied Phys. 100, art. no.124106 (2006).

9:00 AM Student

Q3, Nanocluster and Nanocrystalline Si Trap Distributions within SiO_2/SiO_x/SiO_2 Field Oxides for Radiation-Tolerant Electronics: *Evan Katz*[1]; Zhichun Zhang[1]; Hap Hughes[2]; Kwun-Bum Chung[3]; Gerry Lucovsky[3]; Leonard Brillson[1]; [1]The Ohio State University; [2]Naval Research Laboratory; [3]North Carolina State University

We have used nanoscale depth-resolved cathodoluminescence spectroscopy (DRCLS) and spectroscopic ellipsometry (SE) to measure energies and spatial distributions of Si-related charge traps in SiO_2/SiO_x/SiO_2 field oxides for radiation-tolerant electronics. Suboxide layers within SiO_2/Si structures result in Si nanoclusters that reduce the flatband voltage shift by trapping ionized protons and electrons [1]. Such traps reduce the net positive charge during exposure to ionizing radiation that result in negative flatband voltage shifts and charge leakage pathways. We prepared SiO_2/SiO_x/SiO_2 gate dielectrics with reduced oxide concentrations and monitored their optical absorption and emission features with annealing and irradiation. These nanoscale structures segregate with annealing from amorphous Si into nanocrystalline Si surrounded by SiO_2 [2]. DRCLS and SE provide optical transitions at energies involving not only intra- but also interphase transitions due to their intimate contact and high area. Deconvolved DRCLS spectra distinguished spatially between traps associated with Si nanoclusters, Si nanocrystals, SiO_2 native defects, and Si ion implantation damage used to create Si-rich SiO_2. Understanding the physical nature of such traps may enable control of radiation-induced holes in higher-K dielectric SOI structures.To distinguish trap cathodoluminescence from implanted versus crystalline versus implant-damaged regions in the oxide stack, we varied incident beam energy E_B from 0.5 – 1 keV. The peak rates of electron-hole pair creation inside the SiO_2/SiO_x/SiO_2/Si(100) structure were separated by only ~3 nm. Higher E_B probe the SiO_x "bulk" and the lower SiO_x/SiO_2 regions. For a non-annealed but irradiated (7.6 Mrad(SiO_2)Co-60, 5.7 Mrad/hr) sample, we found defect levels located 3.5 and 3.9 eV below the conduction band of SiO_2. These traps increase with E_B until 0.8 kV, ~10 nm within SiO_x. The 2.00 and 2.55 eV (NBOHC and E' center) peaks increase with E_B and depth, probing deeper into SiO_2. Beyond 10-14 nm below the free surface, the intensity of the 3.5 and 3.9 eV defects decrease. Since the Si implantation occurred only within the outer 10 nm of SiO_x, we associate these defects with Si-nanoclusters and nc-Si grains. We also observed a 0.1 (0.05) eV defect shift to higher SE (DRCLS) energy with annealing. Both techniques are consistent with the energy levels of SiO_2 and Si for trap states at their interface located 0.3 eV above the valence band. Coupled with similar results for annealed and irradiated samples, these results demonstrate that: (i) the 3.9 and 3.5 eV defects located at Si nanoclusters and nanocrystals trap charge within narrow (10 nm) surface layers to improve radiation hardness, (ii) nanocrystals are more efficient traps than nanoclusters, (iii) ion implantation damage can not account for these traps, and (iv) these traps are most effective after annealing plus irradiation. These depth-resolved results validate the carrier trapping mechanism of SiO_x resistance to ionizing radiation.

9:20 AM Student

Q4, Nanoscale Depth-Resolved Electronic Properties of HfO_2/RPAN/Ge and HfSiON/RPAN/Ge Gate Dielectrics for Radiation-Tolerant Electronics: *Zhichun Zhang*[1]; E. J. Katz[1]; K.-B. Chung[2]; G. Lucovsky[2]; L. J. Brillson[1]; [1]Ohio State University; [2]North Carolina State University

We used nanoscale depth-resolved cathodoluminescence spectroscopy (DRCLS) to measure the energies and depth distributions of charge traps in HfO_2 and HfSiON high-k gate dielectrics on remote plasma-assisted nitrided (RPAN)/n-Ge for radiation-tolerant electronics. The drive for higher speed electronics has promoted development of high-k dielectrics to replace SiO_2 and substitution of higher mobility Ge for Si. The mechanisms by which electronically-active defects form in the Ge-dielectric gate stack under different process conditions as well as high energy irradiation are not yet understood. Defect control under these conditions can enable higher speed but also radiation-tolerant high-k dielectric/Ge MOSFET for space applications. Our previous work showed that rapid thermal anneal (RTA) in Ar at T>700°C eliminates the interfacial RPAN layer intended to reduce negative trapped charge for n-MOSFET under bias [1]. RTA also increases the nano-grain dimensions of the as-deposited nanocrystalline

HfO_2 films [1]. O-vacancies and interstitials clustered and pinned at the HfO_2 nanocrystalline grain boundaries trap electrons during exposure to ionizing radiation, leading to flatband voltage shifts and pathways for leakage current [2]. We used remote plasma-enhanced chemical vapor deposition (RPCVD) to deposit crystalline HfO_2 and amorphous HfSiON onto RPAN/n-Ge substrate at 300°C, then measured their optical absorption and emission spectra of samples versus annealing and irradiation. DRCLS provided the energy level transitions within the ultrathin gate dielectric layer and the dielectric-Ge interface, enabling defect identification in these nanoscale regions, their evolution with processing, and methods to control them. From the gate structure of the samples and Monte Carlo simulation of electron-hole pair generation versus incident electron beam energy E_B and excitation depth, E_B=1 keV probes mainly in the gate dielectric layer and the interface. DRCLS spectra show HfO_2-related defect emissions at 2.0, 2.7, 3.5, 4.0, and 4.5eV versus annealing and irradiation. These are assigned to different charge states of O-vacancies and interstitials, corresponding to X-ray absorption spectra (XAS) and spectroscopic ellipsometry (SE) transitions between defect states in the HfO_2 band gap. [2,3] RTA halves defect intensities by annealing out O-vacancies and interstitials and reducing grain-boundary surface area as nanocrystalline HfO_2 grain size increases[4]. However, ^{60}Co irradiation triples defect intensities in these annealed samples. Irradiation alters O-vacancy clustering and charge state in the larger nanocrystalline HfO_2 films, trapping electrons more efficiently in the oxide, potentially shifting flatband voltages. Compared to HfO_2, HfSiON suppresses Ge indiffusion with RTA and has much lower defect densities, particularly after irradiation. Nevertheless, RTA degrades radiation hardness for both HfO_2 and HfSiON. Hence HfSiON deposited on RPAN/n-Ge without RTA is the most radiation tolerant for MOS devices. These studies identify the defect levels in HfO_2 and HfSiON, reveal their radiation tolerance under different processing, and provide guidance for producing radiation-tolerant high-k dielectric/Ge MOSFETs.

9:40 AM Student

Q5, Nano-Gap Electrodes Formed at the Exposed Edge of $Au/Al_2O_3/Au$ Tunnel Structures Grown by Atomic Layer Deposition: *Bing Hu*[1]; Bruce J. Hinds[1]; [1]University of Kentucky

Fabrication of nanometer-scale electrode gaps is a critical step for numerous devices based on single molecule conduction as well as to serve as a probe for the fundamental transport properties of molecular materials such as organic conductors. Several techniques, such as mechanical break junction [1] and electromigration junction [2], have been developed to realize nano-gap electrodes but suffer from scaling and yield issues. Recently, a simple technique to fabricate the exposed edge of metal/Al_2O_3 (2.0 nm)/metal structure by photolithography-liftoff process for molecular electrodes was reported [3]. This technique uses highly controllable film thickness (Al_2O_3) to set the critical spacing between electrodes. After lift-off or etching process, molecules can bridge across the nm-thick insulator connecting top and bottom metal contacts. However, the system, with Ni metal contacts, possessed long term stability issues due to surface oxidation and hillock formation from stress release. Much of the molecular electronics literature to date has utilized Au-thiol chemistry to ensure clean inert surfaces for molecular contacts. However it is difficult to form stable Au-insulator tunnel junctions due to high surface energy and subsequent island growth of oxides on Au. To overcome these limitations, we used atomic layer deposition (ALD) to grow Al_2O_3 layer on Au electrodes that were modified with a self-assembled monolayer of alcohol groups. Reactive ion etching (RIE) was then used to expose the edge of the Au/insulator/Au structure for molecular electrode contacts. The Au/Al_2O_3/SAM/Au tunnel junction, with a very thin insulator layer (1.6 nm), is stable and has a small tunneling current density about 0.01 A/cm2 at 0.1 V. This background tunnel current is two orders lower than that of metal/Al_2O_3 (2.0 nm)/metal structure by photolithography-liftoff process previously reported. In addition to molecular conduction studies, this electrode design has been employed to study photovoltaic organic materials. We have deposited a thin layer of Copper Phthalocyanine (CuPc) on the exposed edge of Au/Al_2O_3 (10 nm)/Au structure and observed large photocurrents that are over two orders higher than that of bulk CuPC material. The nano-scale gap between Au electrodes, which is controlled by the thickness of Al_2O_3, is smaller than the exciton diffusion length of CuPc thus allowing increased photocurrent. Schottcky barrier contact resistance was found to be the primary limiter of charge injection into the organic film. An electrode structure based on the exposed edge of $Au/Al_2O_3/Au$ tunnel junctions can provide a reliable method for the fabrication of molecular-scale devices and more efficient solar cells.

10:00 AM Break

10:20 AM Student

Q6, Surface-Interface Conductivity in Thin Film Gd-doped CeO_2: *Matthew Swanson*[1]; Lakshmi Krishna[1]; Natee Tangtrakarn[1]; Madhana Sunder[1]; P.D. Moran[1]; [1]Michigan Technological University

The ionic conductivity of a Gadolinium doped Ceria (GDC) interface/surface at temperatures between 300-700°C is of interest due to the application of the material as an electrolyte for low temperature Solid Oxide Fuel Cells (SOFCs). It has been asserted in the literature that the exceptionally high ionic conductivity observed in thin GDC films is due to the substrate/film interface or surface acting as a high conductivity path for ions [1, 2]. Those studies were not performed on single crystal GDC and, therefore, did not completely isolate the ionic conduction along the film surface and substrate/film interface. A study to extract the surface and interface contributions to the total ionic conductivity of GDC films has not been reported. This work addresses the need for such an analysis. The approach taken in this work has been to fabricate a series of GDC single-crystal films of varying thicknesses on Al_2O_3 substrates by RF magnetron sputtering and then to measure their conductivities over the 300-700°C temperature range. These data are analyzed to extract the differences in carrier concentration and activation energy of the single-crystal films as a function of film thickness. An analysis is performed to extract separate activation energies and specific conductivities for the bulk and interface/surface components of the total conductivity. In contrast to the assertions in the literature concerning ultrathin GDC films it is found that as the film thickness is decreased, so that the interface and surface conduction mechanism is more predominate, the total ionic conductivity decreases rather than increases. This data is analyzed in the framework of changes in the temperature-dependent carrier concentration and mobility of the surface and interface regions. Analysis of these data suggests that the temperature-dependent, oxygen non-stoichiometry can significantly affect the ionic conductivity of the GDC surface at temperatures lower than around 600°C. The GDC surface becomes disproportionally resistive at lower temperatures as vacancies are replaced with oxygen atoms, effectively reducing the carrier concentration. This reduction in the surface carrier concentration leads to a drop in total film conductivity by a factor of three from the 500 to 100 nm film at 300°C.

10:40 AM

Q7, Growth of Heteroepitaxial $SrRuO_3$ Electrodes on CeO_2 Buffered R-Plane Al_2O_3 Substrates by RF Magnetron Sputtering: *Madhana Sunder*[1]; Peter Moran[2]; [1]Bruker AXS; [2]Michigan Technological University

A method to integrate single crystal $SrRuO_3$ perovskite thin films on to commercially available r-plane (102) Al_2O_3 substrates, using RF magnetron sputtering, is investigated. Single crystal pseudo-cubic (001) $SrRuO_3$ is a conducting oxide that is of interest for use as a bottom electrode layer for the subsequent integration of functional single-crystal Lead based relaxor perovskite films on to (102) Al_2O_3. The Al_2O_3 substrates have properties that make them a particularly good platform for relaxor ferroelectric in that they have a low microwave dielectric constant and a low dielectric loss. Till date there are no reports of epitaxial (001)c $SrRuO_3$ growths on (102)Al_2O_3 substrates. This can be attributed to the presence of a large ~12% mismatch experienced between the cations positioned along <100>c and <010>c $SrRuO_3$ and Al atoms positioned along <-2-41> and <-221> Al_2O_3 on the (102) Al_2O_3 growth surface. This mismatch can be hypothesized to be reduced by use of intermediate single crystal buffer layers. One such buffer layer is CeO_2 and it has been widely reported to grow with the (001) orientation on (102) Al_2O_3 substrates. However, in the literature, conflicting results exist for $SrRuO_3$ growths on CeO_2 templates i.e. both epitaxial (001)c $SrRuO_3$ films and polycrystalline films with mixed orientations ((110)c,(001)c) have been reported. This has been postulated in the literature to be due to the impact of surface dipole moments on interfacial energies. We interpret these orientation differences to be the result of interfacial

reactions that take place at the CeO_2-$SrRuO_3$ interface and intend to test it by carrying out depositions under identical conditions on a (001) CeO_2 template and separately on a $YBa_2Cu_3O_7$ coated CeO_2 template. The resultant out-of-plane orientation, in-plane epitaxial relationship, film crystallinity and film thickness are characterized by means of a high resolution X-ray diffractometer. The $SrRuO_3$ films are deposited on 2 inch (102)Al_2O_3 substrates using an ultra high vacuum confocal magnetron sputtering system. When $SrRuO_3$ was grown directly on the CeO_2 buffer layer, a polycrystalline (110)c $SrRuO_3$ film with multiple in-plane arrangements resulted. However deposition of a ~2 nm thick (001) $YBa_2Cu_3O_7$ layer prior to $SrRuO_3$ growth resulted in single crystal (001)c $SrRuO_3$ films. The (001)c $SrRuO_3$ films exhibited a clean interface and a smooth surface morphology (0.4 nm RMS for a 10 µm * 10 µm AFM scan). The films also exhibited a (002)c $SrRuO_3$ rocking curve FWHM of 0.71° and is the narrowest FWHM reported to date for $SrRuO_3$ films grown on CeO_2 templates. The data is interpreted as indicating that (001)c $SrRuO_3$ films result due to the $YBa_2Cu_3O_7$ layer preventing an interfacial reaction between $SrRuO_3$ and CeO_2, that would otherwise result in the formation of (110)c $SrRuO_3$.

11:00 AM Student

Q8, Evidence of Ferroelectricity Induced by Epitaxial Strain in Calcium Titanate Thin Films Grown by Molecular-Beam Epitaxy: *Charles Brooks*[1]; Eftihia Vlahos[1]; Michael Biegalski[2]; Carl-Johan Eklund[3]; Craig Fennie[4]; Karin Rabe[3]; Venkatraman Gopalan[1]; Darrell Schlom[4]; [1]The Pennsylvania State University; [2]Oak Ridge National Laboratory; [3]Rutgers University; [4]Cornell University

$CaTiO_3$ has been predicted by first principles to have strain-induced ferroelectricity. With sufficient tensile strain the development of a polar instability is predicted to occur with polarization along a <110> pseudocubic direction relative to the primitive perovskite lattice vectors. Unlike the strain-induced ferroelectricity observed in $SrTiO_3$ for both compressive and tensile strains, only tensile strain is predicted to induce ferroelectricity in $CaTiO_3$ due to large oxygen-octahedron rotations present in the bulk equlibrium phase of $CaTiO_3$ [1]. In accordance with these predictions, we report evidence of a ferroelectric transition in strained (100) $CaTiO_3$ films grown by molecular-beam epitaxy (MBE). When deposited on $NdGaO_3$ and LSAT $(LaAlO_3)_{0.3}$-$(SrAl_{1/2}Ta_{1/2}O_3)_{0.7}$ substrates at epitaxially-induced tensile strains of 1.1% and 1.3% respectively, 20 nm thick films of $CaTiO_3$ exhibit characteristics consistent with ferroelectricity in both second harmonic generation (SHG) and dielectric measurements. At 20 K the $CaTiO_3$ film on LSAT has a remnant polarization of ~5µC/cm². The film appears fully commensurate by x-ray diffraction with a substrate limited rocking curve full-width at half max of 9 arc seconds. Both capacitance vs. temperature and SHG intensity vs. temperature results agree that the paraelectric-to-ferroelectric transition occurs around 150 K. SHG also confirms the prediction of the polarization direction being along the psuedocubic perovskite <110> direction. [1] C.-J. Eklund, C.J. Fennie, and K.M. Rabe, Phys. Rev. B 79, 220101(R) (2009).

11:20 AM

Q9, Synchrotron Spectroscopy Detection of Spin-Polarized Bands and Hopping-Induced Mixed Valence for Ti and Sc in $GdSc_{1-x}Ti_xO_3$ for x = 0.18 and 0.25: *Gerald Lucovsky*[1]; Leonardo Miotti[1]; Karen Bastos[1]; Carolina Amada[2]; Darrell Schlom[3]; [1]NC State University; [2]Penn State University; [3]Cornell University

Ti substituted for Sc in nano-grain and single crystal complex oxide d^0 $GdScO_3$ films is incorporated in a trivalent state, Ti^{3+}, creating a mixed d^0-d^1 oxide with composition-dependent transport properties, including an insulator to metal transition for compositions in which Ti exceeds a percolation threshold of ~ 16%. X-ray absorption spectroscopy has been used to study occupied electronic states of the Ti^{3+} atoms, and final states for 2p to 3d core level excitations, O 1s core level excitations to virtual conduction band states, intra d-level excitations, and resonant photoemission. These spectrocopies are interpreted in the context of many electron transitions and distinguish between spin alignment in nano-grain films, and single crystal films identifying hopping-induced multi-mixed valency on Ti and Si sites in "Sc-oxide" planes. Inter-atomic transport provides a novel approach to modulate ferromagnetism associated with a double exchange mechanism. i) O K edge X-ray absorption: Comparisons between nano-grain, and epi-thin films demonstrates differences in spin-up and spin-down correlation energy split bands. Second derivative pre-edge spectra indicate a strong spin-up band at low energy, and a weaker spin-up band separated by ~ 1eV in the epi-films. Randomly orientated nano-grains with dimensions < 3 nm, result in a single broad feature that spans width of the two bands in the epi-films. ii) Ti and Sc $L_{2,3}$ spectra for occupied 2p core levels to 3d levels, have identified differences between spectra in alloy films above and below the percolation threshold. Interpretations in the context of many electron charge transfer multiplet methods has identified the steady-state transfer of electrons between occupied Ti^{3+}, and empty Sc^{3+}, states by an intra-layer steady state hopping process: Ti^{3+}, + Sc^{3+}, >/< Ti^{4+}, + Sc^{2+}, equivalently, Ti d^1 + Sc d^0 >/< Ti d^0 + Sc d^1. iii) Resonant photoemission spectroscopy, energy analyzing photoemitted electrons, indicate two resonances for Ti $L_{2,3}$ and Sc $L_{2,3}$ edge valence band spectra. These are distinguished by different energies within the occupied states of the valence band. The Ti $L_{2,3}$ spectra indicate a resonances above $GdScO_3$ valence band: the Ti^{3+} occupied level, and another within the valence band and assigned to Ti^{4+}. The Sc $L_{2,3}$ spectra indicate two resonances as well; one associated with decrease in the concentration of occupied Sc^{3+} states, and the second with increase the concentration Sc^{2+} occupied states. These changes are consistent charge exchange: Ti d^1 + Sc d^0 >/< Ti d^0 + Sc d^1. Finally, the results of this paper indicate the two conditions necessary for double exchange ferro-magnetism, are met by alloying in Ti in $Gd(Sc,Ti)O_3$: (i) mixed valency of in-plane Ti and Sc atoms, and (ii) hopping transport metallic conductivity. Inter-atomic transport then providesa novel way for current controlled double exchange ferromagnetism.

11:40 AM

Q10, Application of Many Electron Charge Transfer Multiplet (CTM) Theory to Band Edge and Band Defect States in High-K Gate Dielectrics and Complex Functional Oxide Thin Films: *Gerald Lucovsky*[1]; Leonardo Miotti[1]; Chung Kwun-Bum[1]; [1]NC State University

The performance and reliability of high-k gate dielectrics, and complex oxides for advanced devices for nano-CMOS and beyond is determined by the densities of intrinsic bonding defects, and defect precursor bonding arrangements. Theoretical studies have addressed O-vacancy defects in transition metal (TM) oxides for gate dielectric applications, e.g., HfO_2 and ZrO_2. However, these have not taken proper account of the strongly correlated character of TM-atom d-states, The defect states energy levels so obtained are inherently flawed: (i) they allow ground state and excited states to have doubly occupancy of electrons, and (ii) they give the erroneous impression that features observed in spectroscopic ellipsometry, and electron and optically excited luminescence are associated with excitations from, and transitions to the top of the valence band. This leads to an incorrect assignment of electronically-active defects: (i) by assigning shallow traps to defect states other than those associated an O-atom, and (ii) by not identifying a fundament relationship between defect states and nano-grain dimensions and thickness constraints. This paper extends many-electron charge transfer multiplet (CTM) methods from transitions in first row TM $L_{2,3}$ spectra in elemental oxides, and to Zr_2 and Y_2O_3 $M_{2,3}$ transitions, O K empty conduction band edge states, and to O-atom vacancy defect states in pre-edge and vacuum continuum regimes. Many electron transitions for d-state transitions (i) at the conduction edge, (ii) in $L_{2,3}$ and $M_{2,3}$ transitions, and (iii) for O-atom vacancy defects characterized by a d^2 state have for the first time been explained by the different, but theoretically equivalent CTM formulations. A vacancy defect is created by removal of a neutral O-atom from a bonding site. Independent of local coordination of O, removal of an O-atom leaves two electrons donated by O-atom TM bonding partners. It is assumed that these electrons are localized on an equivalent TM atom in a d^2 high spin state. For the transitions from this state, final states can be on any of the TM metal atoms bordering the vacancy. This is critical, and agreement with the multiplicity of defects from this final state configuration is more physical than a delocalized distribution that extends the final state wavefunctions well beyond the immediate bounds of the vacancy. An equivalent CTM many electron approach has also been applied to complex oxides; e.g., ABO_3 cubic perovskites, where A is a first or second row d^0 TM metal, and B is a normal metal, Sr or Ba, or a d^0 lanthanide rare earth such as

Gd. The contributions from tA and B atoms are sequenced at the conduction band edge and are attributed to the p-d transitions using CTMs. This is consistent with studies of $L_{2,3}$ spectra for ionic compounds such as the CaF_2 and the halides of K.

Session R: ZnO Growth and Doping

Thursday AM
June 24, 2010

Room: 141
Location: University of Notre Dame

Session Chairs: Dimitris Pavlidis, Technische Universitat Darmstadt; Jamie Phillips, University of Michigan

8:20 AM Student

R1, Nucleation Layer Based Optimization of MOCVD Grown ZnO by In Situ Laser Interferometry: *Jens-Peter Biethan*[1]; Laurence Considine[1]; Dimitris Pavlidis[1]; [1]Technische Universität Darmstadt

ZnO is a transparent direct bandgap (Eg= 3.37 eV) semiconductor material suitable for electronic and optoelectronic applications. Because of its unique properties, ZnO has recently attracted strong attention. ZnO has an outstanding high exciton binding energy (60 meV), comparable to GaN high saturation velocity and better radiation hardness. Its applications vary from sensors and piezoelectric mechanical systems, to optical and electrical components. Various reports addressed Metalorganic Chemical Vapor Deposition (MOCVD) grown ZnO layers on substrates such as sapphire, glass and silicon, but only few results exist on its deposition on GaN. The use of GaN as a substrate can pave the way for the combination ZnO based heterostructures i.e. ZnO/ZnMgO with more mature GaN technology. This paper reports the optimization of high temperature (HT) ZnO layers grown on c-plane GaN layers by studying the impact of nucleation layer (NL) thickness. A modified Aixtron 200/4 MOCVD system was used for the growth. One of the benefits of using GaN as substrate for the growth of ZnO is the relatively small a-plane lattice mismatch between GaN and ZnO of less than 1.9%. Our studies showed that direct growth of ZnO on GaN at high temperatures leads in relatively poor material quality as evidenced by layer cracking and poor structural quality. To ensure better material quality we implemented the well established for the growth of III-V semiconductors approach, where a thin low temperature grown nucleation layer is used first followed by high temperature grown ZnO. The NL was grown at a temperature ranging from 420°C to 450°C while the HT growth of ZnO took place at 750°C. Oxygen (99.9999 %) and DEZ (bath temperature 30°C) were used as precursors while the carrier gas was selected to be nitrogen. A homemade in-situ interferometry system was used to optimize the nucleation layer growth thickness and to determine the growth rate. The growth rate for the HT ZnO was found to be ~2 µm/h. The in-situ characterization technique proved to be extremely helpful for optimizing the growth conditions. XRD characterization of ~1µm thick ZnO demonstrated a decrease of FWHM from 129 to 50 arcsec by decreasing the nucleation layer from 60 to 40nm. The corresponding FWHM PL values at room temperature were about 10 nm. A stronger decay of reflectance oscillations with time was observed for thicker nucleation layers indicating increased surface roughness. The Hall mobility of the grown ZnO reached values of 108 cm^2/Vs. Based on the measured reflectance thickness oscillations and their degradation during high temperature growth, it was found that the nucleation layer thickness necessary for optimum HT growth of ZnO at 430°C is 40 nm - 50 nm. These results are supported by XRD and photoluminescence measurements.

8:40 AM Student

R2, Influence of Substrate Temperature and Post-Deposition Anneal on Material Properties of Ga-Doped ZnO Prepared by Pulsed Laser Deposition: *Robin Scott*[1]; [1]Arizona State University

Dielectric anti-reflective coatings (ARCs) are widely used to improve the efficiency of solar cells and photodetectors. Transparent conductive oxide (TCO) coatings such as indium tin oxide are highly desirable alternatives to dielectrics. With limited indium resources, much effort has been focused on alternative TCOs like Ga-doped ZnO. Employing a variety of deposition techniques, many groups are striving to achieve resistivities below 1×[10]^(-4) ohm-cm with transmittance approaching theoretical limits. In this study, Ga-doped ZnO films were deposited using pulsed laser deposition (PLD) at 10 mTorr between 25 and 600°C. As-deposited samples were then annealed at 350, 400, and 450°C in either forming gas (FG, 5% H2 in Ar) or vacuum at 1.0 × 10-6 Torr. Atomic force microscopy (AFM) was used to characterize surface roughness of the as-deposited and 400°C FG annealed films. Although there were no measured differences in root mean square (RMS) roughness values, comparing as-deposited to FG annealed films, the 1 × 1 µm2 AFM images suggest a coalescing of grains or smoothing of the surface after anneal. TEM images of the film deposited at 200°C reveal no change in bulk crystallography after FG anneal, but the surface is smoother. The total layer thickness has decreased, which is likely attributed to FG etching, consistent with the apparent surface smoothening observed on AFM images. X-ray diffraction (XRD) measurements in the vicinity of the (002) diffraction suggest that films deposited at temperatures of 25 and 100°C have large tensile c-axis strain corresponding to high defectivity, while substantial improvements in quality occur when films are deposited at temperatures ranging from 200 to 500°C. Hall measurements of the as-deposited films show a monotonic increase in carrier concentration with decreasing deposition temperature and substantial increases in both carrier concentration and mobility after anneal in either FG or vacuum. As no discernable differences in structural characteristics were detected by XRD and TEM, this increase in conductivity after FG anneal is attributed to the passivation of the negatively charged oxygen species that create depletion regions at grain boundaries, the breaking of metal oxide bonds at the grain edges, or the activation of dopants in the grains. The changes observed in surface morphology after FG anneal may impact the electrical behavior, but further studies are needed to confirm this. The influence of PLD deposition temperature and post deposition anneal on the material properties of Ga-doped ZnO films was investigated. Films deposited at 200°C and then annealed at 450°C in FG show net carrier concentration of 6×[10]^20 cm-3 and electron mobility of 30.6 cm2/V·s, corresponding to a resistivity of 3.3×[10]^(-4) ohm-cm and a conductivity of 2899 S/cm. Optical transmittance is measured to be greater than 90% over a wide spectral range.

9:00 AM

R3, Epitaxial Electrochemical-Deposition of ZnO on Graphite and p-GaN Substrates: *Kazuyuki Uno*[1]; Yoshinori Ishii[1]; Ichiro Tanaka[1]; [1]Wakayama University

Electrochemical deposition is a convenient and cost-effective method for the crystal growth of ZnO and other oxide semiconductor materials[1]. We have studied on the mechanism of the electrochemical growth of ZnO[2]. The features which we are focusing attention are (1) low growth temperature under 100°C, (2) possibility of nano-scaled selective growth using photo-resist, and (3) high use-efficiency of source material. In this study, we have studied on the epitaxial growth of ZnO by electrochemical deposition on graphite and p-GaN. Graphite substrates employed in this study were highly oriented pyrolytic graphite (HOPG) substrate. p-GaN substrate was an epitaxial thin film grown on sapphire substrates by MOCVD. This study is a demonstration of the growth of ZnO on graphite with no damage as well as the epitaxial growth. ZnO crystals were cathodically deposited using a two-electrode electrochemical cell. The counter electrode was Pt wire, the electrolyte was 0.1mol/L aqueous solution of zinc nitrate, and the deposition-bath temperature was fixed at 70°C. The deposition current density was 0.5mA/cm^2 and the deposition time was 40min. During the deposition of ZnO on p-GaN, 325nm HeCd laser was irradiated on the p-GaN surface to supply electrons for electrochemical reaction by generating electron-hole pairs. The deposited ZnO films had strong c-surface orientations. FWHM of X-ray rocking curve measurements around ZnO (002) was evaluated. The results are as follows: ZnO(002)/HOPG(002)=1.4°/1.3°, and ZnO(002)/p-GaN(002)=0.13°/0.098°. X-ray pole-figure measurements were also carried out for the estimation of axial orientation of ZnO. ZnO on p-GaN had 6-fold rotational symmetry in the observation of ZnO(1101) and GaN(1101). On the other hand, ZnO on HOPG didn't have any rotational symmetry in ZnO(1-102) and HOPG(1-102). This result indicates that polycrystalline ZnO was grown on a polycrystalline graphite substrate. These X-ray diffraction results suggest that

the electrochemical growth of ZnO occurred epitaxially even though the growth temperature is under 100°C. Photoluminescence measurements were also carried out. Excitonic emissions, such as D^0X and its phonon replicas, were observed at 6K. For the ZnO on HOPG, the excitonic emissions could be observed at 220K. On the other hand, for the ZnO on p-GaN, excitonic emissions disappeared over 80K. The thermal quenching property can be explained; the band alignment of ZnO/GaN heterostructure is expected to be staggered[3], so that the thermally excited carriers were separated and recombine non-radiatively with increasing temperature. The feature of current-voltage characteristic supported the staggered type of band alignment. We will present experimental results of the electrochemical deposition of ZnO on pyrolytic graphite sheets (PGSs) and on a thin graphite film which was flaked from HOPG. [1] M.Izaki, *et al.*, Appl.Phys. Lett.68(1996)2439. [2] K.Uno *et al.*, phys. Stat. sol(c) 5 (2008) 3141. [3] Walle *et al.*, Nature 423 (2003) 626.

9:20 AM Student

R4, Control of ZnO Epitaxial Growth via Focused Ion Beam Induced Damage in Lattice-Mismatched Substrates: *Blake Stevens*[1]; Benjamin Myers[2]; Vinayak Dravid[1]; Scott Barnett[1]; [1]Department of Materials Science and Engineering, Northwestern University; [2]NUANCE Center, Northwestern University

A novel method of controlling epitaxy in ZnO films via focused ion beam (FIB) damage of sapphire substrates will be presented. By pre-patterning the substrates with surface lattice damage, crystal orientation can be controlled in subsequent film growth. This eliminates the need for post-deposition treatments to create structural patterning. The concept is demonstrated with the ZnO/Al_2O_3 system, but the method is likely applicable to a range of different epitaxial film/substrate systems. The process efficiency is similar to methods such as electron beam lithography and is much more efficient than typical FIB lithography via surface sputtering or beam induced deposition. In this study patterns on c-plane sapphire substrates were exposed to various ion beam energies and doses using a Ga^+ ion beam in a FEI Helios NanoLab. Patterns were investigated with different shapes (dots, lines, and boxes) and spacing between damaged regions. ZnO thin films were then deposited on these substrates via dc reactive sputtering. The effect of deposition temperature on crystal structure was investigated, with substrate temperatures ranging from 300°C to 700°C. Film thickness effects were also examined. All films exhibited macroscopic epitaxy as verified by x-ray diffraction. To optimize the FIB induced damage mechanism for this process, the balance between ion range, ion sputtering and ion induced lattice damage was investigated using TRIM calculations. The optimum ion energy is achieved when the maximum amount of damage is induced in the near surface of the substrate with the lowest sputtering yield. Energies in the range of 5-15 keV are preferred to balance the surface defect localization and low sputtering yields at low energy with the high defect generation efficiency at high energy. With 5keV ion beam energy, it was found that the ion induced lattice damage with an area dose of 250μC/cm^2 was sufficient to inhibit epitaxial growth. The film above the damaged substrate regions was polycrystalline in nature and exhibited a different surface morphology, as verified by SEM, TEM, and FIB imaging. Cross-sectional FIB imaging showed a dramatic difference in structure due to channeling contrast. A smearing of selected area electron diffraction (SAED) patterns of the ZnO film further confirmed the epitaxial disruption when examining irradiated areas compared to non-irradiated areas. Electron backscatter diffraction (EBSD) also showed an orientation shift in the ZnO deposited above damaged areas. Using a beam energy of 8keV, which gives a smaller spot size, a sub-100nm pattern was achieved in the ZnO film. Further studies on substrate temperature as well as the effect and location of implanted Ga will also be presented.

9:40 AM

R5, Properties of Nitrogen Molecules in ZnO: *Norbert Nickel*[1]; Marc Gluba[1]; [1]Helmholtz-Zentrum Berlin für Materialien und Energie

During growth nitrogen can be readily incorporated to achieve alloying or doping. For ZnO, which is a very promising material for blue and UV light emitting diodes and lasers, the use of nitrogen has been suggested to achieve p-type doping. Unfortunately, the doping efficiency is rather low. To attain a sufficient hole concentration the nitrogen content has to exceed the hole concentration by 4 orders of magnitude and a vacuum anneal at high temperatures is required to activate the acceptors and to remove residual hydrogen from the sample [1]. This extremely low doping efficiency can have its origin in a number of effects. First, ZnO displays a native n-type behavior and thus, the responsible donors have to be compensated by nitrogen acceptors. Second, infrared and Raman measurements have shown that the presence of nitrogen in ZnO gives rise to the formation of N-H, N-O, and C=N complexes [2], in addition to the formation of N2 molecules observed by electron spin resonance measurements [3]. The presence of these complexes will effectively lower the doping efficiency. Using density-functional theory, we show that nitrogen molecules are capable of causing the formation of localized states in the band gap of ZnO, thereby contributing to the low doping efficiency in an hitherto unexpected way. It is found that N2 causes localized states in the band gap either by forming an N2O molecule or by breaking a Zn-O bond. ZnO crystallizes in the wurtzite structure and thus N2 can be accommodated parallel to the c-axis or the basal plane with its unique axis. For the former case the equilibrium position of N2 is located in the center of a hexagon and one N atom resides in the same plane as the surrounding oxygen atoms When the N2 molecule is placed parallel to the basal plane two stable configurations are found. In the first configuration the nitrogen molecule forms nitrous oxide (N2O) by breaking a Zn-O bond. For the second, energetically more favorable site, the nitrogen molecule breaks a Zn-O bond thereby pushing the O and Zn atoms towards the interstitial sites. Although the N2 molecule does not form a chemical bond with the ZnO lattice a localized state appear in the band gap at about 170 meV above the valence band. This state is attributed to an oxygen p-orbital. Our results are discussed in the light of p-type doping of ZnO. [1] A. Tsukazaki, et al., Nature Materials 4, 42-46 (2005). [2] N. H. Nickel, F. Friedrich, J. F. Rommeluère, and P. Galtier, Appl. Phys. Lett. 87, 211905 (2005).[3] N. Y. Garces, L. Wang, N. C. Giles, L. E. Halliburton, G. Cantwell, and D. B. Eason, J. Appl. Phys. 94, 519-524 (2003).

10:00 AM Break

10:20 AM

R6, High-Quality p-Type ZnO Layers Grown by Co-Doping of N and Te: *Seunghwan Park*[1]; T. Minegishi[1]; J.S. Park[1]; I.H. Im[1]; D.C. Oh[2]; T. Taishi[1]; I. Yonenaga[1]; M.N. Jung[3]; J.H. Chang[3]; Takafumi Yao[1]; [1]Tohoku University; [2]Hoseo University; [3]Korea Maritime University

We will report the epitaxial growth of high-quality p-type ZnO layers on Zn-face ZnO substrates by (N+Te) codoping. As-grown ZnO:[N+Te] films show p-type conductivity with a hole concentration of 4×1016 cm-3, while ZnO:N shows n-type conduction. The photoluminescence of ZnO:N shows broad bound exciton emission lines, while ZnO:[N+Te] layers show dominant AoX emission line at 3.359 eV, with a linewidth as narrow as 1.2 meV. Its X-ray linewidth shows narrower line width of 30 arcsec. Detailed investigation of PL properties of (N+Te) codoped ZnO layers suggest that the binding energy of N acceptors lies in a range of 121~157 meV. We note that as-grown (N+Te)-codoped ZnO layers heteroepitaxially grown on sapphire substrates showed n-type conduction, while they were converted into p-type conduction after annealing.

10:40 AM

R7, Magnetic Properties of Mn and N Doped ZnO: *Mathrubhutham Rajagopalan*[1]; S. Ramasubramanian[1]; J. Kumar[1]; [1]Anna University

Transition metal doping in ZnO is being studied extensively both theoretically and experimentally. Room temperature ferromagnetism in Mn doped ZnO was initially predicted but experiments show diverse magnetic properties at low as well as at high temperatures. Double exchange mechanism is proposed to explain ferromagnetism in TM doped ZnO. In the present work the magnetic moment and the magnetic anisotropic energy (MAE) of Mn and N co doped ZnO for two concentrations namely 4.2% and 6.25% are reported. Tight binding linear muffin-tin orbital method and full potential linear augmented plane wave methods are used. The calculations are based on the density functional theory and local spin density approximation. A periodic 2X2X2 and 2X2X3 wurtzite supercell containing 32 and 48 atoms in a unit cell was used. One or two atoms of Zn and O atoms were substituted by Mn and N atoms which give a concentration of 4.2% and 6.25% respectively. Spin polarised electronic

structure calculations are performed and the magnetic moments at Zn, Mn, O and N sites are calculated. For 4.2% concentration the magnetic moments at Mn and N sites are 3.80 µB and -0.07 µB and for 6.25% they are 3.90 and -0.06 µB respectively. The total magnetic moment at 4.2% and 6.25% are 4.00 and 4.20 µB. The total density of states are also calculated for both the spins and are given below. It has been concluded that 4.2% concentration is half metallic whereas 6.25% is metallic. The magnetic anisopropic energies for the various directions namely [0001], [1100], [1000] and [0100] are calculated for both the concentrations. The MAE is maximum for 4.2% along [0001] direction and the value is 1376.16 J/m**3 whereas for 6.25% along the same direction it is 1047.597 j/m**3. It is concluded that 4.2% concentration of Mn and N codoped in ZnO can be used in spintronic devices and the easy magnetising direction is [0001].

11:00 AM

R8, Effects of p-Type Doping on the ZnO Based Diluted Magnetic Semiconductor Thin Films: *Liping Zhu*[1]; Xuetao Wang[1]; Zhigao Ye[1]; Zhizhen Ye[1]; [1]Zhejiang University

Co-N and Ni-Na co-doped ZnO thin films were fabricated on Si(100) and quartz substrates using pulsed laser deposition technique and the influence of p-type doping on the conduction and magnetism of ZnO based thin films were studied. The thin films obtained at optimal condition show magnetism at room temperature. We examined the samples by XRD, SEM, XPS, Hall testing and superconducting quantum interference device (SQUID) magnetometry. The results indicate that the configuration of the thin films is a completely c-axis orientation wurtzite crystal without any Co or Ni related phases. Co and N atoms substitute Zn and O sites in the form of CoZn and NO for the Co-N co-doped samples, while Ni and Na atoms existing in the form of NiZn and NaZn for the Ni-Na co-doped samples. Hall testing and SQUID results indicate that the Co-N and Ni-Na co-doped thin films are p type with higher carrier concentration and magnetization than the Co and Ni doped ZnO thin films respectively. The doped N or Na changes the conduction type and gives rise to the increasing of magnetization of the ZnO based thin films.

11:20 AM Student

R9, Hydrothermal Synthesis of Wide Bandgap $Be_xZn_{1-x}O$ Nanorods for Solar Blind Photodetection: *Ke Sun*[1]; Shrey Prasad[1]; Joe Lee[2]; Bob Olah[3]; Achyut Dutta[3]; Deli Wang[1]; [1]University of California, San Diego; [2]Tanner Research Inc; [3]Banpil Photonic

ZnO is one of the most investigated wide band gap metal oxide, which finds its successful applications in optoelectronics, such as light emitting devices, photovoltaics, photodetectors, and field emission. The formation of nanowires enables charge separation between the nanowire center and the surface, the enhanced carrier lifetime and consequently much increased light responsive for high sensitivity photodetector applications [1]. $Mg_xZn_{1-x}O$ alloys are broadly studied as solar blind photodetectors for military and aerospace applications. By increasing the Mg atomic fraction to x~0.44, the bandgap can be around 4.2eV, leading to the solar blind region. However, crystal phase segregation between ZnO and MgO was observed for Mg concentrations x>0.36, due to the different crystal structures and large lattice mismatch between hexagonal ZnO and cubic MgO [2]. On the other hand, the value of the energy band gap of BeZnO can be efficiently engineered to vary from the ZnO band gap (3.4eV) to that of BeO (10.6eV) [3]. Both ZnO and BeO are hexagonal crystal structure and the a-axis lattice constant values for ZnO and BeO are 3.249 and 2.698 Å, respectively, which is much less than the MgO and ZnO case. In this study, we report our research progress on low temperature synthesis of $Be_xZn_{1-x}O$ nanorods from a mixture solution of beryllium and zinc salt. Two seeding process are studied: 1) decomposing of beryllium nitrate and zinc acetate alcohol solution at temperature higher than 250°C in Ar/N_2 environment produces BeO and ZnO textured seeds [4] for BeZnO nanorods to grow; 2) we also tested is using sputtered ZnO thin film as seeds. Similarly to hydrolysis of Zinc acetate with addition of hexamethylenetetramine (HMTA) for Zn nanowire growth, beryllium nitrate forms tetrahedral beryllium hydroxide with addition of alkalis which is soluble in excess of hydroxide ions thermally released from HMTA. Then, decomposition of $Be(OH)_2$ and $Zn(OH)_2$ in aqueous solution forms $Be_xZn_{1-x}O$ alloy, where the Be concentration is controlled by the initial Be salt concentration in the solution. Higher decomposition temperature (>110°C) is realized by modifying the Ethylene glycol concentration in water. The optical transmission measurement of nanorods array is studied using iHR550 spectrometer mounted with deuterium UV light source. Bandgap of synthesized nanorods is directly calculated from $(\alpha h\upsilon)^2$ vs. $h\upsilon$ plot [5], where a is the absorption coefficient with respect to average length of nanorods. Since Be has light atoms, its concentration is then determined from the calculated bandgap without using sophisticated equipments. Due to the limit of current UV light source (lowest wavelength 200nm), theoretically the maximum Be concentration that can be measured is 39%. To further improve the aspect ratio of the nanorods, surfactant (Polyethylenimine Mw~800) effect [6] is also investigated.

11:40 AM Student

R10, Synthesis and Charaterization of p-NiO/n-ZnO Heterojunction Diode by Spray Pyrolysis: *Namseok Park*[1]; [1]UCSD

Namseok. Park, Ke, Sun, and Deli, Wang Department of Electrical and Computer Engineering, University of California, San Diego, California 92093-0407, USA We report *p-n* heterojunction diodes composed of transparent oxide semiconductors, *p*-NiO and *n*-ZnO. Transparent oxide thin films of NiO/ZnO were deposited on pre-heated ITO glass substrates using a chemical spray pyrolysis technique. Nickel chloride hexahydrate ($NiCl_2 \cdot 6H_2O$) and Zinc acetate dihydrate ($Zn(CH_3COO)_2$) were chosen as a precursor for the deposition of NiO and ZnO, respectively. The NiO/ZnO *p-n* heterojunctions were fabricated by depositing a ZnO layer on NiO layer sequentially. Films are deposited on various conditions. The effect of substrate temperature and solution concentration on the thin films was investigated by structural, electrical and optical properties of films. The as-prepared NiO films were thin gray in color, uniform and strongly adherent to the substrate. The thickness of films was varied from 200 nm to 300 nm. The surface morphology and optical property of fabricated heterojuction were examined by scanning electron microscopy and spectrometer. The NiO thin film was uniform, homogeneous and with a distribution of fine crystallites except for a very few linearly interlinked small particulates embedded over the smooth surface. ZnO thin films demonstrated a better surface smoothness than NiO. We observed that there existed a homogeneous distribution of quite small grains with edge-like shape. The sample prepared at a higher deposition temperature showed smoother surfaces. This is obviously the result of a decrease of the average crystal size by surface diffusion. It was of great importance to minimize the variation of surface morphology of thin films in order to reduce a leakage current at the *p*-NiO/*n*-ZnO heterojunction and contacts. NiO thin films with a transmission up to 75% and absorption less than 2% were obtained. It could be noticed that the ZnO thin films had a high optical transmittance above 90% and also they had an optical absorbance almost zero in the visible range. The average optical transmittance of the heterojunction diode was 80% in the visible range. A silver metal was formed on top of ITO and *n*-ZnO layers to make Ohmic contact between the metal and films to measure electrical properties. The current-voltage measurements of a *p*-NiO/*n*-ZnO heterojunction diode were performed in the dark and under illumination at room temperature. The device demonstrated a clear rectifying behavior with a typical forward-to-reverse current ratio of 10 in the range of -5 to +5 V. The reverse dark current of this device was 30 nA at -5 V. In addition, an apparent forward threshold voltage occurs at 2.5 V.

Session S: Light Emitting Diodes and Laser Diodes

Thursday AM
June 24, 2010

Room: 155
Location: University of Notre Dame

Session Chairs: Russell Dupuis, Georgia Institute of Technology; Theeradetch Detchprohm, Rensselaer Polytechnic Institute

8:20 AM

S1, Effect of Inaln Electron Blocking Layer in Visible Light-Emitting Diodes on Quantum Efficiency Grown by Metalorganic Chemical Vapor Deposition: *Hee Jin Kim*[1]; Suk Choi[1]; Seong-Soo Kim[1]; Jae-Hyun Ryou[1]; P. Yoder[1]; Russell Dupuis[1]; Kewei Sun[2]; Alec Fischer[2]; Reid Juday[2]; Fernando Ponce[2]; [1]Georgia Institute of Technology; [2]Arizona State University

In this study, we proposed active-layer-friendly InAlN layers which which are lattice-matched to GaN as an electron blocking layer (EBL) for visible III-nitride-based light-emitting diodes (LEDs), and investigated the effect of EBL on efficiency droop. The lower growth temperature, higher conduction band offset, and lattice-matching capability of these InAlN layers are considered to enhance the quantum efficiency of visible LEDs such as blue or green LEDs than conventional AlGaN EBLs by reducing thermal damages of the active layer during EBL growth, providing more electron confinement effect and reducing strain induced defect generation. All epitaxial layer structures were grown by low-pressure metalorganic chemical deposition in a Thomas Swan Scientific Equipment 6×2" reactor system on c-plane sapphire substrates. The LED structures consist of a 3-μm-thick Si-doped GaN layer with an electron concentration of n~5×10^{18} cm^{-3}, a five-period InGaN/GaN (2.5/11 nm) multiple quantum well (MQW) active region, a 20-nm-thick Mg-doped $In_{0.18}Al_{0.92}N$ EBL, a Mg-doped $In_{0.03}Ga_{0.97}N$ layer with a hole concentration of p~2×10^{18} cm^{-3}, and a Mg-doped $In_{0.03}Ga_{0.97}N$ contact layer with a doping concentration of [Mg]~1×10^{20} cm^{-3}. Two kinds of lattice-matched InAlN EBL layers were employed in LED structures with different growth conditions. One was grown at 840°C and 300 Torr (labeled as HT-InAlN EBL) and the other was grown at 780°C and 75 Torr (labeled as LT-InAlN EBL). The growth rate of LT-EBL is 0.065 nm/s which is faster than HT-EBL of 0.013 nm/s. LED with a HT- or LT-InAlN EBL show higher EL intensities in EL intensity than LED without InAlN EBL. This result indicates that the InAlN EBLS is effectively confining electrons by preventing them from escaping the MQWs, leading to the improved quantum efficiencies in the green LEDs. Comparing luminous efficiencies between LEDs with HT-EBL and LT-EBL, the integrated EL intensity of LED with LT-EBL is 30% brighter than that of LEDs with the HT-InAlN EBL at J=40.8 A/cm^2. Since LT-EBL growth happens at higher rates and shorter times, our observations suggest that thermal damage in the active layer may have a significant influence on the device efficiency. We also compared device performance of LED with InAlN EBL with LED with conventional AlGaN EBL. By measuring EL at pulse mode, InAlN EBL is more effective in enhancing quantum efficiency as well as in reducing efficiency droop than conventional AlGaN EBL. Detailed experimental results on quantum efficiency and efficiency droop in blue and green LEDs with various EBLs will be presented.

8:40 AM Student

S2, Fabrication of GaN-Based Laser Diode and Laser Diode Facet Formation: *Wenting Hou*[1]; Wei Zhao[1]; Mingwei Zhu[1]; Theeradetch Detchprohm[1]; Christian Wetzel[1]; [1]Rensselaer Polytechnic Institute

GaN-based materials have gained high interest for the fabrication of green, blue and UV light emitting diodes (LEDs) and laser diodes (LDs). Recent remarkable progress towards green laser diodes by several groups has accelerated the field. Here we discuss aspects of our approach to fabricate green laser diodes, namely epitaxial ridge re-growth, metal waveguiding, and focused ion beam (FIB) coupling mirror formation. The conventional way to form a laser current injection ridge is by etching after photolithography. However, there is ample evidence of ion damage to the active region by the high energy ions in ICP/RIE or CAIBE etching. A promising alternative is the selective re-growth of p-GaN and p-AlGaN cladding layer ridge within the openings of a SiO_2 mask. With good optimization, the re-growth results in smoother sidewalls of the ridge than either of the etching processes. Cracking typically observed in AlGaN layers of high AlN fraction on GaN are found to be readily suppressed in the re-growth process of the μm-wide ridge stripes. At the present stage of development, however, a higher forward voltage of 20 V is observed when compared to etched ridge samples at 8 V at the same current of 8 mA (equivalent a current density of 102 A/cm^2) Inconsistency of the p-GaN doping in the re-grown layers is a possible reason, and further optimization is warranted. Optical characterization of a LD structure usually is hindered by the upper cladding layers and p-contact regions. It therefore seems desirable to complete an LD structure only after the active QW region proves promising as determined by optical gain characterization. To this end, LD structures employing a metal mirror are a suitable supplement to complete the optical resonator. Here we employ a layer of silver on top of the p-layers of the ridge and find a substantial reduction in forward voltage and an increase in light output power. The silver mirror enhances the light output power, particularly at the shorter wavelength portion of the emission spectrum. The FWHM of this peak decreases as the current increases, making this the most likely wavelength of anticipated lasing emission. Crystal cleaving is the most straight forward approach for laser mirror formation. Yet, for accurate length control of the cavity, a combination of ICP/RIE etching with focused ion beam milling is a desired alternative for the formation of the second mirror. Here we demonstrate results of various development stages of the laser mirror formation.This work was supported by a DARPA VIGIL program through the United States Air Force AFRL/SNH under FA8718-08-C-0004. This work was also supported by the National Science Foundation (NSF) Smart Lighting Engineering Research Center (# EEC-0812056).

9:00 AM

S3, Performance Improvement of AlInGaN Visible Laser Diodes by Epitaxial Layer Design: *Jianping Liu*[1]; Jeomoh Kim[1]; Zachary Lochner[1]; Seong-Soo Kim[1]; Yun Zhang[1]; Jae-Hyun Ryou[1]; Shyh-Chiang Shen[1]; P. Yoder[1]; Russell Dupuis[1]; Kewei Sun[2]; Alec Fischer[2]; Reid Juday[2]; Fernando Ponce[2]; [1]Georgia Institute of Technology; [2]Arizona State University

AlInGaN-based blue and green laser diodes (LDs) are of interest for applications in full-color displays. We investigated the effect on the performance characteristics of LDs of epitaxial layer design in two aspects: (1) the effect of an electron blocking layer (EBL) by comparing a typical AlGaN EBL with an abrupt step interface from last quantum-well barrier (QWB) and a combined grading/step EBL with compositional grading from last quantum well (QW), and (2) the effect of optical waveguide layers (WGLs) by comparing GaN and InGaN WGLs. We used a graded composition (grading from the InGaN last QW to the AlGaN EBL) in the AlxGa1-xN EBL instead of a constant Al composition used in the conventional EBL design. As a result of the EBL epitaxial layer design change, the device performance shows a reduced threshold current density as well as a higher slope efficiency for LDs using a graded-composition EBL. We believe the graded EBL mitigates band bending in the last GaN QWB and AlGaN EBL caused by the spontaneous and piezoelectric polarization. The grading/step EBL design is expected to enhance carrier (especially hole) distribution in the MQWs for improved LD performance. In addition, the grading/step EBL design is expected to suppress the electron inversion layer that is formed near AlGaN EBL. Due to the smaller difference of refractive index between AlGaN and GaN materials as the wavelength increases, the optical confinement of the waveguide becomes smaller in blue and longer-wavelength LDs. We used InGaN layers for the WGL in blue and longer-wavelength LDs to utilize the larger refractive index contrast for InGaN compared to GaN. The effects of the InGaN waveguide layers on the optical properties are investigated by comparing LDs with GaN and InGaN WGLs. The advantage of enhanced radiative recombination efficiency using InGaN WGLs was also observed in addition to improved optical confinement. The spontaneous EL peak intensity at 50 mA for the LDs with $In_{0.03}Ga_{0.97}N$ waveguide layers is 80% higher than that of the LDs with GaN waveguide layers. Moreover, the FWHM of the EL at 50 mA for the LDs with $In_{0.03}Ga_{0.97}N$ waveguide layers is 27.8 nm, 6 nm lower than that of the LDs with GaN waveguide layers. LDs with $In_{0.03}Ga_{0.97}N$ waveguides lase (pulsed) at λ =454.6 nm at 300K. The threshold current density Jth is 3.3

kA/cm^2 and the threshold voltage is 5.9V. The use of these waveguide designs in the development of longer-wavelength (green) LDs will also be discussed.

9:20 AM Student

S4, Enhancement of the Light-Extraction Efficiency of GaN-Based Light-Emitting Diodes Using a Graded-Refractive-Index Layer: *Byung-Jae Kim*[1]; Joona Bang[1]; Sung Hyun Kim[1]; Jihyun Kim[1]; [1]Korea University

The light extraction of light-emitting diodes (LEDs) was limited by total internal reflection (TIR), which is caused by the large contrast of the refractive index between air (n=1) and GaN (n=2.5). Recently, graded-refractive-index (GRIN) anti-reflection (AR) layer was widely used for increasing the light extraction efficiency by reducing the Fresnel reflection of photons. The refractive index was gradually controlled from the refractive index of GaN to the refractive index of air in GRIN structures. Indium tin oxide (ITO) and TiO2 have been widely used as the materials of GRIN layer due to their transparency. In this study, benzocyclobutene (BCB) was employed as the material of AR layer due to its high optical transparency (>90%) and simple processing scheme as spin-coating technique. Also, BCB was chemically and mechanically very stable material. We fabricated GRIN AR layer by nanospheres lithography (NSL) using SiO2 nanospheres. Firstly, a BCB film with the thickness of 200nm was spin-coated on the LEDs. Then, SiO2 nanospheres with the diameter of 250nm were spin-coated on BCB layer. The sample was heated at 160°C for 5 seconds, so the bottom half of SiO2 nanospheres was embedded into the BCB layer. Then, SiO2 nanospheres were removed by wet etching using HF-based solution. Consequently, the porous BCB layer with the porosity of 70% was fabricated on the BCB layer, so GRIN BCB layer consisted of two layers as BCB layer (n=1.55) and porous BCB layer (n=1.2). GRIN BCB layer was effective to enhance the light extraction efficiency of LEDs due to the reduction of Fresnel reflection and the side wall emission. The optical data as photoluminescence (PL) and electroluminescence (EL) was compared between LEDs samples with/without GRIN BCB layer. The room temperature PL intensity was increased by 29.7% and 61.3% after fabricating BCB layer and GRIN BCB layer on LEDs. Also, the light output at injection current of 10mA was increased by 9.2% and 22% after fabricating BCB layer and GRIN BCB layer on ITO layer of LEDs, respectively. The details about the experiments and the results will be presented.

9:40 AM Student

S5, Nano-Fabrication of Green AlGaInN LEDs – Structural Wavelength Control and Enhanced Light Extraction: *Christoph Stark*[1]; Theeradetch Detchprohm[1]; Christian Wetzel[1]; [1]Future Chips Constellation, and Department of Physics, Applied Physics, and Astronomy, Rensselaer Polytechnic Institute, Troy, New York, USA

Light emitting diodes (LEDs) are normally grown on large wafers and despite strict process control the final emission wavelength can be inhomogeneous across a wafer. This poses a challenge where LEDs with a precisely known color are needed. An ideal solution would be to shift the wavelength after the wafer is grown. Here, green AlGaInN LEDs, grown by MOVPE, are investigated for the possibility to tailor the internal piezo-electric fields and thereby fine tuning the emission wavelength after the growth. This potentially can be achieved by spatial patterning of the wafer on the nano- to micro-meter range. The patterns investigated consist of "finger structures" with up to 100 nano-patterned LEDs connected to a common contact pad. Typical dimensions of the total device area are 150 µm x 100 µm, whereof the "fingers" have a length of 100 µm. The width and spacing are changed for different devices. These structures are generated by electron beam lithography in PMMA photo resist and a durable Nickel hard mask (70 nm) is obtained by electron beam evaporation and a lift-off technique. This metal layer also serves as top contact to the nano-LEDs and eliminates the need to contact the LEDs individually. The pattern is transferred to the LEDs by an inductively coupled plasma (ICP) mesa etch that penetrates through the active region. The nano-LED device geometry is characterized by scanning electron microscopy (SEM) and voltage-current curves are recorded. Sloped sidewalls are observed which increase the device dimensions. If a constant surface leakage current is assumed, the reverse leakage current density for the devices must increases with smaller dimensions, which is in accordance with IV data. The electroluminescence (EL) for devices with structures down to 200 nm is found to have no wavelength shift relative to devices with 1 µm width. But for the smallest realized patterning dimension of 51 nm, a blue shift in the EL is observed at constant current density of 0.03 kA/cm^2. This supports the feasibility of our approach and we pursue further shrinking of the structure size. Observations by optical microscopy show that the EL of nano-patterned region appears 4 times brighter than the region of the device that is used as a contact pad. This can be explained by a higher light extraction efficiency which results from the increased scattering in this unique device design or by an increased internal efficiency due to a reduced number of defects in the nano-patterned LEDs. Acknowledgements: This work was supported by the National Science Foundation (NSF) Smart Lighting Engineering Research Center (# EEC-0812056).

10:00 AM Break

Session T: AlGaN Growth and Devices

Thursday AM
June 24, 2010

Room: 155
Location: University of Notre Dame

Session Chairs: Theeradetch Detchprohm, Rensselaer Polytechnic Institute; Russell Dupuis, Georgia Institute of Technology

10:20 AM Student

T1, Polarization Induced p-Doped Nitride Quantum Well UV LEDs: *Jai Verma*[1]; John Simon[1]; Vladimir Protasenko[1]; Debdeep Jena[1]; [1]University of Notre Dame

UV LEDs can provide compact sources for uses in microscopy, high density optical storage, studying chemical reactions, and water purification. They can be used to irradiate fluorescent materials to produce broadband emission. III-V nitride AlGaN alloys span a wide range of band gaps from 3.4 eV for GaN (UV) to 6.2 eV for AlN (deep UV). Thus AlGaN based device structures can be utilized to produce light of energy higher than GaN band gap energy. But wide bandgap semiconductors suffer from poor p-type doping owing to large activation energy for Mg dopant. The activation energy increases from 200 meV for GaN to 650 meV for AlN. This is much higher when compared to thermal excitation energy at room temperature (26 meV). III-V nitrides also have large built-in polarization field with spontaneous and strain induced piezoelectric components. GaN QWs have been incorporated into p-n junction UV LED structures that did exploit polarization-induced p-type doping, but had no such wells. Compositionally grading GaN to AlGaN on N-face GaN substrate had led to polarization induced p-type doping. Improved p-type doping resulted in efficient hole injection into the active layers giving higher EL intensity. Moreover, the graded layer provided an electron barrier which is evident by the band diagram. The UV LEDs studied here were grown on n-type N-face GaN free-standing substrates by Plasma Assisted Molecular Beam Epitaxy (PAMBE). Free standing GaN substrates have low dislocation densities (~5e7 cm^{-2}) ensuring low non-radiative recombination rates. An initial growth thermocouple temperature of 600°C is used which is then gradually increased to 660°C and decreased back to 600°C. The nitrogen RF power is kept at 275W throughout the growth. To achieve compositional grading, the Al cell temperature is increased using a computer program while keeping the Ga cell temperature constant. Si and Mg are used for n- and p-type doping. X-ray Diffraction (XRD) and Atomic Force Microscopy (AFM) studies indicate that the intended graded layers and intended GaN quantum wells embedded in AlGaN barriers was successfully realized. We perform mesa etch using ICP and, deposit Ni/Au for p-type contact and Ti/Au for n-type contact to process the grown structures into UV LEDs. The Electroluminescence (EL) spectrum obtained for the GaN QW structure at an injection current of ~75 mA shows a peak at 380 nm, with a shoulder in the spectrum which extends to wavelengths below 360 nm. The emission at energies higher than the bandgap energy of GaN can be attributed to recombination in the graded AlGaN layer. This observation of successful incorporation of quantum wells, and electroluminescence from

AlGaN regions indicate that $Al_xGa_{1-x}N$ QWs and $Al_yGa_{1-y}N$ barriers can now be used to obtain respectable emission intensities for deeper UV or higher energy photons.

10:40 AM

T2, Structural Characterization of Highly Conducting $Al_xGa_{1-x}N$ (x >50%) for Deep Ultraviolet Light Emitting Diode: *Joseph Dion*[1]; Bin Zhang[1]; Qhalid Fareed[1]; Asif Khan[1]; [1]Nitek, Inc.

Research interest in the III-Nitride deep ultraviolet (UV) light emission devices has significantly increased over the past few years. Their potential as a replacement for mercury lamps in several bio-medical, air-water purification and germicidal systems is one of the key drivers for this research. Due to the transparency requirements, the substrate choices for the sub-300 nm AlGaN deep UV surface emission devices, such as light emitting diodes (LEDs), are limited to either single crystal sapphire or AlN. The $Al_xGa_{1-x}N$ multiple quantum well (MQW) based deep UV light emission devices over either of these two substrate types require heteroepitaxy. Highly conductive, high composition (>50%Al) nAlGaN layers are critical to the development of high power deep ultraviolet light emitting diodes. The development of these layers is plagued by the tendency of AlGaN films grown on sapphire to crack. This limits the thickness, and therefore conductivity, that can be achieved. Previous research has shown the beneficial effect of inserting an AlN/AlGaN superlattice (SL) on AlN buffers layers to mitigate cracking1. In this research, the strain relaxation of AlGaN films grown on AlN/Sapphire templates was investigated by off-axis reciprocal space mapping (RSM). Four samples are compared in this study. All samples include a standard AlN buffer layer on sapphire, comprising a high temperature annealing step followed by low temperature AlN nucleation layer and high temperature AlN Pulsed Atomic Layer Epitaxy (PALE) layer. Sample A is a continuous growth of the AlN buffer layer followed by an AlN/AlGaN SL, a thin undoped AlGaN layer and thick silicon doped nAlGaN layer. For Sample B, a template was grown up to the thin undoped AlGaN layer. This template was then used for growth of a thick nAlGaN layer. For Sample C, the same nAlGaN layer was grown directly on a previously grown AlN buffer layer. For Sample D, an AlN/AlGaN SL, a thin undoped AlGaN layer and thick silicon doped nAlGaN layer were grown on a poorer quality AlN buffer layer. The results indicate the nAlGaN films growing on AlN on sapphire templates initially grow in compression, nominally lattice matched to the relaxed AlN buffer layer. This compressive strain is gradually relieved during the course of the thick nAlGaN growth. Relaxed, uncracked nAlGaN films can be grown on high quality AlN layers, with or without inserting a SL. The growth interruption in Samples B and C appears to allow the growth of an unstrained nAlGaN layer without a gradual release of compressive strain. However, on poor quality AlN layers, even the insertion of a superlattice does results in less compressive strain relief. The results will be discussed in detail.

11:00 AM

T3, Epitaxial Growth and Doping of AlGaN Alloys on AlN Single Crystal Substrates: *Ramón Collazo*[1]; Seiji Mita[2]; Jinqiao Xie[2]; Anthony Rice[1]; James Tweedie[1]; Rafael Dalmau[2]; Zlatko Sitar[1]; [1]North Carolina State University; [2]HexaTech, Inc.

As the building blocks of current deep UV light emitting diode technology and high-power electronic devices, AlGaN alloys have attracted considerable attention. In this study, AlGaN films with varying compositions and doping levels were deposited on homoepitaxial AlN layers grown on AlN single crystal substrates. The mismatch between film and substrate causes a compressive strain within the AlGaN layers, varying with composition. Typical engineered relaxation methods include controlled dislocation nucleation or "bending" of existing dislocations from the substrate to provide for the misfit component. Nevertheless, these relaxation mechanisms are based on introducing dislocations into the films which could have an adverse effect on electronic performance. If relaxation is not essential for a given application, relaxation schemes can be avoided altogether in favor of pseudomorphic AlGaN films on AlN. However, this approach may limit the practical range of AlGaN compositions for pseudomorphic structures. In order to study this effect and the effects on n-type doping, AlGaN films of compositions above 60% Al content and thickness around 400 nm were grown by MOVPE on templates consisting of 200 nm thick c-plane homoepitaxial AlN layers on AlN substrates. For the templates, after nitridation of the AlN substrate surface, 200 nm thick AlN films were deposited at a temperature of 1220ºC in a mainly hydrogen atmosphere. AlGaN layers were then deposited at a temperature of 1100ºC by introducing the Ga precursor. Structural characterization was performed by acquiring on- and off-axis x-ray diffraction ω-rocking curves, indicating that the films followed the mosaic structure of the substrate. The reflections in a ω-2θ scan from the (002) planes of AlN and AlGaN can be observed along with Pendellösung thickness fringes around the AlGaN peaks of films with compositions above 80% Al. The occurrence of these fringes was qualitatively attributed to the high quality of the films and interfaces. A partial relaxation of 8% was only observed for the AlGaN film with 65% Al content and 400 nm thickness. For compositions above 65% Al, the films were pseudomorphic. A reciprocal space map of the asymmetric (105) reflection from an AlGaN film with 88% Al content indicated no relaxation. A comparison of the room temperature resistivity of different AlGaN alloy compositions grown on AlN and sapphire substrates with a constant Si doping level of $6x10^{18}$ cm^{-3} was established. AlGaN films grown on AlN substrates consistently exhibited a lower n-type resistivity than those grown on sapphire. An n-type resistivity of 0.1 Ω cm was obtained for an AlGaN film with 80% Al content. The carrier activation energy as a function of Al content in AlGaN for these n-type films was measured. The observed trends will be discussed in light of impurity potential screening and the expected activation energy.

11:20 AM Student

T4, Morphological Development of Homoepitaxial AlN Thin Films Grown by MOCVD: *Anthony Rice*[1]; Ramon Collazo[1]; Seiji Mita[2]; James Tweedie[1]; Jinqiao Xie[2]; Rafael Dalmau[2]; Zlatko Sitar[1]; [1]North Carolina State University; [2]HexaTech, Inc.

AlN thin films were grown on single crystalline (0001)-oriented, Al-polar AlN substrates by metalorganic chemical vapor deposition (MOCVD) to determine the effects of deposition parameters on the thin film microstructure. AlN deposition was conducted at 1100–1250°C under 20 Torr total pressure in H_2 diluent. Trimethylaluminum and ammonia were used as precursors with V/III ratios of 250-500. Triple axis high-resolution x-ray diffraction measurements of the (0002) Bragg peaks of AlN thin films indicated that the films were epitaxial and strain-free. Atomic force microscopy characterization suggests step-flow growth with bi-layer terrace widths of 40 nm and 130 nm for AlN films deposited at 1100°C and 1250°C, respectively. Periodic crystalline faceting was observed with alternating high symmetry (0001) facets and high Miller index facets. The periodic spacing of such facet arrays varied from 80 nm to 450 nm for substrates miscut relative to (0001) by 13° and less than 1°, respectively. Hexagonal pits of up to 800 nm width and 400 nm depth were observed in AlN homoepitaxial thin films deposited at 1100°C. Such pits exhibited an inverted hexagonal pyramid morphology with sidewalls inclined ~45° relative to the surface normal for films deposited on (0001)-oriented substrates. For substrates miscut 13° from (0001), the inclination of pit sidewalls perpendicular to the miscut direction became ~30° or ~60° relative to the surface normal. The average dimension of such pits was found to increase with epitaxial film thickness for AlN deposited at 1100°C: the average pit widths were 400 nm, 600 nm, and 800 nm for film thicknesses of 1 µm, 2 µm, and 3 µm, respectively. No pitting was observed in homoepitaxial AlN thin films deposited at 1250°C. However, pit formation was also observed for multi-layer AlN thin films that consisted of an AlN layer deposited at 1250°C and a subsequent AlN layer deposited at 1100°C. The pit dimensions observed in such multi-layer AlN thin films were found to depend only on the thickness of the layer deposited at 1100°C and were similar to pit dimensions in single-layer AlN thin films of equal thickness deposited at 1100°C. These results are consistent with observations of V-shaped defects in other III-nitride materials in which treading dislocations possessing an edge component intersecting the crystal surface may yield hexagonal pitting. Increasing the radius of curvature of bi-layer terraces by increasing the deposition temperature was found to inhibit the formation of such pits, as predicted by capillary equilibrium theory, but does not prevent the later formation of pits during subsequent deposition at lower temperatures.

11:40 AM Student

T5, Aluminum Gallium Nitride Alloys Grown via Metal Organic Vapor Phase Epitaxy Using Digital Alloy Growth Technique: *L Rodak*[1]; D. Korakakis[1]; [1]West Virginia University

Deep Ultra Violet (UV) emitters are of particular interest for applications including, but not limited to, biological detection and sterilization. Aluminum Gallium Nitride ($Al_xGa_{1-x}N$) alloys are of well suited for UV applications due to the wide direct bandgap that spans the UV range unlike any other direct semiconductor. When grown via Metal Organic Vapor Phase Epitaxy (MOVPE), Al containing alloys are inherently difficult to grow due to the short diffusion length of the Al species and also the high reactivity of the Al containing precursors [1]. This requires high growth temperatures and low reactor pressures when compared GaN growth conditions. As such there has been considerable interest in the development of alternative growth techniques which yield high quality $Al_xGa_{1-x}N$ films [1]. Additionally, strain management in $Al_xGa_{1-x}N$ containing structures is challenging due to the large lattice and thermal mismatches between the binary components. Strain engineering is important to minimize or eliminate certain defects detrimental to device efficiency, such as dislocation or crack formation, and also due to the influence it has on band engineering in this piezoelectric material system [2]. Therefore the development of strain compensating growth techniques remains of critical importance for the fabrication of high quality devices. This work investigates the use of a digital alloy technique as a viable growth method for $Al_xGa_{1-x}N$ alloys and also the influence of different buffer layers on the growth. Digital alloy growth, often called short period superlattices, consists of layers of binary or ternary alloys with a period thickness of a few monolayers (ML) and has previously been reported to be a suitable means of growing III-Nitride alloys [1,3], although most commonly employed in MBE growth. This work targets AlN/GaN superlattices grown on sapphire substrates via MOVPE. The effective AlN mole fraction is varied from 0.2 to 0.9 by adjusting the thickness of the AlN layer. Specifically, the superlattice structures under investigation contain approximately 4 ML of GaN and 1 ML or more of AlN. High resolution X-Ray Diffraction (XRD) is used to determine the superlattice period and c-lattice parameter of the structure, while off-axis XRD reciprocal space maps are used to determine the a-lattice parameter and evaluate the coherency of the growth. The strain in the structures is calculated by comparing the extracted a-lattice parameter to the nominal parameter for an $Al_xGa_{1-x}N$ film with a corresponding AlN mole fraction. $Al_xGa_{1-x}N$ films grown on both AlN and GaN buffer layers are investigated and the impact on the strain formation will be discussed. [1] M. E. Hawkridge et al. Appl. Phys. Lett. 94, 071905 (2009). [2] P.K. Kandaswamy et al. J. Appl. Phys. 106, 013526 (2009).[3] V.N. Jmerik et al. J. Cryst. Growth 311, 2080 (2009).

Session U: Graphene and Nanotubes - Devices

Thursday PM
June 24, 2010

Room: 102
Location: University of Notre Dame

Session Chairs: Huili Grace Xing, Univ of Notre Dame; Debdeep Jena, Univ of Notre Dame

1:30 PM Student

U1, Sub-20 nm Patterning of Graphene Nanoconstrictions Using Nanosphere Lithography and Characterization of Its Electronic Properties: *Nathaniel Safron*[1]; Michael Arnold[1]; [1]University of Wisconsin-Madison

Graphene has accumulated scientific and technological interest due to its unique physics and exceptional electronic properties. The mobility of carriers in pristine graphene exceeds any known material at room temperature, which, coupled with its extremely high thermal coefficient and current density, make it a suitable candidate material for future electronics. However, due to its semi-metallic band structure, the measured ON/OFF ratios of pristine graphene are limited to ~30, even at low temperature. Experimental work has shown that lateral confinement of graphene to sub-20nm dimensions in graphene nanoribbons can induce higher switching ratios by patterning with E-beam lithography or the unzipping of carbon nanotubes. We have recently demonstrated a self-assembly technique to pattern nanoperforated graphene, where a periodic array of holes are etched into a graphene sheet. The resulting graphene material is a 2D-honeycomb, which has sub-20nm nanoconstrictions between the holes. To achieve this patterning resolution, we have implemented a well-studied self-assembly technique, Nanosphere Lithography, and tailored the process conditions to produce a high-fidelity pattern over entire substrates. Briefly, polystyrene nanospheres are self-assembled into a close-packed hexagonal monolayer through surface-tension effects during controlled drying. Using the nanosphere template, we deposit an aluminum oxide precursor via spin-coating which fills the interstices between the spheres in the template. After oxidation of the alumina precursor, the spheres are removed by chemical solvent leaving an oxide honeycomb pattern defined over the substrate. Utilizing a directional reactive ion etch, we can transfer the pattern to the underlying graphene, creating a honeycomb pattern in graphene. By controlling the etching conditions, we have demonstrated control of the transferred nanoconstriction width from 17 - 7 nm. To test the effect of nanopatterning on the electronic properties of graphene, we have fabricated four-wire field-effect devices of pristine, mechanically-exfoliated graphene, and monitored the effect of each processing step. We have demonstrated that the room-temperature switching ratio of the nanostructured graphene varies inversely with constriction width with ON/OFF ratios of up to 450 for the smallest constriction widths of w = 7 nm with field-effect mobilities of ~1 cm2/Vs. We have observed that the minimum conductance of the nanoperforated graphene follows an Arrhenius behavior with temperature, similar to what would be expected for a small-band gap semiconductor. We have determined the effective transport gap of nanoperforated graphene with constriction widths of w=15 nm to be 54 meV. We attribute the enhanced switching ratio of nanopatterned graphene both to the opening of a band gap and due to Coulomb blockade effects, which have been characterized at low temperature. Additionally, our patterning technique enables large-scale construction of 2D arrays of grapheme nanoconstrictions into designed device structures, enabling a multitude of new experimental measurements.

1:50 PM Student

U2, Carrier Transport in Graphene P-N Junctions: *Tian Fang*[1]; Kristof Tahy[1]; Aniruddha Konar[1]; Huili Xing[1]; Debdeep Jena[1]; [1]University of Notre Dame

High carrier mobility and perfect two-dimensional (2D) structure make graphene a promising material for applications in high speed electronic devices. P-N junctions can enable a number of electronic devices, such as tunneling field effect transistors (TFET). Graphene P-N junctions have been realized experimentally by exploiting electrostatic doping. In this work we present theoretical calculation of I-V curves of graphene p-n junction and the corresponding experimental measurements. Graphene is a zero bandgap material. However, in a graphene p-n junction carriers have to tunneling through an effective bandgap formed by the requirement of lateral momentum conservation. In the calculations we assume the electron transport across p-n junction is ballistic. The p-n junction currents include tunneling and thermal emission current. In a forward biased p-n junction, the electrons with low energy can tunnel through the junction and higher energy electrons can go to drain directly by thermal emission. At high bias the thermal current will be dominant. In a reversed biased p-n junction the tunneling current is dominant. Here, we ignore other recombination processes, such as Auger recombination, in the middle of a forward biased p-n junction. We assume the doping electrodes have good electrostatic control of the carriers in the channel, so that the p-n junction is short enough for ballistic transport. In the diffusive transport regime, we have to include other recombination processes. I-V curve calculations show the reverse biased current is dominantly by the tunneling component thus then does not depend on temperature. The forward biased p-n junction has a thermal emission component so the I-V curves show clear temperature dependence at high bias condition. Graphene p-n junctions were achieved by electrostatic doping in our lab. A 30nm wide raphene channel is deposited on a 300nm thick SiO2 substrate. The carrier density in the channel can be modulated by the back gate voltage

along the channel from source to drain. Half of the channel is covered by a top gate. The top gate dielectric is 15nm thick Al2O3 which is deposited by ALD. The carrier density in the channel under the top gate is controlled by both top and back gates. By changing the voltages of the two gates, the channel can be set to p-p, n-n, n-p or p-n dopings. The conductance measurement shows the p-n and n-p channels show comparable conductance to n-n and p-p channels. In conclusion, we have experimentally achieved graphene p-n junctions using a back and a top gate by electrostatic doping. The I-V curves of p-n junctions are calculated theoretically, and are compared with the experimental data.

2:10 PM

U3, Epitaxial Graphene Materials Integration: Effects of Dielectric Overlayers on Structural and Electronic Properties: *Joshua Robinson*[1]; Michael LaBella[1]; Kathleen Trumbull[1]; Xiaojun Weng[1]; Randall Cavalero[1]; Tad Daniels[1]; Zachary Hughes[1]; Matthew Hollander[1]; Mark Fanton[1]; David Snyder[1]; [1]Penn State University EO Center

The realization of a graphene-based electronic technology necessitates large-area graphene production, as well as the ability to integrate graphene with highly insulating films that act as the gate dielectric in field effect transistors (FETs). The use of high-k dielectric materials in graphene-based FETs is also of interest because of the reduced coulombic scattering of charge carriers, and enhanced charge carrier mobility. Although the use of high-k dielectric materials may limit graphene mobility through phonon scattering, graphene FETs fabricated with high-k dielectric materials still outperform those utilizing SiO2. Atomic layer deposition (ALD) provides a means to produce high quality films for gate dielectrics at temperatures below 300C, and has proven to be an excellent technique toward the integration of dielectrics with graphene. However, because ALD is a water-based technique, graphene must undergo surface preparation processes that will permit the deposition of a uniform dielectric film. Previous reports suggest that functionalization of graphene via ozone, nitrogen dioxide, or perylene tetracarboxylic acid (PTCA) prior to ALD of Al2O3 can result in more uniform dielectric film coverage on graphene, with fewer examples of uniform deposition on pristine graphene. Additionally, successful integration of Al2O3 and HfO2 has been accomplished by depositing a thin (2 – 5 nm) metallic Al or Hf film via physical vapor deposition, which fully oxidized when exposed to atmosphere, and served as a uniform nucleation layer for subsequent ALD processing. We present a means to integrate the high-k dielectric materials Al2O3, HfO2, Ta2O5, and TiO2 with epitaxial graphene, compare surface pretreatments, and provide electronic and structural characterization of the dielectric materials on graphene. We present evidence that, uniform coverage of ALD dielectric films on epitaxial graphene is possible through the use of a nucleation layer and optimization of deposition temperature. Additionally, deposition of dielectric materials via ALD impacts the structural and electronic quality of epitaxial graphene. In some cases, atomic layer deposition of high-k dielectrics can improve the mobility of epitaxial graphene by up to 22%, however, most situations result in mobility degradation. The deposition of Al2O3, HfO2, and TiO2 are shown to introduce minimal degradation of the epitaxial graphene structural properties, while Ta2O5 can significantly degrade the graphene structural quality. Finally, we discuss the use of multilayer films that provide uniform coverage and minimal degradation of epitaxial graphene's electronic and structural properties.

2:30 PM

U4, Comparison of Ballistic Performance of Graphene and Planar III-V MOSFETs for RF Low Voltage Applications: *Lingquan (Dennis) Wang*[1]; Vincent Lee[2]; Francisco Lopez[2]; Yuan Taur[2]; Jeong Moon[3]; Peter Asbeck[2]; [1]University of California, San Diego/Global Foundries; [2]University of California, San Diego; [3]Hughes Research Laboratories

Graphene is under study as a MOSFET channel material due to its high carrier velocities, ~10_8cm/sec for electrons and holes. The high carrier velocities even at low kinetic energies are favorable for low operational voltages. Narrow bandgap III-V materials (InSb, InAs and InGaAs, also with peak electron velocities ~10_8cm/sec) are also candidates for high frequency operation at low bias. In this work, we compare the theoretical performance of graphene and narrow bandgap III-V MOSFETs. Our analysis is carried out for the ballistic transport limit, since future high performance devices will likely have gate lengths near or below the carrier mean free path. Our analysis explicitly accounts for the nonparabolic conduction band in III-V's. Our results show that graphene is expected to exhibit superior on-current and transconductance. The device performance is examined from three perspectives: average carrier injection velocity v_{inj} at the virtual source; sheet charge density (Ns) at the virtual source; and ballistic current. Average velocity: For graphene, v_{inj} remains constant at 2vd/p (~6x107 cm/s), regardless of Ns (vd Dirac velocity). For III-V materials, vinj for low carrier densities is determined by (2kT/pm*)1/2 (InSb: 4.6x107 cm/s, In0.47Ga0.53As: 2.7x107cm/sec) and increases with Vgs as the carrier population reaches degeneracy. Due to strong non-parabolicity in III-V's, vinj depends on channel thickness, and gradually saturates at high Ns, becoming comparable to vinj in graphene. The critical value of Vgs where vinj saturates depends on oxide capacitance, and is near Vgs-Vt=0.5 V for InSb at equivalent oxide thickness (EOT) of 1 nm. Ns at the virtual source: For graphene transistors, charge is confined within the graphene layer, avoiding gate capacitance degradation due to finite centroid depth of the electron wavefunction as occurs in III-Vs. The graphene density of states capacitance also benefits from 2x Dirac point degeneracy. Sheet charge density in graphene transistors consists of both electron and holes. Although the overall Ns at the virtual source remains constant as Vds varies, sheet electron and hole densities individually change. Higher Vds results in more holes at the virtual source. For charge balance, more electrons must be present, leading to increasing electron density with increasing Vds. For unipolar devices, however, holes are absent; since increasing Vds discourages backward going electrons, electron density decreases with increasing Vds. Ballistic Current: Combination of large Ns and high vinj at all Ns levels leads to higher drain current for graphene. For representative 1nm EOT case, the ballistic current (transconductance) for a graphene transistor is 1.8mA/m (4.3mS/m), compared to 0.44mA/m (1.9mS/m) for In0.47Ga0.53As, 0.48mA/m (2.1mS/m) for InAs and 0.45mA/m (1.9mS/m) for InSb (Vgs-Vt=Vds=0.3V). However, given ambipolar conduction within graphene transistors, devices may not turn off at low gate bias. Circuit design thus must accommodate a limited ON/OFF current ratio.

2:50 PM

U5, Graphene Fundamental Trade-offs and Asymmetric Bandgap Opening: *Frank Tseng*[1]; Avik Ghosh[1]; [1]University of Virginia

Graphene's tunable energy bandgap has raised considerations as a future candidate for logic devices, although its small band-gap limits its ON-OFF ratio to only around 50, inadequate for digital logic. Regardless of the limited success using current lithographic techniques there is still research interest in extending graphene's bandgap. However, extension of the graphene bandgap comes at a *fundamental cost to mobility* due to an asymptotic constraint on its short wavelength bandstructure. In evaluating materials for future electronic devices it is useful to analyze and compare fundamental material trade-offs using a *three-parameter analysis* of bandgap, mean-free-path and mobility (Eg-λ-μ). From our three-parameter (Eg-λ-μ) we find that for graphene samples where λ<100nm, graphene actually performs worse in terms of electron mobility compared to some III-V semiconductors such as Indium Antimonide (InSb) and Gallium Arsenide (GaAs) with corresponding bandgaps. Fundamentally, extending the bandgap decreases the low-energy curvature and increases the effective mass, as at higher-k the dispersion is asymptotically pinned to its original linear form. We show a way to quantify this fundamental trade-off for all graphitic materials including, monolayer and bilayer graphene, carbon nanotubes, and strained graphene nanoribbons. Recent experiments have also shown 'kinks' in the IV-characteristics due to band-to-band tunneling, as well as current 'saturation' even for zero bandgap graphene. We point out that a linearly decreasing density in 2D-bulk graphene creates only an inflection in the IV as a graphene device inverts its conduction mechanism. Indeed, only a bandgap can create a plateau in the ballistic graphene IV, long enough for current to be truly considered independent of voltage (current-saturation). Scattering mechanisms inherent to graphene or from interfacing materials can add extra degrees of complexity to understanding properties of graphene-based devices. Using a non-equilibrium green's function (NEGF) formalism for transport and self-consistent Born Approximation to model the affect of phonons, we find that graphene's inherent acoustic phonons lower its mobility. Recent results showing asymmetry

between N and P-type conduction in 2D-bulk graphene can be attributed to an asymmetric bandgap opening relative to the Fermi energy; consequently, the electron and hole effective masses are different. From an asymmetric IV we can extract useful parameters such as mobility from the IV slope and bandgap from the voltage width of current plateau and contact capacitances. In addition, the N-to-P type current saturation ratios and the three-parameter (Eg-λ-μ) analysis together are useful in determining λ and providing a quantitative illustration of the asymmetric bandgap opening.

3:10 PM Break

3:30 PM

U6, Hall Effect Mobility of Epitaxial Graphene on Si-Face SiC: *Shin Mou*[1]; John Boeckl[1]; Jeongho Park[1]; Kurt Eyink[1]; David Tomich[1]; John Hoelscher[2]; Lawrence Grazulis[3]; Steve Smith[3]; Weijie Lu[4]; William Mitchel[1]; [1]Air Force Research Laboratory; [2]Wright State University; [3]University of Dayton Research Institute; [4]Fisk University

Graphene has recently attracted a lot of interest as a promising material for next-generation electronic devices such as digital switches and radio-frequency transistors. A key material parameter driving the interest in this material is the Hall mobility and 300 K mobilities greater than 10,000 cm2/Vs have been reported. However, there are only a few studies relating the Hall mobility to carrier densities and other material properties in a systematic way. Therefore, in this study, we report Hall mobility as a function of carrier densities under different growth conditions. Epitaxial graphene films were grown on 10x10 mm^2 samples diced from CMP polished (0001) semi-insulating on-axis SiC wafers. Ultra high vacuum (~ 1E-10 Torr base pressure) and Argon atmospheric pressure sublimation processes were used over a range of growth temperatures and times. Hall mobilities were measured on both bulk samples (10x10 mm^2 and 4x4 mm^2) and small van der Pauw (vdP) crosses of various sizes (width from 2 μm to 250 μm). The values of mobility obtained are within the range of 100 – 500 cm2/Vs. The general trend is that a higher mobility often correlates to a lower carrier density. Raman spectroscopy and X-ray photoemission spectroscopy were used to confirm the presence of graphene. Atomic force microscope was used to characterize the surface morphology and also transmission electron microscope was used to confirm the number of layers of graphene films. The correlation between mobility, growth condition, and morphology are described in order to relate the growth conditions to the values of Hall mobility. The variation within small vdP crosses and the size dependency are also studied. Generally, there are local variations across the wafer but the median mobility values are consistent with those of the bulk measurement from the same 10-10 mm2 sample. Raman mapping, AFM, and XPS measurements are done on local small vdP crosses to find the correlation between local morphologies and Hall mobilities. Generally, higher Hall mobility value often correlates to better uniformity in terms of the morphology. Thus, for the expitaxial graphene grown on (0001) SiC face growth conditions that give smoother morphology and also lower carrier concentration at the same time are needed to optimize the mobility.

3:50 PM Student

U7, Highly Efficient Photovoltaic Devices with Transparent Graphene Electrode and TiOX Layer: *Minhyeok Choe*[1]; Byoung Hoon Lee[1]; Gunho Jo[1]; June Park[2]; Woojin Park[1]; Sangchul Lee[1]; Woong-Ki Hong[1]; Maeng-Je Seong[2]; Yung Ho Kahng[1]; Kwanghee Lee[1]; Takhee Lee[1]; [1]Gwangju Institute of Science and Technology; [2]Chung-Ang University

Graphene, an ultra-thin two-dimensional sheet of covalently bonded carbon atoms, has been attracting great attention in the field of optoelectronics of organic and inorgranic materials. This is because of its outstanding electronic, optical, and mechanical properties, such as quantum electronic transport properties, transparency, mechanical and chemical stability, stretchability, and flexibility. Recently, graphene-based thin films have attracted tremendous attention as a noble transparent electrode material because they are chemically and mechanically robust, electrically conductive, and optically transparent. Our focus is on the application of graphene films as transparent electrodes for organic photovoltaic cells. We present the synthesis of multi-layer graphene (MLG) films by chemical vapor deposition (CVD) and their applications to organic photovoltaic cells. Our MLG films possessed sheet resistances of ~606 /□ at transmittances of ~87% and showed good performance as electrodes for organic photovoltaic cells. Furthermore, cell structure optimization with an inserted TiOX layer enhanced the observed power conversion efficiency up to 3.63% which is the highest efficiency reported for photovoltaic cells with graphene-based electrodes to date.

4:10 PM Student

U8, Integrated Circuits Based on Carbon-Nanotube Transistors and Amorphous-Carbon Thin-Film Load Resistors: *Hyeyeon Ryu*[1]; Daniel Kaelblein[1]; Frederik Ante[1]; Ute Zschieschang[1]; Oliver Schmidt[2]; Hagen Klauk[1]; [1]Max Planck Institute for Solid State Research; [2]Chemnitz University of Technology

Integrated circuits based on carbon-nanotube transistors are potentially useful for electronics on unconventional substrates. From a circuit-design perspective, complementary circuits are preferred, but are difficult to realize, since carbon nanotubes typically only show p-channel behavior. Unipolar circuits require load devices that must have a large resistance to provide gain above unity. In thin-film circuits, load devices are often realized with transistors biased in saturation and having a large length/width ratio. But the resistance of carbon nanotube devices is not a simple function of the length, and the output swing of saturated-load inverters is diminished by the threshold voltage of the load. As an alternative to transistor-based load devices we have developed a low-temperature process to fabricate thin film resistors with linear characteristics and resistances that are easily tuned to provide large gain. We demonstrate the integration of nanotube transistors and thin-film resistors into circuits with full output swing and integrated level-shifting to account for positive threshold voltages. The transistors have aluminum gates patterned by electron beam lithography. The gate dielectric is composed of 3.6 nm thick AlOx (obtained by plasma oxidation) and a 2.1 nm thick organic monolayer (prepared from solution). The carbon nanotubes are deposited from a liquid suspension. Using AFM, an individual nanotube is located on each gate, and AuPd source/drain contacts are defined by e-beam lithography. The best transistors we have obtained have a transconductance of 6 μS, an on/off ratio of 10^7, and a subthreshold slope of 100 mV/decade. Based on the gate capacitance (50 fF) and the transconductance, a cutoff frequency of 20 MHz is projected for these transistors. Load resistors are fabricated by depositing a thin layer of amorphous carbon by RF sputtering and lithographic patterning. Depending on the film thickness, the sheet resistance is between 10^6 and 10^7 Ω/sq. Depending on the geometry, resistances between 10^5 and 10^8 Ω can be designed. Integrated circuits are completed by connecting transistors and resistors with metal interconnects defined by e-beam lithography. Inverters composed of a carbon-nanotube transistor and a carbon load resistor have full output swing, small-signal gain up to 10, and switching frequencies up to 2 MHz.Since our transistors have positive threshold voltages (~0.3 V), the input and output levels of the inverters do not match (the input requires a positive signal to turn the transistor off, but the output produces only negative signals). Therefore, these inverters cannot be cascaded. To realize circuits with matching input and output levels, a level-shift stage composed of two carbon resistors is integrated with each inverter. The level-shift stage translates each input signal towards more positive values and thus allows the inverter to work properly without positive input signals.

4:30 PM

U9, Late News

4:50 PM

U10, Late News

Session V: Quantum Dots, Boxes, and Wires

Thursday PM
June 24, 2010

Room: 126
Location: University of Notre Dame

Session Chairs: James Merz, University of Notre Dame; Diana Huffaker, University of California, Los Angeles

1:30 PM

V1, Toward Conversion from Electron Pairs to Photon Pairs in Quantum Dots: *Ikuo Suemune*[1]; Yasuhiro Idutsu[1]; Makoto Takada[1]; Hirotaka Sasakura[1]; Hidekazu Kumano[1]; [1]Hokkaido University

Quantum information communication and processing are expected to form next-generation highly secure quantum-information networks (QIN). Single photons generated from semiconductor quantum dots (QDs) are expected to play as messenger qubits in QIN. Especially generation of quantum-entangled photon pairs (QEPP) is regarded to be an important key issue to further extend QIN and it has been actively studied to realize on-demand QEPP sources with QDs. Biexciton-exciton cascade photon-pair emission is the major scheme to pursue this direction. But fine-structure splitting (FSS) of exciton states is the widely recognized difficult problem at present. Also it is difficult to realize simultaneous QEPP generation based on spontaneous emissions in QDs in such a manner as the parametric down conversion of an external laser excitation source. In this paper, new possibility of generating QEPP simultaneously with spontaneous emissions in QDs is discussed. Biexciton(XX) and exciton(X) states in a QD generally have different binding energies due to the Coulomb attractive and repulsive forces among the electrons and holes. This results in different oscillator strengths of XX and X and leads to the sequential single photon spontaneous emissions. This is an intrinsic property and seems to be difficult to change. However, this situation can be changed by introducing an additional attractive force between electron pairs [1, 2]. It is well-known that electrons form Cooper pairs below critical temperature via phonon-assisted attractive force between electrons. Recently inter-band radiative recombination processes of electrons and holes in semiconductors were analyzed including the effect of the Cooper-pair formation (the proximity effect) based on second-order perturbation theory[3]. This analysis shows that pairing of spin-singlet electrons drastically enhances the radiative recombination with a pair of holes. Such a drastic enhancement of electroluminescence (EL) has been observed from light emitting diode (LED) with niobium superconducting electrodes [4]. This theory suggests the QEPP generation in this device. These theoretical and experimental results show the possibility of new-type of radiative recombination processes in semiconductors. However for the control of the number state of generated QEPP, inclusion of QDs in the radiative recombination process is essential [2]. The basic requirements to achieve this scheme and the QD-related experiments demonstrating Cooper-pair-based recombination are discussed. For the confirmation of the generated QEPP with high fidelity, it is also required that the generated QEPP are efficiently extracted to the outer optical transmission systems. Some trials towards this direction is also discussed. [1]E. Hanamura, Phys. Stat. Solid. (b) 234, 166 (2002). [2]I. Suemune et. al., Jpn. J. Appl. Phys. 45, 9264 (2006). [3]Y. Asano etal, Phys. Rev. Lett. 103, 187001 (2009). [4]Y. Hayashi etal Appl. Phys. Express 1, 011701 (2008).

1:50 PM

V2, Tensile-Strained Self-Assembled III-V Nanostructures: *Paul Simmonds*[1]; Minjoo Lee[1]; [1]Yale University

We report the first self–assembled growth of dislocation-free, highly uniform, *tensile-strained* III-V nanostructures on a (110) surface. Devices fabricated on the (110) plane of III-V semiconductors could have several advantages over their (001) surface counterparts. Due to suppression of the in-plane Dresselhaus field,[1] carrier spin-lifetimes in (110)-oriented quantum wells can be significantly longer than in equivalent (001)-oriented structures.[2] Additionally, spin-lifetimes can be lengthened by carrier confinement within self-assembled quantum dots (SAQDs).[3] Incorporating the attractive properties of (110) surfaces with SAQDs is expected therefore to lead to novel devices with potentially very long spin-lifetimes. Long spin-lifetime is a fundamental requirement for many spintronic applications. Driven by compressive strain, SAQDs are readily formed in the well-established InAs/GaAs(001) and Ge/Si(001) systems. In contrast, deposition of compressive materials on other low-index surfaces such as (110) typically results in heavily dislocated two-dimensional films.[4] Achieving the combination of SAQDs with a (110) surface has thus been highly challenging. However, analyses of dislocation energetics and kinetics indicate that the strain relaxation behavior of (001)-oriented material can be replicated on (110) surfaces provided the *direction of strain* is inverted.[5] As such, by analogy to compressively strained SAQDs on (001) surfaces, sufficient *biaxial tension* could result in the self-assembly of dislocation-free nanostructures on (110)-oriented material. To establish the validity of this prediction, we used molecular beam epitaxy to deposit tensile-strained GaP on GaAs(110) surfaces. We discovered that GaP spontaneously forms three-dimensional nanostructures at terrace edges on the GaAs surface. Straightforward control of nanostructure size is demonstrated without the bimodality encountered in (001) SAQDs. The nanostructures exhibit high shape and size uniformity, with smaller dots showing no evidence of dislocations in cross-sectional transmission electron microscopy. Tuning of the growth parameters enables control of nanostructure density. No wetting-layer is observed prior to dot formation, which implies a Volmer-Weber growth-mode for the GaP nanostructures. This study represents a proof of concept for self-assembled growth driven by tensile strain on a (110) surface. It is anticipated that this will form the first step towards a more general description of epitaxial nanostructure self-assembly. [1] V. Sih et al., *Nat Phys* 1, 31 (2005). [2] G.M. Müller et al., *Phys. Rev. Lett.* 101, 206601 (2008). [3] L.M. Woods et al., *Phys. Rev. B* 66, 161318 (2002). [4] B.A. Joyce and D.D. Vvedensky, *Mat. Sci. & Eng. R* 46, 127 (2004). [5] E.P. Kvam and R. Hull, *J. Appl. Phys.* 73, 7407 (1993).

2:10 PM Student

V3, Self-Assembled $In_{0.5}Ga_{0.5}As$ Quantum Dots on GaP(001): *Yuncheng Song*[1]; Paul Simmonds[1]; Minjoo Lee[1]; [1]Yale University

We demonstrate growth of $In_{0.5}Ga_{0.5}As$ self-assembled quantum dots (SAQDs) on GaP as a step towards the integration of efficient optoelectronic III-V materials with Si. Although high-quality GaP has been grown on Si, [1-3] its indirect bandgap makes it unsuitable for most photonic applications. Use of dilute-nitride and boron-containing alloys to achieve a direct bandgap on GaP/Si have yielded promising results, [1, 2] but these complex alloys are not fully understood. GaAsP or InGaP buffers can be grown on GaP/Si to attain a direct bandgap, but the additional thickness resulting from grading can cause problems due to thermal expansion mismatch. To avoid these issues, our approach to obtaining light emission on GaP was to start with the well-established $In_xGa_{1-x}As$ material system. $In_xGa_{1-x}As$ on GaP offers both a direct bandgap and suitable carrier confinement. However, the lattice mismatch between $In_xGa_{1-x}As$ and GaP is too large (4-10%) to permit growth of high-quality quantum wells. Instead, we proposed that this high strain could result in the formation of $In_xGa_{1-x}As$ SAQDs, thus providing a relatively simple route to achieving light emission on GaP. We used MBE to deposit various thicknesses of $In_{0.5}Ga_{0.5}As$ on GaP(001). Streaky 2x4 RHEED patterns during homoepitaxy at 590°C indicated that the GaP buffers were smooth, and an RMS roughness of 0.81nm over an area of $(10\mu m)^2$ was measured by AFM. After GaP buffer growth, samples were cooled to 490°C and $In_{0.5}Ga_{0.5}As$ was deposited at 0.2ML/s with V/III ratio ~40. After an initial wetting layer of ~1.1ML, the RHEED pattern changed from streaky to spotty, indicative of the Stranski-Krastanov (S-K) growth mode. The $In_{0.5}Ga_{0.5}As$/GaP QD densities ranged from $2\text{-}7x10^{10}$ cm^{-2} as $In_{0.5}Ga_{0.5}As$ coverage was increased from 1.23–1.95ML, similar to the dot densities in the well-known InAs/GaAs (001) system. [4] Over this $In_{0.5}Ga_{0.5}As$ thickness range, average dot size remained constant, to within error, at ~17 nm in diameter and ~2.5 nm in height. Based upon the common cation and common anion rules, $In_{0.5}Ga_{0.5}As$ SAQDs on GaP are expected to provide effective confinement for both electrons and holes. Further optical and structural characterization will be presented. This work demonstrates the ability to grow $In_{0.5}Ga_{0.5}As$ SAQDs on GaP(001) via the S-K mechanism. We believe that these results are the starting point for a promising new approach to III-V optoelectronic device integration on Si. [1] B.

Kunert, et al, phys. stat. sol. (b) 244, 2730–2739 (2007) [2] H. Yonezu, et al, J. Cryst. Growth, 310, 4757–4762 (2008) [3] T. Grassman et al, Appl. Phys. Lett, 94, 232106 (2009) [4] D. Leonard et al, Phys.Rev. B 50, 11687–11692 (1994)

2:30 PM Student

V4, Time-Resolved Spectroscopy of Single Colloidal CdSe Nanowires with Picosecond Resolution: *Joseph Herzog*[1]; Alexander Mintairov[1]; James Merz[1]; [1]University of Notre Dame

Nanowires (NWs) have the potential to enhance the speed and efficiency of optoelectronic devices; however, there is much unknown about the physics of these colloidal nanowires. Time-resolved (TR) spectroscopy provides useful information about these nanostructures. In the present study we performed TR spectroscopy at low temperatures (~10K) in order to study the emission properties of single colloidal CdSe nanowires (NWs) with diameter ~20 nm. A streak camera with resolution up to 8 picoseconds (pulse width) was used with a micro photoluminescence (μPL) setup to achieve micron spatial resolution measurements on several individual nanowires. We excited the NW samples with the second harmonic of a Ti-sapphire laser (wavelength at 400 nm, pulse frequency of 76 MHz) with a power density reaching the sample that can range from 100 W/cm2 to 25 kW/cm2. We also measured μPL spectra with an 80x, NA = 0.75 micro objective using the pulsed laser. Wide field luminescent images taken with the micro-objective verified that individual nanowires are measured. Low temperature TR spectroscopy of single nanowires shows a red-shift as a function of time which increases with power. At the largest pump powers (25kW/cm2) the spectra peak shifts ~20 meV within 500 psec. The shift is reduced but observable at lower pump powers, e.g., 1.4 meV in 500 psec for 200 W/cm2. In addition to the peak energy shift, the spectra half-width also decreases with time and pump power. At large pump powers the spectra emission range (FWHM) decreases ~40 meV in 500 psec. The peak energy shift as a function of time suggests that excitons populate many discrete localized states ranging in energy. At low temperature excitons are prevented tunneling to lower states before they recombine [1]. We believe that these states come from traps in the nanowire. The larger power densities create more excitons that fill more traps of various energy levels; this causes the largest energy shift in the emission. Work was supported by the National Science Foundation, NSF-NIRT grant No. ECS-06 09249. We are greatful to, Dr. M. Kuno, Chemistry Department, University of Notre Dame, for the NW samples. [1] J.J. Glennon, R. Tang, W. E. Buhro, and R. A. Loomis. Phys. Rev. B 80 081303(R) 2009.

2:50 PM

V5, Late News

3:10 PM Break

3:30 PM

V6, Resonant Periodic Gain InAs Quantum Dot VECSEL: *Alexander Albrecht*[1]; Christopher Hains[1]; Thomas Rotter[1]; Andreas Stintz[1]; Kevin Malloy[1]; Ganesh Balakrishnan[1]; [1]University of New Mexico

Edge-emitting semiconductor lasers based on MBE-grown, self-assembled InAs quantum dot (QD) active regions emitting around 1300 nm have demonstrated excellent device performance, including low sensitivity to operating temperature and record-low thresholds. The application of QDs in vertical-cavity lasers requires the stacking of several QD layers to achieve sufficient gain for lasing. The resulting accumulation of strain can affect material quality and degrade device performance. In this investigation we compared two different arrangements of the QD active regions in a vertical-external-cavity surface-emitting laser (VECSEL) structure, both utilizing a total of 12 InAs QD layers, each embedded inside an InGaAs quantum well. The first, a more traditional VECSEL design consists of groups of 3 closely spaced QD layers placed at 4 adjacent antinodes of the optical standing wave. The second structure employs a purely resonant periodic gain (RPG) structure, with each of the 12 QD layers placed at a separate electrical field antinode. This design allows for greater spacing between the InAs layers, greatly reducing the negative effects of strain accumulation. The devices were mounted to a thermo-electrically cooled stage using thermal grease. A fiber-coupled 808 nm diode laser was used as pump source, focused to a 300 μm diameter spot on the semiconductor surface. A 1% transmission output coupler with 25 cm radius of curvature completed the VECSEL cavity. CW operation was achieved with thermally limited output powers of 400 mW for the RPG structure, compared to only 100 mW for the traditional design. Making use of the growth non-uniformity across the 3 inch GaAs substrate, the operating wavelength could be tuned from 1220 nm to 1280 nm.A portion of the RPG sample was thinned by mechanical polishing to 100 μm and the chip was bonded with indium to a thermal grade polycrystalline CVD diamond heat spreader of 300 μm thickness. The resulting assembly was clamped in a water cooled copper heat sink maintained at a temperature of 20°C. This greatly increased the usable pump power before thermal rollover, resulting in 2.5 W of cw output power, the first reported multi-Watt level QD VECSEL around 1250 nm.

3:50 PM

V7, Quantum Dot Light Emitting Devices and Exciton Recombination Zone: *Seonghoon Lee*[1]; [1]Seoul National University

Colloidal quantum dot (QD)-based light-emitting diodes (QLEDs) have the advantageous features of a narrow emission bandwidth, a wide emission spectral window in the visible region, and a low-cost synthesis based on a solution process. For the realisation of full-colour displays and solid-lighting applications with QLEDs, the development of a fabrication process for the deposition of homogeneous and uniform QD layers over a large area with patterning capability is necessary. Here we present QLEDs over a large area via the elaboration of all-QD multilayer films prepared by a layer-by-layer assembly method, which possess excellent device–performance. From the systematic analysis of the exciton-recombination zone within all-QD multilayer films using a sensing QD layer, optimal QD coverage was found to be 1.2 ~ 1.5 monolayers for the best QLED performance. The total EL emission came mostly at the top QD monolayer (~ 90%) and partially at the second QD monolayer from the top. Multi-coloured QLEDs were also demonstrated by controlled arrangement of variously coloured QDs (red, orange, yellow–green, and green) in the exciton-recombination zone. Practical large-area RGB QLED and flexible solid-state white light emitting devices can be produced.

4:10 PM Student

V8, Thermal Stability in Emission Peak in Multilayer InAs/GaAs Quantum Dot Heterostructure in Laser Application: Nilanjan Halder[1]; Sourav Adhikary[1]; *Subhananda Chakrabarti*[1]; [1]IIT Bombay

Self assembled quantum dots (QDs) are of substantial interest in laser device fabrication due to the strong localization of electronic wave function in these systems leading to an atomic-like density of states. Stacked InAs/GaAs QDs are used in the active region of the laser structures, which increases the active volume of the device and permits to realize enhanced modal gain and low threshold current of the devices. The high temperature growth of AlGaAs-cladding layers for the laser structures leads to pronounced blue-shifting of emission from the QDs caused by In/Ga inter-diffusion. This is undesirable for DFB lasers and VCSELs requiring strict tolerances on operating wavelength. We have investigated the annealing of MBE grown InAs/GaAs multilayer (x10) QDs (MQD) with a combination capping layer of InAlGaAs (30Å) and GaAs (180 Å). The capping/barrier thickness in the MQD samples is optimized in order to produce a 10 layer heterostructure having almost structurally correlated islands upto the final (10th) layer. No frequency shift in the peak emission wavelength is seen even for annealing the samples up to 700°C. XTEM images of the stacked QD samples revealed that the QDs are preserved even annealing up to 800°C, while dissolution of the QDs into the surrounding wetting layer occurred at 850°C. To explain the thermal stability in the emission wavelength a single layer QD (SQD) sample with similar combination cap thickness as the multilayer structure was grown. The peak emission wavelength (1162nm) of the MQD sample remains relatively stable at higher annealing temperatures (upto 700ºC) than the SQD sample. PL spectrum of the as grown MQD sample contains two peaks separated from each other by 125 meV, indicating that the peaks are due to two different families of dots and with increasing annealing temperature only one single peak at 1162 nm becomes prominent due to redistribution of In adatoms leading to a more uniform dot size density. Suppression of the strain-enhanced intermixing in QD microstructures can be ascribed for the

thermal stability of the PL peak. In both the samples there is very less material intermixing at the periphery of the QDs due to the quaternary alloy cap, which creates a In rich region along the QD periphery thereby preventing the strain enhanced In/Ga inter diffusion. But the material intermixing from the barrier at the QD base still continues in the SQD sample during annealing due to the usual compressive strain at the base of the pyramidal QDs, where as in the MQD sample the intermixing at the base is suppressed due to the overlapping vertical strain from the under lying dot layers in the QD stack which maintains a strain relaxed state at the QD base. Acknowledgment: DST, India.

4:30 PM
V9, Enhancement of Luminescence Efficiency in InAs/GaAs Quantum Dots by Proton Irradiation: Sreekumar Rajappan Achary[1]; Saumya Sengupta[1]; *Subhananda Chakrabarti*[1]; Shrikrishna Gupta[2]; [1]Indian Institute of Technology Bombay; [2]Bhabha Atomic Research Centre

Quantum dot (QD) based devices are emerging as an alternate platform for quantum well based devices. Low threshold current density and the ability to tune the emission wavelength from 1500 nm to 1100 nm makes InAs/GaAs QDs more attractive for applications in lasers, infrared detectors, focal plane arrays and in telecommunication. Lots of research is being carried out to improve the characteristics of QDs to reach the theoretically expected device efficiency. One of the major characteristics of InAs/GaAs based QDs, that is being worked on is the photoluminescence (PL) efficiency to realise highly efficient low-threshold QD lasers. To improve the PL efficiency in InAs/GaAs QDs, different techniques are such as deuteration, nitrogen treatment on the QDs before capping, stacking of multi-layers of QDs, and QDs grown in dot-in-the-well structure are used. Leon et al. [1] observed a marginal enhancement of PL efficiency in InGaAs/GaAs QDs due to proton irradiation. The present work elucidates a detailed study on the enhancement of PL efficiency induced by proton irradiation in self assembled InAs/GaAs quantum dots grown over GaAs substrate. Protons of energies ranging from 3 MeV to 5 MeV are used to irradiate QDs. The optimum energy (4 MeV) and fluence required to obtain maximum PL efficiency is investigated. X-ray diffraction analysis showed an enhancement in crystalline quality of the GaAs capping layer. Low temperature PL study exhibited a increase of PL efficiency (upto 7-fold) with increase in proton fluence. The enhancement of PL efficiency is attributed to the annealing of structural defects present in the GaAs matrix that act as a non-radiative recombination centres and release of strain between the QDs and the capping layer, induced by proton irradiation. FWHM of the ground state PL emission decreased from 27.77 meV to 21.29 meV on increasing proton fluence. The thermal spike generated (for few tens of pico second duration) during the passage of protons could have helped to anneal the structural defects and promoted greater homogeneity in size distribution. A similar type of observation was reported by Chakrabarti el al. using nano second pulsed laser annealing on InAs/GaAs QDs [2]. The activation energy of the sample irradiated with protons showed a higher value of 365 meV compared to the as-prepared samples (126 meV). The increase in activation energy depicts the increase of quantum confinement in QDs induced by proton irradiation. Thus by proton irradiation one could enhance quantum confinement and PL efficiency of QDs, which would benefit QD resonant microcavity LEDs and VCSELs, that has limited number of QDs in active region. Financial assistance from DST, is being kindly acknowledged. [1] R. Leon et al., Appl. Phys. Lett. 76, 2074 (2000). [2] S. Chakrabarti et al., J. Electron. Mater. 33, L5 (2004).

4:50 PM
V10, Late News

Session W: Semiconducting and Metallic Nanowires

Thursday PM
June 24, 2010

Room: 129
Location: University of Notre Dame

Session Chairs: David Janes, Purdue University; Xiuling Li, University of Illinois

1:30 PM Student
W1, Single Crystalline Wurtzite GaAs Nanoneedles Epitaxially Grown on Highly Lattice-Mismatched Sapphire with Bright Luminescence: *Wai Son Ko*[1]; Linus Chuang[1]; Michael Moewe[1]; Kar Wei Ng[1]; Shanna Crankshaw[1]; Thai-Truong Tran[1]; Roger Chen[1]; Connie Chang-Hasnain[1]; [1]University of California, Berkeley

Heterogeneous integration of dissimilar single-crystalline materials, such as III-V compound on Si or sapphire, enables functionalities and performance that cannot be achieved with single material system. Yet, lattice mismatch makes growing high quality thin film on dissimilar substrates difficult. Recently high quality nanowires have been demonstrated on substrates with large lattice mismatches [1]. However, in that case, there exists a critical nanowire diameter for a given mismatch, below which single crystalline can be obtained. This, in turn, presents an upper bound of the substrate lattice mismatch to ~15%, on which nanowires with physically meaningful diameters can be attained with the growth of three-dimensional nano-structures. In this paper, we report a completely new growth mechanism that leads to self-assembled, single crystalline GaAs nanoneedles grown on a sapphire substrate with 46% lattice mismatch. The needles exhibit a single crystalline wurzite phase, have a sharp hexagonal pyramid shape and can be scaled to micron size with growth time. The GaAs nanoneedles were grown on a (0001) sapphire substrate in a commercial MOCVD at 400°C. The growth was spontaneous without any prior substrate surface treatment. At typical growth condition, the nanoneedle shows a hexagonal base, six slanted sidewalls and a sharp tip. With one-hour growth time,the nanoneedle has a base diameter of ~600 nm and a height of ~3 μm. Furthermore, high-resolution TEM shows that the tip is ~ 3 nm wide, and the needle has a taper angle of ~11°. TEM and diffraction analysis reveals that the NN has single-crystalline wurtzite structure as opposed to the normal zinc-blende GaAs structure. The effect of growth condition on nanoneedle was studied by varying the growth time. When the growth time was varied, the base dimension and height of the nanoneedle scales linearly, maintaining the same taper angle, even when the growth time was only 1.5 min. This suggests that the nanoneedle nucleates as a seed and grows with a two-dimensional thin-film deposition process on the six sidewall facets. Despite the large 46% lattice mismatch, the NN shows bright photoluminescence. A 514 nm excitation laser is focused down to a ~1.5 μm spot. With 100 μW excitation power, the NN shows emission peak at 1.519 eV at 4 K. The linewidth of the peak is 18 meV. This narrow linewidth indicates the excellent crystal quality of the NN. These high-quality GaAs NNs open an opportunity for integrating high-performance electronic and optoelectronic devices onto highly lattice-mismatched substrates. [1] L. Chuang *et al*, *Appl. Phys. Lett.* 90, 043115 (2007).

1:50 PM
W2, Twinning Superlattice in VLS Grown <110> Planar GaAs Nanowires Induced by Impurity Doping: *Xiuling Li*[1]; Ryan Dowdy[1]; Seth Fortuna[1]; Donald Walko[1]; Jian-Guo Wen[1]; [1]University of Illinois

Self-aligned, twin-free, planar <110> GaAs nanowire growth by metal-organic chemical vapor deposition (MOCVD) through the vapor-liquid-solid (VLS) mechanism has been demonstrated by our group recently (Fortuna, Wen and Li, Nano Letters, 2008). Well-defined transfer and output characteristics with bulk-like mobility have been reported from MESFETs fabricated using these planar nanowires intentionally doped by silicon as the channel materials (Fortuna and Li, IEEE Electron Device Letters, 2009). In this paper, the planar nanowire growth is perturbed by introducing p-type dopants in situ. Twinning superlattice planar nanowires, which could be useful for miniband related

devices, are reported.At doping levels as low as 0.008% Zn/Ga (gas phase ratio), periodic notching along the axis of the nanowire is observed. The notches are confirmed to be <111> twin-plane defects by transmission electron microscopy (TEM), which lead to a <110> planar nanowire superlattice structure with <111> twin-planes. Note that the twin plane superlattice is formed at constant Zn flow without any modulation, and its periodicity corresponds to the nanoparticle catalyst size at a ratio of ~ 0.9. At Zn/Ga gas phase ratio of 0.8% or higher, the nanowire propagate incoherently out-of-plane. There appears to be an incubation period for Zn incorporation and accumulation effect which renders delay in the twinning and causes initially twinned planar nanowires to take off from the plane. In comparison to <111> vertical III-V nanowires, the threshold of impurity level for such structural perturbation is orders of magnitude lower. These observations underscore the atomic nature of the nucleation process in the VLS mechanism, where any perturbation at atomic level such as dopant incorporation can be critical to the free energy of the interface not only between metal catalyst and semiconductor solid surface, but also at the three-phase boundary. In particular, planar nanowires reported here, where this three phase region is not symmetric, can be more easily perturbed to induce structural changes.

2:10 PM Student

W3, Photoluminesence of InGaAs Nano-Pillar Arrays on GaAs Substrate: *Joshua Shapiro*[1]; Adam Scofield[1]; Clayton Tu[1]; Diana Huffaker[1]; [1]UCLA

Catalyst free growth of uniform arrays of InGaAs nanopillars with varying indium fraction on gallium-arsenide (111)B substrate by selective area MOCVD is reported. Pillar formation is studied as a function of pillar diameter. Compositional analysis is determined by energy dispersive spectroscopy and confirmed by temperature dependent photo-luminesence(PL). PL emission at 77K from two different samples with indium fractions of 0.24 and 0.48 is intense at 1.1µm and 1.43µm respectively. Faceted pillars with vertical side walls and a flat hexagonal top surface and with diameters from 100nm to 350nm were formed for estimated indium fraction of 0.24. Pillars with diameters < 200nm are well formed for estimated indium compositions of 0.48, however larger diameter begin to coalesce with their neighbors.

2:30 PM Student

W4, Synthesis and Characterization of GaAs/MnAs Core/Shell Nanowires: *Nicholas Dellas*[1]; Jing Liang[1]; B.J. Cooley[1]; Dave Rench[1]; Jeremy Cardellino[1]; Nitin Samarth[1]; Suzanne Mohney[1]; [1]Pennsylvania State University

Hybrid semiconductor/ferromagnetic heterostructures are of interest for injection of spin polarized currents into semiconductors for spintronic applications. Here we have synthesized GaAs/MnAs core/shell nanowire (NW) heterostructures by catalyst-free molecular beam epitaxy (MBE). Transmission electron microscopy (TEM) reveals that the GaAs core grows with the zinc-blende crystal structure with a [111] growth direction, and in a small population of wires, the crystal structure transitions from zinc-blende into the wurtzite phase with a [001] growth direction. Cross-sectional TEM shows that the MnAs grows epitaxially in the NiAs prototype structure on zinc-blende GaAs core with an epitaxial relation of [201]MnAs||[111]GaAs and (010)MnAs||GaAs(-110). When the GaAs core is found to be in the wurtzite structure, the epitaxial relation between the GaAs and MnAs changes to [001]MnAs||[001]GaAs and (-120)MnAs||(-120)GaAs. Preliminary magnetic force microscopy measurements of these NWs indicate the presence of ferromagnetic domains at room temperature, consistent with the magnetic properties of bulk MnAs crystals which typically have a Curie temperature of 318 K. This work is supported by NSF under the MRSEC program and the NNIN.

2:50 PM Student

W5, Contact Laser Annealing Effects on Indium Oxide Nanowire Transistors: *Seongmin Kim*[1]; Sunkook Kim[1]; Chunghun Lee[1]; Pornsak Srisungsitthisunti[1]; Pochiang Chen[2]; Chongwu Zhou[2]; Xianfan Xu[1]; Minghao Qi[1]; Saeed Mohammadi[1]; Sanghyun Ju[3]; David Janes[1]; [1]Purdue University; [2]University of Southern California; [3]Kyonggi University

Wide band-gap oxide nanowires, such as ZnO, SnO_2 and In_2O_3, are attractive candidate for next-generation electronics, because of their high mobilities and compatibility with low temperature processes. Nanowire transistors (NW-FETs) using these materials could provide the drive electronics for future transparent/flexible displays, based on their optical transparency and mechanical flexibility. Recent studies report several methods to prevent threshold voltage degradation in oxide semiconductor (ZnO and In_2O_3) based-TFT devices. In order to move toward future commercial nano-electronics, it is also necessary to improve and stabilize the transistor characteristics of nanowire devices and to understand the mechanisms responsible for the current-voltage relationships. We have fabricated In_2O_3 NW-FETs using Al and ITO metal contacts, and studied the effects of annealing via femtosecond laser pulses focused on the contact regions. The n-channel NW-FETs utilized single-crystal In2O3 nanowires (d ~ 20 nm) and channel lengths of 1.5-2 microns. In order to investigate the effects of post-metallization S/D annealing, the device electrical characteristics were measured before and after annealing. The Ids-Vds curves of as-fabricated devices deviate significantly from the expected response of a long-channel transistor even at Vds values expected to be in the saturation region, and exhibit significant gds. The annealing induces significant positive shifts in the threshold voltage, a reduced saturation drain voltage and a significantly reduced drain conductance (g_{ds}) in the saturation region, along with modest improvements in the subthreshold slopes. Fully transparent NW-FETs were also fabricated utilizing ITO contacts and glass substrates. After laser annealing the ITO contacts, the threshold voltage is positively shifted, and slight improvements in Ion/Ioff and effective mobility are observed. A small reduction in contact resistance is also observed after annealing. The laser annealing is expected to modify the metal/semiconductor interface, including interface state densities. Also, increased roughness at the contact-nanowire interface after annealing is expected to improve the contact-channel interface, reducing the contact resistance and modifying the Schottky barrier height in the nearby semiconductor region.The low frequency (1/f) noise in single In_2O_3 nanowire transistors was also measured before and after contact laser annealing. The amplitude of the current noise spectrum (S_I) is found to be proportional to I_d^2 in the transistor operating regime. According to the gate dependence of the noise amplitude, the extracted Hooge's constants are ~ 1.11×10^{-2} for as-fabricated devices and ~ 6.47×10^{-3} for laser annealed devices. The reduction of Hooge's constant after laser annealing implies a modification of the interface states and trap centers located in the space charge region. This study provides insights into the contact-dominated transistor properties and reports that laser annealing is a promising optimization technology for the realization of low power transparent/flexible display circuits, in terms of the effects on output conductance and threshold voltage.

3:10 PM Break

3:30 PM Student

W6, Vertical InSb Nanowire Arrays Electrodeposited into Porous Anodic Alumina Templates on Silicon Substrates: *Suprem Das*[1]; Asaduzzaman Mohammad[1]; Yong Chen[1]; Timothy Sands[1]; David Janes[1]; [1]Purdue University

InSb is a III-V direct bandgap semiconductor having zincblende crystal structure, a small bandgap (Eg = 0.17 eV) and the highest carrier mobility (μ_e = 78,000 $cm^2 V^{-1} s^{-1}$) among all bulk semiconductors at room temperature. InSb nanowires have potential applications ranging from high speed, low power logic applications, thermoelectric power generators, Peltier coolers and infrared detectors. Although the Vapor-Liquid-Solid mechanism is often used to grow the nanowires using CVD or MBE methods, these methods are usually expensive and often associated with a wetting issue of the nanowire sidewalls by gold coming from the gold catalyst droplets. In contrast, solution-grown methods of fabricating the nanowires can be effective and also can be exploited for non-lithographic fabrication of nano-devices. In this work, we have synthesized InSb nanowires within porous anodic alumina (PAA) templates having pores of ~ 20 nm diameter. The PAA template utilizes an evaporated film on a silicon wafer (Si/Ti (100nm)/Al (1.5µm)), with a two-step anodization process using 0.3M H_2SO_4 at a voltage of 20V and a temperature of 40C. Prior to nanowire deposition, the alumina barrier layers were removed from the pore bottoms using a reverse anodization process. A direct current electrodeposition method was used to grow the InSb nanowires into the nanopores at various deposition potentials (reduction potentials of -1.0V to -1.5V). The nanowires were characterized using Field Emission Scanning Electron Microscopy (both cross sectional view and planar view), Transmission Electron Microscopy and Raman

Spectroscopy. The FESEM images show that the nanowires have diameters = 20nm and grow along the pores starting from the pore bottom. The TEM image shows the crystalline quality of the InSb nanowires. The room temperature Raman spectra of the nanowires were taken at different laser powers using λ = 532nm excitation source in a backscattered geometry. We observe both the TO and LO phonon modes of InSb zincblende structure along with second order phonon processes involving 2TA and TO-TA phonon modes. The TO and LO modes were observed at $\upsilon \sim 178\ cm^{-1}$ and $194\ cm^{-1}$ respectively and the 2TA and TO-TA modes were observed at $\upsilon \sim 105\ cm^{-1}$ and $140\ cm^{-1}$ respectively. Both the Raman Spectroscopy intensities and Raman shifts can be explained on the basis of size effects and carrier confinement in the semiconductor nanowires.

4:10 PM

W8, Formation of Periodic Nanostructures through Kirkendall Constitutional Interdiffusion in Epitaxial Heterostructures: *Patrick Taylor*[1]; Wendy Sarney[1]; Venkataraman Swaminathan[2]; [1]US Army Research Laboratory; [2]US Army ARDEC

IV-VI materials are of interest for high-performance infrared detectors because they possess extremely large infrared absorption coefficients. However, these technologies are limited by the lack of suitable epitaxial substrate that is matched in both lattice and thermal expansion coefficients. Those mismatches can have effects that reduce photo-carrier diffusion and degrade infrared detection. ZnTe is an interesting new substrate candidate for this system because it has a very close match in lattice constant (misfit ~ 0.33%), and a reasonable match in thermal expansion. (ZnTe: 8.2 X 10-6/K and PbSe: 19.4 X 10-6/K). Using this approach, PbSe infrared active layers having unusually low dislocation density and high crystallinity have been demonstrated. One interesting phenomenon associated with this approach is the spontaneous formation of regularly spaced hollow nanostructures that are formed at the heteroepitaxial interface. We will present evidence showing that these nanostructures are formed by a Kirkendall diffusion mechanism at the interface between PbSe and ZnTe epitaxial layers. SIMS measurements are consistent with a chemical exchange reaction driven by the relatively more rapid diffusion of zinc into the PbSe layer leaving a semi-regular array of hollow nanostructures at the interface. For PbSe epitaxy onto ZnTe, the center-to-center spacing of misfit dislocations would be 96 nm. Using HRTEM, the nanostructures appear to be hollow nanotubes that have a distributed spacing centered between 100-150 nm, which is consistent with the linear equilibrium spacing of misfit dislocations. This consistency suggests that the nanostructures nucleate at the highly strained locations of the interfacial misfit dislocations. HRTEM measurements also show that the formation of the nanostructures is accompanied by the preferential formation of ZnSe and related PbZnSe solid-solution alloys.

4:30 PM Student

W9, Thermal Conductivity of Aluminum Nanowires near Room Temperature: Direct Measurements and Theory: *Nenad Stojanovic*[1]; Sanjeeva Maithripala[1]; Jordan Berg[1]; Mark Holtz[1]; [1]Texas Tech University

Electrical and thermal conductivity are important fundamental material quantities to establish for understanding and predicting device properties when nanoscale dimensions are involved. Obtaining direct results for electrical resistivity is readily achieved. However, direct measurements of thermal conductivity is extremely difficult due to fabrication and parasitic heat transport issues. Direct measurements are reported of thermal conductivity for aluminum nanowires. A nanofabricated electrothermal test structure is described for studying the nanowires near room temperature. Nanowires studied are 100 nm thick with 75, 100, and 150 nm widths. The thermal conductivity is found to be substantially lower than for bulk Al, and to decrease as nanowire width is reduced. Measurements of the electrical resistivity show it to increase with reduced nanowire width. These combined measurements allow examination of the Wiedemann-Franz law and to investigate the importance of phonon heat propagation in metals at room temperature.To aide in the interpretation of the results, we develop an approach for calculating the electron and phonon thermal conductivities, as well as the electrical conductivity. Effects such as surface and grain boundary scattering, which are negligible for larger structures, significantly influence electrical and thermal properties of nanoscale objects. The conventional wisdom for metals holds that thermal transport is predominantly by electrons, and that contribution due to lattice vibrations—that is, thermal transport by phonons—is negligible. Furthermore, it is usually assumed that transport by electrons is identical for describing current and heat. These assumptions are often used to justify the use of the Wiedemann-Franz law to infer thermal conductivity based on measurements of electrical resistivity. Our experiments suggest a breakdown of the Wiedemann-Franz law at the nanoscale. Solution of the Boltzmann transport equation for both electrons and phonons in nanowires will be used to examine the applicability of Wiedemann-Franz law at the nanoscale. It is found that Wiedemann-Franz law can be used to obtain the electronic component of thermal conductivity to good approximation, but that the phonon term must be considered in order to properly estimate total thermal conductivity of metallic nanowires. The calculations are extended to theoretically treat several other metals at room temperature.

4:50 PM

W10, Simulation of the Influence of Grain Boundaries on Resistivity via the Wigner-Fokker-Planck Equation: *Richard Sharp*[1]; Katayun Barmak[1]; [1]Carnegie Mellon University

The resistivity of polycrystalline conductors such as copper increases sharply as the size of a conducting sample approaches the mean free path of the electrons. Models for this phenomenon have been based on surface scattering of electrons (Fuchs and Sondheimer) and on grain boundary scattering (Mayadas and Shatzkes). Recent experimental results from Barmak and collaborators attribute the majority of the effect to grain boundary scattering. Here, we employ a temperature dependent open quantum kinetic model, the Wigner-Fokker-Planck (WFP) equation, to examine the resistivity size effect at the grain boundary level. Temperature dependence and the full quantum nature of the model, allowing nearby grain boundaries to interact in a nonlinear manner, yield a more detailed model than those above or subsequent refinements such as that of Warkusz.The WFP equation models the time evolution of the Wigner function, which is the Wigner transform of the quantum density operator into the phase space of the system. In the model, electrons interact with an electric potential and phonons. The electron-phonon scattering is applied by using a quantum Fokker-Planck operator, effectively a heat bath of harmonic oscillators, adding lattice temperature to the model. The WFP equation is related to Schroedinger's equation, indeed the two are equivalent when electron-phonon scattering is neglected in the WFP equation, and less directly to the Boltzmann equation through its mathematical form and phase space representation of the solution. Our initial simulations consider a one-dimensional model of a copper wire inspired by the situation considered by Mayadas and Shatzkes: a wire in which all grain boundaries are perpendicular to the axis parallel to the current and uniform in this cross section. The grain boundary is introduced as a square potential barrier and added to a linear potential resulting from a constant electric field. A single temperature dependent model parameter, the coupling strength between the system and heat bath, is determined by calibrating the free system (a wire with no grain boundaries) so that it yields the bulk resistivity of copper. The steady state solution of the WFP equation is computed using the discontinuous Galerkin method (as implemented by Gamba, Gualdani, and Sharp), open-system boundary conditions such as those discussed by Frensley, and an applied linear potential to drive a current past the grain boundary. The current density and thus resistivity of the wire are recovered from the steady state Wigner function. The approach, which has been established for the basic situation described here, will allow detailed examination of the grain boundary effect on resistivity.

Session X: Narrow Bandgap Semiconductors: Infared Detectors and Lasers

Thursday PM
June 24, 2010

Room: 131
Location: University of Notre Dame

Session Chairs: L. Ralph Dawson, University of New Mexico; Mark Wistey, University of Notre Dame

1:30 PM

X1, Minority Carrier Lifetime in LWIR Type II Superlattice Detector Structures Using Time-Resolved Photoluminescence: *Blair Connelly*[1]; Grace Metcalfe[1]; Paul Shen[1]; Kevin Clark[2]; Paul Pinsukanjana[2]; Michael Wraback[1]; [1]U.S. Army Research Laboratory; [2]Intelligent Epitaxy Technology, Inc.

Type II InAs/GaSb superlattice (T2-SL) long wavelength infrared (LWIR) detectors for the 8-12 μm wavelength range are expected to have lower dark current noise than HgCdTe photodetectors due to the suppressed Auger recombination rate that comes from the ability to engineer the band gap. One of the primary limiting factors in the performance of these devices is the minority carrier lifetime, which is directly related to the dark current noise and quantum efficiency. Previous studies have determined the recombination lifetime in LWIR T2-SLs by analyzing the dark current versus voltage and quantum efficiency. These studies rely on modeling, while optical measurements can provide a more direct measurement. However, there has been no reported optical measurement of the minority carrier lifetime in these devices. We present a direct optical measurement of the minority carrier lifetime. These optical measurements help determine the mechanisms that limit the performance of LWIR detectors and guide growth techniques to improve device performance. Time-resolved photoluminescence (PL) measurements are used to determine the rise time and decay rate of the PL intensity. Carriers are excited using an ultrafast laser pulse (~100 fs) at 4.5 μm, at a repetition rate of 250 kHz. PL from the sample is collected using reflective optics, and detected with a fast HgCdTe detector (3 ns temporal resolution). The PL signal is isolated from laser scattering using a longpass filter at 7.2 μm and recorded using a PCI card. Measurements made on a p-on-n homojunction LWIR detector structure based on an InAs/GaSb T2-SL on a GaSb substrate will be presented. The epi wafer was grown with a multi-wafer production molecular beam epitaxy reactor. Data are taken at 11 K and at 77 K, the anticipated operating temperature of the device. Peak PL intensity and PL lifetime are observed to increase with a decrease in temperature. The temporal evolution of PL at a carrier density of ~10^{16} cm^{-3} can be fit with a single exponential decay characterized by a time constant of 33 ns or 78 ns for 77 K or 11 K, respectively. This behavior suggests that nonradiative recombination dominates the recombination process, since the nonradiative lifetime increases with decreasing temperature while the radiative lifetime decreases with decreasing temperature. Under low injection conditions, the PL signal is proportional to the density of excess minority carriers. The measured PL lifetime increases with decreasing pump power, indicating that the injection density is higher than the background doping density. Therefore, the measured lifetime represents the lower bound for a LWIR detector under normal operating conditions. Preliminary measurements using lower pump powers indicate a PL lifetime greater than 60 ns at 77 K and 100 ns at 11 K.

1:50 PM Student

X2, MOCVD Growth of InAs/GaSb Type-II Superlattice Structures and Photodiodes for Mid-Infrared Detection: *Yong Huang*[1]; Jae-Hyun Ryou[1]; Russell Dupuis[1]; Adam Petschke[2]; Martin Mandl[2]; Shun-Lien Chuang[2]; [1]Georgia Institute of Technology; [2]University of Illinois at Urbana-Champaign

InAs/GaSb-based type-II superlattice (T2SL) structures have been exploited as photodetectors and light emitters operating in a wide wavelength range (from 3 μm to 32 μm) of the infrared (IR) spectral region. However, operating detectors based on this particular material system have been exclusively grown by molecular beam epitaxy (MBE). In this paper, we report on the metalorganic chemical vapor deposition (MOCVD) growth of InAs/GaSb type-II superlattices and demonstrate the first MOCVD-grown InAs/GaSb T2SL photodiode. During the growth of the InAs/GaSb SL structures by MOCVD, gas switching and interfacial (IF) layer control are of critical importance. It was found that there exists an additional tensile strain in the InAs/GaSb SLs without any intentional interfacial layer (IF), presumably attributed to the formation of GaAs IF layer. InAsSb and InGaSb IF layers were thus introduced at the superlattice interfaces to compensate the tensile strain and hence to improve the overall material quality of the superlattice structures. The optimal morphology and low strain was achieved via a combined interfacial layer scheme with 1 monolayer (ML) InAsSb + 1 ML InGaSb layers. In this case the gas switching in one period is a smooth InAs -> InAsSb -> InGaSb -> GaSb -> InGaSb -> InAsSb -> InAs, and formation of any InSb- or GaAs-like interfaces is completely avoided. RMS roughness is only 0.172 nm for 20×20 μm^2 scan area and the separation between the SL 0th-order peak and the substrate is only ~448 arcsec, corresponding to an in-plane lattice mismatch of ~0.17%.Using this scheme, a p-i-n photodiode structure with a 360-period InAs/GaSb superlattice was grown on a GaSb substrate, which operates at 78 K with a cut-off wavelength of ~9 μm and a peak responsivity of 0.6 A/W at ~6 μm. The overall detectivity is 1.6×10^9 Jones which is more than two orders of magnitude lower than those in state of the art InAs/GaSb-based T2SL devices for this wavelength grown by MBE. The performance degradation is attributed to the surface defects such as hillocks and high background doping levels in the InAs/GaSb i-SL. Nevertheless, these data show the first successful demonstration and feasibility of MOCVD-grown InAs/GaSb T2SL photovoltaic detectors. There is much room for improvement in the device performance through optimization of the material quality and MOCVD-oriented design of the device structure. Further work is currently being carried out on dry etching and surface passivation of the materials to enhance the sensitivity of the detectors.

2:10 PM Student

X3, Investigation of Passivation Techniques on InAs/GaSb Strained Layer Superlattice Long Wave Infrared Detectors: *Maya Narayanan Kutty*[1]; Elena Plis[1]; Stephen Myers[1]; Ha Sul Kim[1]; Nutan Gautam[1]; Ralph Dawson[1]; Sanjay Krishna[1]; [1]University of New Mexico

Considerable interest has been garnered by infrared (IR) detectors operating in the long wave IR (LWIR) spectral region (8–14μm) due to their wide ranging applications in the fields of medical diagnostics, meteorology, astronomy, search and rescue, missile detection, and satellite based surveillance. The available technologies in the current market at this wavelength range are Mercury-Cadmium-Telluride (MCT) and quantum-well-infrared (QWIP) detectors. MCT detectors face problems in the epitaxial growth of mercury-based compounds limiting manufacturing yield and QWIPs exhibit an inability to absorb normal incident light. The crucial advantage of InAs/(In,Ga)Sb strained layer superlattices technology is that its effective bandgap can be tuned within 3-32μm by modifying the individual material thicknesses. SLS technology also encompasses benefits such as normal incidence absorption, low tunneling currents, enhanced carrier lifetimes due to suppressed Auger-7 recombination processes, compositional uniformity over a large area and commercial availability of low defect density substrates. The reason InAs/ (In,Ga)Sb SLS detectors are yet to be commercialized is due to the detrimental effect of surface leakage currents on device performance. These surface leakage currents are a large component of the total dark current and they arise from abrupt termination of the crystal lattice at the surface leading to interfacial traps and dangling bonds and hence to the pinning of the Fermi level at the surface. Moreover, the native oxides formed due to the exposure to atmosphere are found to be conducting. These surface effects can be minimized by passivating the surface of the SLS devices and this presentation is a compilation of the results of passivating techniques we have undertaken on our LWIR SLS devices.The reported passivation study was performed on InAs/GaSb SLS LWIR detectors with p-i-n design grown by solid-source molecular-beam epitaxy (MBE) technique with the 100% cut-off wavelength ~ 11.7μm at 77K.The device structure was formed by 14ML InAs/7ML GaSb SLS non-intentionally doped (n.i.d) absorber grown on top of n-type contact layer (8ML InAs/8ML GaSb SLS with Te-doped InAs layers) and capped by GaSb p-type (Be) top-contact layer. Dark current measurements reveal the reduction of noise current by two orders of magnitude

after SU8 passivation (from 2.4A/cm2 for unpassivated device to 24mA/cm2 for passivated device, 30K, bias=-0.1V). At zero bias, R0A (SU-8 passivated)~ 13 x 10-2ohm-cm2 which is an order of magnitude larger when compared to R0A (unpassivated) ~ 22 x 10-3ohm-cm2. During the presentation the optical and electrical characteristics of SLS LWIR detectors (dark current density, resistance-area product at zero bias, responsivity and detectivity) studied for two different passivation treatments (SU-8 and SiNx) will be discussed in detail and compared with those reported in the literature for the p-i-n detectors operating in the same wavelength range.

2:30 PM Student

X4, Investigation of Antimonide Infrared Detectors Based on the nBn Design: *Stephen Myers*[1]; Arezou Khoshakhlagh[1]; Elena Plis[1]; Maya Kutty[1]; Ha Sul Kim[1]; Nutan Gautam[1]; Brianna Klein[1]; Ralph Dawson[1]; Sanjay Krishna[1]; [1]University of New Mexico

Infrared detectors are important tools with many wide ranging applications including defense, security, astronomy and medical diagnostics. The applications of infrared detectors are however limited by expensive and bulky cooling systems which are required for them to operate properly. The development of heterostructure designs capable of increasing operating temperature and reducing dark current density has thus become very important. Recently unipolar designs utilizing barrier regions have gained much interest for achieving these characteristics. The nBn structure as developed by Maimon and Wicks utilizes an n-type contact region "n", a barrier region "B" with a large conduction band offset but no offset in the valence band, and a n-type absorber region. The large conduction band offset blocks electrons while allowing minority carriers to flow unimpeded. This design reduces dark current associated with generation-recombination (G-R) by alleviating the presence of a depletion region, as in the case of a p-i-n photodiode, making the detector diffusion limited at all temperatures. Another advantage that can be utilized with the nBn design is the suppression of surface leakage current which is a significant challenge of state of the art p-i-n designs, by utilization of shallow etching. In a typical p-i-n device, one pixel is distinguished from neighboring pixels by mesa isolation etching, however, with nBn shallow etching a pixel is distinguished from neighboring pixels by the minority carrier diffusion length. In order to fully capitalize on this design the different regions need to be optimized in terms of composition and doping level. The doping level is important because it dictates the offset of the bandstructure between the different regions. Previously, a study was conducted that investigated different doping levels of the absorber region of an InAs/GaSb superlattice nBn detector which revealed that careful tuning of the absorber doping level can improve device characteristics in terms of dark current density and detectivity. The barrier is a key component of the nBn design since it controls the flow of majority and minority carriers. It must be thick enough to prevent tunneling of majority carriers (electrons) and high enough to avoid thermal excitation in the conduction band. The doping level in the barrier region affects the valence band offset which impacts the behavior of the minority carriers (holes) consequently influencing the total dark and photo current of the detector. In this presentation a detailed study of the barrier region composition and doping level will be analyzed along with their impact on the device performance.

2:50 PM

X4, Late News

3:10 PM Break

3:30 PM Student

X6, Quinternary GaInAsSbP on GaAs Substrates Grown by Metal Organic Vapor Phase Epitaxy (MOVPE): *Toby Garrod*[1]; Peter Dudley[1]; Jeremy Kirch[1]; Sangho Kim[1]; Luke Mawst[1]; Thomas Kuech[1]; [1]University of Wisconsin-Madison

The capability to grow bulk lattice matched material, with band gap energies less than that of GaAs, is of interest for applications in concentrated photovoltaic devices. Material development is this area has focused on the incorporation of dilute amounts of nitrogen into conventional III/V crystals, although short minority carrier diffusion lengths, narrow depletion widths, deep level defects and high carbon incorporation have limited the performance in MOVPE grown devices. The ability to grow narrow band gap material free of nitrogen would be advantageous for the electronic properties of these devices. Quinternary materials, although complex, offer a higher degree of freedom for materials development with knowledge of the incorporation properties of constituent elements. Recent reports of this material system were in the growth of mid-infrared light emitting diodes on GaSb substrates by liquid phase epitaxy (LPE) [1,2]. To our knowledge, there have been no reports of this material grown lattice matched GaAs by MOVPE. Growth studies have been performed on GaInAsSbP thin film alloys, grown on (100) GaAs substrates by MOVPE utilizing liquid group III and group V metal organic precursors. Room temperature photoluminescence studies of nominally lattice matched material to (100) GaAs substrates exhibits a band gap energy of 1.37 eV($Ga_{(0.76)}In_{(0.24)}As_{(0.25)}Sb_{(0.025)}P_{(0.725)}$, $\Delta a/a=8.4\times10^{-4}$, V/III=67). High resolution x-ray diffraction (HRXRD), ω-2θ rocking curves around the (004) reflection for GaAs, were used to determine the lattice mismatch of the out-of-plane lattice parameter of the GaInAsSbP films. Due to the complex nature of the GaInAsSbP alloy, it is difficult to determine the composition by conventional measurements and assuming Vegard's Law. Therefore, calibrated secondary ion mass spectroscopy (SIMS) was used on selected samples to determine the actual solid phase compositions of the GaInAsSbP material. Future work with this material system will be to determine the lowest possible band gap energy for lattice matched material and to evaluate the effects of dilute amounts (<1%) of nitrogen into the GaInAsSbP material. This work is funded by Army Research Lab (ARL), contract number W911NF-09-2-0008. 1. A. Krier, V. M. Smirnov, P. J. Batty, M. Yin, K. T. Lai, S. Rybchenko, S. K. Haywood, V. I. Vasil'ev, G. S. Gagis and V. I. Kuchinskii, Appl. Phys. Lett. 91, 082102 (2007). 2. A. Krier, V. M. Smirnov, P. J. Batty, V. I. Vasil'ev, G. S. Gagis and V. I. Kuchinskii, Appl. Phys. Lett 90, 211115 (2007).

3:50 PM Student

X7, Growth of $GaAs_{1-x}Bi_x/Al_yGa_{1-y}As$ Multi-Quantum Well Structures on GaAs: *Takuma Fuyuki*[1]; Yoriko Tominaga[1]; Kazuya Yamada[1]; Kunishige Oe[1]; Masahiro Yoshimoto[1]; [1]Kyoto Institute of Technology

$GaAs_{1-x}Bi_x/Al_yGa_{1-y}As$ multi-quantum wells (MQWs) have been successfully grown by molecular beam epitaxy (MBE). Intensity oscillation and streaky patterns of *in situ* reflection high-energy electron diffraction (RHEED) suggested the layer-by-layer growth of $GaAs_{1-x}Bi_x/Al_yGa_{1-y}As$ MQWs. Clear satellite peaks attributed to periodical structures were observed in X-ray diffraction (XRD) measurements. Depth profile of secondary ion mass spectrometry (SIMS) confirmed periodical incorporation of Al and Bi. The cross-sectional transmission microscopy (TEM) images showed that $GaAs_{1-x}Bi_x/Al_yGa_{1-y}As$ MQWs with a smooth interface can be fabricated without distinct segregation. III-V semiconductor alloys including semimetallic components, such as $GaAs_{1-x}Bi_x$ with semimetallic GaBi, have been proposed as materials having temperature-insensitive bandgaps. The material with a temperature-insensitive bandgap is expected to be applicable to a laser diode (LD) of which the wavelength is kept constant against ambient temperature variation. The MQW is a key structure for fabrication of LDs. As Bi was utilized as a surfactant in the growth of III-V semiconductors, it was segregated easily during the growth. We demonstrated that low-temperature growth (<400°C) efficiently suppressed segregation of Bi atoms, and $GaAs_{1-x}Bi_x$/GaAs MQWs were successfully realized without distinct segregation in previous study. It is notable that $GaAs_{1-x}Bi_x$ showed brightly luminescent nature in spite of the low-temperature growth. This implies that Bi atoms play some role in improving crystalline quality during the growth. In this study, we have extended the growth technique to $GaAs_{1-x}Bi_x/Al_yGa_{1-y}As$ MQWs toward efficient carrier confinement. $GaAs_{1-x}Bi_x/Al_yGa_{1-y}As$ MQWs ($0.03< x <0.05$, $0< y <0.3$) were grown on GaAs(001) substrates by MBE at a substrate temperature of 350°C. The thicknesses of $Al_yGa_{1-y}As$ and $GaAs_{1-x}Bi_x$ layers were designed to be 14 and 7 nm, respectively, with a periodical number of 10. In RHEED observation, a (2x1) superstructure was observed during the growth of $GaAs_{1-x}Bi_x$ layers in contrast with a (1x1) patterns during growth of $Al_yGa_{1-y}As$ layers. Persistent RHEED intensity oscillation was observed as well as the streaky RHEED patterns during both layers, suggesting layer-by-layer growth of $GaAs_{1-x}Bi_x/Al_yGa_{1-y}As$ MQWs. Clear satellite peaks attributed to

periodical structures were observed in XRD measurements. Thickness of each period derived from the position of satellite peaks agreed with designed values for all MQWs. This indicates that fabrication of $GaAs_{1-x}Bi_x/Al_yGa_{1-y}As$ MQW structures can be controlled precisely without a distinct diffusion of Bi atoms. Depth profile of SIMS confirmed periodical incorporation of Al and Bi. TEM images with low magnification demonstrated fabrication of the quantum-well structure with a smooth interface. Clear lattice images are observed for both the $Al_yGa_{1-y}As$ and $GaAs_{1-x}Bi_x$ layers in the high-magnification TEM images. It is concluded that the $GaAs_{1-x}Bi_x/Al_yGa_{1-y}As$ MQWs with a smooth interface can be fabricated without distinct segregation.

4:10 PM Student

X8, Perforated (In)GaSb Quantum Wells on GaSb Substrates through the Use of As_2 Based In-Situ Etches: *P. Ahirwar*[1]; T. J. Rotter[1]; S. Clark[1]; C. P. Hains[1]; A. R. Albrecht[1]; L.R. Dawson[1]; G. Balakrishnan[1]; [1]Center for High Technology Materials, University of New Mexico

The InGaSb quantum wells (QW) represent a very promising technology for room-temperature mid-Infrared semiconductor lasers. These wells are grown under very high strain conditions and their emission can reach very long wavelengths if the strain in the wells is managed. The high strain has the added advantage of suppressing Auger non-radiative recombination in the wells. Traditional approaches for growing highly strained active regions include strain compensation and low-temperature growth. However, even these techniques can only accommodate a slightly elevated level of strain. Another option for the growth of highly strained active regions is the use of the Stranski-Krastanov (SK) growth mode to produce quantum dots. However, the SK growth mode is not viable in the III-Sb material system since highly strained (>5% mismatch) antimonide layers tend to form completely relaxed islands through interfacial misfit dislocation arrays. In this paper we present the growth of perforated InGaSb QW on a GaSb substrate. The growth of the material is done in a VG V80 molecular beam epitaxy (MBE) reactor. The InGaSb quantum wells are grown with a variety of thicknesses and are subsequently etched by an As_2 flux. The As_2 etches into the antimonide material resulting in nano-scale holes in a random pattern. The presence of these holes permits the InGaSb layer to relax in the in-plane direction thus relieving a significant amount of the strain. The study includes the growth of single InGaSb QWs with the In percentage varying from 0 to 60%. The samples are exposed to a variety of As_2 fluxes at different growth temperatures to study etch rate and etch profile. The samples are analyzed using atomic force microscopy, scanning electron microscopy, transmission electron microscopy and high-resolution x-ray diffraction. Samples with intact wells and with etched wells are compared and the difference in strain is measured. The effect of the etching process on the quantum wells is investigated using photoluminescence. In order to ensure, that the etch does not progress beyond the quantum well, etch stop layers are investigated. We have identified thin layers of InAs as a potential etch stop layer. Most of the present results are based on low-Indium percentage QWs and we will study how the etch process will change in the presence of high-Indium percentage QWs. The capping process of a perforated well is non-trivial. Currently the cap layers are grown such that they coalesce over the voids. Alternately the growth can also be performed such that the voids are completely filled. We shall also investigate the presence of threading dislocation in the growth due to the capping process. Finally, we shall study how the excess arsenic (etchant) incorporates into the matrix.

4:30 PM Student

X9, Antimonide VECSELs on AlGaAs DBRs: P. Ahirwar[1]; *T. J. Rotter*[1]; A. R. Albrecht[1]; S. Clark[1]; C.P. Hains[1]; L. R. Dawson[1]; G. Balakrishnan[1]; J. V. Moloney[2]; [1]Center for High Technology Materials (CHTM), University of New Mexico, Albuquerque, NM 87106; [2]College of Optical Sciences, University of Arizona, Tucson, AZ 85721

We present an optically pumped vertical-external-cavity surface-emitting laser (VECSEL) with high output power at 2 µm achieved through the integration of III-Sb active regions with AlGaAs Distributed Bragg Reflectors (DBRs)[1]. The laser's active region includes GaInSb/AlGaSb type I quantum wells. The optical cavity is provided by a high reflectivity AlGaAs/GaAs DBR and an external mirror which also serves as the output coupler. The novelty in this approach is the combination of a GaSb based active region with a GaAs based DBR, both of which are monolithically grown on a GaAs substrate[2]. The strain due to the lattice mismatch between the GaSb-based active region (lattice constant close to 6.1 Å) and the GaAs-based DBR (lattice constant close to 5.65 Å) is relieved by the formation of an interfacial misfit (IMF) array at the GaSb/GaAs interface[3,4]. GaSb based VECSELs were previously grown on GaSb based DBRs. While high power devices have been achieved with this technology, the device performance is limited by a smaller index contrast of GaSb based DBRs compared to GaAs based DBRs and higher absorption of the laser's emission in GaSb compared to GaAs. The work described in this talk is based on crystal growth by molecular beam epitaxy (MBE), along with the basic crystal characterization techniques such as X-ray diffraction (XRD), photoluminescence (PL), surface nomarski microscopy and atomic force microscopy (AFM). We shall also provide detailed lasing data for lasers at 2 µm both pulsed and CW. We shall discuss the technical challenges related to the MBE growth of such structures, which are numerous. First, the IMF based growth of III-Sb on GaAs leads to differences in strain and relaxation of the epilayer as compared to growth on GaSb substrates. This influences the optical emission from the III-Sb active region, since it depends on the compressive strain in the quantum wells. It requires an independent development of the active region, grown on GaAs. Second, the transfer of the IMF growth technology from growth on GaAs substrates to growth on the MOCVD grown AlGaAs/GaAs DBR is nontrivial. The challenges include the IMF formation on the DBR surface, which is slightly rougher than a GaAs substrate's surface, and the growth temperature control, since the DBR's heat conductivity differs from that of a GaAs substrate. We shall also discuss the development of longer wavelength VECSELs in the MWIR (2.5 to 3.5 µm). This discussion will include active region development and DBR performance at these wavelengths.

4:50 PM Student

X10, Effect of Aluminum Composition on Current-Voltage Characteristics of AlGaSb/InAs Tunnel Junction: *Yeqing Lu*[1]; Alan Seabaugh[1]; Huili Xing[1]; Tom Kosel[1]; Siyuranga Koswatta[2]; Hanjun Zhu[3]; Kevin Clark[3]; Jenn-Ming Kuo[3]; Pinsukanjana Paul[3]; Patrick Fay[1]; [1]University of Notre Dame; [2]IBM T. J. Watson; [3]IntelliEPI

Tunneling field effect transistors (TFETs) with staggered band alignment have recently attracted considerable interest because of their potential use in low power, high performance logic applications. The low tunneling barrier height and small effective mass in AlGaSb/InAs heterostructures may enable high tunneling current density, and the large band gap of AlGaSb suppresses off-state current. However, little experimental study has been done of the band alignment in this material system as a function of ternary composition. In this work, a set of $Al_xGa_{1-x}Sb$/InAs samples was grown by molecular beam epitaxy (MBE), and heterostructure tunnel diodes were fabricated. Secondary ion mass spectroscopy (SIMS) was used to measure the dopant and aluminum profiles, and current-voltage (I-V) and low temperature I-V were measured to characterize the tunneling junction. The MBE growth used Be and Si as the dopant species for p-AlGaSb and n-InAs respectively. At the interface between AlGaSb and InAs, the dopant flux was turned off, resulting in a 2 nm thick unintentionally-doped AlGaSb layer at the P+/N+ junction. The samples were capped with highly doped GaSb to facilitate ohmic contact. A Be dopant slope of 23 nm/decade at the tunnel junction was observed in the SIMS profile. Devices were fabricated using a self-aligned process to minimize access resistance. A Ti/Au/Ti emitter was first formed by lift-off on the P+ GaSb layer, followed by selective wet etching of the AlGaSb in 1:5 $NH_4OH:H_2O$ and the InAs in 1:2 citric acid:H_2O_2 to form the mesa. This metallization has been previously found to minimize mesa etch undercut [1]. The self-aligned bottom contact is then formed by electron beam evaporation of a Ti/Au contact. Current-voltage characteristics for diodes fabricated with different Al mole fractions (x=0, 0.12, 0.2, and 0.27 as determined by SIMS) were compared. The corresponding peak current densities were measured (0.048, 0.13, 0.22, 0.5 mA/µm^2) and found to decrease as expected with increasing Al content. From [2], the band alignment is expected to transition from broken to staggered at x=0.4. However, due to lower-than-expected Al incorporation, the highest Al composition achieved experimentally was 0.28, and this diode clearly demonstrates negative differential resistance

(NDR) indicating that the bands have not yet crossed. In addition, due to the low effective mass and the relatively high doping concentration, significant degeneracy in the InAs may also be contributing. From temperature dependent measurement, peak current almost does not change with temperature, but valley current shows a thermionic character as expected. This work is supported by the Nanoelectronics Research Initiative (NRI) through the Midwest Institute for Nanoelectronics Discovery (MIND).

Session Y: III-N Nanostructures

Thursday PM
June 24, 2010

Room: 138
Location: University of Notre Dame

Session Chairs: Andrew Armstrong, Sandia National Laboratories; Alec Talin, NIST

1:30 PM Student
Y1, Dislocation Filtering in GaN Nanorods: *Robert Colby*[1]; Zhiwen Liang[1]; Isaac Wildeson[2]; Timothy Sands[3]; R. Garcia[1]; Eric Stach[1]; [1]Purdue University, School of Materials Engineering; [2]Purdue University, School of Electrical and Computer Engineering; [3]Birck Nanotechnology Center

Dislocation filtering in GaN by selective area growth through a nanoporous template is examined both by transmission electron microscopy and numerical modeling. These nanorods grow epitaxially from the (0001)-oriented GaN underlayer through the ~100 nm thick template and naturally terminate with hexagonal pyramid-shaped caps. It is demonstrated that, for a certain window of geometric parameters, a threading dislocation growing within a GaN nanorod is likely to be excluded by the strong image forces of the nearby free surfaces. Approximately 3000 nanorods were examined in cross-section, including growth through 50 nm and 80 nm diameter pores. The very few threading dislocations not filtered by the template turn towards a free surface within the nanorod, exiting less than 50 nm past the base of the template. The potential active region for light emitting diode devices based on these nanorods would have been entirely free of threading dislocations for all samples examined. A greater than two orders of magnitude reduction in threading dislocation density can be surmised from a data set of this size. A finite element-based implementation of the eigenstrain model was employed to corroborate the experimentally observed data and examine a larger range of potential nanorod geometries, providing a simple map of the different regimes of dislocation filtering for this class of GaN nanorods. These results indicate that nanostructured semiconductor materials are effective at eliminating deleterious extended defects, as necessary to enhance the optoelectronic performance and device lifetimes compared to conventional planar heterostructures.

1:50 PM Student
Y2, Threading Defect Elimination in GaN Nanostructures: *Ashwin Rishinaramangalam*[1]; Stephen Hersee[1]; Michael Fairchild[1]; Lei Zhang[2]; Petros Varangis[2]; [1]The Center for High Technology Materials, The University of New Mexico; [2]Nanocrystal Corporation

This paper describes the elimination of threading dislocations (TDs) in GaN nanowire and nanowall structures grown by Metal Organic Chemical Vapor deposition (MOCVD). The templated nanostructure growth process uses high-purity metal organic and ammonia precursors as in regular MOCVD growth, and avoids the use of metal catalysts. The nanostructures were grown selectively onto underlying planar (0001) GaN films using nano-patterned templates. The threading defect density in the underlying planar GaN film was in the range 10^8 to 10^9 cm^{-2}. TDs were imaged using bright-field cross-sectional transmission electron microscopy (XTEM) analysis of thinned nanowire and nanowall samples. The density of threading defects in [0001] GaN nanowires approaches zero even though these nanostructures are epitaxially connected to an underlying planar GaN film that has a defect density in the range 10^8 to 10^9 cm^{-2}. XTEM reveals that the nominal [0001] line direction of a TD changes when that TD enters a GaN nanostructure. The line direction of the TDs bends towards the (0001) plane, and the dislocation rapidly terminates at a {1-100} sidewall facet of the nanostructure. We propose that the driving force for this elimination process is the reduction of the dislocation line energy. This line energy is reduced for a TD that bends and terminates at a sidewall compared to a TD that continues to propagate along the nanowire. A simple model is also proposed, where in the TDs are shown to bend and terminate at a sidewall simply by climb. A conversion to another defect-type does not appear to be required and furthermore, conversion to a different defect is expected to be energetically unfavorable. This TD elimination mechanism is expected to be active in any [0001] GaN nanostructure, where a surface is in close proximity to the threading defect. Nanostructures clearly offer a unique opportunity to fabricated defect-free GaN-based devices.Acknowledgment: This work was supported in part by the Engineering Research Centers Program of the National Science Foundation under NSF Cooperative Agreement No. EEC-0812056. Any Opinions, findings and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect those of the National Science Foundation.

2:10 PM Student
Y3, Yellow-Orange Luminescence from III-Nitride Nanopyramid Heterostructures: *Isaac Wildeson*[1]; David Ewoldt[1]; Robert Colby[1]; Zhiwen Liang[1]; Dmitri Zakharov[1]; R. Edwin Garcia[1]; Eric Stach[1]; Timothy Sands[1]; [1]Purdue University

One of the current major thrusts in the light emitting diode (LED) research community is developing a solution for the "green gap" – that is, the current lack of an efficient yellow-green LED technology. Of the available materials systems, the III-nitrides currently appear as the most promising for resolving the green gap and extending the range of efficient luminescence across the visible spectrum in a single materials system. The III-nitrides, however, possess numerous challenges including high threading dislocation densities, a large lattice mismatch and miscibility gap between InN and GaN, and strong polarization-induced electric fields within quantum wells. The focus of the current work is to utilize nanoheteroepitaxy for quantum well growth in an attempt to mitigate both the high threading dislocation density and the large lattice mismatch between GaN and InN. Theoretical investigations have illustrated that the effective critical thickness of a heterostructure can be significantly increased if growth is conducted on nanostructures that allow lateral strain relaxation [1]. Specifically, our work focuses on selective-area organometallic vapor phase epitaxy of III-nitride nanopyramid heterostructures through dielectric growth masks that accurately control the size and position of the nanopyramids, as well as serve as effective dislocation filters for threading dislocations within the underlying GaN films [2]. Furthermore, by varying the growth parameters, the geometry of the nanopyramids can be altered at specific stages of the heterostructure growth to produce active regions that are either predominantly quantum wells or predominantly quantum dots. We will discuss in detail the luminescent properties of nanopyramid heterostructures by analyzing both photoluminescence (PL) and electroluminescence (EL) results. Temperature-dependent PL measurements often used for estimations of internal quantum efficiency yield a ratio of the integrated PL intensity at 300K over the integrated PL intensity at 4K of 10.3%. PL also reveals a change in peak emission energy with temperature that follows a "double s-shape" (red-shift, blue-shift, red-shift, blue-shift), instead of the commonly observed single "s-shape" (red-shift, blue-shift, red-shift). The origin of the "double s-shaped" PL trend may result from two distinct groups of indium-rich clusters that produce band-tail states, or may result from contributions of yellow defect luminescence at high temperatures. EL reveals a 45 nm red-shift between nanopyramid LEDs and thin-film LEDs that were grown together, suggesting higher InN incorporation in the strain-relaxed nanopyamids during growth. This material is based in part on work supported by the Department of Energy under Award No. DE-FC26-06NT42862. [1]. E. Ertekin, et.el., J. Appl. Phys. 97, 114325 (2005). [2]. P. Deb, et.el., Nano Lett. 5, 1847 (2005).

2:30 PM Student

Y4, Molecular Beam Epitaxial Growth and Characterization of InGaN/GaN Dot-in-a-Wire Nanoscale Heterostructures on Si: *Jiale Wang*[1]; Yi-Lu Chang[1]; Feng Li[1]; Zetian Mi[1]; [1]McGill University

There has been an escalating interest in developing high efficiency green and red emitting InGaN/GaN LEDs for all LED and smart lighting applications. Such devices, however, generally exhibit very low internal quantum efficiencies, due to the presence of large defect densities and the strain induced polarization field. Greatly reduced defect densities and strain distribution, on the other hand, can be achieved in nanowire heterostructures, due to the effective lateral stress relaxation. Additionally, the use of quantum dots further provide 3-dimensional carrier confinement and drastically reduced nonradiative carrier recombination associated with the presence of surface states. In this context, we have studied the molecular beam epitaxial (MBE) growth and characterization of nearly defect-free InGaN/GaN dot-in-a-wire as well as dot-on-a-wire nanoscale heterostructures on Si(111) substrates, which exhibit strong emission in the green, yellow, and red wavelength range, with an internal quantum efficiency of ~ 45%. The nanowire heterostructures were grown on Si(111) substrates using a Veeco Gen II MBE system equipped with a radio frequency plasma source. The wires exhibit diameters of ~ 30 – 50 nm and are of a wurtzite structure and aligned along the c-axis. The high resolution TEM analysis confirms that the InGaN quantum dots and surrounding GaN barrier layers are nearly free of dislocations. It is also observed from the detailed TEM analysis that each InGaN dot is not compositionally uniform, with the presence of In-rich nanoclusters, due to phase segregation. However, such In-rich nanoclusters are not observed for InGaN quantum dots grown GaN nanowires without any capping layer. Optical properties of InGaN/GaN dot-in-a-wire nanoscale heterostructures were investigated using temperature-variable photoluminescence spectroscopy. By varying the In compositions in the dots, we have achieved strong green, yellow, and amber emission, which exhibit a relatively high room temperature internal quantum efficiency of ~ 45% of that measured at ~ 10 K. In addition, strong red emission (~ 0.66 μm) has been measured from InGaN/GaN dot-on-a-wire nanoscale heterostructures. The photoluminescence intensity of the red-emitting InGaN quantum dots is nearly a factor of 2 of that of GaN, in spite of the much thicker GaN segments, compared to the dots, which further confirms the excellent optical quality of InGaN quantum dots. Optical properties of single InGaN/GaN dot-in-a-wire nanoscale heterostructures, as well as the achievement of green and red-emitting InGaN/GaN dot-in-a-wire LEDs on Si are being investigated and will be presented.

2:50 PM Student

Y5, Electrochemical Etching of GaN and Its Applications: *Yu Zhang*[1]; Qian Sun[1]; Chris Yerino[1]; Benjamin Leung[1]; Qinghai Song[1]; Coung Dang[1]; Sang-wan Ryu[2]; Hui Cao[1]; Arto Nurmikko[3]; Jung Han[1]; [1]Yale University; [2]Chonnam National University; [3]Brown University

The importance of GaN devices in display, data storage, and lighting applications is clearly established by now. In a more forward-looking manner, one may rightly ask about new opportunities the wide bandgap III-nitride family could offer, and new dimensions one could introduce to the existing technologies. In this talk we describe an electrochemical procedure to selectively etch conducting n-type GaN layers. We also present a few proof-of-concept demonstrations of device structures facilitated by this simple method of etching. Wet etching of Ga-polar GaN at room temperature can only be done through photoelectrochemical (PEC) etching method where photoexcited holes as minority carriers mediate an oxidation-etching mechanism. This procedure has been incorporated into a selective etching technique with a combination of epitaxial heterostructures (InGaN/GaN) and bandgap selective photoexcitation. Recently, a few groups have pursued the wet-etching of "GaN-compatible" layers, layers that have sufficiently different chemical compositions and are more amenable to wet-etching. Two of such GaN-compatible layers are AlInN and CrN, and there have been already interesting demonstrations. Our work in based on a recent observation that a heavily doped (N_D>2x10^{18}cm^{-3}) GaN can be selectively etched in an oxalic-acid electrochemical etching. Distinct advantages of using n-GaN as the "sacrificial layer" for etching include (1) complete lattice matching to conventional GaN structures with negligible degradation in microstructure or morphology, (2) complete freedom in thickness design toward 1D, 2D, and 3D photonic-electronic-mechanical structures, and (3) the possibility of tuning the etching pathways at microscale through conductivity, bias, and solution, thus offering a new tool set to etch, to undercut, and to "texture" GaN. Figure 1(a) and (b) show GaN microdisk array and preliminary result of mode pattern of a microdisk (10 μm diameter) under optical pumping, Figure 1(c) shows the formation of GaN microdisk where the lower cladding is nanoporous GaN in stead of air, thus greatly improving the structural robustness. The effect of optical confinement can be seen from the contrast of annular rings under Nomarski (Figure 1(d)), figure 1(e) shows another example of lateral undercut etch in forming distributed Bragg reflector (DBR) structures. It is worth noting that under reduced bias or doping level, nanoporous GaN is produced as a new class of GaN material with tunable index of refraction for photonic structure. Figure 1(f) illustrates the use of nanoporous GaN for form a three-period DBR. Figure 2 show (a) a GaN cantilever prepared by the EC etching and (b) Spectral response of a GaN cantilever compared with a reference spectrum. The reference was obtained at un-etched wafer surface. Figure 3 shows the nanocrystal GaN obtained by sonicating nanoporous GaN in DI water.

3:10 PM Break

Session Z: Point and Extended Defects and Doping in Wide Bandgap Materials

Thursday PM
June 24, 2010

Room: 138
Location: University of Notre Dame

Session Chairs: Alec Talin, NIST; Andrew Armstrong, Sandia National Laboratories

3:30 PM

Z1, Luminescence Recombination Dynamics of Ytterbium Implanted GaN Epilayers: Wojciech Jadwsienczak[1]; *Jingzhou Wang*[1]; Andre Anders[2]; [1]Ohio University; [2]Lawrence Berkeley National Laboratory

In the past Yb-doped III-V semiconductors were extensively investigated due to the relative simplicity of the Yb^{3+} electronic structure ($4f^{13}$). Those studies proved to be useful in better understanding of other RE^{3+} ions doped III-V semiconductors. During the last few years rare earth (RE) ions doped III-nitride (III-N) semiconductors received significant interests because their unique luminescence and magnetic properties [1,2]. Among investigated RE-doped III-Ns ytterbium has been the least studied. Recent theoretical calculations predict that the Yb^{3+} ion can occupy different optically active centers in GaN and AlN hosts [3,4].In this project we investigated Yb^{3+} ions implanted to GaN grown by hydride vapor phase epitaxy (HVPE) on (0001) Sapphire and GaN grown by metal-organic chemical vapor deposition (MOCVD) on (0001) Sapphire, respectively. The photoluminescence and photoluminescence kinetics of these samples have been studied with continuous and pulse photo-excitations in 360 nm – 1100 nm spectra range at different temperatures. The characteristic Yb^{3+} ion emission spectra were observed between 970 nm -1050 nm. There are more emission lines than predicted by theory for Yb^{3+} ions occupying a C_{3v} symmetry site in the GaN host. The number of luminescence transition lines observed at low temperature between the spin-orbit levels $^2F_{5/2}$-$^2F_{7/2}$ indicates that Yb^{3+} ions are involved in different optically active centers. Luminescence kinetics results confirmed that Yb^{3+} ions occupy at least two major distinct lattice site locations. Based on obtained experimental data we will discus the excitation mechanism for Yb^{3+} ions in GaN which can be generalized for all RE^{3+} ions in III-Nitride semiconductors. Furthermore, better understanding of the structural and opto-electrical properties of Yb^{3+} ion in GaN may find useful in energy harvesting applications where Yb^{3+} ion works as sensitizer. [1] J. H. Park, and A. J. Steckl, J Appl. Phys., Vol. 98, 056108 (2005). [2] H. J. Lozykowski, and W. M. Jadwisienczak, phys. stat. sol (b), Vol.244, 2109 (2007). [3] M. Dammak, S. Kammoun, R. Maalej, T. Koubaa, and M. Kamoun, J. Alloys Compd.,, Vol.18, 432 (2007).[4] T. Koubaa, M. Dammak, M. Kammoun, W. M. Jadwisienczak, H. J. Lozykowski, and A. Anders, J. Appl. Phys. Vol.106, 013106 (2009).

3:50 PM

Z2, Energy Levels of Nd^{3+} Ions in *In Situ* Doped AlN: *Grace Metcalfe*[1]; Eric Readinger[1]; Ryan Enck[1]; Paul Shen[1]; Michael Wraback[1]; [1]US Army Research Laboratory

Rare-earth (RE) doped semiconductors have found many applications in solid-state lasers, light-emitting displays and devices, and optical fiber telecommunications. Wurtzite nitrides are particularly attractive host materials due to their strong ionic bonds that can enhance the intra-4fn transition probability in the RE^{3+} ion, and high thermal conductivity necessary for maximizing performance of high power/high temperature devices. In addition, it has been shown that thermal quenching decreases with increasing band gap, making the widest band gap nitride AlN an appealing host material. AlN doped with RE ions, particularly Er and Eu, has been extensively studied. However, little is known about AlN doped with Nd, which has found immense success as the dopant in solid state lasers (i.e. Nd:YAG and Nd:YVO_4). In this paper, we report on *in situ* doping with Nd of AlN grown by plasma-assisted molecular beam epitaxy (PA-MBE). The Stark energy levels of the Nd^{3+} ion in AlN are resolved by photoluminescence (PL) and photoluminescence excitation (PLE) spectroscopy. The AlN layer was grown on *c*-plane sapphire by PA-MBE and consists of an AlN buffer layer followed by a ~0.6 µm-thick Nd-doped AlN layer. The sample was cooled to ~ 13K and pumped with a continuous wave Ti: Sapphire laser tunable between 750 to 1000 nm and with an excitation power of ~350 mW. The resulting luminescence was collected into a spectrometer and onto a Ge detector. Strong emission is observed at low temperature in the PL spectrum due to transitions from the $^4F_{3/2}$ doublet to the $^4I_{9/2}$, $^4I_{11/2}$, and $^4I_{13/2}$ manifolds. Due to the crystal field experienced by substitutional Nd-ions at Al sites, there are a total of J+1/2 Stark sublevels in each manifold, where J is the total angular momentum. The PL peaks appear in pairs separated by 5.0 meV, indicating the splitting energy of the $^4F_{3/2}$ doublet. The most intense emission peaks are observed from transitions to the $^4I_{11/2}$ manifold, with the strongest emission line at 1.12 eV (1108 nm). The PLE spectrum detected at the strongest emission energy 1.12 eV (1108 nm) at low temperature shows transitions from the $^4I_{9/2}$ ground state to the upper states $^4F_{5/2}$, $^2H_{9/2}$, $^4F_{7/2}$, and $^4S_{3/2}$. The strongest emission occurs at an excitation energy of 1.48 eV (835 nm). The energy levels of Nd in AlN are slightly shifted with respect to those which we previously measured in PA-MBE grown GaN, as evidenced by the splitting energy of the $^4F_{3/2}$ doublet (4.2 meV in GaN versus 5.0 meV in AlN). The shifted energy levels are due to the changes in the environment experienced by the Nd ions in AlN as compared to GaN, most likely caused by differences in the crystal-field or strain with substitutional doping at the Ga or Al site.

4:10 PM

Z3, Correlation of InGaN Growth Parameters, Defects and MQW Radiative Efficiency for Blue to Green Emission: *Andrew Armstrong*[1]; Mary Crawford[1]; Daniel Koleske[1]; Stephen Lee[1]; [1]Sandia National Laboratories

Deep-green emitting light emitting diodes are necessary for multi-chip color mixing for higher efficiency solid-state lighting. However, the internal quantum efficiency (IQE) of $In_xGa_{1-x}N$/GaN multi-quantum wells (MQWs) decreases as x increases to extend the emission wavelength from blue to green. The cause for this "green gap" is not fully understood. The quantum-confined Stark effect (QCSE) decreases IQE of *c*-plane $In_xGa_{1-x}N$/GaN MQWs with increasing x. However, reduced efficiency at longer wavelengths is observed for non-polar $In_xGa_{1-x}N$/GaN LEDs, where the QCSE is not operative, suggesting that non-radiative recombination centers (NRCs) play an important role, too.[1] Increasing x enhances strain in the InGaN well and requires reduced InGaN growth temperature (T_g), which can increase defect populations. Hence, understanding the influence of InGaN-related defects and controlling their incorporation is important for optimizing InGaN/GaN MQWs for green emission. To quantitatively correlate InGaN growth conditions with defect incorporation and study the resultant impact on the IQE of $In_xGa_{1-x}N$/GaN MQWs, we combined deep level optical spectroscopy (DLOS) with lighted capacitance-voltage (LCV) and photoluminescence. The properties and densities of deep level defects in coherently-strained $In_xGa_{1-x}N$/GaN (x=0.17,0.21) epi-layers were compared to the change in MQW IQE at 450 nm (x=0.17) versus 540 nm (x=0.21). *c*-plane InGaN epi-layers used for DLOS and InGaN wells in the MQW samples were grown under nominally the same conditions. To asses the influence of InGaN T_g on defect incorporation and IQE independent of polarization or strain effects, $In_{0.17}Ga_{0.83}N$/GaN MQWs were grown with 690C<T_g<760°C while holding constant other MQW growth and structural parameters. A 3.6x decrease in IQE was observed with reduced T_g and attributed to excess defect incorporation, since the QCSE was constant in these samples. DLOS and LCV study of corresponding epi-layers grown at 690°C and 750°C confirmed an $In_{0.17}Ga_{0.83}N$ deep level 1.7 eV above the valence band, whose density increased 3x for reduced T_g. We hypothesized that the 1.7 eV deep level is a NRC degrading IQE. To study the potential role of the 1.7 eV in the "green gap," $In_{0.21}Ga_{0.79}N$/GaN MQW and DLOS samples were grown at 730°C. A sharp drop in IQE coincident with a 4x increase in [1.7 eV] for $In_{0.21}Ga_{0.79}N$ relative to $In_{0.17}Ga_{0.83}N$ films was observed. Greater enhancement of [1.7 eV] for only a 20°C reduction in T_g when indium was also increased suggests that reducing T_g and increasing indium content act in concert to enhance defect incorporation and degrade IQE. Possible origins and potential mitigation of the 1.7 eV level will be discussed. Sandia is a multi-program laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under Contract No. DE-AC04-94AL85000. 1. H. Yamada et al. Appl. Phys. Exp. 1 041101 (2008).

4:30 PM Student

Z4, Proton-Irradiated AlGaN/GaN HEMT at 5 MeV Protons: *Hong-Yeol Kim*[1]; Jihyun Kim[1]; Jaime Freitas, Jr.[2]; Michael Mastro[2]; [1]Korea University; [2]US Naval Research Laboratory

The efficiency and compact footprint of AlGaN/GaN high electron mobility transistor (HEMT) based circuits are attractive for communications applications in satellites. In low earth orbit, high energy protons bombard onto the device, which can cause degradation of the electrical properties. The optical and electrical properties of AlGaN/GaN epilayers grown on sapphire irradiated with high energy proton were investigated by low-temperature photoluminescence (PL) spectroscopy (with the 325 nm line of a He-Cd laser) and current-voltage measurements. The proton energy and fluence were 5 MeV and $2x10^{15}$ protons/cm^2, respectively. PL results prior to and after HEMT irradiation showed that the near bandedge peak at 355 nm decreased by 94 % as compared with that of the un-irradiated sample. In this PL data, two new lines at 350.27 and 359.53 nm were observed after irradiation, indicating that high-energy protons introduce defects within the structure, which reduce the intensity of the near bandedge emission band and lead to a disorder-generated LO phonon band. Electrical properties of the irradiated AlGaN/GaN were characterized to examine the role of the defects introduced by proton-irradiation. After proton irradiation, saturation current (I_{DS}-V_{DS}) decreased by 46 % at a 6 V source-drain voltage and 0 V gate voltage. The electrical parameters were relatively less sensitive than the optical parameters to the effects of proton irradiation. This suggests that the two-dimensional electron gas at AlGaN/GaN interface was very resistant to the proton irradiation. A simulation suggested that a thin electron channel is easily disrupted under low energy irradation but is transparent to higher energy protons. In contrast, the simulation suggests a thicker channel region presents a larger volume to absorb high energy protons and create deleterious defects.

4:50 PM

Z5, Effect of Traps Spatial Localization on GaN HEMT Static Characteristics: *Alessandro Chini*[1]; Valerio Di Lecce[1]; Michele Esposto[1]; Gaudenzio Meneghesso[2]; Enrico Zanoni[2]; [1]Università di Modena e Reggio Emilia; [2]Università di Padova

GaN HEMTs are continuously showing their impressive potential for RF and power switching application. Nevertheless their reliability still needs to be investigated in order to use them in commercial and military applications. Several authors have reported performance degradation both in the dynamic and static characteristics [1,2,3,4] of GaN HEMTs due to the formation of trap states [1,4] within the AlGaN barrier layer when high electric fields are applied to the gate-drain device junction. In this work we discuss how trap state formation during reverse gate-source and gate-drain step-stress tests can affect device static characteristics, and show through numerical simulations how the observed degradation can be explained by means of localized defects at the gate-source

or gate-drain edge in the AlGaN barrier. The devices tested were GaN HEMT grown on SiC substrates with a total gate periphery of 4x25µm and a 0.3µm gate length. Part of the devices tested were step-stressed by applying a negative gate-drain voltage of -2.5V/step for a total time of 5 minutes with the source terminal left open, while other devices were step-stressed by applying a negative gate-source voltage of -2.5V/step for a total time of 5 minutes with the drain terminal left open. In both cases device static I-V characteristics remained unchanged up to reverse voltage of approximately 25V after which a significant increase in reverse current as well as a decrease in DC current levels were observed. Gate-drain stressed devices showed an increase in output conductance as well as a softening of the knee-voltage while gate-source stressed ones showed a reduction of DC current levels in the I-V characteristics whose still showed a sharp knee and a low output conductance. Numerical Simulations carried out by means of the commercial DESSIS-ISE (Synopsis Inc.) simulator showed that acceptor traps placed at 0.5eV from the conduction band at the gate-drain or the gate-source edge within the AlGaN barrier can qualitatively explain the observed different devices degradation when applying gate-drain or gate-source high electric fields. [1] Joh Jungwoo et al., "Impact of Electrical Degradation on Trapping characteristics of GaN High Electron Mobility Transistors", IEEE IEDM 2008, Dec. 2008. [2] A. Chini et al., "Correlation between DC and rf degradation due to deep levels in AlGaN/GaN HEMTs", IEEE IEDM 2009, Dec. 2009. [3] E. Zanoni et al., "Localized damage in AlGaN/GaN HEMTs induced by reverse bias testing", IEEE Electron Device Letters, May 2009. [4] A. Chini et al., "Evaluation of GaN HEMT degradation by means of pulsed I-V, leakage and DLTS measurements", IET Electronics Letters, Apr. 2009.

THURSDAY PM

Session AA: Oxide Defects, Localized States, and Nanostructures

Thursday PM
June 24, 2010

Room: 141
Location: University of Notre Dame

Session Chairs: Holger von Wenckstern, Univ Leipzig; Martin Allen, Univ Canterbury

1:30 PM

AA1, Vacancy Defect and Defect Cluster Energetics in Ion-Implanted ZnO: *Leonard Brillson*[1]; Yufeng Dong[1]; Filip Tuomisto[2]; Andrej Kuznetsov[3]; Bengt Svensson[3]; [1]Ohio State University; [2]Aalto University; [3]University of Oslo

Despite nearly sixty years of research, several fundamental issues surrounding ZnO remain unresolved. Chief among these have been the difficulty of p-type doping and the role of compensating native defects. Oxygen vacancies (V_O), V_O complexes, Zn interstitial-related complexes, and residual impurities such as hydrogen and aluminum are all believed to be donors in ZnO, while Zn vacancies (V_Zn) and their complexes are considered to be acceptors. Although their impact on carrier compensation is recognized, the physical nature of the donors and acceptors dominating carrier densities in ZnO is unresolved. It remains a challenge to correlate the commonly observed 1.9-2.1 eV "red" and 2.3-2.5 eV "green" luminescence emissions with specific native defects. Previous optical absorption, photoluminescence, electron paramagnetic resonance, and depth-resolved cathodoluminescence spectroscopy (DRCLS) studies indicate a correlation between the "green" optical transition and O vacancies (V_O).[1] Still controversial, however, is how such visible emissions correlate with the energetics of Zn/O vacancies, interstitials, and their complexes overall. This work clearly identifies the physical nature of the defects dominating optical features of this widely studied semiconductor and, in turn, these defects provide a consistent explanation for ZnO's effective free carrier densities on a local scale.[2] We have used depth-resolved cathodoluminescence, positron annihilation, and surface photovoltage spectroscopies to determine the energy levels of Zn vacancies and vacancy clusters in bulk ZnO crystals. Here we augment the depth-resolved luminescence of energy level transitions involving native defects with recent positron annihilation spectroscopy (PAS) results to determine the energetics of V_Zn and their complexes in ZnO over both surface and near surface regions (7~1500 nm) in ion (Li or N) implanted and annealed bulk ZnO. The correspondence between these PAS native defect distributions and the DRCLS intensity distributions versus depth permits us to identify the luminescence energy associated with isolated VZn defects (~1.6 eV) as well as the energy shift due to vacancy cluster (1.9~2.1 eV) formation. Surface photovoltage spectroscopy (SPS) yields the positions of these levels with respect to the ZnO band edges. We associate the remaining deep level DRCLS emission (2.3~2.5 eV) with positively charged V_O-related defects, which are not detected by PAS, and describe how the balance between these donor and acceptor defects accounts for depth-dependent resistivity in these irradiated crystals. Taking these depth-resolved techniques altogether, we clearly identify the optical transitions and energies of V_Zn and vacancy clusters, the effects of different annealing methods on their spatial distributions in ion-implanted ZnO, and the contribution of V_Zn and V_O to near-surface resistivity. [1] L. J. Brillson et al., Appl. Phys. Lett. 90, 102116 (2007). [2] Y. Dong et al., Phys. Rev. B 81, R081201 (2010).

1:50 PM

AA2, O-H-Li-Complex in Hydrothermally Grown Single Crystalline ZnO: *Klaus Magnus Johansen*[1]; Hallvard Haug[1]; Pekka Tapio Neuvonen[1]; Knut Erik Knutsen[1]; Lasse Vines[1]; Edouard V Monakhov[1]; Andrej Yu. Kutnetsov[1]; Bengt Gunnar Svensson[1]; [1]University of Oslo

Results from Fourier Transform Infrared Spectroscopy (FTIR) and Secondary Ion Mass Spectrometry (SIMS) have been correlated to investigate the nature of the 3577 cm^{-1} local vibrational mode in four different hydrothermally grown ZnO wafers. This mode has previously been identified as the local vibrational mode of OH^- adjacent to Li on Zn-site [1], also referred to as the O-H-Li-complex. In this work we show that the integrated absorption of the 3577 cm^{-1} band does in fact not follow the variation in the total Li-concentration between the different wafers. Rather, it turns out that the strength of the band is correlated with the presence of non-homogenously distributed Li along the c-axis, as revealed by SIMS. Interestingly, the Li-distribution is reproduced in the lateral directions, as if Li is decorating an underlying structure of basal plane defects. This indicates that the 3577 cm^{-1} is only observed when there is a presence of basal plane defects in addition to Li and H.

2:10 PM

AA3, Induced Gap States at Zinc Oxide Surfaces and Interfaces: M.W. Allen[1]; J.G. Partridge[1]; D.H.-S. Kim[1]; *S.M. Durbin*[1]; [1]University of Canterbury

There has been considerable progress in our understanding of defects and doping in ZnO, despite the fact that the various preparation techniques (molecular beam epitaxy, sputtering, pulsed laser deposition, as well as bulk techniques such as hydrothermal and pressurized melt) yield considerably different material in terms of optical and electronic characteristics. Still, many open questions remain about surface and bulk defects, as well as doping limitations in this material. Metal-semiconductor junctions provide an interesting window into fundamental characteristics of a semiconductor, especially when high quality rectifying (Schottky) junctions can be realized. Beyond enabling transient techniques such as DLTS, even the basic properties of the junction and its formation create a probe for interface states which are often intimately related to bulk defect levels. However, practical aspects of fabricating Schottky contacts, such as lateral inhomogeneity, contaminants, and defects, can complicate the comparison of experimentally obtained barrier heights to theoretical predictions and extraction of information about intrinsic properties. The diode ideality factor η (which should approach unity for laterally homogeneous interfaces, after accounting for image force effects) is also strongly affected by the same issues, and correlations can be observed between barrier height and η when measuring large numbers of devices. Intriguingly, ZnO could prove to be an interesting test case for evaluating various theoretical Schottky contact formation models, as it is significantly more ionic than most semiconductors, resulting in weaker Fermi pinning due to interface states. ZnO also does not require the removal of a native oxide layer for device processing, thereby avoiding often aggressive cleaning procedures which can roughen or otherwise damage the surface. We have fabricated arrays of rectifying metal-ZnO contacts using bulk wafers and a wide variety of metals, using an eclipse pulsed laser deposition technique which

results in large barrier heights (typically > 0.8 eV) and low η (approaching the image force limit). Using the electrical characteristics of these near-ideal diodes, we evaluate both Tung's chemical bonding and Moench's metal induced gap states + electronegativity models. The lack of agreement with either of these popular models raises several questions, including whether predictions for the branch point energy in ZnO — a key parameter of induced gap states relevant to discussions of heterointerfaces as well as doping ability and gap states — are accurate. This work was supported in part by Marsden Fund grant UOC0604, the MacDiarmid Institute for Advanced Materials and Nanotechnology, and the University of Canterbury.

2:30 PM

AA4, Optical Properties of Gd Implanted ZnO Single Crystals: *John Kennedy*[1]; Peter Murmu[1]; Andreas Markwitz[1]; Ben Ruck[2]; Ruben Mendelsberg[3]; Roger Reeves[4]; P Malar[5]; Thomas Osipowicz[5]; [1]GNS Science; [2]Victoria University of Wellington; [3]The MacDiarmid Institute of Advanced Materials and Nanotechnology; [4]University of Canterbury,; [5]National University of Singapore

Rare earth (RE) elements doped Zinc oxide (ZnO) is being investigated intensively for spintronics applications. RE elements (e.g. Eu, Er, Tm and Gd) have been reported to create optical centres, and room temperature ferromagnetism in ZnO. The study of doping effects along with intrinsic defects in ZnO is of particular interest for better understanding of altered electronic structure which eventually modifies the optical and magnetic properties of the material. We present the results from a study of unimplanted and Gd implanted ZnO (0001) single crystals with fluences ranging from 4.6x1014 to 1.1x1016 Gd ions per square centimetre at an energy of 30 keV. The corresponding Gd atomic concentrations varied from 0.5 to 8.4 % per formulae unit. Average implantation depths were 10 to 12 nm and the maximum depth ranged from 20 to 25 nm. The implanted samples were subsequently annealed in a vacuum for 30 minutes at 650 and 750 □C. Rutherford backscattering and channeling techniques were employed to analyse the crystalline quality, damage recovery and Gd lattice site location. It was found that most of the Gd ions are incorporated into substitutional sites after the implantation. Photoluminescence (PL) of unimplanted ZnO shows the enhanced green emission on vacuum annealing along with typical UV emission at 5K. Most likely oxygen vacancies (VO), created by desorption of oxygen during vacuum annealing, could be origin of green luminescence. UV emission is due to recombination of an exciton bound to a neutral donor and its intensity is reduced in the Gd implanted samples due to structural degradation. Orange light emission is observed in place of green, which suggests the oxygen vacancies are compensated most likely by implanted Gd ions which in turn reduce the green emission. However, the exact origin of the orange emission is not known at present. Detailed results from structural, morphological and optical measurements will be presented at the conference.

2:50 PM

AA5, High-Resolution Laplace DLTS on $Mg_xZn_{1-x}O$ PLD Thin Films: *Holger von Wenckstern*[1]; Florian Schmidt[1]; Kerstin Brachwitz[1]; Matthias Schmidt[1]; Christof Dietrich[1]; Marius Grundmann[1]; [1]Universität Leipzig

The increasing interest in wide bandgap semiconductors puts, besides GaN-based material, ZnO and its alloys in the focus of semiconductor research. Potential applications are, e.g., UV optoelectronics, front contacts of solar cells, transparent transistors and HEMTs. For all these applications a profound knowledge of deep level defects in ZnO and related alloys is necessary for optimization of performance. Electrical investigations like deep level transient spectroscopy (DLTS) of binary ZnO revealed that the so-called E3 defect, having thermal activation energy E_t of 300 meV and an apparent capture cross-section σ_{app} of 2 &times 10^{-16} cm^2, is incorporated independent of the growth method. Laplace deep level transient spectroscopy (LDLTS) showed that a defect called E3' with similar emission rate as the E3 defect may also exist in bulk ZnO and thin films [1]; the separation of E3 and E3' is usually not possible with DLTS. For ZnO-based alloys such as MgZnO and CdZnO, having higher and lower bandgap than ZnO, respectively; very little data about defects exist. Only a recent study provides E_t and σ_{app} of E3 in $Mg_xZn_{1-x}O$ for $x < 0.09$ determined by thermal admittance spectroscopy (TAS) and DLTS [2]. In this contribution we will report TAS, DLTS and LDLTS measurements on $Mg_xZn_{1-x}O$ thin films with $x < 0.05$ to provide first comprehensive data on the incorporation of E3 and E3' in this ZnO-based alloy. We used ZnO and $Mg_xZn_{1-x}O$ thin films grown by pulsed-laser deposition on a-plane sapphire substrates. For all samples a 200 nm thick degenerately conducting ZnO:Al layer was deposited prior to the main layer to be used as Ohmic back contact of the diodes. Circular Schottky contacts were realized by reactive sputtering of Pd. All samples exhibit high rectification and low series resistance and are suited for TAS, DLTS and LDLTS. We demonstrate that defect parameters obtained from conventional DLTS are often erroneous for samples containing both the E3 and the E3' defect due to their similar emission rates. We provide means to conclude on the existence of the E3' defect in a particular sample by acquiring DLTS signals for different filling pulse lengths. Nevertheless, the electrical parameters of E3 and E3' may only be unambiguously determined by LDLTS. The LDLTS measurements on $Mg_xZn_{1-x}O$ thin films clearly show the incorporation of both E3 and E3' for low Mg-contents x &le 0.005. However, we do not observe E3' in samples with x &ge 0.009. This result could help to understand the higher reproducibility of $Mg_xZn_{1-x}O$ compared to ZnO MESFETs [3]. [1] Auret *et al.*, Physica B **401-402**, 378 (2007). [2] von Wenckstern *et al.*, J. Electron. Mater. (available online, DOI: 10.1007/s11664-009-0967-0). [3] Grundmann *et al.*, Mat. Res. Soc. Symp. Proc. **1201** (2010), in press.

3:10 PM Break

3:30 PM Student

AA6, Observation of a Strong Polarization Induced Quantum-Confined Stark Effect in $Mg_XZn_{1-X}O$/ZnO Quantum Wells: *Matthias Brandt*[1]; Holger von Wenckstern[1]; Marko Stölzel[1]; Alexander Müller[1]; Gabriele Benndorf[1]; Martin Lange[1]; Jan Zippel[1]; Jörg Lenzner[1]; Christof Dietrich[1]; Michael Lorenz[1]; Marius Grundmann[1]; [1]Universitaet Leipzig

The quantum-confined Stark effect (QCSE) has been observed for samples grown by molecular beam epitaxy (MBE) containing a $Mg_xZn_{1-x}O$/ZnO quantum well (QW)[1]. For the occurrence of the QCSE a difference in the electric polarization at the heterointerfaces, a significantly large QW width and abrupt interfaces are required. Quantum confinement effects in $Mg_xZn_{1-x}O$/ZnO QWs grown by pulsed laser deposition (PLD) were previously observed[2]. However, even for high QW widths no significant influence of the QCSE on the 2K luminescence was detected in these experiments. Similar results are reported by numerous authors for PLD grown $Mg_xZn_{1-x}O$/ZnO QWs[3]. In the experimental study reported here, the laser fluence in the PLD process was controlled in order to modify the energy of the particles in the laser plasma. This had a tremendous influence on the sharpness of the heterointerfaces. For an adequate choice of the laser fluence a systematic redshift of the QW luminescence with increasing well width of up to 230 meV below the emission of the free exciton in bulk ZnO was observed. Additionally, due to the decreased overlap of the electron and hole wave-functions the transition probability is reduced. An increase in the exciton lifetime up to 0.3ms is observed. Values previously reported for MBE grown samples[1], showing very high quality QW interfaces, are quantitatively different, with the longer decay time for a given red-shift in the PLD QWs. $Mg_xZn_{1-x}O$/ZnO heterostructures were grown by pulsed laser deposition (PLD) on a-plane sapphire and ZnO substrates. $Mg_xZn_{1-x}O$ grows pseudomorphically on ZnO substrates, leading to perfectly organized vicinal surfaces[4]. Pendellösung-oscillations were observed in high resolution X-ray diffraction, confirming the sharpness of the interfaces. A systematic linear dependence of the c-axis lattice constant on the Mg content in the barrier layer is seen for the samples grown on ZnO. The relation was explained by classical elastic theory, as well as similar data obtained on films grown by MBE[5]. In order to cover a large number of different thicknesses, wedge-shaped QWs were grown by leaving off substrate rotation during growth. Crystallizing in the wurtzite structure, both ZnO and $Mg_xZn_{1-x}O$ possess a spontaneous polarization. Upon the formation of a heterostructure an additional piezoelectric polarization component is introduced, increasing or diminishing the polarization. The difference in the spontaneous polarization in adjacent ZnO and $Mg_xZn_{1-x}O$ layers and its dependence on the Mg content x can be estimated from the thickness dependence of the transition energy and the exciton lifetime in the QW.

3:50 PM

AA7, Low Temperature Electrochemical Growth of ZnO Nanobelts, Nanowalls, Nanospikes and Nanowires: Growth Mechanism and Field Emission Study: *Debabrata Pradhan*[1]; Kam Leung[1]; [1]University of Waterloo

ZnO nanostructures are promising materials with a potential for several applications such as in the photonics, opto-electronics, electron field emissions and solar cells. In the present work, we deposited both the two-dimensional (i.e. nanowalls and nanobelts) and one-dimensional (i.e. nanospikes and nanowires) ZnO nanostructures on inexpensive conducting glass and plastic substrate using a facile electrochemical deposition technique. All the electrodeposition experiments were performed below 70°C. The electrolyte concentration, deposition temperature and deposition potential were found to significantly control the morphology of ZnO nanostructures. Glancing angle X-ray diffraction and transmission electron microscopy were used to obtain the crystallinity and growth direction of different ZnO nanostructures. Energy dispersive X-ray analysis and depth profiling X-ray photoelectron spectroscopy were used to measure the composition of as-synthesized materials, which suggested the cause for different nanostructure formation. In particular, Cl^- ions capping on the preferred [0001] growth direction of ZnO under fast hydroxylation kinetics condition observed at a higher $Zn(NO_3)_2.6H_2O$ electrolyte concentration (>0.05 M). The electron field emission measurement showed higher emission current density at a lower electric field from the nanospikes as compared to that of the nanowalls. This is attributed to the tapered tips of the nanospikes geometry which concentrates a higher electric field in comparison to the nanometer thick ledge of nanowalls. The nanospikes showed a turn-on electric field of 3.2 V/μm for 1 μA/cm^2 and threshold field of 6.6 V/μm for 1.0 mA/cm^2. This superior field emission property makes the nanospikes to be one of the best ZnO field emitter fabricated on a glass substrate at low temperature.

4:10 PM Student

AA8, Synthesis and Field Emission Characterizations of Well-Aligned Single-Crystal Al-Doped ZnO Nanowires Grown at Low Temperature: *Po-Yu Yang*[1]; Jyh-Liang Wang[2]; Wei-Chih Tsai[3]; Der-Ming Kuo[3]; Hau-Yuan Huang[3]; I-Che Lee[1]; Chia-Tsung Chang[1]; Sih-Yin Wang[4]; Shui-Jinn Wang[3]; Huang-Chung Cheng[1]; [1]National Chiao Tung University; [2]Ming Chi University of Technology; [3]National Cheng Kung University; [4]Chang Jung Christian University

ZnO nanowires (NWs) have attracted considerable interests as field emitters because of thermal stability, chemical stability, and high mechanical strength.1-3 Recently, the ZnO nanostructures are doped with group III metal elements, such as Al, In, and Ga, which can increase their electrical properties. To data, the low-temperature fabrications of Al-doped ZnO (AZO) NWs arrays and according field emission (FE) properties have not been reported yet. Therefore, the hydrothermal method was proposed to synthesis the pure ZnO and AZO NWs on glass substrates at a relatively low temperature, i.e. 85 °C. In this work, the optical, physical, and field emission characteristics of the low-temperature pure ZnO and AZO NWs with various dopant concentrations were systematically addressed. In experiments, a 200 nm-thick AZO film was sputtered on glass substrates to serve as a seed layer for the growth of pure ZnO and AZO NWs. The precursor solution containing zinc nitrate hexahydrate (Zn (NO3)2□6H2O, 2.5 mmol), hexamethylenetetramine (HMTA, 2.5 mmol) and distilled water. The aluminum nitrate nonahydrate (Al (NO3)3□9H2O) powders were used as the doping source to add in the precursor solution. Then the samples were placed in the mixed solution at 85 °C for 1 hour in a regular laboratory oven on a hot plate. After hydrothermal growth method growth, the samples were washed in DI water and dried in air. The FE-SEM images of the pure and AZO NW arrays growth were performed on the AZO/glass substrate. Both the Al-doped and undoped ZnO nanowires are well ordered and vertically aligned with controllable length (~1 μm) were obtained on the substrate. The near band-edge (NBE) emission peaks of pure ZnO and AZO NWs shift from 380 nm to 372 nm as the concentration of Al increases. This phenomenon was reported as blue-shift in emission peak and can be connected to Burstein–Moss effect because of the presence of the doped Al in the NWs. The FE characteristics of the pure ZnO and AZO NWs arrays with different Al-atomic concentration grown on AZO/glass substrates. The FE characteristics of AZO NWs arrays demonstrated the higher current density, lower turn-on field and lower threshold field, compared with that of pure ZnO NWs arrays. It suggests that the field emission characters of the ZnO NWs are noticeably improved with Al-doping and proportional to Al-doping amount. In short, a low-temperature hydrothermal growth method which is simple and easy to scale-up has been employed to synthesize the well-aligned arrays of AZO NWs with superior field emission characteristics, implying the potential for fabricating flexible optoelectronic and field emission devices.

4:30 PM Student

AA9, Correlation of ZnO Polar Surface Nanostructure with Native Point Defects: *Tyler Merz*[1]; Daniel Doutt[1]; Leonard Brillson[1]; [1]The Ohio State University

We used a complement of nanoscale depth-resolved cathodoluminescence spectroscopy (DRCLS), atomic force microscopy (AFM), Kelvin-probe force microscopy (KPFM), and surface photovoltage spectroscopy (SPS) to identify how surface morphology, nanostructure, and polarity of ZnO surfaces correlate with electronically-active native point defects. ZnO is a promising optoelectronic semiconductor with a striking ability to grow nanostructures, but its electronic surface and interface states are not well understood despite their impact on transport and recombination. Previous near-surface DRCLS showed that nanoscale asperities on bare ZnO surfaces exposed to ambient atmosphere for several months can have high trapped charge densities that dramatically increase free carrier recombination and band bending [1]. Not only do surface morphology and recombination velocity correlate within the outer tens of nanometers, but they associate with specific native point defects. SPS measures the filling and emptying of these states and thereby their energy level position in the band gap. In turn, CLS associates these optical transitions with oxygen and zinc vacancies, VO and VZn, respectively. Positron annihilation spectroscopy (PAS) showed that 2.1eV DRCLS emission correlates with VZn vs. depth, anticorrelating with 2.5 eV VO emission [2]. Furthermore, our KPFM-based SPS allowed us to correlate DRCLS optical emissions with optical filling and emptying transitions of the same near-surface regions across ZnO surfaces on a nanometer scale. These localized measurements also reveal Zn vacancy concentrations that increase with proximity to the most common nanostructures - nanorods, nanoclumps, step edges, and starburst patterns. These defects in fact play a role in spontaneous growth of nanoscale surface features. SPS spectra (fig. 1) display evidence for VZn charge emptying within fields of nano-"bumps" but not in flat ZnO surface areas. Near individual nanobumps, 2.1eV trap densities increase with proximity (fig.2) as do 2.1 eV vs. band gap nano-CLS spectra emissions. SEM-imaged hexagonal nano-pits display 2.1 eV intensities on the ZnO (0001) surface showing that growth of nanoscale features is mediated by the creation of sub-surface Zn vacancies as free surface Zn oxidizes. Furthermore, KPFM maps (fig. 3) before (a) vs. after (b) 2.25 eV illumination show increased potential that reveals large concentrations of VZn distributed non-uniformly around and extending away from AFM pit features. Low (<1 keV) electron beam energy DRCLS spectra and probe depths < 25nm show different deep level emissions dominating (fig.4) for the two polar surfaces. VZn emission dominates the Zn (0001) face while VO dominates O (000-1) spectra. These polarity affects manifest themselves not only in DRCLS but in potential maps and surface morphology as well. Our findings demonstrate the importance of polar effects in forming the surface and near-surface defects that in turn control the spontaneous formation of nanoscale asperities on ZnO surfaces.

4:50 PM Student

AA10, Evolution and Growth of Nanostructures on ZnO with Staged Annealing: *Daniel Doutt*[1]; Tyler Merz[1]; Leonard Brillson[1]; [1]The Ohio State University

We used atomic force microscopy (AFM), Kelvin probe force microscopy (KPFM), and surface photovoltage spectroscopy (SPS) to establish how nanostructures grow on polar ZnO surfaces. We have already shown that nanostructures grow spontaneously on ZnO surfaces with prolonged air exposure. These observations suggest that ZnO nanostructures grow by oxidation of Zn at the free ZnO surface and the extraction of Zn atoms from the underlying lattice. In order to explore the thermodynamics of this process, we have measured the

morphology, electric potential, and defect distributions of ZnO surfaces as a function of annealing temperature in flowing oxygen over a 400 ºC temperature range. These measurements reveal dramatic changes in surface morphology for both the Zn and O polar surfaces, the evolution of crystallographically oriented patterns with increasing temperature. These results confirm the pivotal role of ambient oxygen in the ZnO surface growth processes and reveal a characteristic activation energy that is consistent with theoretical predictions for Zn interstitial diffusion. AFM and KPFM maps (fig. 1) show the changes in surface morphology and contact potential with respect to temperature and gas exposure for representative 10x10 um areas of the same Zn (0001) surface. Deep (~150 nm) well defined hexagonal pits are seen on the room temperature and annealed surfaces with spoke-like trenches extending away from the corners and faces of hexagonal pits and trenches. Both these pits and the trenches show pronounced (> 50 mV) potential increases that increase further with annealing temperature. Conversely, O-polar (000-1) surfaces (fig. 2) initially show similar patterns with only light pitting, no well-defined geometry, and raised spokes extending from the edges of pits. After a 200 ºC anneal, this pitting increases with strong (~150 mV) negative potentials associated with pits and spokes. At 300ºC we see a dramatic growth of nanoscale "bumps" ranging from ~ 5 – 50 nm in height and further potential change. After the 300 ºC anneal, the difference in KPFM maps of the surface in the dark vs. after 2.25 eV illumination, i.e., optical transitions that empty VZn defect levels and reduce band bending [2], highlight the pronounced nonuniformities of these VZn potential variations.From the AFM increase in nanorod mass vs. temperature, Arrhenius plots of the oxygen face yield an activation energy of ˜150+10 meV. This low value suggests that the ZnO nanostructure growth occurs by Zn interstitial diffusion. Indeed, Zn interstitials are calculated to be fast diffusers with migration barriers of 0.57 eV [1]. The characteristic patterns of rays or trenches extending away from nanofeatures appear to align with crystallographic directions and suggest preferential pathways with lower migration barriers than in the bulk. Thus, coupled AFM, KPFM, and SPS appears to opens up a new avenue for studying nanostructures.

Session BB: III-V Novel Electronic Devices

Thursday PM
June 24, 2010

Room: 155
Location: University of Notre Dame

Session Chairs: Andrew Allerman, Sandia National Laboratories; Michael Manfra, Purdue University

1:30 PM Student

BB1, Demonstration and Room Temperature Electrical Characteristics of a Nitride Hot Electron Transistor with GaN Base of 10 nm: *Sansaptak Dasgupta*[1]; Nidhi Nidhi[1]; A. Raman[1]; J. S. Speck[2]; Umesh Mishra[1]; [1]ECE Dept. UCSB; [2]Materials Department, UCSB

A Hot Electron Transistor (HET) works on the principle of injection of 'hot' electrons above a barrier into a transit region (base), where they travel with minimal scattering and are collected in the collector. It is thus possible to obtain near ballistic transport in these devices, larger current drives and operation at frequencies higher than conventional (diffusive transport) transistors. In this work, we report on GaN based unipolar HETs which show room temperature operation. The device structure consists of 40 nm of AlGaN (24%) Si doped 1 x 10^{18} cm^{-3}, a 10 nm GaN base doped 1 x 10^{19} cm^{-3} and a 7% AlGaN collector doped 7 x 10 ^{17} cm^{-3}. The epilayer is grown by PAMBE on GaN (0001) templates. The device is fabricated by etching the emitter mesa to the base and then etching the base down to the collector contact layer, and subsequent depostion of ohmic metal stack of Al/Au. The Base-Emitter diode and base-collector diodes which are isotype N-n junctions have been characterized and they show thermionic emission characteristics at forward bias. Common base measurements demonstrate an α of ~ 0.97 which is commensurate with a β of 35 - 40. Peaks due to quasi ballistic transport of hot electrons which are injected into the base are observed in conductance measurements (δIc δVcb). Device analysis and effect of different e-b and b-c barriers would be discussed.

1:50 PM Student

BB2, Novel Cs-Free GaN Photocathodes: Neeraj Tripathi[1]; L. Bell[2]; Shouleh Nikzad[2]; Mihir Tungare[1]; Puneet Suvarna[1]; Ryan Vinson[1]; *Fatemeh (Shadi) Shahedipour-Sandvik*[1]; [1]University at Albany, State University of New York; [2]Jet Propulsion Laboratory, California Institute of Technology

GaN and AlGaN based photocathodes have attracted considerable attention for their application in image intensifiers, astronomy and UV detection and emission systems. Small electron affinity of AlGaN alloy allows development of high quantum efficiency negative electron affinity (NEA) photocathodes with significant advantages such as solar blindness, radiation hardness and low noise. Conventional photocathodes achieve NEA by cesiating the photocathode surface. Fabrication, optimization, and installation in vacuum is required for cesiated photocathodes due to the high chemical activity of the Cesium. Such requirement increases cost and limits the range of potential applications. Further, such photocathodes have been reported to suffer from chemical instability and degradation with time. Here we report on a novel Cs-free GaN based photocathode that utilizes band engineering near the photocathode surface to achieve permanent NEA. Device structure is composed of a Mg doped GaN template grown on sapphire, followed by Si-delta doping and a thin n+GaN cap. By placing a Si delta doped layer on the Mg doped GaN surface conduction band of the overall structure is pulled close to the Fermi level of the p-GaN. A thin n+GaN cap is deposited to provide stability to the Si-delta doped layer. Device design parameters including Si-delta doping and thickness of n+GaN cap layers play a critical role in determining the emission threshold and quantum efficiency of the device. Further, polarization induced charges at the device surface influence the device characteristics. We have performed physics based simulations to optimize the device design parameters taking into account polarization induced surface charges. Device structures have then been epitaxially grown using a Veeco D180 MOCVD system and characterized using secondary ion mass spectroscopy (SIMS) and photoemission (PE) measurements. A series of growth experiments with varying conditions have been performed to optimize Si incorporation in the delta doped layer and quality and thickness of the n+GaN cap layer. Emission threshold of the device has been observed to increase with increase in the n+GaN cap thickness. Such behavior has been successfully modeled and is attributed to local electric fields caused by the negative polarization induced surface charges. Quantum efficiency of the device follows systematic exponential decay with increase in n+GaN cap thickness. Increase in Si incorporation in the delta doped layer, up to the optimum value, has shown to improve device characteristics. Further increase in Si incorporation caused increase in emission threshold and degradation of the photocathode surface. Results of our simulation and experimental work including device growth, optimization and characterization will be discussed.

2:10 PM

BB3, Influence of MOVPE Growth Conditions on Intersubband Absorption in AlN –AlGaN Superlattices: *Andrew Allerman*[1]; Jonathan Wierer[1]; Qiming Li[1]; Mary Crawford[1]; Stephen Lee[1]; [1]Sandia National Laboratories

The large conduction band offset (~ 2 eV) in AlN and GaN heterostructures, along with rapid (< 1ps) intersubband (ISB) transitions between confined states drives interest in utilizing AlN-GaN superlattices for ultra-fast, optical switches (~1 Tb/s) and electro-optical modulators operating at telecom wavelengths (λ = 1.55 μm). Optical ISB absorption in nitride quantum wells has been previously observed down to 1.08 μm with absorption recovery times of 150-400 fs. To date, structures grown by molecular beam epitaxy have exhibited ISB absorption at the shortest wavelengths with the narrowest line-width, indicative of monolayer abrupt interfaces. Growth of similar structures by metal-organic vapor phase epitaxy (MOVPE) has resulted in ISB absorption at longer wavelengths with broader line-widths. The lower performance of structures grown by MOVPE has been attributed to interface roughness and thickness fluctuations due to the higher growth temperatures typically employed. Recently, Yang *et. al.* have reported ISB absorption peaked at 1.52 μm in MOVPE structures grown at significantly lower growth temperatures (830°C) where the wells were grown by means of a pulsed-growth approach to increase the electron concentration. In this work, we investigate the effect of MOVPE growth conditions on the performance of AlN-AlGaN superlattices designed to exhibit ISB transitions in

the near infrared without the need for pulsed growth approaches. Superlattices consisting of 20 periods of AlN barriers (~ 52Å) and $Al_{0.10}Ga_{0.90}N$ wells (10-15 Å) were grown conventionally, without pulsing, on 2.8 µm thick AlN films on sapphire. Wells were doped with Si at levels that achieved electron concentrations of $5x10^{19}$ or $1x10^{20}$ cm^{-3} in separate calibration growths. Optical absorption was measured by Fourier transform infrared spectroscopy on samples that are 5-8 mm wide with facets polished at ~45°. A significant shift in absorption to shorter wavelengths and narrower linewidths was observed in samples grown at lower growth temperatures suggesting improved interface abruptness. Absorption was peaked at 1.64 µm with a FWHM of 130 meV in a sample grown at the lowest temperature investigated, 760°C. Omega-2theta x-ray diffraction (XRD) scans about the (0002) reflection of samples grown at lower temperatures (885-760°C) showed additional higher-order satellite peaks that were not observed in samples grown at high temperature (1010°C). TEM images confirm improvement in interface abruptness in ISB structures grown at lower temperatures. AFM images reveal step-flow growth in all samples; however, pits and more complex structures appear at step edges in samples grown at 930°C and lower. Relationships between growth conditions, interface abruptness and ISB absorption will be discussed. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

2:30 PM Student

BB4, Engineering Ferromagnetism in Gd-Doped GaN Two-Dimensional Electron Gases: *Jing Yang*[1]; D. Hoy[1]; S. Carnevale[1]; E. Uchaker[1]; R. Myers[1]; [1]Ohio State University

In ferromagnetic semiconductors, the magnetization and spin polarization can be controlled with an electric field. These properties could be utilized in proposed spin-transistors in which, besides traditional charge gain, spin inputs and outputs could be electrically controlled and amplified. Such a device would exhibit low power switching and offer a spin functional platform for novel logic and memory devices. While hole-mediated ferromagnetism in GaMnAs is well established, after more than a decade of intensive work it exhibits low Curie temperatures (~170K) and requires unpractical electric fields to control the ferromagnetism. There are countless reports of above room temperature ferromagnetism in magnetically-doped wide band gap semiconductors, including bulk $Ga_{1-x}Gd_xN$. Unfortunately for these materials, evidence of a coupling between the electronic structure of the host semiconductor and the ferromagnetic phase is lacking. Here we utilize confinement and polarization engineering to explore magnetic coupling between Gd-ions and electron spins in AlN/GaN two dimensional electron gases (2DEGs) grown by plasma-assisted molecular bean epitaxy. Such 2DEGs might enable an n-type ferromagnetic semiconductor heterostructure that could be easily controlled with a gate bias. Structural characterization by SIMS, AFM, and HRXRD is used to study the incorporation of Gd in GaN by both δ-doping and statistical doping and to test for second phase precipitates, such as rock salt GdN. Using SQUID and Hall effect measurements, we examine the dependence of the magnetic and electronic properties as a function of the distance (d) between δ-doped Gd (~$10^{14}$$cm^{-2}$) region and the AlN/GaN interface which is adjacent to the high density electron sheet (~$10^{13}$$cm^{-2}$). Initial structures exhibit ferromagnetism, but additional optical and electronic measurements are needed to determine if the observed ferromagnetism is coupled to the electronic structure of the 2DEG.

2:50 PM

BB5, Nearly Ideal Current-Voltage Characteristics of Schottky Barrier Diodes Directly Formed on GaN Free-Standing Substrates: *Jun Suda*[1]; Kazuki Yamaji[1]; Yuichirou Hayashi[1]; Tsunenobu Kimoto[1]; Kenji Shimoyama[2]; Hideo Namita[3]; Satoru Nagao[3]; [1]Kyoto University; [2]Mitsubishi Chemical Corporation; [3]Mitsubishi Chemical Group Science and Technology Research Center, Inc

GaN-based electronic devices have attracted much attention due to its potential for low on-resistance and high operation temperature. At present, these devices are fabricated by using epitaxial layers. On the other hand, most of Si electronic devices are directly formed on Si substrate without epitaxial growth process. Recently, high-quality GaN free-standing substrates are available by various methods. It is important to assess the possibility of GaN-based electronic devices directly formed on GaN substrates. In this study, we fabricated Schottky barrier diodes directly on hydride vapor phase epitaxy (HVPE)-grown GaN free-standing substrates. Substrates with different donor concentrations ranging from $1x10^{16}$ to $2x10^{17}$ cm^{-3} were prepared. The threading-dislocation densities (TDD) of these substrates were estimated to be $3x10^6$ cm^{-2} by cathodoluminescence mapping. After formation of backside Ohmic contacts by Ti/Al, Ni Schottky contacts were formed by physical evaporation directly on chemical mechanical polished (CMP) GaN surfaces. The diameter of electrode is 100-300 µm. Current-voltage (I-V) characteristics and capacitance-voltage (C-V) characteristics were measured at room temperature. We have measured 10-50 diodes for each substrate. A small number of diodes exhibited leaky characteristics. We excluded these diodes from the following analysis, since these diodes may contain macroscopic defects originating from substrate itself or device processing. The diodes showed ideal forward I-V characteristics. The I-V curves were well fitted by the formula ($I=I_0\{\exp(eV/nkT)-1\}$) with series resistance. Ideality factors (n) of the diodes were 1.02-1.03 for all substrate. Barrier heights of these diodes were estimated to be 0.93 eV from I_0. Almost identical barrier heights were obtained from built-in potential of $1/C^2$-V plots. The doping range investigated is rather high. In the case, thermionic field emission (TFE) instead of simple thermionic emission (TE) should be considered. We calculated reverse I-V characteristics by TFE theory with values of barrier height and accurate doping concentration obtained from forward I-V and C-V characteristics. Measured reverse I-V characteristics showed excellent agreement with the calculations. The agreement was observed for all diodes with the doping range investigated. As a reference, we also fabricated Schottky diodes on GaN heteroepitaxial layers grown on sapphire substrates by metalorganic vapor phase epitaxy (MOVPE). The TDD of layers was 10^9 cm^{-2}. The diodes exhibited good forward characteristics. However, for reverse bias, measured currents were four orders of magnitude larger than that predicted from TFE theory. Reverse leakage is severely affected by high-density threading dislocations in the MOVPE-grown GaN diodes.These results indicate that surface damaged layer due to CMP process and leakage current due to threading dislocations ($3x10^6$ cm^{-2}) are negligible for Schottky diodes directly fabricated on HVPE-grown GaN substrates with doping range of $1x10^{16}$ to $2x10^{17}$ cm^{-3}. Our results show that CMP-processed HVPE-grown GaN substrates have a potential for electronic device fabrication.

3:10 PM Break

Session CC: III-N HEMTs II

Thursday PM
June 24, 2010

Room: 155
Location: University of Notre Dame

Session Chairs: Andrew Allerman, Sandia National Laboratories; Michael Manfra, Purdue University

3:30 PM Student

CC1, High Al Composition $Al_{0.72}Ga_{0.28}N$/AlN/GaN Heterostructures with High Mobility Two-Dimensional Electron Gases: *Guowang Li*[1]; Yu Cao[1]; Huili Xing[1]; Debdeep Jena[1]; [1]University of Notre Dame

Low Al composition (<40 %) AlGaN high-electron mobility transistors (HEMTs) have been an excellent technology platform for both high power and high frequency applications. Deep sub-micrometer HEMTs with decreasing barrier thickness are required to further boost the device performance. For AlN barrier, low contact resistance comparable to AlGaN barrier is hampered by the wide band gap of AlN (6.2 eV). A high Al composition AlGaN barrier layer can provide a high 2-D electron-gas (2DEG) density, and allow AlGaN thickness scaling. However, few groups reported on the growth of high Al composition AlGaN/GaN HEMT structures and the room temperature (RT) electron mobility has been limited to 500 cm^2/Vs with Al composition higher than 70%. Molecular beam epitaxy (MBE) grown high Al composition AlGaN has been observed to

suffer spontaneous phase modulation. We report the study of 2DEG structures with high Al composition (>70%) AlGaN grown by plasma-assisted MBE. In metal-rich regime, with the Ga flux of (1.1 - 1.3) × 10^{-7} torr, Al flux of 4.3 × 10^{-8} torr, RF power of 275 W and thermocouple temperature ranging from 580 to 680°C, the epitaxial growth of relatively thick (>3 nm) high Al composition AlGaN directly on top of GaN always results in hexagonal stripes. The origin of the stripes is still under investigation, and we suspect it might be related to lateral phase separation. However, by inserting an ultrathin (<1 nm) AlN spacer, the surface morphology was dramatically modified and consisted of atomic steps. The growth rate and Al composition of the AlGaN layer were calibrated by high-resolution X-ray diffraction (XRD) measurement of a nine-period 2.7 nm/0.6 nm/26.7 nm $Al_{0.72}Ga_{0.28}N$ /AlN/GaN multiple quantum well calibration structure. The AlN spacer thickness was kept around 0.6 nm. The polarization-induced 2DEG density increases with total barrier thickness for samples with AlN spacer and 72% AlGaN. For HEMTs heterostructures with 3.9 nm/0.6 nm $Al_{0.72}Ga_{0.28}N$ /AlN barrier, at room temperature the 2DEG mobility reaches 1140 cm^2/Vs at a sheet density of 2.3 × 10^{13} cm^{-2}, which yields low sheet resistance of 238 /□. For the samples without AlN spacer the electron mobility is typically about 120 cm^2/Vs at room temperature and there was no clear increase at 77 K. In conclusion, we have succeeded in demonstrating high Al composition alloy AlGaN/GaN HEMT structures with high carrier mobility. An ultrathin AlN interlayer was crucial to suppress phase separation and yield high mobilities, paving the way for deep submicron HEMTs.

3:50 PM Student

CC2, Two-Dimensional Electron Gas in $In_XAl_{1-X}N$/Aln/GaN Heterostructure Field-Effect Transistors Depending on Indium Composition: *Suk Choi*[1]; Hee Jin Kim[1]; Zachary Lochner[1]; Bravishma Narayan[1]; Yun Zhang[1]; Shyh-Chiang Shen[1]; Jae-Hyun Ryou[1]; Russell Dupuis[1]; [1]Georgia Institute of Technology

AlGaN/GaN heterostructure have been successfully used for heterostructure field-effect transistors (HFETs) as high density two-dimensional electron gas (2DEG) can be generated effectively from their large lattice mismatch and high piezoelectric field. However, attempts to enhance device performance by increasing Al composition in AlGaN barrier layer have not been very successful, because large tensile strain caused by high Al composition leads to relaxation of barrier layer and low crystalline quality which reduces 2DEG density. To resolve this problem, use of nearly in-plane lattice-matched InAlN barrier with ~18% of In composition on top of GaN is proposed. Lattice-matching $In_{0.18}Al_{0.82}N$ barrier layer can minimize strain-induced layer quality depreciation while its higher spontaneous polarization field than $Al_{0.25}Ga_{0.75}N$ generates high density of 2DEG and high carrier mobility over AlGaN/GaN HFETs. In addition, strain and polarization field engineering is possible by controlling In composition of barrier layer. If the In composition in InAlN barrier layer is lower than 18%, tensile strain in the layer will produce piezoelectric field which is aligned in the same direction to spontaneous polarization field and threshold voltage will be negatively shifted. On the contrary, In composition higher than 18% in barrier layer will produce compressive strain and piezoelectric field which is antiparallel to spontaneous polarization field. As a result, piezoelectric polarization field and spontaneous polarization field compensate each other, and threshold voltage shifts toward positive direction. Therefore, InAlN/GaN HFET structure with appropriate In composition and compressively strained barrier layer is expected to exhibit enhancement mode operation with positive threshold voltage. In this study, we report novel method for 2DEG engineering to achieve enhancement mode operation of InAlN/GaN HFETs. InAlN/GaN heterostructures with high quality InAlN layer were grown by using metalorganic chemical vapor deposition (MOCVD) with various In composition from 18% to 25%. The threshold voltage of fabricated HFETs were measured to be -3V for HFETs with $In_{0.18}Al_{0.82}N$, -1.25V for $In_{0.22}Al_{0.78}N$, and -0.1V for $In_{0.25}Al_{0.75}N$. The fabricated device shows good feasibility for enhancement mode operation of InAlN/GaN HFETs. Characterization on epitaxial structure and HFET devices will be reported.

4:10 PM

CC3, Source-Drain Regrowth by MBE in Metal-Face AlN/GaN HEMTs: *Chuanxin Lian*[1]; Yu Cao[1]; Ronghua Wang[1]; Guowang Li[1]; Tom Zimmermann[1]; Debdeep Jena[1]; Huili Xing[1]; [1]University of Notre Dame

AlGaN/GaN HEMTs have established themselves in high speed high power electronic applications, thanks to the large breakdown field, heterostructure design freedom, and unique polarization-induced 2DEG properties. A challenge in improving the HEMT frequency performance is scaling down the device dimension both laterally and vertically at the same time without sacrificing the 2DEG transport properties. Compared with AlGaN/GaN, AlN/GaN structures allow very small gate-2DEG distance (1-4 nm) for the ease of vertical scaling while maintaining decent 2DEG properties: large 2DEG density, high mobility and good charge confinement . Besides downscaling of the device dimension, low source/drain contact resistance is also required for high frequency performance. By far, the ohmic contact resistance on AlN/GaN source/drain areas is usually above 0.4 ·mm due to the large energy barrier height of AlN. In this work, we have explored the source/drain regrowth with heavily-doped (In)GaN materials on metal-face AlN/GaN heterostructures. The AlN/GaN heterostructure sample used in this work was grown by MBE in a Veeco Gen 930 system. The AlN barrier is 4 nm thick; and the 2DEG density and mobility are measured to be 3.1e13 cm-2 and 1193 cm2/V.s, resulting in a sheet resistance of 170 /sq. Other GaN HEMT structures have also been used for developing the device fabrication and regrowth processes. The HEMT source/drain areas were first etched, and then, using tungsten as regrowth mask, heavily doped (Si: ~ 10e20 cm-3) InN(30 nm)/graded-InGaN(50 nm)/GaN (20 nm) were regrown by MBE. Control samples were also prepared by regrowing the same structure on semi-insulating GaN templates for further characterization. After regrowth, the amorphous material deposited on the tungsten mask was removed by molten KOH, and the tungsten mask was removed by H2O2. The XRD scans on the control samples reveal that a linearly graded InGaN from GaN to InN can be successfully regrown. The TLM measurement of non-alloyed Ti-based ohmic contacts deposited on a control sample indicates that contact resistances of ~ 0.2 ·mm with sheet resistances of ~ 100 /sq can be achieved on the regrown InN/InGaN/GaN. In the first regrowth experiment of source/drain on a HEMT, a gap was observed between the regrown material and the 2DEG channel, leading to a large contact resistance. To eliminate the gap, the migration enhanced epitaxy (MEE) technique was applied. After exploring several growth conditions, no gap was seen under SEM and AFM imaging. However, electrical measurements using non-alloyed Ti-based contacts on the regrown source/drain in HEMTs showed unacceptably large resistances. To understand its causes, the transmission electron microscope investigation is under way to interrogate the regrowth-sidewall interface. Studies are also currently being carried out to minimize damages to the 2DEG channel during the sample preparation as well as regrowth.

4:30 PM Student

CC4, AlGaN/GaN High Electron Mobility Transistors for Large Current Operation Achieved by Selective-Area Growth Using Plasma-Assisted Molecular Beam Epitaxy: *Liang Pang*[1]; Hui-Chan Seo[1]; Patrick Chapman[1]; Philip Krein[1]; Jung-Hee Lee[2]; Kyekyoon Kim[1]; [1]University of Illinois at Urbana-Champaign; [2]Kyungpook National University

GaN is a promising candidate material for high-power device applications. Although much progress has been made on GaN-based microwave power devices, power switching devices is still a new and immature research area, despite the fact that they have wide applications like inverters. In developing devices for power-switching applications, there are three key challenges: achievement of low on-state resistance, high current density and high breakdown voltage. We previously reported that selective-area growth (SAG) by plasma-assisted molecular beam epitaxy (PAMBE) is able to improve the contact resistance and current density over conventional contact scheme including ion-implantation. Twofold increase in the breakdown voltage also shows that unlike ion-implantation, SAG does no harm to the device breakdown behavior. In this study, SAG is employed to fabricate high electron mobility transistors (HEMTs) for high current operations. Furthermore, use of a gate insulator is investigated to confirm that GaN HEMTs processed by SAG is able to achieve

high breakdown voltages. An $Al_{0.26}Ga_{0.74}N$ (25 nm)/GaN (50nm)/semi-insulating GaN (2.2µm) on sapphire substrate prepared by MOCVD was used as the starting material. Device isolation and recessed drain/source structure were achieved by dry etching. SAG was done by growing a 54nm thick n^+-GaN layer ($1.0x10^{19}cm^{-3}$) with PAMBE and subsequently removing the poly-GaN and SiO_2 mask by a molten KOH solution. Alloyed metals of Ti/Al/Ti/Au were deposited on n^+-GaN for the Ohmic contact, and Ni/Au metals for the Schottky gate. For gate insulation, a layer of SiN/SiO_2 was deposited by PECVD in the gate region before gate metal deposition. Each device unit consisted of four HEMTs (W_g=100µm) sharing the same source, drain and gate electrodes. 15 device units were connected by wire bonding for large current operations. Single device unit processed via SAG showed a current of over 0.1A, more than twice that of the one without SAG. Significant improvement of on-state resistance was also observed. A maximum current of 1.4A was achieved for a total gate width of only 6mm. The current density was higher than many of the previously reported values, demonstrating that same current level can be achieved with smaller device area when SAG is employed. Schottky property between the gate and the drain for single device unit was studied. At V_{gd}=200V, the gate leakage was as low as 0.7mA. The breakdown voltage under high current operation will be measured by the curve tracer, and the power device figure of merit (FOM) will be investigated.

4:50 PM

CC5, Transport Studies of AlGaN/GaN Heterostructures with Variable SiN_x Passivant Stress: Tamara Fehlberg[1]; Jason Milne[1]; Gilberto Umana-Membreno[1]; Stacia Keller[2]; Umesh Mishra[2]; Brett Nener[1]; *Giacinta Parish*[1]; [1]The University of Western Australia; [2]University of California (Santa Barbara)

It is well known that AlGaN/GaN-based transistors are highly suitable for high power and/or high frequency, robust operation in applications such as RF and mm-wave communications, power electronics and more. To achieve success in development of such devices it has been necessary to introduce steps to circumvent certain properties that are device-detrimental, some of which are not yet completely understood. One such issue is that of the use of dielectric layers. These have been introduced as passivation to combat the well-known issue of DC-RF current dispersion, for field plating, and for gate dielectrics to achieve enhancement-mode devices, necessary for power switching applications. For the most part, the effect of the introduced dielectric layers has been investigated with respect to overall transistor device performance, that is, macroscopic parameters such as drain current, rather than the effect on the 2DEG channel itself. However, assessing the changes induced in the transport properties of the 2DEG as a result of application of these layers is an important step in gaining a better understanding of the role of these layers in altering device performance. In this work, the influence of passivation with silicon nitride of different stress states on the 2DEG transport in $Al_xGa_{1-x}N$/GaN heterostructures is presented for the first time as a function of varying Al mole fraction (x). Samples from four heterostructures with x = 0.15, 0.23, 0.29 and 0.35 were deposited with SiN_x by plasma enhanced chemical vapour deposition under compressive, neutral (slightly compressive), and tensile stress conditions (stress was measured for the same films deposited on silicon wafers). For each piece (different compositions and different SiN_x layers) Hall bars were fabricated and the transport properties were measured using a variable magnetic field Hall technique, at 25, 77, 150 and 300K, up to 12T magnetic field. All types of SiN_x passivant induced an increase in 2DEG concentration, consistent with previous published results for SiN_x passivation. In addition, however, the 2DEG mobility increased significantly after passivation for the sample with x = 0.15. The more tensile the film stress, the greater was the percentage increase in mobility. However this percentage change decreased with increasing Al mole fraction. It is evident that silicon nitride passivation of $Al_xGa_{1-x}N$/GaN structures induces different changes in 2DEG carrier concentration and mobility, dependent on both stress in the SiN_x thin film and the Al mole fraction. It is equally apparent that there is a complex relationship between these different factors, and that the stress in the SiNx passivation layer plays some, but not always the principal, role in determining the 2DEG transport properties. Thus tailoring of the deposition conditions to optimise transport properties is critical for a given passivant and Al mole fraction, to maximise device performance.

Session DD: Oxide Semiconductor Heterojunction Diodes

Friday AM
June 25, 2010

Room: 102
Location: University of Notre Dame

Session Chairs: Deli Wang, Univ of California, San Diego; Jamie Philips, Univ of Michigan

8:20 AM

DD1, Ultraviolet Photodetectors with Novel Oxide Thin Films: *Shizuo Fujita*[1]; Takumi Ikenoue[1]; Naoki Kameyama[1]; Takayoshi Oshima[1]; [1]Kyoto University

A variety of wide band gap oxide semiconductors, which are recognized as stable and environmental-friendly materials, can meet various demands for detectable wavelength, sensitivity, cost, and endurance of ultraviolet photodetectors, in contrast to III-nitride semiconductors which always needs high-cost and dangerous sources for their growth. In this presentation, we report several oxide semiconductors we have developed as the materials for ultraviolet photodetectors. Ga_2O_3 possesses large band gap of 4.8 eV (258 nm), which is suitable for UV-C photodetectors. HIgh quality Ga_2O_3 substrates allow the Schottky-type photodetectors using high-resistive layers formed on the substrates by thermal annealing in oxygen atmosphere. The photodetector exhibited the photoresponsivity of 0.037 A/W at 250 nm with the external quantum efficiency of 18 %. The photodetector was capable of detecting solar-blind light of as weak as 1 nW/cm^2 from the flame in normal room lighting. Robust properties of Ga_2O_3 against defect generation have allowed hundred-hours operation without noticeable degradation as a power monitor for a low-pressure mercury lamp (254nm, 40 mW/cm^2). A SnO_2 semiconductor, whose band gap is about 4 eV (310 nm), is desirable for UV-B photodetectors. Molecular beam epitaxy (MBE) and thermal annealing resulted in high resistive (5×10^6 cm) SnO_2 layers on sapphire substrates. Forming interdigital Au/Ni electrodes on the SnO_2 layer, the sample operated as a UV-B photodetector with the photoresponsivity of 0.023 A/W at 290 nm with the external quantum efficiency of 10%. Oxide semiconductors can be grown by low-cost and solution-based growth techniques, which allow simple fabrication process and inexpensive devices. With the ultrasonic spray mist chemical vapor deposition where safe and inexpensive sources can be used in a simple system, Schottky-type photodetectors of PEDOT:PSS/ZnMgO were successfully fabricated on glass substrates using metal mask patterning. In spite of the low cost and low power consumption processes for the device fabrication, the photodetectors exhibited reasonably high photoresponsivity, for example, 0.074 A/W at 320 nm with the external quantuim efficiency of 36.5%. The cut-off wavelengths were tunable between 370 and 300 nm by the Mg concentrations in ZnMgO. We believe that oxide semiconductors can be key materials for the photodetectors of ultraviolet light of a variety of wavelengths and intensity.

8:40 AM Student

DD2, Polarization-Sensitive Schottky Photodiodes Based on A-Plane ZnO/ZnMgO Multiple Quantum-Wells: *Gema Tabares*[1]; Adrian Hierro[1]; Christiane Deparis[2]; Christian Morhain[2]; Jean-Michel Chauveau[2]; [1]ISOM-Dept. Ingenieria Electrica, Universidad Politecnica de Madrid, Spain; [2]CRHEA-CNRS

ZnO is attracting much attention since it is a perfect candidate for various sensors, including piezoelectric devices and UV photodetectors. Particularly, polar-ZnO shows spontaneous polarization and a piezoelectric field along the c-direction, so in order to exploit its polarization potential, nonpolar ZnO whose polar axis lies in the growth plane is a good candidate for developing polarization-sensitive photodetectors (PSPDs). We present here an analysis of the spectral response dependence on light polarization of Schottky photodiodes based on non-polar a-plane ZnO/MgZnO multiple quantum wells (MQW) grown on R-plane sapphire by molecular beam epitaxy. The structures have varying QW thickness, from 1.5 to 5.6 nm, and varying Mg contents in the barrier, from 29 to 40%, allowing the absorption edge to be tuned from 3.38 to 3.51 eV. Semitransparent Au-Schottky diodes (100 Å) with an excellent rectifying behavior have been achieved through optimization of the surface passivation with H2O2. Coplanar to the Schottky contacts, extended back ohmic contacts have been defined with a Ti/Al/Ti/Au layer. Under illumination with above quantum-well excitation energy the I-V characteristics become non-rectifying, with large saturation currents and ideality factors. The origin of this I-V degradation under illumination will be addressed through analysis of the spectral and time response of the detectors. The photodiodes present a sharp absorption edge in their responsivity characteristics. As an example, the responsivity of the ZnO/ZnMgO (MQW) photodiode shows a sharp onset at 3.38 eV, for un-polarized light illumination conditions and a UV/VIS rejection ratio of 10^4. In order to analyze the polarization sensitivity of the photodiodes, a Glan-Taylor prism was used to linearly polarize the light. The normalized spectral response of the ZnO/$Mg_{0.37}$ $Zn_{0.63}O$ MQW-photodiode for polarization angles between 90º and 0º respect to the c-axis shows absorption edges at 3.35 eV (E perpendicular to the polar axis, E-c) and 3.37 eV (E parallel to the polar axis, E||c), respectively. The responsivity shows a clear shift of the absorption edge by ~23 meV, with a maximum differential responsivity ($R\text{-}/R_{\|}$) of 0.38 at 3.37 eV. Using the un-normalized responsivities, the PSPD has ($R\text{-}/R_{\|}$)max= 5 mA/W. At 3.37 eV the polarization sensitivity contrast ($R\text{-}/R_{\|}$) reaches ~2.5. Taking into account the accumulated residual strain at the QWs, the excitonic resonances for E-c and E||c light polarization conditions may be assigned to the E_1 and E_2 transitions, respectively.

9:00 AM

DD3, A New Approach to Make ZnO-Cu_2O Heterojunctions for Solar Cells: *Aurelien Du Pasquier*[1]; Ziqing Duan[1]; Yicheng Lu[1]; [1]Rutgers State University

Recently, the ZnO-Cu_2O heterojunction based solar cells have attracted considerable research interests due to the low-cost and abundance of the materials and favorable electronic properties. Cuprous oxide (Cu_2O) is a p-type semiconductor with a direct bandgap energy of 2.1 eV. Cu_2O acts as a photovoltaic absorber that can be grown by various methods including thermal oxidation of Cu foils [1], MOCVD [2], or electrochemical deposition [3].It has been shown that Cu_2O-ZnO p–n heterojunctioncan be made by deposition of p-Cu_2O onto n-ZnO using electrochemical deposition [4] or magnetron sputtering [5]. Several Transparent Conducting Oxide/Cu_2O heterojunctions show good photovoltaic results. For example, solar power conversion efficiency of 1.2% was obtained with Al-doped ZnO-Cu_2O [6]; the highest efficiency reported to date was 2% in a sputtered MgF2/ ITO/ZnO/Cu_2O device using MgF_2 as antireflection coating [7]. We report a new approach to make ZnO-Cu_2O heterojunctions. Previously, we demonstrated a novel three-dimensinal (3-D) ZnO photoelectrode consisting of single crystalline ZnO nanotip array integrated with a Ga-doped ZnO (GZO) transparent conducting oxide (TCO) film [8,9]. In the current fabrication process, ZnO nanotips are grown by MOCVD on FTO substrates, then copper is electrochemically deposited on ZnO, and further converted to Cu_2O via a treatment in boiling copper sulfate solution. Through this process, pure Cu_2O phase is obtained, verified by the XRD measurements. Such heterojuction solar cells display a high (>80%) quantum efficiency of photocurrent, 400 mV open circuit voltage and 40 microA/cm^2 short-circuit current. The effects of deposition sequence (ZnO-Cu_2O vs. Cu2O-ZnO) and ZnO morphologies (dense films vs. nanotips) on I-V characteristics of FTO/ZnO-Cu_2O/Au devices will be presented and discussed. 1.N.A. Mohemmed Shanid, M. Abdul Khadar, Thin Solid Films 516 6245–6252 (2008). 2. G. G. Condorelli, G. Malandrino, and I. Fragala, Chem. Mater. 6, 1861 (1994). 3. Y. Tang, Z. Chen et al., Materials Letters 59 (2005). 4. D.K. Zhang, Y.C. Liu, Y.L. Liu, H. Yang, Physica B 351, 178 (2004). 5. K. Akimoto, S. Ishizuka, M. Yanagita, Y. Nawa, G.K. Paul, T. Sakurai, Sol. Energ. 80 715 (2006). 6. H. Tanaka, T. Shimakawaa, T. Miyata, Thin Solid Films 80 469-470, (2004). 7. A. Mittiga, E. Salza, F. Sarto et al., Appl. Phy. Lett. 88, 163502 (2006). 8. A.Du Pasquier, H. Chen and Y. Lu, Appl. Phy. Lett. 89 (1), 253513 (2006). 9. H. Chen, Z. Duan Y. Lu and A. Du Pasquier, J. Electronic Mat. 38, (2009).

9:20 AM Student

DD4, Double Heterojunction Metal-Semiconductor-Metal Photodetector Using ZnO/Si Structure: *Tingfang Yen*[1]; Juhyung Yun[1]; Sung Jin Kim[1]; Alexander Cartwright[1]; Wayne Anderson[1]; [1]SUNY-Buffalo

High photocurrent generation has been obtained by using a ZnO/Si double heterojunction photodetector (DHP) with metal–semiconductor-metal (MSM) structure contact. Two back to back ZnO/Si heterojunctions have been formed with two interdigitated Au/Yb contacts deposited upon ZnO with contact spacing of 2 μm. The I-V curve displayed symmetric MSM characteristics and photocurrent was one magnitude larger for n-ZnO/p-Si and two magnitudes larger for n-ZnO/n- Si than the sum of photocurrent generated from each monolayer of ZnO and Si at 20V. The high sensitivity of photocurrent has been achieved with n-ZnO/n-Si DHP showing photo to dark current ratio of 5053 and responsivity of 3.13 A/W. Two main reasons for this greatly increased photocurrent are discussed. An avalanche multiplication process occurs when applied voltage exceeds flat band voltage. Thus, under illumination, the device acts like an avalanche photodiode with internal photocurrent gain. The avalanche multiplication was obtained by gain versus bias voltage characteristic for different temperatures. Since the thickness of lightly doped ZnO is much less compared to the heavily doped n-Si, higher built-in electric field in the ZnO regions can separate electron-hole pairs and cause a tunneling current. In addition, photoluminescence result shows less defect emission with ZnO/Si structure than ZnO/SiO_2. Thus, the spectral response result was improved because of better quality of ZnO thin film with ZnO/Si structure, the ZnO acting as a passivation layer for the Si, and larger photon absorption provided by ZnO.

9:40 AM Student

DD5, A Study of Indium Doped-ZnO/p-Si(111) Diode Characteristics with Various In Mole Fraction: *Jong Hoon Lee*[1]; Hong Seung Kim[1]; Bo Ra Jang[1]; Ju Young Lee[1]; Nak Won Jang[1]; Bo Hyun Kong[2]; Hyung Koun Cho[2]; Won Jae Lee[3]; [1]Korea Maritime University; [2]Sungkyunkwan University; [3]Dong-eui University

ZnO material is attractive for using optical devices, solar cells, transparent conducting oxide electrodes, and transparent thin film transistors because of its wide band gap (3.37 eV) energy and large exciton binding energy (60 meV). Recently, although the results of p-type ZnO film have been reported, it is still difficulty to growth of reliable p-type ZnO material due to the low solubility of the dopant and the highly self-compensating process upon doing. For these reasons, the p-n junction structure have attempted with other p-type materials such as p-GaN, p-SiC and p-Si. Especially, the p-type silicon substrate has various advantages such as large area substrate, low cost and excellent Si-based technology. An un-doped ZnO material has dominant n-type conductivity at room temperature due to the native defects such as zinc interstitials (Zn_i) and oxygen vacancies (V_o), or present of hydrogen. A study of the ZnO about the carrier concentration is to obtain high carrier concentration (over 10^{20} /cm^3) for substitution of indium tin oxide. The high carrier concentration of n-type ZnO can be obtained as high doping (over 1 at. %) in the ZnO with group III donor impurities such as Ga, Al and In. As the p-n junction diode need to the properties of semi-conductor, we attempted low doping in the ZnO films with indium (0.6, 1, 5, and 10 at. %) for a stable n-type properties on diode characteristics. In this work, our aim is to investigate relationship between changed dido characteristics and effect of In-doping in the ZnO. The In-doped ZnO was deposited by using a pulsed laser deposition system with In-doped ZnO target. The structural characteristics of In-doped ZnO films were investigated by XRD and TEM. The electrical properties of In-doped ZnO films were measured by Hall measurement and the diode characteristics were investigated by current-voltage measurement. The electrical properties of In-doped ZnO films were changed to increase the carrier concentration up to 3.0×10^{19} and to decrease resistivity up to the 1.5×10^{-2} -cm. Also, the diode characteristics were considerably change by the effect of In-doping. Especially, In-doped ZnO/p-Si diodes show very low reverse current density about 2.8×10^{-6} A/cm^2 (In 10 at. %) at -5 V and high on-off ratio (In 10 at. %) about 2.5×10^{-6} at ±5 V. The hetero structure diode exhibited typical current-voltage behaviors with turn-on voltages of 1.8 ~ 4.6 V and with series resistance of 37 ~ 99 Ω. The different diode characteristics may be related on the changed structures of ZnO films by indium doping and we discuss about the relationship between the diode characteristics and the effect of In-doping in the ZnO films. (NIPA-2009-C1090-0903-007 & Human Resource Training Project for Strategic Technology).

10:00 AM Student

DD6, Effects of High - Energy Electron Irradiation on Pd/ZnO/Si MSM Photodetector: Conduction Mechanisms and Radiation Resistance: *Franklin Catalfamo*[1]; Tingfang Yen[1]; Juhyung Yun[1]; Wayne Anderson[1]; [1]University at Buffalo

ZnO/Si metal-semiconductor-metal (MSM) photodetectors with palladium contacts were fabricated and subjected to high-energy electron beam irradiation (HEEBI) in order to observe the effects of space or other high radiation environments on the conduction mechanisms. A medical linear accelerator was used to incrementally irradiate the samples using 12 MeV electrons to a total fluence of $1x10^{13}$ cm^{-2}. Since room temperature annealing of defects in ZnO has been postulated [1-2], current - voltage measurements were performed one day and seven days post irradiation in an attempt to observe this phenomenon. For the highest fluence, $1x10^{13}$ cm^{-2}, the dark and photocurrents were documented at intervals of 3, 12, 26 and 47 days after irradiation. Space charge limited conduction (SCLC) is the dominant current transport mechanism and is attributed to the ZnO layer. I-V plots for the dark current show SCLC in the velocity saturation (ohmic) regime where $J\alpha V$, while plots for photocurrent reveal certain radiation effects on the regime of SCLC observed over a voltage range. Bias of up to 1.0 V resembles the trap-free mobility regime according to the Mott-Gurney law ($J\alpha V^2$) for lower HEEBI fluence. Higher fluence data are closer to the ballistic regime ($J\alpha V^{3/2}$). The 1.0 - 5.5 V bias region shows the mobility regime in the trap-filling transition mode according to the Mark-Helfrich Law ($J\alpha V^{m+1}$). In the bias region 5.5 - 40.0 V, a sub-ohmic I-V behavior is noted where $J\alpha V^{1/2}$. HEEBI fluence of $1x10^{13}$ cm^{-2} minimally increases dark current and decreases photocurrent. These effects are mitigated over time by an apparent room temperature annealing of radiation damage. This too is attributed to the nanocrystalline ZnO layer, thereby demonstrating not only zinc oxide's well-known radiation resistance but also its resiliency to damage incurred. 1. Auret, F.D., et al., *Electrical characterization of 1.8 MeV proton-bombarded ZnO*. Applied Physics Letters, 2001. 79(19): p. 3074-3076. 2. Tuomisto, F., et al., *Introduction and recovery of point defects in electron-irradiated ZnO*. Physical Review B, 2005. 72(8).

10:20 AM Break

10:40 AM
DD7, Late News

11:00 AM
DD8, Late News

11:20 AM
DD9, Late News

11:40 AM
DD10, Late News

Session EE: Epitaxy Materials and Devices

Friday AM
June 25, 2010

Room: 126
Location: University of Notre Dame

Session Chairs: Seth Bank, Univ of Texas, Austin; Archie Holmes, Univ of Virginia

8:20 AM Student

EE1, Overgrowth Investigation of Epitaxial Semimetallic Nanoparticles for Photonic Devices: *Adam Crook*[1]; Hari Nair[1]; Keun Park[1]; Edward Yu[1]; Seth Bank[1]; [1]University of Texas at Austin

Metallic structures with feature sizes small compared to the wavelength of optical radiation have become extremely useful for photonic devices. Surface plasmons have been exploited for various applications including molecular

sensing, light focusing, near-field optical microscopy and enhanced near-field semiconductor absorption. The integration of metallic nanoparticles (e.g. silver, gold, etc.) is currently limited to *ex situ* deposition on the device periphery, as most metal systems cannot be epitaxially integrated into semiconductors. An alternate class of materials, which is compatible with the growth of photonic devices, is required to reach the full potential of nanostructured metallic features. The rare-earth monopnictides are rocksalt semimetals that can be embedded epitaxially into III-V semiconductors. To date, most studies of ErAs nanoparticles have focused on power conversion devices and terahertz emission sources where high optical quality overgrowth in close proximity to the nanoparticles has not been of paramount importance. For monolithic integration with other photonic devices, particularly long-wavelength vertical-cavity surface-emitting lasers (VCSELs), a careful analysis of the overgrowth material must be conducted. GaAs-based tunnel junctions, with ErAs nanoparticles embedded at the p^+/n^+ interface, were grown by solid-source molecular beam epitaxy (MBE) on silicon-doped GaAs (100) substrates. Silicon and beryllium were used as the n-type and p-type dopants, respectively. Surface roughness and local conductivity were measured by atomic force microscopy (AFM) for tunnel junctions of varying p-type capping layer thickness. The RMS surface roughness versus capping layer thickness demonstrated some surface roughening during the initial stages of overgrowth. However, the RMS roughness eventually recovered to ~1 monolayer after sufficiently thick GaAs overgrowth. From the conductive AFM measurements, it was clear that the roughening was not correlated with the location of the ErAs nanoparticles. In addition to surface morphology, the optical quality of the overgrown layers was investigated with photoluminescence (PL). PL structures were grown on semi-insulating GaAs (100) substrates, under conditions nominally identical to those of the tunnel junctions. PL structures with and without ErAs nanoparticles exhibited comparable optical emission from the overgrown $In_{0.1}Ga_{0.9}As$ quantum wells. This demonstrates for the first time that the ErAs nanoparticles can be overgrown with high-quality III-Vs. Epitaxial integration of ErAs nanoparticles compatible with III-V optical devices appears quite promising for incorporation into a number of (nano)photonic devices, including long-wavelength VCSELs where smooth interfaces are critical for the quantum wells, as well as, the distributed Bragg reflector mirrors. In addition. the availability of plasmonic nanomaterials that can be monolithically integrated with III-Vs is exciting for subwavelength photonic devices and circuits for future applications. This work was supported by Dr. Mike Gerhold of ARO and DARPA through a Young Faculty Award.

8:40 AM Student

EE2, Regrown InGaAs Tunnel Junctions for TFETs: *Guangle Zhou*[1]; Haijun Zhu[2]; Paul Pinsukanjana[2]; Yung-Chung Kao[2]; Tom Kosel[1]; Patrick Fay[1]; Mark Wistey[1]; Alan Seabaugh[1]; Huili Xing[1]; [1]University of Notre Dame; [2]IntelliEPI

Interband tunnel field-effect transistors (TFETs) are under development for low-power applications because of their intrinsically low subthreshold swing and low off-state leakage. To maximize lateral tunnel current in planar TFETs, a self-aligned regrown TFET process has been proposed. In this paper, the first regrown vertical InGaAs tunnel junctions are demonstrated using molecular beam epitaxy (MBE) and current-voltage characteristics (I-V) are used to characterize the junctions. CBr_4 and elemental Si were used as the dopant sources in the MBE growth. In the same run two 2 inch n^+ InGaAs wafers were first grown with a Si doping concentration of 1 x 10^{19} cm^{-3}, below its solubility of 6 x 10^{19} cm^{-3}, capped with a 2 nm unintentionally doped (UID) InGaAs layer. After being unloaded from the chambers, one wafer was etched in $1H_2SO_4$-$8H_2O_2$-$160H_2O$ solution for 3 seconds while no pretreatment on the other. This 1:8:160 wet etch was expected to remove 15 nm InGaAs. Both wafers were then co-loaded for regrowth. A 2 nm UID InGaAs layer was first regrown, followed by a 30 nm p^+ InGaAs layer with a C doping concentration of 5 x 10^{19} cm^{-3}, below its solubility of 2 x 10^{20} cm^{-3}. The surface roughness (rms) of the regrown tunnel junctions measured by atomic force microscopy (AFM) is 2.2 nm for the etched wafer and 1.8 nm for the unetched one, respectively, over a scan size of 10 µm x 10 µm. The $In_{0.53}Ga_{0.47}As$ regrown tunnel diodes were fabricated using a self-aligned process to minimize access resistances. A contact resistance of 3.3 x 10^3 •µm^2 was measured. Current-voltage (I-V) characteristics of regrown tunnel junctions on the etched and unetched wafers clearly show negative differential resistance (NDR) under positive bias. On the etched wafer a peak-to-valley ratio of 2.4 and a peak current of 0.14 mA/µm^2 were measured. On the unetched wafer smaller peak-to-valley ratios (1.8) and smaller peak currents (0.074 mA/µm^2) were observed. In addition, we compared the regrown tunnel junctions with an as-grown $In_{0.53}Ga_{0.47}As$ tunnel junction with the same doping profile but a 3 nm UID InGaAs interlayer. With larger peak-to-valley ratio (15), the as-grown tunnel junction, however, shows smaller peak current (0.065 mA/µm^2) than both types of the regrown ones. In conclusion, NDR was observed on the regrown $In_{0.53}Ga_{0.47}As$ tunnel junctions in spite of the defects possibly incorporated at the regrowth interface. Comparison with the as-grown tunnel junctions indicates that the defects at the regrowth interface contribute to the observed higher peak current and lower peak-to-valley ratio in the regrown tunnel junctions. This work is supported by the Nanoelectronics Research Initiative (NRI) through the Midwest Institute for Nanoelectronics Discovery (MIND). The authors are thankful to Dr. Siyuranga Koswatta from IBM for helpful discussions.

9:00 AM Student

EE3, Molecular Beam Epitaxy of Very Thin Fluoride Films on Ge(111) and Its Application to Resonant Tunnelling Diodes: *Keita Takahashi*[1]; Takao Oshita[1]; Kazuo Tsutsui[1]; [1]Tokyo Institute of Technology

The heteroepitaxial structures of fluorides, such as $CaF_2/CdF_2/CaF_2$, grown on Si(111) substrates are promising candidate for producing Si-based resonant tunnelling devices [1][2]. However, strong chemical reaction of CdF_2 with Si substrate is a significant problem in this material system, so that growth temperature is reduced lower than 100ºC and crystalline quality of the epitaxial layers grown at such low temperatures is not good. We propose a Ge buffer layer introduced at the interface between fluorides and Si since Ge is less reactive with CdF_2. As a preliminary study of the idea, we investigated growth of very thin fluoride layers on bulk Ge(111) substrates, and succeeded in fabrication of fluoride resonant tunnelling diodes (RTDs) on the bulk Ge substrates. In experiments, CaF_2, $Ca_{0.42}Sr_{0.58}F_2$ (lattice matched with Ge) or SrF_2 films were grown on heavily doped n-type Ge(111) substrates by using solid source molecular beam epitaxy. The thicknesses of these films were 1.5 nm for AFM and RHEED observations of the grown surfaces and 5 nm for evaluation of *I-V* characteristics on metal-insulator-semiconductor diodes. The two-step growth method in which the fluorides were deposited at room temperature followed by an in situ annealing at 200-500ºC was employed as well as the conventional single step growth at 500ºC. RTDs were fabricated on Ge substrates by using the initial fluoride layer grown under the optimized condition. The various fluoride layers grown by the single step growth method at 500ºC always exhibited island growth. However, island formation was fond to be accommodated relatively for the $Ca_{0.42}Sr_{0.58}F_2$ film. This is probably due to lattice matching effect. Introduction of two-step growth method is strongly effective for improvement of surface condition comparing to the single step method, and annealing at 290ºC provided the best properties in smooth surface and good crystallinity. For the growth of the $Ca_{0.42}Sr_{0.58}F_2$ films grown by the two-step growth method, low leakage current was obtained for the annealing at temperatures lower than 300ºC while leakage current increased at temperatures higher than 350ºC. Therefore, $Ca_{0.42}Sr_{0.58}F_2$ film grown by the two-step growth with annealed at 300ºC was fond to be optimal condition for the initial layer on Ge(111) substrates. RTDs with $Ca_{0.42}Sr_{0.58}F_2$ (3nm) / CdF_2 (3nm) / $Ca_{0.42}Sr_{0.58}F_2$ (3nm) structure were grown at 300ºC on Ge(111), in which the initial $Ca_{0.42}Sr_{0.58}F_2$ layer was grown by the two-step method. The *I-V* characteristics showed obvious negative differential resistance. The successful RTD operation is owing to the good properties of the initial fluoride layer grown on Ge substrates. The successful growth at 300ºC indicates that reduced chemical reactivity of Ge to CdF_2 is effective, and it is significant for high quality growth of fluoride layers for good electrical properties of RTDs.

9:20 AM Student

EE4, Hole Mobility Improvement in Strained InGaSb Quantum Well with Carbon Doping: *Chichih Liao*[1]; K. Y. Cheng[1]; [1]UIUC

The low hole mobility of p-type compound semiconductors prevents the realization of high performance III-V-based field-effect transistor complementary circuits. Recently, it was shown that incorporation of compressive strain in the

channel layer could increase the in-plane two-dimensional hole gas (2DHG) mobility of antimonide-based quantum well (QW) materials [1]. Beryllium (Be) was used as the dopant in previous studies, but Be would easily diffuse out into adjacent layers during the growth process. The channel layer may thus have higher background doping with increased impurity scattering. In this research, we used carbon as the p-type dopant to avoid dopant diffusion. The growth was carried out using gas-source molecular beam epitaxy, and the p-type doping was achieved using a carbon-tetrabromide source via an ultra-high vacuum leak valve. The strained In(x)Ga(1-x)Sb QW structure was metamorphically grown on semi-insulating InP substrates, using Al(x)Ga(1-x)Sb/AlAsSb as the composite barrier layers. High-resolution X-ray diffraction (HRXRD) rocking curve of the as-grown sample showed the AlSb buffer layer was 98% relaxed and the indium composition in the strained In(x)Ga(1-x)Sb QW was 0.3. The corresponding compressive strain in the In(x)Ga(1-x)Sb QW is 1.2%. With optimization of growth conditions and modification of the barrier layer, the room-temperature hole mobility of an In(0.3)Ga(0.7)Sb QW reference structure (without carbon delta-doping) increased from 360 to 600 cm^2/V-s. Compared with pure GaSb QW structure, the hole mobility improvement is about 66% at a similar sheet carrier concentration. Carbon delta-doping was also proved to be effective, which could increase the sheet carrier concentration to 4.1E11/cm^2 with three-second flow of carbon-tetrabromide. The hole mobility decreased to 400 cm^2/V-s with the increasing carrier concentration. The results suggest that the doping concentration of the In(0.3)Ga(0.7)Sb channel can be easily controlled using carbon-tetrabromide as the delta-doping source. References[1] Bennett. B et al. Appl. Phys. Lett. 91, 042104 (2007)

9:40 AM Student

EE5, Growth and Thermal Conductivity of Polycrystalline GaAs Grown on CVD Diamond Using Molecular Beam Epitaxy: *Stephen Clark*[1]; P Ahirwar[1]; F Jaeckel[1]; C Hains[1]; A Albrecht[1]; P Schjetnan[1]; T Rotter[1]; L Dawson[1]; G Balakrishnan[1]; P Hopkins[2]; A Phinney[2]; J Hader[2]; J Moloney[3]; J Moloney; [1]CHTM; [2]Sandia National Laboratories; [3]College of Optical Sciences UA

One of the major challenges for designing heat sinks for very high-power semiconductor devices is the necessity to be in a direct physical contact with the heat source. The best heat conductor is diamond which can be manufactured in single-crystal form and in a polycrystalline form using chemical vapor deposition, with the former form being significantly more complex to realize than the latter. A simple yet extensively used configuration for thermal management in high power III-V devices consists of a diamond heat spreader mounted on a conventional copper heat sink that is subsequently cooled by chilled water or glycol. For optimal heat transfer however, it is desired to have the surface of a single-crystal diamond, polished to sub-nanometer RMS roughness, put into direct contact with the heat source thus spreading the heat from the concentrated region in the III-V to the diamond spreader. Attempts have been made to introduce either a capillary fluid (water or ethanol) or Indium alloy solder to bond the diamond to the heat source. In principle, this approach would work if the surface of the diamond were perfectly flat. However, the rough surface of the polycrystalline diamond prevents efficient wetting for either fluid or solder. Thus the currently used techniques do not fully exploit the heat-spreading capability of diamond and a better approach to bonding the III-V device to diamond is required. In the presentation made we shall discuss the use of poly-GaAs on CVD diamond as a wafer-bonding alternative to Indium solder and capillary bonding. In this paper we present the growth and characterization of polycrystalline GaAs thin-films on polycrystalline Chemical Vapor Deposition (CVD) diamond by Low-Temperature Molecular Beam Epitaxy (LT-MBE). The LT-GaAs adheres very strongly to the CVD diamond layer and can easily be polished down to an RMS surface roughness of 1 to 5 nm. This polished surface represents more than an order of magnitude in surface roughness reduction when compared to a CVD Diamond surface. This makes the polished LT-GaAs on diamond layer an ideal wafer-bonding interface for high-power semiconductor devices. The samples were grown at 0.2 µm/hr with a substrate temperature of 250ºC and a 1:8 III/V beam flux ratio. The samples were analyzed by in-situ reflective high-energy electron diffraction (RHEED) during MBE growth, X-Ray diffraction, and atomic force microscopy for surface roughness. We also measured the thermal conductivity of the GaAs layer on CVD diamond using pump-probe time domain thermoreflectance.

10:00 AM Break

10:20 AM

EE6, Thick HVPE Growth of Patterned Semiconductors for Nonlinear Optics: *Candace Lynch*[1]; David Bliss[1]; Vladimir Tassev[1]; George Bryant[1]; Cal Yapp[2]; [1]AFRL; [2]Solid State Scientific Corp.

There is a growing need within the Department of Defense for compact and efficient sources of coherent radiation operating in the mid-IR and terahertz. One approach involves frequency conversion in quasi-phase-matched (QPM) nonlinear optical materials such as GaAs and GaP. QPM in these materials is achieved by periodically inverting the crystallographic lattice orientation to yield a grating in which the sign of the nonlinear coefficient is modulated. The QPM structure is created using thick epitaxial growth on a patterned template – replication of the template produces a grating with periodic antiphase domains. However, fabrication of these structures presents three challenges – first, the final crystal must be on the order of a millimeter thick (or greater) to accommodate the pump and signal beams as they propagate across the structure. Second, the crystal must be grown with a periodic array of crystallographic inversion domains with widths as small as 15 microns (for conversion from 2 microns to mid-IR) and as large as a millimeter (for conversion to THz). Finally, the defects must be controlled to minimize optical loss mechanisms. Growth of very thick layers on the templates is especially challenging due to the need to maintain vertical propagation of the antiphase domain walls, which are initially aligned along {110} planes. When the domain walls stray from the {110} planes, the patterned structure loses coherency, decreasing the efficiency of the nonlinear interaction. Measurements indicated that the domain wall bending decreased as the growth temperature was reduced. The substrate miscut and the template design also affect the vertical propagation of domain walls. We will describe the use of low-pressure Hydride Vapor Phase Epitaxy (HVPE) to grow crystals of QPM GaAs, achieving GaAs growth rates in excess of 200 microns/hr and producing epitaxial GaAs layers of up to 1.2 mm in thickness. Utilizing templates produced by MBE GaAs/Ge/GaAs epitaxy or by wafer bonding, we have produced mm-thick QPM-GaAs with domain walls that extend through the thickness of the layer. Such materials have successfully been used to generate IR and THz radiation.

10:40 AM Student

EE7, Effects of Carrier Localization on Emission Spectra of Dilute GaAsN Materials Doped with Silicon: *Yan He*[1]; A.M. Mintairov[1]; J.L. Merz[1]; Y. Jin[2]; R.S. Goldman[2]; I. Akimov[3]; T. Goedde[3]; D. Yakovlev[3]; [1]University of Notre Dame; [2]University of Michigan; [3]Technical University of Dortmund

The dilute nitrides (i.e., GaAs containing small amounts of nitrogen) continue to be a topic of great technological interest because of the rapid decrease of the GaAs bandgap with only a few percent of nitrogen. It was shown using high-spatial-resolution photoluminescence (HSR PL) spectroscopy that these materials often contain quantum-dot-like compositional fluctuations arising from nitrogen phase separation effects.[1, 2] Here we study the effect of silicon doping on the formation of such compositional fluctuations in $GaAs_{1-x}N_x$ using conventional HSR and time-resolved PL. For these studies, undoped and Si-doped GaAsN films with free carrier concentrations of 1.4E15 cm-3, 3E16 cm-3, 6.27E16 cm-3 and 5.82E17 cm-3 were grown by rf plasma-assisted molecular beam epitaxy, and subsequently rapid thermal annealed.[3] At T ~ 10K, we observe a strong decrease of emission intensity and a definite red shift of the PL peak position in the Si-doped GaAsN films. We also observe some increase of luminescence intensity with the increase of doping level. In Si-doped GaAsN films, we do not observe sharp emission lines related to quantum dots (QDs) using HSR PL measurements. Time-resolved PL experiments reveal a nearly two times shorter emission decay times in Si-doped GaAsN film. We suppose that most of the observations can be explained assuming local modulation-doping, which leads to activation of deep band-tail states in emission spectra. The nature of these states might correlate with the formation of NN pairs.[4-6] We believe these optical results reveal new structural properties in Si-doped dilute nitride GaAs alloys. This work has been supported under NSF/DMR06-06406. References: [1]A. M. Mintairov, T. H. Kosel, K. Sun, V. Ustinov and J. L. Merz. *MRS Mater. Res. Soc. Symp. Proc. 838E (2005) O3.* [2]A.M. Mintairov, K.Sun, J.L. Merz,

H. Yuen, S. Bank, M. Wistey, J.S. Harris, G. Peake, A. Egorov, V. Ustinov, R. Kudrawiec, and J. Misiewicz. *Semicond. Sci. Technol. 24, 075013 (2009).* [3]Y. Jin, Y. He, H. Cheng, R.M. Jock, T. Dannecker, M. Reason, A.M. Mintairov, C. Kurdak, J.L. Merz, and R.S. Goldman. *Appl. Phys. Lett. 95, 092109 (2009).* [4]D.G. Thomas, J.J. Hopfield, and C.J. Frosch. *Phys. Rev. Lett. 15, 857 (1965).* [5]S. Fahy, A. Lindsay, H. Ouerdane, and E. P. O'Reilly. *Phys. Rev. B 74, 035203 (2006).* [6]L. Bellaiche and A. Zunger. *Phys. Rev. B 57, 4425 (1998).*

11:00 AM Student

EE8, Fabrication and Characterization of Free-Standing InGaAs/GaAs Quantum Dot Microbelt-like Optical Resonators: *Feng Li*[1]; Zetian Mi[1]; [1]McGill University

Recently, semiconductor tubes, formed when a coherently strained semiconductor heterostructure is selectively released from the host substrate, have emerged as a promising technique to realize a new class of nanophotonic devices. They offer many distinct characteristics for laser operation, including ultrahigh Q-factors, directional emission, and well-defined polarization. To achieve an exact tailoring of the 3-dimensionally confined optical modes, we have investigated the fabrication and emission characteristics of optical microcavities formed by such semiconductor tubes using a belt-like geometry at the inner surface, wherein self-organized InGaAs/GaAs quantum dots are incorporated as the gain media. We have measured sharp, polarized optical resonance modes in such microbelt-like tube resonators, with emission wavelengths in the range of 1.1 – 1.3 μm and Q-factors varying from 1,000 to ~ 3,000. The InGaAs/GaAs quantum dot heterostructure was grown on a 50nm AlAs sacrificial layer on GaAs substrate. Semiconductor tubes were formed when the AlAs layer was selectively etched, due to the relaxation of strain. To achieve free-standing tube structures, a U-shaped mesa, with a deeply etched region between its two side pieces, was first defined. Subsequently, a ridge waveguide was introduced by performing a very shallow (~ 5 nm) etch on the mesa. The widths and lengths of the waveguide vary from 1 – 5 μm and from 15 – 30 μm, respectively. The formation of the semiconductor tube creates a belt-like geometry at the tube inner surface, thereby leading to the unique microbelt-like optical resonator with the confined optical modes precisely controlled by the belt width, height, and length. In this experiment, the tube diameter is ~5 μm and the wall thicknesses vary from 50 to 250 nm. Optical properties of the InGaAs/GaAs quantum dot microbelt-like optical resonators were studied using micro-photoluminescence spectroscopy. The emission spectrum of a microbelt device consists of several groups of sharp optical resonance modes, with the dominant mode in each group primarily determined by the azimuthal confinement around the tube circumference. Other optical modes within each azimuthal group, however, are directly related to the optical confinement by the belt along the tube axial direction. The optical resonance modes can be exactly tailored by varying the belt width and thickness. With a belt width of ~ 1.5 μm and tube wall thickness of ~ 100 nm, only the fundamental axial mode can be observed, which exhibit a spectral linewidth of ~ 0.7 nm and a Q-factor of ~ 2,000. Emission characteristics of micro-belt tube resonators with various belt widths, tube diameters and wall thicknesses are being investigated. These results, in conjunction with the achievement of microbelt lasers and laser arrays will be presented.

11:20 AM

EE9, MBE Grown InGaAsSbN/GaSb Single Quantum Wells for Mid-Infrared Applications: *Sudhakar Bharatan*[1]; Shanthi Iyer[1]; Jia Li[1]; Thomas Rawdanowicz[2]; [1]North Carolina A&T State University; [2]North Carolina State University

In this paper we will present comprehensive study of growth and characterization of InGaAsSbN quantum well (QW) heterostructures grown on GaSb by solid source molecular beam epitaxy, using valved antimony and arsenic source and RF plasma N source for potential light-emitting devices in the mid-infrared region. A systematic study of correlating the growth conditions and effect of N incorporation on the emission, crystalline, microstructure and vibrational characteristics of the strained single QW structure, using variety of characterization techniques will be presented. 10 K PL emission at 2.28 μm, with a lowest full width at half maxima (FWHM) of 5 meV which shifted to 2.30 μm on in-situ annealing has been observed. Raman spectroscopy studies in InGaAsSb QWs indicate the presence of Sb antisite defects in these layers, as evidenced by the dominant elemental A_{1g} Sb mode. However, in InGaAsSbN QWs Sb antisites are suppressed, with the preferential formation of Sb-N defects, along with the appearance of intense 2nd order GaSb and GaN modes. The high quality of these nitride QW layers were further attested to by the presence of well resolved Pendellosung fringes on high resolution x-ray diffraction (HRXRD) and sharp, abrupt interfaces on the corresponding TEM images. This work is supported by the Army Research Office (Grant No. W911NF-07-1-0577).

11:40 AM

EE10, Late News

Session FF: Si and Ge Nanowires

Friday AM
June 25, 2010

Room: 129
Location: University of Notre Dame

Session Chairs: Diana Huffaker, University of California, Los Angeles; Chen Yang, Purdue University

8:20 AM Student

FF1, The Influence of the Catalyst on Dopant Incorporation during Si and Ge Nanowire Growth: *Justin Connell*[1]; Eric Hemesath[1]; Daniel Perea[2]; Zakaria Al Balushi[3]; Kwon Nam Sohn[1]; Jiaxing Huang[1]; Lincoln Lauhon[1]; [1]Northwestern University; [2]Los Alamos National Laboratory; [3]Pennsylvania State University

Silicon and germanium nanowires (Si and GeNWs) are promising materials for electronic applications due to their high aspect ratio and the ability to incorporate dopant molecules in-situ during growth. Unfortunately, the frequently employed gold catalyst used in vapor-liquid-solid (VLS) growth of Si and GeNWs exhibits a high solubility for dopants such as boron and phosphorous[1] - a property that leads to diffuse interfaces when attempting to grow *p-n* junctions. We have explored the abruptness of dopant homojunctions in VLS grown nanowires using atom probe tomography to correlate fundamental thermodynamic parameters with junction abruptness. Growth from alloy nanoparticles has also been explored as a potential means to rationally control dopant solubility, and hence junction abruptness, during growth. We previously demonstrated that local electrode atom probe (LEAP) tomography can be used to precisely map the three-dimensional positions and chemical identities of the atoms in a nanowire sample with sub-nm spatial resolution[1]. Si and GeNWs were grown using a hot-walled CVD reactor, with silane and germane as the semiconductor precursor sources, and p- and n-type growth was performed using diborane and phosphine, respectively. During growth, the dopant gas flows were removed, and growth was continued in order to fully deplete the catalyst of the retained dopant species. By measuring the decay in dopant concentration along the length of the nanowire using LEAP tomography, we are able to determine the dopant solubilities in Au during growth, as well as the segregation coefficients. Core-shell Au-Cu_2O nanoparticle catalysts have also been synthesized for use as alloy seeds for NW growth. Upon annealing at 450ºC, these particles form an Au-Cu alloy, with the alloy composition determined by the thickness of the Cu_2O shell. GeNW growth with these particles was performed at 320ºC, which is well below the Au-Ge and the Cu-Ge eutectic temperatures, suggesting growth proceeds via the vapor-solid-solid (VSS) mechanism. We anticipate that dopant solubility in a solid catalyst will be markedly lower than that of a liquid catalyst, which may enable the growth of atomically abrupt *p-n* homojunction NWs.

8:40 AM

FF2, Size Effects in Semiconductor Nanowire Synthesis at the Ultimate Limit: *Shadi Dayeh*[1]; Eli Sutter[2]; Peter Sutter[2]; S. T. Picraux[1]; [1]Los Alamos National Laboratory; [2]Brookhaven National Laboratory

Progress in the synthesis of semiconductor nanowires has prompted intensive discussions of the science of their growth and the technological applications they promise. While for many applications, nanowires with bulk-like electronic properties are sufficient, devices with novel functionality, such as single

electron logic, or solar cells utilizing exciton multiplication, ultimately require harnessing the quantum confinement effects that arise in ultrathin nanowires with diameters below 10 nm. At this scale, the processes involved in the widely used vapor liquid solid (VLS) technique for nanowire growth remain poorly understood. Also a minimum size below which the VLS process can no longer be used for nanowire synthesis is anticipated based on thermodynamic considerations. Here we exploit an extreme level of diameter and placement control in the VLS synthesis of germanium nanowires to establish systematic size effects at small diameters and the ultimate nanowire diameters achievable in VLS growth. Our experiments demonstrate a decrease in the nanowire growth rate at lower diameters, and a concomitant increase in the equilibrium Ge concentration of the liquid Au-Ge drop mediating VLS nanowire growth. Both effects are described quantitatively by an analytical model, based on the Gibbs-Thomson effect. Combining experimental data and this model, we establish the minimum nanowire diameter, and its dependence on growth parameters such as temperature and the addition of dopants. Our results provide a rational basis for the synthesis of semiconductor nanowires at the ultimate size limit.

9:00 AM Student

FF3, Growth and Applications of Silicon/Germanium Axial Nanowire Heterostructures: *Cheng-Yen Wen*[1]; Mark Reuter[2]; John Bruley[2]; Jerry Tersoff[2]; Suneel Kodambaka[3]; Eric Stach[1]; Frances Ross[2]; [1]Purdue University; [2]IBM; [3]University of California, Los Angeles

Silicon and germanium heterojunction nanowires are required for device applications that require tailoring of both band-gap and carrier confinement near the interface. For better device performance, interfacial defects due to large lattice mismatch should be avoided. Similarly, abrupt composition changes at the junction interface are also crucial. It has been shown that dislocation-free interfaces between two materials with a large lattice mismatch can be fabricated in nanowire structures, because the coherent lattice strain near the interface is easily relaxed. Similar results have been demonstrated in Si/Ge heterojunction nanowires using the vapor-liquid-solid (VLS) growth method; however, the resulting composition change at the interface junction is not sharp, due to a reservoir effect in the liquid catalyst: the commonly used liquid AuSi eutectic catalyst for the VLS growth method contains 20% Si. When switching the growth precursors from Si to Ge, Si can not be immediately depleted from the liquid catalyst, and, as a result, there is a gradual composition change at the interface. We show that the use of solid catalysts and the vapor-solid-solid (VSS) method can overcome this problem. We chose $AlAu_2$ alloy as the catalyst, because this compound has a higher eutectic temperature with Si or Ge than pure Au (this allows us to operate with the VSS growth with a reasonable growth rate), and it shows strong catalytic activity. Another benefit is that the medium eutectic temperature of $AlAu_2$ with Si allows us to switch the growth mode between VLS and VSS. We first grow nanowires in the VLS mode, in order to have a fast growth rate, and then cool the sample to solidify the catalyst. The heterojunction is grown by modulating the gas precursors in the VSS mode. Nearly atomically abrupt interfaces in Si/Ge nanowire junction structures can be fabricated using this approach. We can not measure the actual solubility of Si or Ge in the catalyst, but, from in-situ TEM measurements of the step flow kinetics at the interface, we find evidence that supports our assumption of low Si solubility in the catalyst. Theoretical predictions show that Si nanowires containing a thin Ge layer have different electronic properties. To further understand the properties of such structures for applications in band-gap engineering, we use the VSS technique to fabricate ultra-thin Ge layers in Si nanowires and study lattice strain near the interface using lattice images and geometrical phase analysis. Here, we first describe the growth of the Si/Ge nanowire heterostructures using in-situ transmission electron microscopy and show the abruptness and interface perfection using analytical microscopy and lattice images. We will discuss practical considerations of applying this growth method and analyze the strain field of the small Ge quantum dot structure in Si nanowires.

9:20 AM Student

FF4, SiGe/Si Selective Etch Structures for Nanowire Release and Assembly: *Sharis Minassian*[1]; Xiahua Zhong[2]; Xiaojun Weng[3]; Theresa Mayer[2]; Joan Redwing[4]; [1]Department of Chemical Engineering; [2]Department of Electrical Engineering; [3]Materials Research Institute; [4]Department of Chemical Engineering, Department of Materials Science and Engineering, Materials Research Institute, The Pennsylvaina State University

Producing monodisperse silicon nanowires (SiNWs) with uniform length has been a critical difficulty in the bottom-up assembly of nanowire devices. SiNWs grown by the vapor-liquid-solid (VLS) method attach firmly to the growth substrate, making it difficult to remove them for single nanowire device assembly. Ultra-sonic agitation is frequently used to break the wires off of the substrate; however, they break at differing lengths, degrading the yield of successful wire integration and device fabrication. To achieve uniform nanowire lengths, we have investigated the use of SiGe/Si axial-heterostructure nanowire and selective etching to remove the SiGe segment and release the SiNW segment. Preferential etching of $Si_{1-x}Ge_x$ alloys over pure Si can be obtained by using hydrogen peroxide solution when x>65%.[1] To attain Ge-rich SiGe nanowire segment at temperatures above 400ºC, which is more compatible with SiNW growth conditions, disilane (1% in H_2) and germane (2% in H_2) gases were chosen as Si and Ge sources. As opposed to silane which results in Si-rich SiGe nanowires at T>400ºC,[2] disilane enabled the growth of SiGe nanowires with a broader composition range of Ge at higher temperatures. The heterostructure nanowires were grown in a hot wall LPCVD reactor at 425ºC and 13Torr. Oxidized silicon wafers coated with 3nm Au thin film were used as substrates. A 5mm long segment of $Si_{1-x}Ge_x$ was initially grown followed by a Si segment approximately 1µm in length.

Both straight and kinked heterostructure nanowires were observed. The SiGe segments were generally tapered (~40-80nm/µm for 5 nanowires measured), but the tapering was negligible for Si segments with diameters of 51±15nm. TEM analysis showed that in a straight wire both segments were grown along [211] direction. In a kinked nanowire, the SiGe segment grew in the [111] direction, but the growth direction changed to [110] in the Si segment. The composition of the SiGe from XEDS analysis was estimated to be (85.1±0.8)at% Ge, which is in the range of interest for the selective etching process. The etching effect of H_2O_2 (30% solution for 30 minutes) was explored on SiGe and Si nanowires grown separately at similar conditions to that of heterostructure nanowires, and it was confirmed that the solution rapidly etches the SiGe nanowires but does not affect the SiNWs. The process was performed on SiGe-Si heterostructure nanowires; the as-grown SiGe segment was etched away from the substrate releasing the SiNWs off of it. The length of the released wires was measured to be 980±178nm, which is in agreement with our expectation. The impact of selective etching on the alignment yield of nanowires will also be discussed. [1] M. Stoffel et al., Semicond. Sci. Technol., 23, 085021, (2008). [2] K.K. Lew et al., J. Mater. Res., 21, 2876, (2006).

9:40 AM

FF5, Diffusion Formation of Nickel Silicides Contacts in Silicon Nanowires: Yuval Yaish[1]; *Michael Beregovsky*[1]; Alexander Katsman[2]; [1]Electrical Engineering, Technion; [2]Materials Engineering, Technion

Silicon nanowires (SiNWs) field effect transistors (FETs) with a surrounding gate may enable further scaling of CMOS devices due to their thin body and cylindrical geometry. Of fundamental importance is the method in which contacts to the nanowire channel are being formed. One promising method utilizes thermally activated axial intrusion of nickel silicides into the SiNW from pre-patterned Ni reservoirs located at both ends of the wires. Such intrusion of Ni-silicide involves different thermally activated processes such as volume, surface and interface diffusion of Ni, each being characterized by a certain time, temperature and SiNW diameter dependencies. Up to date a comprehensive understanding of these processes is still missing. In the present work these dependencies were investigated during axial growth of nickel silicide in SiNWs for a temperature range of 300-440°C and wire diameters of 30-60nm. Nickel electrodes were deposited on randomly dispersed SiNWs followed by rapid thermal annealing processes at different temperatures and for different times. Silicide intrusions were investigated by atomic force microscopy and scanning

electron microscopy. The following results were analyzed in the framework of diffusion phase formation model that we have published recently. The main part of the intrusion consists of monosilicide NiSi, as was confirmed by measuring the electrical resistance of the wire after full silicidation. Nickel silicide intrusion length, L, showed a typical diffusion dependence on the annealing time, t, and temperature, T: $L = kt^{1/2}\exp(-Q/2k_BT)$, where Q is the diffusion activation energy, and k is proportionality coefficient depending on the wire diameter. We have studied the dependence of k on the wire diameter, and the activation energy for the growth was found to be ~1.7 eV which is typical for nickel interface diffusion processes in nickel silicides. It was concluded that the growth of nickel silicide intrusion is controlled by surface diffusion of nickel along the outer surface of the silicide formed and not by nickel diffusion through the silicide bulk.

10:00 AM Break

10:20 AM Student

FF6, Comparative Study of Ni-Silicide and Germanide Formation in Contacts to Si and Ge Nanowires: *Nicholas Dellas*[1]; Sharis Minassian[1]; Joan Redwing[1]; Suzanne Mohney[1]; [1]Pennsylvania State University

Previous studies have shown that Ni-silicide phase formation in Ni contacts to SiNWs can differ from the phase formation sequence observed for thin Ni films on Si wafers. In the well-studied case of a thin film on a Si wafer, one often observes sequential phase formation beginning with orthorhombic Ni_2Si, followed by NiSi upon increased time and temperature, and finally nucleation of $NiSi_2$ at temperatures in excess of 700°C. This sequential formation is not what has been observed in previous reports of Ni-silicidation of SiNWs. We have found that the phase formed is dependent on the growth direction of the SiNW. In the case of SiNWs with a [112] growth direction, a metastable high-temperature phase, hexagonal θ-Ni_2Si, is formed and stabilized when annealed from 350 to 700°C for 2 min. We also observe that the Ni-silicide has an epitaxial orientation with respect to the SiNW of θ-$Ni_2Si[001]||[11\text{-}1]$ and θ-$Ni_2Si(100)||Si(112)$. The second case is that of SiNWs with a [111] growth direction. We find $NiSi_2$ is the first phase to form after anneals of 350, 400, 450 and 550°C for 2 min, and it also forms with an epitaxial relationship to the SiNW: $NiSi_2[1\text{-}10]||Si[1\text{-}10]$ and $NiSi2(111)||Si(111)$. After anneals of 600 and 700°C for 2 min, a conversion from $NiSi_2$ to NiSi is observed.We have performed similar experiments, substituting GeNWs for the SiNWs and studying the solid state reaction between a Ni film and a GeNW to form Ni-germanides. We find that the reaction begins axially down the GeNW at a temperature of 350°C, and the phase that forms has a similar crystal structure to the hexagonal θ-Ni_2Si phase identified to form in the reaction of Ni with SiNWs with a [112] growth direction. From indexing the diffraction patterns, the Ni-germanide phase could be either Ni_2Ge or Ni_3Ge_2; however, these two phases cannot easily be differentiated because the space groups for the two crystal structures are identical, the only difference being the occupancy of sites by Ni or Ge atoms resulting in different stoichiometries. After annealing at 400°C for 2 min, the same hexagonal Ni-germanide phase is identified, with the exception that in some cases a thin layer (10 nm) of orthorhombic NiGe is formed at the reaction front between the hexagonal Ni-germanide and GeNW. Higher temperature annealing at 500°C results in a break in the GeNW away from the germanide/Ge interface. Further work is underway to determine if Ni-germanide formation in GeNWs has a dependence on the growth direction of the GeNWs, as was previously observed for the Ni/SiNW system.

10:40 AM Student

FF7, High Responsivity Vertical Si Nanowire Photodetector Arrays: *Yi Jing*[1]; Cesare Soci[1]; Ke Sun[1]; Matt Chandrangsu[1]; Atsushi Ohoka[1]; Deli Wang[1]; [1]University of California, San Diego

Semiconductor nanowire photodetectors have attracted extensive interest for applications in sensing, imaging and optical interconnects. It has been demonstrated that nanowire photodetectors have high photoconductive gain ($>10^8$) attributing to the deep level surface trap states and reduced dimensionality. While planar nanowire photodetector arrays exhibit significantly higher sensitivity than their bulk counterparts, vertically aligned nanowire arrays can further enhance the light absorption due to the waveguiding effect caused by the refractive index difference between vertical nanowires and surrounding materials, which increases effective coupling efficiency. In this study, a vertical Si nanowire photodetector array with individually addressability was investigated and its optical characteristics were characterized. P-type (100) silicon-on-insulator (SOI) wafers with device layer thickness of 5μm and doping of ~10^{15} cm^{-3} were used in this research. E-beam lithography and a combination of Inductively Coupled Plasma (ICP) and Reactive Ion Etch (RIE) process were carried out to anisotropically etch an 8×8 vertical Si nanowire array with 4μm pitch size. The vertical photodetector devices were created by embedding the nanowires in spin-on glass and depositing the electrodes. Using crossbar structure, the photodetector array can be individually addressed. The photoresponse of each individual device were measured under uniform white light illumination to demonstrate the feasibility of this array as image sensor. The results show 100% yield functional devices and the photodetectors exhibit a high photo responsivity of greater than 550A/W at room temperature. The high responsivity mainly arises from two factors: (1) the enhancement of the carrier lifetime caused by the trapping of carriers in the surface states; (2) decrease of the carrier transit time due to small dimension of nanowire devices. Thus, a small pixel size Si nanowre image senor with high responsivity was demonstrated. The pixel size can be further scaled down by decreasing the nanowire spacing and this result can be expanded to large scale, high resolution image sensor device by nanoimprint lithography.

11:00 AM

FF8, Si Nanowire Mats for Large-Area Electronics: *William Wong*[1]; Sourobh Raychaudhuri[1]; Sanjiv Sambandan[1]; Rene Lujan[1]; Robert Street[1]; [1]Palo Alto Research Center

Silicon nanowires (Si NWs) have the potential to enhance conventional thin-film transistor (TFT) device structures that will enable high-performance devices in a wide variety of large-area electronics applications. The nanowires also provide greater options for device integration ranging from direct growth to jet-printed suspensions in a liquid. These aspects can greatly reduce fabrication complexities and increase functionality for novel large-area flexible electronics. One simple approach to device fabrication is the use of Si NW mats that replace the semiconducting thin-film layer in a TFT device. This structure can offer increase device performance compared to conventional disordered thin-film semiconductors while providing increased mechanical flexibility. In order to better understand the boundaries and limits for such devices, we have fabricated and tested Si NW field-effect transistors (FETs) using nanowire mats in place of conventional amorphous silicon films. Bottom- and top-gate FETs were fabricated using a mechanical transfer technique. Silicon nanowires were first grown from a gold seed layer by the vapor-liquid-solid process using chemical-vapor deposition onto silicon substrates. The undoped silicon nanowires were then transferred using a sliding contact method to assemble the nanowires from the growth substrate onto the device wafer. Conventional thin-film processing techniques were then used to fabricate devices with different contact metals and encapsulation materials. Bottom gate p-channel and n-channel FETs were fabricated using Ti/Au and TiW contact metals, respectively. The as-fabricated p-channel (n-channel) devices (having a thermal SiO^2 gate dielectric) showed threshold voltages of -10V (+12V), field-effect mobility of 12cm^2/Vs (15 cm^2/Vs), and on-off ratios of 10^4. Top-gate FETs, having plasma-enhanced chemical-vapor deposited SiO_2 gate dielectric layers, were used to create "wrap-around" NW-FETs. These devices were found to have improved on-off ratios of 10^5 and higher field-effect mobility (~ 100 cm^2/Vs) compared to the bottom gate devices. The NW mats were also used to fabricate a 180×160 pixel FET backplane array. Each pixel was 300 microns square with a 300 micron pitch and the resulting fabricated array showed high yield when scanned and measured by capacitive-charge mapping. We will also discuss the effect of different passivation layers on device performance and stability and how these characteristics are implemented in the fabrication of the backplane array for a reflective display.

11:20 AM
FF9, Jet-Printed and Dielectrophoretically Aligned Nanowires for Large Area Electronics: *Sourobh Raychaudhuri*[1]; William Wong[1]; Sanjiv Sambandan[1]; Rene Lujan[1]; Robert Street[1]; [1]Palo Alto Research Center

The ability to integrate Si nanowires (Si NW) on plastic substrates may greatly enhance the performance of low cost flexible electronics. Si nanowire properties can be controlled during growth and leveraged to produce nanowires which are tailored for specific applications. Being able to then harvest these wires and distribute them across a large area substrate in a controlled manner opens up many opportunities for high performance large area and flexible electronics. In this talk we report on Si NW field effect transistors (FETs) fabricated using ink-jet printing as a means to distribute Si NW mats at specified locations across a donor substrate. The Si nanowires were first grown on a Si substrate. The growths were carried out in a chemical vapor deposition system using the vapor-liquid-solid growth process with either Au nanoparticles or an Au thin film to seed the growths. The nanowires were removed from the growth substrate and suspended in water. The nanowire suspension was then loaded into a commercially available ink jet printer and printed onto device substrates. As a means to control the position and orientation of the printed nanowires, an AC electric field was applied across predefined electrodes on the device substrate. This approach to assembling printed nanowires resulted in well-aligned nanowires along the channel region of the FET having channel lengths between 3 to 13 microns and channel widths of 2 to 8 microns. The printed nanowires were then processed into top-gate and bottom-gate transistors using conventional lithographic techniques. The p-type devices showed threshold voltages of around -5 volts, hole mobilities greater than 10 cm^2/V/s and on-off ratios greater than 10^5. We will also discuss several aspects of printing necessary for good device yields and the effect of varying AC electric fields on the printing and assembly process. Finally we will discuss how to make use of these techniques in a scalable way and demonstrate how they can be used to fabricate a TFT backplane that is sufficient to drive reflective display media.

11:40 AM
FF10, Late News

Session GG: Thermoelectrics and Thermionics

Friday AM
June 25, 2010

Room: 131
Location: University of Notre Dame

Session Chairs: Joshua Zide, Univ of Delaware; Peter Moran, Michigan Technological Univ

8:20 AM Student
GG1, Bulk-like Thermionic Energy Conversion Device Fabricated from Laminated Nanostructured Metal/Semiconductor Superlattices: *Jeremy Schroeder*[1]; David Ewoldt[1]; Polina Burmistrova[1]; Robert Wortman[1]; Timothy Sands[1]; [1]Purdue University

Thermionic carrier transport in metal/semiconductor superlattices is a promising energy conversion approach based on nanocomposite materials. Current research focuses on thin-film sputter deposited transition metal nitride superlattices for improving ZT via energy barrier filtering (increased power factor) and interface scattering of phonons (suppressed thermal conductivity). However, even if these superlattices prove successful in enhancing ZT, barriers exist between research-based thin-film superlattices and practical bulk-like device structures. For example, optimal power density in thin-film thermoelectric devices requires superlattice leg lengths in the range of 50-200µm. Such leg lengths are impractical for sputtered deposited films due to lengthy deposition times, high residual growth stress, and varying crystal quality. One approach to realizing long leg lengths is through laminating multiple thin-film superlattices to create bulk-like structures. Effective laminate structures require negligible parasitics be introduced by the bonding layers. Simple analysis shows that the electrical and thermal parasitics are less than 10% when using a bonding medium of high thermal and electrical conductivity, such as copper or gold, and assuming a low contact resistance (~$1\times10^{-8}\Omega$-cm^2) between the bonding medium and superlattice. The metal/semiconductor superlattice structure offers the benefit of a metal-metal contact between the bonding medium and metal nitride, which should offer low contact resistance. Five micrometer ($Hf_{0.5}$, $Zr_{0.5}$)N/ScN superlattices with 12nm period were deposited on 2" 100-silicon substrates by reactive DC magnetron sputtering. One micrometer of gold was deposited on the superlattices followed by Au-Au thermocompression bonding of two 2" superlattices, thereby creating a bilayer structure. The structure was diced into 5mm x 5mm pieces followed by selective etching of the silicon substrates in tetramethyl ammonium hydroxide (TMAH) with the HfN buffer layer acting as an effective TMAH etch stop. The resulting 12µm superlattice bilayer foils were stress balanced with respect to the Au-Au bond interface and they were robust enough to be handled with vacuum tweezers. One micrometer of gold was then deposited on both sides of the superlattice bilayer foils followed by stacking and Au-Au thermocompression bonding of twenty bilayer foils (although the number of stacked bilayers is practically unlimited). The final 290µm thick laminate structure was an artificial bulk-like structure fabricated from 200µm of nanostructured superlattice films and 90µm of gold bonding medium. The 5mm x 5mm laminate was subsequently diced and polished into 300µm x 300µm x 290µm devices for electrical and thermal characterization. These laminate devices demonstrate a route forward towards realizing practical thermoelectric devices based on nitride metal/semiconductor superlattices.

8:40 AM Student
GG2, Epitaxial Growth of Transition Metal Nitrides on MgO via DC Magnetron Sputtering: *Robert Wortman*[1]; Jeremy Schroeder[1]; Polina Burmistrova[1]; Laura Cassels[2]; Joshua Zide[2]; Timothy Sands[1]; [1]Purdue University; [2]University of Delaware

The transition metal nitrides are an important group of materials due to their high melting temperature and hardness. These qualities make them ideal for wear and cutting surfaces. Furthermore, the group IIIa-nitrides have recently gained interest as semiconductors, specifically scandium nitride and its alloys. Scandium nitride is an indirect gap semiconductor with a bandgap of ~0.9 eV. Scandium nitride has been shown to be of interest in thermoelectric devices[1] as well as in optoelectronic and other device applications[2] in pure and alloyed form. We are reporting on the epitaxial growth of scandium nitride films via DC magnetron sputtering. MgO is the substrate of choice for epitaxial growth of ScN as both adopt the rocksalt crystal structure with comparable lattice parameters (6.4% lattice mismatch), and as an insulator, MgO is ideal for studies of the ScN film properties. Scandium nitride films grown on MgO substrates show resistivity values as high as 10 m -cm for films grown in an Ar/N2 ambient at 50 mTorr and 850°C, as well as rocking curve full width half max values as low as 0.67° for films grown at 20 mTorr and 850°C. The sputtering system is load locked and has a base pressure below 3 x 10^{-7} Torr for all growths. Growth pressure was varied from 5 to 50 mTorr, the temperature from 550°C to 850°C, and the sputtering gun power from 50W to 200W. From these studies, the optimal parameters for growing high resistivity, high mobility ScN are determined. The results of X-ray diffraction, mobility and carrier concentration will be presented. 1 J.M. Gregoire, S.D. Kirby, M.E. Turk, R.B. van Dover, Structural, electronic and optical properties of (Sc,Y)N solid solutions, Thin Solid Films, Volume 517, Issue 5, 1 January 2009, Pages 1607-1609. 2 M. Zebarjadi, Z. Bian, R. Singh, A. Shakouri, R. Wortman, V. Rawat, T. Sands, Thermoelectric Transport in a ZrN/ScN Superlattice, Journal of Electronic Materials, Volume 38, Number 7, Pages 960-963.

9:00 AM Student
GG3, Enhancement of Thermoelectric Efficiency in $Si_{1-x}Ge_x$/Si Heterostructures: *Md Hossain*[1]; Harley Johnson[1]; [1]University of Illinois at Urbana-Champaign

Thermoelectric nanostructured materials, especially quantum heterostructures, have drawn enormous attention recently due to their remarkable promise in energy generation and conversion. However, maximizing the efficiency of thermopower generation involves optimizing several interdependent transport properties including electronic conductivity, Seebeck coefficient, and thermal

conductivities of phonons and electron. Low dimensional and nanostructured materials have recently been demonstrated to exhibit superior thermoelectric properties compared to their bulk counterparts. The effect of physical dimension has been shown to reduce thermal conductivity which enhances thermoelectric efficiency – thermoelectric figure of merit or *ZT* – of the device. Although electronic structure dependent properties can influence thermopower generation at different temperature regimes and length scales, particularly where mean free path of phonons and electrons are comparable to the low dimension of the device, their role on *ZT* remains unknown. In this work, using a combination of first-principles derived electronic structure and a Boltzmann transport formalism it is revealed that alloying in heterostructures can substantially improve thermopower while small length scales lead to degradation in Seebeck coefficient *S*. At room temperature the Seebeck coefficients for pure Si and Ge are computed to be 760 μV/K and 380 μV/K respectively. At the same temperature for a 3.3 nm heterostructure with layer thickness ratio $Si_{0.5}Ge_{0.5}$:Si = 1:1 the maximum Seebeck coefficient is 336 μV/K and for a similar size heterostructure with Ge:Si = 1:1 the maximum Seebeck coefficient is 129 μV/K. The maximum values for $Si_{0.5}Ge_{0.5}$:Si = 1:1 and Ge:Si = 1:1 occur at a chemical potential (carrier density) of 0.0025 Ry ($6x10^{18}$ cm^{-3}) and 0.0058 Ry ($3x10^{19}$ cm^{-3}), respectively. This behavior changes as a function of temperature. Therefore, even though lower physical dimension reduces *S*, a combination of temperature and doping level can be sought to maximize *ZT*. Furthermore, the Lorentz number, which is defined as the ratio of electronic thermal conductivity and electronic conductivity and has a constant value according to the Wiedemann-Franz law for metals, is found to increase by a factor of 2 for lower carrier concentration. Within a reasonable doping range (less than 10^{20} cm^{-3}) no change in Lorentz number is found for the heterostructure, indicating the doping level at which it exhibits metallic transport character. To find an optimized combination of temperature, doping, carrier concentration, and layer thickness ratio for enhanced *ZT* transport, calculations are carried out with several energy dependent relaxation time functions as well as a constant relaxation time approximation. Thus, their relative effects on transport properties are also demonstrated in this work.

9:20 AM

GG4, Isothermal Method for Rapid, Steady-State Measurement of Thermoelectric Materials and Devices: *Patrick Taylor*[1]; Sudhir Trivedi[2]; Witold Palosz[2]; [1]US Army Research Laboratory; [2]Brimrose Corporation

A simple, highly accurate method for characterizing thermoelectric materials, partially assembled devices and full devices is presented. In this work, we introduce non-contact radiative heat as a new, independently controlled heat flow that can be used to force isothermal conditions during thermoelectric measurements. Under isothermal conditions, the steady-state heat flows can be determined with high accuracy because parasitic heat flows (e.g., that along the sensing thermocouples, Thomson heat) become negligible and that enables accurate determination of thermoelectric properties such as thermal conductivity. This method applies to bulk and thin-film materials, and can also be extended to determine device performance metrics including coefficient of performance. To validate the method, samples of (Bi,Sb)2(Se,Te)3 alloy bulk materials were prepared by a vertical Bridgman technique. The samples typically had an area-to-length ratio of 0.405 cm2/cm. The Seebeck coefficient was found to be +178 microvolts/Kelvin, the electrical resistivity was determined to be 0.74 milliohm-cm, and the thermal conductivity was determined to be 14.9 mWatt/cm-K. The thermal conductivity was determined by the comparison method and that was compared to that measured using the new technique.

9:40 AM

GG5, Late News

10:00 AM Break

10:20 AM Student

GG6, Thermomagnetic Transport Properties of $(Ag_xSbTe_{x/2+1})_{15}(GeTe)_{85}$ Thermoelectric Materials: *Yi Chen*[1]; Christopher Jaworski[1]; Xinbing Zhao[2]; Joseph Heremans[1]; [1]Ohio State University; [2]Zhejiang University

Nonstiochiometric $(Ag_xSbTe_{x/2+1})_{15}(GeTe)_{85}$ thermoelectric materials have been prepared by the air quenching method with x varying from 0.4 to 1.2. All samples exhibit good electrical performances and low thermal conductivities, and as a consequence, the ZT maximum reaches 1.5 when x = 0.6. Thermoelectric and thermomagnetic transport properties, including Hall and Nernst effect are measured and analyzed in this material system. We then use the "method of four coefficients" on the resistivity, Seebeck, Hall and Nernst coefficients to reveal the scattering mechanisms in these high carrier density materials, alongside with the electron Fermi energy, density-of-states effective mass, and electron mean free path.

10:40 AM Student

GG7, Thermoelectric Properties of Sn-Rich $Pb_{1-x}Sn_xTe$ Alloys Doped with Indium: *Yibin Gao*[1]; Joseph Heremans[1]; [1]The Ohio State University

It has been reported that PbTe doped with Tl has a significant increase in Seebeck coefficient and thus ZT because Tl induces a resonant impurity level in the valence band of PbTe[1]. Indium as an another Group III impurities has also been reported as a resonant level in PbTe and solid solution with SnTe. Previous studies have been focusing on $Pb_{1-x}Sn_xTe$ doped with indium on Pb-rich side[2], however, little is known about the properties of In dopant on Sn-rich side. Here we present our results on Seebeck coefficient, electrical conductivity, Hall coefficient and transverse Nernst-Ettinghausen coefficient as a function of Sn (x=0.5–1) and In concentrations in the temperature range between 80 K and 480K. Our preliminary results indicate that indium is a resonant level in these alloys and therefore can increase power factor over alkali doped material. Reference: [1] Heremans, J. P. et al. (2008). "Enhancement of Thermoelectric Efficiency in PbTe by Distortion of the Electronic Density of States." Science 321(5888): 554-557.[2] Jovovic, V et al. (2008). "Low temperature thermal, thermoelectric, and thermomagnetic transport in indium rich $Pb_{1-x}Sn_xTe$ alloys." Journal of Applied Physics 103(5): 053710-7.

11:00 AM

GG8, Incorporation of $AgSbTe_2$ to $Pb_{1-x}Sn_xTe$ by Mechanical Alloying of End Compounds: Aaron D. LaLonde[1]; Lakshmi Krishna[1]; Eric D. Hintsala[1]; *P.D. Moran*[1]; [1]Michigan Technological University

The benchmark alloys for highly functional thermoelectric material in the 500-700 K temperature range have been (y)($AgSbTe_2$)-(1-y)($Pb_{1-x}Sn_xTe$) material processed by melt alloying where nanostructures are formed as inclusions during post processing thermal treatment and have been reported to be the likely cause of the large *ZT* values. The reproduction of these structures has proven difficult by the lack of comparable results being reported in the literature. This alloy system, though promising as a highly functional thermoelectric material, will require the development of processing techniques more amenable to reproducing these non-equilibrium compositional inhomogeneities if the system's potential is to be realized. This work investigates a different approach to obtain the reported alloy structure containing areas of compositional variation reported to be responsible for increased thermoelectric functionality. The approach taken is to produce the end compounds of $Pb_{1-x}Sn_xTe$ (x=0.1, 0.2, 0.3) and $AgSbTe_2$ by mechanical alloying elemental powders followed by mixing and consolidation to form the desired (y)($AgSbTe_2$)-(1-y)($Pb_{1-x}Sn_xTe$) alloy. A 2-step mechanical alloying process was developed to produce $AgSbTe_2$ with a crystallite size of ~28 nm with only trace presence of the Ag_2Te phase present. After the end compounds were mixed and consolidated the resultant electrical conductivity, carrier mobility and carrier concentration were measured and compared to consolidated samples without the $AgSbTe_2$ addition. Analysis of all samples was done by xray diffraction and determined the lattice parameter, composition, phases present, and size and an estimation of the spacing between inclusions of any secondary phases present in the consolidated material. The consolidated material was found to be n-type for the 3 compositions investigated both with and without the inclusion of $AgSbTe_2$. It was observed that the increase in Sn composition as well as the inclusion of $AgSbTe_2$ results in the addition of p-type carriers to the material. There was no xray diffraction evidence that the mixing of the two distinct phases in powder form resulted in a two phase solid with $AgSbTe_2$ inclusions, despite having started with submicron $AgSbTe_2$ particles and having only subjected the solid to ~550 °C during consolidation. This result is consistent with $AgSbTe_2$ and $Pb_{1-x}Sn_xTe$ forming a solid solution over these compositions. The carrier mobility values have been compared to an analysis of the mobility that would result from

carrier scattering by phonons only. The room-temperature mobility observed in these materials is attributed to a contribution of electron scattering from both phonons and small amounts of SnO_2 and elemental Pb and Sn. This work provides a basis for further development for the (y)($AgSbTe_2$)-(1-y)($Pb_{1-x}Sn_xTe$) material system made by mechanical alloying and mixing of the end compounds and provides evidence that material processed by this method has potential to result in highly functional thermoelectric material.

11:20 AM Student

GG9, Electron Transport Properties of Mechanically Alloyed N-Type $Pb_{1-x}Sn_xTe$ Thermoelectric Elements: *Lakshmi Krishna*[1]; Aaron Lalonde[1]; Eric Hintsala[1]; Matthew Swanson[1]; Peter Moran[1]; [1]Michigan Technological University

Commercial thermoelectric (TE) materials for use in power generation must demonstrate a combination of high figure of merit at the operating temperature ($ZT = \sigma S^2/k$, where σ is the electrical conductivity, S is the Seebeck coefficient and k is the thermal conductivity) and must be made by a cost-effective process for large scale production of the material. Traditionally, bulk TE materials are made by melt-alloying the elemental powders of high purity(≥ 99.999 %). Recent demonstration[1] of a mechanical alloying (MA) process to transform elemental powders into solid $Pb_{0.5}Sn_{0.5}Te$ with thermoelectric functionality comparable to bulk melt-alloyed material has spurred interest in the further investigation of this approach to cost-effectively fabricate high performance thermoelectric power generation material. In order to determine the potential of the mechanically alloyed $Pb_{1-x}Sn_xTe$, the degree to which the mobility of the charge carriers is impacted by the impure starting materials and the microstructural features induced by the MA process must be determined. In this work we analyze experimental room temperature carrier concentration and mobility data in conjunction with the temperature dependence of the electronic conductivity measured from 300K to 750K and experimental Seebeck coefficient measurements from 300K to 600K taken from n-type discs of PbSnTe made by consolidating mechanically alloyed 99.9 % pure elemental Pb, Sn, Te powders with x ranging from 10 % to 30 % and compare the experimentally measured temperature dependence of the electronic mobility to that which would be expected for single crystal PbSnTe doped to the same carrier concentration. The transport coefficients that would be expected for single crystal PbSnTe are calculated by using the Boltzmann equation with an energy dependent relaxation time approximation within the framework of Kane model for energy dispersion. The non-parabolic conduction band and light hole valance band at L-point and the parabolic heavy hole valance band at the Σ-point are considered when calculating the transport properties. The major scattering mechanisms taken into account are due to phonons and alloy scattering of carriers. The impact of carrier scattering in all three bands are explicitly taken into account. At room temperature the electronic mobilities of the mechanically alloyed material are less than what would be expected for single crystal material. However, in the temperature regime (500 K to 700 K) for which the thermoelectric material is expected to operate in power generation applications, the difference between the experimentally obtained mobilities from the MA material and the values calculated for perfect single crystal material are within ~10-15 %. The processing-induced degradation of mobility observed at room temperature has little impact on the transport properties of the material in the temperature regime of interest. 1. A.D.Laonde and P.D.Moran, Journal of Electronic Materials, Vol 39, No 1, 8, 2010.

11:40 AM

GG10, Late News

Session HH: Semiconductor Processing, Surfaces and Contacts

Friday AM
June 25, 2010

Room: 138
Location: University of Notre Dame

Session Chairs: Douglas Hall, University of Notre Dame; Suzanne Mohney, Pennsylvania State University; Lisa Porter, Carnegie Mellon University

8:20 AM Student

HH1, Effect of Contact Modification on Charge Transport at Different Length Scales in Poly(3-Hexylthiophene)-Based Bottom-Contact Field-Effect Transistors: *Kumar Singh*[1]; Tomasz Young[1]; Toby Nelson[1]; John Belot[1]; Richard McCullough[1]; Tomasz Kowalewski[1]; Ponnusamy Nachimuthu[2]; Suntharampillai Thevuthasan[2]; Lisa Porter[1]; [1]Carnegie Mellon University; [2]Pacific Northwest National Laboratory

In this study we report the effect of modification of contacts on the field-effect mobility of poly(3-hexylthiophene) (P3HT) in bottom-contact field effect transistors (FETs). The Au contacts are modified by (a) recessing the contacts in the SiO_2 gate oxide surface to get *planar* OFETs and (b) using bis-trifluoromethane-benzenethiol (BTFMBT) molecules that form self-assembled monolayers (SAMs) on the contacts. Atomic force micrographs (AFM) of extremely thin P3HT films show that planarization of the contacts results in remarkable improvement in polymer morphology in the vicinity of the contacts. In the case of contact modification by the SAMs, the work function of the Au contacts increases from 5.0±0.1 eV to 5.6±0.1 eV, as measured using ultraviolet photoelectron spectroscopy. Both conditions cause a decrease in the contact resistance (R_C) in comparison with conventional bottom-contact (*normal*) OFETs. For example, R_C for *planar* OFETs, $R_{C(planar)}$ = 0.4 M , and SAM-modified OFETs, $R_{C(SAM)}$ = 0.18 M , are lower than that for the conventional OFETs, $R_{C(normal)}$ = 0.61 M at a gate voltage V_G = -80 V. Interestingly it is observed that upon contact modification, the charge transport improves only in short channel length OFETs (L ~ 3-10 μm), whereas the field-effect mobilities (μ) are less effected for OFETs with longer channel lengths (e.g., at L = 3 μm and V_D = -80 V, μ_{planar} = 0.25 $cm^2V^{-1}s^{-1}$, μ_{SAM} = 0.26 $cm^2V^{-1}s^{-1}$, and μ_{normal} = 0.15 $cm^2V^{-1}s^{-1}$; at L = 20 μm, μ_{planar} ~ μ_{SAM} ~ μ_{normal} ~ 0.06 $cm^2V^{-1}s^{-1}$). Wide area AFM scans of OFETs of channel lengths, L = 10 μm and 30 μm show that the P3HT nanofibrils extend across short channels but not across long channels. The effects on contact resistance and mobility can be explained based on a difference in charge transport for short- and long-channel devices due to the nanofibril morphologies.

8:40 AM Student

HH2, Low Pressure Chemical Vapor Deposition of Conformal Boron Thin Films on Deep RIE-Etched Si Substrates: *Nicholas LiCausi*[1]; Justin Clinton[1]; Yaron Danon[1]; James Lu[1]; Ishwara Bhat[1]; [1]Rensselaer Polytechnic Institute

Recently there has been significant research in solid-state neutron detectors since these can be used for the detection of nuclear materials necessary for homeland security applications. Many of these detectors work on the principle of converting thermalized fission neutrons into alpha-particles and detecting the ionization produced by the alpha-particles interaction with the p-n junction. This is necessary because the neutron is charge-neutral and cannot be sensed by standard semiconductor p-n junction. The conversion of neutrons to alpha-particles requires a material with high thermal neutron cross-section. Typically boron-10 or lithium-6 fluoride is used. We have selected boron-10 because it has a higher cross-section and therefore can result in higher efficiency. In order to improve detection efficiency, non-planar film geometry must be employed. This is to accommodate a fundamental mismatch in required B-10 thicknesses. To maximize the probability that an incident neutron will interact with a B-10 atom, the layer must be very thick (~45 μm). However, for the generated alpha-

particles to escape, the B-10 layer must be thin (~2-3 µm). Otherwise, the alpha-particles will be reabsorbed by the B-10. This mismatch led us to the use of high aspect-ratio holes with Si p-n junctions. A variety of high aspect-ratio trench/hole geometries of Si p-n junctions have been studied for this work. Trench depths vary from 15–60 µm and widths range from 2–8 µm. Due to the high aspect-ratio of these trenches, Low Pressure Chemical Vapor Deposition (LPCVD) is favorable for boron deposition. Also, the described LPCVD requires equipment/precursors that are existing in many manufacturing facilities, allowing for high-volume, low-cost production. Boron is deposited on deep RIE-etched Si p-n junctions in a low pressure horizontal CVD reactor. Pressures ranging from 250–1000 mtorr under a 1 sccm diborane flow have been studied. It is believed that the B_2H_6 behaves like SiH_4 in Si deposition. Experiments with temperatures from 400–700 °C have been performed. Experiments involved pre-deposition purging and temperature stabilization, then a 30 minute growth period and subsequent cooling in N_2. Films have been characterized with Scanning Electron Microscope (SEM) imaging. Growth rates as high as 1 µm/hr have been observed. Films thickness ranged from 0.2–1.0 µm. Also, conformal coverage inside the high aspect ratio holes has been studied. As the growth pressure dropped below 300 mtorr the conformal coverage improved. Additional review includes film morphology and strain. High film-stress is observed. Stress often leads to spontaneous cracking/pealing of the film within minutes or after as long as weeks. Stress for a 0.6 µm film is ~850 MPa at 300K. Future work will be discussed. This material is based upon work supported by the US Department of Homeland Security under grant award number 2008-DN-077-ARI008-003.

9:00 AM Student

HH3, Assessment of the Passivation Capabilities of Two Different Covalent Modifications on GaP (100): *David Richards*[1]; Dmitry Zemlyanov[1]; Albena Ivanisevic[1]; [1]Purdue University

The ability to manipulate semiconductor surfaces with organic molecules is attractive due to the potential of making biosensors more compatible and implantable. Silicon has been a heavily researched semiconductor surface for chemical passivation due mainly to its domination of the optoelectronic industry. Recently, the advancement of semiconductor technology has allowed other semiconductors to become attractive platforms for biosensors. Gallium phosphide is a III-V semiconductor material that is commonly used in high temperature and light-emitting devices. The potential for surface atoms to leach into the surrounding media causes problems for biocompatibility. Organic molecules are capable of tying up the loose bonds on the surface and thus preventing leaching and the formation of dissolvable oxide layers. This study compares the ability of two similar organic molecules to form covalent bonds with the GaP (100) surface. Undecenoic acid (UDA) is a terminal alkene that can potentially form Ga-C bonds and mercaptoundecanoic acid (MUA) is a thiol that can be used to generate Ga-S bonds. The conditions required for alkene grafting are less hazardous (no high temperatures or high vacuum) and less time-consuming due to the alkene's ability to form covalent bonds with the surface by way of a radical initiation step caused by irradiation with UV light. The chemical passivation capabilities of each molecule were assessed by exposing the functionalized surfaces to different media including water, various pH solutions, and various concentrations of H2O2 in saline. The surfaces were investigated by contact angle measurements, atomic force microscopy (AFM), and X-ray photoelectron spectroscopy (XPS). Toxicity levels, which are important for sensing applications, were evaluated by inductively coupled plasma – mass spectrometry (ICP-MS) on the media in which surfaces were stored in order to identify any gallium leaching from the substrates. Both molecules formed fairly disordered monolayers demonstrated by comparable oxide thicknesses. The UDA molecules demonstrated better stability compared to MUA based on water contact angle measurements. Data extracted from XPS results indicated a tilt angle of roughly 55° for UDA and 84° for MUA. In terms of coverage, UDA formed 1 – 1.5 monolayers while MUA formed less than half of a monolayer. With respect to toxicity, the UDA-functionalized GaP provided better passivation which was confirmed by less gallium leaching into water and saline solutions. Overall, the superior passivation provided by UDA demonstrates that alkene grafting has better potential for modifying GaP based devices such as implantable sensors.

9:20 AM Student

HH4, Comparison of Ga-Polar and N-Polar GaN by KOH Photoelectrochemical Etching: *Younghun Jung*[1]; Fan Ren[2]; Soohwan Jang[3]; Jihyun Kim[1]; [1]Korea University; [2]University of Florida; [3]Dankook University

III-nitride materials have made huge progress in optical devices, such as light emitting diode (LEDs), and laser diode(LDs). Wet chemical etch has been widely used in fabrication process and analysis. We studied KOH-based wet etch to optimize the process conditions and device performances. Specially, optical and structural the GaN according to the progress of wet-etch is very important. However, the comparison between N-face and Ga-face has been rarely investigated. We report the differences of the etching mechanism on each face. We studied the effects of KOH solution at each face (Ga-,N-) of GaN. To find the etching rates of each face, both faces were PEC-etched for the same time. We used various concentrations (1M, 2M, and 4M) at 50°C KOH solutions under UV illumination. The surface morphology and optical properties of G- and N- face were characterized by atomic force microscope, scanning electron microscope (SEM) and reflectivity measurements. SEM images showed the differences in surface morphologies of each face depending on the concentrations of KOH solutions. The hexagonal pyramid on the surface confirmed that c-plane growth. The summary of root mean square (RMS) data at various etching conditions shows changing of surface mophology. When the molar concentrations of KOH solution are increased in 10min etching process, the Ga-face became more flat. In contract the N-face became rough, which was in consistent with the reflectance data. The surface morphology and the optical properties had changed with the extended KOH etching. When the concentration of solution was increased, the surface roughness of the Ga-face also was increased. Detail about the mechanism of PEC etching and the results will be discussed.

9:40 AM

HH5, N-Type Electrodes for GaN-Based Vertical Light Emitting Diodes: Joon-woo Jeon[1]; Seong-Han Park[1]; Jihyung Moon[2]; June-O Song[2]; Gon Namgoong[3]; *Tae-Yeon Seong*[1]; [1]Korea University; [2]LG innotek; [3]Old Dominion University

High-power GaN-based vertical light-emitting diodes (VLEDs) are of considerable importance for their applications in solid state lighting. Formation of high-quality ohmic contacts having low-resistance and excellent reliability is essential for the fabrication of high-performance GaN-based VLEDs. For top-emission LEDs, n-ohmic contacts are easily formed on Ga-polar n-GaN using either Ti- or vanadium (V)-based schemes. However, for n-type side-up VLEDs (where the n-GaN has N-polarity), n-type ohmic contacts were shown to be difficult to achieve. For example, when Ti/Al contacts to hydride vapour phase epitaxy-grown n-GaN were annealed above 500ºC, Ga-polar n-contact showed ohmic behaviours with a contact resistivity of ~$10^{-5}\Omega cm^2$, but N-polar n-contacts exhibited non-ohmic behaviours. It was also shown that the electrical characteristics of Ti/Al contacts to N-polar n-GaN thin films prepared by a laser lift-off (LLO) process were significantly degraded upon annealing at temperatures in excess of 300 ºC. The better characteristic was attributed to the generation of polarization-induced two-dimensional electron gas caused by the formation of interfacial AlN on p-GaN. It was, however, shown that the use of 5 nm-thick Pd interlayers produced was very effective in improving the electrical properties of Ti/Ai-based contacts upon annealing at temperatures in excess of 450ºC as compared to Ti/Al contacts to LLO-prepared N-polar n-GaN. The better electrical behaviours were attributed to the formation of stable AlN at the interface. The different argument is indicative of the complicated role by which the interfacial AlN layer plays during an annealing process. In this work, in order to obviate any effects associated with the interfacial AlN, we have investigated the electrical properties of Al-free V-based contacts to different polar n-GaN. Our Ga-polar and N-polar n-GaN samples have been prepared by MOCVD, molecular beam epitaxy (MBE) and an LLO process. It is shown that regardless of the crystal polarities, all the samples exhibit similar electrical characteristics. The as-deposited samples are ohmic, but become non-ohmic when annealed at 300 - 500ºC. The samples are ohmic again at 700ºC. Based on the x-ray photoemission spectroscopy and Auger electron spectroscopy results,

the ohmic and degradation behaviours are explained in terms of the formation of donor-like surface defects and Ga vacancies, which are generated by dry etching, the outdiffusion of Ga, and the formation of nitide phases.

10:00 AM Break

10:20 AM Student

HH6, In-situ Ohmic Contacts to p-InGaAs: *Ashish Baraskar*[1]; Vibhor Jain[1]; Mark Wistey[2]; Evan Lobisser[1]; Brian Thibeault[1]; Yong Ju Lee[3]; Arthur Gossard[1]; Mark Rodwell[1]; [1]University of California, Santa Barbara; [2]University of Notre Dame; [3]Intel Corporation

Very low resistance metal-semiconductor contacts are crucial for the performance of transistors in THz bandwidths. The base and emitter contact resistivities (ρ_c) in heterojunction bipolar transistors (HBTs) must decrease in proportion to the inverse square of the transistor cutoff frequency. A ρ_c of less than $1x10^{-8}$ -cm^2 is required for III-V HBTs and FETs for having simultaneous 1.5 THz f_t and f_{max}. Ohmic contacts to p-type $In_{0.53}Ga_{0.47}As$ have been studied extensively because of its application as the base contacts in InP based HBTs. Pd has shown ρ_c = 6.3 x 10^{-8} -cm^2 to p-InGaAs, but penetrates into the semiconductor by combined chemical reaction and diffusion. Low resistivity, thermally stable contacts having < 5 nm metal penetration depth are required for HBTs having < 20 nm thick base layers. Here we report $\rho_c = (2.0 \pm 0.8)\times10^{-8}$ -cm^2 for in-situ Mo contacts to p-type $In_{0.53}Ga_{0.47}As$. The semiconductor epilayers were grown by solid source MBE. A 100 nm undoped $In_{0.52}Al_{0.48}As$ layer was grown on a semi-insulating InP (100) substrate, followed by 100 nm of carbon doped $In_{0.53}Ga_{0.47}As$. 20 nm of Mo was deposited in an electron beam evaporator attached to the MBE chamber under ultra high vacuum. Mo was deposited on half of the surface of the samples using a shadow mask. Hall measurements were done on the samples not coated with Mo. Samples coated with Mo were processed into transmission line model (TLM) structures for contact resistance measurement. Ti (20 nm)/Au (500 nm)/Ni (50 nm) contact pads were patterned on the samples using photolithography and lift-off after an e-beam deposition. Mo was then dry etched in an SF_6/Ar plasma using Ni as a mask. Resistances were measured by four-point (Kelvin) probing. The processed samples were annealed under nitrogen atmosphere at 250°C for 120 minutes, replicating the thermal cycle experienced by a base contact during transistor fabrication. The ρ_c achieved for the un-annealed samples was $(2.0 \pm 0.8)\times10^{-8}$ -cm^2, which is the lowest reported to date for Ohmic contacts to p-type InGaAs. As determined through Hall measurements, the active carrier concentration, mobility and sheet resistance was 1.1 × 10^{20} cm^{-3}, 39.6 cm^2/Vs and 150 /□, respectively. The annealed samples show a ρ_c of $(2.5 \pm 0.9)\times10^{-8}$ -cm^2. TEM images of the annealed samples show a uniform and abrupt Mo-InGaAs interface, indicating minimal intermixing of the metal semiconductor layers. We speculate that the increase in ρ_c upon annealing may be due to the presence of an interfacial carbon layer which degrades upon annealing. Although ρ_c increases to $(2.5 \pm 0.9)\times10^{-8}$ -cm^2 upon annealing, in-situ Mo remains a strong candidate for base Ohmic contacts in THz HBTs.

10:40 AM Student

HH7, Degradation of Ohmic and Schottky Contacts on InGaAs MHEMTs during Bias Stressing: *Erica Douglas*[1]; Ke Hung Chen[1]; Chih Yang Chang[1]; Lii-Cherng Leu[1]; Chien-Fong Lo[1]; Byunghwan Chu[1]; Fan Ren[1]; Stephen Pearton[1]; [1]University of Florida

Numerous studies have shown that InGaAs based metamorphic high electron mobility transistors (MHEMTs) have similar mean time to failure (MTTF) as that of InP based HEMTs, about 106 hours. However, InGaAs MHEMTs require a substantial burn-in process in order to stabilize device performance and eliminate infant mortality. Typically, drain current decreases while Ohmic contact resistance increases during electrical stress and stabilizes within 24-60 hours. In order to study the device reliability and failure mechanisms, both high temperature storage tests and DC stress tests were performed on MHEMTs. InAlAs/InGaAs MHEMTs, obtained from a vendor, were stressed for 36 hours at a drain voltage of 3V. Additional devices underwent a thermal storage test at 250°C for 36 hours. Transmission line method (TLM) structures were also stressed under similar conditions. The InAlAs/InGaAs MHEMTs employed a two finger Ti/Pt-based Schottky gate design with a length of 150 nm, a gate width of with 75 µm, and 1.2 µm spacing between both gate/drain and gate/source. The TLM patterns also present on the device chip employed 45 X 70 µm pads with gaps of 3, 6, 9, 12 and 15 µm. Under both DC and thermal stress conditions, the drain current decreased about 12.5%. Therefore, the devices suffered from an increase in parasitic resistance during stressing. The TLM patterns were stressed in order to examine the effect of the gate on the increase of the parasitic resistance and degradation of drain-source current.The total resistance of the TLM structures increased significantly with time in the first 12 hrs of thermal storage at 250°C, while the specific contact resistivity increases much more than sheet resistance. The gate characteristics of the thermal and DC stressed HEMTs showed significant degradation and gate current increased several orders in both forward and reverse bias conditions. This indicates that the contact between the Ohmic metal and semiconductor dominated the degradation during the thermal storage. Devices stressed under DC suffered from substantial gate sinking, in which the bottom Pt layer of the Pt/Ti/Pt/Au mushroom gate diffused into the InAlAs gate contact layer. The energy-dispersive x-ray spectroscopy (EDS) elemental analysis was used to analyze the Pt diffusion depth the gate region. The high current density, 1 × 10^5 A/cm2, flowing across the thin ohmic metal then across the metal semiconductor interface into the semiconductor the Ohmic metal caused the Ohmic metal to diffuse during the burn-in process. This caused the electromigration-induced voids and the formation of additional metal spikes at the edge of the Ohmic metal contact pads.

11:00 AM Student

HH8, Characterization of Thin InAlP Native Oxide Gate Dielectric Layers for GaAs MOSFET Applications: *Wangqing Yuan*[1]; Douglas Hall[1]; [1]University of Notre Dame

Due to high electron mobility, low gate leakage current and the potential for positive threshold, GaAs-based III-V MOSFETs are of interest for high-speed circuit applications. The quality of gate dielectrics is crucial for III-V MOSFET devices. The thermal grown InAlP oxide (InAlP-ox) is promising in terms of its low processing cost, excellent insulating property, as well as an inward growth mechanism, which provides a cleaner oxide-semiconductor channel interface. In the fabrication of GaAs MOSFET devices utilizing thin InAlP native oxides, the oxidation process must be accurately understood and controlled. In this work, variable angle spectroscopic ellipsometry (VASE) is utilized to both characterize InAlP oxidation kinetics and to accurately determine the final thickness of the oxide. To accurately characterize the oxidation of thin (5 nm) InAlP layers used in a MOSFET structure (to yield an ~8 nm thick native oxide dielectric layer), accurate optical constants of each material and an accurate model describing the oxidation dynamics of InAlP are required. The optical constants of InAlP and InGaP (lattice matched to GaAs) have been determined by a multi-sample VASE analysis (1.45 to 5.45 eV, 300 K) of 100 and 200 nm thick epilayers. The optical constants of InAlP-ox are determined by analysis of a 30 nm InAlP epilayer on GaAs, fully oxidized at 440°C for 85 min. The InAlP-ox optical constants are described by Tauc-Lorentz (TL) oscillator terms, and the optical constants of InAlP and InGaP are described by Hersinger-Johs parameterized semiconductor oscillator functions. Comparisons are made between the optical constants of the fully-oxidized and "over-oxidized" InAlP-ox samples (oxidation times of 128 and 170 min). Upon full oxidation, no significant thickness change of the InAlP-ox layer is observed. However, with increasing oxidation time, the oxide refractive index n~1.6 below its bandgap decreases, and the bandgap increases (from ~3.3 to ~4.5 eV). These results suggest that the oxidation rate of the aluminum component in InAlP is faster than that of the less reactive indium component, and that the indium component continues to oxidize after full oxidation of the aluminum component is reached. Accordingly, a three-layer model (ambient/InAlP-ox/EMA/InAlP/GaAs substrate) is used to test InAlP and InAlP-ox optical constants for a 100 nm InAlP film partially oxidized for 100, 120, 130 and 140 min. The effective medium approximation (EMA) layer describes the incomplete oxidation of the indium component in InAlP-ox, and excellent agreement between thickness values measured by transmission electron microscopy (TEM) imaging and VASE confirms the accuracy of our optical constants. Finally, these models have also been extended to accurately fit the thickness of <10 nm InAlP-ox gate oxides grown directly upon a multi-layer MOSFET heterostructure. The deviation of InAlP-ox thickness results

determined by VASE from those determined by TEM is within 4%.

11:20 AM
HH9, Post-Growth InGaAsP Quantum Well Intermixing for High Saturation Power Semiconductor Optical Amplifiers: *Jonathan Klamkin*[1]; Jason Plant[1]; David Chapman[1]; Douglas Oakley[1]; Antonio Napoleone[1]; Kevin Ray[1]; Paul Juodawlkis[1]; [1]Lincoln Laboratory, Massachusetts Institute of Technology

Quantum well intermixing (QWI) is a technique whereby quantum wells (QWs) can be altered following epitaxial growth. This technique provides a means for controlling the QW bandedge selectively across a semiconductor wafer, allowing for the realization of novel optoelectronic devices and photonic integrated circuits. For the InGaAsP material system, ion-implantation-enhanced interdiffusion is one of the more successful QWI techniques demonstrated. With this technique, ion implantation is used to create vacancies that promote intermixing of atoms at the interfaces of QWs and barriers during a subsequent annealing step. The intermixing reshapes the QWs and effectively increases the bandgap energy. In this work, we have developed a QWI technique specifically tailored for the bandedge shift required to realize a novel multi-section semiconductor optical amplifier (SOA) that is based on the slab-coupled optical waveguide (SCOW). The performance of SOAs can be improved with a multi-section device architecture incorporating a pre-amplifier region and a post-amplifier region. We have proposed using QWI to create a novel multi-section SOA whereby the bandedge and in turn gain spectrum can be tailored along the length of the device to improve the inherent tradeoff between gain and output power, and to increase efficiency. The QWI process used for fabricating the multi-section SOAs entails a dielectric masked selective implant of Phosphorous ions, removal of the dielectric mask by wet chemical etching, dielectric encapsulation of the sample to prevent desorption during the subsequent annealing steps, and high temperature annealing. The initial implant and the processing steps should be designed to minimize damage to the underlying QW layers. It is therefore desirable to minimize the ion distribution in the vicinity of the QWs. The implant energy and dose need to be considered, as well as high temperature processing steps prior to the annealing steps that could lead to premature diffusion of vacancies. The annealing for interdiffusion can damage the QWs by forming traps; however the damage is also repaired by the annealing. This damage can be quantified by monitoring photoluminescence (PL) peak intensity. For the multi-section SOA described, it is beneficial to tailor the QWI process based on the amount of bandedge shift desired while subsequently minimizing damage. Here we have optimized a QWI process for desired bandedge shifts for a multi-section SCOW SOA. The device design requires bandedge wavelength shifts in the range of 30-60 nm; therefore it is desirable that the PL intensity, used to quantify recovery of the damage material, be maximized for such shifts. Following experimentation, it was shown that with an implant energy and dose of 80 keV and 3.0e14 cm^{-2}, corresponding to an implant range and straggle of 89 nm and 44 nm, the PL intensity was fully recovered following the QWI process.

11:40 AM
HH10, Late News

Session II: Heteroepitaxy on Silicon

Friday AM
June 25, 2010

Room: 141
Location: University of Notre Dame

Session Chairs: Ralph Dawson, Univ of New Mexico; Ganesh Balakrishnan, Univ of New Mexico

8:20 AM Student
II1, Reduction in Operation Voltage of Light Emitting Diodes Fabricated in Si/III-V-N/Si Heterostructure: *Keisuke Yamane*[1]; Shintaro Yamada[1]; Yuzo Furukawa[1]; Hiroshi Okada[1]; Akihiro Wakahara[1]; [1]Toyohashi University of Technology

Monolithic integration of III-V(-N)-based photonics and Si-based electronics has been attracted for realizing a novel optoelectronic integrated circuits (OEICs)[1]. We have demonstrated monolithic OEIC test chip, in which Si-based MOSFETs and GaPN-based III-V-N light emitting diodes (LEDs) are integrated into a lattice-matched Si/III-V-N/Si heterostructure [2]. In this structure, however, the operation voltage of the LEDs resulted in relatively high due to the Si-capping layer grown on the III-V-N layer. In this work, we investigated the effects of the Si-capping layer on an electrical property and succeeded in the reduction in the operation voltage of the LEDs. Firstly, Si/p^+-GaPN/p-GaPN/n-GaPN (referred to as sample A) and Si/p-GaPN/n-GaPN (referred to as sample B) structure were grown on n-Si substrates by molecular beam epitaxy. Here, the carrier concentrations for p^+-GaPN and p-/n-GaPN were designed to be $5x10^{19}$ cm^{-3} and $5x10^{17}$ cm^{-3}, respectively. After the growth, in order to obtain p-Si-capping layers with carrier concentration of over $1x10^{18}$ cm^{-3}, both samples were annealed at 900°C following boron ion implantation into the Si-capping layers. These processes are based on our original fabrication process of the monolithic OEIC test chip [2]. The Al electrodes with 500 μm in diameter and AuSb broad contacts were used to form Ohmic contacts for the p-Si-capping layers and the n-Si substrates, respectively. Both samples were cleaved into 1x1 mm^2 chip and current-voltage (I-V) curves were measured. The operation voltage to obtain the current density of 1 A/cm^2 is 1.5 V in sample A. This value is almost the same as that of a typical GaPN homojunction (HJ)-LED on a Si substrate without a Si-capping layer. The operation voltage of sample B is 1 eV higher than that of sample A. The valence band offset between GaP and Si has been estimated to be 1.05 eV [3]. Due to this valence band offset, 50-nm-thick depletion layer is formed in the p-GaPN layer at the p-GaPN/p-Si heterointerface in sample B. This depletion layer acts as thick potential barrier for holes injected from the p-Si-capping layer. In the case of p^+-GaPN/p-Si heterointerface in the sample A, the depletion layer thickness is decreased to 5 nm. This thickness would be thin enough for holes to penetrate the potential barrier by the tunnel effect. Therefore, the operation voltage is lowered by adding the p^+-GaPN layer in between the p-GaPN layer and the p-Si-capping layer. [1] I. Hayashi, Jpn. J. Appl. Phys. 32 (1993) L266. [2] H. Yonezu, Y. Furukawa, A. Wakahara, J. Cryst. Growth. 310 (2008) 4757. [3] I. Sakata, H. Kawanami, Appl. Phys. Exp. 1 (2008) 091201.

8:40 AM
II2, GaN/AlN Heterostructures on Vertical {111} Fin Facets of Si (110) Substrates: *Mark Holtz*[1]; Vladimir Kuryatkov[1]; Wen Feng[1]; Mahesh Pandikunta[1]; J. Woo[2]; H. Harris[2]; D. Garcia[3]; Sergey Nikishin[1]; [1]Texas Tech University; [2]Texas A&M University; [3]SVTC

Architectures analogous to silicon fin field effect transistors (FinFETs) are of current interest for achieving high device density. The high mobility and high breakdown field of III-nitride materials, along with a wide range of alloy compositions for band structure engineering, makes devices based on vertically-oriented fins of these materials interesting for a range of applications. Fin architectures provide novel design opportunities such as the formation of non- and semi-polar surfaces, and compatibility with silicon for future integration with conventional electronics. These attributes are promising for multiple electronic device technologies operating at high speeds. In order to explore these possibilities, experiments are first needed to obtain thin (sub-micron) AlN/GaN sidewall growth on Si fin structures with high aspect ratios, and the material properties must be investigated. In this work we explore substrate structuring to produce silicon fins with vertical {111} plane sidewalls. Using these structured substrates we develop selective area epitaxy (SAE) for growing thin (0001) AlN/GaN layers on the vertical sidewalls.We will describe our recent progress using metallorganic vapor phase epitaxy to develop selective sidewall epitaxy of AlN/GaN on vertical fins of silicon. Silicon (110) wafers are structured to form fins with {111} sidewall facets. By adapting a pulsed layer epitaxy method, AlN buffer layers are grown with uniform thickness < 100 nm on vertical {111} surfaces, followed by GaN which grows selectively on the AlN to form the sidewall fin structures. Height is controlled by etching of the Si stripes and GaN width is controlled by growth duration. Raman measurements of the GaN show very narrow line widths, consistent with excellent material quality. Spatial dependence of micro-cathodoluminescence mapping of the GaN band gap emission shows compressive strain in the GaN at the AlN interface relaxes closer to the fin corners.

9:00 AM Student

II3, 2µm Thick Device Quality GaN on Si(111) Using AlGaN Graded Buffer: *Benjamin Leung*[1]; Qian Sun[1]; Christopher Yerino[1]; Yu Zhang[1]; Jung Han[1]; Hongwei Li[2]; Dong Lee[2]; Eric Armour[2]; Ajit Paranjpe[2]; [1]Yale University; [2]Veeco Compound Semiconductor, Inc.

As opposed to the conventional use of sapphire or SiC substrates, silicon enables scaling to large diameter wafers, significant cost reduction, enhanced thermal and electrical properties, and the potential for on-chip integration between GaN and Si electronics. GaN epitaxially grown on Si(111) by MOCVD has been shown not only to be a viable method of obtaining high-quality epitaxial films, but the inherent benefits of using silicon as a substrate provides significant advantages for production of light emitting diodes and high frequency/high power transistors. To overcome the large lattice mismatch (17%) and huge difference in thermal expansion coefficient (54%) in obtaining high-quality crack-free layers, techniques proposed include the use of AlGaN graded buffer layers, superlattices, and AlN interlayers. AlGaN graded buffers have been adopted by many groups as an effective way for strain management and dislocation reduction. However, there has yet to be an in-depth study revealing the stress evolution and dislocation reduction mechanism within the AlGaN graded buffer layer. Here, we present a detailed study of step-graded AlGaN buffers leading to 2µm crack-free GaN with XRD symmetric rocking curve FWHM (0002) 475 arcsec, and skew-symmetric (10-11) 1050 arcsec. The samples were grown on Si(111) in a horizontal metalorganic chemical vapor deposition reactor. Trimethylgallium (TMGa), trimethylaluminium (TMAl), and ammonia (NH3) were used as the precursors for Ga, Al, and N, respectively. A 0.2 µm AlN buffer was deposited at 1150°C, followed by step-graded AlGaN graded layer with various grading profiles and thicknesses ranging from 0.4 µm to 1.2 µm. The samples were monitored by in-situ reflectance and curvature measurements, and analyzed by ex-situ high-resolution x-ray diffraction, TEM, Nomarski and SEM to probe surface morphology, stress evolution and defect reduction mechanisms in the AlGaN graded buffer layers. By the use of AlGaN layers, in-situ reflectance shows instant oscillations indicating a quasi-2D growth mode. Surface morphology was improved by the use of thin AlGaN layers, as correlated to film stresses measured by in-situ deflectance. It is shown that the ramp sequence during high temperature surface treatment for thermal removal of oxide and Al predeposition prior to deposition of HT-AlN buffer are critical for good crystallinity of subsequent layers. Mosaic tilt is characterized by x-ray rocking curve analysis on each of the AlGaN layers, showing defect evolution through the layers. With direct visualization using reciprocal space mapping of the asymmetric (10-15) and (11-24) diffractions, the stress relaxation can be directly observed, enabling the growth of an AlGaN buffer scheme reducing the tensile stress to support a high-quality 2 µm thick crack free GaN layer. The characteristics of LED and HEMT device structures grown on this template will be presented.

9:20 AM Student

II4, Compositionally-Graded Layers Composed of Tandem InGaAs InGaP Alloys and Pure GaAsSb Alloys to Engineer the InP Lattice Constant on GaAs Substrates: *Li Yang*[1]; Mayank Bulsara[1]; Kenneth Lee[1]; Eugene Fitzgerald[1]; [1]Massachusetts Institute of Technology

InP and semiconductor alloys lattice-matched to InP enable various state-of-the-art electronic and optical devices. Our research is motivated by the desire to integrate InP-based devices on Si substrates, specifically by engineering the lattice constant from Si to that of InP. This includes three major challenges: bridging the lattice constant of Si to that of Ge, accommodating the Ge/GaAs nonpolar/polar interface, and engineering the lattice constant from GaAs to that of InP. We focus primarily on the last challenge, establishing the InP lattice constant on (001) GaAs substrates with a 6° miscut. The specification of the 6° miscut is important because it provides step structures which eliminate antiphase disorder during the growth of GaAs on Ge. Two approaches for MOCVD-grown compositionally graded metamorphic buffers, which enable virtual InP lattice constant substrates on GaAs were investigated. The first approach consisted of tandem graded layers of InGaAs and InGaP with compositional grading of the In concentration. This tandem approach is necessary because phase separation in InGaAs alloys at XIn>0.30 leads to rough surface and high threading dislocation density (TDD). We first grew InGaAs graded buffers at 700 °C with targeted In concentration of XIn=0.30 on both on-axis (001) GaAs and (001) GaAs with 6° miscut. The graded InGaAs grown on on-axis (001) GaAs did not exhibit phase separation and gave a TDD of 1.9e6 cm-2 with a surface roughness of 7.5 nm. While InGaAs grown on 6° offcut GaAs exhibited serious phase separation, resulting in high TDD (~ 5e8 cm-2) and rough surface morphology (roughness ~ 26.1 nm). However, that phase separation in the InGaAs on 6° offcut GaAs can be suppressed if we lower the growth temperature from 700°C to 450°C at higher In concentration because of the lower surface diffusivities of In and Ga atoms at lower growth temperature. The suppression of phase separation, in turn, dramatically reduces the TDD to 1.4e6 cm-2 and the surface roughness to 7.5 nm for In0.30Ga0.70As graded buffer. Using the graded InGaP system at a growth temperature of 650°C to continually grade the lattice from In0.30Ga0.70As to InP allowed us to achieve InP on 6° offcut GaAs with a TDD of 7.9e6 cm-2 and a surface roughness of 30.0 nm. The second approach used GaAsSb alloys with compositional grading of the Sb concentration. Graded mixed-anion GaAsSb alloys grown at 575°C did not exhibit phase separation, resulting in high quality InP lattice constant films on GaAs. A GaAsSb alloy (grading rate ~ 1.06% strain/um) lattice-matched to InP on 6° offcut GaAs with TDD of 4.7e6 cm-2 and roughness of 7.4 nm was demonstrated. The TDD of the GaAsSb graded buffer can be further lowered to 2.7e6 cm-2 if a lower grading rate (0.64% strain/µm) is used.

9:40 AM

II5, Characterization of Standard and Ferromagnetic Schottky Barriers on GaP/GaP and GaP/Si Epi-Layers: *Chris Ratcliff*[1]; Tyler Grassman[1]; Andrew Carlin[1]; Mark Brenner[1]; Jonas Beardsley[1]; Jon Pelz[1]; Steven Ringel[1]; [1]Ohio State University

One of the fundamental goals of current spintronics-based research is the efficient and controllable injection of electrons with a particular spin alignment into Si. Although recent success has generated interest in the possibilities of advanced silicon devices[1], much of the physics involved with the spin injection process is not yet fully understood. To this end, gallium phosphide is well suited as it is the closest lattice matched III-V material to silicon (0.37% misfit) and has a large band gap relative to silicon. The GaP/Si system has been the subject of interest for decades due to its potential as a gateway to III-V/Si integration. Recent work on MBE grown GaP/Si has resulted in high quality crystalline thin films[2]. By use of this process, which includes Si homoepitaxy and migration enhanced epitaxy III-V nucleation, GaP films free of defects related to the heterovalent interface can be grown to the precise thicknesses required for spin injection (~1-10nm). Much work remains to be done, however, on the characterization of these thin heteroepitaxial GaP/Si films and the GaP/Si interface. In addition to the fairly uncharacterized GaP/Si system, there is also little known about the nature of metal/GaP Schottky contacts, which are necessary for metal/GaP/Si tunnel-barrier spin-injection. To this end, Au/GaP and Fe/GaP Schottky diodes were fabricated to facilitate the characterization of the resulting metal-semiconductor contacts. Current-voltage data shows similar, strong rectifying behavior for both metals, and internal photoemission (IPE) experiments reveal Schottky barriers for Au and Fe to be 1.15 and 1.14eV, respectively. The negligible difference in resultant barrier heights compared to the 0.6eV difference in work functions between the two metals indicates a Fermi level pinning mechanism for Schottky barrier formation on GaP. Therefore, because Fe, a ferromagnetic metal, makes a good Schottky barrier with GaP, and the fact that the epitaxial GaP can be grown to desired doping levels and thicknesses, the effective tunneling barrier can be tailored to promote efficient spin injection into silicon. In order to fully understand the efficacy of the Fe/GaP/Si system as a spin injection tunnel barrier, we must first characterize all of the materials and interfaces involved. To this end, work will continue on the characterization of metal/GaP Schottky barriers, which in turn enables the materials level characterization of the GaP epitaxial layers through the use of such as advanced techniques as deep level transient and optical spectroscopies. Additionally, we intend to probe and will report the effects of GaP/Si interfacial quality on the barrier heights and other properties of resultant metal/GaP/Si devices. [1]Dash et al., Nature, 462, 491-494 (2009); [2] Grassman et al., Appl. Phys. Lett. 94, 232106 (2009).

10:00 AM Break

10:20 AM

II6, Silicon Nanostructures Ion Implanted with Carbon and Nitrogen as an Electron Emitting Device: *Damian Carder*[1]; Andreas Markwitz[1]; John Kennedy[1]; [1]GNS Science

The search for cold cathode electron emitters with low-turn on field, high emission current density and high stability remains an active area of research. Silicon incorporating carbon and/or nitrogen is an attractive option for this purpose. This is due to the compatibility with silicon processing technologies and the expected enhanced properties of SiC(N). A cold cathode device from this material system should be more robust, partly due to the superior high temperature performance.Here we demonstrate electron emission from silicon-based nanostructures following ion implantation with carbon and nitrogen. Self-assembled silicon nanostructures were prepared on the surface of wafer silicon, to act as a template, prior to multiple low-energy ion implantations of carbon and nitrogen. Following ion implantation the original distinct surface structure was lost. However, it is shown that a two step electron beam annealing process successfully re-establishes the nanoscale self-assembled surface features. The composition of the ion implanted and annealed layers have been studied using nuclear reaction analysis (NRA) and Rutherford backscattering spectrometry (RBS) which indicate a $Si_{0.6}C_{0.1}N_{0.3}$ layer extending from the surface to a depth of 110 - 130 nm. Electron emission has been measured from the as-implanted and post-annealed samples. The as-implanted sample has a relatively high turn on field of 44 V/µm for a current density of 0.01 mA/cm^2. The implanted and annealed sample, however, shows a low turn on field of 10 V/µm for the same current density. This is comparable to other SiC-based nanostructure electron emission devices. The field emission characteristics demonstrate the promise and feasibility of this method for silicon-based cold cathode technologies.

10:40 AM

II7, High-Quality (211)B CdTe on (211) Si Substrates Using Metal-Organic Vapor-Phase Epitaxy: *Sunil Rao*[1]; Shashidhar Shintri[1]; Justin Markunas[2]; Randolph Jacobs[2]; Ishwara Bhat[1]; [1]Rensselaer Polytechnic Institute; [2]U. S. Army RDECOM CERDEC NVESD

(211)B CdTe is the preferred buffer layer for epitaxial growth of device quality (211)B $Hg_{1-x}Cd_xTe$ films on (211) Si substrates. Molecular beam epitaxy (MBE) has been used to obtain high quality (211)B CdTe films on (211)Si substrates. The 19% lattice-mismatch between CdTe and Si has limited the threading dislocation (TD) density in state-of-the-art MBE-grown material in the mid-10^5cm^{-2} to low-10^6cm^{-2} range. Higher growth temperatures (>400^{o}C) and techniques like epitaxial lateral overgrowth (ELO) used during metal-organic vapor-phase epitaxy (MOVPE) could help in further reducing the TD density. We have previously reported on the successful MOVPE growth of (211)B CdTe on Si substrates using Ge and ZnTe interfacial layers. A cyclic annealing procedure has been used to improve crystal quality during growth of 8µm – 10µm thick CdTe films. The cyclic annealing enhances threading dislocation motion and increases the probability of dislocation interaction and annihilation reactions. Everson etch pit density (EPD) is used to characterize the TD density in (211)B CdTe films. A reduction in Everson EPD was observed for CdTe films grown using the cyclic annealing procedure, EPD was 1x10^7cm^{-2} for a 5µm thick un-annealed film compared with 4x10^6cm^{-2} for a 5µm thick film grown using a cyclic annealing procedure. The lowest EPD observed in this study was 2x10^6cm^{-2} for an 8µm thick film. The good crystal quality of the grown films was also characterized by a low x-ray diffraction (XRD) (422) rocking-curve full-width–at-half-maximum (FWHM) of 85 arc-s. This FWHM value is superior to the previous best FWHM value of 140 arc-s reported for MOVPE grown (211)B CdTe/Si. One of the current challenges in our MOVPE process is the rough surface morphology of the grown CdTe films. The films display an orange-peel-like surface texture when observed using a Nomarski contrast optical microscope. In addition, polycrystalline lumps (density varying from 1x10^3cm^{-2} to 1x10^5cm^{-2}) are also observed on the surface. A modification in the growth temperature from 325^{o}C to 350^{o}C has enabled us to eliminate these polycrystalline lumps. Efforts are currently underway to optimize the other growth process parameters in order to improve the over-all surface morphology.

This work was partially supported by US Army STTR contract W911NF-07-C-0105 through Agiltron Inc. (Dr. Matthew Erdtmann) and US ARMY STTR contract W911NF-08-C-0071 through Brimrose Corporation. Many discussions with Dr. P. Wijewarnasuriya of ARL are also appreciated. We thank Dr. William Clark of ARO for all his encouragement.

11:00 AM Student

II8, Metalorganic Vapor Phase Epitaxial Growth of (211)CdTe on Nanopatterned (211)Ge/Si Substrates Using Full Wafer Block Copolymer Lithography: *Shashidhar Shintri*[1]; Sunil Rao[1]; Huafang Li[1]; Smita Jha[2]; C Liu[2]; Thomas Kuech[2]; Witold Palosz[3]; Sudhir Trivedi[3]; Fred Semendy[4]; Priyalal Wijewarnasuriya[4]; Yuanping Chen[4]; Ishwara Bhat[1]; [1]Rensselaer Polytechnic Institute; [2]University of Wisconsin-Madison; [3]Brimrose Corp. of America; [4]U.S. Army Research Laboratory

Heteroepitaxial growth of HgCdTe on Si substrates is being pursued for the fabrication of large format infrared focal plane arrays. Prior to the growth of HgCdTe, a buffer layer of CdTe is first grown on Si. Molecular beam epitaxy has been the method of choice for growing high quality (211)B oriented CdTe on (211)Si substrates. But the 19% lattice mismatch between CdTe and Si has limited the threading dislocation (TD) density in the state-of-the-art MBE grown material to the low 10^6cm^{-2} range. To reduce the TD density further, various techniques are being pursued such as patterned growth, lateral epitaxial overgrowth etc. In this work, we have investigated MOVPE growth of CdTe on nano-patterned Ge/(211)Si substrates. MOVPE of CdTe directly on Si is difficult due to the presence of Si native oxide. However, by growing a thin Ge layer on Si using germane gas, it has been shown that single crystal CdTe films can be grown on Ge/Si substrates. First, a film (~0.3µm) of Ge is grown on (211)Si, followed by the deposition of 25nm thick SiO_2 layer. A self-assembled block-copolymer (BCP) mask layer has been used to generate a hexagonal pattern of 20 nm holes on 40 nm centers in the 25 nm SiO_2 layer. CdTe is grown on this composite substrate using dimethylcadmium and diisopropyltelluride in a low pressure MOVPE system. Initial growth conditions have been established for selectively growing CdTe within these holes leading to a dense array of small, epitaxial CdTe islands, which has been verified by SEM. The growth of CdTe was carried at temperatures ranging from 325-420°C and pressures varying from 25-250 torr to get the best conditions for selective growth. TEM of a 2µm thick film grown on nano-patterned substrate shows two types of stacking faults generated near the interface, one originating from the Ge/CdTe interface along the <111> direction (F1) and the other originating from the oxide walls and propagating perpendicular to the substrate surface (F2). Blocking of defect motion at the walls of the oxide patterns shows promise for defect reduction in the epitaxial films. A comparison has been made with the epitaxial CdTe grown on blanket Ge/Si wafers, which shows the stacking faults extending into the CdTe layer without annihilation. Selective area electron diffraction (SAED) shows that CdTe grown on blanket Ge/Si wafer is off around 2° with respect to the substrate, where as no such misorientation is observed for the layers grown on nanopatterned substrates. Further growth and characterization results including XRD and AFM of the films will be discussed during the presentation. This work was partially supported by US Army STTR contract W911NF-08-C-0071 through Brimrose Corporation.

11:20 AM Student

II9, Effects of Ex-Situ Cycle Annealing on Dislocation Densities of HgCdTe/CdTe/Si Layers: *Stuart Farrell*[1]; Gregory Brill[2]; Yuamping Chen[2]; Priyalal Wijewarnasuriya[2]; Rao Mulpuri[1]; Nibir Dhar[3]; Karl Harris[4]; [1]George Mason University; [2]U.S. Army Research Laboratory, Sensors and Electronic Devices Directorate; [3]DARPA; [4]Penn State Electro-Optics Center

HgCdTe on Si is a desirable material system for producing large format infrared focal plane arrays. However molecular beam epitaxial (MBE) growth of HgCdTe/CdTe/Si results in layers with large dislocation densities, generally measuring between mid 10^6 cm^{-2} to low 10^7 cm^{-2}. This fact has been shown to result in poorer long-wavelength infrared focal plane array performance with respect to HgCdTe grown on bulk lattice matched CdZnTe substrates. We have developed a process of ex-situ cycle annealing which is capable of consistently reducing the dislocation density in a HgCdTe/Cd/Te/Si layer to ~1x10^6 cm^{-2}.

In this technique, the HgCdTe/CdTe/Si sample is placed face down on a clean piece of a silicon wafer along with ~ 0.5 mL of Hg in a sealed quartz ample, and subjected to multiple number of annealing cycles between the temperatures of 250 °C and 400 °C. The dislocation reduction has been shown quantitatively via etch pit density (EPD) measurements and supported qualitatively via the full width at half maximum (FWHM) measurement of x-ray rocking curves. The main parameter that has been linked to lower EPD is the number of annealing cycles the sample undergoes. An increase in the annealing temperature has been shown to have a minor secondary effect on the resulting dislocation density for temperatures beyond ~400 °C. Below this temperature, there is little to no change in dislocation density. Variations in cycle duration, total annealing time and as-grown dislocation density do not seem to play a major role in the post annealed measurements of the dislocation density with respect to un-annealed material. Excessive amount of Hg during annealing resulted in serious surface pitting, which is deleterious for device applications. For comparison, thermal cycle annealing also has been performed on HgCdTe layers grown on lattice matched CdZnTe substrates. Further properties and parameters of the annealing cycles, such as ramp rate and fine control of exact temperature profiles will be presented.

11:40 AM
II10, Late News

Session JJ: Nonpolar-Semipolar III-Ns

Friday AM
June 25, 2010

Room: 155
Location: University of Notre Dame

Session Chairs: Jae-Hyun Ryou, Georgia Institute of Technology; Christian Wetzel, Rensselaer Polytechnic Institute

8:20 AM Student
JJ1, Internal Quantum Efficiency of Polar and Non-Polar GaInN/GaN Multiple Quantum Wells: *Liang Zhao*[1]; Yufeng Li[1]; Theeradetch Detchprohm[1]; Christian Wetzel[1]; [1]Rensselaer Polytechnic Institute

The heteroepitaxial growth of GaInN/GaN quantum wells (QWs) on c-plane sapphire has long been the favored approach for high power green light emitting diodes (LEDs). However, the strong electric fields in the QWs have been considered a possible reason for the rapid drop of quantum efficiency as the injection current density increases above some 10 A/cm^2. Therefore, growth along non-polar axes, e.g., on a-plane and m-plane, carries a high promise for higher quantum efficiency at higher drive current densities. In this work, we have estimated the internal quantum efficiency (IQE) as a function of excitation power density for GaInN/GaN green MQW structures of both, polar (c-plane) and non-polar (a- and m-plane), growth orientation. We measured the photoluminescence (PL) intensity, both, as function of temperature and optical excitation density. Excitation was performed in resonance with the QWs at 405 nm in cw mode. Under the assumption of negligible non-radiative recombination at T = 4.2 K we obtained an upper estimate of IQE at room temperature. At room temperature (297 K), PL peak wavelengths are 550 nm (c-plane), 485 nm (m-plane), and 510 nm (a-plane). Under optical excitation, the highest IQE value at room temperature is found at about 50% in the c-plane sample at an excitation density of 0.8 kW/cm^2. With increasing excitation density, IQE drops quickly and reaches 33% at 280 kW/cm^2. For the non-polar material the highest IQE is found in the m-plane structure with 36%. The a-plane structure reaches 28%. Furthermore, in both non-polar cases, IQE is found to increase with excitation density, reach their respective maxima at around 2 kW/cm^2. Unlike the polar c-plane case, IQE in both non-polar orientations remains roughly unchanged for higher excitation densities up to the highest tested level of 280 kW/cm^2. At the highest excitation level, IQE values in the m-plane structure actually supersede those in the c-plane material. These results suggest that non-polar a- and m-plane structures show high promise to outperform polar c-plane structures in particular at high excitation levels, such as typically achieved under higher current injection. This work was supported by a DOE/NETL Solid-State Lighting Contract of Directed Research under DE-EE0000627. This work was also supported by the National Science Foundation (NSF) Smart Lighting Engineering Research Center (# EEC-0812056).

8:40 AM Student
JJ2, Optical Polarization of Non-Polar GaInN/GaN LEDs: *Shi You*[1]; Theeradetch Detchprohm[1]; Mingwei Zhu[1]; Wenting Hou[1]; Christian Wetzel[1]; [1]Rensselaer Polytechnic Institute

For GaInN/GaN quantum well (QW) growth along the polar c-axis, huge piezoelectric fields are induced across the QWs that lead to strong Stokes shift in light emission that varies with drive current. Those effects of the piezoelectric polarization can be reduced or avoided by growth along axes perpendicular to the c-axis, e.g. along the m- and a-axes. With the crystal c-axis lying within the QW plane, anisotropic strain is induced that lifts the degeneracy of the GaInN valence band states. The result is a high degree of linear polarization of the emitted light. Linearly polarized light emitters are ideally paired with polarizer transmission modulators such as liquid crystal displays. Suppressing the polarization state of light that cannot be transmitted by the modulators can significantly enhance display system's efficiency, where only linearly polarized light can be transmitted. In this study, we have investigated the optical polarization properties of GaInN/GaN based non-polar LEDs grown on bulk GaN substrate. The polarization ratio is defined as ρ = (I_max-I_min)/ (I_max+I_min) where I_max is the maximum and I_min is the minimum light intensity when measured through a rotated linear polarizer. From the electroluminescence measurement of a green m-plane GaInN/GaN based LED, linear polarization along the a-axis dominates with a single peak at 505 nm, while the polarization component along the c-axis shows a much weaker peak at 491 nm, and the polarization ratio is found to be ρ = 0.77. The polarization ratio of a series of m-plane and a-plane GaInN/GaN MQW samples with different peak emission wavelength is analyzed by room temperature photoluminenance measurement. The excitation laser is 325 nm HeCd laser at power density 10 mW/mm^2. M-plane GaInN/GaN structures reach a polarization ratio of 0.7 at 460 nm and this value grows to 0.9 at 515 nm peak wavelength. For a-plane structures we always find lower values of 0.53 at 400 nm and about 0.6 at 480 nm – 510 nm. The optical polarization performance of c-plane and m-plane LEDs is also compared. For the m-plane LEDs with polarization ratio as large as 0.8, deployment of such device should result in a 55% power saving over a combination of non-polarized c-plane LED with a polarizing filter. Such great advantage in optical polarization of m-plane GaN based LED predicts its future application as the polarized light emitter. This work was supported by DOE/NETL Solid-State Lighting Contract of Directed Research under DE-EE0000627. This work was also supported by the National Science Foundation (NSF) Smart Lighting Engineering Research Center (# EEC-0812056).

9:00 AM Student
JJ3, Anisotropic Carrier Mobility in GaN Quantum Well Grown in Non-Polar Direction: Polarization Induced Dipole and Interface Roughness Scattering: *Aniruddha Konar*[1]; Tian Fang[1]; Nan Sun[1]; Debdeep Jena[1]; [1]University of Notre Dame

GaN-heterojunction based high-electrom mobility transistors (HEMT) has paved the way towards high speed, high power electronics. Though the built-in polarization field in polar-GaN (grown along c axis) has been exploited to achieve dopant free HEMT, for optical devices polarization field plays a negative role due to quantum confined Stark effect. GaN grown in polar direction cannot be used in bipolar devices due to unavailability of hole doping. Moreover, polar GaN-based MOSFET is hard to pinch-off due to inherent presence of two dimensional electron gas (2DEG) at GaN surface. So the recent trend is to explore optical and transport properties of GaN grown in non-polar (m or a plane) direction. Though optical properties of non-polar GaN based devices have been studied quite extensively, transport properties of these devices have not been addressed so far. In this work, we have theoretically investigated charge transport in non-polar GaN quantum well (QW) structures. Let us consider a thin non-polar GaN QW of thickness a sandwiched between aluminum nitride (AlN) barrier as shown in fig. 1a). To consider charge transport in this structure,

we have figure out all sources of disorders present in the QW. One of the most important source of scattering mechanism for thin QW is interface roughness (IRF) as a result of improper growth conditions. GaN, grown along non-polar direction (m plane) shows parallel trench/stripe like patterns which extend infinitely perpendicular to c axis in the plane of GaN. Another new source of disorder in our structure is the polarization bound charges associated with each interface roughness. The difference of in-plane polarization of GaN and AlN induces bound charges at opposite faces of each roughness as shown in fig.1b). These bound charges can be modeled as infinite line charges (fig 1c)) and carrier can scatter from the potential originating from these line charges. We have also considered remote ionized impurity scattering and polar optical phonon scattering in our calculation. Among all the scattering mechanisms mentioned in the above section, interface roughness and polarization-induced line charge scattering are anisotropic (carrier does not feel any potential along the direction of roughness and line charges) but remote ionized impurity and polar-optical phonon scattering found to be isotropic in nature. Using Fermi golden rule and Boltzmann transport equation electron mobility has been calculated. Mobility also shows anisotropic behavior as shown in fig. 2. At room temperatures mobility anisotropy washes out due to strong isotropic polar-optical phonon scattering. In conclusion, we have investigated the charge transport in GaN QW grown in non-polar direction and predicted anisotropic nature of carrier mobility.

9:20 AM

JJ4, MBE Growth of Nitrogen-Face Aluminum Nitride by Polarity Inversion Using Magnesium Overdoping: *Craig Moe*[1]; Wendy Sarney[1]; Anand Sampath[1]; Michael Wraback[1]; [1]U.S. Army Research Laboratory

The growth of aluminum nitride is attracting a great deal of research interest as its wide bandgap and alloying with other III-nitrides make it highly desirable for deep ultraviolet emitters and photodetectors. While most conventional nitride semiconductor devices are grown along the [0001] direction, recent studies have indicated potential benefits of N-face material in both optoelectronic and electronic devices. In this work, we achieve N-face AlN through the overdoping of III-polar AlN with magnesium. Samples were grown by plasma-assisted molecular beam epitaxy on sapphire substrates. An initial buffer layer of Al-face material was deposited at a thickness of 440 nm. Following this, an inversion layer of AlN heavily doped with magnesium was grown at various thicknesses and Mg beam equivalent pressures. Samples were then capped with undoped AlN and silicon-doped GaN. Polarity inversion of the material was observed first through reflection high-energy electron diffraction (RHEED) analysis of the surface, looking for the 3 × 3 reconstruction indicative of N-face nitride material [1]. Polarity was then confirmed with the etching of the top GaN layer in an aqueous solution of KOH. Since KOH selectively etches the nitrogen but not the gallium face of GaN, this results in a roughened surface only when the material is N-face. The GaN cap layer was grown for just this purpose as both faces of AlN etch in KOH. For a Mg beam equivalent pressure of 3.5×10^{8} Torr and a substrate growth temperature of 900°C, samples with a Mg overdoped layer thickness up to 110 nm did not exhibit inverted polarity, while samples with a thickness of 180 nm and above did show polarity inversion. An intermediate thickness of 140 nm displayed a 3 × 3 reconstruction but did not etch in KOH, indicating only a partial inversion of AlN domains. Moreover, when the Mg BEP was dropped to 1.4×10^{8} Torr no polarity inversion was observed for the sample containing the 180 nm-thick Mg overdoped layer. From these measurements we were able to bound the Mg flux and thickness range of the Mg doped layer required for AlN inversion at this growth temperature, which is five to eight times thicker than the values of 25 to 40 nm reported in the literature for the inversion of GaN [2]. Further studies of the dependence of this phenomenon on growth temperature, Mg flux, and Mg doped layer thickness, along with TEM studies of the Mg doped layer, will be presented. [1]E. S. Hellman, MRS Internet J. Nitride Semicond. Res. 3, 11 (1998). [2]S. Pezzagna, P. Vennegues, A. D. Wieck, and J. Massies, Appl. Phys. Lett. 87, 062106 (2005).

9:40 AM

JJ5, Electro-Thermo-Mechanical Simulation of AlGaN/GaN HFETs and MOSHFETs: *Anusha Venkatachalam*[1]; William James[1]; Samuel Graham[1]; [1]Georgia Institute of Technology

AlGaN/GaN-based heterostructure field effect transistors (HFETs) are excellent candidates for high power and high frequency applications. However, current collapse and large gate leakage currents in these devices limit the output performance. Recently, gate insulation has shown to significantly reduce the leakage currents and enable device operation under high gate biases. Several oxides such as SiO_2, Al_2O_3, MgO and Sc_2O_3 have been used as gate insulators, giving rise to metal-oxide-semiconductor HFETs (MOSHFETs) with lower gate leakage currents. Additionally, owing to the complex nature of reliability failure in these devices, it is not clear what the operational stresses are, and it becomes imperative to assess the role of these stresses in long term reliability. In this paper, we focus on the electrical, thermal and mechanical modeling of GaN-based transistors under steady state and pulse mode conditions. Using a coupled electro-thermo-mechanical procedure, we compare self-heating effects and thermal stresses in HFETs and MOSHFETs under various operating conditions, and investigate the influence of device design parameters and boundary conditions on the thermal and mechanical properties. 2-D electrical simulations were performed using the Sentaurus Device simulator, while thermal and mechanical simulations were performed with COMSOL using a one-way coupling procedure. COMSOL was used to first solve the continuum heat transfer equation using the heat generation obtained from Sentaurus Device, and then the thermal expansion strain was determined, followed by the solution of the elasticity equation. Electrical simulations were carrier out near the active regions of the device, while the domain was extended for thermal and mechanical simulations to model realistic heat diffusion. The stress in the device was modeled in two dimensions as in-plane. The active region of the MOSHFET consisted of a 30 nm $Al_{0.2}Ga_{0.8}N$ barrier, a 0.45 µm GaN channel region and a 10 nm SiO_2 insulator layer under the gate. The gate was 2 µm long and 150 µm wide. The HFET comprised of a 25 nm $Al_{0.23}Ga_{0.77}N$ barrier, a 1.2 µm GaN layer with a gate length of 1 µm and gate width of 200 µm. In both cases, the substrate thickness was assumed to be 200 µm. Temperature dependent thermal conductivities were used for the materials in the device. Thermal boundary resistances, thermal effects of metallization, and residual stresses were ignored for simplification purposes. The electrical simulations under steady state indicated that at V_{gs}=0 V, the AlGaN/GaN MOSHFET structure exhibited about 40% increase in the saturated drain current due to the presence of oxide under the gate. Thermal and mechanical simulations showed that the peak temperature at 40 V drain bias was about 10% higher in MOSHFETs and consequently, the thermal stress was also higher under steady state, with the peaks occurring near the drain end of the gate contact.

10:00 AM Break

Session KK: Indium Nitride

Friday AM
June 25, 2010

Room: 155
Location: University of Notre Dame

Session Chairs: Thomas Myers, Texas State University; Steven Durbin, University of Canterbury

10:20 AM

KK1, Mg Doped InN and Search for P-Type InN: *Ke Wang*[1]; Ryosuke Iwamoto[1]; Tomohiro Yamaguchi[1]; Kazuaki Kagawa[1]; Tsutomu Araki[1]; Yasushi Nanishi[1]; Nate Miller[2]; Marie Mayer[2]; Joel W Ager[2]; Kin Man Yu[2]; Wladek Walukiewicz[2]; [1]Ritsumeikan University; [2]Lawrence Berkeley National Laboratory

Recently Mg-doped InN epilayers have attracted much interest to achieve p-type InN in order to exploit its potential device applications. In this work, several series of Mg-doped InN layers were grown by radio frequency plasma assisted

molecular beam epitaxy (RF-MBE) and characterized by various techniques. Mg-doped InN layers were grown at 450°C on GaN/sapphire templates. Mg doping concentration is controlled by Mg cell temperature varying from 150 to 250°C. Secondary ion mass spectrometry (SIMS) measurements have shown Mg concentration increases from $2x10^{18}$ to $5x10^{20}cm^{-3}$ in this temperature range. Influence of undoped InN buffer layers from 0~60nm on Mg doping under same growth conditions has been studied as well. Electrolyte capacitance-voltage (ECV) results have demonstrated net acceptors for InN with Mg concentration from $2x10^{19}$ to $1x10^{20}cm^{-3}$. When applied bias across the interface between electrolyte and InN:Mg is high enough, the surface accumulated electrons can be depleted and thus a depletion layer on the InN side can form with further bias. As a consequence, in C^{-2} vs voltage profiles, a maximum peak can be observed. The peak position for InN with net acceptors shifts from usual n-type InN (net donors in depletion). This shift is due to different band bending and Fermi level position between n- and p-type. The C^{-2} peak shift of p-type InN from n-type is about 0.3~0.6 V, which depends on the Mg doping levels and growth conditions. The slope in depletion condition indicates net acceptor concentration from $7.2x10^{18}$ to $6.0x10^{19}cm^{-3}$. We have noticed the values can vary slightly with measuring frequency but a trend following Mg doping levels is kept. Thermopower measurements have demonstrated positive Seebeck coefficients for some samples at room temperature, confirming existence of free holes. For some samples, although ECV results have demonstrated net acceptors, the Seebeck coefficients are negative but quite close to zero. In fact, our results on a set of InN:Mg samples varying only the thickness of undoped InN buffer layers (n-type) have revealed their significant contribution to the measured Seebeck coefficients. The Seebeck coefficients dramatically changed their signs from -13 to 250μV/K when the thickness of buffer layers decreases from 60 to 0 nm, keeping all other growth conditions exactly the same. The net acceptor concentration estimated from ECV measurements is very close, from 6.0 to $3.3x10^{19}cm^{-3}$ for these samples. Therefore, the dramatic change of Seebeck coefficients is exclusively attributed to the n-type InN buffer layers. Strong PL has been observed for InN with low Mg doping levels. PL spectra clearly demonstrate two peaks: at 0.678eV due to InN band-to-band transition, and at 0.606eV, which is attributed to conduction band to acceptor level transition. Therefore, the acceptor energy level is determined to be 72meV above valence band minimum.

10:40 AM Student

KK2, Dislocation Reduction via Epitaxial Lateral Overgrowth of InN by Selective-Area-Growth of RF-MBE: *Jumpei Kamimura*[1]; Katsumi Kishino[1]; Akihiko Kikuchi[1]; [1]Sophia University

InN has potentialities for optical device applications because of its narrow bandgap of 0.6-0.8 eV. However, there is a difficulty in obtaining a high crystalline quality InN due to the low dissociation temperature and lack of lattice-matched substrates. In general, sapphire is used as a substrate for the growth of InN. So far various buffer layer techniques and an increased film thickness up to 10 μm have been employed, which were valid to some extent, but inefficient in decreasing the dislocation density below 10^9 cm^{-2}. Meanwhile, selective-area growth (SAG) provided epitaxial lateral overgrowth (ELO); it is a dramatically-effective method for reduction of threading dislocation of GaN, as well developed with HVPE and MOVPE. Contrarily, SAG of InN has not been well developed yet. The SAG by MOVPE of InN was tried on GaN template using SiO2 masks, following the conventional SAG of GaN. For preventing crystal deposition on SiO2 masks, a high temperature growth was necessary, but which induced decomposition of InN. Recently, by use of Molybdenum mask, Denker et al. reported SAG of InN at low temperature by rf-MBE. In this study, the SAG of InN was beautifully obtained, by which the first achievement of ELO in InN crystals was demonstrated. Prior to the growth, a thin Mo film was deposited on c-plane sapphire substrate by electron beam evaporation. Subsequently we prepared Mo-mask patterns through electron beam lithography and dry etching, in which hexagonally shaped holes with diameter of 433 nm were arranged in triangular lattice of lattice constant of 1000 nm. After initial nitridation of the substrate surface at 550°C, InN was grown at 510-580°C for 1-60 min. by rf-MBE, producing InN micro-crystals. The grown InN micro-crystals were evaluated with SEM, TEM and micro-PL spectroscopy. The growth of the InN micro-crystals proceeded as follows; the nucleation occurred firstly inside the holes opened in the Mo-mask and then hexagonal nano-disks were formed at 5 min. and then InN grew laterally and vertically. At 60 min., hexagonal geometry columnar InN micro-crystal arrays in closed packing scheme were prepared. The height and diameter were approximately 1.5 μm and 1.0 μm, respectively. TEM observation confirmed that a large number of threading dislocations (10^9-10^{10} cm^{-2}) arose at InN/sapphire interface and propagated in the center area of the InN micro-crystals along the crystal c-axis, while laterally overgrown side areas were nearly dislocation-free. The micro-PL spectrum at room temperature showed the PL-FWHM of 54 meV at the peak energy of 0.63eV, indicating a high quality of the InN. Acknowledgment: This study was partly supported by Grants-in-Aid for Scientific Research on Priority Areas No.18069010, and (B) No.18310079 from the MEXT, Japan.

11:00 AM

KK3, Growth Orientation Control of InN by Pulsed Excitation Deposition: *Hiroshi Fujioka*[1]; Tomoaki Fujii[2]; Atsushi Kobayashi[2]; Jitsuo Ohta[2]; Masaharu Oshima[1]; [1]The University of Tokyo, JST-CREST; [2]The University of Tokyo

We have succeeded in grown orientation control of InN by the use of YSZ substrates with various surface orientations and pulsed excitation deposition (PXD). Growth of nitride semiconductors with nonpolar and sempolar planes has attracted much attention because they can reduce the undesirable effects of the built-in fields. We have recently found that hexagonal InN grows epitaxially on YSZ substrates with various orientations while keeping the epitaxial relationship of YSZ(111)//InN(0001) and InN[11-20]//YSZ[1-10]. With this notion, we prepared YSZ substrates with various orientations to obtain InN(1-10m) and InN(11-2n) with various indices, m and n. We confirmed the growth of InN(1-105), InN(1-103), InN(2-205), InN(1-101) on YSZ(112), YSZ(113), YSZ(110), and YSZ(100), respectively. We have also confirmed the growth of InN(11-27), InN(11-26), and InN(11-24) on the YSZ substrates with the (111) plane inclined toward the YSZ[1-10] direction by 23.8°, 28.3°, and 38.9° from the sample normal. These results indicate that epitaxial relationship of InN[0001]// YSZ[111] and InN[11-20]//YSZ[1-10] is quite universal for this InN/YSZ system probably because the arrangement of atoms on the YSZ(111) plane is quite similar to that for InN(1000) and the lattice mismatch between YSZ(111) and InN(0001) is as small as 2.7%. Since we succeeded in choosing growth direction of semipolar InN at will, we have investigated the growth direction dependence of the surface morphology of semipolar InN using AFM. We have found that the growth directions with the low Miller indices lead to smooth surfaces. This fact indicates that the precise control of the surface direction of the YSZ substrates is inherently important for devices that utilize hetero-interfaces. We have also tried to grow the semipolar-AlN/InN hetero-structure which can be used for the fabrication of devices such as future InN based FETs. Although the growth of AlN on the semipolar InN films at conventional growth temperatures for AlN caused serious intermixing reactions between AlN and InN, the use of the PXD low temperature growth technique leads to formation of an atomically abrupt semipolar-AlN/InN heterointerface. In summary, we have found that we can control growth orientation of semipolar InN and fabricate the semipolar-AlN/InN heterostructure by the use of PXD and YSZ substrates with various orientations.

11:20 AM Student

KK4, Optical and Electrical Transport Properties of Nearly Intrinsic and Si-Doped InN Nanowires: *Yi-Lu Chang*[1]; Feng Li[1]; Jiale Wang[1]; Hieu Nguyen[1]; Zetian Mi[1]; [1]McGill University

InN nanowires have emerged as a promising candidate for a range of nanoelectronic and nanophotonic devices, due to its low direct bandgap, high electron mobility, and large saturation velocity. However, conventional InN nanowires exhibit tapered morphology and extremely large inhomogeneity. Consequently, a thorough understanding of their fundamental optical and electrical transport properties has not been possible, which severely limit their device applications. In this context, we have performed a detailed investigation of the molecular beam epitaxial (MBE) growth and characterization of non-tapered, nearly homogeneous InN nanowires, which exhibit a very narrow photoluminescence (PL) linewidth of ~ 10 meV, compared to the commonly

reported values of ~ 50 - 100 meV. It is further observed that both the optical and electrical transport properties of InN nanowires depend strongly on the Si-doping concentrations. In this experiment, InN nanowires were grown on Si(111) substrates using MBE. Prior to the growth initiation, a thin (~ 0.5 nm) In seeding layer was first deposited on the Si substrate, which can promote the formation and nucleation of InN nanowires. Both non-doped and Si-doped InN nanowires, with Si concentrations in the range of ~ 1×1017 – 1×1019 cm-3, were grown and characterized. The resulting InN nanowires exhibit non-tapered morphology and are nearly free of dislocations. The optical properties of InN nanowires were studied using temperature variable PL spectroscopy. We measured a record narrow spectral linewidth of < 10 meV at 5 K. With the increase of excitation power, there is a considerable blue shift in the peak energy and a drastic increase in the spectral linewidth. Such a strong band-filling effect and the absence of Burstein-Moss shift has not been previously observed, suggesting the achievement of nearly intrinsic InN nanowires. We have also measured the electrical transport properties of single InN:Si nanowires, which exhibit a resistivity of ~ 0.002 O cm. The temperature-dependent optical and electrical transport properties of such InN nanowires, as well as their dependence on Si doping concentrations are being investigated. These results, in conjunction with the achievement of single InN nanowire lasers will be presented.

11:40 AM Student

KK5, Growth Optimization of Si_3N_4 on GaN by Metal-Organic Chemical Vapor Deposition: *Brian Swenson*[1]; Ramya Yeluri[1]; Umesh Mishra[1]; [1]University of California at Santa Barbara

Si_3N_4 is commonly used in the Gallium-Nitride system (GaN, AlGaN) as both a gate insulator and as a passivation layer. Interface states exist at the interface between Si_3N_4 and GaN due to defects, dislocations and vacancies [J. Elec. Mat., Vol. 36, No. 9 (2007)] to name a few. In order to improve device performance and reliability, the growth of Si_3N_4 on GaN must be optimized to reduce the creation of interface states. The Photo-Assisted Capacitance-Voltage measurement [Swenson et al. J. Appl. Phys. 106, 064902 (2009)] was used to determine the interface state density. The growth temperature was varied from 800C to 1220C to find an optimum temperature that minimizes the generation of interface states. The optimal growth temperature was found to be at or above 1165C; the growth temperature of GaN. Temperatures above the GaN growth temperature also yielded optimal results (up to 1220C). The interface state density ranged by almost an order of magnitude from 1.15e13 cm^{-2} eV^{-1} at 800C to 2.1e12 cm^{-2} eV^{-1} at 1220C.

Index

K

L

M

S

T

U

V

W

X

Y

Z

CONFERENCE NOTES

CONFERENCE NOTES

CONFERENCE NOTES

TMS

Your Professional Partner for Career Advancement

EXPANDING YOUR HORIZONS

Get involved with the **Electronic, Magnetic, & Photonic Materials Division (EMPMD**) of TMS! Members actively promote technical exchange and assist in professional development through programming, publications, continuing education, mentorship, and professional recognition. **EMPMD** addresses the synthesis and processing, structure, properties, and performance of electronic, photonic, magnetic and superconducting materials, as well as the materials used in packaging and interconnecting such materials in device structures. **EMPMD** consists of 10 committees, including the Electronic Materials Committee, which sponsored this conference.

To become a member of TMS, apply online at **www.tms.org/Society/membership.html.**

ABOUT TMS

The Minerals, Metals & Materials Society (TMS) is a professional organization that encompasses the entire range of materials and engineering, from minerals processing and primary metals production to basic research and the advanced applications of materials. If at any time before, during or after the event you would like to offer suggestions or comments, your input is always welcome.

TMS EMPMD Electronic, Magnetic & Photonic Materials Division

www.tms.org

BE MATERIALS MINDED

TMS is committed to environmental responsibility as we fulfill our mission to promote global science and engineering by going green at our headquarters, conferences and through membership communication.

Be materials-minded. *Join* TMS *in reducing, reusing and recycling.*

PROGRAM GRID

Room	Wednesday		Thursday		Friday
	AM	PM	AM	PM	AM
McKenna Hall		**REGISTRATION on First Level:** Tuesday: 3:00-5:00 PM Wednesday: 7:30 AM-5:00 PM Thursday: 7:30 AM-4:00 PM Friday: 7:30-10:00 AM		**EXHIBITION:** Wednesday: 9:30 AM-1:30 PM; 3:00-4:00 PM; 6:00-8:00 PM Thursday: 10:00 AM-1:30 PM; 3:00-4:00 PM	
Jordan Auditorium	EMC Plenary Lecture / Student Awards				
102	Session A: High-K Gate Dielectrics	Session G: Oxide Semiconductor Thin Film Transistors	Session M: Graphene - Materials and Characterization	Session U: Graphene and Nanotubes - Devices	Session DD: Oxide Semiconductor Heterojunction Diodes
126	Session B: Non-Destructive Characterization	Session H: Materials and Devices for Flexible Electronics	Session N: Molecular Electronics and Chem / Bio Sensors	Session V: Quantum Dots, Boxes, and Wires	Session EE: Epitaxy Materials and Devices
129	Session C: Nanoscale Characterization	Session I: Nanomagnetic and Spintronic Materials	Session O: SiC: Characterization and Growth	Session W: Semiconducting and Metallic Nanowires	Session FF: Si and Ge Nanowires
131	Session D: Narrow Bandgap Semiconductor Bulk Materials and Devices	Session J: Thin Film Photovoltaics	Session P: One-Dimensional Photovoltaics	Session X: Narrow Bandgap Semiconductors: Infared Detectors and Lasers	Session GG: Thermoelectrics and Thermionics
138	Session E: Materials Integration: Wafer Bonding	Session K: III-Nitride Nanowires	Session Q: Oxide Thin Films	Session Y: III-N Nanostructures Session Z: Point and Extended Defects and Doping in Wide Bandgap Materials	Session HH: Semiconductor Processing, Surfaces and Contacts
141			Session R: ZnO Growth and Doping	Session AA: Oxide Defects, Localized States, and Nanostructures	Session II: Heteroepitaxy on Silicon
155	Session F: Silicon Carbide Devices	Session L: III-N HEMTs I	Session S: Light Emitting Diodes and Laser Diodes Session T: AlGaN Growth and Devices	Session BB: III-V Novel Electronic Devices Session CC: III-N HEMTs II	Session JJ: Nonpolar-Semipolar III-Ns Session KK: Indium Nitride